AIC8800D80I

Preliminary Low-Energy WiFi6/BTDM5.4 SoC
Data Sheet.

AIC Semiconductor (Shanghai) CO., Ltd.
March 5, 2025

Author: AICSEMI
version 1.0.2
www.aicsemi.com

Contents

1 General Description

AIC8800D80I is a 22nm, highly integrated SoC with dual band WiFi6, BTDM 5.4 and high performance Wlan CPU for wireless application. It provides miniaturized solutions that reduce design costs with minimal material.

1.1 WiFi Features

- CMOS single-chip fully-integrated RF, Modem and MAC
- One-chip power amplifier/low-noise amplifier for both bands
- Supports IEEE 802.11a/b/g/n/ac/ax specifications with single stream transmission and reception
- Supports 2.4GHz/5GHz band, the 5G band includes U-NII-1 U-NII-2A U-NII-2C and U-NII-3
- Supports MCS0–MCS11 in 20/40/80 MHz channels in both uplink and downlink direction with maximum 600.4 Mbps data rate
- In addition to the regular bandwidth, 5MHz/10MHz is also supported
- RX sensitivity -99dBm in 11b 1M mode
- Tx power up to 23dBm in 11b mode, 18dBm in HT/VHT/HE MCS7 mode
- Supports LDPC in Tx and Rx for all modes for performance improvement
- Supports space-time block coding (STBC) reception for all modes
- Supports beamforming as beamformee for 802.11ac and 802.11ax mode with explicit compressed feedback
- Supports short GI mode in TX and RX for HT
- Supports MU-MIMO operation as reception for 802.11ac and 802.11ax mode
- Supports OFDMA for efficient resource utilization in both Tx and Rx direction in 802.11ax mode
- Supports Wi-Fi6 TWT
- Supports DCM, Extended Range, partial bandwidth (106 tone) mode for coverage enhancement in 802.11ax mode
- Supports midamble based channel estimation for time-various channel in 802.11ax mode
- Algorithms to improve performance in presence of Bluetooth and blocking interference
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities for both Tx and Rx
- Available per-packet channel quality and signal strength measurements
- Supports STA, AP, Wi-Fi Direct modes concurrently
- Supports WEP/WPA/WPA2/WPA3-SAE Personal, MFP
- Supports IEEE 802.11d/w/k/r/v/e/h/i

1.2 BTDM5.4 Features

- Complies with Bluetooth Core Specification Version 5.4 with provisions for supporting future specifications
- Supports all the mandatory and optional features of Bluetooth low energy 5.4
- Supports advanced master and slave topologies
- Supports BR/EDR/BLE (1/2Mbps/LongRange S2/8)
- Bluetooth Class 1 Class 2 or Class3 transmitter operation
- Bluetooth Low Energy Class 1 Class 1.5 Class 2 or Class3 transmitter operation
- Supports BLE audio
- Host controller interface (HCI) using a high-speed UART interface
- PCM for audio data
- Adaptive frequency hopping (AFH) for reducing radio frequency interference

1.3 Other Features

- Supports SDIO3.0/USB2.0/HCI_UART/PCM interface
- Integrated low power timer and watchdog
- 1024 bits Efuse

1.4 Packaging Information

- Compact profile package 5mm×5mm×0.75mm QFN48

1.5 Application

- IOT device
- Wireless device

2 Platform Description

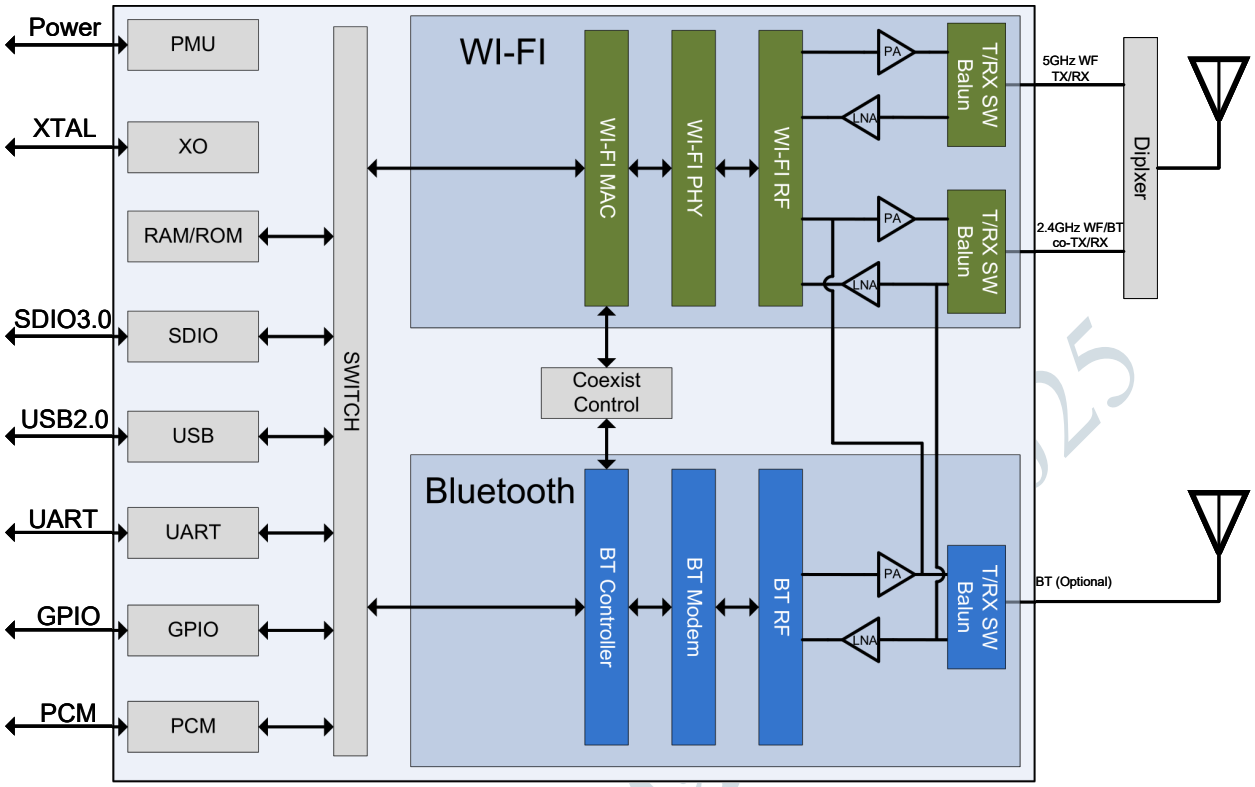


Figure 1: AIC8800D80I Block Diagram

3 Pins Description

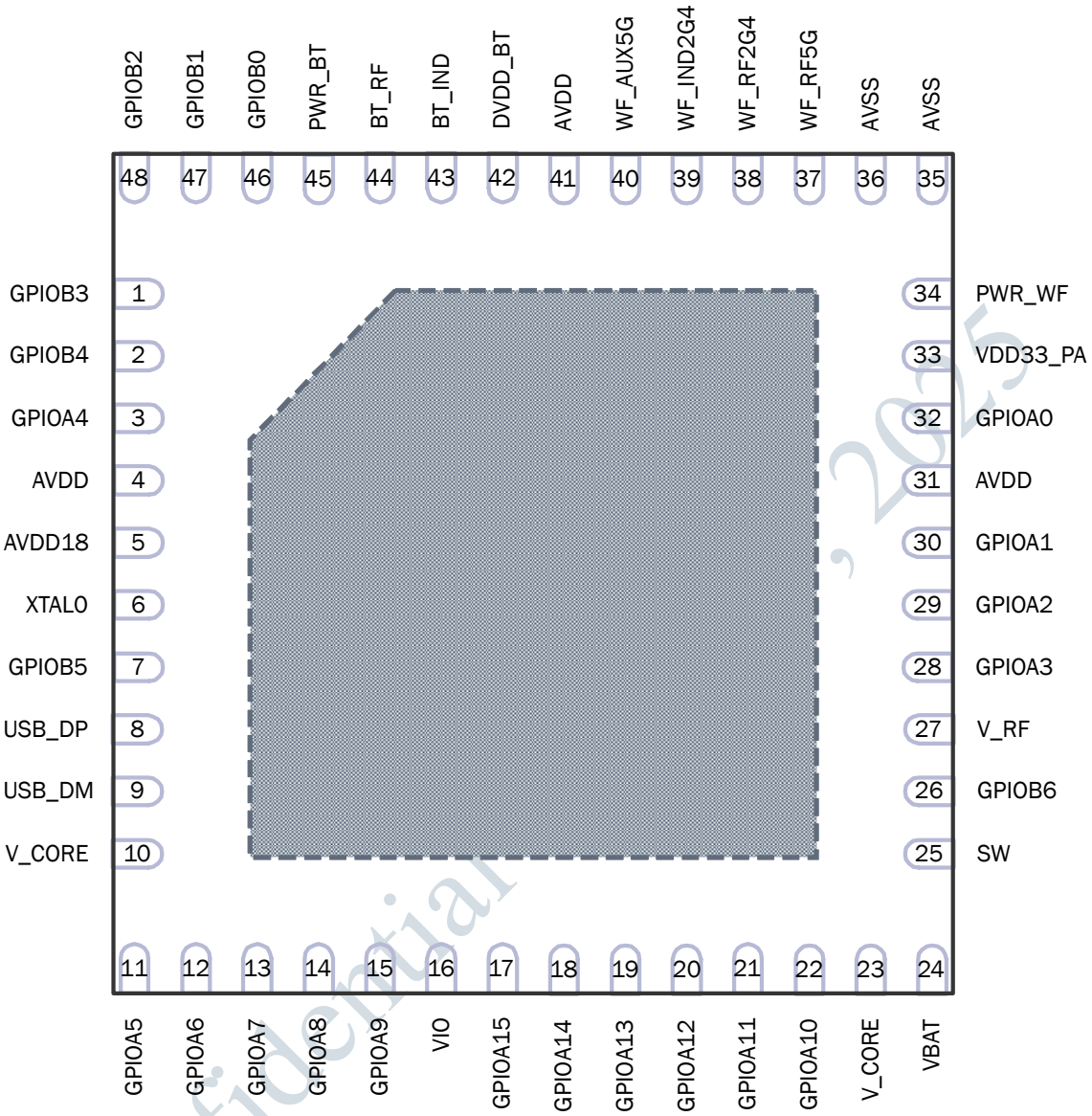


Figure 2: AIC8800D80I Pin Map

Table 1: AIC8800D80I Pin Description

Pin Name	QFN NO.	I/O	Description
RF			
WF_RF2G4	38	I/O	WiFi 2.4G RF
WF_IND2G4	39		WiFi 2.4G RF Ground, connect a 1.4nH inductor to ground
WF_RF5G	37	I/O	WiFi 5G RF
WF_AUX5G	40	I	WiFi 5G RX Aux
BT_RF	44	I/O	BT RF
BT_IND	43		BT RF Ground, connect a 1.4nH inductor to ground
AVSS	35		Connect to the ground
AVSS	36		Connect to the ground
PMU			

Table 1: AIC8800D80I Pin Description

Pin Name	QFN NO.	I/O	Description
AVDD	4		Need 1uF decoupling capacitor
AVDD	31		Need 1uF decoupling capacitor
AVDD	41		Need 1uF decoupling capacitor
AVDD18	5		Power output 1.8v, internal Efuse supply voltage, connect a 1uF decoupling capacitor
V_CORE	10		Need 1uF decoupling capacitor, connect to pin23
V_CORE	23		Digital Supply Voltage
VIO	16	I	IO Power Supply, Support 1.8v/3.3v
VBAT	24	I	System power supply
SW	25	O	Power Output For V_RF
V_RF	27	I	RF Supply Voltage
VDD33_PA	33	I	PA Supply Voltage
PWR_WF	34	I	WiFi system enable
PWR_BT	45	I	BT system enable
DVDD_BT	42		Need 1uF decoupling capacitor
CLK			
XTAL0	6	I	40M Crystal In
GPIO			
GPIOA0	32	I/O	GPIO
GPIOA1	30	I/O	GPIO
GPIOA2	29	I/O	GPIO
GPIOA3	28	I/O	GPIO
GPIOA4	3	I/O	GPIO
GPIOA5	11	I/O	GPIO
GPIOA6	12	I/O	GPIO
GPIOA7	13	I/O	GPIO
GPIOA8	14	I/O	GPIO
GPIOA9	15	I/O	GPIO
GPIOA10	22	I/O	GPIO
GPIOA11	21	I/O	GPIO
GPIOA12	20	I/O	GPIO
GPIOA13	19	I/O	GPIO
GPIOA14	18	I/O	GPIO
GPIOA15	17	I/O	GPIO
GPIOB0	46	I/O	GPIO
GPIOB1	47	I/O	GPIO
GPIOB2	48	I/O	GPIO
GPIOB3	1	I/O	GPIO
GPIOB4	2	I/O	GPIO
GPIOB5	7	I/O	GPIO
GPIOB6	26	I/O	GPIO
USB_DP	8	I/O	USB
USB_DM	9	I/O	USB

4 Electrical Characteristics

4.1 DC Electrical Specification

Table 2: DC Electrical Specification

Symbol	Description	MIN	TYP	MAX	Unit
VBAT	Supply Voltage for System	3.0	3.3	3.6	V
V_RF	Supply Voltage for V_RF	1.26	1.4	1.54	V
V_CORE	Internal power supply for V_CORE	0.6	0.9	1.0	V
VDD33_PA	Supply Voltage for PA	3.0	3.3	3.6	V
AVDD18	Internal power supply for Efuse	1.8	2.0	2.2	V
DVDD_BT	Internal power supply for BT RF	0.8	1.05	1.4	V
AVDD	Connected with V_RF inside the chip	1.26	1.4	1.54	V
VIO	Supply Voltage for VIO, VIO=1.8V	1.71	1.8	1.89	V
	Supply Voltage for VIO, VIO=3.3V	3.135	3.3	3.465	V

4.2 Absolute Maximum Ratings

The absolute maximum ratings in Table 4 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 3: Environmental rating

Rating	Symbol	Value	Uint
DC supply for the VBAT	VBAT	-0.5 to +3.9	V
DC supply for the PA	AVDD33_PA	-0.5 to +3.9	V
DC supply for the GPIO	VIO	-0.5 to +3.9	V

4.3 Environmental ratings

Table 4: Environmental rating

Symbol	Description	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	-40	27	85	℃
T_{store}	Store Temperature	-55		125	℃
Relative Humidity	Operation			85	%
	Storage			60	%

Note: if ambient temperature requires -40∼85℃, additional tests are needed to ensure system stability.

5 Power Management Unit

5.1 Description

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the AIC8800D80I. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

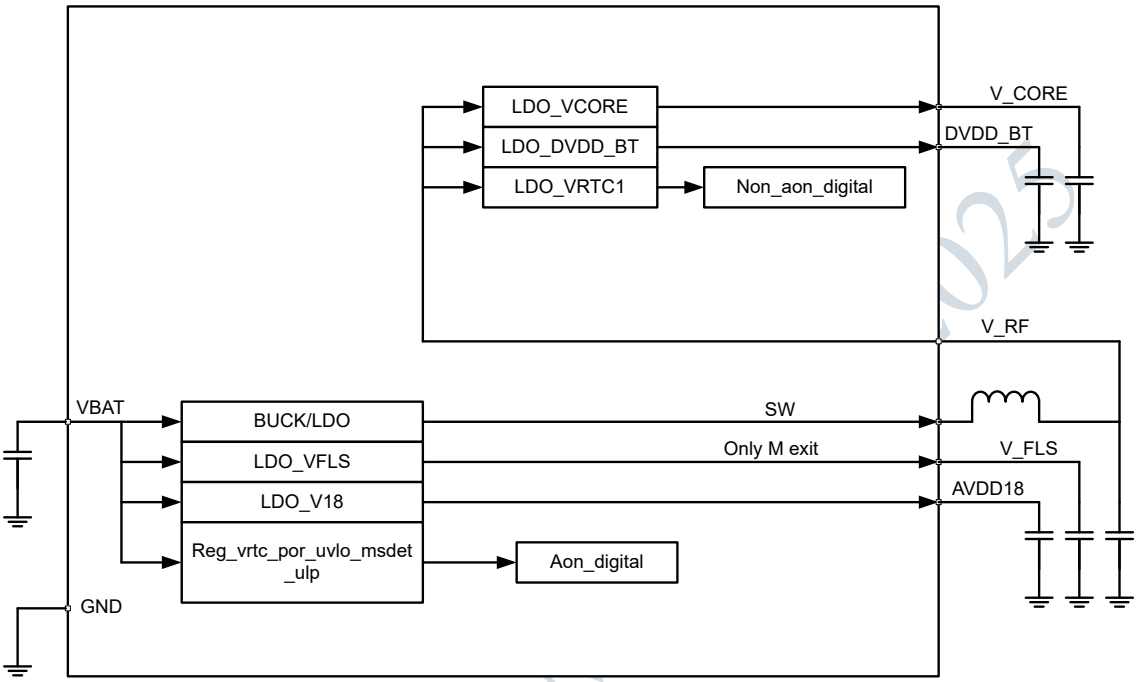


Figure 3: AIC8800D80I PMU Diagram

5.2 PMU Features

- VBAT to 1.4Vout (500 mA maximum) V_RF Buck switching regulator or LDO
- VBAT to 1.8Vout (100 mA maximum) AVDD18
- 1.4V to 0.9Vout (300 mA maximum) V_CORE
- 1.4V to 0.9Vout (100 mA maximum) DVDD_BT
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto calibration by the crystal clock for precise wake up timing from low power modes

5.3 V_RF Buck Switching Regulator

Table 5: V_RF Buck Switching Regulator Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage	Min value is Limited BY UVLO	3.0	3.3	3.6	V
PWM mode switching frequency	-		1.8		MHz
PWM output current	-	-	-	500	mA
Output voltage range	Programmable, 25 mV steps. Default=1.4V	-	1.4	-	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM. Before trimming	-10	-	10	%
PWM ripple voltage, static	Measure with 20MHz bandwidth limit. Static Load. VBAT=3.3V, Vout=1.4V, Fsw=1.8MHz, 4.7uH inductor L>2uH effective, Cap+Board total-ESR<20 mΩ, Cout=4.7uF, Cout ESL<200pH	-	4.5	20	mV
PWM mode peak efficiency	Peak Efficiency at 200mA load Fsw=1.8MHz PWM, L>3uH effective inductor Tmax=1mm, 0805 inch Inductor DCR=275mΩ	-	85	-	%
LP-PFM mode efficiency	Efficiency at 0.4mA load PFM L=4.7uH effective inductor Tmax=1mm, 0805 inch inductor DCR=275mΩ	-	80	-	%
Start up time from power down	VBAT=3.3V always on. Time from PWR_WF rising edge to RFBUCK/LDO reaching 1.4V	-	1.85	-	ms
External inductor	0806 inch size, 4.7uH, DCR<300mΩ, Isat>250mA	-	4.7	-	uH
External output capacitor	Ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V	-	4.7	-	uF
External input capacitor	For VBAT pin, ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V	-	4.7	-	uF

5.4 AVDD18

Table 6: AVDD18 Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, Vin	Min value is Limited BY UVLO	3.0	3.3	3.6	V
Output current	-	-	-	100	mA
Output voltage range, Vo	Programmable in 0.1V steps. Default=2V	-	2	-	V
Dropout voltage	At max. load	-	-	200	mV
Output voltage DC accuracy	Includes line/load regulation, before trimming	-10	-	10	%
Quiescent current	No load	-	15	-	uA
	Max load at 100 mA	-	1.1	-	mA
Line regulation	Vin from 2.7V to 3.6V, max load	-	-	3.5	mV/V
Load regulation	Load from 1mA to 100mA, Vin=3.3V	-	-	0.3	mV/mA
PSRR	Vin=3.3V, Vo=2.0V, Co=1uF, Max load, 100Hz to 100kHz	20	-	-	dB
LDO turn on time	Reference ready. Vo from 0 to 2.0V, Co=1uF	-	30	-	us
Output over current limit	-	120	-	-	mA
External output capacitor, Co	Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V	0.1	1	2.2	uF
External input capacitor	For VBAT pin, ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V	-	4.7	-	uF

5.5 V_CORE

Table 7: V_CORE Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, Vin	Min=Vo+0.25V=1.15V dropout voltage requirement must be met under maximum load for performance specifications	1.15	1.4	1.6	V
Output current	-	0.1	-	300	mA
Output voltage range, Vo	Programmable in 18mV steps. Default=0.9V	0.6	0.9	1	V
Dropout voltage	At max load	-	-	250	mV
Output voltage DC accuracy	Includes line/load regulation, before trimming	-10	-	10	%
Quiescent current	No load	-	18	-	uA
	300mA load	-	2	-	mA
Line regulation	Vin from 1.15V to 1.6V, max load	-	-	16	mV/V
Load regulation	Load from 1mA to 300mA, Vin=1.4V	-	-	0.03	mV/mA
Leakage current	Power down, Vin=1.4V, typical at Tj=25°C	-	0.9	-	uA
	Power down, Vin=0.9V, typical at Tj=25°C	-	0.3	-	uA
PSRR	100Hz to 100kHz, Vin≥1.2V, Co=1uF	20	-	-	dB
LDO turn on time	Reference ready. Vo from 0 to 0.9V, Co=1uF	-	13	-	us
External output capacitor, Co	Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V	0.1	1	2.2	uF
External input capacitor	Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V	1	-	-	uF

5.6 DVDD_BT

Table 8: DVDD_BT Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, Vin	Min=Vo+0.25V=1.3V dropout voltage requirement must be met under maximum load for performance specifications	1.3	1.4	1.6	V
Output current	-	0.1	-	100	mA
Output voltage range, Vo	Default=1.05V	0.8	1.05	1.4	V
Dropout voltage	At max load	-	-	200	mV
Output voltage DC accuracy	Includes line/load regulation, before trimming	-10	-	10	%
Quiescent current	No load	-	30	-	uA
	Max load at 100mA	-	1.1	-	mA
Line regulation	Vin from 1.3V to 1.6V, max load	-	-	3.5	mV/V
Load regulation	Load from 1mA to 100mA, Vin=1.4V	-	-	0.3	mV/mA
PSRR	Vin=1.4V, Vo=1.05V, Co=1uF, Max load, 100Hz to 100kHz	20	-	-	dB
LDO turn on time	Reference ready. Vo from 0 to 1.05V, Co=1uF	-	30	-	us
Output over current limit	-	120	-	-	mA
External output capacitor, Co	Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V	0.1	1	-	uF

5.7 Pwrkey

PWR_WF, is used to power up the regulators and take the respective section out of reset. The V_RF and V_core power up when the reset signals are deasserted. All regulators are powered down only when PWR_WF is deasserted.

Table 9: PWR_WF Electrcal Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	VIH	For Chip ON pin	1.125	-	3.6	V
Input low voltage	VIL	-	VSS	-	0.625	V
Pull down resistance (Internal)	PRD	-	-	200	-	kΩ
REG ON time	TREG_ON	-	8	-	-	ms
REG OFF time	TREG_OFF	-	6	-	-	ms

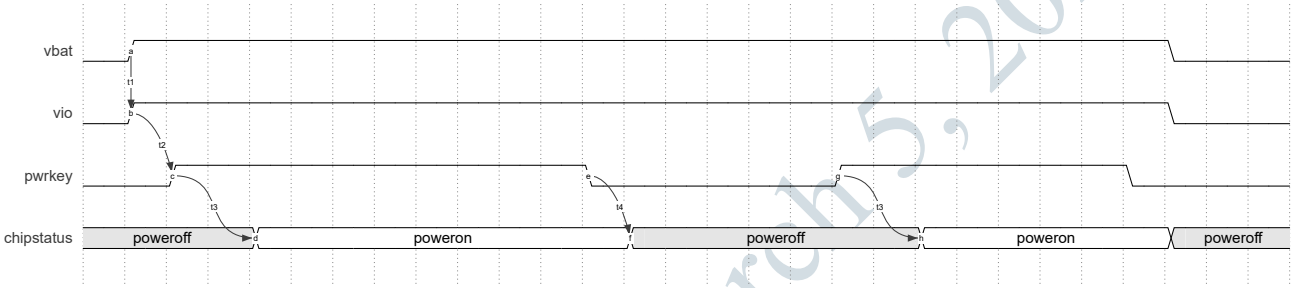


Figure 4: AIC8800D80I Power ON/OFF Timing

Table 10: Power ON/OFF Specifications

Symbol	Discription	Min	Typ	Max	Unit
t1	VIO's power time ≥ VBAT's	0	-	-	ms
t2	PWR_WF's high time ≥ VIO's	0	200	-	us
t3	Chip all power on ready time	-	8	-	ms
t4	Hold PWR_WF low for a sufficient amount of time to ensure that the chip is completely shut down	6	-	-	ms

Note: In practical applications where VIO=1.8V, if the VIO is powered on earlier than VBAT, there is no problem for the chip

6 External Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. Colpitts type oscillator circuits is adopted to provide high quality reference clock. Only one lead pin is required and external load capacitors are saved. The table below lists the requirement for the crystal unit.

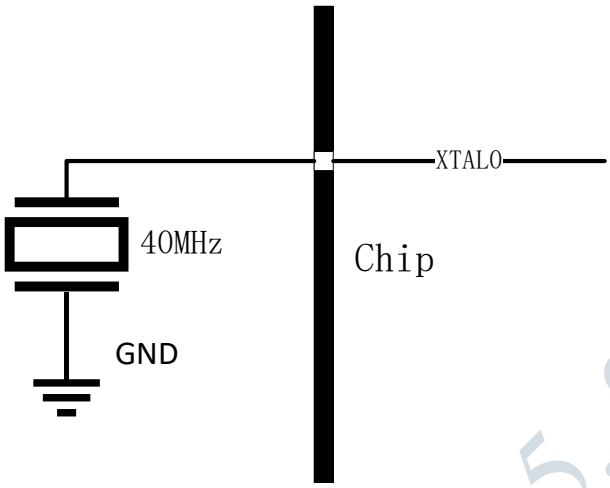


Figure 5: Colpitts mode

Table 11: Colpitts mode crystal requirement

Symbol	Parameter	Value	Note
F0	Nominal Frequency	40MHz	
ΔF/F0	Frequency Tolerance	±10ppm	@25 °C±3 °C
TC	Frequency Stability	±10ppm	Over Operating Temp. Range (Reference 25 °C)
ESR	Equivalent Series Resistance	<40Ω	
CL	Load Capacitance	10pF	
TS	Pulling Sensitivity	≥15ppm/pF	
DL	Drive Level	>100uW	
Amp	Oscillation Amplitude	>2Vpp	Oscilloscope probe input capacitance <1pF

7 Interface

AIC8800D80I supports a variety of data interfaces.

7.1 SDIO

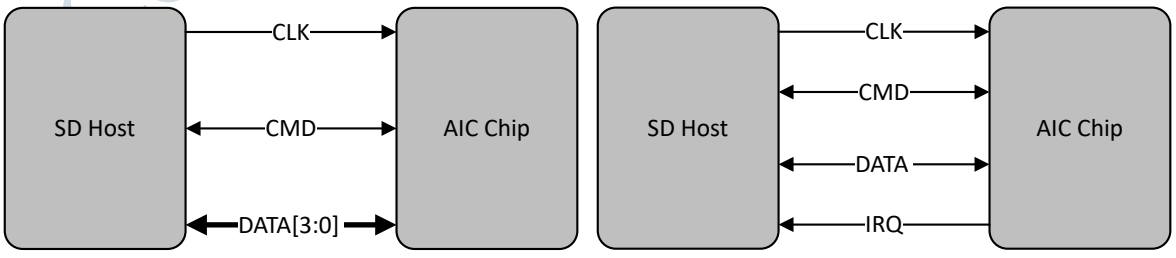
7.1.1 Description

In the SDIO application, the data of WiFi is transmitted through the SDIO, the data of Bluetooth is transmitted through the UART, and the audio data can be transmitted either UART or PCM.
The AIC8800D80I WLAN section support for SDIO version 3.0, the feature is as follow:

- SDIO card specification version 3.0
- Support 4-bit bus width
- SDR25 mode 50MHz@3.3v pad
- SDR50 mode 100MHz@1.8v pad
- SDR104 mode 208MHz@1.8v pad
- DDR50 mode 50MHz@1.8v pad
- Support hardware CRC generation and error detection
- Support block size of 1 to 65535 bytes

Table 12: SDIO Pin Description

Pin NO.	SD-4Bit Mode		SD-1Bit Mode	
P17	DATA2	Data line 2	NC	Not used
P18	DATA3	Data line 3	NC	Not used
P19	CMD	Command line	CMD	Command line
P20	CLK	Clock	CLK	Clock
P21	DATA0	Data line 0	DATA	Data line
P22	DATA1	Data line 1 or interrupt	IRQ	Interrupt



(a) SDIO-4Bit Mode (b) SDIO-1Bit Mode

Figure 6: SDIO Mode

7.1.2 SDIO Timing

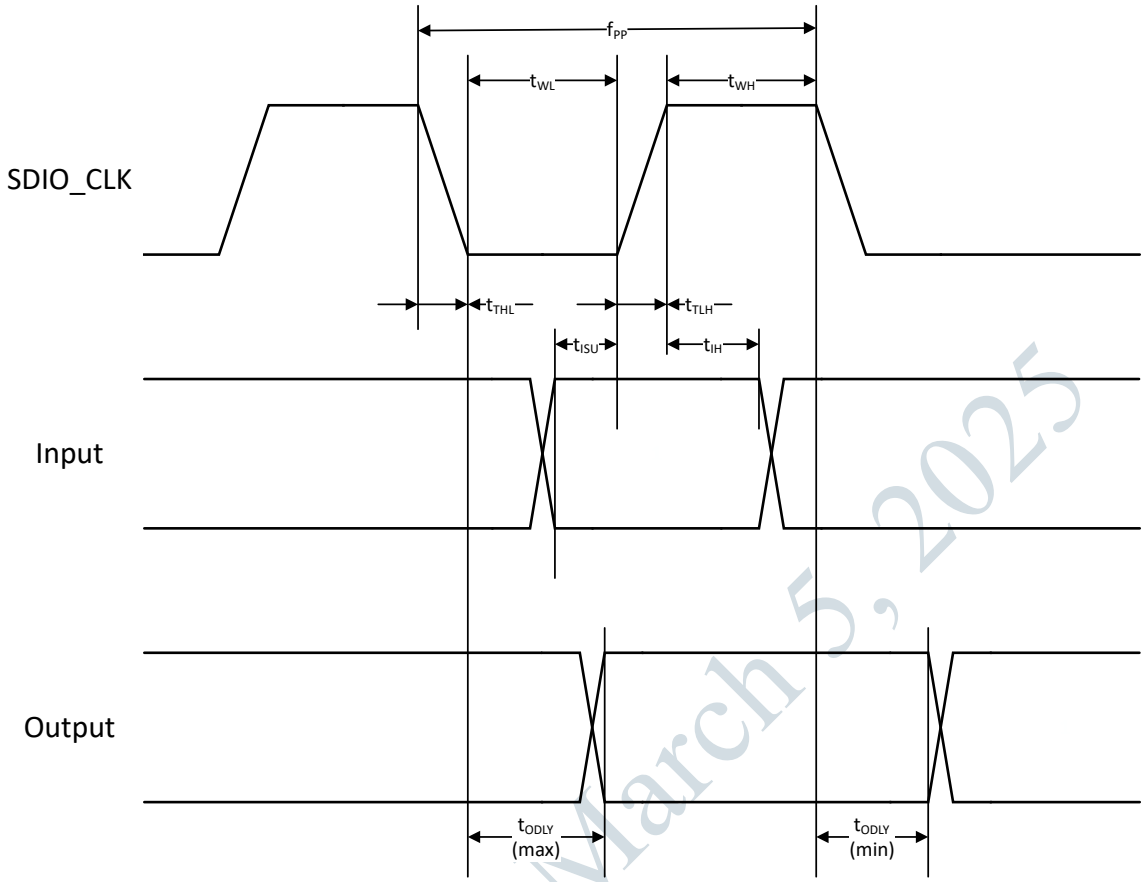


Figure 7: SDIO default mode timing

Table 13: SDIO default mode timing

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)					
Frequency - Data Transfer mode	f_{PP}	0	-	25	MHz
Frequency - Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	10	-	-	ns
Clock high time	t_{WH}	10	-	-	ns
Clock rise time	t_{TLH}	-	-	10	ns
Clock fall time	t_{THL}	-	-	10	ns
Inputs: CMD, DAT(referenced to CLK)					
Input setup time	t_{ISU}	5	-	-	ns
Input hold time	t_{IH}	5	-	-	ns
Outputs: CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	0	-	14	ns
Output delay time - Identification mode	t_{ODLY}	0	-	50	ns

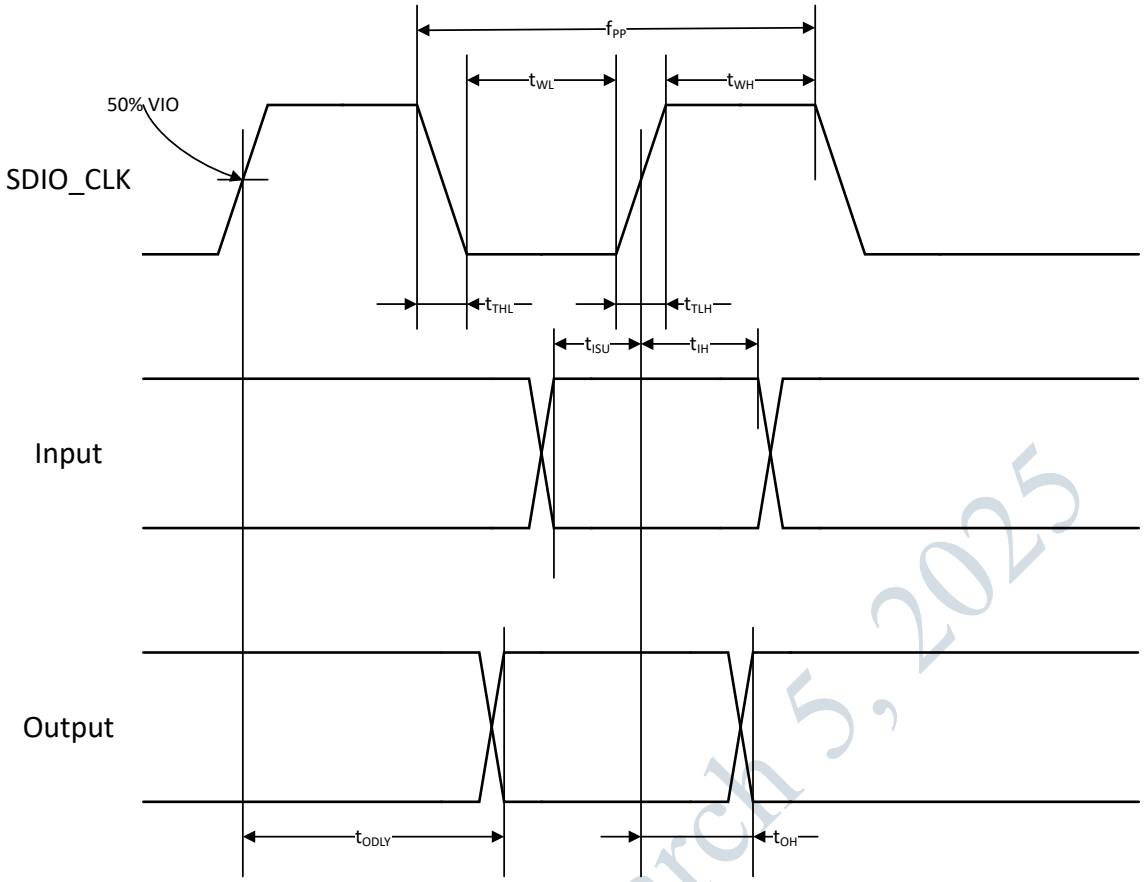


Figure 8: SDIO high speed mode timing

Table 14: SDIO high speed mode timing

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)					
Frequency - Data Transfer mode	f_{PP}	0	-	50	MHz
Frequency - Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	7	-	-	ns
Clock high time	t_{WH}	7	-	-	ns
Clock rise time	t_{TLH}	-	-	3	ns
Clock fall time	t_{THL}	-	-	3	ns
Inputs: CMD, DAT(referenced to CLK)					
Input setup time	t_{ISU}	6	-	-	ns
Input hold time	t_{IH}	2	-	-	ns
Outputs: CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	-	-	14	ns
Output hold time	t_{OH}	2.5	-	-	ns

7.2 USB2.0

7.2.1 Description

In the USB application, the data of Bluetooth/WiFi is transmitted through the USB, and the audio data can be transmitted either USB or PCM.
The AIC8800D80I WLAN section support for USB version 2.0, the feature is as follow:

- Complies with USB Specification Revision 2.0 for WLAN and Bluetooth controller
- Supports up to 7 bidirectional endpoints, including control endpoint 0
- Supports packet-based, Dynamic FIFO memory allocation for endpoints for small FIFOs and flexible efficient use of RAM
- Supports endpoint FIFO sizes that are not powers of 2, to allow the use of contiguous memory locations

7.2.2 USB Timing

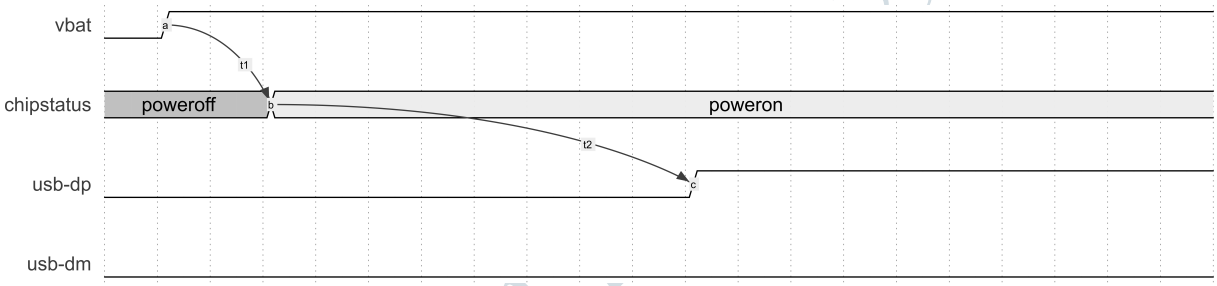


Figure 9: Powerup USB Initial

t1: chip all power on ready time ≥ power up time + 8ms.
t2: usb dp pull up time ≥ chip all power on ready time + 22ms

8 GPIO

AIC8800D80I has a total of 23 GPIO pins, including GPIOA0∼15 and GPIOB0∼6. These GPIOs can be configured with registers for different functions.

8.1 Threshold

Table 15: IO Threshold

VIO	Symbol	IO Threshold
1.8V	V_{inh}	1.320V
1.8V	V_{inl}	0.470V
3.3V	V_{inh}	2.840V
3.3V	V_{inl}	0.300V

8.2 IO Assignment

8.2.1 General Application

In the general design, the chip pin assignment is referred to Table 16, the public driver cab be used directly.

Table 16: General IO Assignment

GPIO	Pin NO.	Assignment	Type	Description
GPIOA0	32	PCM_FSYNC	I/O	PCM sync signal, can be master (output) or slave (input)
GPIOA1	30	PCM_CLK	I/O	PCM clock, can be master (output) or slave (input)
GPIOA2	29	PCM_DIN	I	PCM data input
GPIOA3	28	PCM_DOUT	O	PCM data output
GPIOA4	3	BT_UART_RX	I	UART receive data
GPIOA5	11	BT_UART_TX	O	UART transmit data
GPIOA6	12	BT_UART_CTS	I	UART clear to send
GPIOA7	13	BT_UART_RTS	O	UART request to send
GPIOA8	14	UART_RX	I	Debug UART RX
GPIOA9	15	UART_TX	O	Debug UART TX
GPIOA10	22	SDIO_DATA1	I/O	SDIO data1
GPIOA11	21	SDIO_DATA0	I/O	SDIO data0
GPIOA12	20	SDIO_CLK	I	SDIO clock
GPIOA13	19	SDIO_CMD	I/O	SDIO command
GPIOA14	18	SDIO_DATA3	I/O	SDIO data3
GPIOA15	17	SDIO_DATA2	I/O	SDIO data2
GPIOB0	46	HST_WAK_WF	I	Host wake up WLAN, reserved pin, this function is implemented through the SDIO
GPIOB1	47	WF_WAK_HST	O	WLAN wake up host
GPIOB2	48	BT_WAK_HST	O	BT wake up host
GPIOB3	1	HST_WAK_BT	I	Host wake up BT
GPIOB4	2		I/O	GPIO

Table 16: General IO Assignment

GPIO	Pin NO.	Assignment	Type	Description
GPIOB5	7		I/O	GPIO
GPIOB6	26		I/O	GPIO

8.2.2 Special Application

In the special design, such as external FEM, dual antenna switching, etc, the chip pin assignment is referred to Table 17. Such applications require special firmware.

Table 17: Special IO Assignment

GPIO	Pin NO.	Assignment	Type	Description
GPIOA0	32	5G_RX	O	FEM control for 5G RX
GPIOA1	30	2G4_RX	O	FEM control for 2.4G RX
GPIOA2	29	5G_TX	O	FEM control for 5G TX
GPIOA3	28	2G4_TX	O	FEM control for 2.4G TX
GPIOA4	3	BT_UART_RX	I	UART receive data
GPIOA5	11	BT_UART_TX	O	UART transmit data
GPIOA6	12	BT_UART_CTS	I	UART clear to send
GPIOA7	13	BT_UART_RTS	O	UART request to send
GPIOA8	14	UART_RX	I	Debug UART RX
GPIOA9	15	UART_TX	O	Debug UART TX
GPIOA10	22	SDIO_DATA1	I/O	SDIO data1
GPIOA11	21	SDIO_DATA0	I/O	SDIO data0
GPIOA12	20	SDIO_CLK	I	SDIO clock
GPIOA13	19	SDIO_CMD	I/O	SDIO command
GPIOA14	18	SDIO_DATA3	I/O	SDIO data3
GPIOA15	17	SDIO_DATA2	I/O	SDIO data2
GPIOB0	46	HST_WAK_WF	I	Host wake up WLAN, reserved pin, this function is implemented through the SDIO
GPIOB1	47	WF_WAK_HST	O	WLAN wake up host
GPIOB2	48	BT_WAK_HST	O	BT wake up host
GPIOB3	1	HST_WAK_BT	I	Host wake up BT
GPIOB4	2	ANT_SW	O	Antenna switch control
GPIOB5	7		I/O	GPIO
GPIOB6	26		I/O	GPIO

8.3 IO Status

Table 18: Default Status of IO

GPIO	Pin NO.	Function	Type	Pull
GPIOA0	32	SW_CLK	I	UP
GPIOA1	30	SWD	I/O	UP
GPIOA2	29	GPIOA2	I/O	DN
GPIOA3	28	GPIOA3	O	DN
GPIOA4	3	GPIOA4	I/O	DN

Table 18: Default Status of IO

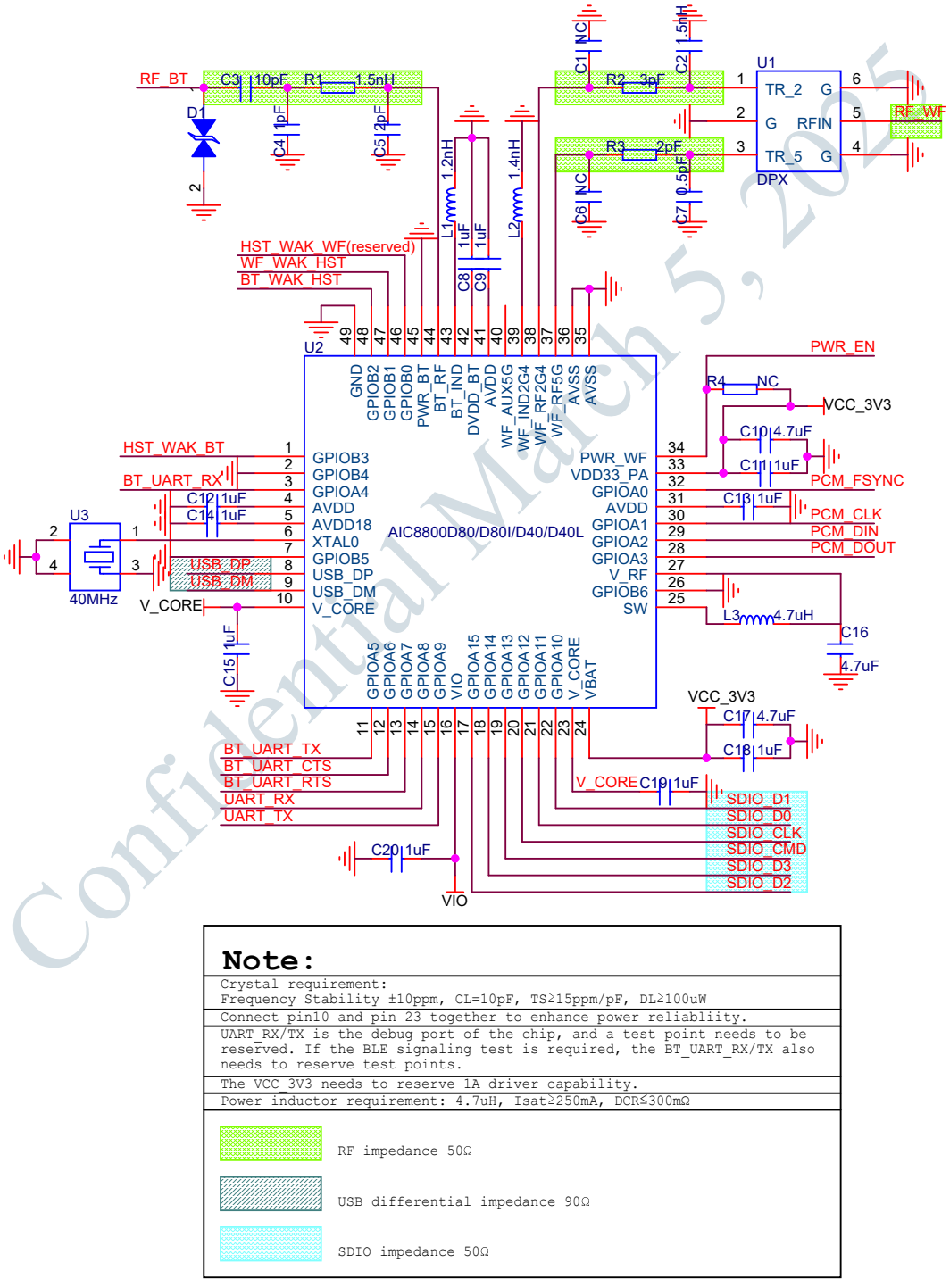
GPIO	Pin NO.	Function	Type	Pull
GPIOA5	11	GPIOA5	I/O	DN
GPIOA6	12	GPIOA6	I/O	DN
GPIOA7	13	GPIOA7	I/O	DN
GPIOA8	14	UART0_RX	I	UP
GPIOA9	15	UART0_TX	O	OFF
GPIOA10	22	SDIO_DATA1	I/O	UP
GPIOA11	21	SDIO_DATA0	I/O	UP
GPIOA12	20	SDIO_CLK	I	OFF
GPIOA13	19	SDIO_CMD	I/O	UP
GPIOA14	18	SDIO_DATA3	I/O	UP
GPIOA15	17	SDIO_DATA2	I/O	UP
GPIOB0	46	GPIOB0	I/O	UP
GPIOB1	47	GPIOB1	I/O	UP
GPIOB2	48	GPIOB2	I/O	DN
GPIOB3	1	GPIOB3	I/O	DN
GPIOB4	2	GPIOB4	I/O	DN
GPIOB5	7	GPIOB5	I/O	DN
GPIOB6	26	GPIOB6	I/O	DN

I: Input signal
O: Output signal
I/O: Input/Output signal
UP: Pulled up (of 50KΩ)
DN: Pulled down (of 50KΩ)
OFF: Neither pulled up nor pulled down

9 Application Circuit

The AIC8800D80I Bluetooth RF design supports two modes, BT Only Mode and BT Coant Mode. The advantage of the BT Only Mode is that it can operate simultaneously with WiFi 2.4G, Combined with AIC's excellent coexistence design, it can provide higher throughput and superior Bluetooth performance. The advantage of the BT Coant Mode is that it saves space and cost.

9.1 BT Only Mode



Note:

Crystal requirement:
Frequency Stability ±10ppm, CL=10pF, TS≥15ppm/pF, DL≥100uW

Connect pin10 and pin 23 together to enhance power reliablity.

UART_RX/TX is the debug port of the chip, and a test point needs to be reserved. If the BLE signaling test is required, the BT_UART_RX/TX also needs to reserve test points.

The VCC_3V3 needs to reserve 1A driver capability.

Power inductor requirement: 4.7uH, Isat≥250mA, DCR≤300mΩ

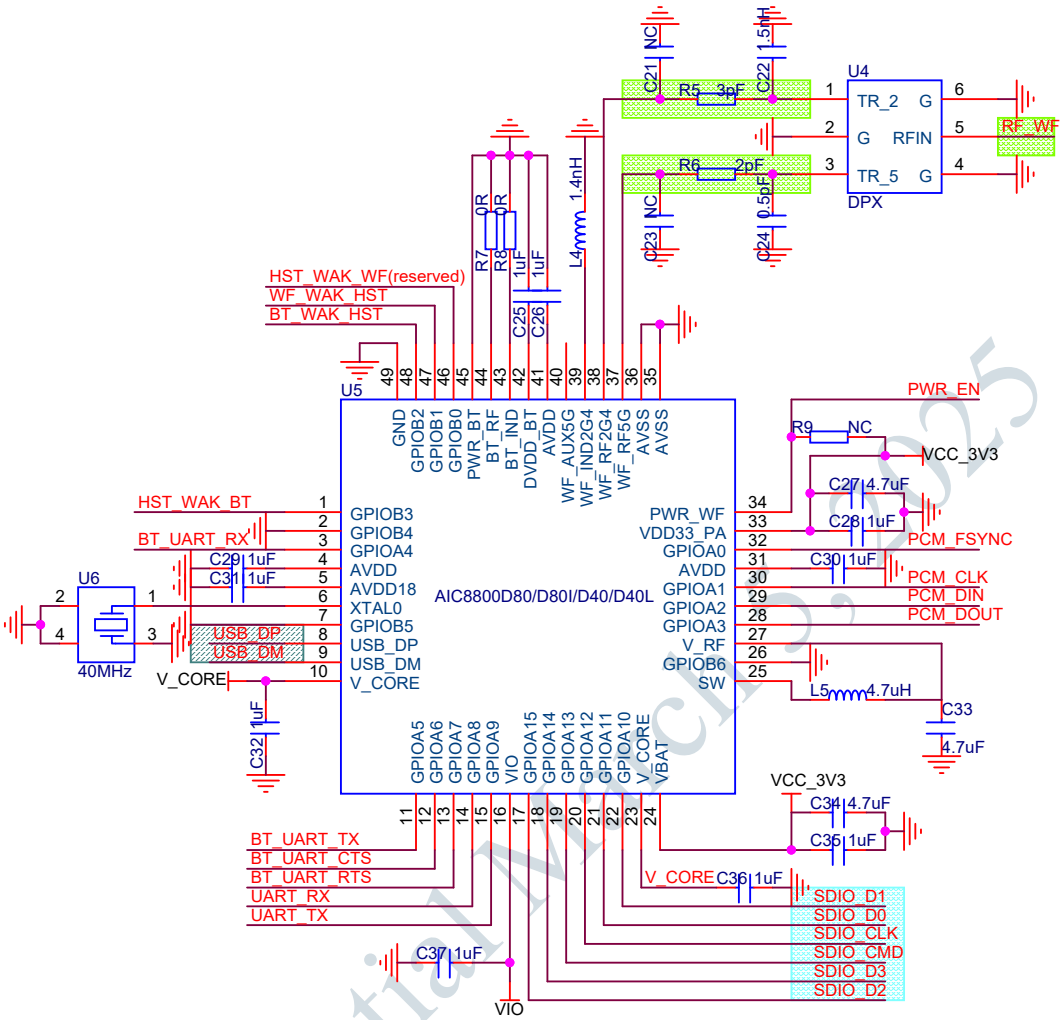
RF impedance 50Ω

USB differential impedance 90Ω

SDIO impedance 50Ω

Figure 10: AIC8800D80I BT Only Mode Application Circuit

9.2 BT Coant Mode



Note:

Crystal requirement:
Frequency Stability ±10ppm, CL=10pF, TS≥15ppm/pF, DL≥100uW

Connect pin10 and pin 23 together to enhance power reliabliity.

UART_RX/TX is the debug port of the chip, and a test point needs to be reserved. If the BLE signaling test is required, the BT_UART_RX/TX also needs to reserve test points.

The VCC_3V3 needs to reserve 1A driver capability.

Power inductor requirement: 4.7uH, Isat≥250mA, DCR≤300mΩ

RF impedance 50Ω

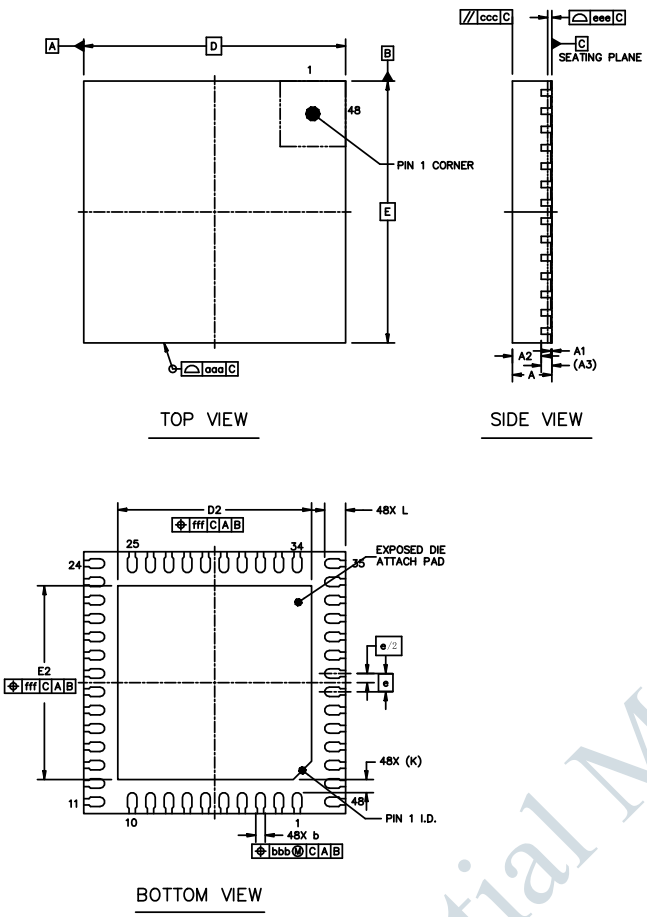
USB differential impedance 90Ω

SDIO impedance 50Ω

Figure 11: AIC8800D80I BT Coant Mode Application Circuit

10 Package Physical Dimension

10.1 Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	3.6	3.7	3.8
	Y	E2	3.6	3.7	3.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Figure 12: AIC8800D80I Packaging

10.2 Reel Information

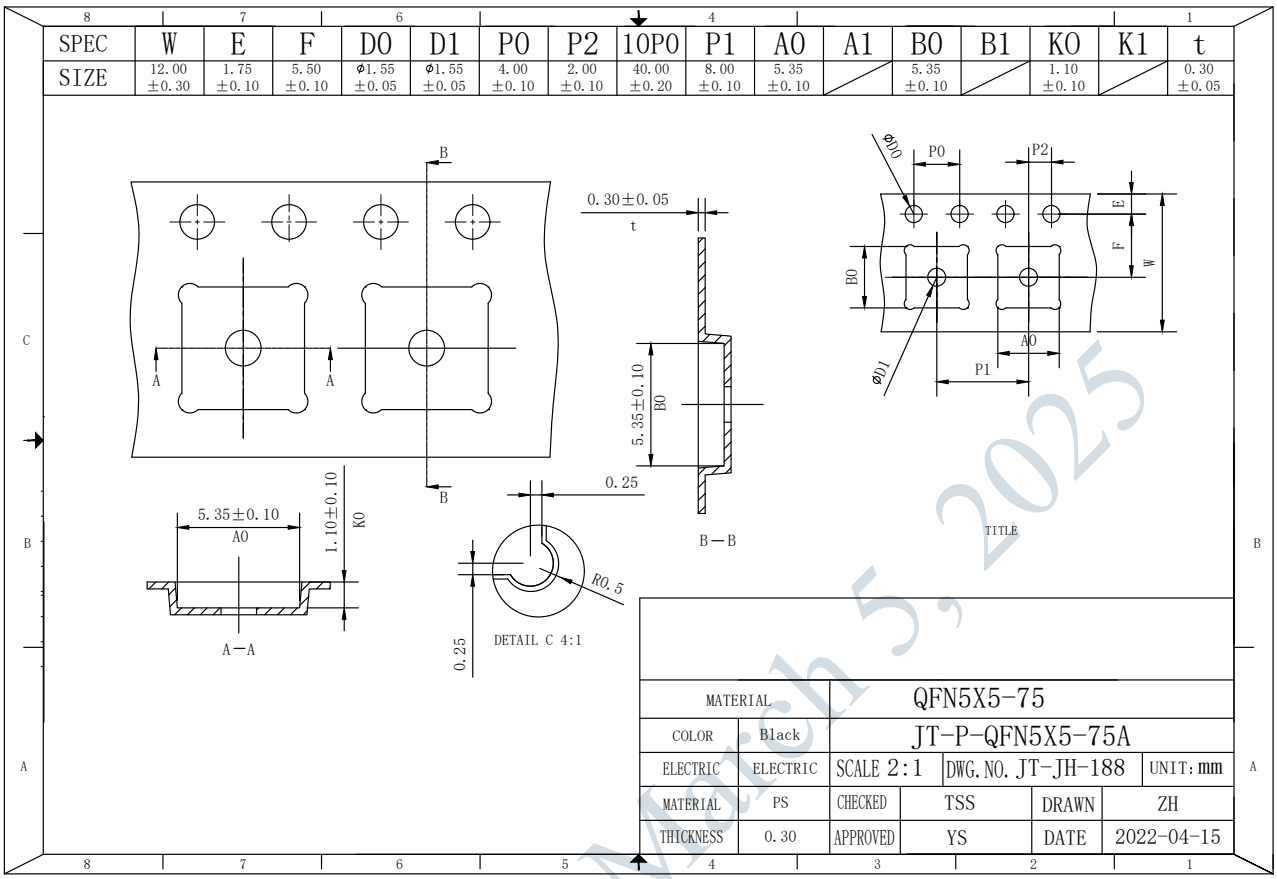
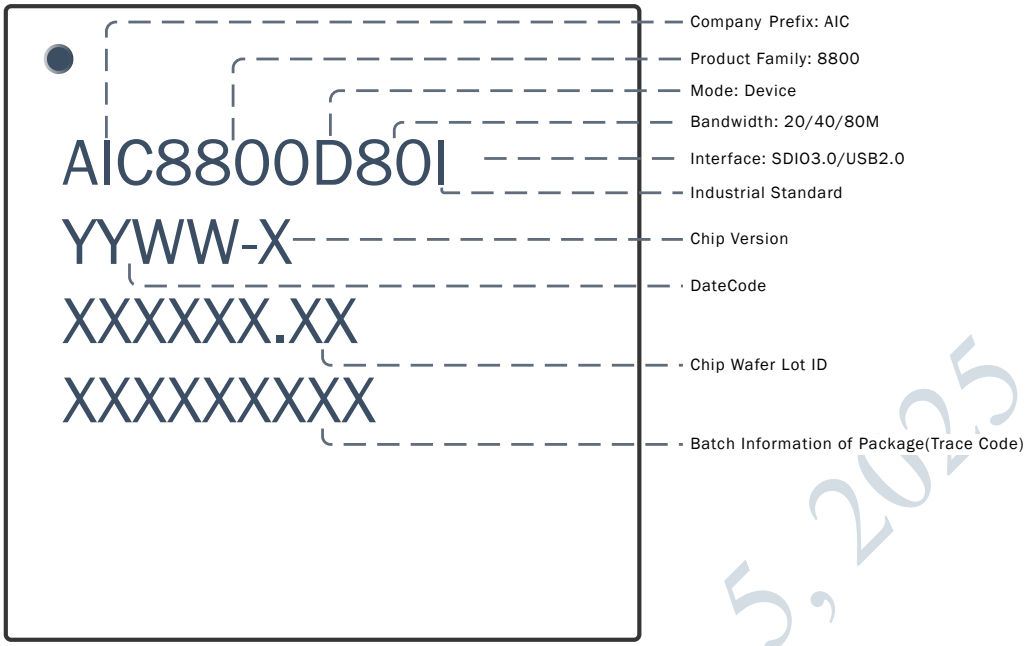
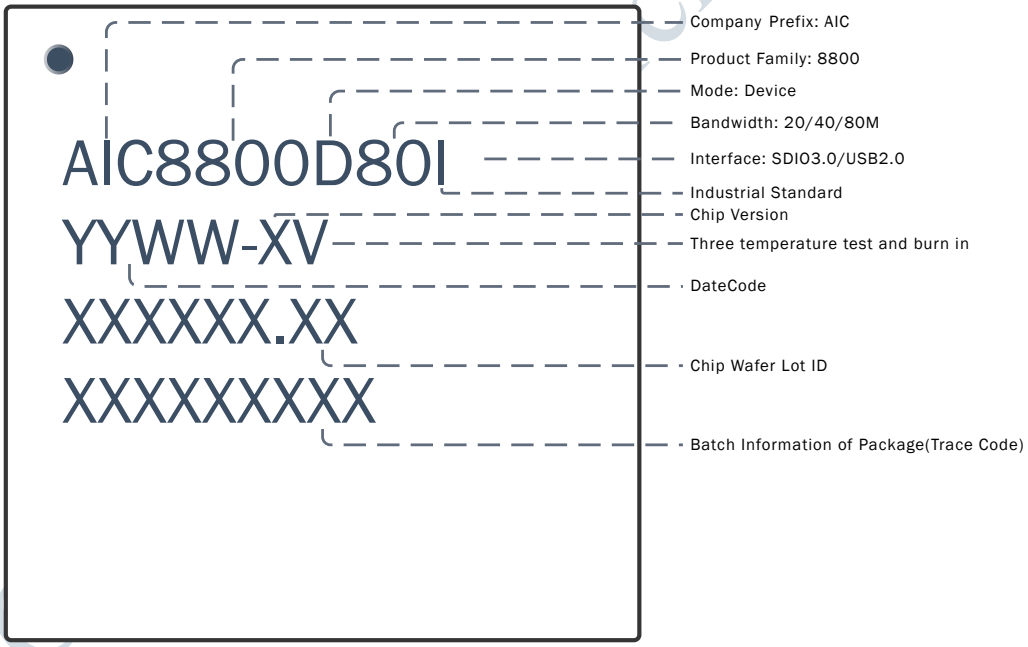


Figure 13: AIC8800D80I Reel Information

10.3 Product Identification



(a) AIC8800D80I Silk Screen A



(b) AIC8800D80I Silk Screen B

Figure 14: AIC8800D80I Silk Screen

10.4 Package Thermal Characteristics

Table 19: Package Thermal Characteristics

Characteristic	**Value**
θ_{JA} in still air(°C/W)	46.46
θ_{JB} (°C/W)	4.657
θ_{JC} (°C/W)	9.759
ψ_{JT} (°C/W)	0.3
ψ_{JB} (°C/W)	3
Maximum junction temperature T_j (°C)	125
Maximum power dissipation (W)	1.5

10.5 Ording information

Table 20: Ordering Information

Part Number	**Package**	**Description**	**Operating Ambient Temperature**	**Additional Test**
AIC8800D80I	48 pin QFN package 5mm*5mm, 0.35mm pitch	Dual-band 2.4GHz and 5GHz WiFi6+Bluetooth 5.4	$-40\,°C$ to $85\,°C$	Three temperature test
AIC8800D80I-V	48 pin QFN package 5mm*5mm, 0.35mm pitch	Dual-band 2.4GHz and 5GHz WiFi6+Bluetooth 5.4	$-40\,°C$ to $85\,°C$	Three temperature test and burn in

11 Reliability characteristics

Table 21: Reliability characteristics

Test Items	Test Condition	Test Criteria
HTOL	T_j=125 °C, 1000hrs, 1.1Vcc	JESD22-A108
LTOL	T_a=−40 °C, 1000hrs, 1.1Vcc	JESD22-A108
ESD	HBM:±2000V Class 2	JS-001-2023
	CDM:±250V Class C1	JS-002-2022
LU	±200mA Class I	JESD78F.02-2023
Solder ability	steam aging:8hrs; 245 °C, 5s	J-STD-002D-2013
HTST	150 °C (500/1000hrs)	JESD22-A103
LTST	−40 °C (168/1000hrs)	JESD22-A119
TCT	−65 °C to 150 °C, Dwell=15min, 500/1000Cycles	JESD22-A104E-2014
PCT	121 °C, 100%RH, 205kPa, 96/168hrs	JESD22-A102E-2015
UHAST	130 °C, 85%RH, 33.3psia, 96hrs	JESD22-A118
BHAST	130 °C, 85%RH, 33.3psia, 1.1Vcc, 96hrs	JESD22-A110E.01-2021
Precon MSL3	Level 3, Bake: 125 °C, 24hrs. Moisture Soak:30 °C,60%, 192hrs. Reflow : 260 °C, 3 times	JESD22-A113

12 Solder Reflow Profile

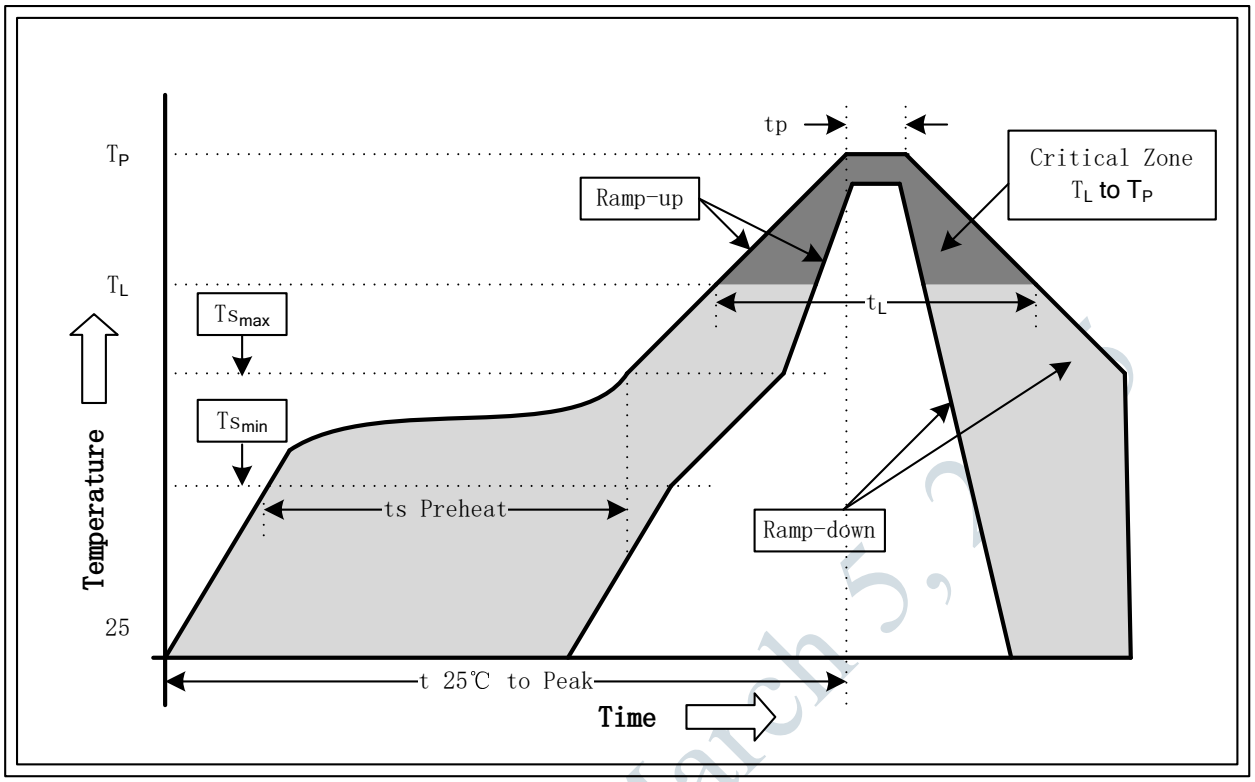


Figure 15: Classification Reflow Profile

Table 22: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 183 °C 60-150seconds	 217 °C 60-150 seconds
Peak /Classification Temperature(Tp)	See the table 23	See Table 24
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 23: Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	**Volume mm3 <350**	**Volume mm3 ≥350**
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table 24: Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	**Volume mm3 <350**	**Volume mm3 350–2000**	**Volume mm3 >2000**
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm–2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Note 1: All temperature refers topside of the package. Measured on the package body surface.
Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 24.
Note 3: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non integral heat sinks.
Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package maysill exist.
Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table 22, Table 23, Table 24 whether or not lead free.

13 Change List

The following Table 25 summarizes revisions to this document.

Table 25: Change List

Rev	Date	Auther	Change description
V1.0.0	20230417	AICSEMI	initial version
V1.0.1	20241205	AICSEMI	Add the description of each power supply parameter Add the description of interface Add the description of GPIO
V1.0.2	20250305	AICSEMI	Add the silkscreen about AIC8800D80I-V Add the ording information about AIC8800D80I-V

14 RoHS Compliant

The products meet the requirements of Directive 2011/65/EU of Europe Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). The products are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals.

15 ESD Sensitivity

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site. AIC products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment.

16 Disclaimer

The information provided here is believed to be reliable; AICSEMI assumes no reliability for inaccuracies and omissions. AICSEMI assumes no reliability for the use of this information and all such information should entirely be at the user's own risk. Specifications described and contained here are subjected to change without notice on the purpose of improving the design and performance. All of this information described herein should not be implied or granted for any third party. AICSEMI does not authorize or warrant any AICSEMI products for use in the life support devices or systems.

For technical questions and additional information about AICSEMI Inc.:
Website: www.AICSEMI.com
Mailbox: support@AICSEMI.com
AICSEMI (Shanghai), Inc.
Tel: +86-10-84097662
Fax: +86-10-84097662