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1. General Description

AIC8800DW is a highly integrated chip with 2.4GHz Wi-Fi6 for wireless application.

1.1 Wi-Fi Features

- CMOS single-chip fully-integrated RF, Modem and MAC
- Support 2.4GHz Wi-Fi6
- Data rates up to 286.8Mbps@TX and 229.4Mbps@RX with 20/40MHz bandwidth
- RX sensitivity -98dBm in 11b 1M mode
- Tx power up to 20dBm in 11b mode, 18dBm in HT/VHT/HE40 MCS7 mode
- Support STA, AP, Wi-Fi Direct modes concurrently
- Support STBC, beamforming
- Support Wi-Fi6 TWT
- Support Two NAV, Buffer Report, Spatial reuse, Multi-BSSID, intra-PPDU power save
- Support LDPC
- Support MU-MIMO, OFDMA
- Support DCM, Mid-amble, UORA
- Support WEP/WPA/WPA2/WPA3-SAE Personal, MFP

1.2 Other Features

- Supports SDIO/USB2.0/HCI_UART/PCM interface
- Integrated low power timer and watchdog
- 512 bits eFuse



1.3 Packaging Information

- Compact profile package: 4mm×4mm×0.85mm QFN36

1.4 Applications

- IoT device
- Wireless device

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2. Platform Description

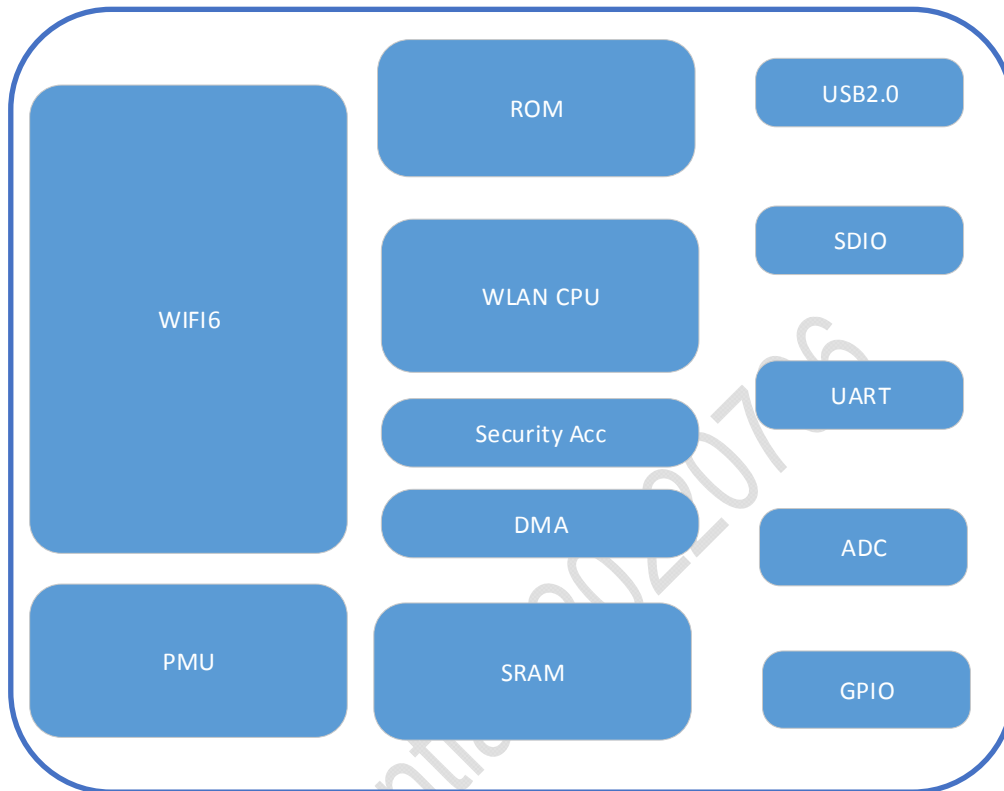


Figure2-1 AIC8800DW Block Diagram



3. Electrical Characteristics

Table 3-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VBAT	Supply Voltage from battery or LDO	2.97	3.3	3.63	V
T _{amb}	Ambient Temperature	-20	27	+80	°C
V _{IL}	CMOS Low Level Input Voltage	0		0.3*VIO	V
V _{IH}	CMOS High Level Input Voltage	0.7*VIO		VIO	V
V _{TH}	CMOS Threshold Voltage		0.5*VIO		V

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4. PINS Description

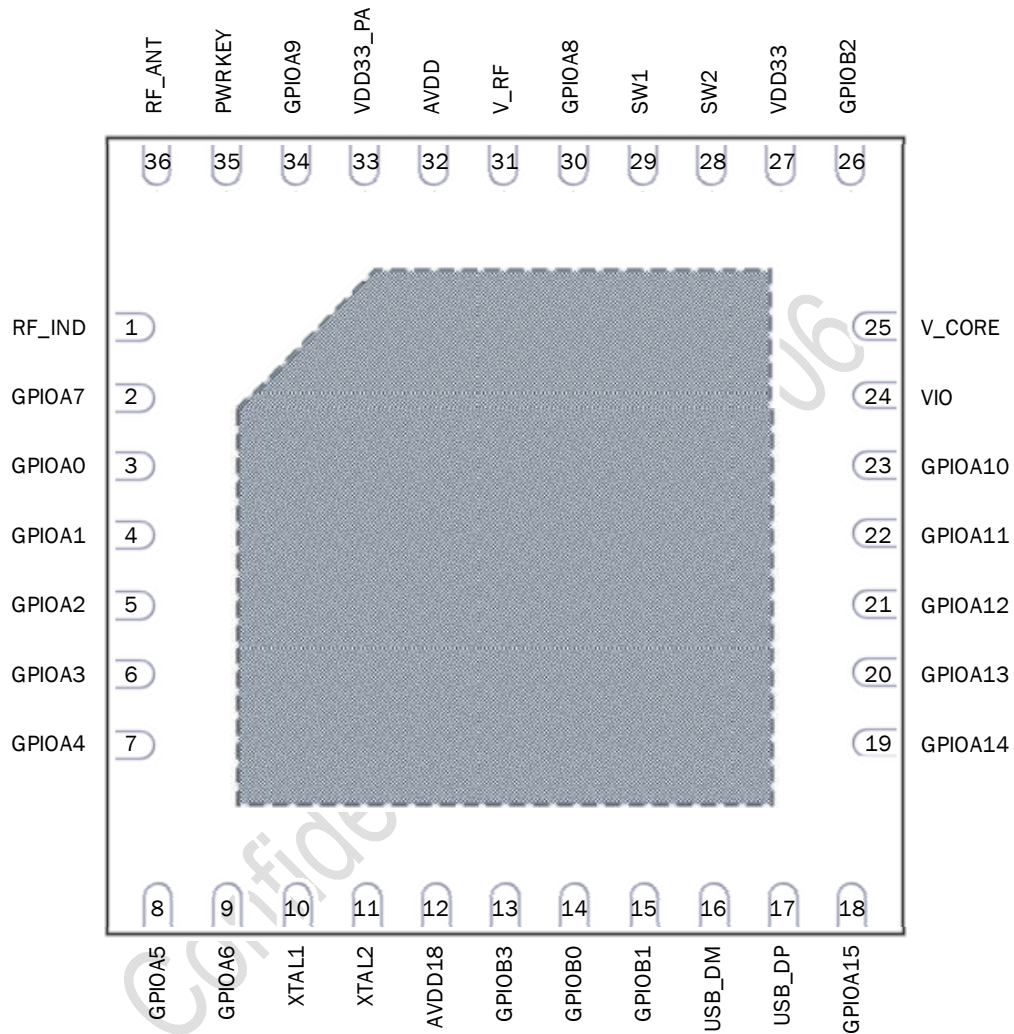


Figure 4-1 AIC8800DW Pin Map


Table 4-1 AIC8800DW Pins Description

PIN NAME	QFN NO.	I/O	DESCRIPTION
RF			
RF_ANT	36	I/O	RF 2.4G, Connect to the output π type matching network.
RF_IND	1		RF ground, Connect to the output a 1.4nH inductor to ground.
PMU			
PWRKEY	35	I	Power Key, high level effective, Internal 200K pull-down resistance to ground.
V_RF	30	I	RF Circuit Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
SW1	29	O	Connect to Pin 28
VDD33	27	I	System Circuit Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
AVDD	32		1.3V Voltage .Bypass with a Capacitor to GND. The capacitor is used by the on-chip V_RF voltage regulator. Do not share the bypass-capacitor ground vias with any other branches
VDD33_PA	33	I	RF PA Voltage Input. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches
AVDD18	12	O	1.8V Voltage Output. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches
VIO	24	I	IO Power Supply. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches
SW2	28	O	Switch node of the regulator. Connect to the output a 10uH(Sat Current $\geq 200\text{mA}$, $R_{DC} \leq 300\text{mohm}$) inductor
V_CORE	25	I	0.9V Voltage Input.Digital Core Circuit Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
CLK			
XTAL1	10	I	Internal/External Oscillator Input. To use the internal oscillator, a 26M Crystal may be connected across XTAL1 and XTAL2. To use external clock, a external clock connected to the XTAL1 pin Through an external 100 pF coupling capacitor. In this case, the XTAL2 pin must be connected to ground.
XTAL2	11	O	Internal Oscillator Output. A 26M Crystal may be connected across XTAL1 and XTAL2. If XTAL2 is not used, it must be tied to GND.
GPIO			
GPIOA0	3	I/O	General-purpose Input/Output
GPIOA1	4	I/O	General-purpose Input/Output
GPIOA2	5	I/O	General-purpose Input/Output
GPIOA3	6	I/O	General-purpose Input/Output
GPIOA4	7	I/O	General-purpose Input/Output
GPIOA5	8	I/O	General-purpose Input/Output
GPIOA6	9	I/O	General-purpose Input/Output
GPIOA7	2	I/O	General-purpose Input/Output

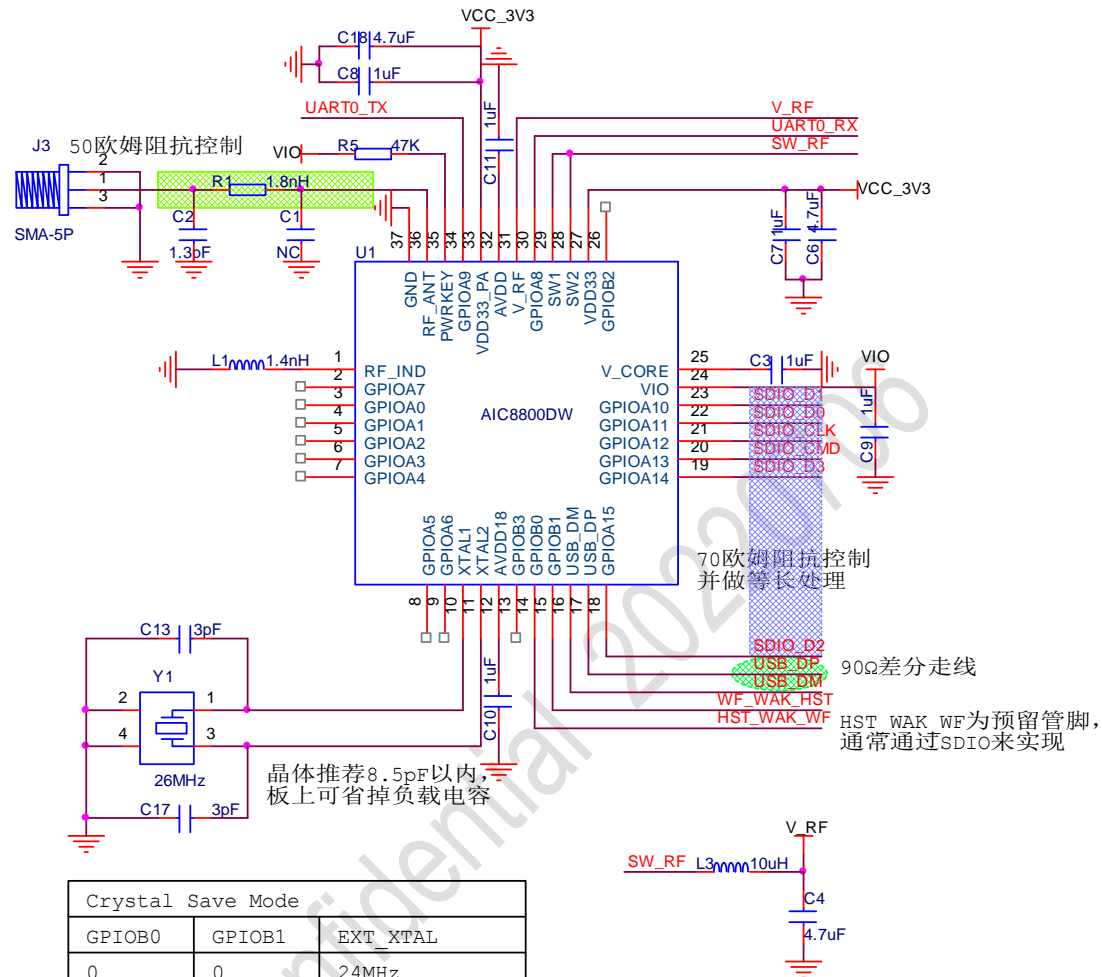


PIN NAME	QFN NO.	I/O	DESCRIPTION
GPIOA8	30	I/O	General-purpose Input/Output
GPIOA9	34	I/O	General-purpose Input/Output
GPIOA10	23	I/O	General-purpose Input/Output
GPIOA11	22	I/O	General-purpose Input/Output
GPIOA12	21	I/O	General-purpose Input/Output
GPIOA13	20	I/O	General-purpose Input/Output
GPIOA14	19	I/O	General-purpose Input/Output
GPIOA15	18	I/O	General-purpose Input/Output
GPIOB0	14	I/O	General-purpose Input/Output
GPIOB1	15	I/O	General-purpose Input/Output
GPIOB2	26	I/O	General-purpose Input/Output
GPIOB3	13	I/O	General-purpose Input/Output
USB_DM	16	I/O	D+ Pin of the USB cable
USB_DP	17	I/O	D- Pin of the USB cable

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5. Application Circuit





6. Package Physical Dimension

6.1 Package Dimensions

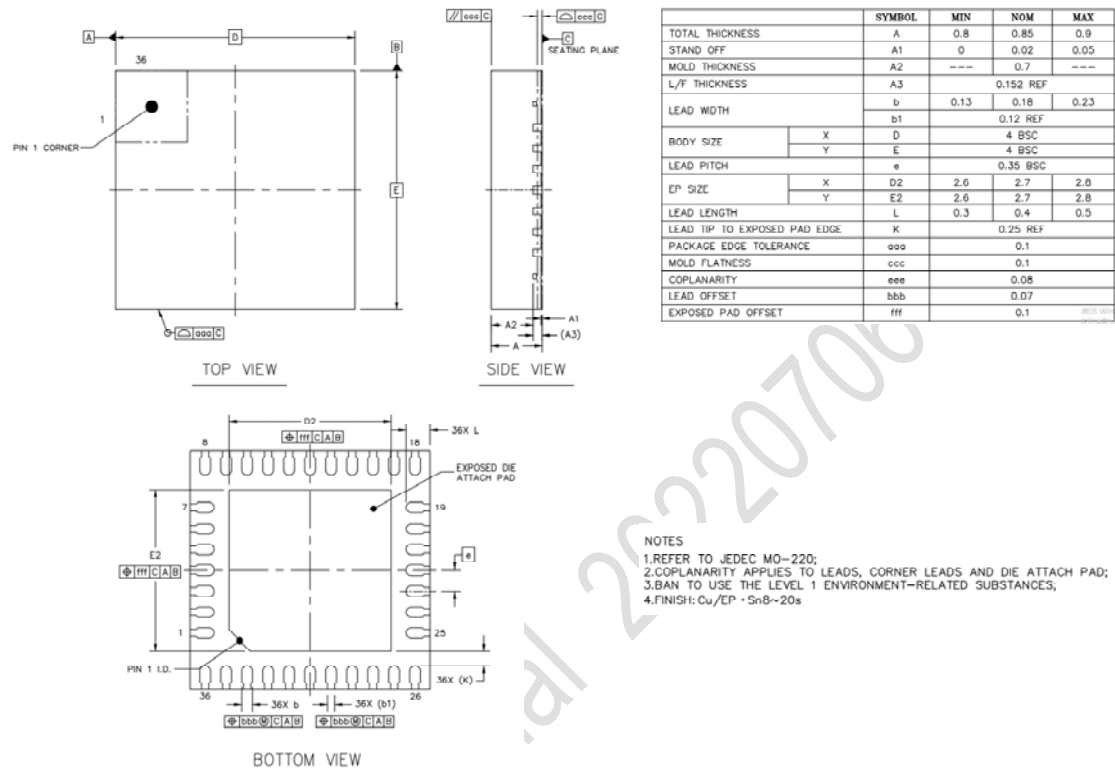
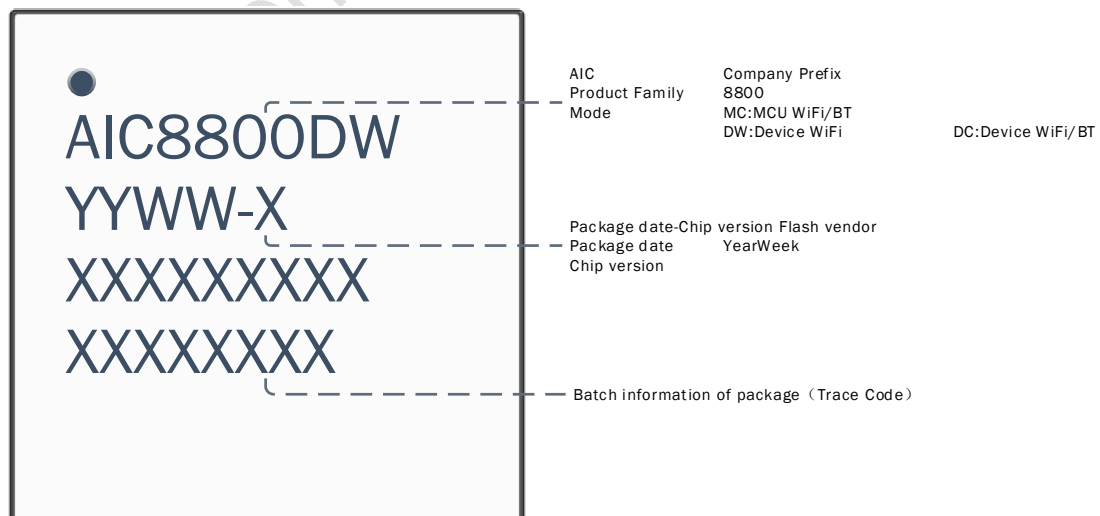


Figure 6-1 AIC8800DW-QFN36

6.2 Product Identification



7. Solder Reflow Profile

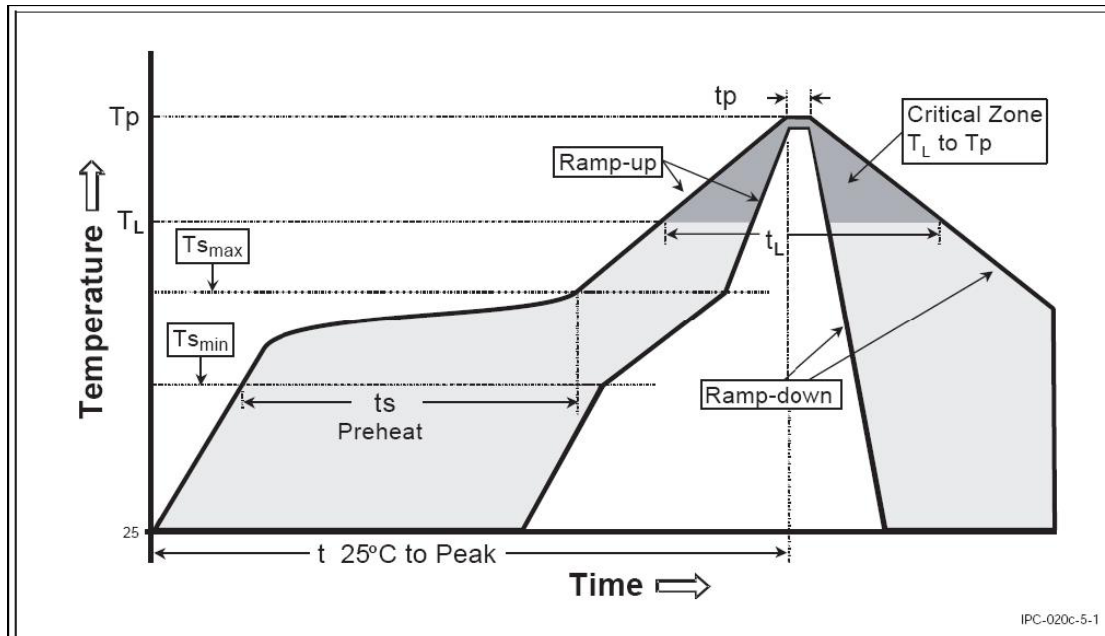


Figure.8-1 Classification Reflow Profile

Table 7-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	3 °C/second max.	3 °C/second max.
Preheat		
-Temperature Min (T _{smin})	100 °C	150 °C
-Temperature Max (T _{smax})	100 °C	200 °C
-Time (t _{smin} to t _{smax})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183 °C	217°C
-Time (t _L)	60-150seconds	60-150 seconds
Peak /Classification Temperature(T _p)	See Table 11-2	See Table 11-3
Time within 5 oC of actual Peak Temperature (t _p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

**Table 7-2 Sn-Pb Eutectic Process – Package Peak Reflow Temperatures**

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table 7-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 350-2000	Volume mm3 >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Note 1: All temperature refers topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 11-3.

Note 3: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may still exist.

Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table 7-1, 7-2, 7-3 whether or not lead free.



8. Change List

The following table summarizes revisions to this document.

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	20220520	AICSEMI	Initial version

9. RoHS Compliant

The products meet the requirements of Directive 2011/65/EU of Europe Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). The products are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals.

10. ESD Sensitivity

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site. BES products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment.



11 Disclaimer

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