Preliminary AIC8800D80P Low-Energy Wi-Fi6/BTDM5.4 SoC

Data Sheet

Revision: 1.0
May 2023

1. General Description

AIC8800D80P is a highly integrated chip with dual band Wi-Fi6, BTDM5.4 for wireless application.

1.1 Wi-Fi Features

- CMOS single-chip fully-integrated RF, Modem and MAC
- Support 2.4GHz/5GHz Wi-Fi6
- Data rates up to 600.4Mbps with 20/40/80MHz bandwidth
- Support 5MHz/10MHz mode
- RX sensitivity -97dBm in 11b 1M mode
- Tx power up to 23dBm in 11b mode, 18dBm in HT/VHT/HE MCS7 mode
- Support STA, AP, Wi-Fi Direct modes concurrently
- Support STBC, beamforming
- Support Wi-Fi6 TWT
- Support Two NAV, Buffer Report, Spatial reuse, Multi-BSSID, intra-PPDU power save
- Support LDPC
- Support MU-MIMO, OFDMA
- Support DCM, Mid-amble, UORA
- Support WEP/WPA/WPA2/WPA3-SAE Personal, MFP

1.2 BTDM5.4 Features

- Supports all the mandatory and optional features of Bluetooth 2.1+EDR/3.0/4.x/5.3/5.4
- Supports advanced master and slave topologies

1.3 Other Features

- Supports USB2.0/PCIE/HCI_UART/PCM interface
- Integrated low power timer and watchdog
- 512 bits eFuse

1.4 Packaging Information

- Compact profile package：5mm×5mm×0.75mm QFN48

1.5 Applications

- IoT device
- Wireless device

2. Platform Description

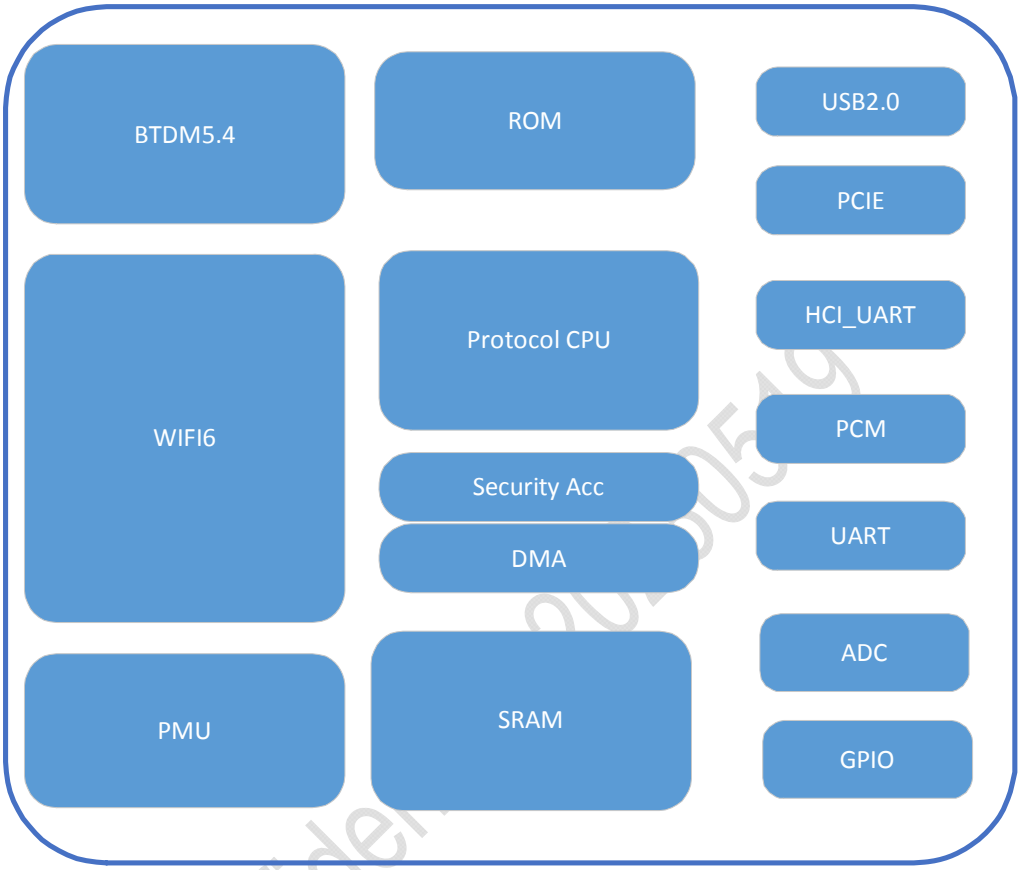


Figure2-1 AIC8800D80P Block Diagram

3. PINS Description

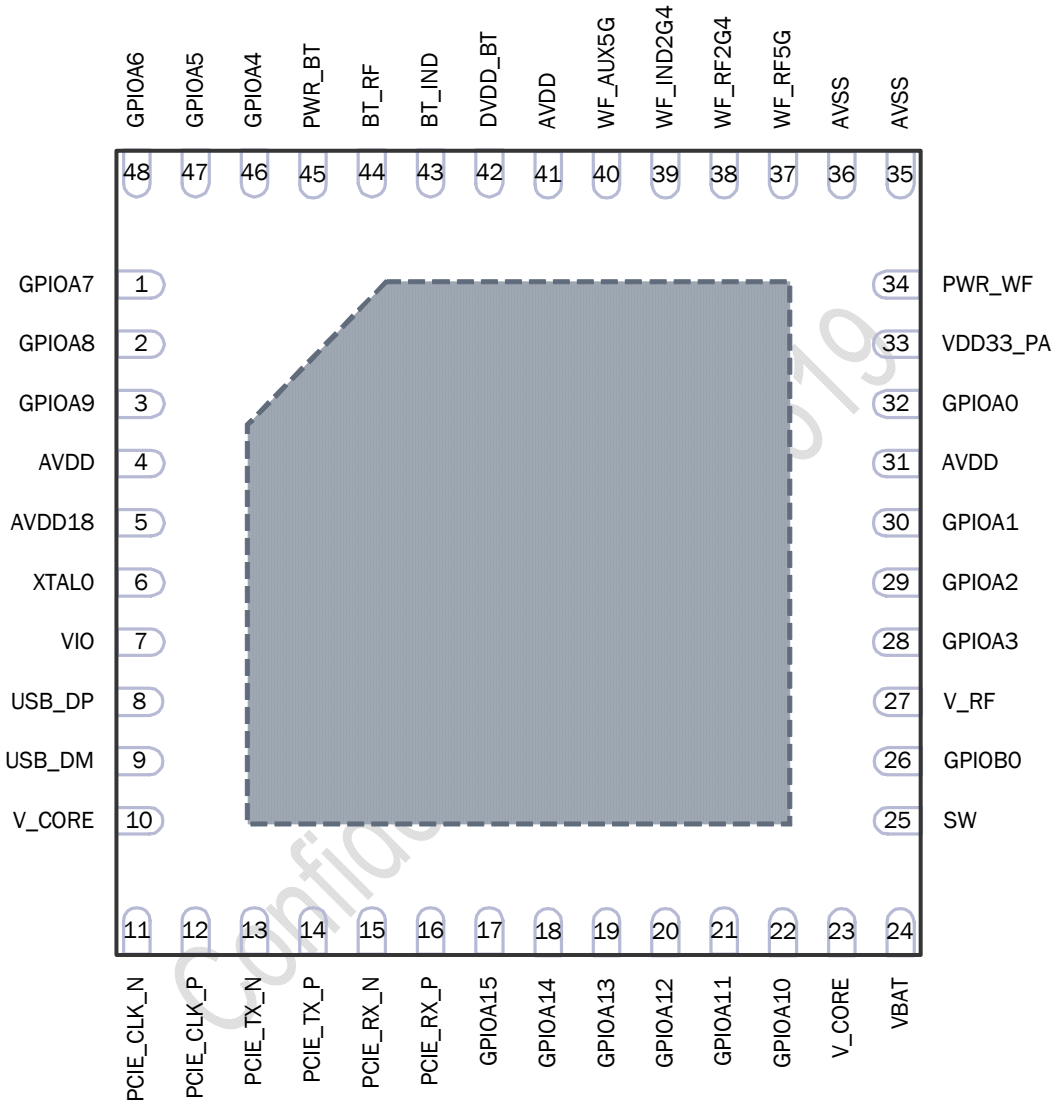


Figure 3-1 AIC8800D80P Pin Map

Table 3-1 AIC8800D80P_48pin Pins Description

TERMINAL			DESCRIPTION
PIN NAME	QFN NO.	I/O	
RF			
WF_RF2G4	38	I/O	WiFi 2.4G RF
WF_IND2G4	39		WiFi 2.4G RF Ground, connect a 1.2nH inductor to ground
WF_RF5G	37	I/O	WiFi 5G RF
WF_AUX5G	40	I	WiFi 5G RX Aux
BT_RF	44	I/O	BT RF
BT_IND	43		BT RF Ground, connect a 1.2nH inductor to ground
AVSS	35		Connect to the ground
AVSS	36		Connect to the ground
PMU			
AVDD	4		Need 1uF decoupling capacitor
AVDD	31		Need 1uF decoupling capacitor
AVDD	41		Need 1uF decoupling capacitor
AVDD18	5		Power output 1.8v, internal Efuse supply voltage, connect a 1uF decoupling capacitor
V_CORE	10		Need 1uF decoupling capacitor, connect to pin23
V_CORE	23		Digital Supply Voltage
VIO	7	I	IO Power Supply, Support 1.8v/3.3v
VBAT	24	I	System power supply
SW	25	O	Power Output For V_RF
V_RF	27	I	RF Supply Voltage
VDD33_PA	33	I	PA Supply Voltage
PWR_WF	34	I	WiFi system enable
PWR_BT	45	I	BT system enable
DVDD_BT	42		Need 1uF decoupling capacitor
CLK			
XTAL0	6	I	40M Crystal In
GPIO			
GPIOA0	32	I/O	GPIO
GPIOA1	30	I/O	GPIO
GPIOA2	29	I/O	GPIO
GPIOA3	28	I/O	GPIO
GPIOA4	46	I/O	GPIO
GPIOA5	47	I/O	GPIO
GPIOA6	48	I/O	GPIO
GPIOA7	1	I/O	GPIO
GPIOA8	2	I/O	GPIO
GPIOA9	3	I/O	GPIO
GPIOA10	22	I/O	GPIO
GPIOA11	21	I/O	GPIO
GPIOA12	20	I/O	GPIO
GPIOA13	19	I/O	GPIO
GPIOA14	18	I/O	GPIO
GPIOA15	17	I/O	GPIO
GPIOB0	26	I/O	GPIO
USB_DP	8	I/O	USB

TERMINAL			DESCRIPTION
PIN NAME	QFN NO.	I/O	
USB_DM	9	I/O	USB
PCIE_CLK_N	11	I/O	
PCIE_CLK_P	12	I/O	
PCIE_TX_N	13	I/O	Need a 100nF capacitor in series
PCIE_TX_P	14	I/O	Need a 100nF capacitor in series
PCIE_RX_N	15	I/O	
PCIE_RX_P	16	I/O	

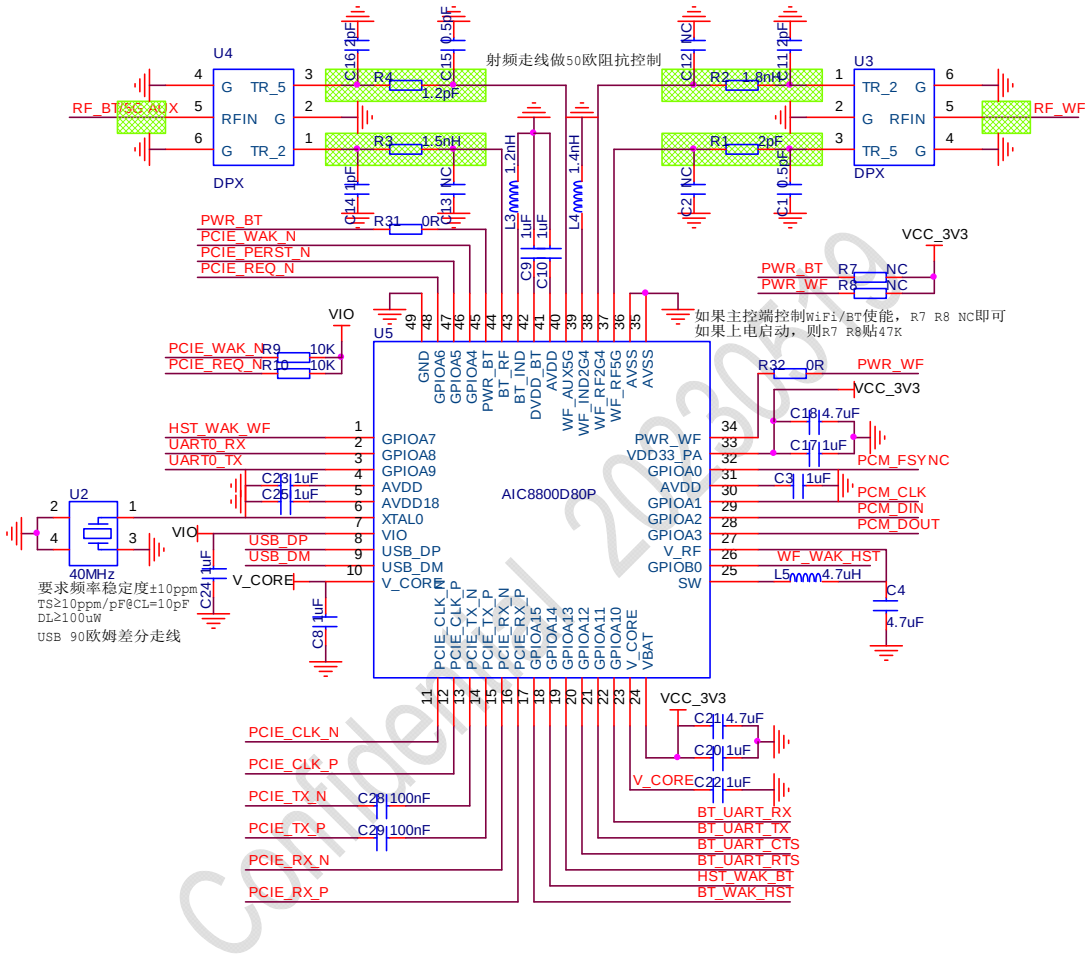
4. Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

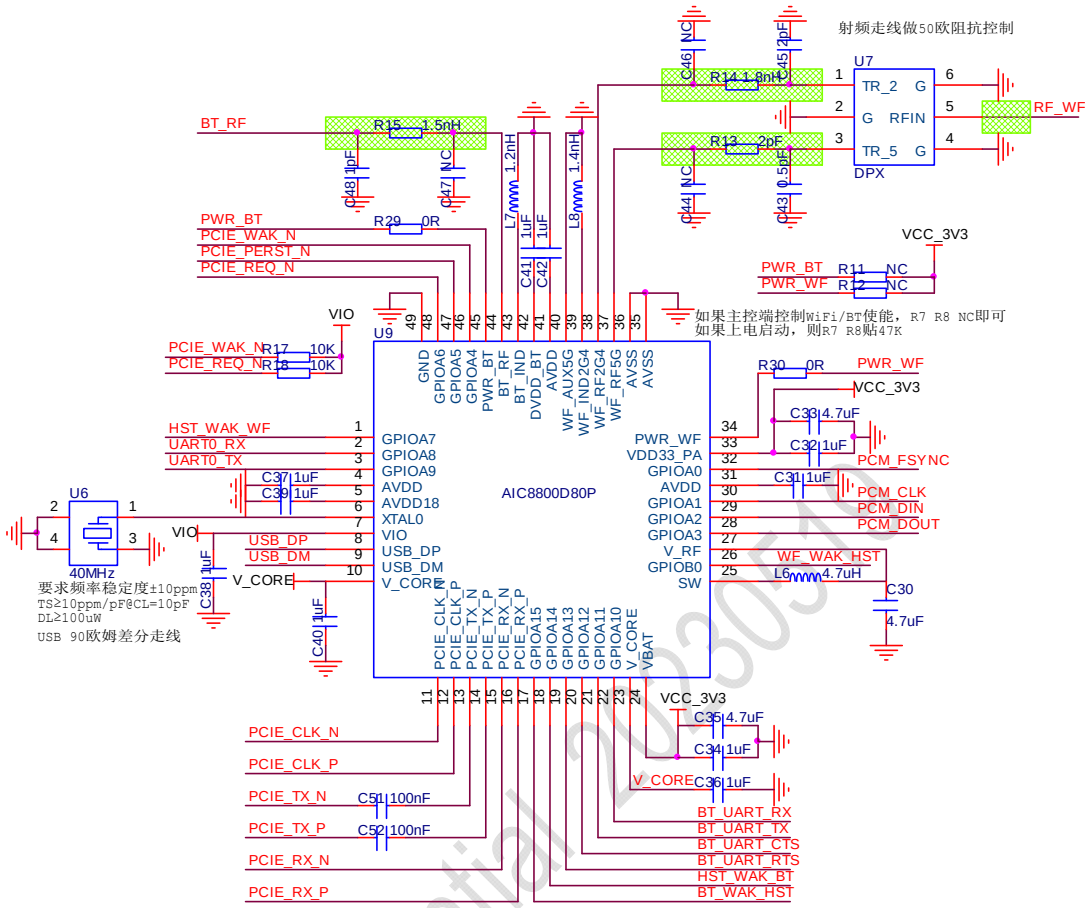
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VBAT	Supply Voltage for System	3	3.3	3.6	V
V_RF	Supply Voltage from SW_RF	1.0	1.3	1.5	V
V_CORE	Internal power supply for V_CORE	0.81	0.9	1.05	V
VDD33_PA	Supply Voltage for PA	3	3.3	3.6	V
AVDD18	Internal power supply for Efuse	1.69	1.8	2.49	V
DVDD_BT	Internal power supply for BT RF	1	1.15	1.5	V
AVDD	Connected with V_RF inside the chip	1.0	1.3	1.5	V
T_{amb}	Ambient Temperature	-20	27	+80	℃
T_{store}	Store Temperature	-55		+125	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VIO	V
V_{IH}	CMOS High Level Input Voltage	0.7*VIO		VIO	V
V_{TH}	CMOS Threshold Voltage		0.5*VIO		V

5. Application Circuit

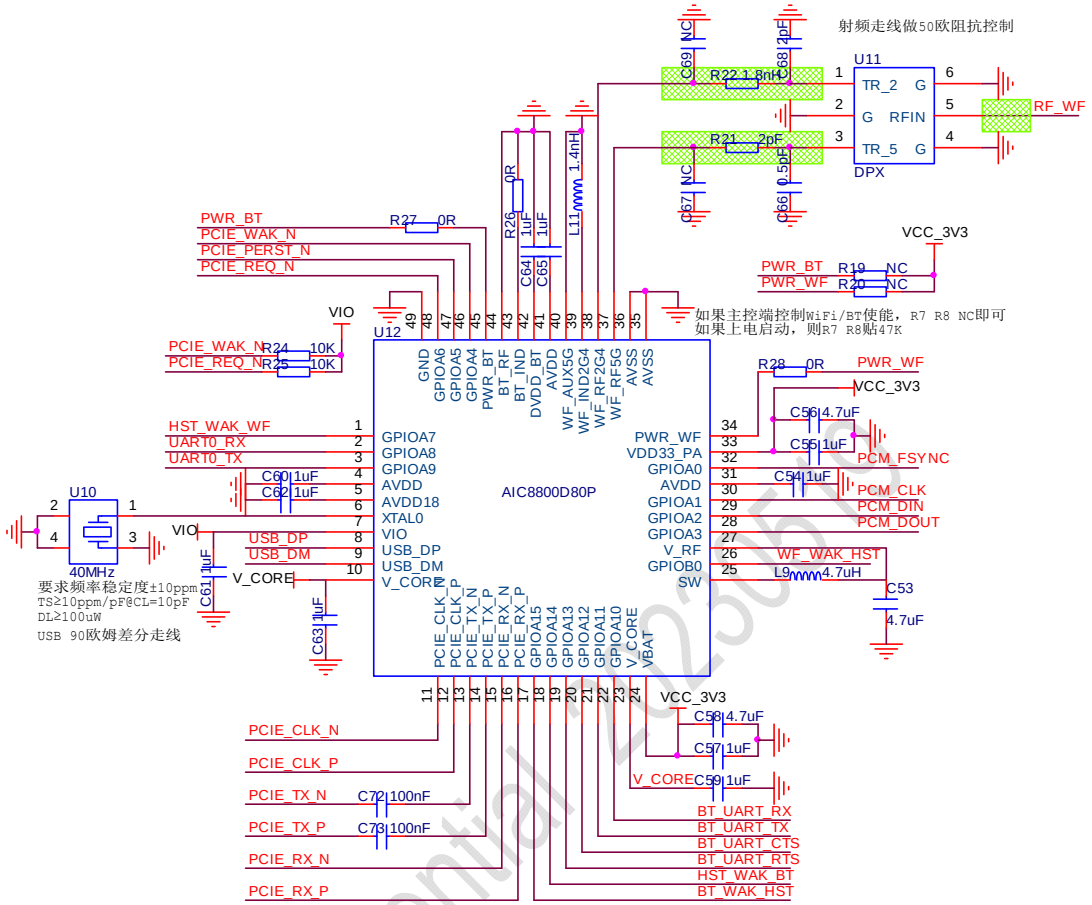
5.1 General design



5.2 General design no AUX5G

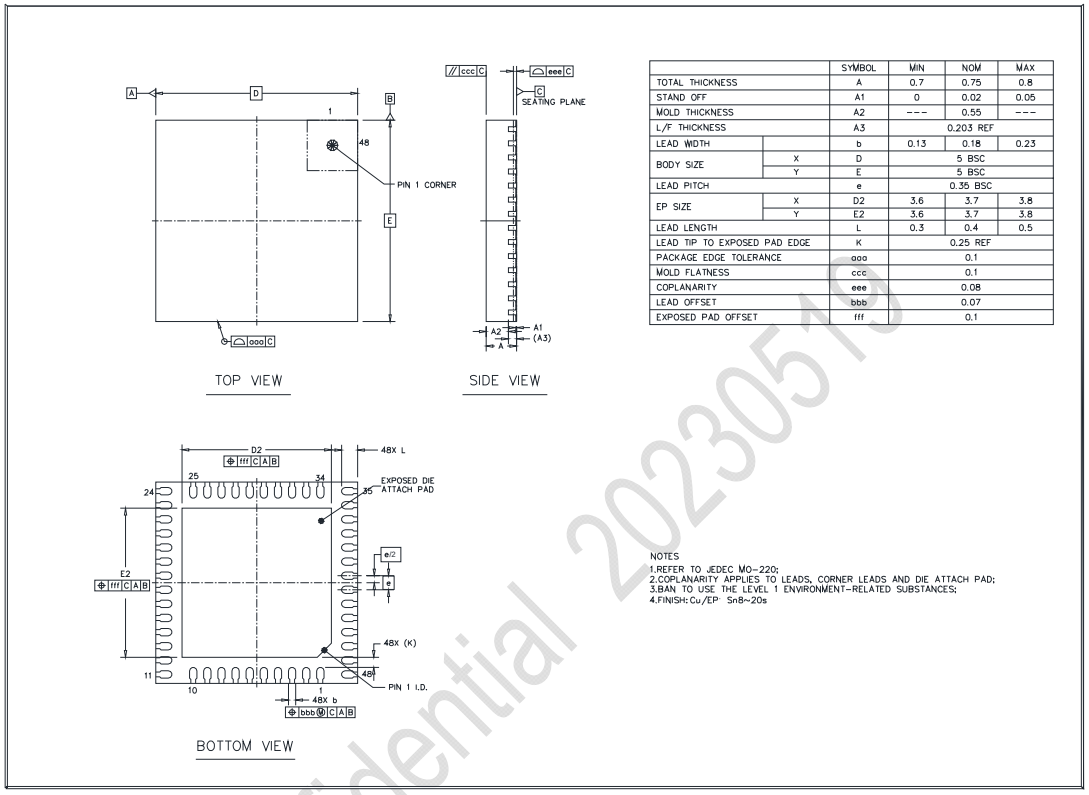


5.3 Co-ant design



6. Package Physical Dimension

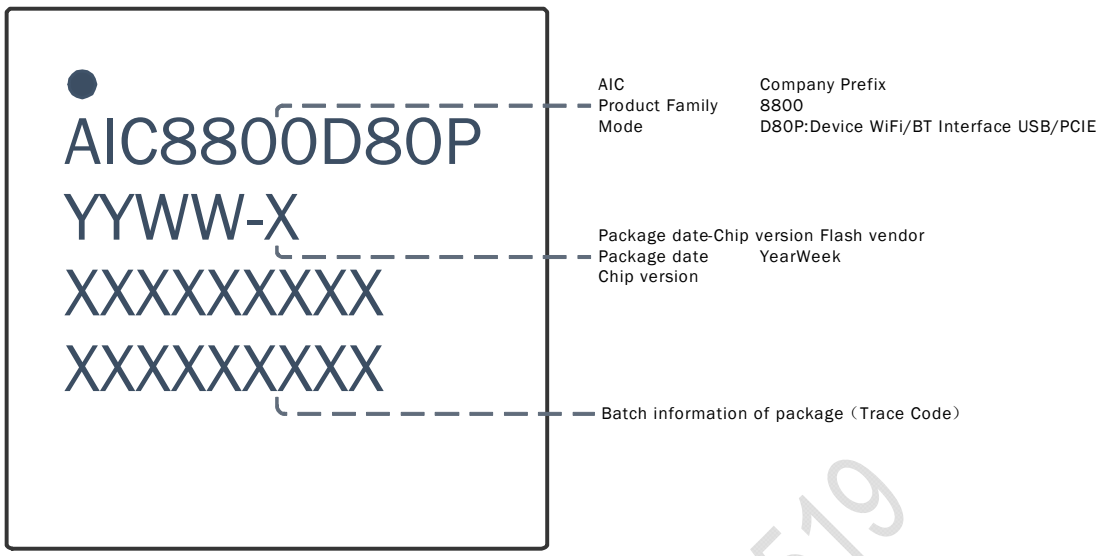
6.1 Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	3.6	3.7	3.8
	Y	E2	3.6	3.7	3.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP Sn8~20s

6.2 Product Identification



	Band	BW	5G Fem	Package	Type	BT	Interface	Flash
D80	2.4G/5.8G	20/40/80	Integration	5x5 QFN48	Device	BTDM5.4	USB2.0/SDIO3.0	No
D80L	2.4G/5.8G	20/40/80	Integration	5x5 QFN48	Device	BLE5.4	USB2.0/SDIO3.0	No
D40	2.4G/5.8G	20/40	Integration	5x5 QFN48	Device	BTDM5.4	USB2.0/SDIO3.0	No
D40L	2.4G/5.8G	20/40	Integration	5x5 QFN48	Device	BLE5.4	USB2.0/SDIO3.0	No
D80P	2.4G/5.8G	20/40/80	Integration	5x5 QFN48	Device	BTDM5.4	USB2.0/PCIE	No
M80	2.4G/5.8G	20/40/80	Integration	5x5 QFN48	MCU	BTDM5.4	USB2.0/SDIO3.0	Integration
M80F	2.4G/5.8G	20/40/80	Integration	5x5 QFN48	MCU	BTDM5.4	USB2.0/SDIO3.0	External
M40	2.4G/5.8G	20/40	Integration	5x5 QFN48	MCU	BTDM5.4	USB2.0/SDIO3.0	Integration

7. Reliability characteristics

Table 7-1 Reliability test report

Test Items	Test Condition	Test Criteria
HTOL	Tj≥125℃ 2000hrs	JESD22-A108F
ESD	HBM:±3000V Class 2	JS-001-2017
	CDM:±800V Class C2b	JS-002-2018
Latch up	±800mA Class Ⅰ	JESD78
Solder ability	Steam aging:8hrs; 245℃, 5s	J-STD-002D-2013
High Temperature Storage	150℃ （1000h）	JESD22-A103
TCT	-65℃～ 150℃, Dwell=15min, 500/1000Cycles	JESD22-A104E-2014
uHAST	130 ℃ /85%RH/ 33.3psig/96hrs	JESD22-A118
PCT	121℃, 100%RH, 205 kPa, 96/168hrs	JESD22-A102E-2015
Moisture sensitivity level	Level 3 Bake:125℃,24hrs Soak:30℃,60%	J-STD-020D

8. Solder Reflow Profile

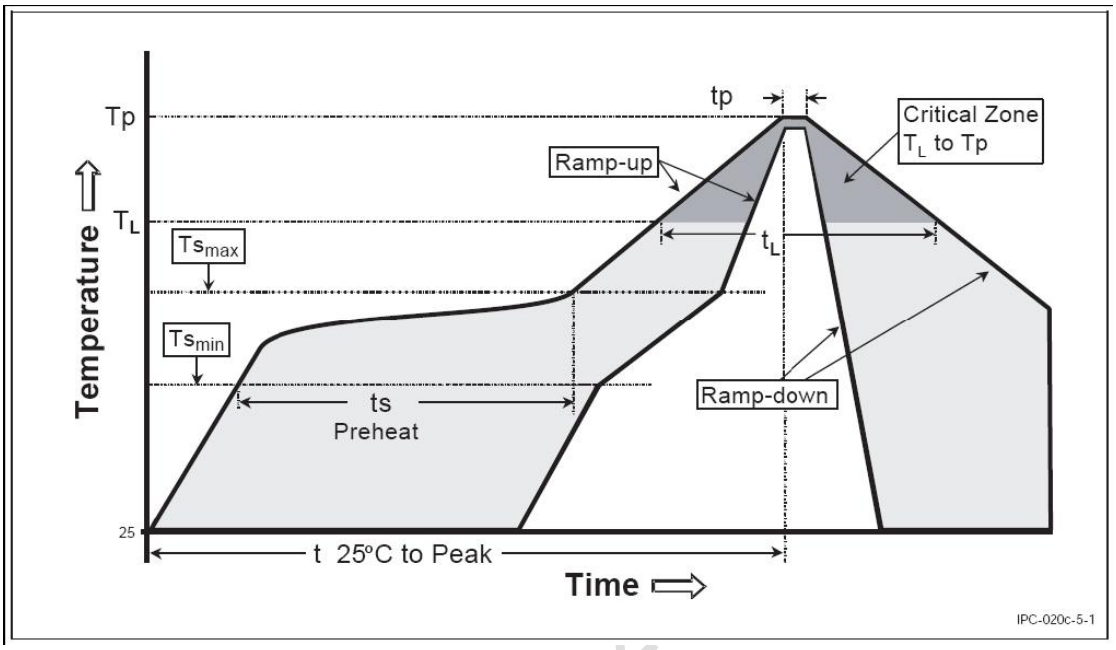


Figure8-1 Classification Reflow Profile

Table 8-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	3 ℃/second max.	3 ℃/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	 100 ℃ 100 ℃ 60-120 seconds	 150 ℃ 200 ℃ 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 183 ℃ 60-150seconds	 217℃ 60-150 seconds
Peak /Classification Temperature(Tp)	See Table 8-2	See Table 8-3
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 ℃/second max.	6 ℃/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 8-2 Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
＜2.5mm	240 + 0/-5 ℃	225 + 0/-5 ℃
≥2.5mm	225 + 0/-5 ℃	225 + 0/-5 ℃

Table 8-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 ＜350	Volume mm3 350-2000	Volume mm3 ＞2000
＜1.6mm	260 + 0 ℃ *	260 + 0 ℃ *	260 + 0 ℃ *
1.6mm – 2.5mm	260 + 0 ℃ *	250 + 0 ℃ *	245 + 0 ℃ *
≥2.5mm	250 + 0 ℃ *	245 + 0 ℃ *	245 + 0 ℃ *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 ℃. For example 260+ 0 ℃) at the rated MSL Level.			

Note 1: All temperature refers topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ℃, - X ℃ (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 ℃. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 11-3.

Note 3: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package maysill exist.

Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table8-1, 8-2, 8-3 whether or not lead free.

9. Change List

The following table summarizes revisions to this document.

REV	DATE	AUTHER	CHANGE DESCRIPTION
V0.1	20220808	AICSEMI	Initial version
V1.0	20230519	AICSEMI	

10. RoHS Compliant

The products meet the requirements of Directive 2011/65/EU of Europe Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). The products are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals.

11. ESD Sensitivity

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site. BES products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment.

12 Disclaimer

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