AIC8800D80X2P

Preliminary Low-Energy WiFi6/BTDM5.4 SoC
Data Sheet.

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version 1.0.2
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Contents

1 General Description

AIC8800D80X2P is a 22nm, highly integrated SoC with 2T2R dual band WiFi6, BTDM 5.4 and high performance Wlan CPU for wireless application. It provides miniaturized solutions that reduce design costs with minimal material.

1.1 WiFi Features

- CMOS single-chip fully-integrated RF, Modem and MAC

- Intergrated PA LNA and Tx/Rx switch

- Supports 2.4GHz/5GHz WiFi6

- Supports 2.4GHz/5GHz band, the 5G band includes U-NII-1 U-NII-2A U-NII-2C and U-NII-3

- Physical data rates up to 1201.0Mbps with 20/40/80MHz bandwidth

- Supports 802.11a/b/g/n/ac/ax

- Supports 2 spatial stream transmission and high performance reception

- Supports 2 Rx maximum rejection combining receiver for all modes

- Supports STA, AP, Wi-Fi Direct modes concurrently

- Supports STBC

- Supports beamforming as beamformee up to 4x2

- Supports WiFi6 TWT

- Supports Two NAV, Buffer Report, Spatial reuse, Multi-BSSID, intra-PPDU power save

- Supports LDPC

- Supports downlink MU-MIMO, OFDMA

- Supports uplink MU-MIMO, OFDMA

- Supports ER, DCM, Mid-amble, UORA

- Supports WEP/WPA/WPA2/WPA3-SAE Personal, WAPI

- Supports IEEE 802.11d/w/k/r/v/e/h/i

1.2 BTDM5.4 Features

- Complies with Bluetooth Core Specification Version 5.4 with provisions for supporting future specifications

- Supports all the mandatory and optional features of Bluetooth low energy 5.4

- Supports advanced master and slave topologies

- Supports BR/EDR/BLE (1/2Mbps/LongRange S2/8)

- Bluetooth Class 1 Class 2 or Class3 transmitter operation

- Bluetooth Low Energy Class 1 Class 1.5 Class 2 or Class3 transmitter operation

- Supports BLE audio

- Host controller interface (HCI) using a high-speed UART interface

- PCM for audio data

- Adaptive frequency hopping (AFH) for reducing radio frequency interference

1.3   Other Features

- Supports PCIE2.0/PCIE1.0/USB2.0/HCI_UART/PCM interface

- Integrated low power timer and watchdog

- 1024 bits Efuse

1.4   Packaging Information

- Compact profile package 6mm×6mm×0.75mm QFN60

1.5   Application

- IOT device

- Wireless device

2 Platform Description
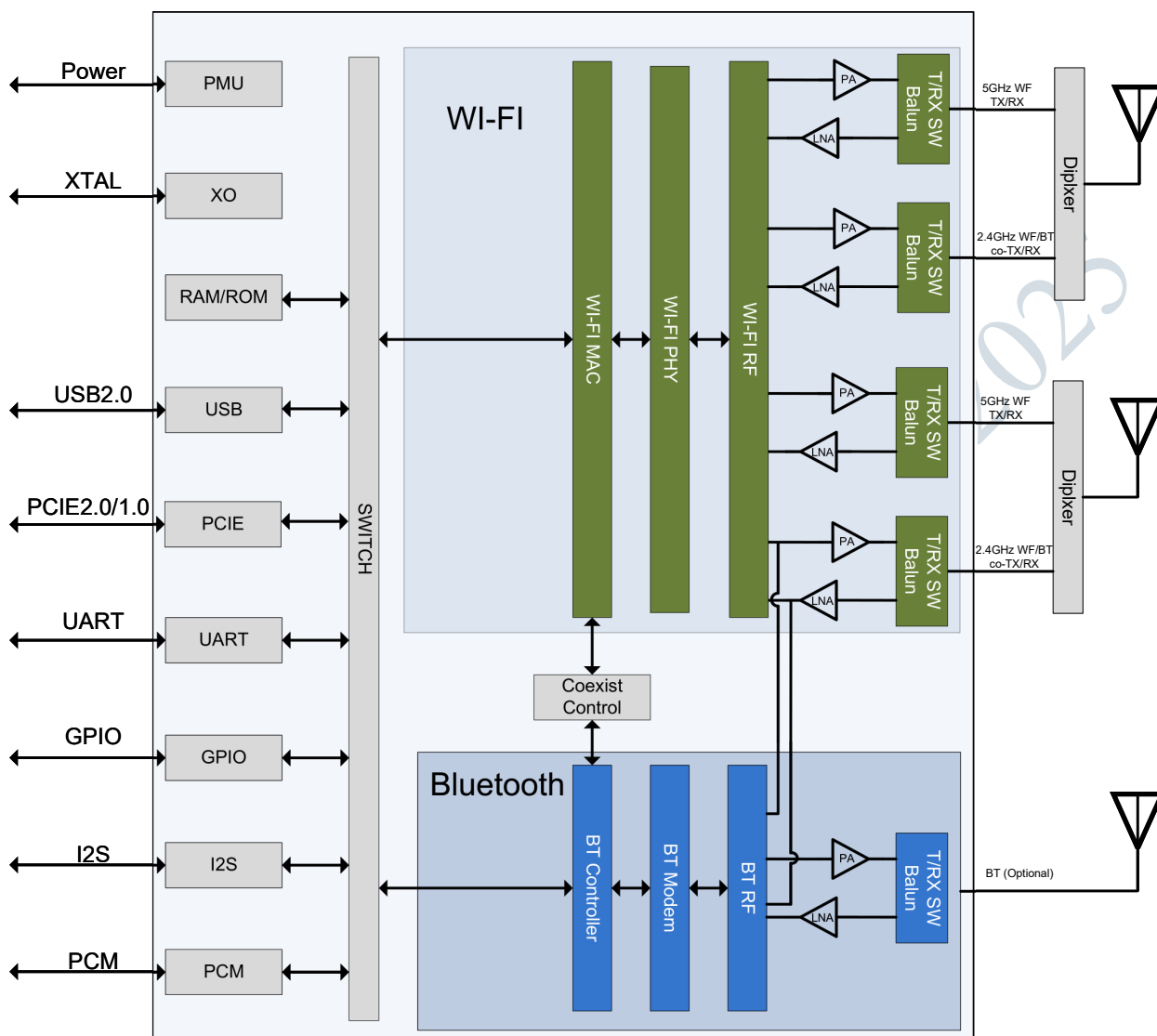
Figure 1: AIC8800D80X2P Block Diagram

3   Pins Description
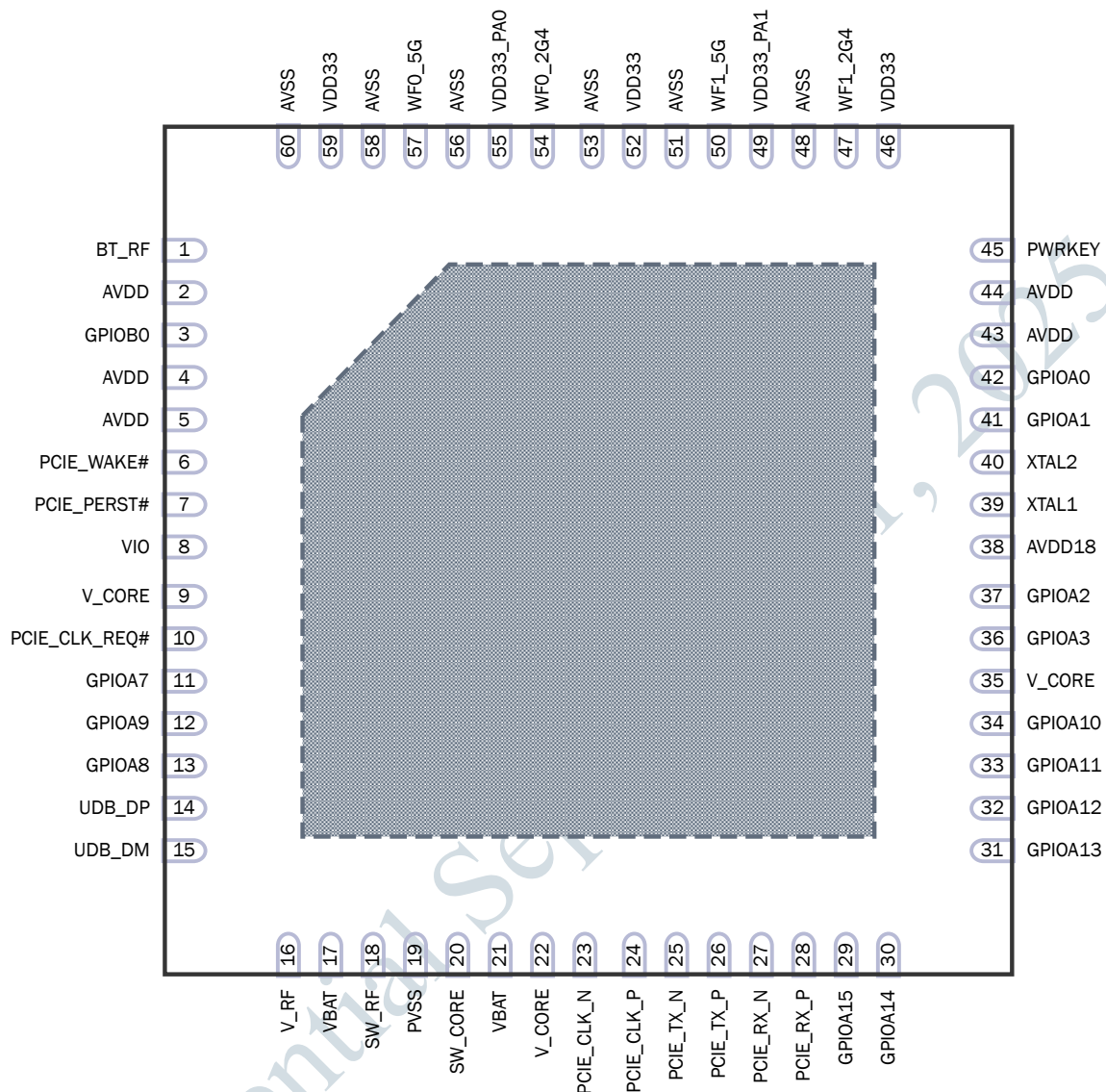
Figure 2: AIC8800D80X2P Pin Map

Table 1: AIC8800D80X2P Pin Description

Pin Name	QFN NO.	I/O	Description
RF			
BT_RF	1	I/O	BT RF IO
WF1_2G4	47	I/O	WF1 2.4G RF IO
WF1_5G	50	I/O	WF1 5G RF IO
WF0_2G4	54	I/O	WF1 2.4G RF IO, shared with BT in co-antenna mode
WF0_5G	57	I/O	WF0 5G RF IO
AVSS	48		Connect to the ground
AVSS	51		Connect to the ground
AVSS	53		Connect to the ground
AVSS	56		Connect to the ground
AVSS	58		Connect to the ground

Table 1: AIC8800D80X2P Pin Description

Pin Name	QFN NO.	I/O	Description
AVSS	60		Connect to the ground
EPAD	61		EPAD, connect to the ground via mutiple holes, ensure the chip to work properly and heat dissipation
PMU			
AVDD	2	I	BT power supply, connect the inductor which connect pin18 and a capacitor, please connect the net of the capacitor
AVDD	4	I	WF0 power supply, connect the inductor which connect pin18, please connect the net of the capacitor and a capacitor
AVDD	5	I	WF ABB power supply, connect the inductor which connect pin18, please connect the net of the capacitor and a capacitor
V_CORE	9	I	Connect the inductor which connect pin20 and a capacitor, please connect the net of the capacitor and a capacitor
V_RF	16	I	Connect the inductor which connect pin18 and a capacitor
VBAT	17	I	Connect a 4.7uF decoupling capacitor closely and 3.3V power supply
SW_RF	18	O	Connect a 2.2uH inductor closely, and a 10uF capacitor connect the other side of the inductor
PVSS	19		Connect to the ground
SW_CORE	20	O	Connect a 2.2uH inductor closely, and a 10uF capacitor connect the other side of the inductor
VBAT	21	I	Connect a 4.7uF decoupling capacitor closely and 3.3V power supply
V_CORE	22	I	Connect the inductor which connect pin20 and a capacitor
VIO	8	I	VIO power supply, support 1.8/3.3v, connect a 1uF capacitor closely
V_CORE	35	I	Connect the inductor which connect pin20 and a capacitor, please connect the net of the capacitor and a capacitor
AVDD18	38	O	1.8v power supply for XTAL and EFUSE
AVDD	43	I	Power supply for RF clock and LO, connect the inductor which connect pin18, please connect the net of the capacitor and a capacitor
AVDD	44	I	WF1 power supply, connect the inductor which connect pin18, please connect the net of the capacitor and a capacitor
PWRKEY	45	I	Chip enable, active high
VDD33	46	I	WF1 2.4G TX 3.3v power supply
VDD33_PA1	49	I	WF1 2.4/5G PA 3.3v power supply
VDD33	52	I	WF0 2.4G and WF1 5G TX 3.3v power supply
VDD33_PA0	55	I	WF0 2.4/5G PA 3.3v power supply
VDD33	59	I	BT and WF0 5G TX 3.3v power supply
CLK			

Table 1: AIC8800D80X2P Pin Description

Pin Name	QFN NO.	I/O	Description
XTAL1	39	I	40M Crystal In
XTAL2	40		Connect to the ground
GPIO			
GPIOA0	42	I/O	GPIO
GPIOA1	41	I/O	GPIO
GPIOA2	37	I/O	GPIO
GPIOA3	36	I/O	GPIO
GPIOA7	11	I/O	GPIO
GPIOA8	13	I/O	GPIO
GPIOA9	12	I/O	GPIO
GPIOA10	34	I/O	GPIO
GPIOA11	33	I/O	GPIO
GPIOA12	32	I/O	GPIO
GPIOA13	31	I/O	GPIO
GPIOA14	30	I/O	GPIO
GPIOA15	29	I/O	GPIO
GPIOB0	3	I/O	GPIO☐ pull down this pin when power on, the chip will be boot mode
PCIE_WAKE#	6	I/O	PCIE WAKE Open Drain with pull up on platform, active low
PCIE_PERST#	7	I	PCIE Reset, active low
PCIE_CLK_REQ#	10	I/O	Reference clock request signal, active low
PCIE_CLK_N	23	I	PCIE reference clock signals(100MHz)
PCIE_CLK_P	24	I	PCIE reference clock signals(100MHz)
PCIE_TX_N	25	O	PCIE TX differential signals, a series 100nF capacitor is required
PCIE_TX_P	26	O	PCIE TX differential signals, a series 100nF capacitor is required
PCIE_RX_N	27	I	PCIE RX differential signals
PCIE_RX_P	28	I	PCIE RX differential signals
USB_DP	14	I/O	USB data positive
USB_DM	15	I/O	USB data minus

4 Electrical Characteristics

4.1 DC Electrical Specification

Table 2: DC Electrical Specification

Symbol	Description	MIN	TYP	MAX	Unit
VBAT	Supply Voltage for System	3.0	3.3	3.6	V
V_RF	Supply Voltage for V_RF	1.26	1.4	1.54	V
V_CORE	Internal power supply for V_CORE	0.6	0.9	1.0	V
VDD33	Supply Voltage for WF0/1 2.4G/5G TX abd BT	3.0	3.3	3.6	V
VDD33_PA0	Supply Voltage for WF0 2.4G/5G PA	3.0	3.3	3.6	V
VDD33_PA1	Supply Voltage for WF1 2.4G/5G PA	3.0	3.3	3.6	V
AVDD18	Internal power supply for XTAL and Efuse	1.8	2.0	2.2	V
AVDD	Connected with V_RF	1.26	1.4	1.54	V
VIO	Supply Voltage for VIO, VIO=1.8V	1.71	1.8	1.89	V
	Supply Voltage for VIO, VIO=3.3V	3.135	3.3	3.465	V

4.2 Absolute Maximum Ratings

The absolute maximum ratings in Table 4 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 3: Environmental rating

Rating	Symbol	Value	Uint
DC supply for the VBAT	VBAT	-0.5 to +3.9	V
DC supply for the WF TX and BT	VDD33	-0.5 to +3.9	V
DC supply for the WF0 PA	VDD33_PA0	-0.5 to +3.9	V
DC supply for the WF1 PA	VDD33_PA1	-0.5 to +3.9	V
DC supply for the GPIO	VIO	-0.5 to +3.9	V

4.3 Environmental ratings

Table 4: Environmental rating

Symbol	Description	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	-20	27	80	°C
T_{store}	Store Temperature	-40		125	°C
Relative Humidity	Operation			85	%
	Storage			60	%

5 Power Management Unit

5.1 Description

Two Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the AIC8800M80X2P. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.
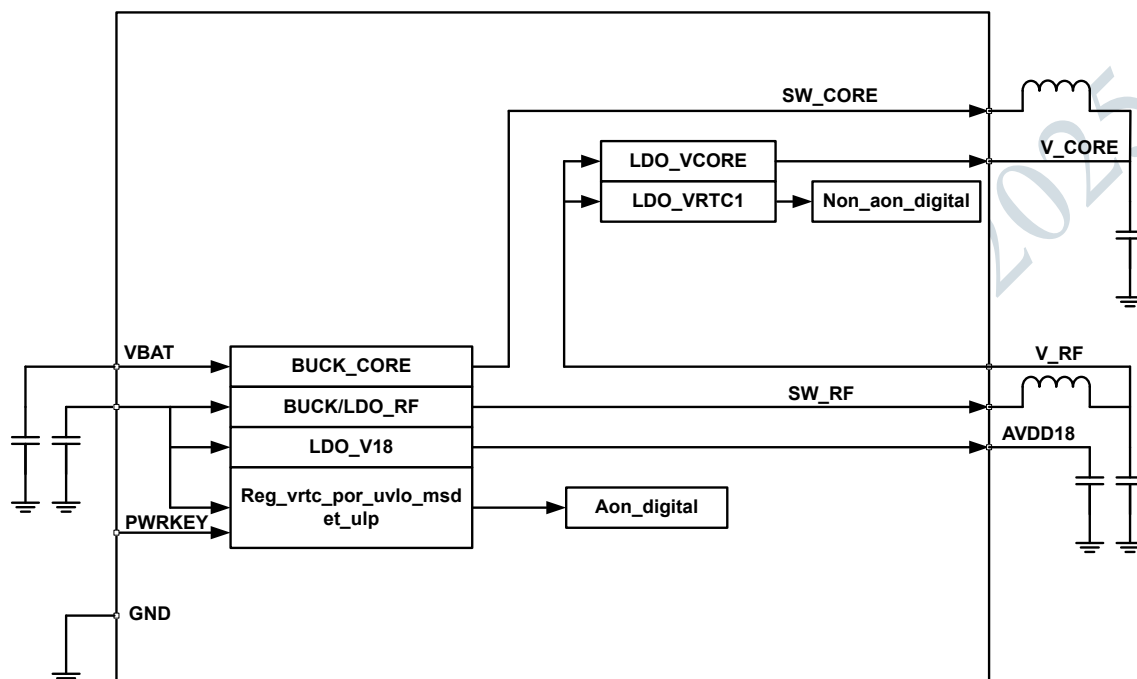
Figure 3: AIC8800D80X2P PMU Diagram

5.2 PMU Features

- VBAT to 1.4Vout (1000 mA maximum) V_RF Buck switching regulator or LDO

- VBAT to 2Vout (100 mA maximum) AVDD18

- VBAT to 0.9Vout (1000 mA maximum) V_CORE Buck switching regulator

- 1.4V to 0.9Vout (500 mA maximum) V_CORE LDO

- Additional internal LDOs (not externally accessible)

- PMU internal timer auto calibration by the crystal clock for precise wake up timing from low power modes

5.3 V_RF Buck Switching Regulator

Table 5: V_RF Buck Switching Regulator Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage	Min value is Limited BY UVLO	3.0	3.3	3.6	V
PWM mode switching frequency	-		2.5		MHz
PWM output current	-	-	-	1000	mA
Output voltage range	Programmable, 25 mV steps. Default=1.4V	-	1.4	-	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM. Before trimming	-10	-	10	%
PWM ripple voltage, static	Measure with 20MHz bandwidth limit. Static Load. VBAT=3.3V, Vout=1.4V, Fsw=2.5MHz, L=2.2uH effective, Cap+Board total-ESR<20 mΩ, Cout=10uF, Cout ESL<200pH	-	4.5	-	mVpp
PWM mode peak efficiency	Peak Efficiency at 450mA load Fsw=2.5MHz PWM, L=2.2uH effective inductor DCR=80mΩ	-	85	-	%
External inductor	2.2uH, DCR≤100mΩ, Isat≥700mA, Irms≥1A	-	2.2	-	uH
External output capacitor	Ceramic, X5R, ESR<20mΩ at 4MHz, 10uF±20%, 6.3V	-	10	-	uF
External input capacitor	For VBAT pin, ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V	-	4.7	-	uF

5.4 V_CORE Buck Switching Regulator

Table 6: V_CORE Buck Switching Regulator Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage	Min value is Limited BY UVLO	3.0	3.3	3.6	V
PWM mode switching frequency	-		2.5		MHz
PWM output current	-	-	-	1000	mA
Output voltage range	Programmable, 25 mV steps. Default=0.9V	-	0.9	-	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM. Before trimming	-10	-	10	%
PWM ripple voltage, static	Measure with 20MHz bandwidth limit. Static Load. VBAT=3.3V, Vout=0.9V, Fsw=2.5MHz, L=2.2uH effective, Cap+Board total-ESR<20 mΩ, Cout=10uF, Cout ESL<200pH	-	3.6	-	mVpp
PWM mode peak efficiency	Peak Efficiency at 350mA load Fsw=2.5MHz PWM, L=2.2uH effective inductor DCR=80mΩ	-	85	-	%
External inductor	2.2uH, DCR≤100mΩ, Isat≥700mA, Irms≥1A	-	2.2	-	uH
External output capacitor	Ceramic, X5R, ESR<20mΩ at 4MHz, 10uF±20%, 6.3V	-	10	-	uF
External input capacitor	For VBAT pin, ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V	-	4.7	-	uF

5.5 AVDD18

Table 7: AVDD18 Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, Vin	Min value is Limited BY UVLO	3.0	3.3	3.6	V
Output current	-	-	-	100	mA
Output voltage range, Vo	Programmable in 0.1V steps. Default=2V	-	2	-	V
Dropout voltage	At max. load	-	-	200	mV
Output voltage DC accuracy	Includes line/load regulation, before trimming	-10	-	10	%
Quiescent current	No load	-	15	-	uA
	Max load at 100 mA	-	1.1	-	mA
Line regulation	Vin from 3.0V to 3.6V, max load	-	-	3.5	mV/V
Load regulation	Load from 1mA to 100mA, Vin=3.3V	-	-	0.3	mV/mA
PSRR	Vin=3.3V, Vo=2.0V, Co=1uF, Max load, 100Hz to 100kHz	20	-	-	dB
LDO turn on time	Reference ready. Vo from 0 to 2.0V, Co=1uF	-	30	-	us
Output over current limit	-	120	-	-	mA
External output capacitor, Co	Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V	1	-	2.2	uF
External input capacitor	For VBAT pin, ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V	-	4.7	-	uF

5.6 V_CORE LDO

Table 8: V_CORE LDO Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, Vin	Min=Vo+0.25V=1.15V dropout voltage requirement must be met under maximum load for performance specifications	1.2	1.4	1.6	V
Output current	-	0.1	-	500	mA
Output voltage range, Vo	Programmable in 18mV steps. Default=0.9V	0.6	0.9	1	V
Dropout voltage	At max load	-	-	300	mV
Output voltage DC accuracy	Includes line/load regulation, before trimming	-10	-	10	%
Quiescent current	No load	-	28	-	uA
	500mA load	-	2.5	-	mA
Line regulation	Vin from 1.2V to 1.6V, max load	-	-	30	mV/V
Load regulation	Load from 1mA to 500mA, Vin=1.4V	-	-	0.03	mV/mA
Leakage current	Power down, Vin=1.4V, typical at Tj=25°C	-	12.3	-	uA
	Power down, Vin=0.9V, typical at Tj=25°C	-	3.8	-	uA
PSRR	100Hz to 100kHz, Vin≥1.4V, Co=1uF	20	-	-	dB
LDO turn on time	Reference ready. Vo from 0 to 0.9V, Co=1uF	-	13	-	us
External output capacitor, Co	Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V	1	-	-	uF

5.7 PWRKEY

PWRKEY, is used to power up the regulators and take the respective section out of reset. The V_RF and V_CORE power up when the reset signals are deasserted. All regulators are powered down only when PWRKEY is deasserted.

Table 9: PWRKEY Electrcal Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	VIH	For Chip ON pin	1.25	-	3.6	V
Input low voltage	VIL	-	VSS	-	0.55	V
Pull down resistance (Internal)	PRD	-	-	200	-	kΩ
REG ON time	TREG_ON	-	8	-	-	ms
REG OFF time	TREG_OFF	-	6	-	-	ms
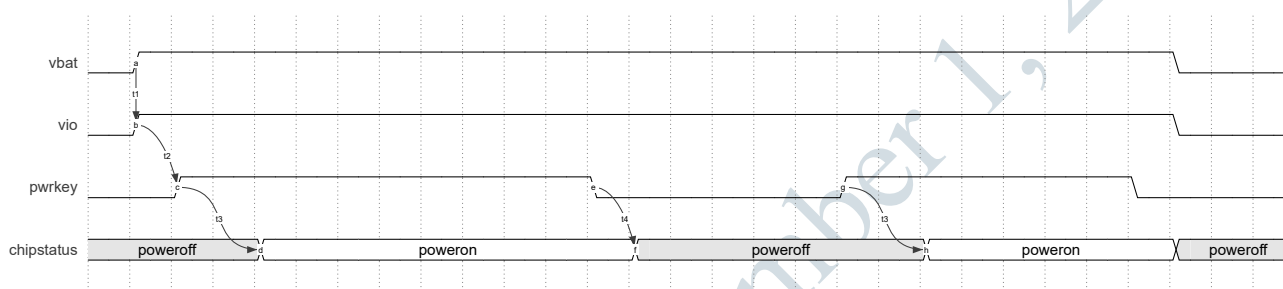
Figure 4: AIC8800D80X2P Power ON/OFF Timing

Table 10: Power ON/OFF Specifications

Symbol	Discription	Min	Typ	Max	Unit
t1	VIO's power time ≥ VBAT's	0	-	-	ms
t2	PWRKEY's high time ≥ VIO's	0	200	-	us
t3	Chip all power on ready time	-	8	-	ms
t4	Hold PWRKEY low for a sufficient amount of time to ensure that the chip is completely shut down	6	-	-	ms

Note: In practical applications where VIO=1.8V, if the VIO is powered on earlier than VBAT, there is no problem for the chip

6 External Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. Colpitts type oscillator circuits is adopted to provide high quality reference clock. Only one lead pin is required and external load capacitors are saved. The table below lists the requirement for the crystal unit.
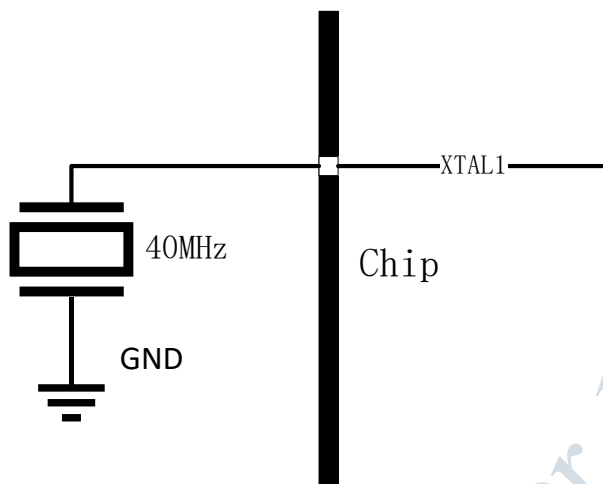
Figure 5: Colpitts mode

Table 11: Colpitts mode crystal requirement and performance

Symbol	Parameter	Value	Note
F0	Nominal Frequency	40MHz	
ΔF/F0	Frequency Tolerance	$\pm$10ppm	@25 °C$\pm$3 °C
TC	Frequency Stability	$\pm$10ppm	Over Operating Temp. Range (Reference 25 °C)
ESR	Equivalent Series Resistance	$<$40Ω	
CL	Load Capacitance	10pF	
TS	Pulling Sensitivity	$\geq$15ppm/pF	
DL	Drive Level	$>$200uW	
Amp	Oscillation Amplitude	$>$2Vpp	Oscilloscope probe input capacitance $<$1pF

7 Interface

AIC8800D80X2P supports a variety of data interfaces.

7.1 PCIE

7.1.1 Description

In the PCIE wireless network adapter application, the data of WiFi is transmitted through the PCIE, the data of Bluetooth is transmitted through the USB/UART, and the audio data can be transmitted either USB/UART/PCM.
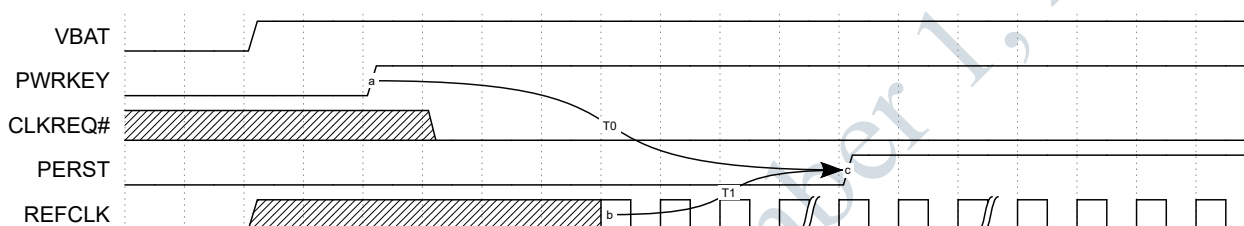The AIC8800D80X2P WLAN section support for PCIE version 2.0 and 1.0.

7.1.2 PCIE Timing

Figure 6: PCIE Timing

T0: T0>20ms, recommended 50ms.
T1: T1>100us

Table 12: REFCLCK DC Specifications and AC Timing Requirements

Symbol	Parameter	100MHz Input		Unit
		Min	Max	
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns
V_{IH}	Differential Input High Voltage	+150		mV
V_{IL}	Differential Input Low Voltage		-150	mV
V_{CROSS}	Absolute crossing point Voltage	+250	+550	mV
$V_{CROSSDELTA}$	Variation of Vcross over all rising clock edges		+140	mV
V_{MAX}	Absolute Max input voltage		+1.3	V
V_{MIN}	Absolute MIN input voltage		0	V
Duty Cycle	Duty Cycle	40	60	%

7.2 USB2.0

7.2.1 Description

In the USB application, the data of Bluetooth/WiFi is transmitted through the USB, and the audio data can be transmitted either USB or PCM.

The AIC8800D80X2P WLAN section support for USB version 2.0, the feature is as follow:

- Complies with USB Specification Revision 2.0 for WLAN and Bluetooth controller

- Supports up to 7 bidirectional endpoints, including control endpoint 0

- Supports packet-based, Dynamic FIFO memory allocation for endpoints for small FIFOs and flexible efficient use of RAM

- Supports endpoint FIFO sizes that are not powers of 2, to allow the use of contiguous memory locations
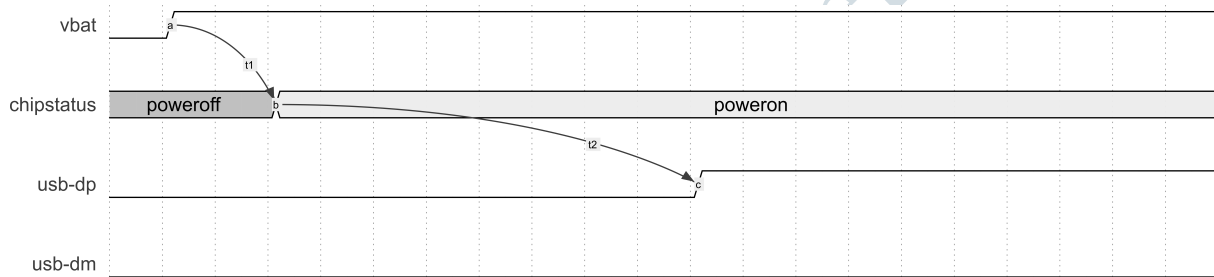
7.2.2 USB Timing

Figure 7: Powerup USB Initial

t1: chip all power on ready time $\geq$ power up time + 8ms.
t2: usb dp pull up time $\geq$ chip all power on ready time + 22ms

8 GPIO

AIC8800D80X2P has a total of 14 GPIO pins, including GPIOA0~3, GPIOA7~15 and GPIOB0. These GPIOs can be configured with registers for different functions.

8.1 Threshold

Table 13: IO Threshold

VIO	Symbol	IO Threshold
1.8V	V_{inh}	1.320V
1.8V	V_{inl}	0.470V
3.3V	V_{inh}	2.840V
3.3V	V_{inl}	0.300V

8.2 IO Assignment

8.2.1 General Application

In the general design, the chip pin assignment is referred to Table 14, the public driver cab be used directly.

Table 14: General IO Assignment

GPIO	Pin NO.	Assignment	Type	Description
GPIOA0	42	PCM_FSYNC	I/O	PCM sync signal, can be master (output) or slave (input)
GPIOA1	41	PCM_CLK	I/O	PCM clock, can be master (output) or slave (input)
GPIOA2	37	PCM_DIN	I	PCM data input
GPIOA3	36	PCM_DOUT	O	PCM data output
GPIOA10	34	BT_UART_RX	I	UART receive data
GPIOA11	33	BT_UART_TX	O	UART transmit data
GPIOA12	32	BT_UART_CTS	I	UART clear to send
GPIOA13	31	BT_UART_RTS	O	UART request to send
GPIOA8	13	UART_RX	I	Debug UART RX
GPIOA9	12	UART_TX	O	Debug UART TX
GPIOA14	30	BT_WAK_HST	O	BT Wake up host
GPIOA15	29	HST_WAK_BT	I	Host Wake up BT
GPIOA7	11	WF_WAK_HST	O	Wlan wake up host wlan
GPIOB0	3	HST_WAK_WF	I	Host wake up

8.3   IO Status

Table 15: Default Status of IO

GPIO	Pin NO.	Function	Type	Pull
GPIOA0	42	SW_CLK	I	UP
GPIOA1	41	SWD	I/O	UP
GPIOA2	37	GPIOA2	I/O	DN
GPIOA3	36	GPIOA3	O	DN
GPIOA7	11	GPIOA7	I/O	DN
GPIOA8	13	UART0_RX	I	UP
GPIOA9	12	UART0_TX	O	OFF
GPIOA10	34	GPIOA10	I/O	DN
GPIOA11	33	GPIOA11	I/O	DN
GPIOA12	32	GPIOA12	I/O	DN
GPIOA13	31	GPIOA13	I/O	DN
GPIOA14	30	GPIOA14	I/O	DN
GPIOA15	29	GPIOA15	I/O	DN
GPIOB0	3	GPIOB0	I/O	UP

I: Input signal

O: Output signal

I/O: Input/Output signal

UP: Pulled up (of 50KΩ)

DN: Pulled down (of 50KΩ)

OFF: Neither pulled up nor pulled down

9   Application Circuit

The AIC8800D80X2P Bluetooth RF design supports two modes, BT Only Mode and BT Coant Mode. The advantage of the BT Only Mode is that it can operate simultaneously with WiFi 2.4G, Combined with AIC's excellent coexistence design, it can provide higher throughput and superior Bluetooth performance. The advantage of the BT Coant Mode is that it saves space and cost, BT_RF NC when Coant mode was selected.
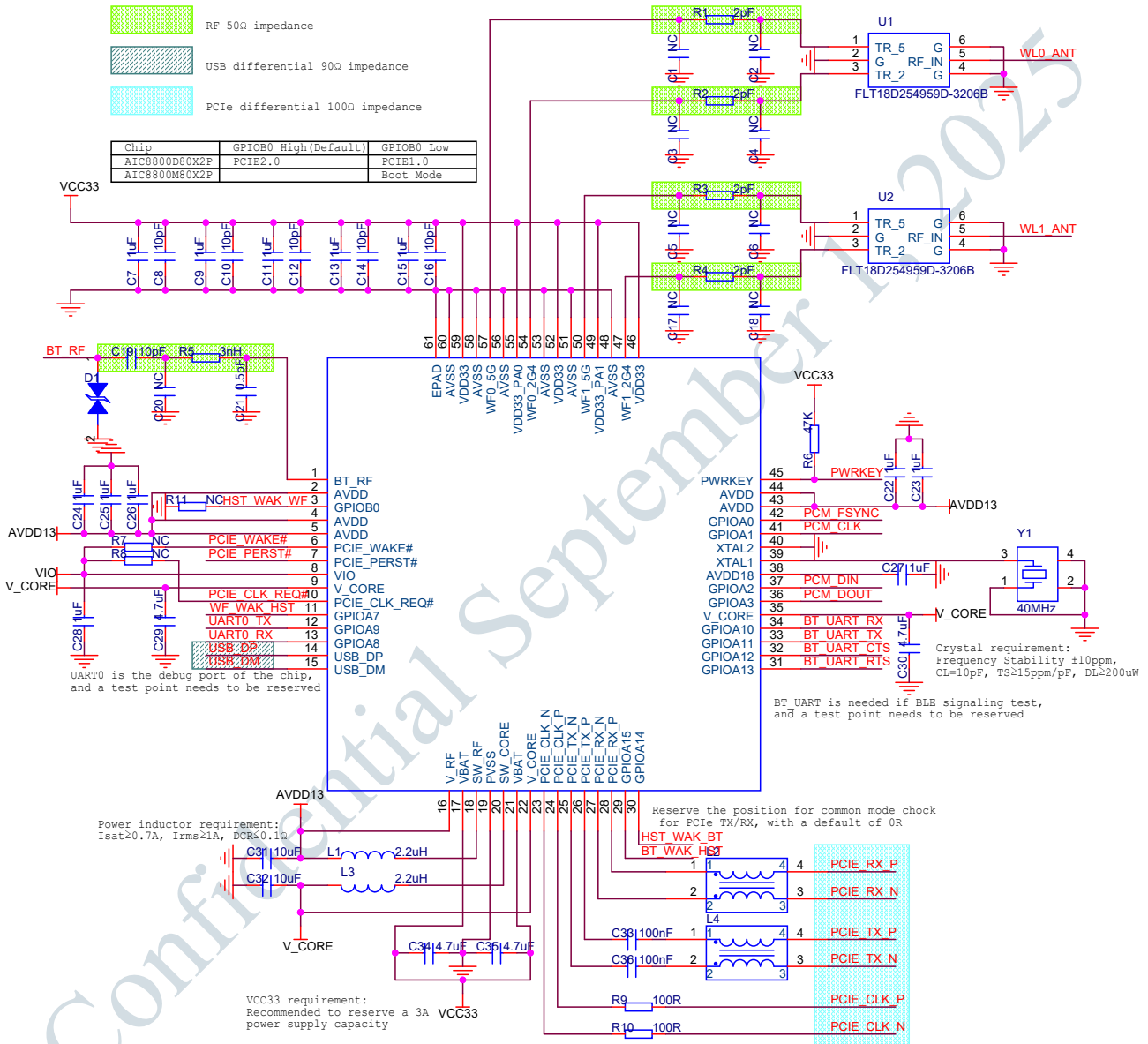

Figure 8: AIC8800D80X2P Application Circuit

10 Package Physical Dimension
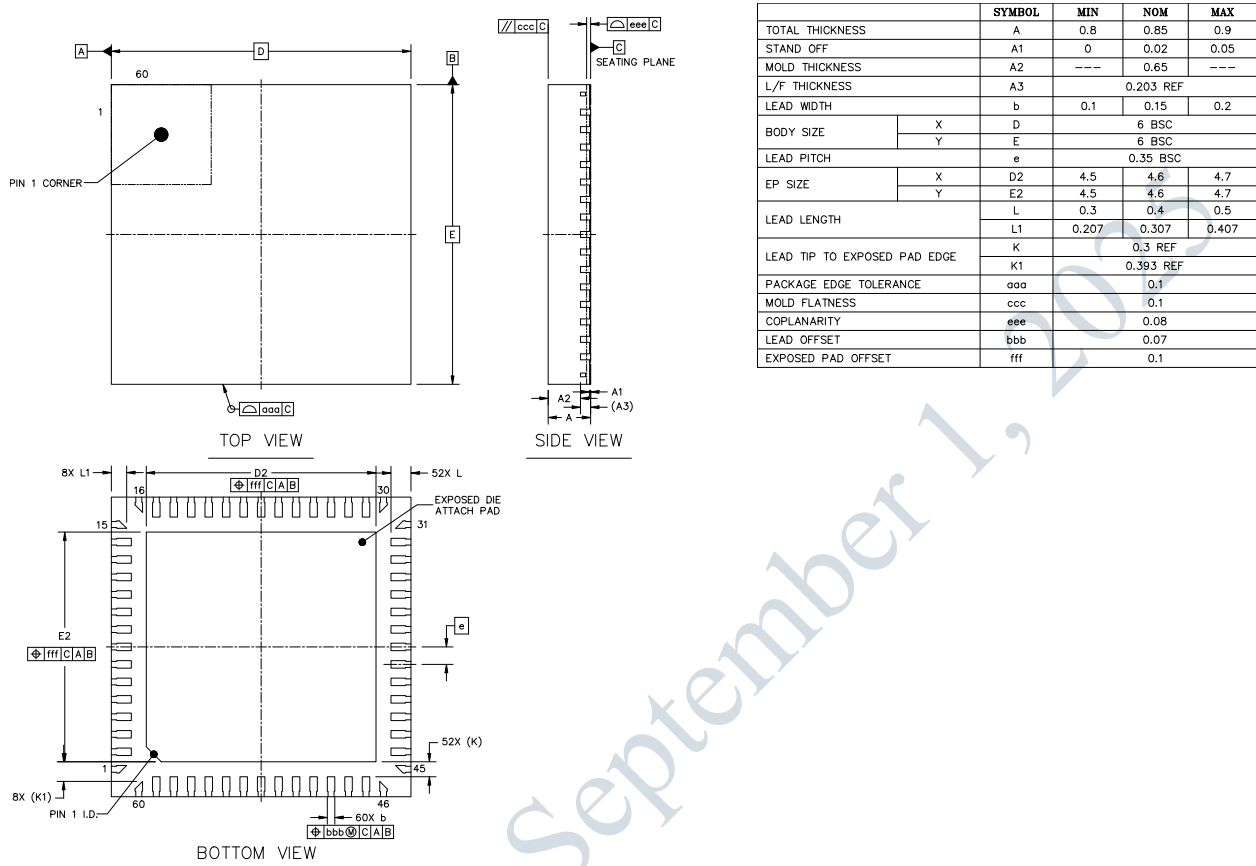
10.1 Package Dimensions

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.9
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.65	---
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.1	0.15	0.2
BODY SIZE X	D		6 BSC	
Y	E		6 BSC	
LEAD PITCH	e		0.35 BSC	
EP SIZE X	D2	4.5	4.6	4.7
Y	E2	4.5	4.6	4.7
LEAD LENGTH	L	0.3	0.4	0.5
	L1	0.207	0.307	0.407
LEAD TIP TO EXPOSED PAD EDGE	K		0.3 REF	
	K1		0.393 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.07	
EXPOSED PAD OFFSET	fff		0.1	

Figure 9: AIC8800D80X2P Packaging

10.2 Reel Information

SPEC	W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	K0	K1	t
SIZE	16.00 ±0.30	1.75 ±0.10	7.50 ±0.10	1.50 +0.10	1.50 +0.10	4.00 ±0.10	2.00 ±0.10	40.00 ±0.20	8.00 ±0.10	6.30 ±0.10		6.30 ±0.10		1.10 ±0.10		0.30 ±0.05

材料特性(MATERIAL)		TITLE	QFN6X6-85 P1=8		
COLOR	Black	DWG. NO.	JT-P-QFN6X6-85 P1=8A		
ELECTRIC	ELECTRIC	SCALE 1:1	DWG. NO:		UNIT: mm
MATERIAL	PS	CHECKED	TSS	DRAWN	ZH
THICKNESS	0.30	APPROVED	YS	DATE	2023-06-16
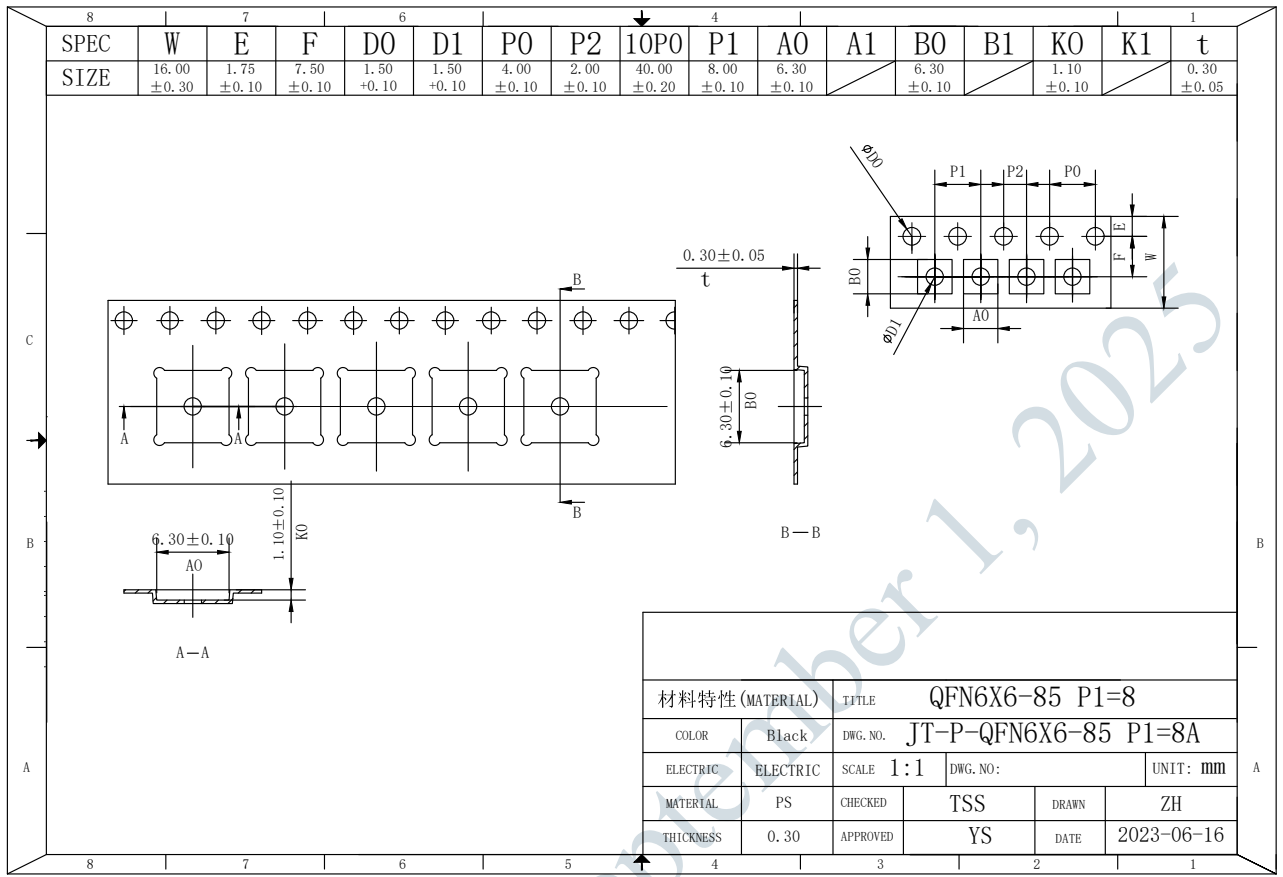
Figure 10: AIC8800D80X2P Reel Information

10.3 Product Identification

Figure 11: AIC8800D80X2P Silk Screen
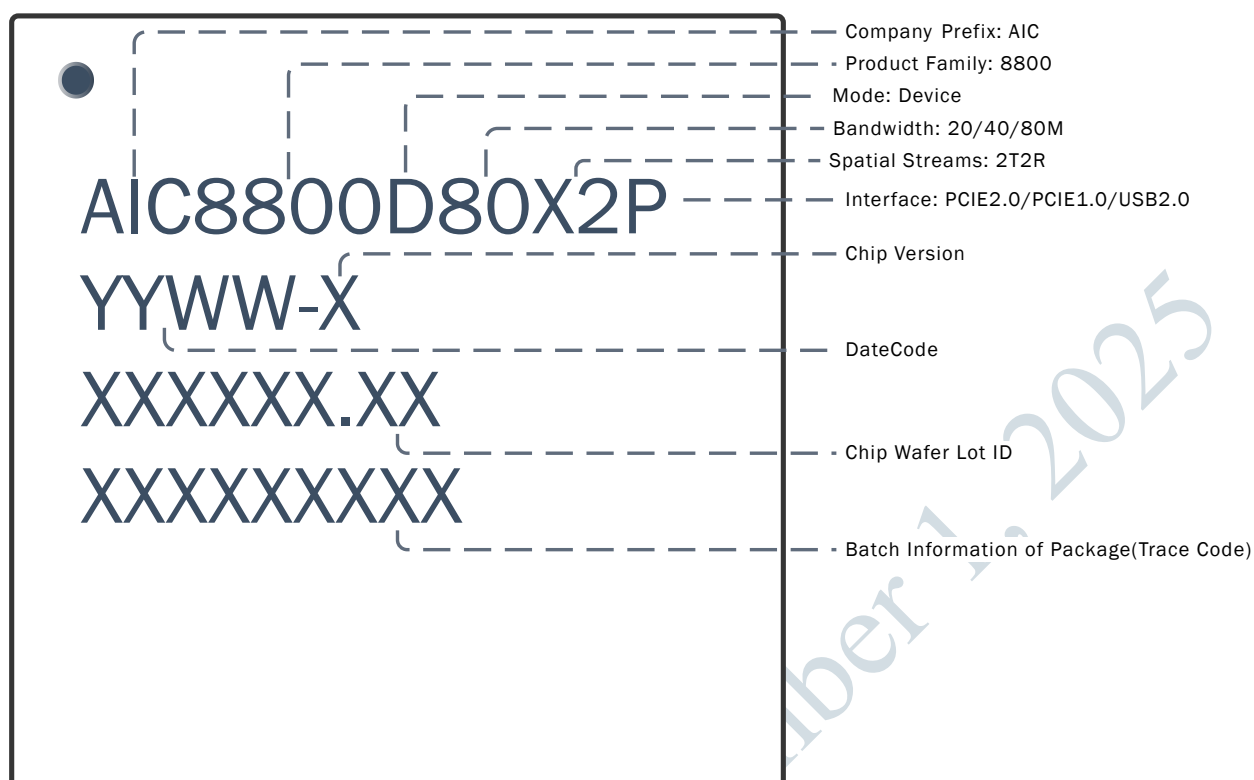
10.4 Package Thermal Characteristics

Table 16: Package Thermal Characteristics

Characteristic	Value
θ_{JA} in still air(°C/W)	44.574
θ_{JB} (°C/W)	9.433
θ_{JC} (°C/W)	9.406
ψ_{JT} (°C/W)	0.4
ψ_{JB} (°C/W)	2.7
Maximum junction temperature T_j (°C)	125
Maximum power dissipation (W)	7.59

10.5   Ording information

Table 17: Ordering Information

Part Number	Package	Description	Operating Ambient Temperature
AIC8800D80X2P	60 pin QFN package 6mm*6mm, 0.35mm pitch	2T2R Dual-band 2.4GHz and 5GHz WiFi6+Bluetooth 5.4	$-20\,°C$ to $80\,°C$

11 Reliability characteristics

Table 18: Reliability characteristics

Test Items	Test Condition	Test Criteria
HTOL	T_j=125 °C, 1000hrs, 1.1Vcc	JESD22-A108
LTOL	T_a=−20 °C, 1000hrs, 1.1Vcc	JESD22-A108
ESD	HBM:±2000V Class 2	JS-001-2023
	CDM:±250V Class C1	JS-002-2022
LU	±200mA Class I	JESD78F.02-2023
Solder ability	steam aging:8hrs; 245 °C, 5s	J-STD-002D-2013
HTST	150 °C (500/1000hrs)	JESD22-A103
LTST	−40 °C (168/1000hrs)	JESD22-A119
TCT	−65 °C to 150 °C, Dwell=15min, 500/1000Cycles	JESD22-A104E-2014
PCT	121 °C, 100%RH, 205kPa, 96/168hrs	JESD22-A102E-2015
UHAST	130 °C, 85%RH, 33.3psia, 96hrs	JESD22-A118
BHAST	130 °C, 85%RH, 33.3psia, 1.1Vcc, 96hrs	JESD22-A110E.01-2021
Precon MSL3	Level 3, Bake: 125 °C, 24hrs. Moisture Soak:30 °C,60%, 192hrs. Reflow : 260 °C, 3 times	JESD22-A113

12 Solder Reflow Profile

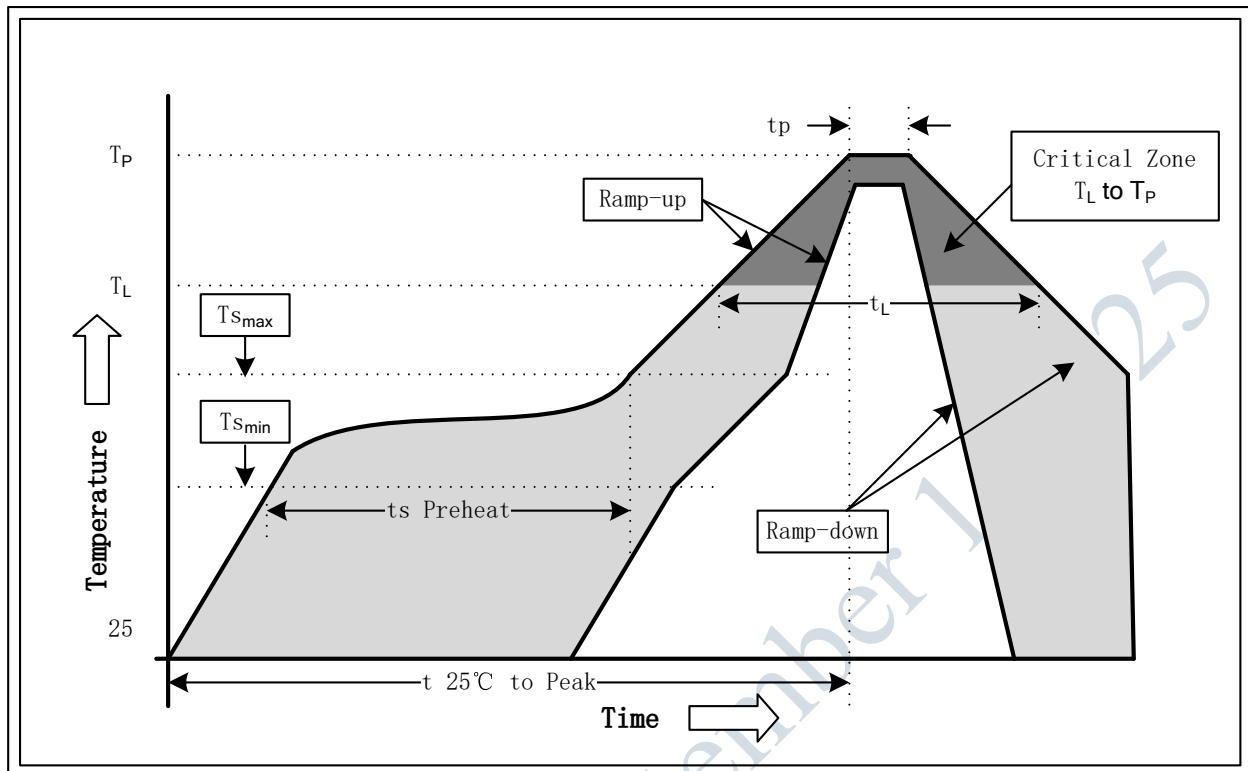Figure 12: Classification Reflow Profile

Table 19: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	100 °C 100 °C 60-120 seconds	150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	183 °C 60-150seconds	217 °C 60-150 seconds
Peak /Classification Temperature(Tp)	See the table 20	See Table 21
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 20: Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table 21: Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 350–2000	Volume mm3 >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm–2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Note 1: All temperature refers topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 21.

Note 3: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package maysill exist.

Note 5: Components intended for use in a "lead-free" assembly process shall be evaluated using the "lead free" classification temperatures and profiles defined in Table 19, Table 20, Table 21 whether or not lead free.

13 Change List

The following Table 22 summarizes revisions to this document.

Table 22: Change List

Rev	Date	Auther	Change description
V1.0.0	20230417	AICSEMI	initial version
V1.0.1	20241205	AICSEMI	Add the description of each power supply parameter Add the description of interface Add the description of GPIO
V1.0.2	20250813	AICSEMI	Adjust the pin assignments of GPIOB0 and GPIOA7

14 RoHS Compliant

The products meet the requirements of Directive 2011/65/EU of Europe Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). The products are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals.

15 ESD Sensitivity

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site. AIC products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment.

16 Disclaimer

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