# *AIC8800M80P*

Preliminary Low-Energy WiFi6/BTDM5.4 SoC
Data Sheet.

*AIC Semiconductor (Shanghai) CO., Ltd.*
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Author: AICSEMI
version 1.0.1
*www.aicsemi.com*

# Contents

# 1 General Description

AIC8800M80P is a 22nm, highly integrated SoC with dual band WiFi6, BTDM 5.4 and high performance Wlan CPU for wireless application. It provides miniaturized solutions that reduce design costs with minimal material.

## 1.1 WiFi Features

- CMOS single-chip fully-integrated RF, Modem and MAC
- Intergrated PA LNA and Tx/Rx switch
- Supports IEEE 802.11a/b/g/n/ac/ax specifications with single stream transmission and reception
- Supports 2.4GHz/5GHz band, the 5G band includes U-NII-1 U-NII-2A U-NII-2C and U-NII-3
- Supports MCS0–MCS11 in 20/40/80 MHz channels in both uplink and downlink direction with maximum 600.4 Mbps data rate
- In addition to the regular bandwidth, 5MHz/10MHz is also supported
- RX sensitivity -99dBm in 11b 1M mode
- Tx power up to 23dBm in 11b mode, 18dBm in HT/VHT/HE MCS7 mode
- Supports LDPC in Tx and Rx for all modes for performance improvement
- Supports space-time block coding (STBC) reception for all modes
- Supports beamforming as beamformee for 802.11ac and 802.11ax mode with explicit compressed feedback
- Supports short GI mode in TX and RX
- Supports MU-MIMO operation as reception for 802.11ac and 802.11ax mode
- Supports OFDMA for efficient resource utilization in both Tx and Rx direction in 802.11ax mode
- Supports Wi-Fi6 TWT
- Supports DCM, Extended Range, partial bandwidth (106 tone) mode for coverage enhancement in 802.11ax mode
- Supports midamble based channel estimation for time-various channel in 802.11ax mode
- Algorithms to improve performance in presence of Bluetooth and blocking interference
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities for both Tx and Rx
- Available per-packet channel quality and signal strength measurements
- Supports STA, AP, Wi-Fi Direct modes concurrently
- Supports WEP/WPA/WPA2/WPA3-SAE Personal, MFP
- Supports IEEE 802.11d/w/k/r/v/e/h/i

## 1.2 BTDM5.4 Features

- Complies with Bluetooth Core Specification Version 5.4 with provisions for supporting future specifications
- Supports all the mandatory and optional features of Bluetooth low energy 5.4
- Supports advanced master and slave topologies
- Supports BR/EDR/BLE (1/2Mbps/LongRange S2/8)
- Bluetooth Class 1 Class 2 or Class3 transmitter operation
- Bluetooth Low Energy Class 1 Class 1.5 Class 2 or Class3 transmitter operation
- Supports BLE audio
- Host controller interface (HCI) using a high-speed UART interface
- PCM for audio data
- Adaptive frequency hopping (AFH) for reducing radio frequency interference

## 1.3 Other Features

- Supports PCIE/USB2.0/HCI_UART/PCM interface
- Integrated low power timer and watchdog
- 1024 bits Efuse

## 1.4 Packaging Information

- Compact profile package 5mm×5mm×0.75mm QFN48

## 1.5 Application

- Wireless network adapter

# 2 Platform Description

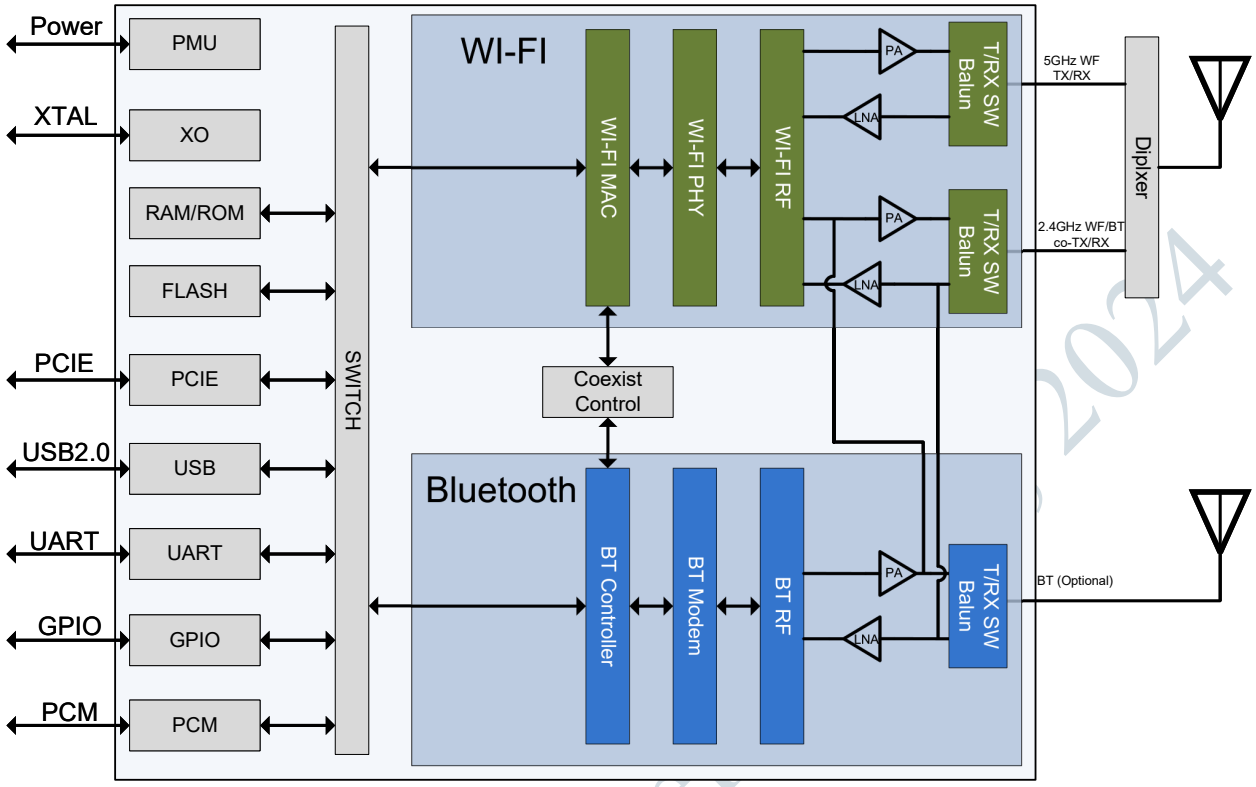



Figure 1: AIC8800M80P Block Diagram

# 3 Pins Description

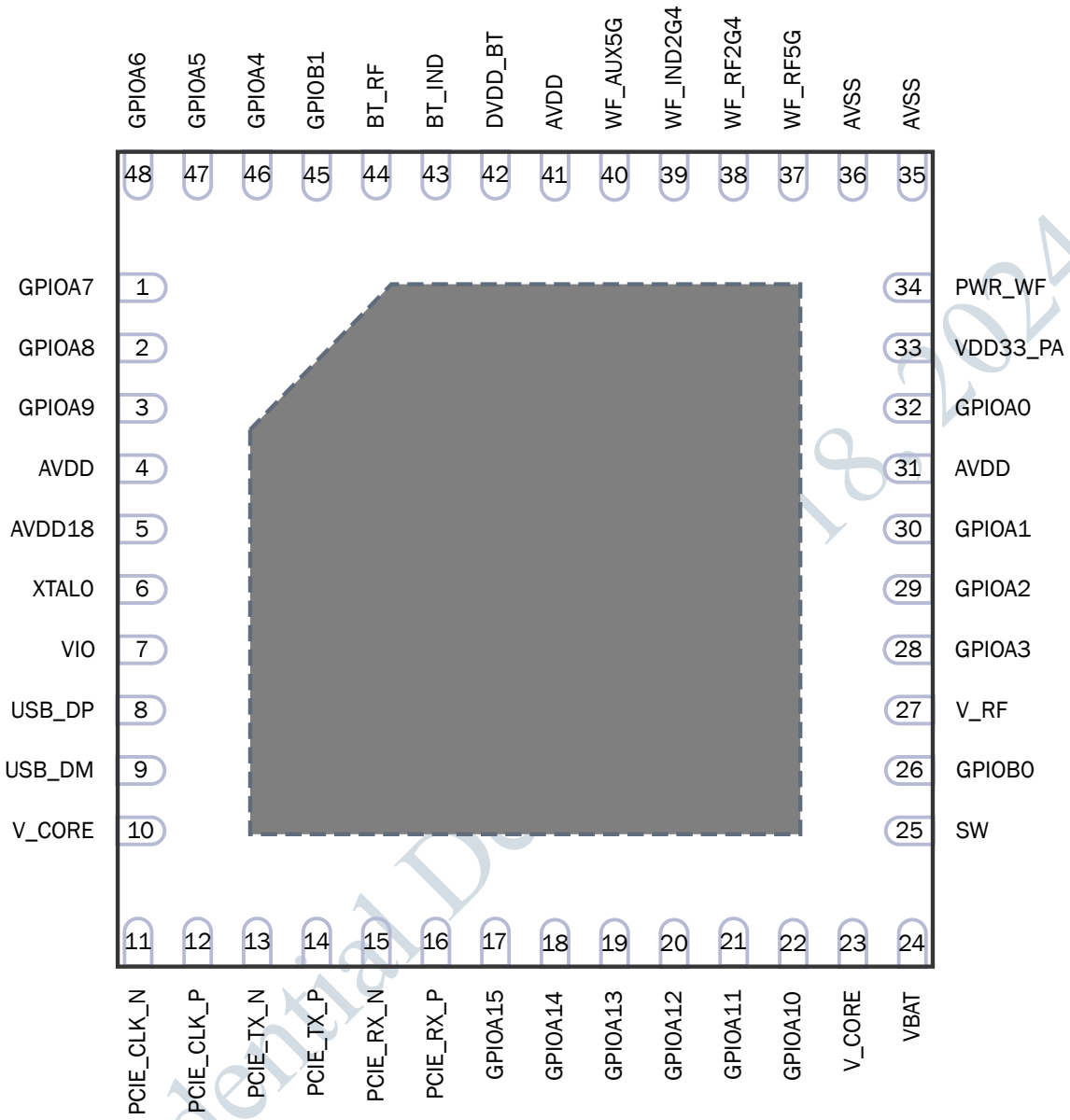



Figure 2: AIC8800M80P Pin Map

Table 1: AIC8800M80P Pin Description

| Pin Name | QFN NO. | I/O | Description |
|---|---|---|---|
| **RF** | | | |
| WF_RF2G4 | 38 | I/O | WiFi 2.4G RF |
| WF_IND2G4 | 39 | | WiFi 2.4G RF Ground, connect a 1.4nH inductor to ground |
| WF_RF5G | 37 | I/O | WiFi 5G RF |
| WF_AUX5G | 40 | I | WiFi 5G RX Aux |
| BT_RF | 44 | I/O | BT RF |
| BT_IND | 43 | | BT RF Ground, connect a 1.4nH inductor to ground |
| AVSS | 35 | | Connect to the ground |
| AVSS | 36 | | Connect to the ground |

Table 1: AIC8800M80P Pin Description

| Pin Name | QFN NO. | I/O | Description |
|---|---|---|---|
| **PMU** | | | |
| AVDD | 4 | | Need 1uF decoupling capacitor |
| AVDD | 31 | | Need 1uF decoupling capacitor |
| AVDD | 41 | | Need 1uF decoupling capacitor |
| AVDD18 | 5 | | Power output 1.8v, internal Efuse supply voltage, connect a 1uF decoupling capacitor |
| V_CORE | 10 | | Need 1uF decoupling capacitor, connect to pin23 |
| V_CORE | 23 | | Digital Supply Voltage |
| VIO | 7 | I | IO Power Supply, Support 1.8v/3.3v |
| VBAT | 24 | I | System power supply |
| SW | 25 | O | Power Output For V_RF |
| V_RF | 27 | I | RF Supply Voltage |
| VDD33_PA | 33 | I | PA Supply Voltage |
| PWR_WF | 34 | I | WiFi system enable |
| DVDD_BT | 42 | | Need 1uF decoupling capacitor |
| **CLK** | | | |
| XTAL0 | 6 | I | 40M Crystal In |
| **GPIO** | | | |
| GPIOA0 | 32 | I/O | GPIO |
| GPIOA1 | 30 | I/O | GPIO |
| GPIOA2 | 29 | I/O | GPIO |
| GPIOA3 | 28 | I/O | GPIO |
| GPIOA4 | 46 | I/O | GPIO |
| GPIOA5 | 47 | I/O | GPIO |
| GPIOA6 | 48 | I/O | GPIO |
| GPIOA7 | 1 | I/O | GPIO |
| GPIOA8 | 2 | I/O | GPIO |
| GPIOA9 | 3 | I/O | GPIO |
| GPIOA10 | 22 | I/O | GPIO |
| GPIOA11 | 21 | I/O | GPIO |
| GPIOA12 | 20 | I/O | GPIO |
| GPIOA13 | 19 | I/O | GPIO |
| GPIOA14 | 18 | I/O | GPIO |
| GPIOA15 | 17 | I/O | GPIO |
| GPIOB0 | 26 | I/O | GPIO, pull down GPIOB0 and GPIOB1 the chip will be down-load mode |
| GPIOB1 | 45 | I/O | GPIO, pull down GPIOB1 the chip will be device mode |
| USB_DP | 8 | I/O | USB |
| USB_DM | 9 | I/O | USB |
| PCIE_CLK_N | 11 | I/O | |
| PCIE_CLK_P | 12 | I/O | |
| PCIE_TX_N | 13 | I/O | Need a 100nF capacitor in series |
| PCIE_TX_P | 14 | I/O | Need a 100nF capacitor in series |
| PCIE_RX_N | 15 | I/O | |
| PCIE_RX_P | 16 | I/O | |

# 4 Electrical Characteristics

## 4.1 DC Electrical Specification

Table 2: DC Electrical Specification

| Symbol | Description | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| VBAT | Supply Voltage for System | 3.0 | 3.3 | 3.6 | V |
| V_RF | Supply Voltage for V_RF | 1.26 | 1.4 | 1.54 | V |
| V_FLS | Supply Voltage for Flash | - | 3.0 | - | V |
| V_CORE | Internal power supply for V_CORE | 0.6 | 0.9 | 1.0 | V |
| VDD33_PA | Supply Voltage for PA | 3.0 | 3.3 | 3.6 | V |
| AVDD18 | Internal power supply for Efuse | 1.8 | 2.0 | 2.2 | V |
| DVDD_BT | Internal power supply for BT RF | 0.8 | 1.05 | 1.4 | V |
| AVDD | Connected with V_RF inside the chip | 1.26 | 1.4 | 1.54 | V |
| VIO | Supply Voltage for VIO, VIO=1.8V | 1.71 | 1.8 | 1.89 | V |
| | Supply Voltage for VIO, VIO=3.3V | 3.135 | 3.3 | 3.465 | V |

## 4.2 Absolute Maximum Ratings

The absolute maximum ratings in Table 4 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 3: Environmental rating

| Rating | Symbol | Value | Uint |
|---|---|---|---|
| DC supply for the VBAT | VBAT | -0.5 to +3.9 | V |
| DC supply for the PA | AVDD33_PA | -0.5 to +3.9 | V |
| DC supply for the GPIO | VIO | -0.5 to +3.9 | V |

## 4.3 Environmental ratings

Table 4: Environmental rating

| Symbol | Description | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{amb}$ | Ambient Temperature | -20 | 27 | 80 | ℃ |
| $T_{store}$ | Store Temperature | -55 | | 125 | ℃ |
| Relative Humidity | Operation | | | 85 | % |
| | Storage | | | 60 | % |

# 5 Power Management Unit

## 5.1 Description

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the AIC8800M80P. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

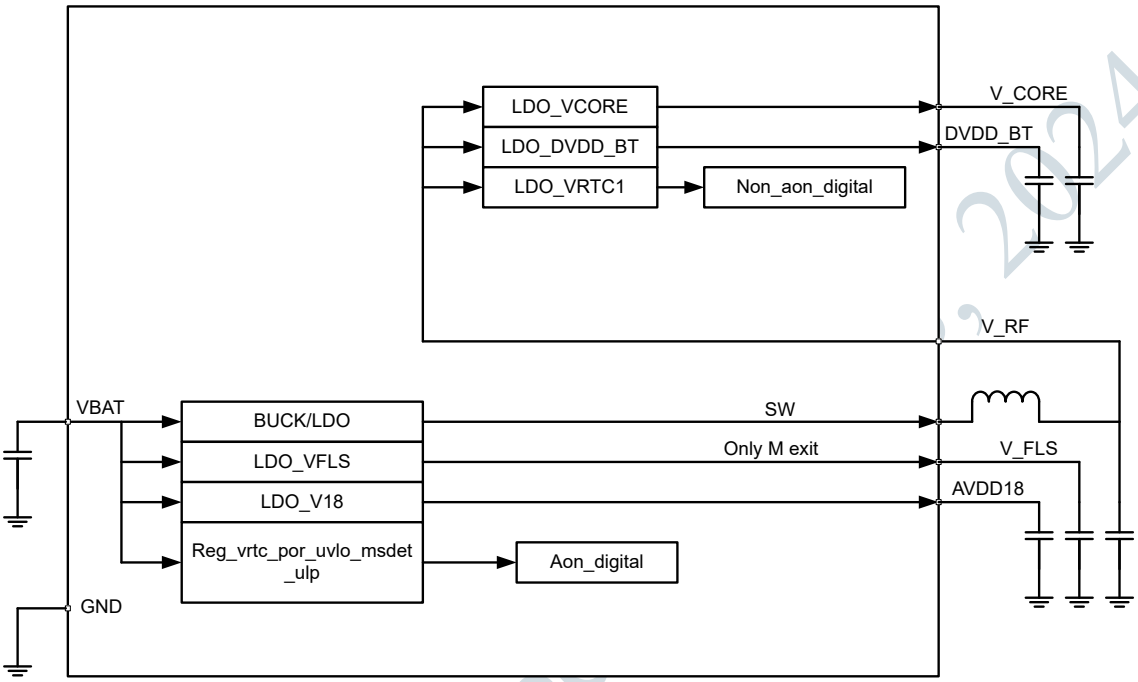



Figure 3: AIC8800M80P PMU Diagram

## 5.2 PMU Features

- VBAT to 1.4Vout (500 mA maximum) V_RF Buck switching regulator or LDO
- VBAT to 3.0Vout (80 mA maximum) V_FLS
- VBAT to 1.8Vout (100 mA maximum) AVDD18
- 1.4V to 0.9Vout (300 mA maximum) V_CORE
- 1.4V to 0.9Vout (100 mA maximum) DVDD_BT
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto calibration by the crystal clock for precise wake up timing from low power modes

## 5.3 V_RF Buck Switching Regulator

Table 5: V_RF Buck Switching Regulator Specifications

| Specification | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input supply voltage | Min value is Limited BY UVLO | 3.0 | 3.3 | 3.6 | V |
| PWM mode switching frequency | - | | 1.8 | | MHz |
| PWM output current | - | - | - | 500 | mA |
| Output voltage range | Programmable, 25 mV steps. Default=1.4V | - | 1.4 | - | V |
| PWM output voltage DC accuracy | Includes load and line regulation. Forced PWM. Before trimming | -10 | - | 10 | % |
| PWM ripple voltage, static | Measure with 20MHz bandwidth limit. Static Load. VBAT=3.3V, Vout=1.4V, Fsw=1.8MHz, 4.7uH inductor L>2uH effective, Cap+Board total-ESR<20 mΩ, Cout=4.7uF, Cout ESL<200pH | - | 4.5 | 20 | mV |
| PWM mode peak efficiency | Peak Efficiency at 200mA load Fsw=1.8MHz PWM, L>3uH effective inductor Tmax=1mm, 0805 inch Inductor DCR=275mΩ | - | 85 | - | % |
| LP-PFM mode efficiency | Efficiency at 0.4mA load PFM L=4.7uH effective inductor Tmax=1mm, 0805 inch inductor DCR=275mΩ | - | 80 | - | % |
| Start up time from power down | VBAT=3.3V always on. Time from PWR_WF rising edge to RFBUCK/LDO reaching 1.4V | - | 1.85 | - | ms |
| External inductor | 0806 inch size, 4.7uH, DCR<300mΩ, Isat>250mA | - | 4.7 | - | uH |
| External output capacitor | Ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V | - | 4.7 | - | uF |
| External input capacitor | For VBAT pin, ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V | - | 4.7 | - | uF |

## 5.4 V_FLS

Table 6: V_FLS Specifications

| Specification | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input supply voltage, Vin | Min=Vo+0.25V=3.25V dropout voltage requirement must be met under maximum load for performance specifications | 3.0 | 3.3 | 3.6 | V |
| Output current | - | - | - | 80 | mA |
| Output voltage range, Vo | Programmable, Default=3.0V | - | 3.0 | - | V |
| Dropout voltage | At max. load | - | - | 250 | mV |
| Output voltage DC accuracy | Includes line/load regulation, before trimming | -10 | - | 10 | % |
| Quiescent current | No load | - | 18 | - | uA |
| | Max load at 80 mA | - | 0.9 | - | mA |
| Line regulation | Vin from 3.0V to 3.6V, max load | - | - | 3.5 | mV/V |
| Load regulation | Load from 1mA to 80mA, Vin=3.3V | - | - | 0.3 | mV/mA |
| PSRR | Vin=3.3V, Vo=3.0V, Co=1uF, Max load, 100Hz to 100kHz | 20 | - | - | dB |
| LDO turn on time | Reference ready. Vo from 0 to 3.0V, Co=1uF | - | 45 | - | us |
| Output over current limit | - | 120 | - | - | mA |
| External output capacitor, Co | Ceramic, X5R, 0201 inch, ESR<50mΩ at 4MHz, 1uF±20%, 6.3V | 0.1 | 1 | 2.2 | uF |
| External input capacitor | For VBAT pin, ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V | - | 4.7 | - | uF |

## 5.5 AVDD18

Table 7: AVDD18 Specifications

| Specification | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input supply voltage, Vin | Min value is Limited BY UVLO | 3.0 | 3.3 | 3.6 | V |
| Output current | - | - | - | 100 | mA |
| Output voltage range, Vo | Programmable in 0.1V steps. Default=2V | - | 2 | - | V |
| Dropout voltage | At max. load | - | - | 200 | mV |
| Output voltage DC accuracy | Includes line/load regulation, before trimming | -10 | - | 10 | % |
| Quiescent current | No load | - | 15 | - | uA |
| | Max load at 100 mA | - | 1.1 | - | mA |
| Line regulation | Vin from 3.0V to 3.6V, max load | - | - | 3.5 | mV/V |
| Load regulation | Load from 1mA to 100mA, Vin=3.3V | - | - | 0.3 | mV/mA |
| PSRR | Vin=3.3V, Vo=2.0V, Co=1uF, Max load, 100Hz to 100kHz | 20 | - | - | dB |
| LDO turn on time | Reference ready. Vo from 0 to 2.0V, Co=1uF | - | 30 | - | us |
| Output over current limit | - | 120 | - | - | mA |
| External output capacitor, Co | Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V | 0.1 | 1 | 2.2 | uF |
| External input capacitor | For VBAT pin, ceramic, X5R, ESR<20mΩ at 4MHz, 4.7uF±20%, 6.3V | - | 4.7 | - | uF |

## 5.6 V_CORE

Table 8: V_CORE Specifications

| Specification | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input supply voltage, Vin | Min=Vo+0.25V=1.15V dropout voltage requirement must be met under maximum load for performance specifications | 1.15 | 1.4 | 1.6 | V |
| Output current | - | 0.1 | - | 300 | mA |
| Output voltage range, Vo | Programmable in 18mV steps. Default=0.9V | 0.6 | 0.9 | 1 | V |
| Dropout voltage | At max load | - | - | 250 | mV |
| Output voltage DC accuracy | Includes line/load regulation, before trimming | -10 | - | 10 | % |
| Quiescent current | No load | - | 18 | - | uA |
| | 300mA load | - | 2 | - | mA |
| Line regulation | Vin from 1.15V to 1.6V, max load | - | - | 16 | mV/V |
| Load regulation | Load from 1mA to 300mA, Vin=1.4V | - | - | 0.03 | mV/mA |
| Leakage current | Power down, Vin=1.4V, typical at Tj=25°C | - | 0.9 | - | uA |
| | Power down, Vin=0.9V, typical at Tj=25°C | - | 0.3 | - | uA |
| PSRR | 100Hz to 100kHz, Vin≥1.2V, Co=1uF | 20 | - | - | dB |
| LDO turn on time | Reference ready. Vo from 0 to 0.9V, Co=1uF | - | 13 | - | us |
| External output capacitor, Co | Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V | 0.1 | 1 | 2.2 | uF |
| External input capacitor | Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V | 1 | - | - | uF |

## 5.7 DVDD_BT

Table 9: DVDD_BT Specifications

| Specification | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input supply voltage, Vin | Min=Vo+0.25V=1.3V dropout voltage requirement must be met under maximum load for performance specifications | 1.3 | 1.4 | 1.6 | V |
| Output current | - | 0.1 | - | 100 | mA |
| Output voltage range, Vo | Default=1.05V | 0.8 | 1.05 | 1.4 | V |
| Dropout voltage | At max load | - | - | 200 | mV |
| Output voltage DC accuracy | Includes line/load regulation, before trimming | -10 | - | 10 | % |
| Quiescent current | No load | - | 30 | - | uA |
| | Max load at 100mA | - | 1.1 | - | mA |
| Line regulation | Vin from 1.3V to 1.6V, max load | - | - | 3.5 | mV/V |
| Load regulation | Load from 1mA to 100mA, Vin=1.4V | - | - | 0.3 | mV/mA |
| PSRR | Vin=1.4V, Vo=1.05V, Co=1uF, Max load, 100Hz to 100kHz | 20 | - | - | dB |
| LDO turn on time | Reference ready. Vo from 0 to 1.05V, Co=1uF | - | 30 | - | us |
| Output over current limit | - | 120 | - | - | mA |
| External output capacitor, Co | Ceramic, X5R, 0201 inch, 1uF±20%, 6.3V | 0.1 | 1 | - | uF |

## 5.8 Pwrkey

PWR_WF, is used to power up the regulators and take the respective section out of reset. The V_RF and V_core power up when the reset signals are deasserted. All regulators are powered down only when PWR_WF is deasserted.

Table 10: PWR_WF Electrcal Specifications

| Specification | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input high voltage | VIH | For Chip ON pin | 1.125 | - | 3.6 | V |
| Input low voltage | VIL | - | VSS | - | 0.625 | V |
| Pull down resistance (Internal) | PRD | - | - | 200 | - | kΩ |
| REG ON time | TREG_ON | - | 8 | - | - | ms |
| REG OFF time | TREG_OFF | - | 6 | - | - | ms |

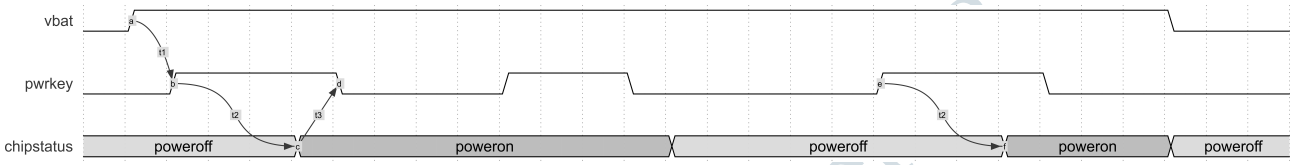



Figure 4: AIC8800M80P Power ON/OFF Timing

**t1**: VIO's power on time ≥ VBAT's
**t2**: chip all power on ready time ≥ power key high time + 8ms
**t3**: in mcu mode, when power off, power key must keep high ≥ 8ms+6ms(default chip has 6ms high protection, this function can be disable by software configure)
**Note**: In practical applications, if the VIO is powered on earlier than VBAT, there is no problem for the chip

# 6 External Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. Colpitts type oscillator circuits is adopted to provide high quality reference clock. Only one lead pin is required and external load capacitors are saved. The table below lists the requirement for the crystal unit.

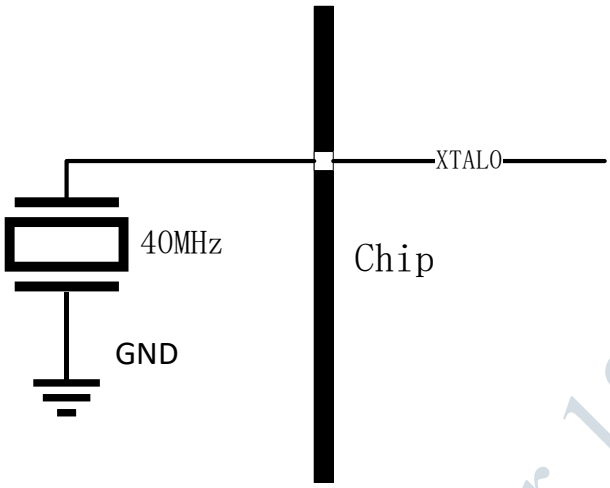



Figure 5: Colpitts mode

Table 11: Colpitts mode crystal requirement

| Symbol | Parameter | Value | Note |
|---|---|---|---|
| F0 | Nominal Frequency | 40MHz | |
| ΔF/F0 | Frequency Tolerance | ±10ppm | @25 °C±3 °C |
| TC | Frequency Stability | ±10ppm | Over Operating Temp. Range (Reference 25 °C) |
| ESR | Equivalent Series Resistance | <40Ω | |
| CL | Load Capacitance | 10pF | |
| TS | Pulling Sensitivity | ≥15ppm/pF | |
| DL | Drive Level | >100uW | |

# 7 Interface

AIC8800M80P supports a variety of data interfaces.

## 7.1 PCIE

### 7.1.1 Description

In the PCIE wireless network adapter application, the data of WiFi is transmitted through the PCIE, the data of Bluetooth is transmitted through the USB, and the audio data can be transmitted either UART or PCM.
The AIC8800M80P WLAN section support for PCIE version 1.0.

### 7.1.2 PCIE Timing

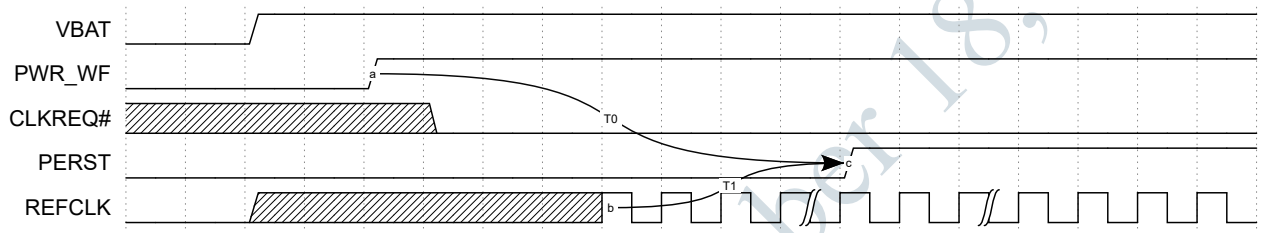



Figure 6: PCIE Timing

**T0**: T0>20ms, recommended 50ms.
**T1**: T1>100us

## 7.2 USB2.0

### 7.2.1 Description

In the USB application, the data of Bluetooth/WiFi is transmitted through the USB, and the audio data can be transmitted either USB or PCM.
The AIC8800M80P WLAN section support for USB version 2.0, the feature is as follow:

- Complies with USB Specification Revision 2.0 for WLAN and Bluetooth controller
- Supports up to 7 bidirectional endpoints, including control endpoint 0
- Supports packet-based, Dynamic FIFO memory allocation for endpoints for small FIFOs and flexible efficient use of RAM
- Supports endpoint FIFO sizes that are not powers of 2, to allow the use of contiguous memory locations

### 7.2.2 USB Timing

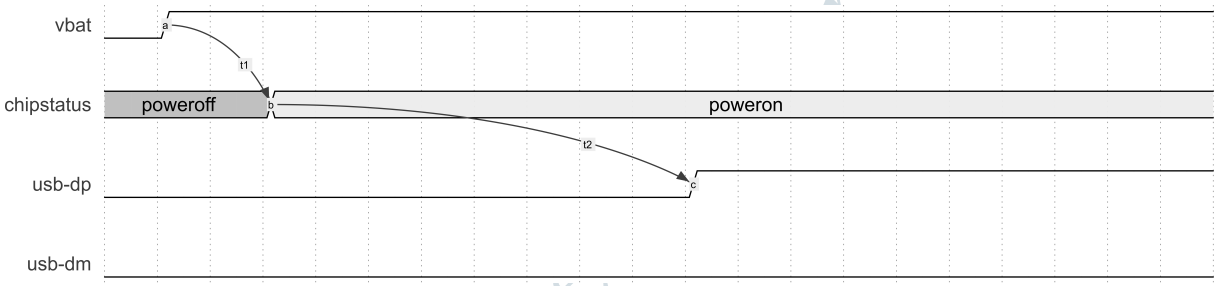



Figure 7: Powerup USB Initial

**t1**: chip all power on ready time ≥ power up time + 8ms.
**t2**: usb dp pull up time ≥ chip all power on ready time + 22ms

# 8 GPIO

AIC8800M80P has a total of 18 GPIO pins, including GPIOA0∼15 and GPIOB0∼6. These GPIOs can be configured with registers for different functions.

## 8.1 Threshold

Table 12: IO Threshold

| VIO | Symbol | IO Threshold |
|---|---|---|
| 1.8V | $V_{inh}$ | 1.320V |
| 1.8V | $V_{inl}$ | 0.470V |
| 3.3V | $V_{inh}$ | 2.840V |
| 3.3V | $V_{inl}$ | 0.300V |

## 8.2 IO Assignment

In the general design, the chip pin assignment is referred to Table 13, the public driver cab be used directly.

Table 13: General IO Assignment

| GPIO | Pin NO. | Assignment | Type | Description |
|---|---|---|---|---|
| GPIOA0 | 32 | PCM_FSYNC | I/O | PCM sync signal, can be master (output) or slave (input) |
| GPIOA1 | 30 | PCM_CLK | I/O | PCM clock, can be master (output) or slave (input) |
| GPIOA2 | 29 | PCM_DIN | I | PCM data input |
| GPIOA3 | 28 | PCM_DOUT | O | PCM data output |
| GPIOA4 | 46 | PCIE_WAK_N | I/O | PCIE_WAK_N |
| GPIOA5 | 47 | PCIE_PERST_N | I | PCIE_PERST_N |
| GPIOA6 | 48 | PCIE_REQ_N | I/O | PCIE_REQ_N |
| GPIOA7 | 1 | HST_WAK_WF | I | Host wake up Wlan |
| GPIOA8 | 2 | UART_RX | I | Debug UART RX |
| GPIOA9 | 3 | UART_TX | O | Debug UART TX |
| GPIOA10 | 22 | BT_UART_RX | I | UART receive data |
| GPIOA11 | 21 | BT_UART_TX | O | UART transmit data |
| GPIOA12 | 20 | BT_UART_CTS | I | UART clear to send |
| GPIOA13 | 19 | BT_UART_RTS | O | UART request to send |
| GPIOA14 | 18 | HST_WAK_BT | I | Host wake up BT |
| GPIOA15 | 17 | BT_WAK_HST | O | BT wake up host |
| GPIOB0 | 26 | WF_WAK_HST | O | Wlan wake up host |
| GPIOB1 | 45 | GPIOB1 | I/O | GPIOB1 |

## 8.3 IO Status

Table 14: Default Status of IO

| GPIO | Pin NO. | Function | Type | Pull |
|---|---|---|---|---|
| GPIOA0 | 32 | SW_CLK | I | UP |
| GPIOA1 | 30 | SWD | I/O | UP |
| GPIOA2 | 29 | GPIOA2 | I/O | DN |
| GPIOA3 | 28 | GPIOA3 | O | DN |
| GPIOA4 | 46 | GPIOA4 | I/O | DN |
| GPIOA5 | 47 | GPIOA5 | I/O | DN |
| GPIOA6 | 48 | GPIOA6 | I/O | DN |
| GPIOA7 | 1 | GPIOA7 | I/O | DN |
| GPIOA8 | 2 | UART0_RX | I | UP |
| GPIOA9 | 3 | UART0_TX | O | OFF |
| GPIOA10 | 22 | GPIOA10 | I/O | DN |
| GPIOA11 | 21 | GPIOA11 | I/O | DN |
| GPIOA12 | 20 | GPIOA12 | I/O | DN |
| GPIOA13 | 19 | GPIOA13 | I/O | DN |
| GPIOA14 | 18 | GPIOA14 | I/O | DN |
| GPIOA15 | 17 | GPIOA15 | I/O | DN |
| GPIOB0 | 26 | GPIOB0 | I/O | UP |
| GPIOB1 | 45 | GPIOB1 | I/O | UP |

**I**: Input signal
**O**: Output signal
**I/O**: Input/Output signal
**UP**: Pulled up (of 50KΩ)
**DN**: Pulled down (of 50KΩ)
**OFF**: Neither pulled up nor pulled down

# 9 Application Circuit

The AIC8800M80P Bluetooth RF design supports two modes, BT Only Mode and BT Coant Mode. The advantage of the BT Only Mode is that it can operate simultaneously with WiFi 2.4G, Combined with AIC's excellent coexistence design, it can provide higher throughput and superior Bluetooth performance. The advantage of the BT Coant Mode is that it saves space and cost.

## 9.1 BT Only Mode

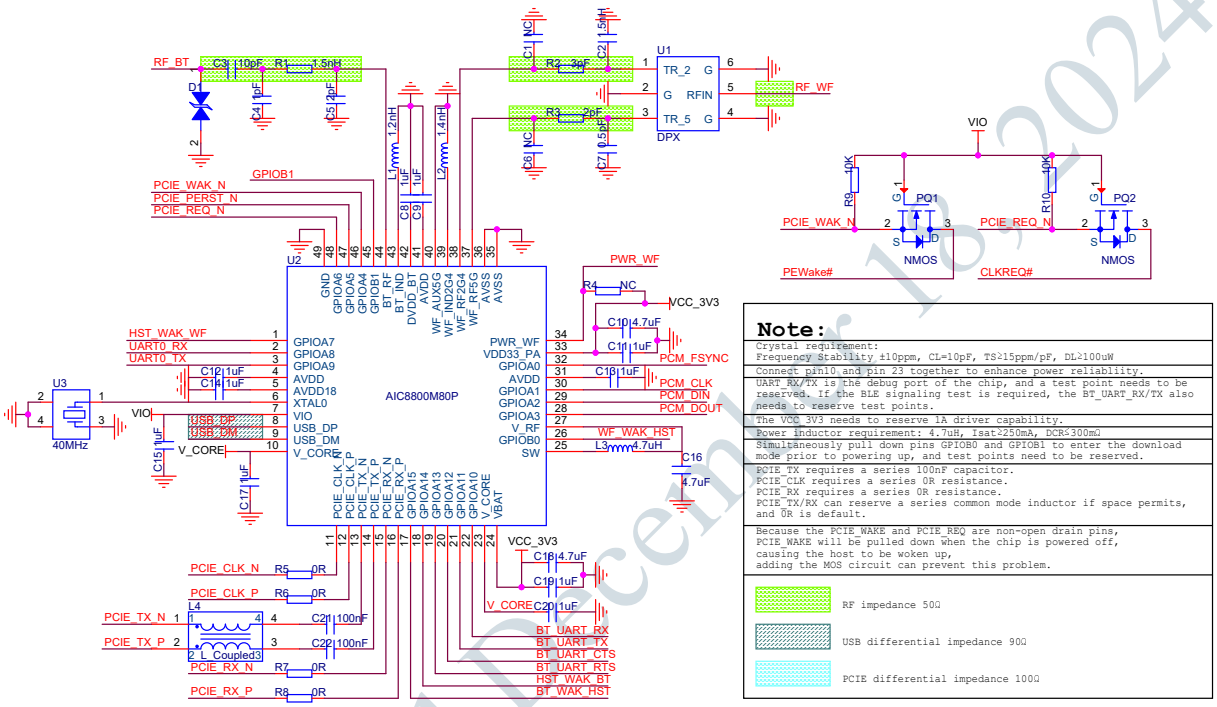



Figure 8: AIC8800M80P BT Only Mode Application Circuit

## 9.2 BT Coant Mode

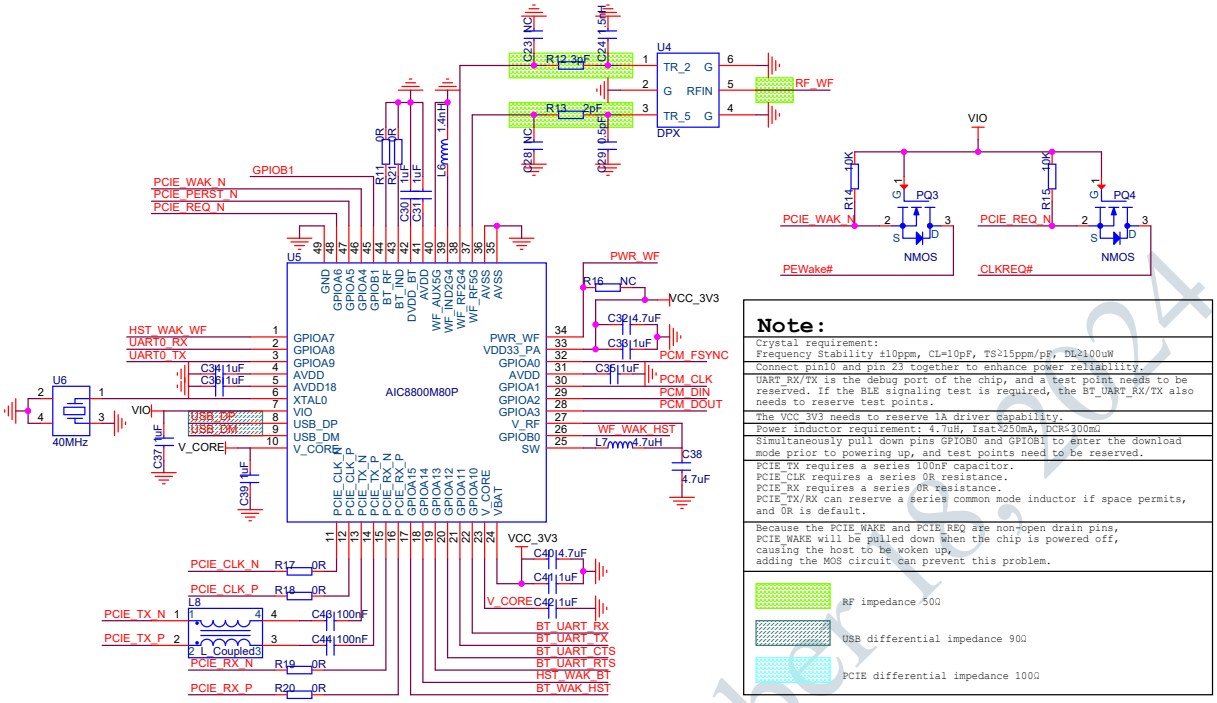
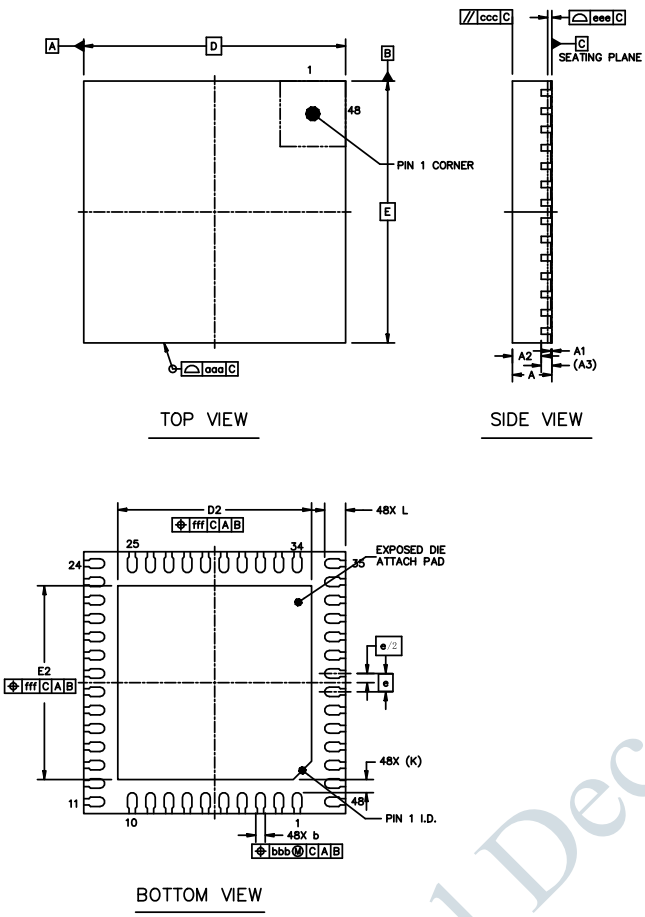



Figure 9: AIC8800M80P BT Coant Mode Application Circuit

# 10 Package Physical Dimension

## 10.1 Package Dimensions




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.7 | 0.75 | 0.8 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.55 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.13 | 0.18 | 0.23 |
| BODY SIZE | X | D | | 5 BSC | |
| | Y | E | | 5 BSC | |
| LEAD PITCH | | e | | 0.35 BSC | |
| EP SIZE | X | D2 | 3.6 | 3.7 | 3.8 |
| | Y | E2 | 3.6 | 3.7 | 3.8 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 0.25 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.07 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

Figure 10: AIC8800M80P Packaging

## 10.2 Reel Information

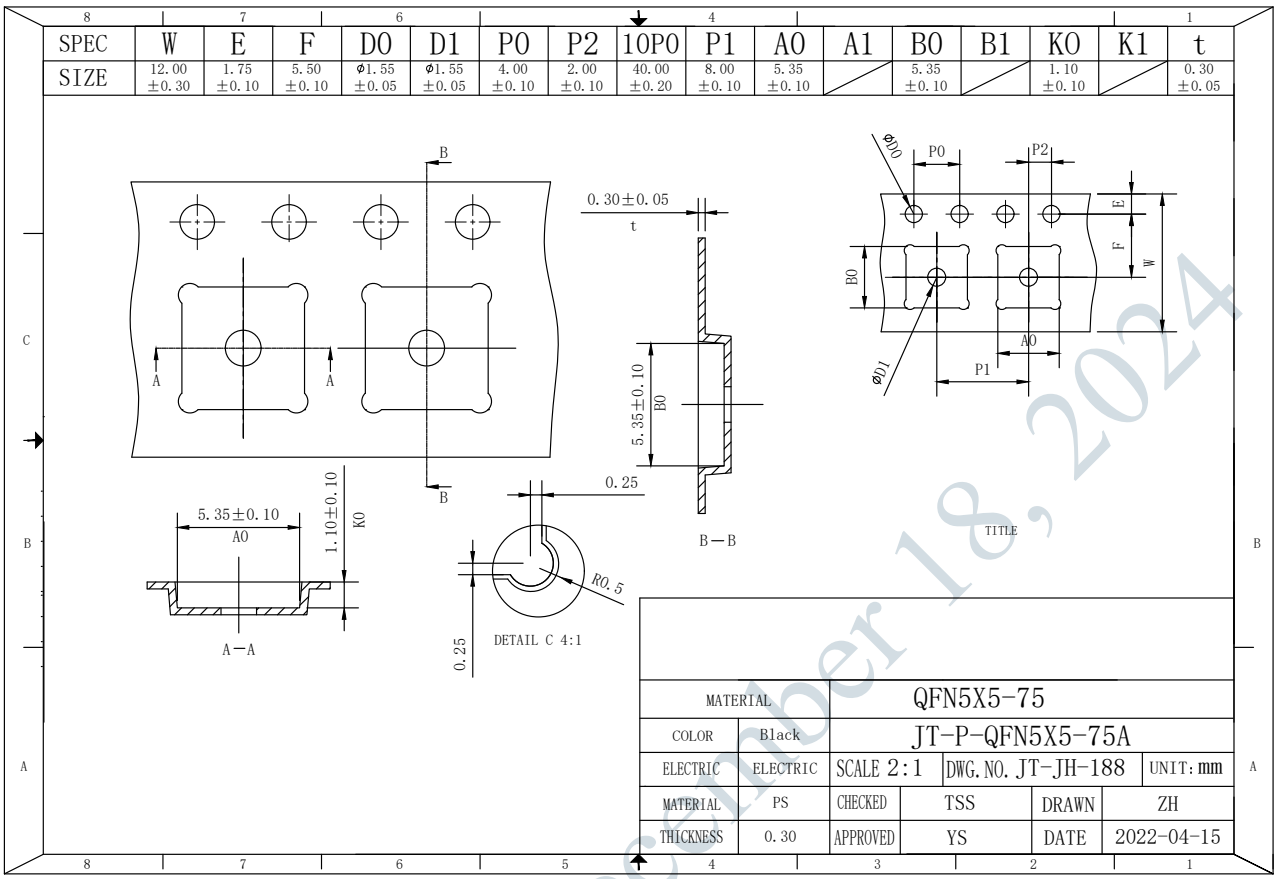



Figure 11: AIC8800M80P Reel Information

## 10.3 Product Identification

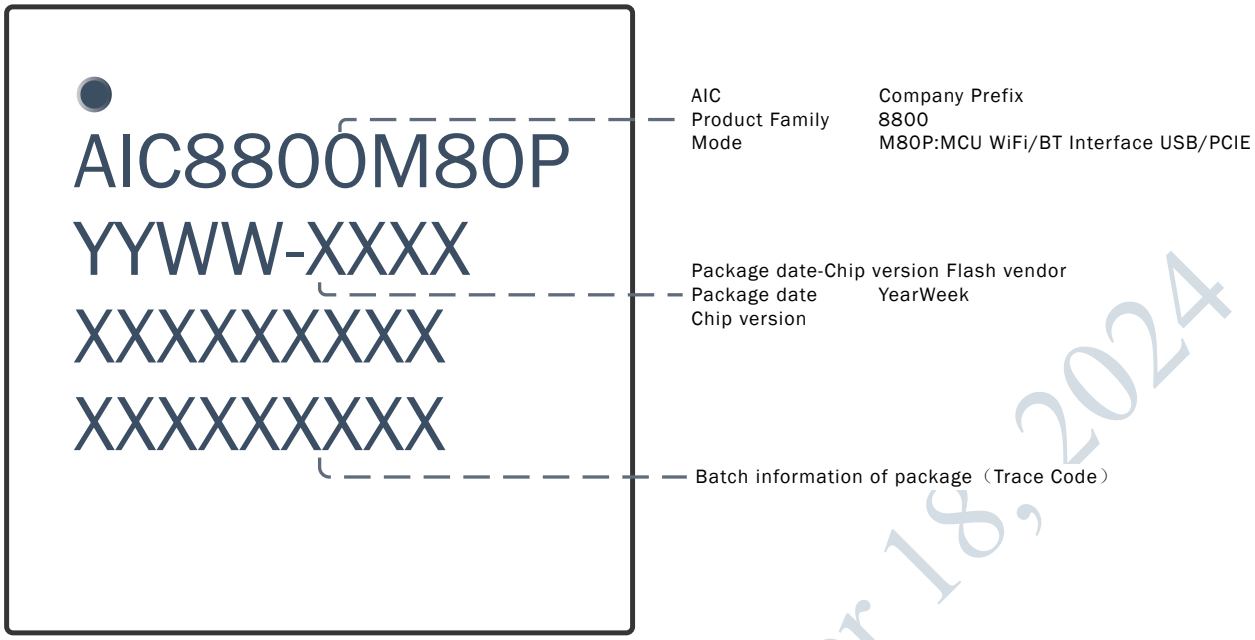



Figure 12: AIC8800M80P Silk Screen

## 10.4 Package Thermal Characteristics

Table 15: Package Thermal Characteristics

| **Characteristic** | **Value** |
|---|---|
| $\theta_{JA}$ in still air(°C/W) | 46.46 |
| $\theta_{JB}$ (°C/W) | 4.657 |
| $\theta_{JC}$ (°C/W) | 9.759 |
| $\psi_{JT}$ (°C/W) | 0.3 |
| $\psi_{JB}$ (°C/W) | 3 |
| Maximum junction temperature $T_j$ (°C) | 125 |
| Maximum power dissipation (W) | 1.5 |

## 10.5 Ording information

Table 16: Ordering Information

| **Part Number** | **Package** | **Description** | **Operating Ambient Temperature** |
|---|---|---|---|
| AIC8800M80P | 48 pin QFN package 5mm*5mm, 0.35mm pitch | Dual-band 2.4GHz and 5GHz WiFi6+Bluetooth 5.4 | −20 °C to 80 °C |

# 11 Reliability characteristics

Table 17: Reliability characteristics

| Test Items | Test Condition | Test Criteria |
|---|---|---|
| HTOL | $T_j$=125 °C, 1000hrs, 1.1Vcc | JESD22-A108 |
| LTOL | $T_a$=−40 °C, 1000hrs, 1.1Vcc | JESD22-A108 |
| ESD | HBM:±2000V Class 2 | JS-001-2023 |
| | CDM:±250V Class C1 | JS-002-2022 |
| LU | ±200mA Class I | JESD78F.02-2023 |
| Solder ability | steam aging:8hrs; 245 °C, 5s | J-STD-002D-2013 |
| HTST | 150 °C (500/1000hrs) | JESD22-A103 |
| LTST | −40 °C (168/1000hrs) | JESD22-A119 |
| TCT | −65 °C to 150 °C, Dwell=15min, 500/1000Cycles | JESD22-A104E-2014 |
| PCT | 121 °C, 100%RH, 205kPa, 96/168hrs | JESD22-A102E-2015 |
| UHAST | 130 °C, 85%RH, 33.3psia, 96hrs | JESD22-A118 |
| BHAST | 130 °C, 85%RH, 33.3psia, 1.1Vcc, 96hrs | JESD22-A110E.01-2021 |
| Precon MSL3 | Level 3, Bake: 125 °C, 24hrs. Moisture Soak:30 °C,60%, 192hrs. Reflow : 260 °C, 3 times | JESD22-A113 |

# 12 Solder Reflow Profile

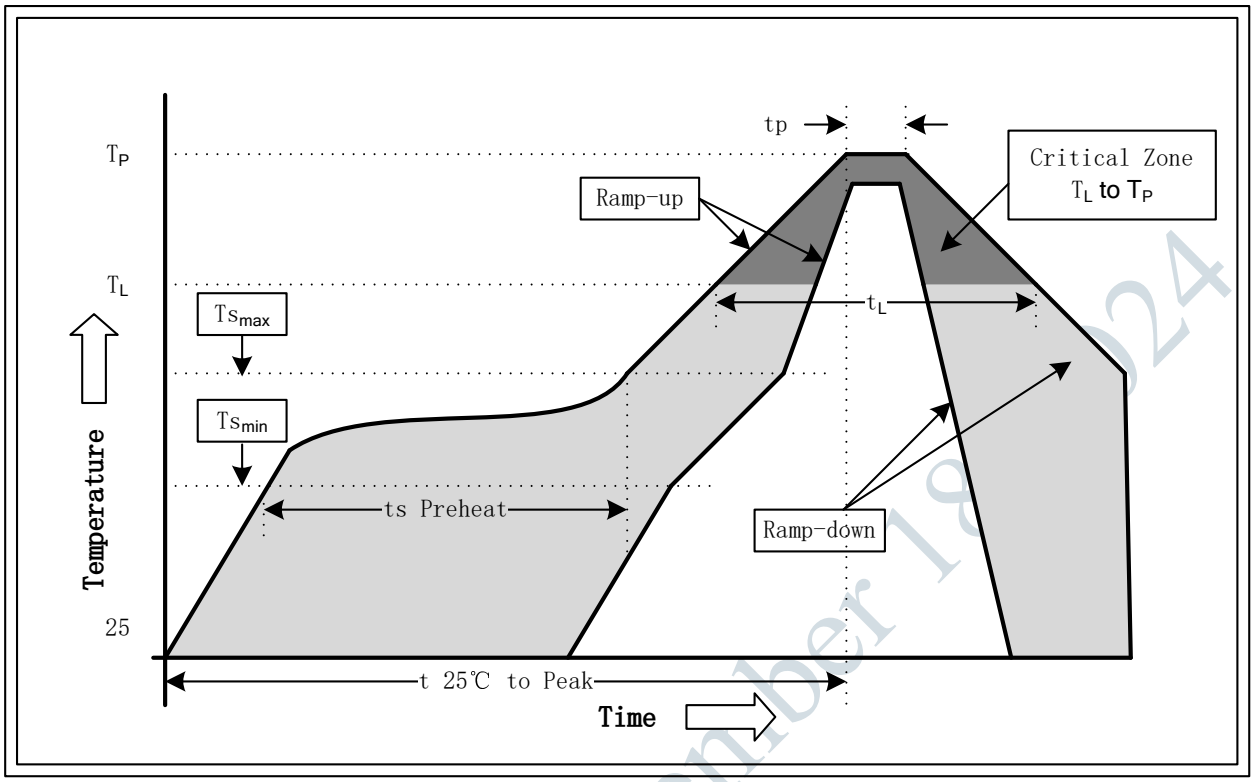



Figure 13: Classification Reflow Profile

Table 18: Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| Average Ramp-Up Rate (TSmax to Tp) | 3 °C/second max. | 3 °C/second max. |
| Preheat<br>-Temperature Min (Tsmin)<br>-Temperature Max (Tsmax)<br>-Time (tsmin to tsmax) | <br>100 °C<br>100 °C<br>60-120 seconds | <br>150 °C<br>200 °C<br>60-180 seconds |
| Time maintained above:<br>-Temperature (TL)<br>-Time (tL) | <br>183 °C<br>60-150seconds | <br>217 °C<br>60-150 seconds |
| Peak /Classification Temperature(Tp) | See the table 19 | See Table 20 |
| Time within 5 oC of actual Peak Temperature (tp) | 10-30 seconds | 20-40 seconds |
| Ramp-Down Rate | 6 °C/second max. | 6 °C/seconds max. |
| Time 25 oC to Peak Temperature | 6 minutes max. | 8 minutes max. |

Table 19: Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

| Package Thickness | Volume mm3 <350 | Volume mm3 ≥350 |
|---|---|---|
| <2.5mm | 240 + 0/-5 °C | 225 + 0/-5 °C |
| ≥2.5mm | 225 + 0/-5 °C | 225 + 0/-5 °C |

Table 20: Pb-free Process – Package Classification Reflow Temperatures

| Package Thickness | Volume mm3 <350 | Volume mm3 350–2000 | Volume mm3 >2000 |
|---|---|---|---|
| <1.6mm | 260 + 0 °C * | 260 + 0 °C * | 260 + 0 °C * |
| 1.6mm–2.5mm | 260 + 0 °C * | 250 + 0 °C * | 245 + 0 °C * |
| ≥2.5mm | 250 + 0 °C * | 245 + 0 °C * | 245 + 0 °C * |
| *Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C ) at the rated MSL Level. | | | |

**Note 1**: All temperature refers topside of the package. Measured on the package body surface.
**Note 2**: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 20.
**Note 3**: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non integral heat sinks.
**Note 4**: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package maysill exist.
**Note 5**: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table 18, Table 19, Table 20 whether or not lead free.

# 13 Change List

The following Table 21 summarizes revisions to this document.

Table 21: Change List

| Rev | Date | Auther | Change description |
|---|---|---|---|
| V1.0.0 | 20230417 | AICSEMI | initial version |
| V1.0.1 | 20241205 | AICSEMI | Add the description of each power supply parameter<br>Add the description of interface<br>Add the description of GPIO<br>Modify the definition about pin 45 |

# 14 RoHS Compliant

The products meet the requirements of Directive 2011/65/EU of Europe Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). The products are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals.

# 15 ESD Sensitivity

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site. AIC products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment.

# 16 Disclaimer

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For technical questions and additional information about AICSEMI Inc.:
Website: www.AICSEMI.com
Mailbox: support@AICSEMI.com
AICSEMI (Shanghai), Inc.
Tel: +86-10-84097662
Fax: +86-10-84097662