Preliminary AIC8800DC Low-Energy Wi-Fi6/BT5.2 SoC

Data Sheet

Revision: 1.2
Apr 2024

1. General Description

AIC8800DC is a highly integrated chip 2.4GHz Wi-Fi6, BT5.2 for wireless application.

1.1 Wi-Fi Features

- CMOS single-chip fully-integrated RF, Modem and MAC
- Support 2.4GHz Wi-Fi6
- Support 20/40MHz bandwidth
- Data rates up to 286.8Mbps@TX and 229.4Mbps@RX
- RX sensitivity -99dBm in 11b 1M mode
- Tx power up to 20dBm in 11b mode, 18dBm in HT/VHT/HE40 MCS7 mode
- Support STA, AP, Wi-Fi Direct modes concurrently
- Support STBC, beamforming
- Support Wi-Fi6 TWT
- Support Two NAV, Buffer Report, Spatial reuse, Multi-BSSID, intra-PPDU power save
- Support LDPC
- Support MU-MIMO, OFDMA
- Support DCM, Mid-amble, UORA
- Support WEP/WPA/WPA2/WPA3-SAE Personal, MFP

1.2 BTDM5.2 Features

- Supports all the mandatory and optional features of Bluetooth 2.1+EDR/4.x/5.2
- Supports advanced master and slave topologies
- Use an optimization method to assess channel quality, AFH enhancement

1.3 Other Features

- Supports SDIO/USB2.0/HCI_UART/PCM interface
- Integrated low power timer and watchdog
- 512 bits eFuse

1.4 Packaging Information

- Compact profile package：4mm×4mm×0.85mm QFN36

1.5 Applications

- IoT device
- Wireless device

2. Platform Description

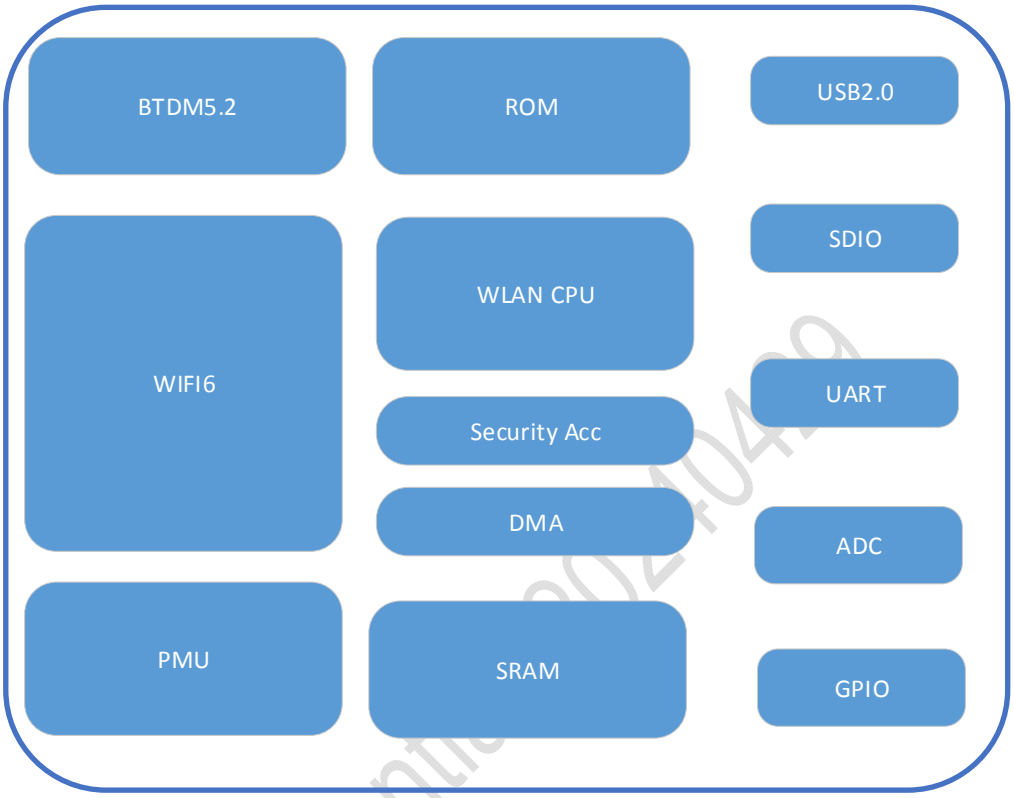


Figure2-1 AIC8800DC Block Diagram

3. Electrical Characteristics

Table 3-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VBAT	Supply Voltage For System	2.97	3.3	3.63	V
V_RF	Supply Voltage For RF	1.2	1.4	1.5	V
V_CORE	Supply Voltage For Digital	0.8	0.9	1	V
AVDD18	Supply Voltage For Efuse	1.62	1.8	1.98	V
θ JA			45.9		℃/W
θ JB			12.3		℃/W
θ JC			22.3		℃/W
T_j	Maximum Junction Temperature			125	℃
T_{amb}	Ambient Temperature	-20	27	+80	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VIO	V
V_{IH}	CMOS High Level Input Voltage	0.7*VIO		VIO	V
V_{TH}	CMOS Threshold Voltage		0.5*VIO		V

4. PINS Description

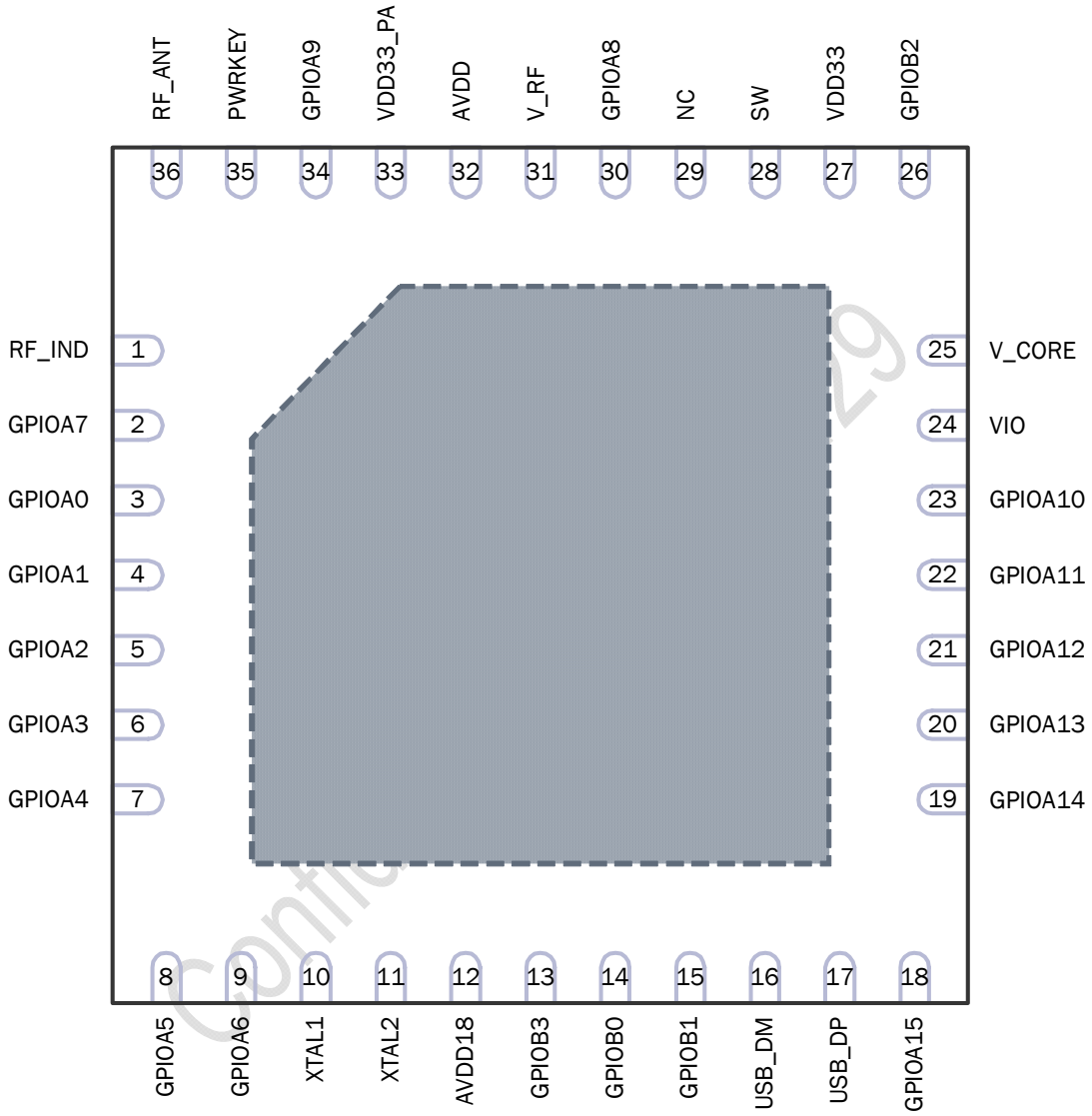


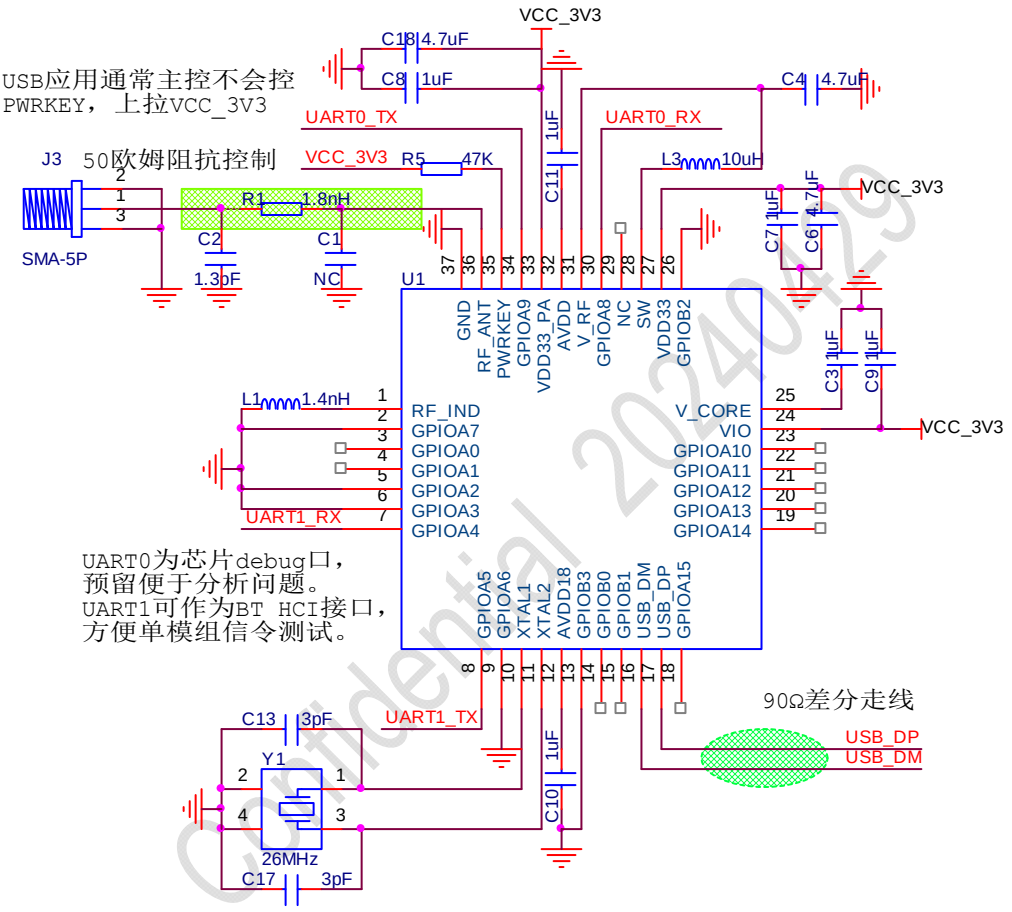
Figure 4-1 AIC8800DC Pin Map

Table 4-1 AIC8800DC Pins Description

PIN NAME	QFN NO.	I/O	DESCRIPTION
RF			
RF_ANT	36	I/O	RF 2.4G, support BT Dual Mode
RF_IND	1		RF ground, connect a 1.4nH inductor to ground
PMU			
PWRKEY	35	I	Power Key, high level effective, Internal 200K pull-down resistance
V_RF	31	I	RF supply voltage
NC	29		NC
VDD33	27	I	System supply voltage
AVDD	32		Connect a 1uF decoupling capacitor to ground
VDD33_PA	33	I	RF PA voltage input
AVDD18	12	O	1.8V voltage output, supply voltage for internal Efuse, connect a 1uF decoupling capacitor to ground
VIO	24	I	IO Power Supply, support 1.8/3.3v
SW	28	O	Supply voltage for V_RF
V_CORE	25	I	Digital core circuit supply voltage, connect a 1uF decoupling capacitor to ground
CLK			
XTAL1	10	I	Crystal input. If Crystal save mode XTAL1 through a 100 pF coupling capacitor, in this mode, XTAL2 must be tied to ground
XTAL2	11	O	Crystal output. If Crystal save mode XTAL2 must be tied to ground
GPIO			
GPIOA0	3	I/O	GPIO
GPIOA1	4	I/O	GPIO
GPIOA2	5	I/O	GPIO
GPIOA3	6	I/O	GPIO
GPIOA4	7	I/O	GPIO
GPIOA5	8	I/O	GPIO
GPIOA6	9	I/O	GPIO
GPIOA7	2	I/O	GPIO
GPIOA8	30	I/O	GPIO
GPIOA9	34	I/O	GPIO
GPIOA10	23	I/O	GPIO
GPIOA11	22	I/O	GPIO
GPIOA12	21	I/O	GPIO
GPIOA13	20	I/O	GPIO
GPIOA14	19	I/O	GPIO
GPIOA15	18	I/O	GPIO
GPIOB0	14	I/O	GPIO
GPIOB1	15	I/O	GPIO
GPIOB2	26	I/O	GPIO
GPIOB3	13	I/O	GPIO
USB_DM	16	I/O	USB data minus
USB_DP	17	I/O	USB data plus

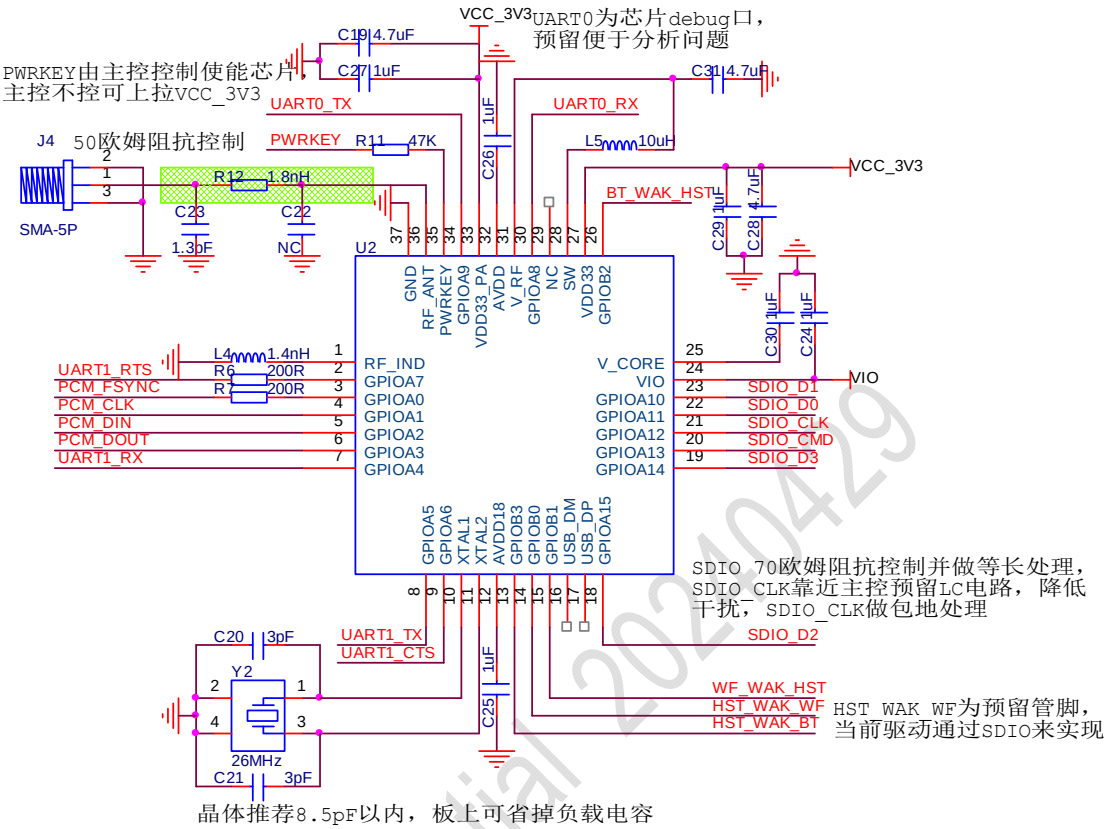
5. Application Circuit

5.1 USB application circuit



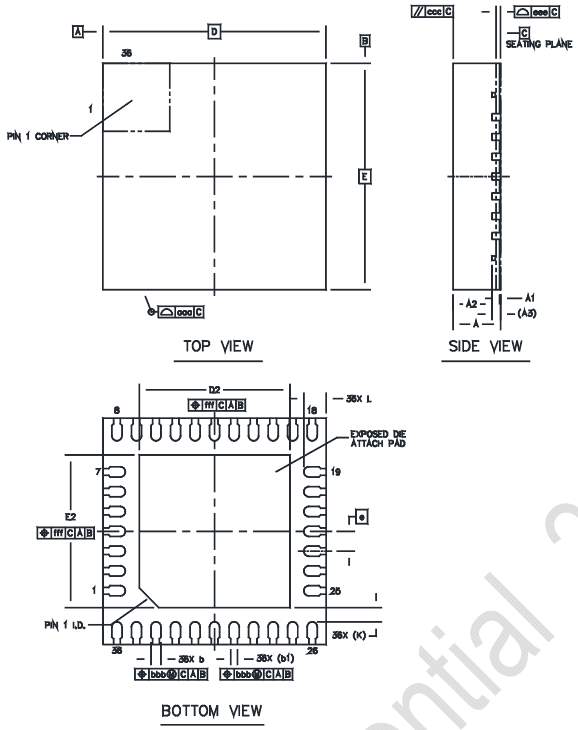
晶体推荐8.5pF以内，板上可省掉负载电容

5.2 SDIO application circuit



6. Package Physical Dimension

6.1 Package Dimensions

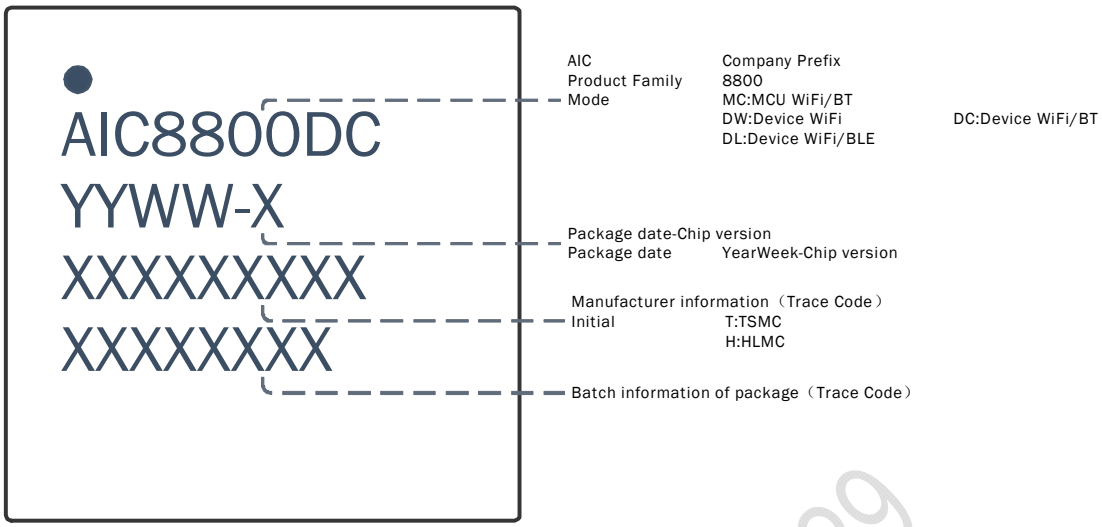


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
		b1		0.12 REF	
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	2.6	2.7	2.8
	Y	E2	2.6	2.7	2.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP：Sn8~20u

Figure 6-1 AIC8800DC-QFN36

6.2 Product Identification



	Band	BW	5G Fem	Package	Type	BT	Interface	Flash	Psram	Vbat Range（v）	Operating tem(℃)
DC	2.4G	20/40	No	4x4 QFN36	Device	BTDM5.2	USB2.0/SDIO2.0	No	No	3~3.6	-20~80
DW	2.4G	20/40	No	4x4 QFN36	Device	No	USB2.0/SDIO2.0	No	No	3~3.6	-20~80
DL	2.4G	20/40	No	4x4 QFN36	Device	BLE5.2	USB2.0/SDIO2.0	No	No	3~3.6	-20~80
MC	2.4G	20/40	No	4x4 QFN36	MCU	BTDM5.2	USB2.0/SDIO2.0	Integration	No	2.3~5	-20~80
FC	2.4G	20/40	No	4x4 QFN36	MCU	No	USB2.0/SDIO2.0	External	No	2.3~5	-20~80

7. Reliability characteristics

Table 7-1 Reliability test report

Test Items	Test Condition	Test Criteria
HTOL	Tj≥125℃ 2000hrs	JESD22-A108F
ESD	HBM:±3000V Class 2	JS-001-2017
	CDM:±800V Class C2b	JS-002-2018
Latch up	±800mA Class Ⅰ	JESD78
Solder ability	Steam aging:8hrs; 245℃, 5s	J-STD-002D-2013
High Temperature Storage	150℃ （1000h）	JESD22-A103
TCT	-65℃～ 150℃, Dwell=15min, 500/1000Cycles	JESD22-A104E-2014
uHAST	130 ℃ /85%RH/ 33.3psig/96hrs	JESD22-A118
PCT	121℃, 100%RH, 205 kPa, 96/168hrs	JESD22-A102E-2015
Moisture sensitivity level	Level 3 Bake:125℃,24hrs Soak:30℃,60%	J-STD-020D

8. Solder Reflow Profile

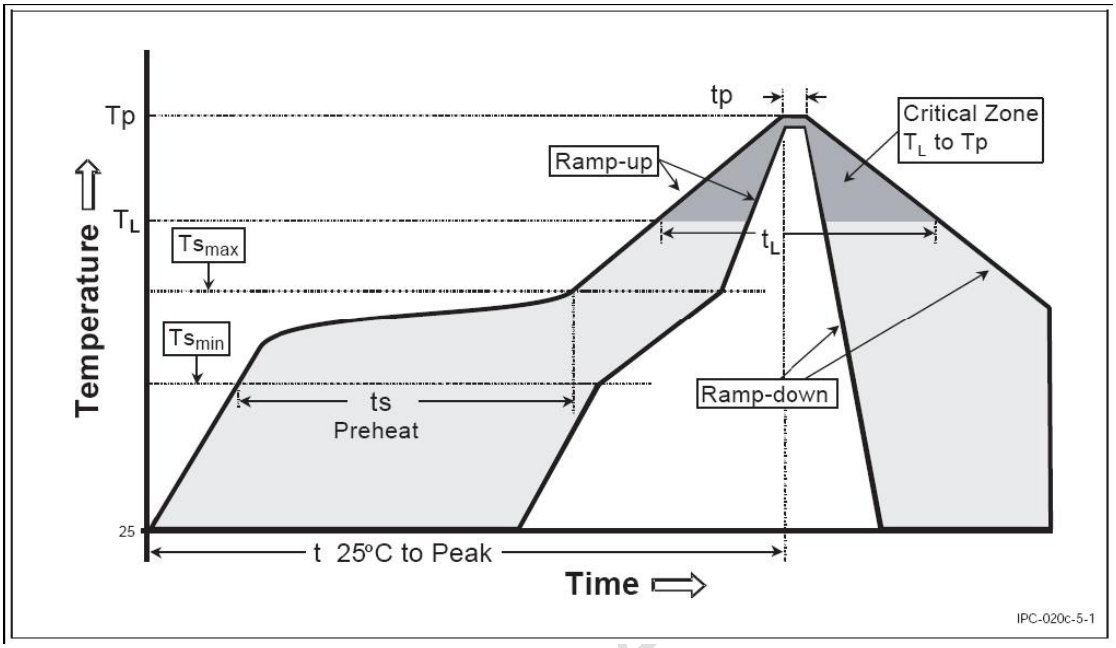


Figure.8-1 Classification Reflow Profile

Table 8-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	3 ℃/second max.	3 ℃/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	 100 ℃ 100 ℃ 60-120 seconds	 150 ℃ 200 ℃ 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 183 ℃ 60-150seconds	 217℃ 60-150 seconds
Peak /Classification Temperature(Tp)	See Table 8-2	See Table 8-3
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 ℃/second max.	6 ℃/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 8-2 Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
＜2.5mm	240 + 0/-5 ℃	225 + 0/-5 ℃
≥2.5mm	225 + 0/-5 ℃	225 + 0/-5 ℃

Table 8-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 ＜350	Volume mm3 350-2000	Volume mm3 ＞2000
＜1.6mm	260 + 0 ℃ *	260 + 0 ℃ *	260 + 0 ℃ *
1.6mm – 2.5mm	260 + 0 ℃ *	250 + 0 ℃ *	245 + 0 ℃ *
≥2.5mm	250 + 0 ℃ *	245 + 0 ℃ *	245 + 0 ℃ *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 ℃. For example 260+ 0 ℃) at the rated MSL Level.			

Note 1: All temperature refers topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ℃, - X ℃ (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 ℃. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 8-3.

Note 3: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package maysill exist.

Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table8-1, 8-2, 8-3 whether or not lead free.

9. Change List

The following table summarizes revisions to this document.

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	20220520	AICSEMI	Initial version
1.1	20230228	AICSEMI	Release version
1.2	20240429	AICSEMI	▪ Modify silkscreen information ▪ Update the application circuit

10. RoHS Compliant

The products meet the requirements of Directive 2011/65/EU of Europe Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). The products are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals.

11. ESD Sensitivity

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site. AIC products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment.

12. Disclaimer

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