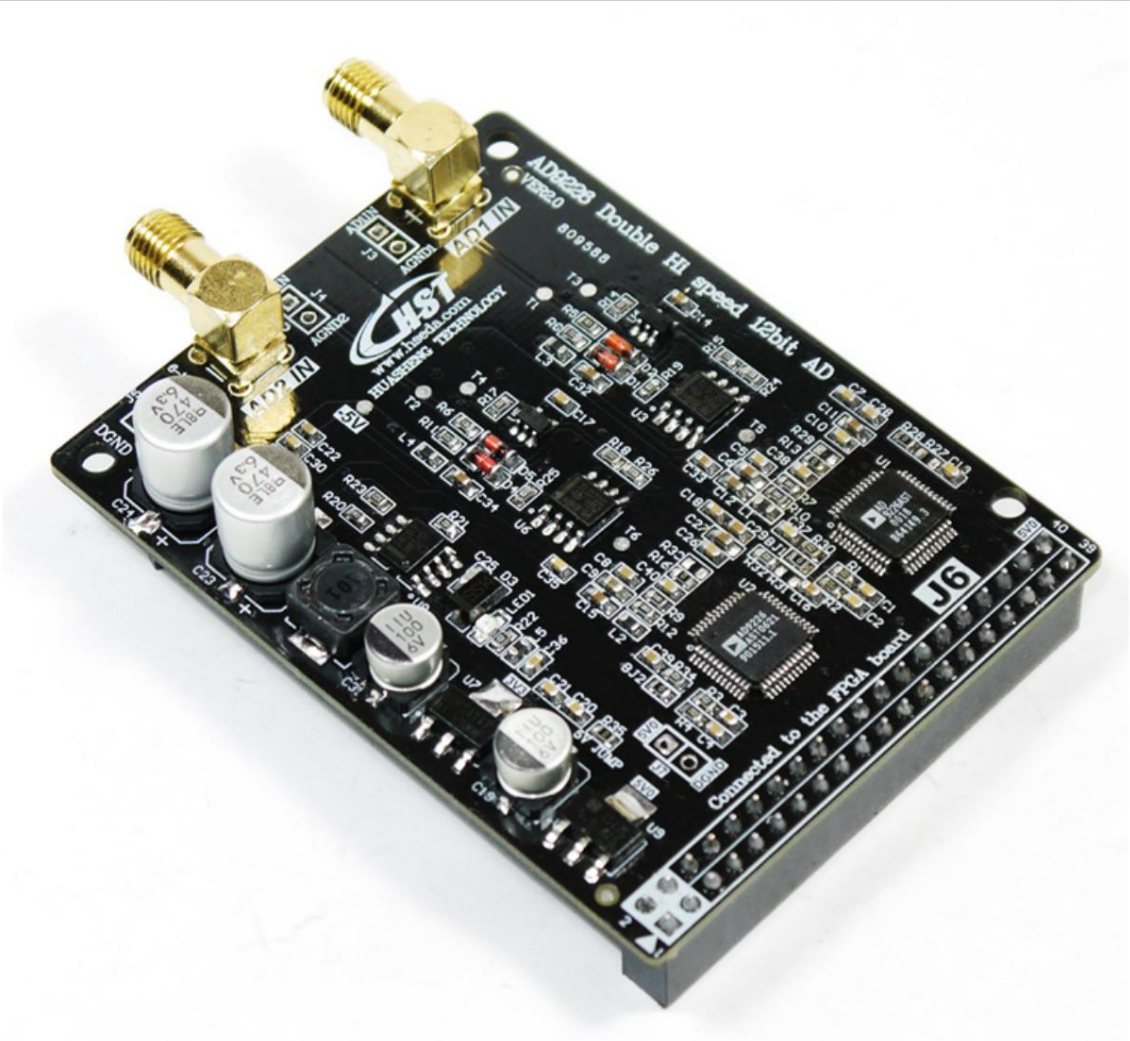
HSEDA

High Speed Dual Channel AD Acquisition Module User Manual

VER2.0



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http://www.hseda.com

content

content.....2

1. **Module parameters**.....3

2. **Module structure** 3

3. Introduction to **AD9226** 4

Four, **AD9226** functional block diagram 5

5. **AD9226** Timing Diagram 5

6. **AD9226** configuration 5

7. **Attenuator circuit**.....8

Eight, **AD8065** operational amplifier 9

Nine, **interface definition** 9

10. AD experiment operation steps 10

11. **SignalTap II waveforms** 11

12. **System combination photos** 12

13. **Experiment Display** 14

14. **Frequently Asked Questions about Experiments** 16

1. Module parameters

ÿModule model: HSAD9226V2.0

ÿ AD model: AD9226;

ÿNumber of channels: 2 channels;

ÿ AD digits: 12bit;

ÿ Maximum sampling rate: 65MSPS;

ÿInput signal voltage range: -5V~+5V;

ÿ Power supply: single 5V or 6-12V input

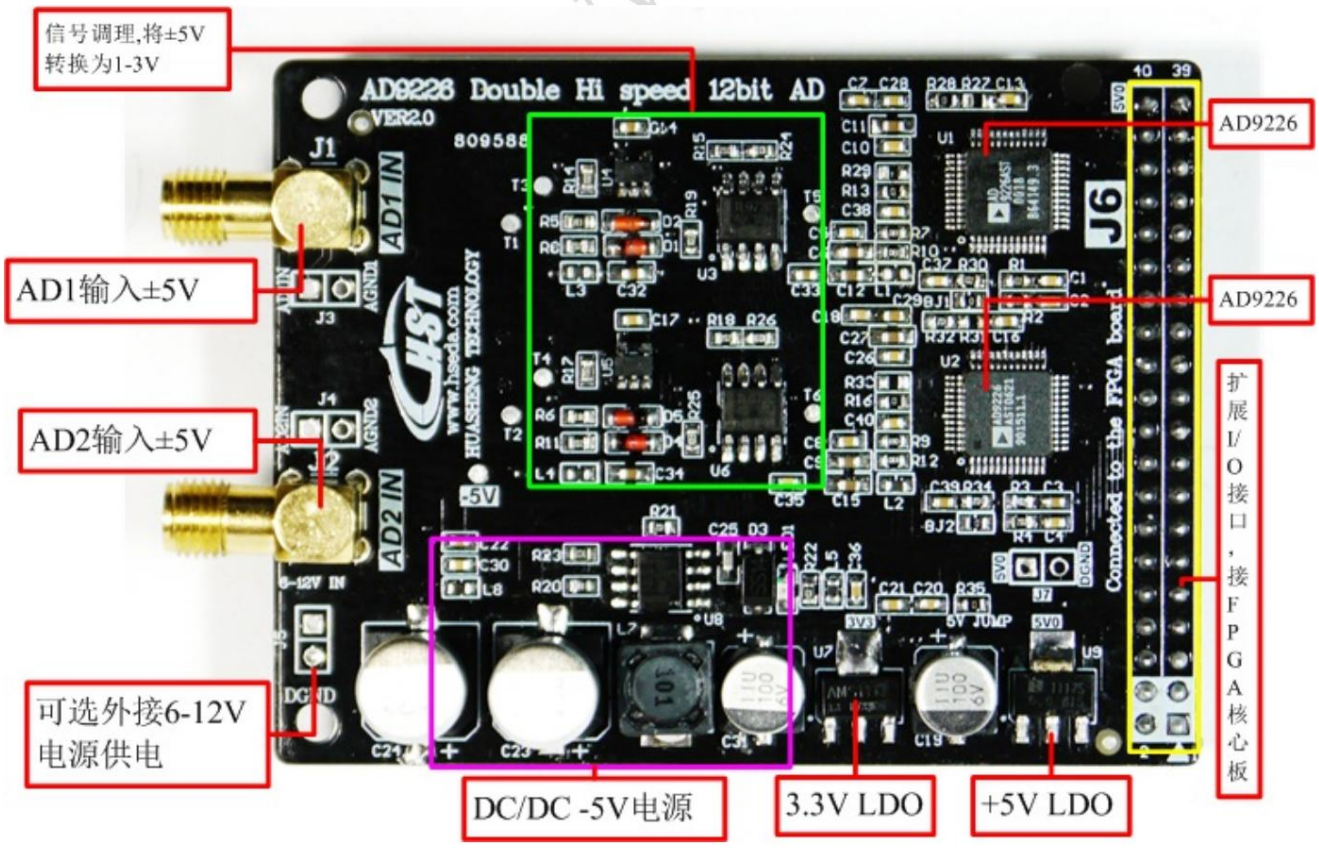
ÿThe number of PCB layers of the module: 2 layers, senior engineer wiring, separation of digital and analog power supply and GND;

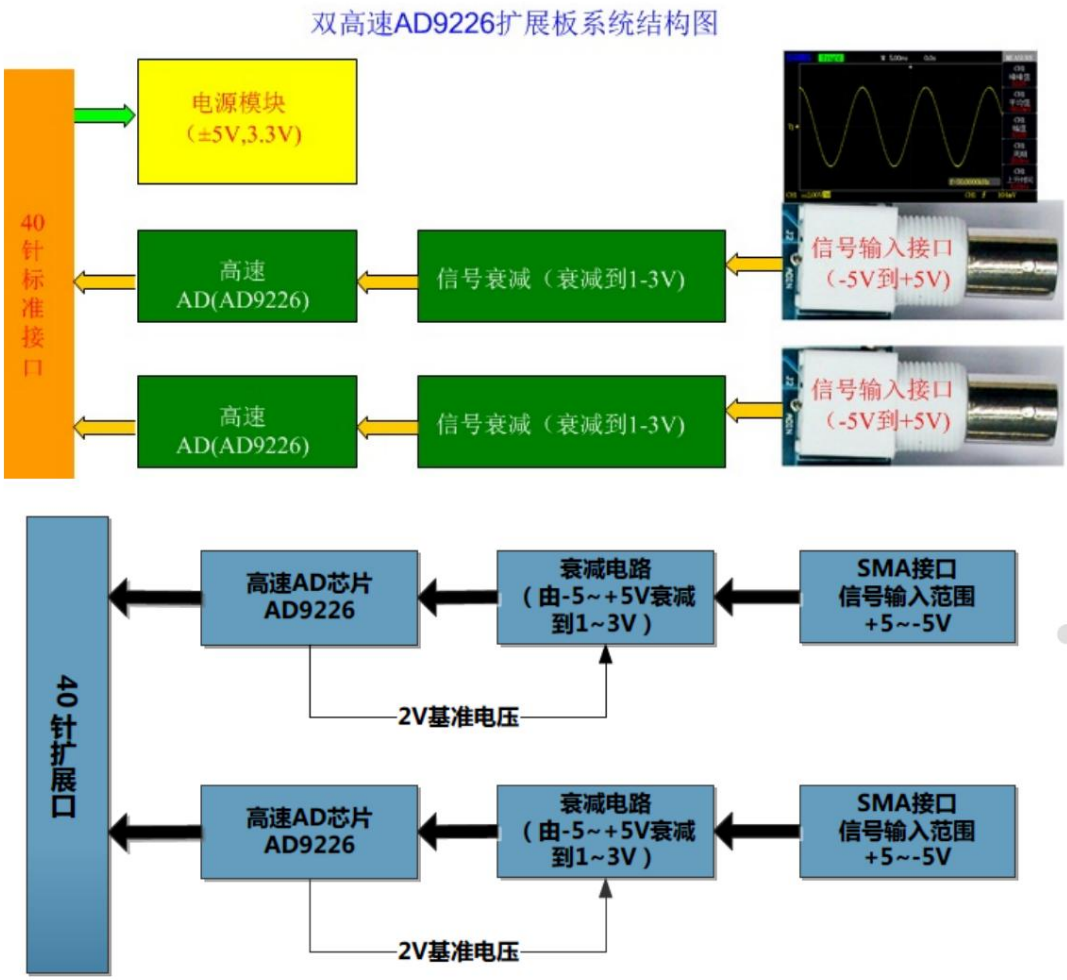
ÿ Module interface: 40-pin 2.54mm pitch row seat, the direction is downward;

ÿWorking temperature: -40°~85° The chips used in the module meet the industrial temperature range

ÿInput interface: SMA interface and 2.54MM pitch pin header

2. Module structure





3. Introduction to **AD9226**

The dual-channel 12bit AD acquisition module adopts two pieces of AD9226 from ADI. This chip is a single-chip,

12-bit, 65 MSPS analog-to-digital converter (ADC) with single-supply operation and an on-chip high-performance track-and-hold amplifier

and reference voltage source. It uses a multi-stage differential pipeline architecture with data rates up to 65 MSPS over the entire operating temperature range

Guaranteed no missing codes.

The ADC uses a high-speed, low-cost CMOS process and a novel architecture that achieves the resolution and speed of existing bipolar

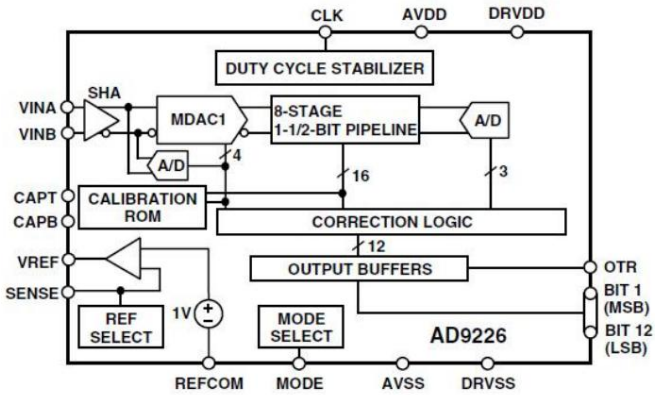
the level of performance solutions at a much lower cost of power consumption.

The input of the AD9226 enables easy interfacing with imaging, ultrasound, and communication systems. Using a true differential input structure, the user can

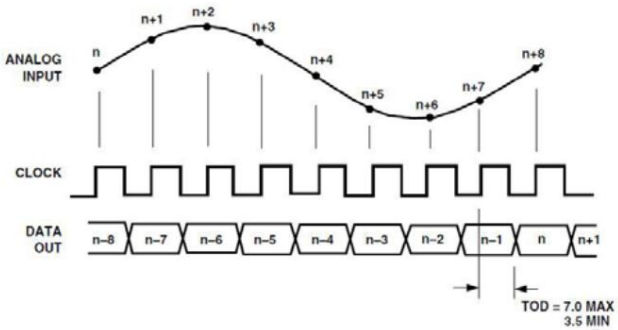
to select various input ranges and offsets including single-ended applications. Dynamic performance is excellent. Sample-and-hold amplifiers are suitable for multiplexed systems that switch full-scale levels in consecutive channels, or

Suitable for sampling single-channel inputs at the highest Nyquist rate and higher.

Four, **AD9226** functional block diagram



Five, **AD9226** timing diagram



Through this timing diagram, we can see that there is no need to configure the AD chip, we only need to provide the clock

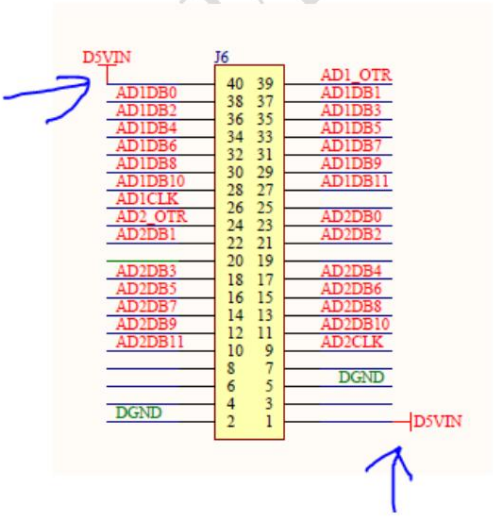
CLOCK, the chip can directly collect data, and the operation is very simple.

Six, **AD9226** configuration

Module power supply

options: There are two

power supply methods. The first: we can choose to use J6's 1 pin or 40 pin to provide 5V power supply directly from the FPGA core board.

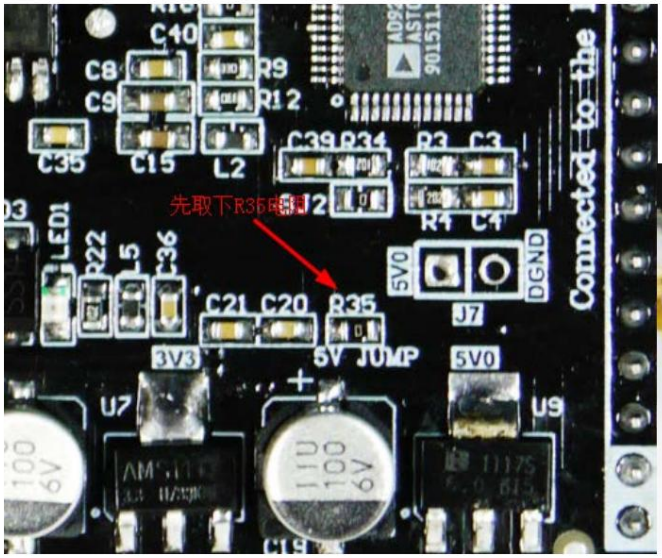


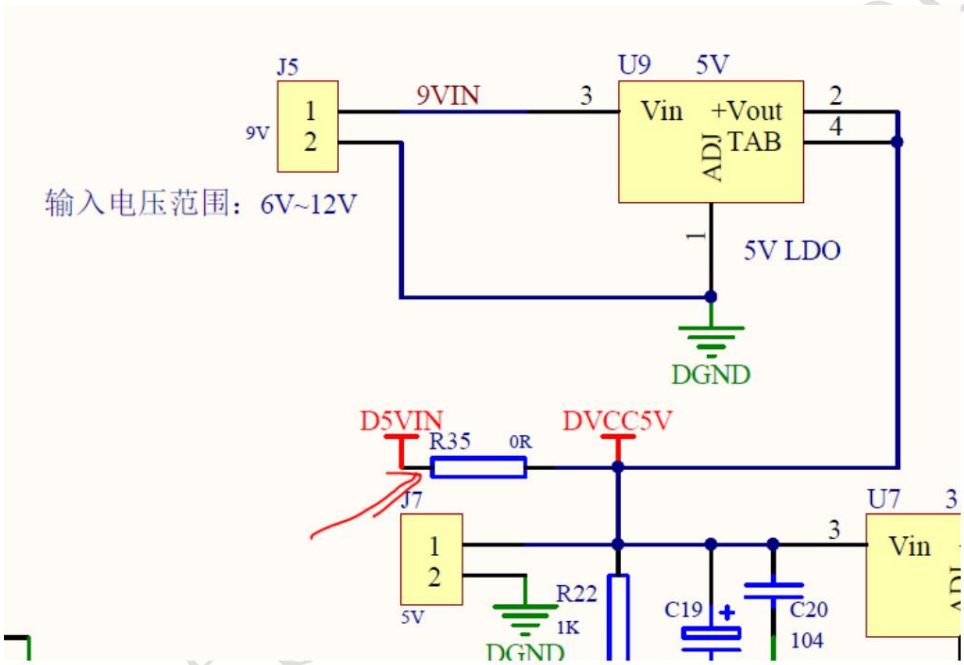
The second: we can use J5 on the board to provide 6-12 power supply, because there is a 5V LDO chip on the board. Therefore, low noise and high stability can be obtained.

fixed 5V power supply. To supply power in this way, first remove the **R35** resistor on the board . Only then can the module be powered individually. Otherwise it is possible

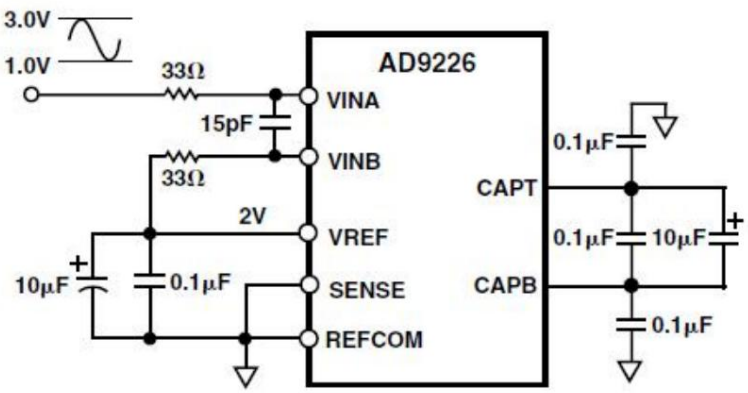
The 5V power is input to the FPGA core board through the J6 input through this resistor. Thus damaging the FPGA core board. Please be careful after removing **R35**

can be powered in this way.





AD chip working mode configuration description:



According to the figure above, we configure the AD9226 as a single-ended input mode with an input range of 1.0V-3.0V. In this mode

In the formula, VREF is the reference voltage of 2V, and the input range of VINA is 1.0-3.0V.

Let me explain here that there are a few points to pay attention to in the AD9226 when designing the hardware:

1. AD9226 This chip supports differential input and single-ended input, and can be used according to the design requirements.

To make a choice, we choose the single-ended input mode when designing. For other modes, see AD9226 chip hand

book.

2. The circuit we designed selects the AD9226 internal reference source, VREF is the reference voltage output port, which can provide

Two reference voltages, 1V and 2V. It is selected by SENSE. When SENSE is connected to GND, it provides

2V reference; 1V reference is provided when SENSE is connected to VREF. The connection we choose is

Provides a connection for a 2V reference voltage. We use this 2V reference voltage in the circuit to design the attenuation

circuit, please refer to the schematic diagram for details.

3. The input range of VINA is determined by VREF. When VREF=2V, the input range of VINA is

2V (3V-1V=2V); when VREF=1V, the input range of VINA is 1V (1.5V-0.5V=1V).

Pin 35 and pin 43 MODE have the function of data format selection, the output data format of AD9226 has two

kinds, Binary Output Mode and Two's Complement Mode.

The following table shows the mode selection,

Table II. DFS Pin Controls

DFS Function	Pin 35 Connection
Straight Binary	AVSS
Two's Complement	AVDD

Table III. Clock Stabilizer Pin

Clock Restore Function	Pin 43 Connection
Clock Stabilizer Enabled	AVDD
Clock Stabilizer Disabled	AVSS

From this table, we can see that when pin 35 is connected to AVDD, the selection mode is Two's Complement

Mode, when connected to AVSS, the selection mode is Binary Output Mode. When designing, we chose

Binary Output Mode means that R27 and R29 on the board are not installed. If installed, it is Two's Complement

Mode.

The following table shows the difference between the two modes and the output data format

Note: This table is provided by the official document, but we think there are still errors in it. After our test, when VREF=2V

When it should be VIN-VINB=-1/2VREF=-1 or 1/2VREF=1, the corresponding values are 1000 000

000 or 0111 1111 1111, not -VREF or VREF as mentioned above, because at this time, VINB=2V, and

The range of VINA is 1V~3V, and the range of VINA-VINB is -1V~1V, namely -1/2VREF~1/2VREF. everyone can

Test to see if this is the case, if there is a problem, you can contact us to discuss and correct it.

The OTR pin of AD9226 is Out of Range, that is, the input voltage range detection function.

We can judge whether the input voltage exceeds the range where the chip is designed. The following table is the truth table

When OTR is 1, it means that the voltage range we have collected exceeds the design range.

Input (V)	Condition (V)	Binary Output Mode	Two's Complement Mode	OTR
VINA–VINB	< – VREF	0000 0000 0000	1000 0000 0000	1
VINA–VINB	= – VREF	0000 0000 0000	1000 0000 0000	0
VINA–VINB	= 0	1000 0000 0000	0000 0000 0000	0
VINA–VINB	= + VREF – 1 LSB	1111 1111 1111	0111 1111 1111	0
VINA–VINB	≥ + VREF	1111 1111 1111	0111 1111 1111	1

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

Seven, attenuation circuit

The function of the attenuation circuit is to reduce the input voltage according to a certain proportion to make it meet the input of the AD input.

Scope. Generally, the input range of the AD input terminal is very small. Take AD9226 as an example. We set its voltage input range as

1.0V-3.0V, and we need to meet the voltage input range of -5V to +5V, then we will be -5V to +5V voltage

It can be reduced to the range of 1V-3V. Therefore, the function of the attenuation circuit is produced. We have designed a meeting

For the attenuation circuit required above, his conversion formula is:

Vout=(1/5)Vin+2

When Vin=-5V, Vout=1V; When Vin=5V, Vout=3V;

Just meet our above requirements. After converting to a digital signal, reverse the above conversion formula to convert the digital signal Amplify to get the true value of the input voltage.

Note: After the signal passes through the attenuation circuit, there will be a certain error, we can regard its error as a linear error, Manual calibration of the signal reduces the margin of error.

Eight, **AD8065** operational amplifier

In the attenuation circuit, we use a high-performance, 145MHz operational amplifier AD8065, AD8065

FastFET The amplifiers are voltage feedback amplifiers with FET inputs for excellent performance and ease of use. AD8065 is

Single amplifier, fabricated on Analog Devices' proprietary XFCB process, operates with very low noise (7.0 nV/ÿHz and 0.6

fA/ÿHz), the input impedance is very high.

The AD8065 has a wide supply voltage range of 5V to 24V, can operate from a single supply, and has a bandwidth of 145MHz, suitable for various applications. Additionally, these amplifiers feature rail-to-rail outputs, making them even more versatile.

Despite the low cost, these devices still provide excellent overall performance. The differential gain and phase error of these amplifiers 0.02% and 0.02°, and 0.1 dB flatness at 7 MHz, ideal for video applications. In addition, these devices

Features a high slew rate of 180 V/îs, excellent distortion performance (-88 dBc spurious free dynamic range (SFDR) at 1 MHz),

Very high common-mode rejection (ÿ100 dB) and low input offset voltage (1.5 mV, max at warm-up).

With only a typical supply current of 6.4 mA per amplifier, the AD8065/AD8066 are capable of driving up to 30 mA

load current.

9. Interface Definition

illustrate:

The data bits of **AD9226** are reversed. For example, **AD2DB11** corresponds to data bit **D0. AD2DB0 corresponds to data D11.** Be careful, if the user when using it yourself.

(The triangle arrow pin with a box on the **PCB** is pin **1)**

Dual AD9226 corresponding pins (EP4CE30 VER2.0/3.0/4.0 Core board J11)					Dual AD9226 corresponding pins (EP4CE30 VER2.0/3.0/4.0 core board J6)			
Device Name	U1 AD1	U2 AD2	**FPGA** mapping shoot pin		Device Name	U1 AD1	U2 AD2	**FPGA** mapping shoot pin
J11-1			5V		J6-1			5V
J11-2			GND		J6-2			GND

J11-3			PIN_B22	J6-3			PIN_A11
J11-4			PIN_C20	J6-4			PIN_B12
J11-5			GND	J6-5			GND
J11-6			PIN_C22	J6-6			PIN_F11
J11-7			PIN_D20	J6-7			PIN_E11
J11-8			PIN_D21	J6-8			PIN_E12
J11-9		AD2CLK	PIN_D22	J6-9		AD2CLK	PIN_G13
J11-10		AD2DB11	PIN_E21	J6-10		AD2DB11	PIN_F13
J11-11		AD2DB10	PIN_E22	J6-11		AD2DB10	PIN_E13
J11-12		AD2DB9	PIN_F17	J6-12		AD2DB9	PIN_D13
J11-13		AD2DB8	PIN_F19	J6-13		AD2DB8	PIN_C13
J11-14		AD2DB7	PIN_F20	J6-14		AD2DB7	PIN_B13
J11-15		AD2DB6	PIN_F21	J6-15		AD2DB6	PIN_A13
J11-16		AD2DB5	PIN_F22	J6-16		AD2DB5	PIN_G14
J11-17		AD2DB4	PIN_G17	J6-17		AD2DB4	PIN_F14
J11-18		AD2DB3	PIN_G18	J6-18		AD2DB3	PIN_E14
J11-19			PIN_H17	J6-19			PIN_B14
J11-20			PIN_H18	J6-20			PIN_A14
J11-21		AD2DB2	PIN_H19	J6-21		AD2DB2	PIN_G15
J11-22		AD2DB1	PIN_H20	J6-22		AD2DB1	PIN_F15
J11-23		AD2DB0	PIN_H21	J6-23		AD2DB0	PIN_E15
J11-24		AD2_OTR	PIN_H22	J6-24		AD2_OTR	PIN_D15
J11-25			PIN_J17	J6-25			PIN_C15
J11-26	AD1CLK		PIN_J18	J6-26	AD1CLK		PIN_B15
J11-27	AD1DB11		PIN_J21	J6-27	AD1DB11		PIN_A15
J11-28	AD1DB10		PIN_J22	J6-28	AD1DB10		PIN_D17
J11-29	AD1DB9		PIN_K17	J6-29	AD1DB9		PIN_C17
J11-30	AD1DB8		PIN_K18	J6-30	AD1DB8		PIN_B17
J11-31	AD1DB7		PIN_K19	J6-31	AD1DB7		PIN_A17
J11-32	AD1DB6		PIN_K21	J6-32	AD1DB6		PIN_B18
J11-33	AD1DB5		PIN_K22	J6-33	AD1DB5		PIN_A18
J11-34	AD1DB4		PIN_L21	J6-34	AD1DB4		PIN_D19
J11-35	AD1DB3		PIN_L22	J6-35	AD1DB3		PIN_C19
J11-36	AD1DB2		PIN_M19	J6-36	AD1DB2		PIN_B19
J11-37	AD1DB1		PIN_M20	J6-37	AD1DB1		PIN_A19
J11-38	AD1DB0		PIN_M21	J6-38	AD1DB0		PIN_B20
J11-39	AD1_OTR		PIN_M22	J6-39	AD1_OTR		PIN_A20
J11-40			5V	J6-40			5V

Ten, AD experiment operation steps

1. First, connect the AD module to the 40-pin standard expansion port of the FPGA development board (in the case of power down).

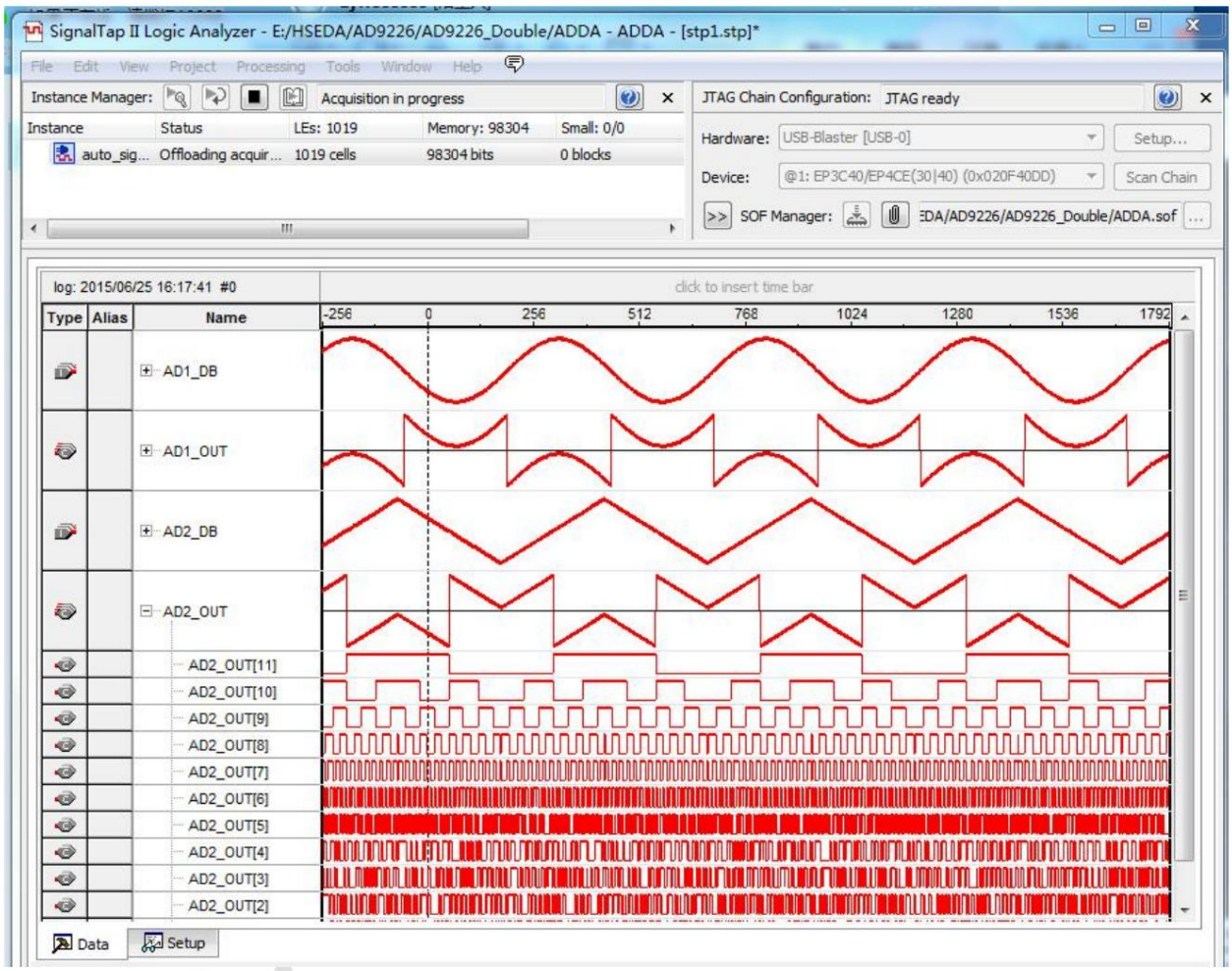
2. Connect your signal source to the AD input port (Note: AD port input range: -5V~+5V).

3. Using the Quartus II software, download the program to the FPGA (the test program is available for download in our forum).

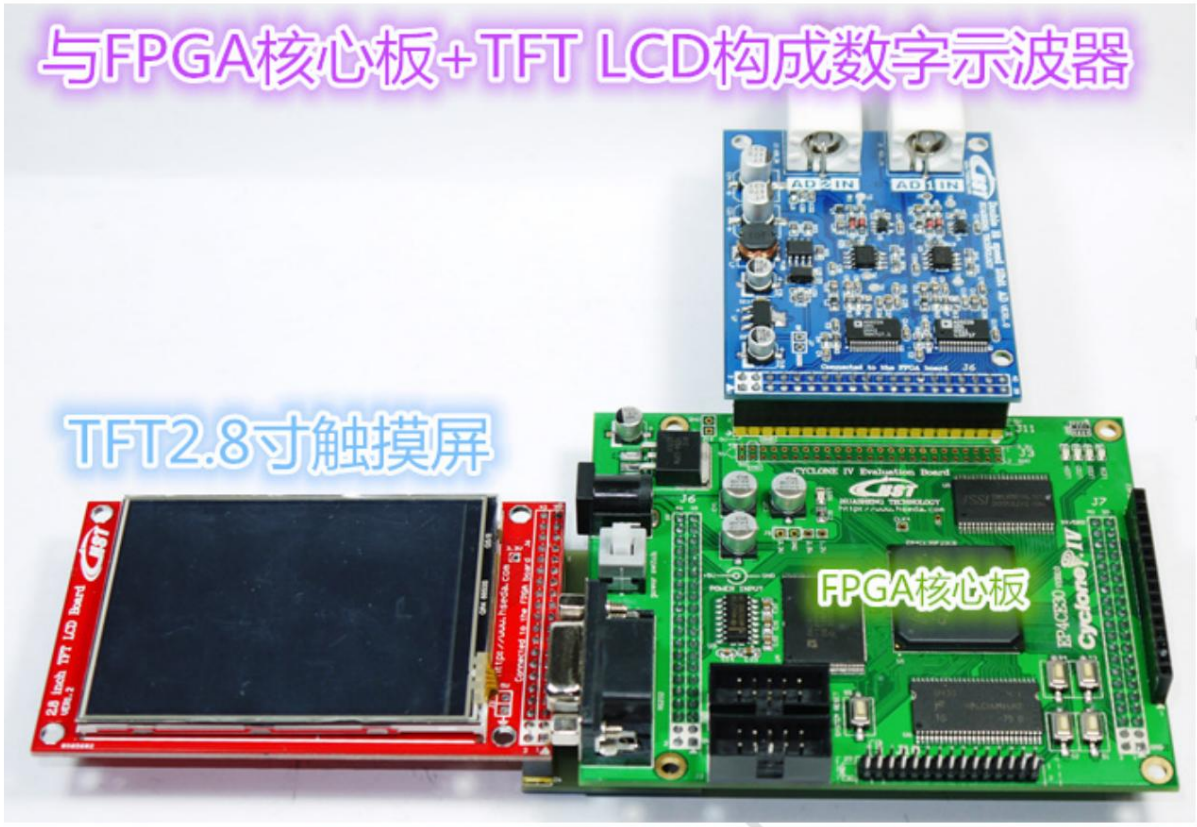
4. Data was acquired in real time using SignalTap II.

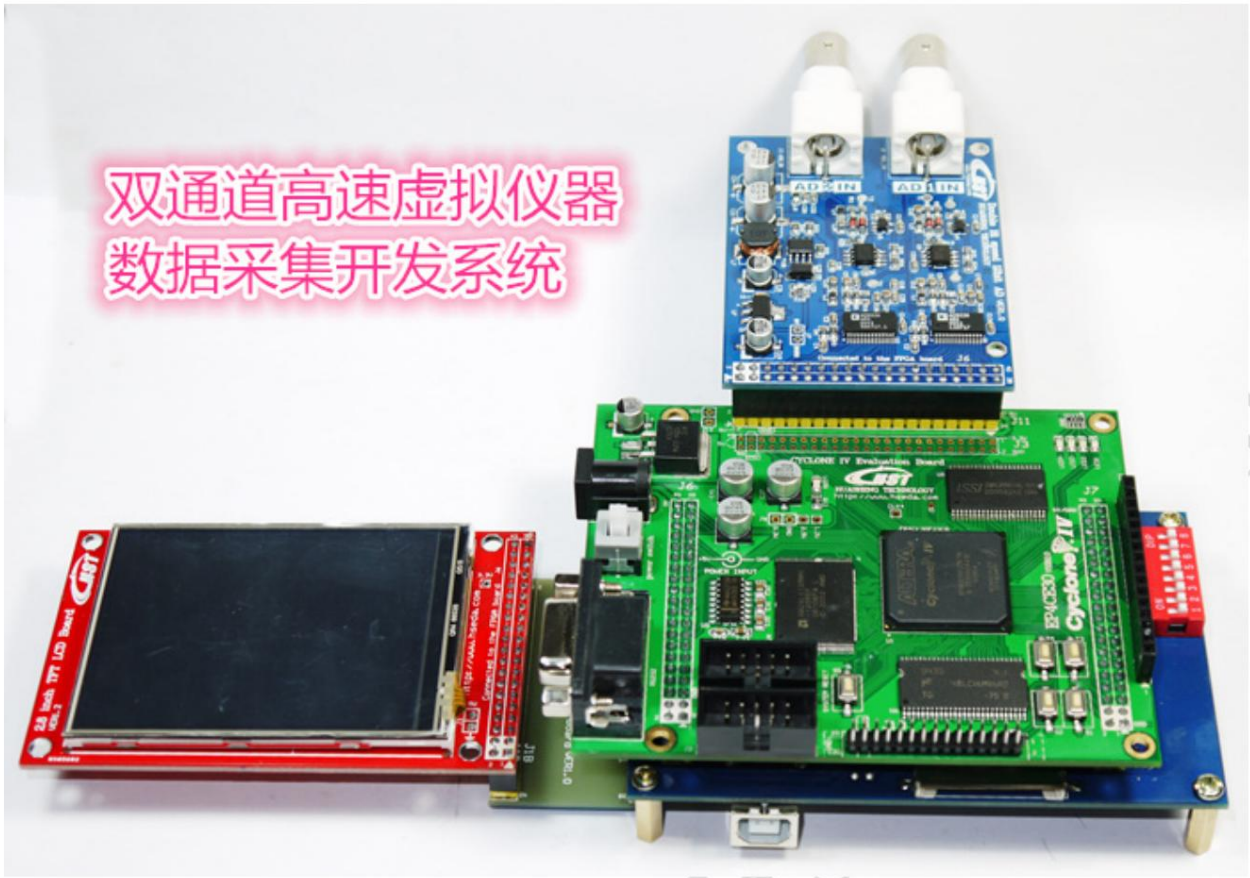
11. **SignalTap II** waveform

The waveform below is the data waveform collected by the tool SignalTap II in Quartus II

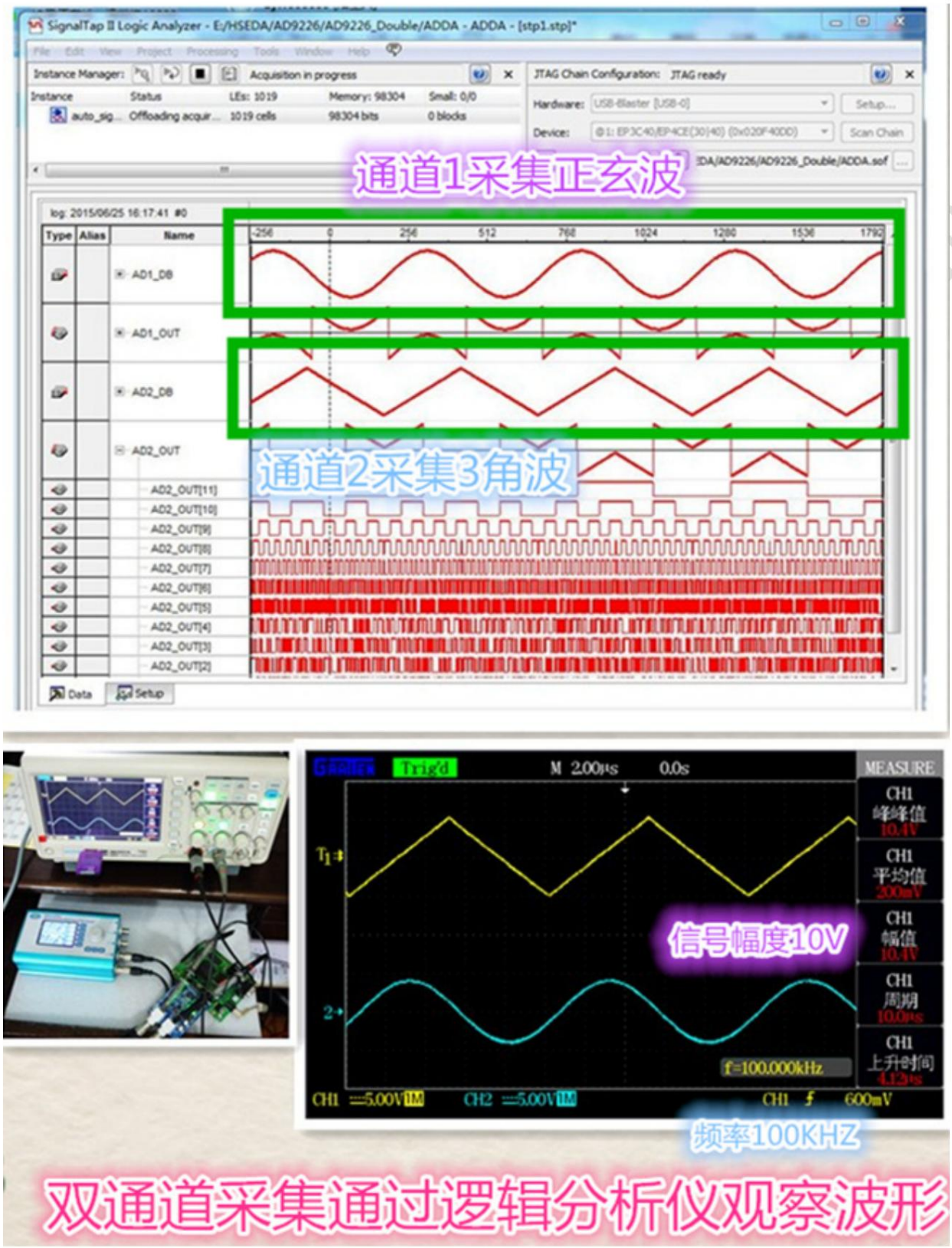


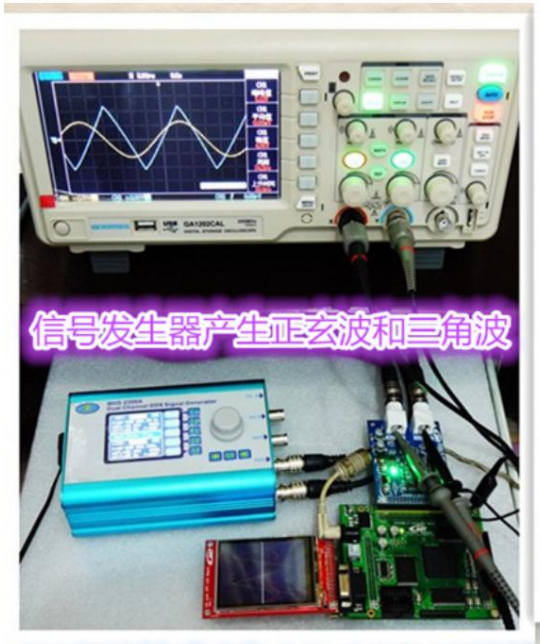
12. System combination photos

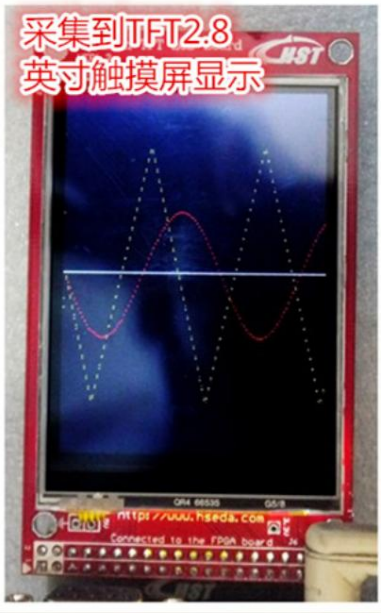




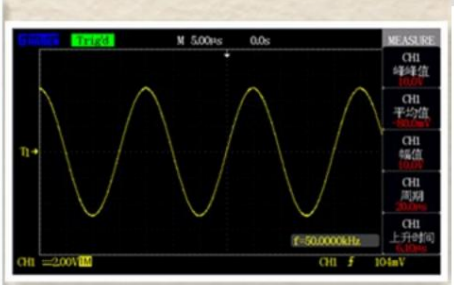
13. Experimental display

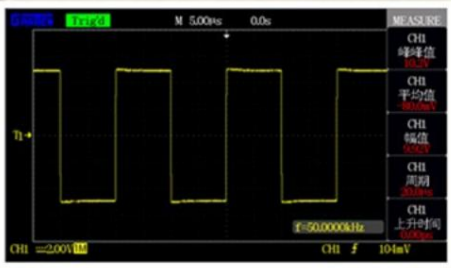


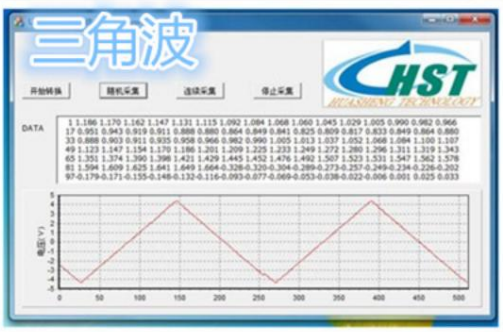


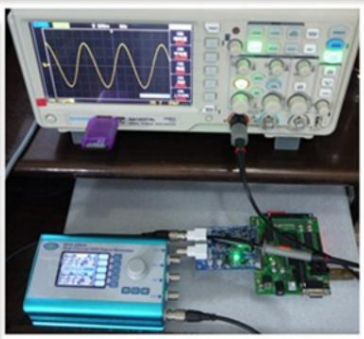


双通道高速AD9226采集信号到TFT屏显示









虚拟仪器AD采集数据通过USB
传输到PC端显示和保存数据

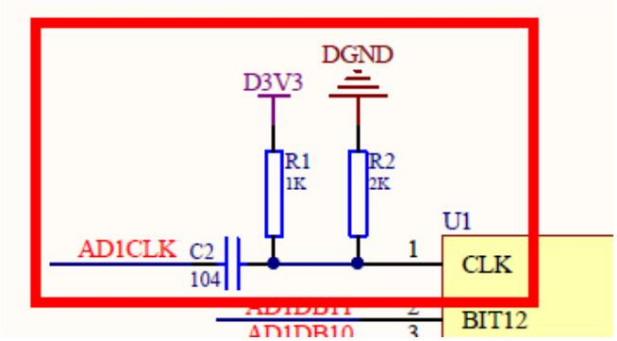
14. Experiment FAQ

1. Why can't the AD module run at low frequency? Answer: Because our

AD chip is a high-speed chip, we have performed RC shaping processing on the clock to the AD chip. If you want the AD chip to run at a lower frequency, you can remove

the isolation capacitor C2, that is, short-circuit C2. Our best acquisition is preferably a clock frequency above 1Mhz. The running clock frequency of our supporting routine is 50MHZ. The actual measurement can reach

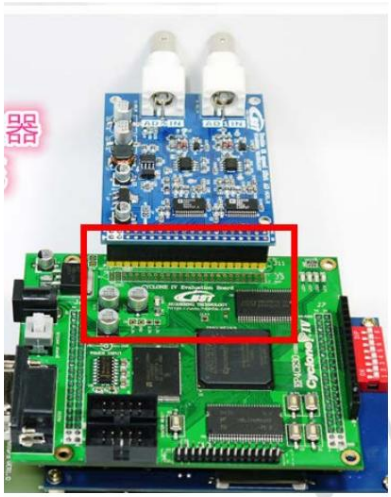
up to 100MHZ. If the wiring distance between the FPGA core board and the AD module is very short.



2. Why is there noise or voltage instability when the AD module is connected to the FPGA target board with a DuPont cable? Answer: Because our AD chip

runs in high-speed parallel mode, our recommended connection method is board-to-board connection, and the FPGA is connected to the IO port The distance should not be too long, otherwise it will affect the speed and

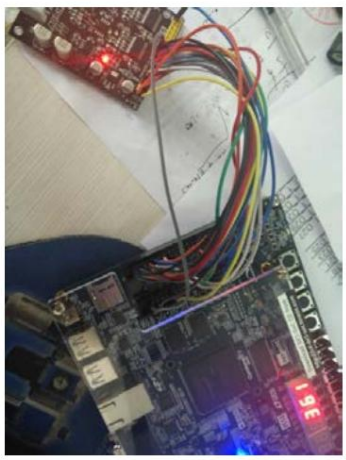
frequency of acquisition.

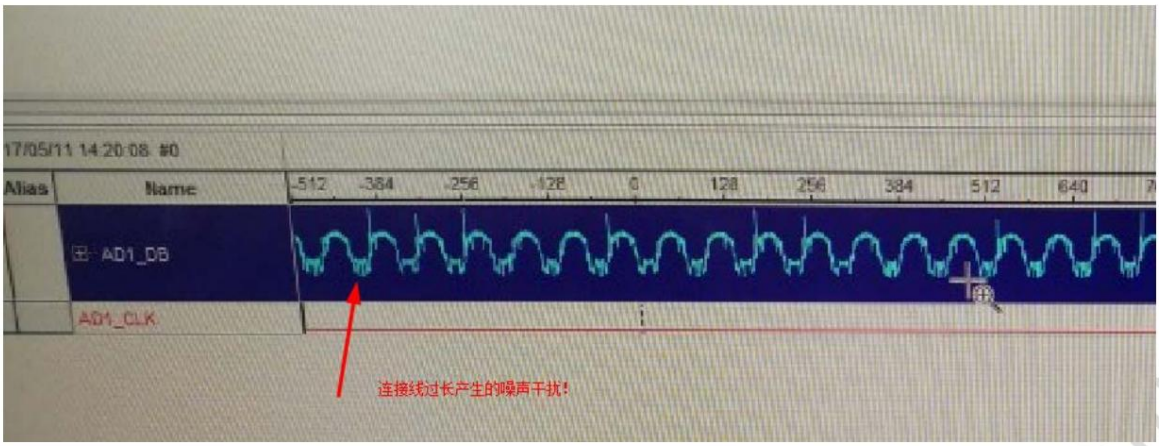


If the user uses a DuPont cable to connect, the connection should not exceed 5CM, otherwise noise interference will occur, because the AD module has a large working current, and

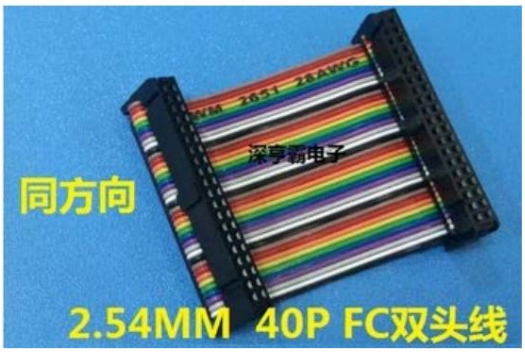
And pay attention to the good connection with the target board GND. The AD module is best powered separately, 5V power supply, pay attention to the stability of the power supply.

The following connection methods may cause noise interference.





It is recommended to use this type of cable connection, and the length should not exceed 5CM, otherwise it will cause noise interference or reduce the sampling frequency.



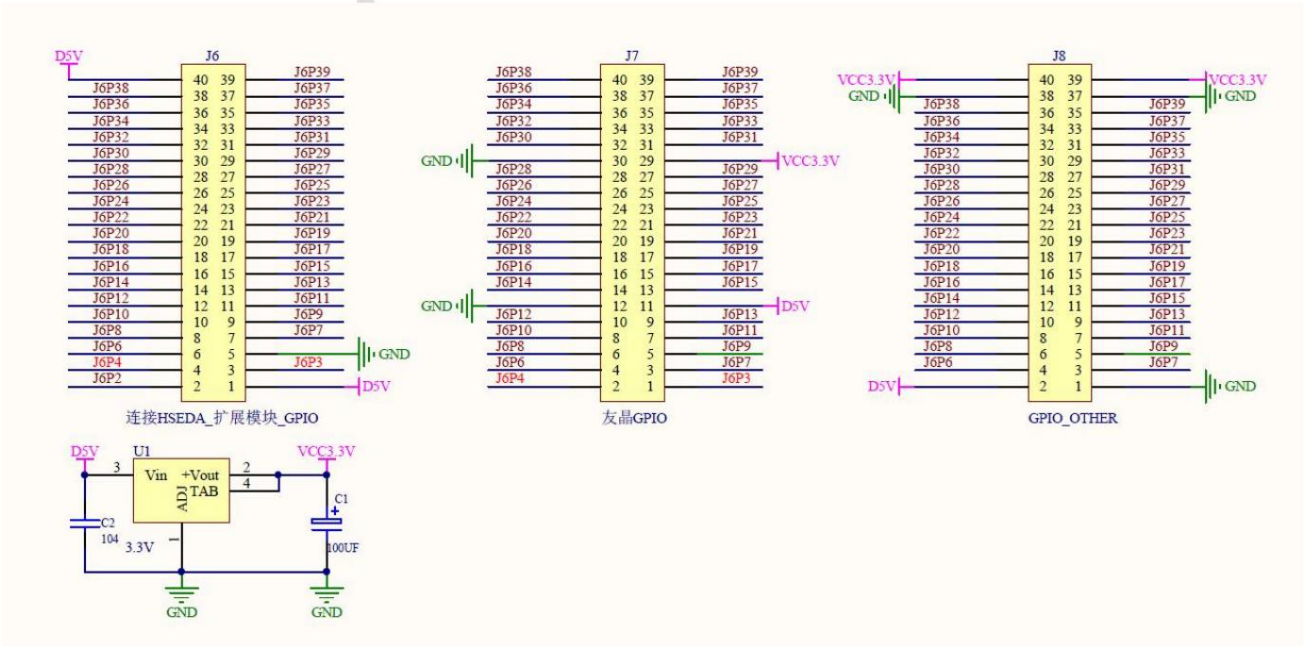
3 Why is the temperature high when the AD chip is working? Answer:

Because AD9226 is a high-speed digital-analog hybrid chip, the operating temperature will be very high, which is normal. Don't worry about damage.

4 How does the AD module of Huasheng EDA connect to the development boards of other

companies? A: For the convenience of users, we have specially designed the corresponding interface adapter board for users. The development board interface commonly used in the market can be connected through the adapter board. For example, Taiwan Youjing, or Shanghai Black Gold Development Board. Adapter board purchase link: https://item.taobao.com/item.htm?spm=a1z10.5-c.w4002-17218964840.81.fc5735fbLmOzLZ&id=562759035971

Schematic diagram of the adapter board



AD9226引出IO信号定义(HSEDA接口J6)

引脚定义	信号名称	引脚定义	信号名称
1	5V	2	GND
3		4	
5	GND	6	
7		8	
9	AD2CLK	10	AD2DB11
11	AD2DB10	12	AD2DB9
13	AD2DB8	14	AD2DB7
15	AD2DB6	16	AD2DB5
17	AD2DB4	18	AD2DB3
19		20	
21	AD2DB2	22	AD2DB1
23	AD2DB0	24	AD2_OTR
25		26	AD1CLK
27	AD1DB11	28	AD1DB10
29	AD1DB9	30	AD1DB8
31	AD1DB7	32	AD1DB6
33	AD1DB5	34	AD1DB4
35	AD1DB3	36	AD1DB2
37	AD1DB1	38	AD1DB0
39	GND	40	5V

AD9226引出IO信号定义通过转接板V2.0转换(友晶接口J7)

引脚定义	信号名称	引脚定义	信号名称
1		2	
3		4	
5	AD2CLK	6	
7	AD2DB10	8	AD2DB11
9	AD2DB8	10	AD2DB9
11	5V	12	GND
13	AD2DB6	14	AD2DB7
15	AD2DB4	16	AD2DB5
17		18	AD2DB3
19	AD2DB2	20	
21	AD2DB0	22	AD2DB1
23		24	AD2_OTR
25	AD1DB11	26	AD1CLK
27	AD1DB9	28	AD1DB10
29		30	GND
31	AD1DB7	32	AD1DB8
33	AD1DB5	34	AD1DB6
35	AD1DB3	36	AD1DB4
37	AD1DB1	38	AD1DB2
39		40	AD1DB0

AD9226引出IO信号定义过转接板V2.0转换(黑金接口J8)

引脚定义	信号名称	引脚定义	信号名称
1	GND	2	5V
3		4	
5	AD2CLK	6	
7	AD2DB10	8	AD2DB11
9	AD2DB8	10	AD2DB9
11	AD2DB6	12	AD2DB7
13	AD2DB4	14	AD2DB5
15		16	AD2DB3
17	AD2DB2	18	
19	AD2DB0	20	AD2DB1
21		22	AD2_OTR
23	AD1DB11	24	AD1CLK
25	AD1DB9	26	AD1DB10
27	AD1DB7	28	AD1DB8
29	AD1DB5	30	AD1DB6
31	AD1DB3	32	AD1DB4
33	AD1DB1	34	AD1DB2
35		36	AD1DB0
37	GND	38	GND
39	3.3V	40	3.3V