VHDL Lab2 Report

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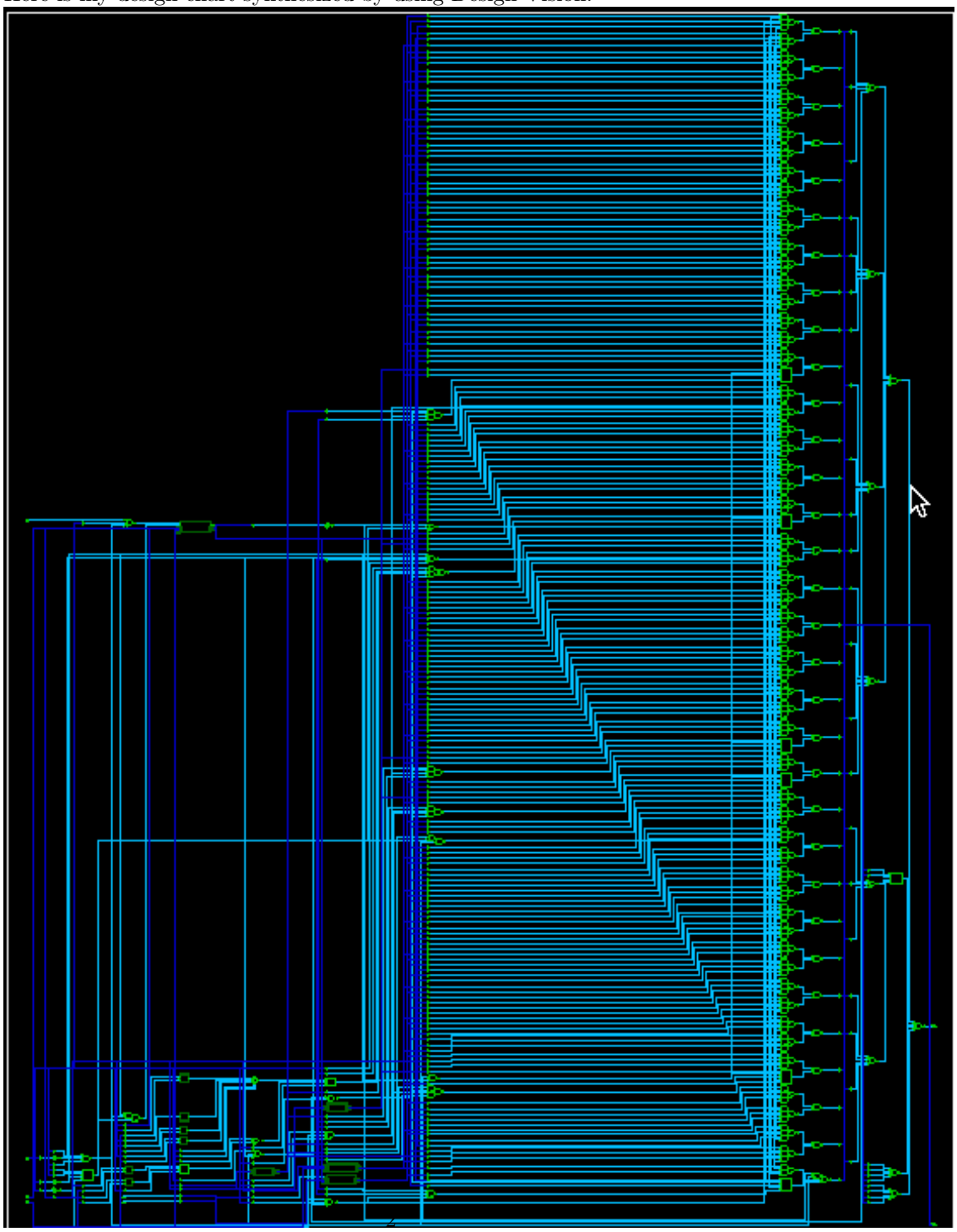
1 Design Chart

Here is my design chart synthesized by using Design Vision.



2 Some other charts and descriptions

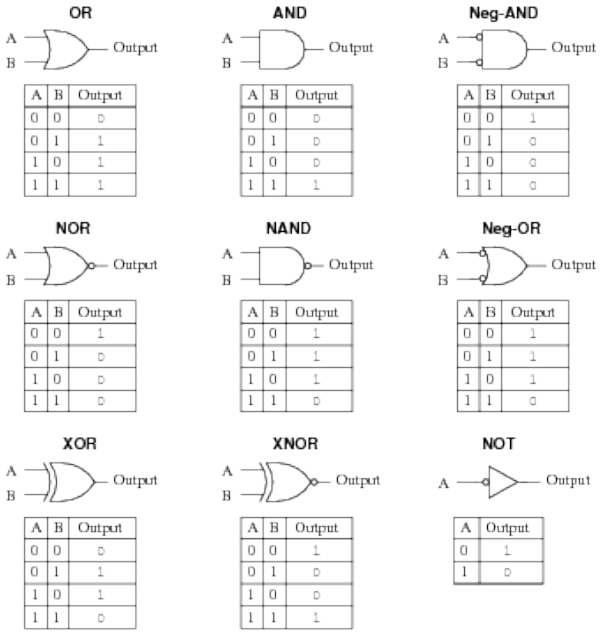
Since this time we don't need to build the circuit from drawing a K-Map, it is far more easier to build a ALU.
For the logic gate part, I just need to write down the sum of products and make it by stacking up the NAND gate (like this):

```
module AND (a, b, c);
        input  a, b;
        output c;
        wire nand_0;
        // IMPLEMENTATION
        nand nand1(nand_0, a, b);
        NOT N1(nand_0, c);
endmodule

module OR (a, b, c);
        input  a, b;
        output c;
        wire not_0, not_1;
        // IMPLEMENTATION
        NOT N1(a, not_0);
        NOT N2(b, not_1);
        nand(c, not_0, not_1);
endmodule

module NOT (a, b);
        input  a;
        output b;
        // IMPLEMENTATION
        nand(b, a, a);
endmodule
```

Once we got these basic logic gates done by using NAND gate, we can then use them to build up more complex gates such as NOR, XOR, XNOR gates.
Here are the truth tables:



Since the Lab2 didn't require us to draw the K-Maps, I'm going to ommit them here.

3 Problems

The main problem in my Verilog design were 2 important errors:

1. Putting another always block inside a always block.
   This caused me to seriously delayed the progress of this assignment for few days and I had no clue about what is going wrong.

2. Wrong array size in my wire variables.
   With this typo, I spent about 3 hrs to find the error in my Decoder and Arbiter and found nothing.(here)

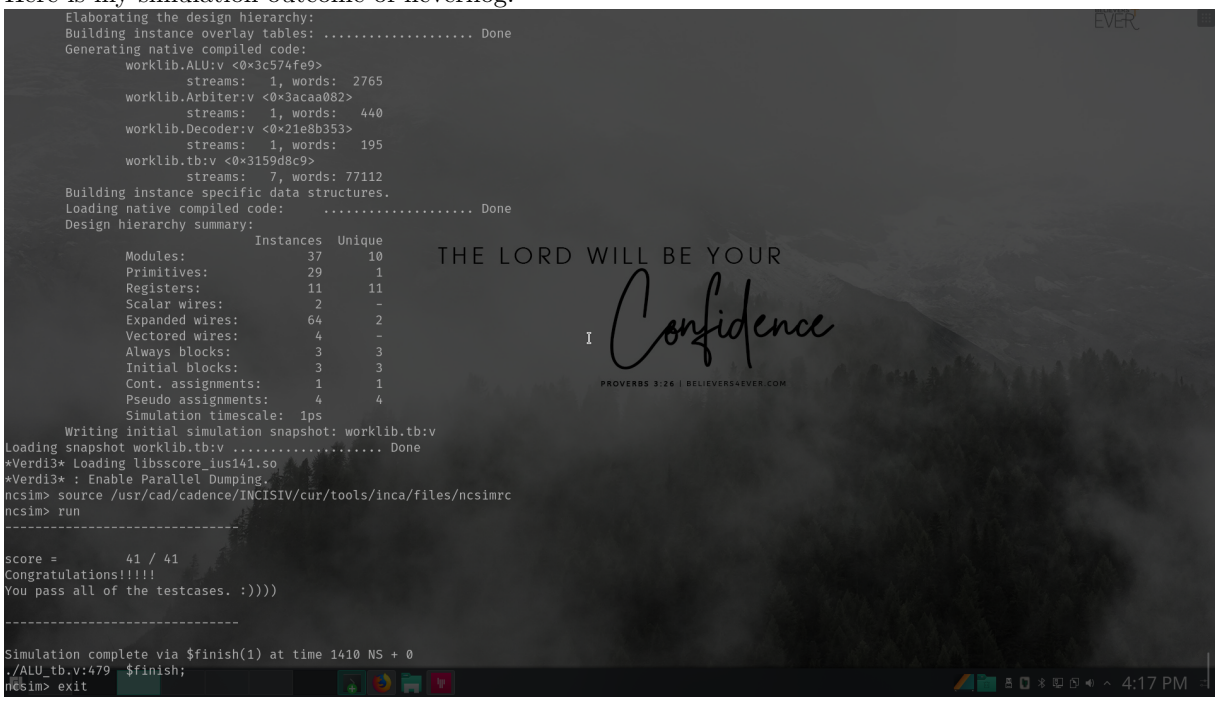
   ```
   wire [32-1:0]  dec_1;
   wire [5-1:0] arb_1;
   ...
   4'b1110: Y = dec_1;
   4'b1111: Y = arb_1;
   ```

   If we assign the input with the size that is too small, then it will fill up Y's remaining blanks with 'z's, which is not our desired '0's.

To sum it up, it was nothing but careless typos and conceptual inaccurarcy.

4 Simulation Outcome

Here is my simulation outcome of ncverilog:



5 Report Area

The content inside my report area txt file.