Arquitectura de Computadores Avançada

General Description

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Bolonha Model

- It promotes a student-centred teaching by
  - stimulating an autonomous learning
  - proposing the *problem solving* paradigm as the main methodological strategy for teaching
  - stressing the development of specific skills vs. a more or less automatic building up of general knowledge.
- It establishes very precise metrics on the work being carried out
  - the academic week is defined to be 40 hours of effective work, meaning a total of 30 ECTS credits
    - 1 ECTS = 4/3 h of weekly study
  - each course of the curriculum is assigned a very definite work load
    - ACA: 6 ECTS $\Rightarrow$ 8 h of weekly study (attending classes + home work).

Main Objectives

- to introduce the most relevant design concepts present in recent generations of processors and how they affect the performance of a computer system
- to describe the organization of the memory hierarchy, in particular cache and virtual memory
- to get acquainted with computer architecture simulation tools and how they can be used to assess performance.

Learning Outcomes

- to understand the architecture and the most important decisions taken on the design of modern processors and how they affect program execution
- to be able to plan and carry out a set of simulations for testing different processor configurations.

Prerequisites

- good operating knowledge on digital circuit design
- basic notions on computer architecture and on communication protocols with input-output devices (pooled I/O, interrupt driven I/O and DMA based I/O)
- programming skills in C Language and VHDL at a fair to good level.

Syllabus

- Fundamentals of quantitative design and analysis
- Pipelined processors organization and limitations to their operation
- Memory hierarchy: cache memory and virtual memory
- Exploitation of parallelism at the instruction level: dynamic scheduling, hardware-based speculation and multiple instruction issue
- Exploitation of parallelism at data level: vector processors and instruction set extensions for multimedia
- Exploitation of parallelism at the data/task level (GPUs): multithreading and multiprocessors

Main bibliography

- *Computer Architecture - a Quantitative Approach*, J.Hennessy, D.A.Patterson, 5th Edition, Morgan Kaufmann, 2012
- *Computer Organization and Architecture – Designing for Performance*, W. Stallings, 9th Edition, Prentice Hall, 2013

Important note – One of these books should be really read!

Lectures

Lectures present specific topics of the syllabus. The adopted approach tries to entice the students to participate actively in the discussion and to help them to develop skills of critical reasoning and to learn general techniques of problem solving.

A recording of the each lecture will be made available.

During the allotted period of time, the students are invited to present their doubts by e-mail. A detailed answer will be given as soon as possible and both the questions (in an anonymous way) and the answers will be posted in the elearning site for general consultation.

Lab classes - 1

Labs follow the motto "*you learn by doing*" and aim the completion of small tasks to prepare the students for the work assignments.

***Work assignment* 1 – Digital circuitry simulation**

Implementing and evaluating specific features in a pipelined architecture.

***Work assignment* 2 – CUDA / OpenCl programming**

Solving a computer intensive task in a GPU architecture.

Students are organized in working groups composed of two elements. Each group must present and defend their own solution to the proposed problems.

Lab classes - 2

Labs take place in site at department rooms 101 and 102.

For safety reasons due to the COVID 19 pandemic, each lab class is split in two halves and the students are assigned for the duration of the semester to one of the rooms. After the assignment is made, no changes will be allowed.

A record of the students present at each room for each class will always be made and will be reported to the health authorities if requested.

An effort will be made to ensure the proper operating conditions as prescribed by the health authorities.

In the week of December 6 to 12, labs classes P3 and P4 will be moved to the afternoon of December 9 (15h – 17h and 17h – 19h, respectively) due to the holiday of December 8.

Tutorials

Tutorials take place every week on Thursdays, at 18h.

For some of them, a recording of the solution of the small task, assigned to the lab classes of the week before, will be made available. For all of them, the students are invited to present their doubts by e-mail. An detailed answer will be given as soon as possible and both the questions (in an anonymous way) and the answers will be posted in the elearning site for general consultation.

They will have, when a recording is made available, an expositive character and aim to help the students to overcome deficiencies in background knowledge as well as to provide a space for the discussion of specific aspects of the course.

Themes to be treated include

- Digital circuitry modeling
- CUDA / Open Cl programming.

Grading - 1

$$course\ grade = \frac{5 \times theoretical\ mark + 5 \times lab\ mark}{10}$$

- rounding is always carried out *half up* to unities, except when the lab mark is higher than the theoretical mark by more than three units; in this case, rounding is carried out *half down*
- *theoretical grading*
  - written examination (época normal ou época de recurso)
  - challenge placed during lectures (optional)
  - *minimum mark* equal to 8,5 units (always rounded to unities)
- *lab grading*
  - composed of *work assignment* 1 and *work assignment* 2, each having equal weight
  - *minimum mark* equal to 8,5 units (always rounded to unities)

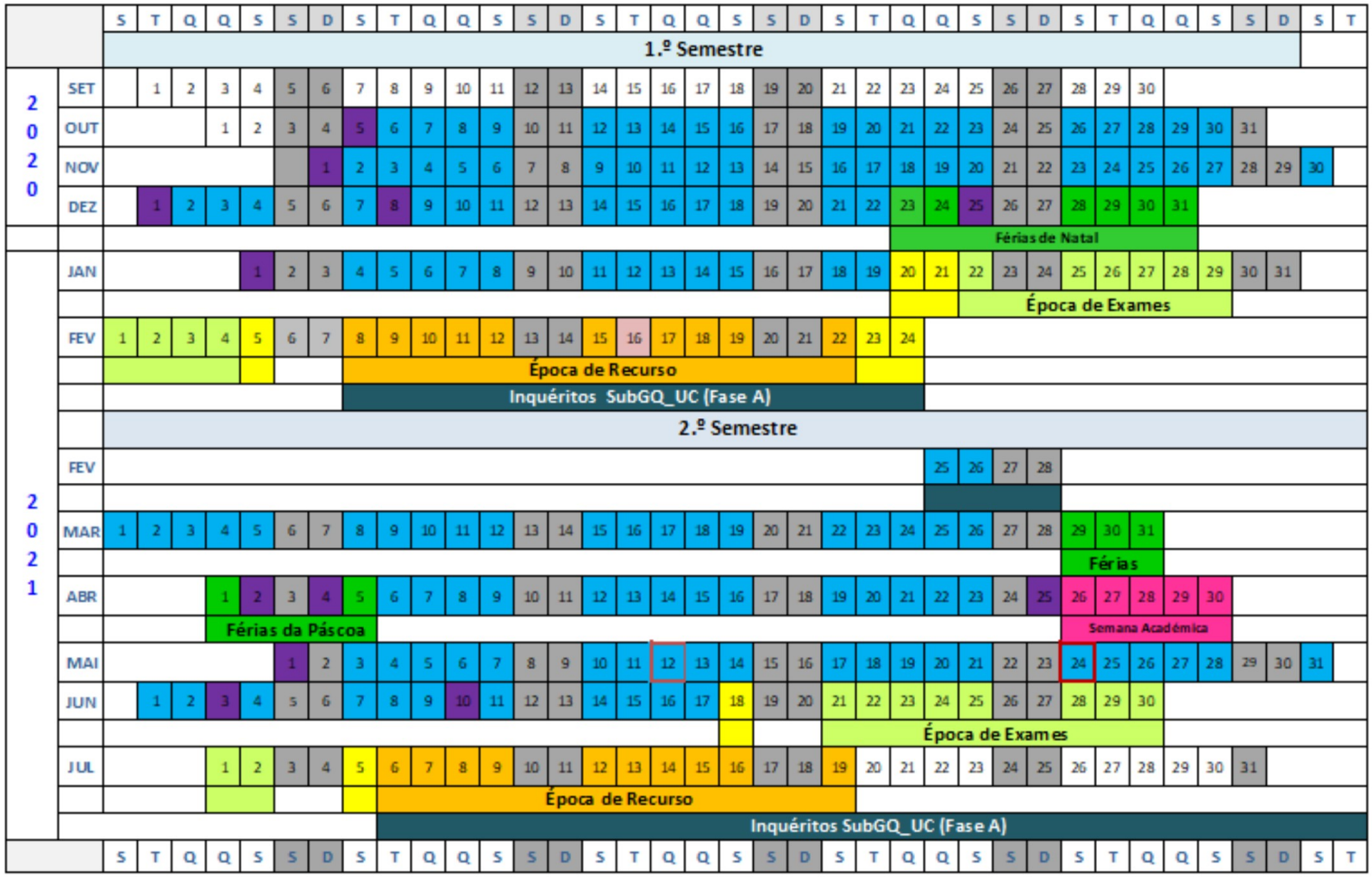
Grading - 2

- *Pass*
  - both theoretical and lab marks higher or equal to 8,5 units ***and*** course grade higher or equal to 10 units
- *Fail*
  - theoretical mark lower than minimum mark ***or*** lab mark lower than minimum mark ***or*** final grade lower than 10 units
- *Fail by minimum mark*
  - lab mark lower than minimum mark
- *Fail by absence (regular student)*
  - missing more than seven lab classes

Final remarks

- the lab mark is limited to 17 units
  - a higher grade requires an additional assignment
- special dates
  - deadline for delivering work assignment 1: 9 de Dezembro de 2020
  - deadline for delivering work assignment 2: 19 de Janeiro de 2021
- all documentation about the course can be found in the *e-learning* site (moodle)
- any further questions may be answered by the course operational document or by myself.

Calendar


1.º Semestre
2020
SET
OUT
NOV
DEZ
Férias de Natal
2021
JAN
Época de Exames
FEV
Época de Recurso
Inquéritos SubGQ_UC (Fase A)
2.º Semestre
FEV
MAR
Férias
ABR
Férias da Páscoa
Semana Académica
MAI
JUN
Época de Exames
JUL
Época de Recurso
Inquéritos SubGQ_UC (Fase A)