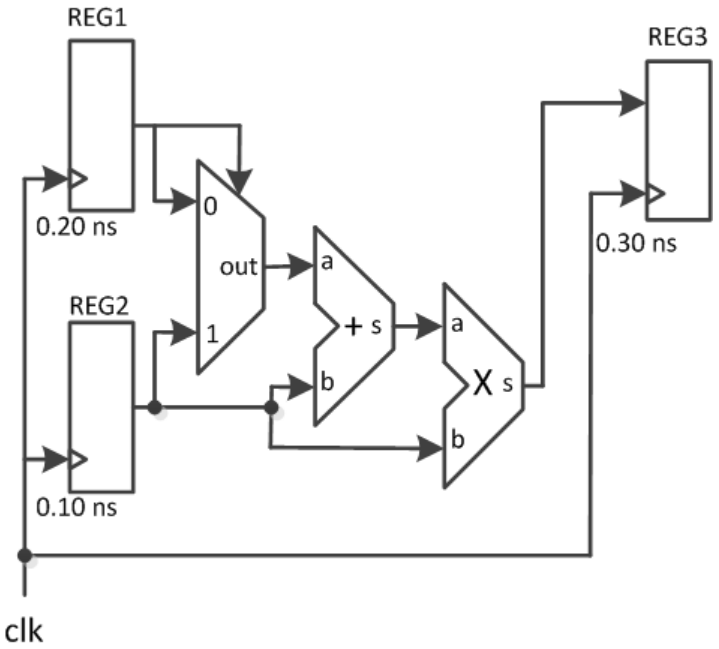
Exercises - TOC

Lesson 2 – Physical Analysis

1.- In the following circuit, the propagation values of its combinational and sequential components are:

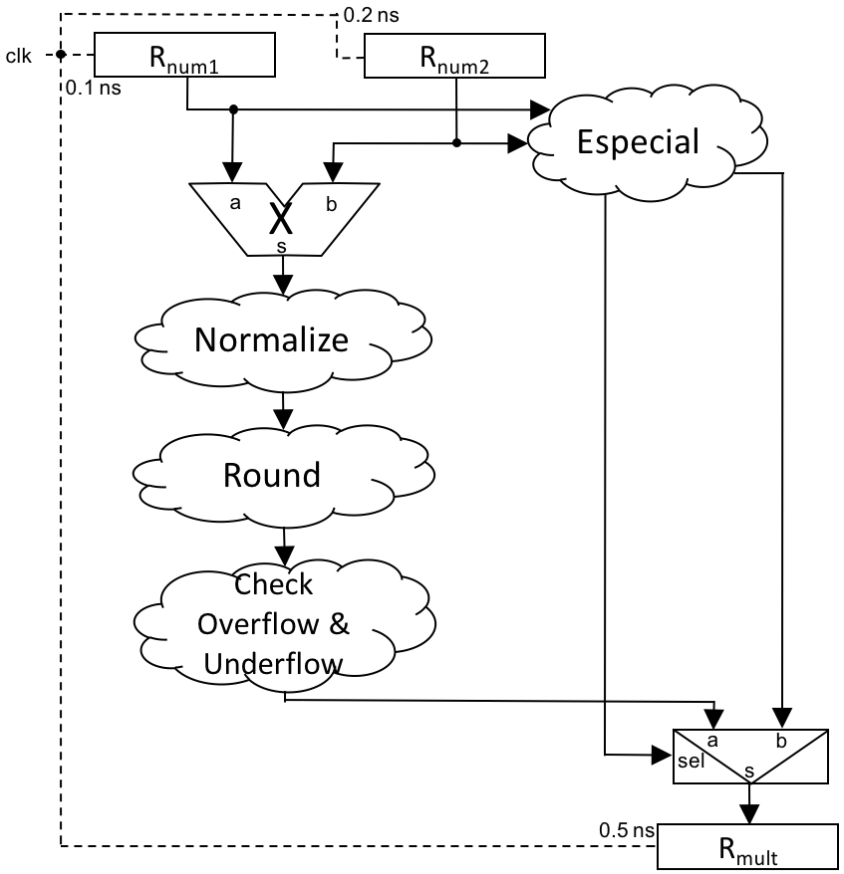
- ADD(a→s) = 2.75 ns
- ADD(b→s) = 2.60 ns
- MUL(a→s) = 2.75 ns
- MUL(b→s) = 2.60 ns
- MUX(sel→out) = 0.50 ns
- MUX(0→out) = 0.50 ns
- MUX(1→out) = 0.40 ns.
- $t_{clk-2-q}$ = 0.10 ns
- t_{setup} = 0.15 ns
- t_{hold} = 0.20 ns.



Provided that the values in the `clock` lines correspond to the propagation delay from the clock source to the register:

a. Could this circuit work properly at 250 MHz? Justify the answer.
b. Indicate the range of delays of MUL(a→s) for which the circuit can work correctly at 250 MHz.
c. Assuming that the delay of MUL(a→s) is 2.60 ns, would it be possible, through segmentation, to make this circuit work at 250 MHz? In that case, indicate where the segmentation registers(s) should be placed to make it possible; and prove if, indeed, it is possible for the segmented circuit to operate at 250 MHz. Are there new hold violations with this modification? If so, how could they be solved? Assume that the clock delay of the new register(s) is 0.3 ns.

2.- The circuit of the figure is an implementation (not too optimized) of the Data Path that a certain TOC teacher has proposed to his estimated students for the calculation of the multiplication of two numbers following the IEEE754 standard.



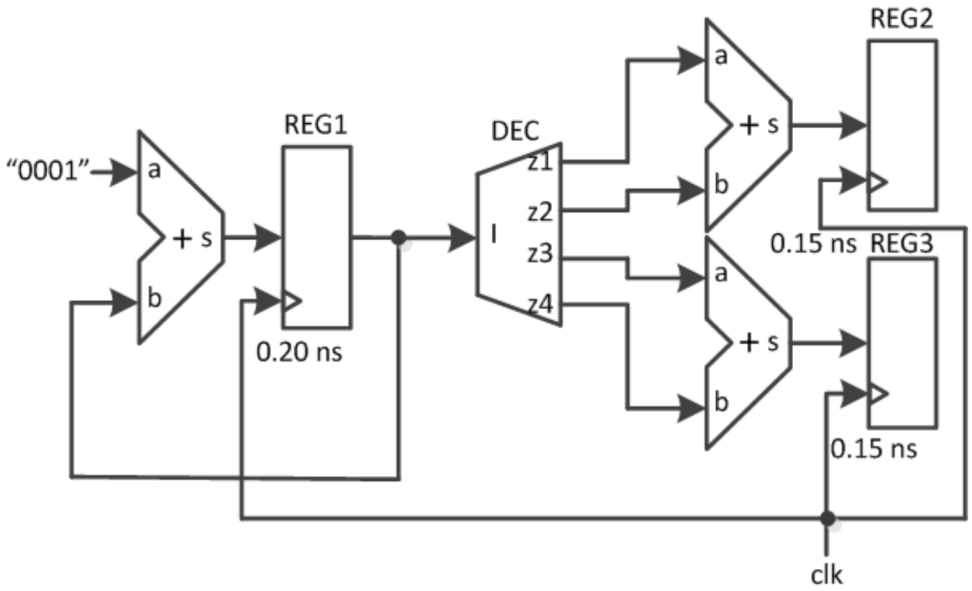
The propagation values of its combinational and sequential components are the following:

- MUL(a → s) = MUL(b → s) = 5.75 ns
- MUX(a → s) = MUX(b → s) = MUX(sel → s) = 0.25 ns
- Special = 3.75 ns
- Normalize = 2.5 ns
- Round = 1.25 ns
- Check Overflow & Underflow = 0.5 ns
- $t_{clk\text{-}2\text{-}q}$ = 0.15 ns
- t_{setup} = 0.20 ns
- t_{hold} = 0.10 ns.

Provided that the values in the `clock` lines correspond to the propagation delay from the clock source to the register:

a. We want this circuit to work in one of the laboratory FPGAs, which have a 100MHz oscillator. Would it be possible? Justify the answer and identify the critical path.
b. Indicate the range of frequencies in which this Data Path can work correctly.
c. Indicate what architectural improvement could be introduced so that this data route could work correctly at the desired frequency, and demonstrate that said objective is met. As a consequence of the modification introduced, do other unwanted side effects occur? Justify the answer. (Assume that the clock delay of any added register in the design is 0.2ns). NOTE: Ignore the changes that should be introduced in the Control Unit associated with this Data Path.

3.- In the following circuit:



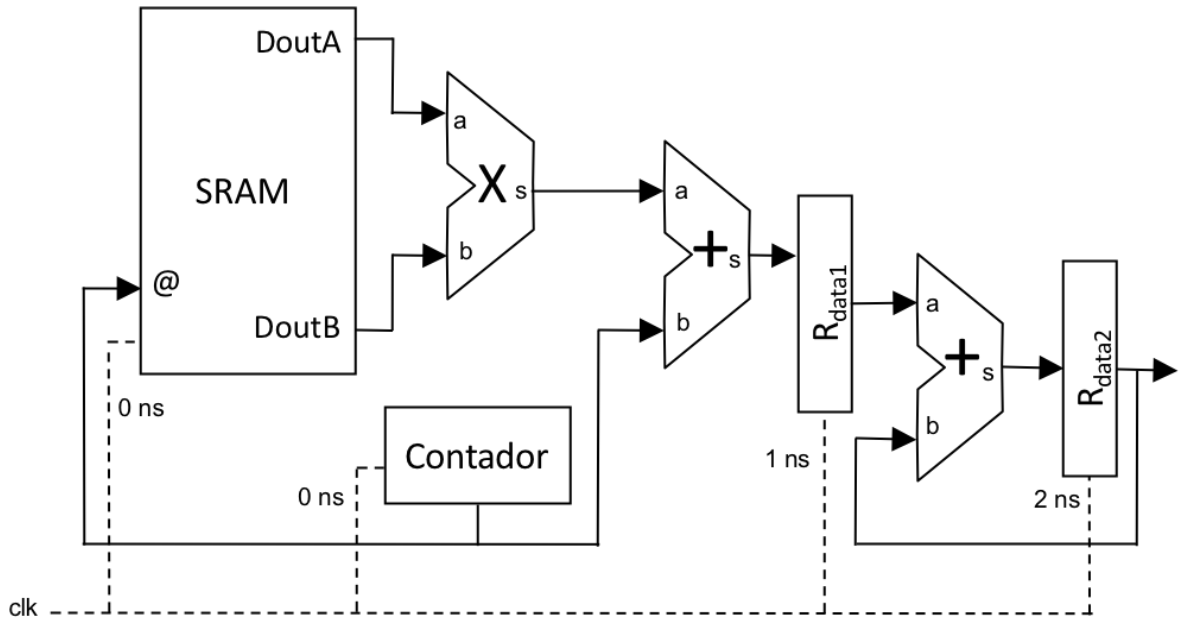
the propagation values of its combinational and sequential components are:

- ADD(a→s)= 1.40 ns
- ADD(b→s) = 1.10 ns
- DEC(I→z1) = DEC(I→z2) = DEC(I→z3) = DEC(I→z4) = 0.60 ns.
- $t_{clk\text{-}2\text{-}q}$ = 0.15 ns
- t_{setup} = 0.20 ns
- t_{hold} = 0.10 ns.

Provided that the values in the `clock` lines correspond to the propagation delay from the clock source to the register:

a. Justify if this circuit can work properly at 500 MHz. Calculate the range of frequencies for which this circuit can work properly. Justify the answer.
b. Indicate the delay range of the decoder for which the circuit would work correctly at 500 MHz. Assume that DEC(I→z1) = DEC(I→z2) = DEC(I→z3) = DEC(I→z4).
c. Would it be possible, through segmentation, to make this circuit work at 500 MHz? In that case, indicate where the segmentation registers(s) should be placed to make it possible; and prove if, indeed, it is possible for the segmented circuit to operate at 500 MHz. Assume that the clock delay of the new register(s) is 0.3 ns.

4.- In the following circuit:



the propagation values of its combinational and sequential components are:

- ADD(a → s) = ADD(b → s) = 1 ns
- MUL(a → s) = MUX(b → s) = 2.50 ns
- $t_{clk\text{-}2\text{-}q}$ = 0.15 ns
- t_{setup} = 0.20 ns
- t_{hold} = 0.10 ns.

Provided that the values in the `clock` lines correspond to the propagation delay from the clock source to the register:

a. Find the critical path and justify if the circuit can operate correctly at 500 MHz
b. Indicate the delay range of the multiplier for which the circuit can operate correctly at 500 MHz. Assume that MUL(a→s) = MUL(b→s).
c. Would it be possible, through segmentation, to make this circuit work at 500 MHz? In that case, indicate where the segmentation registers(s) should be placed to make it possible; and prove if, indeed, it is possible for the segmented circuit to operate at 500 MHz. Assume that the clock delay of the new register(s) is 1 ns.