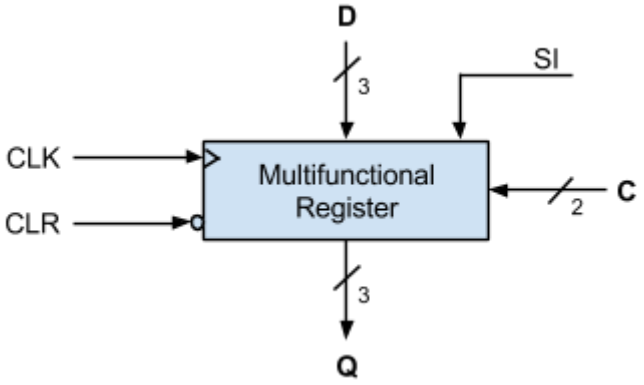
Lab 4: Design and Implementation of a Multifunctional Register

1 Overview

The goal of this lab is to design and build a multifunctional register like the one depicted in the following Figure:



C_1	C_0	**Q**(k+1)	Function
0	0	**D**(k)	Parallel load
0	1	$Q_0(k),Q_2(k),Q_1(k)$	Rotation to right
1	0	$Q_1(k),Q_0(k)$,SI(k)	Shift left
1	1	**Q**(k)	Same value

The circuit will have the following set of ports:

- A 3-bit parallel output ***Q***, which show the data stored in the register
- A 3-bit parallel input ***D***, where we must place the input data (for parallel load)
- A serial input *SI*, 1-bit input to shift data to the left
- A 2-bit control input ***C***, to select the function to perform
- A clock input *CLK*
- An asynchronous input *CLR*, to clean the register (***Q***=000), active Low.

2 Development

2.1 Design phase

- The circuit design must be completed at home. It must be summarized in the corresponding lab notebook.
- The behavior of the circuit must be designed using D flip-flops and 4-to-1 multiplexers.

2.2 Building and debugging phase

- Use the following ICs to mount the circuit: **7474** (2 D flip-flops, triggered by rising edge and asynchronous initialization signals - to 0 and 1 - active Low), **74153** (2 4-to-1 multiplexers, with common control signals and separate enable signals, active low).
- Connect ***D***, ***C***, *SI*, and *CLR* inputs to switches.
- Connect *CLK* to a pulse switch
- Connect ***Q*** to three leds
- **Check all the working modes and validate the final design**. It the circuit does not perfectly work, it must be debugged to find the errors and repair them.

2.3 Using the function generator

- Configure the function generator in order to produce a square wave of 1 Hz
- Connect the TTL output of the function generator to the *CLK* input of your circuit
- Connect the pulse switch output to the CLR input
- When the circuit is correctly working, show your implementation to your lab professor