4bit full adder/subtractor

Projetos de Hardware e Interfaciamento

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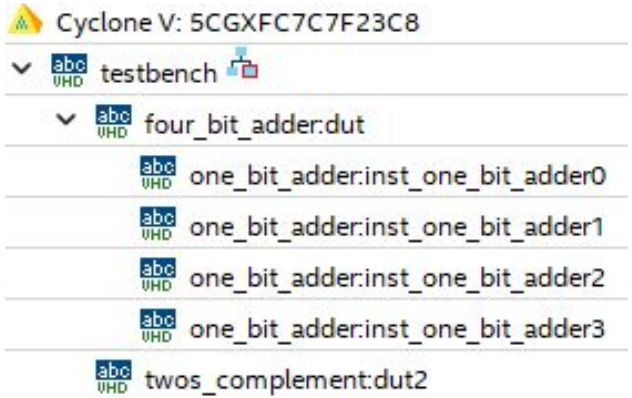
Project

Requirements

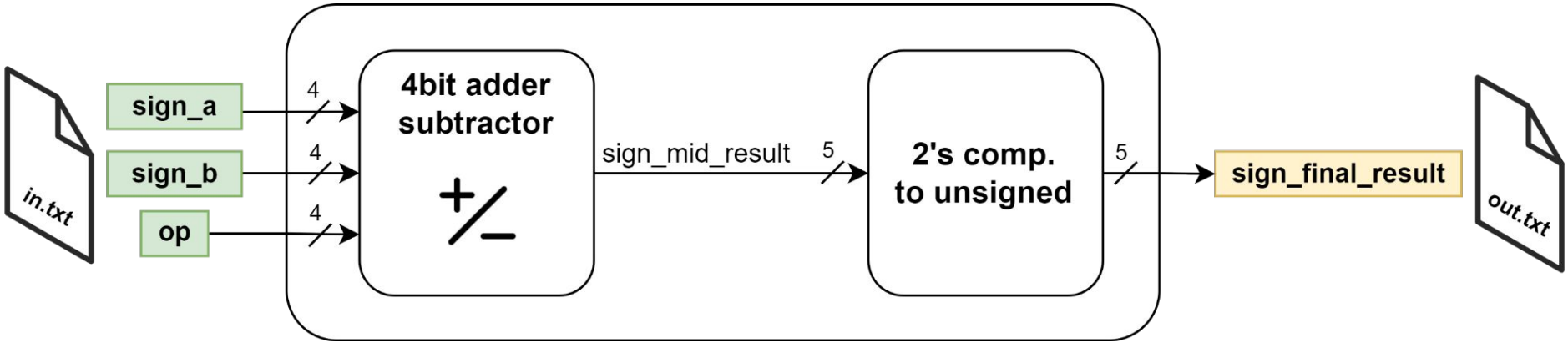
- **1bit full adder** from logic gates using std_logic_1164;
- From the 1bit adder, build a top-level file that implements a **4bit adder**;
- The 4bit adder must be configured to allow **sum or subtraction** operations;

Hierarchy



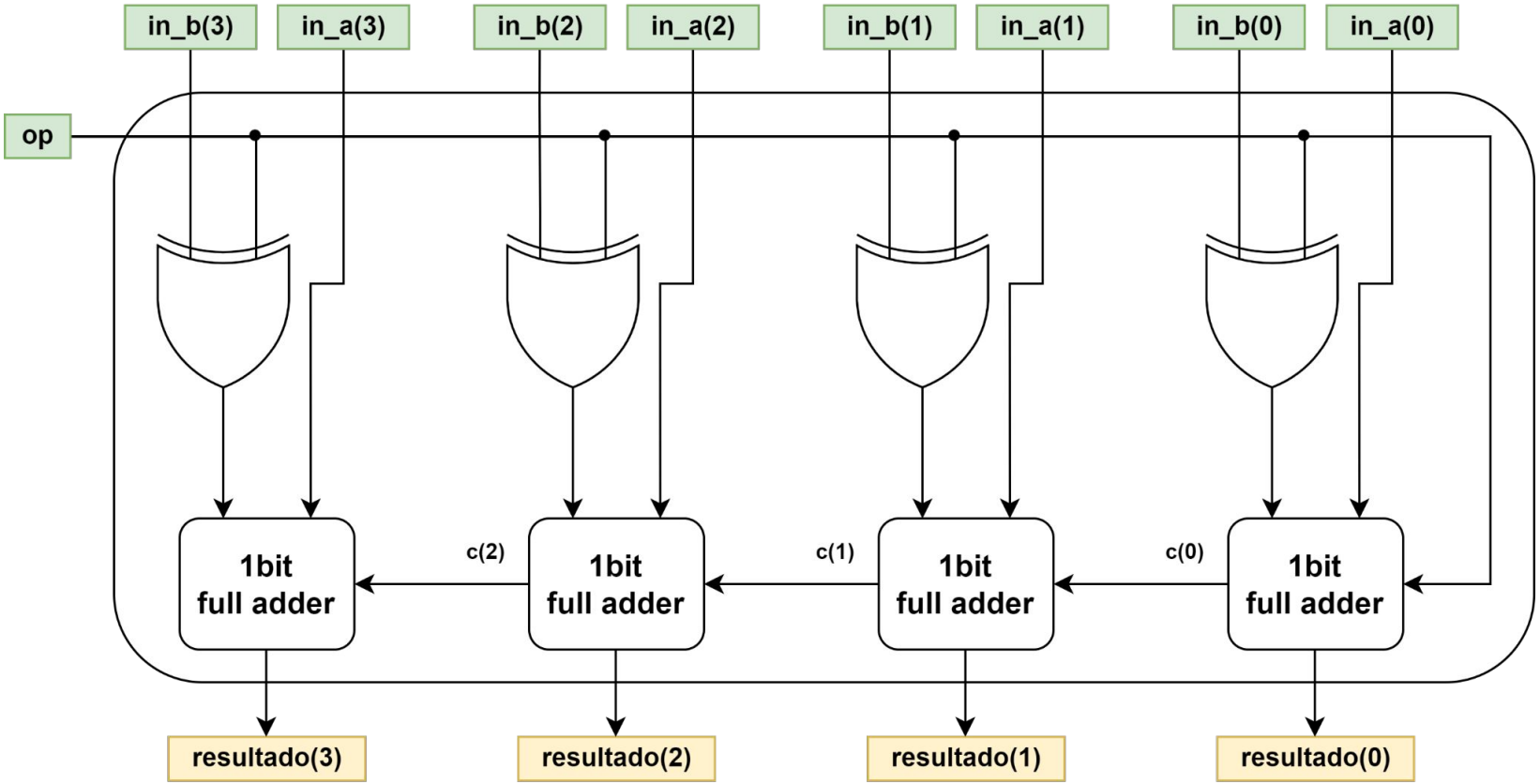
Logic gates

Testbench



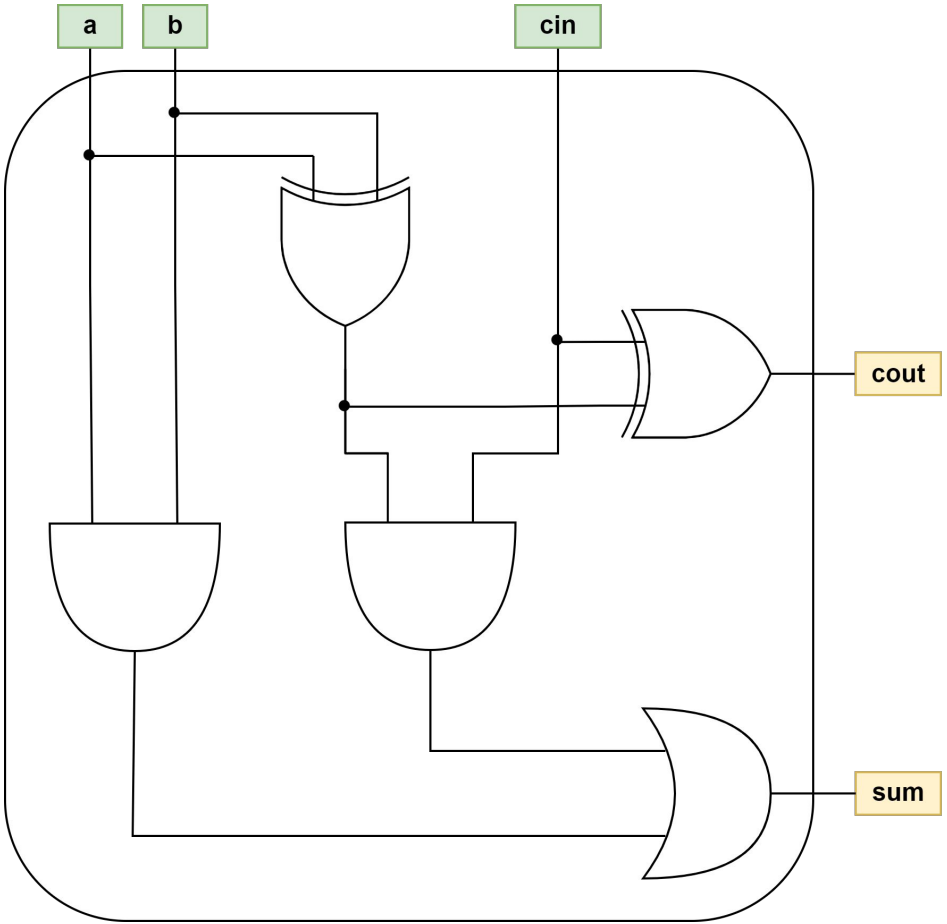
Logic gates

4bit adder/subtractor



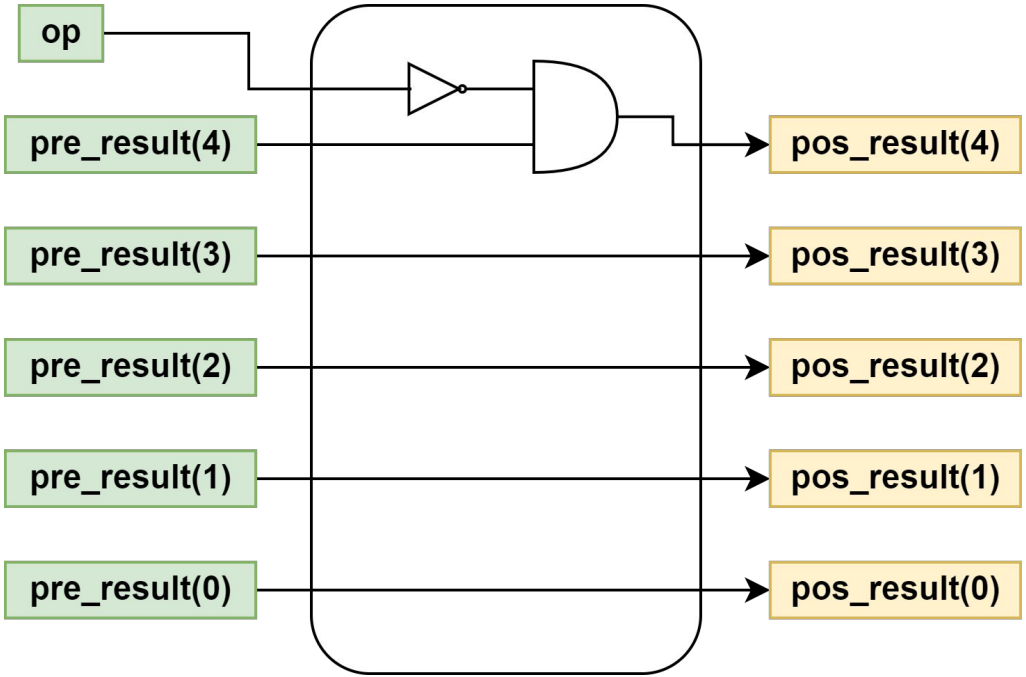
Logic gates

1bit full adder



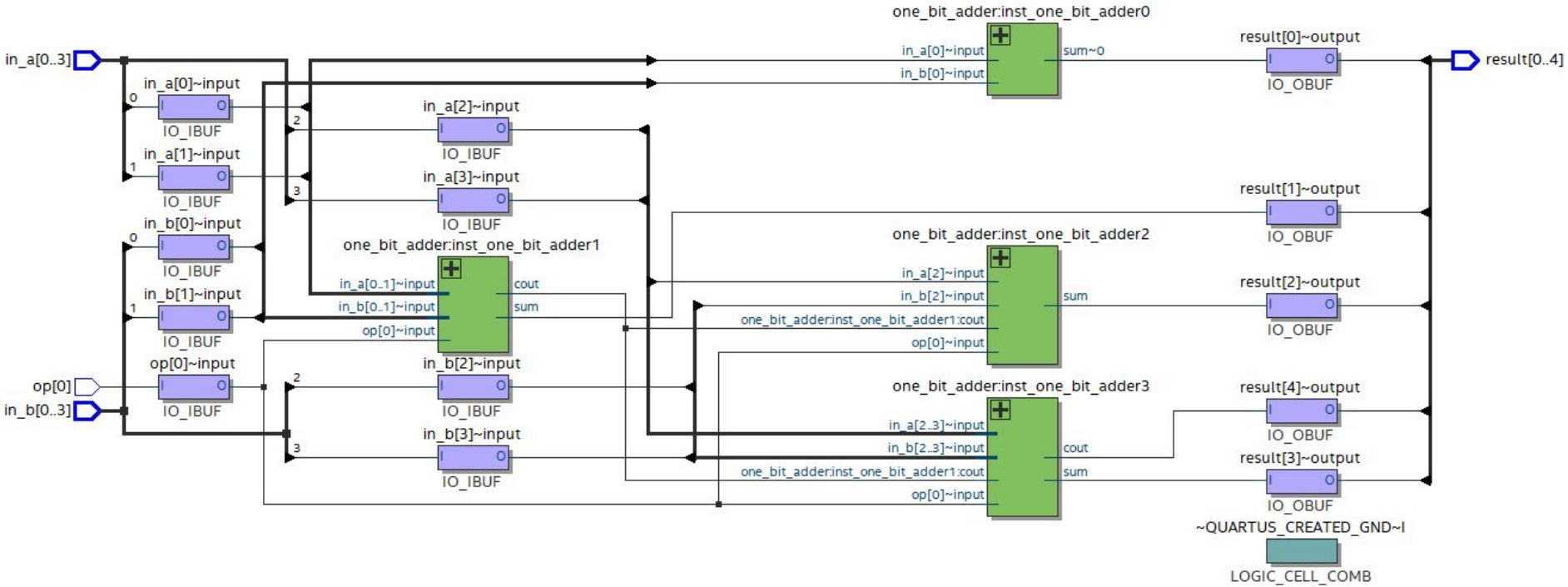
Logic gates

2’s complement to unsigned



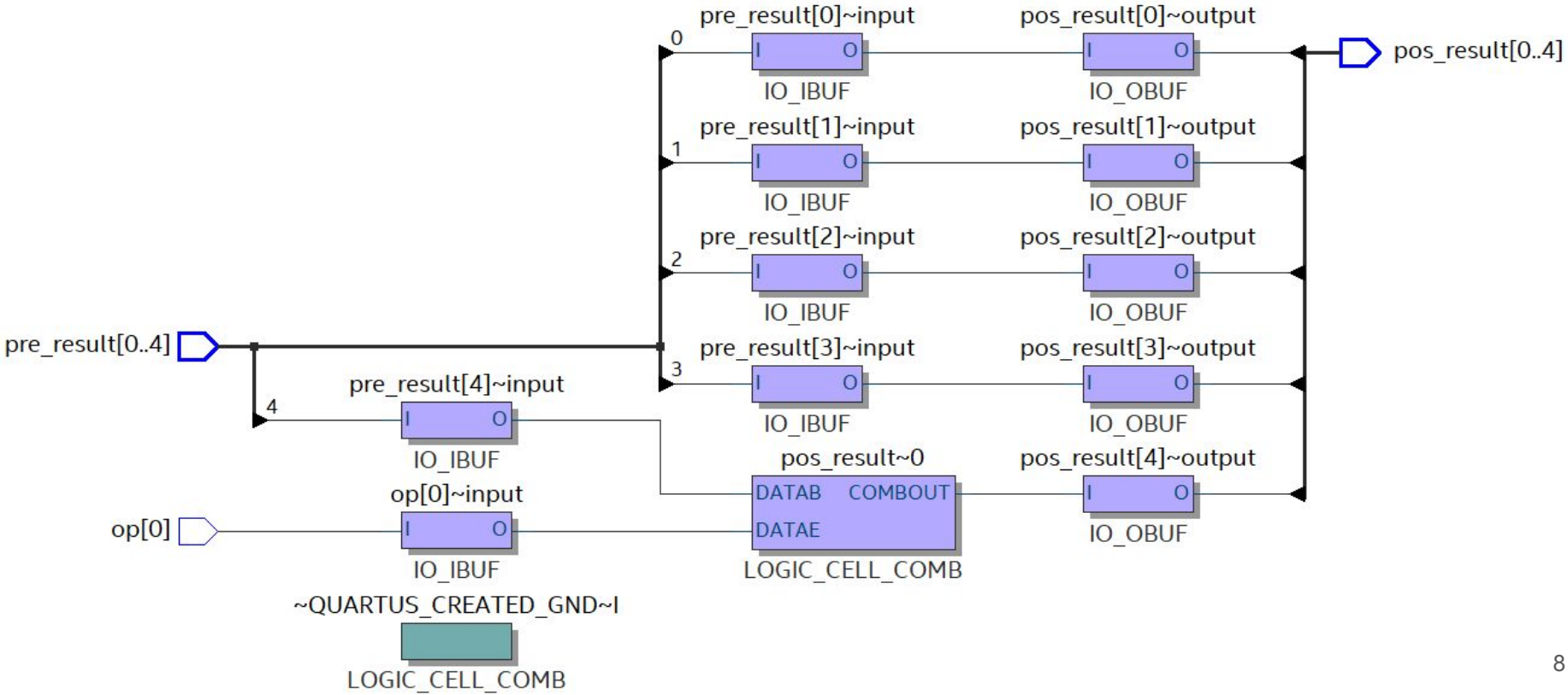
Register transfer level

4bit adder/subtractor



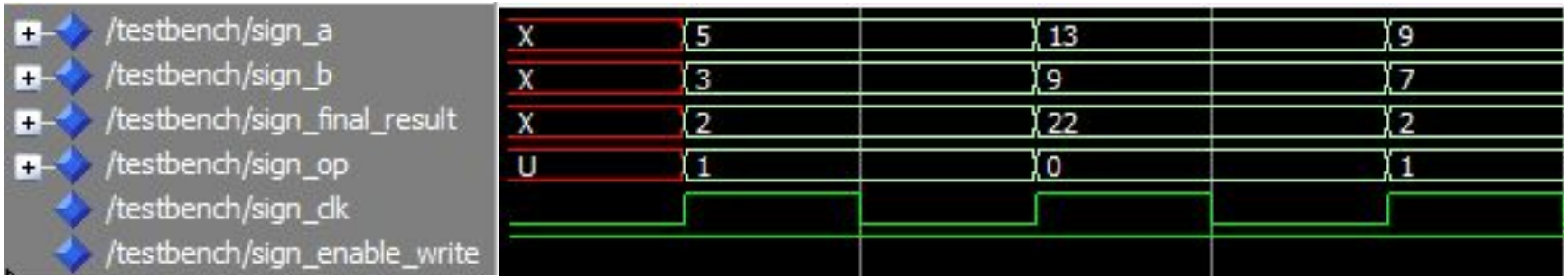
Register transfer level

2’s complement to unsigned

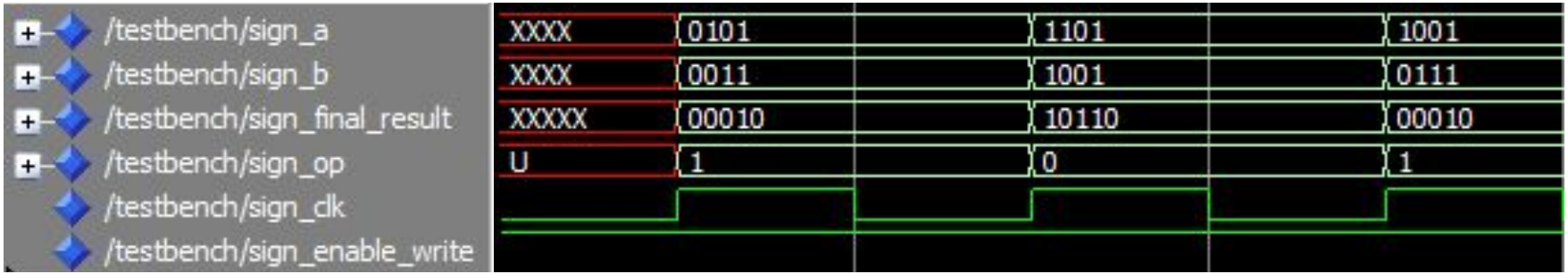


Simulation

Modelsim



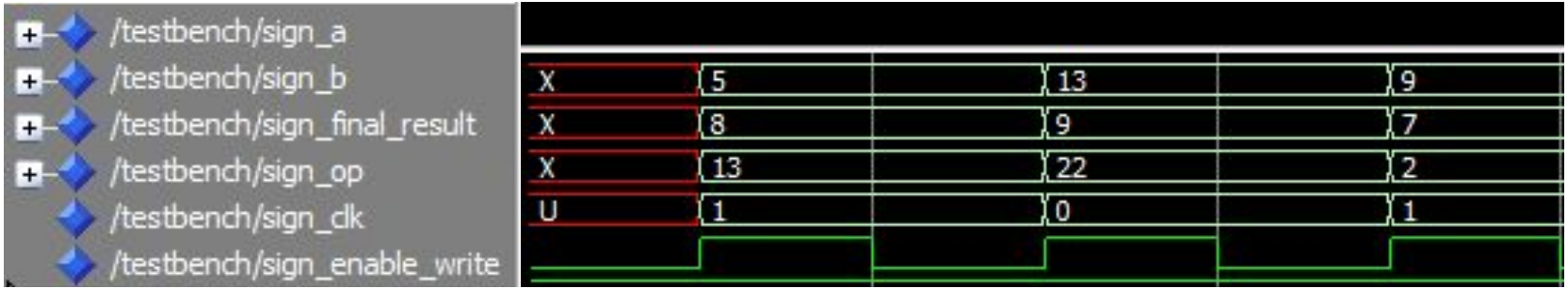
sign_a, *sign_b* and *sign_final_result* as **unsigned**



sign_a, *sign_b* and *sign_final_result* as **binary**

Simulation

Modelsim



Limitation: the 2nd operator (sign_b) must be smaller than the the 1st (sign_a).