



**ISEL**

**DEETC**

Departamento de  
Engenharia Electrónica e  
de Telecomunicações e  
de Computadores

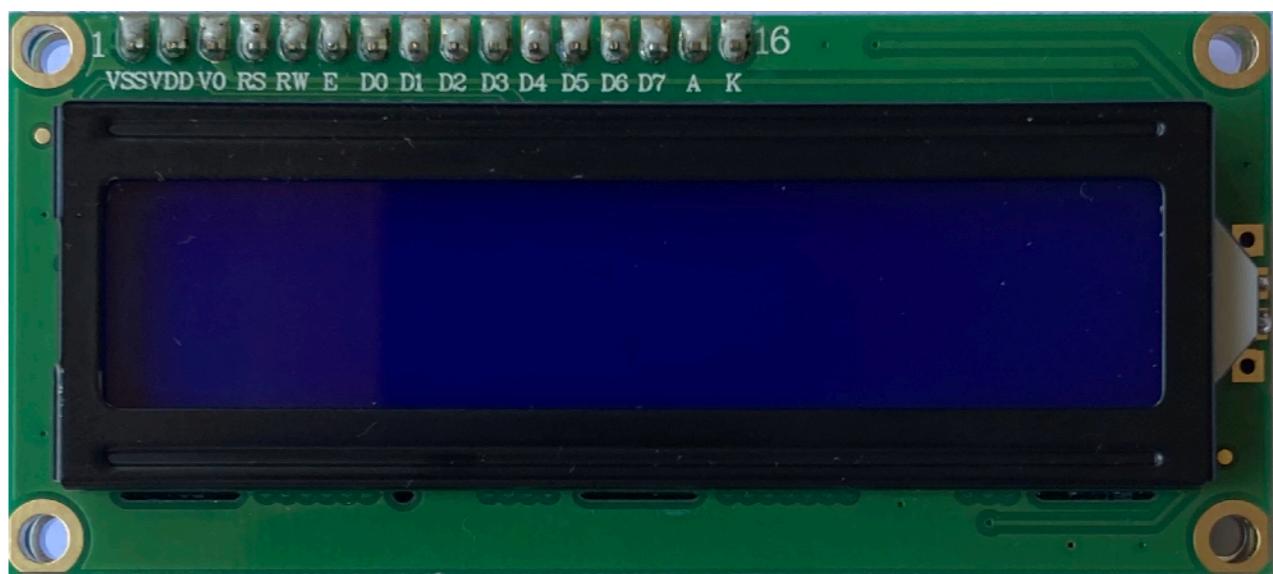
# **Laboratório de Informática e de Computadores**

2021 / 2022 verão

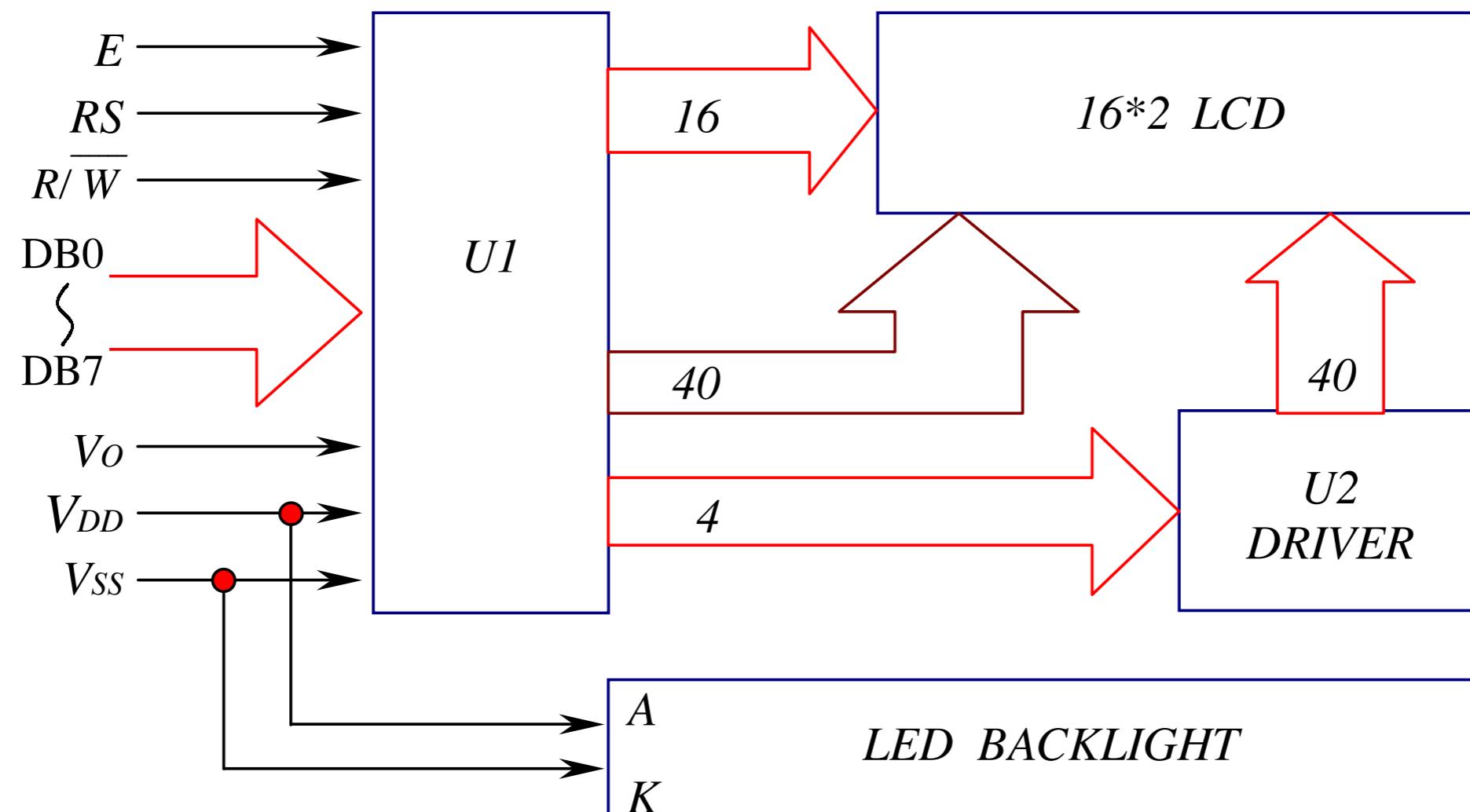
**LEIC**

# Liquid Cristal Display

Pin No	Name	I/O	Description
1	Vss	Power	GND
2	Vdd	Power	+5v
3	Vo	Analog	Contrast Control
4	RS	Input	Register Select
5	R/W	Input	Read/Write
6	E	Input	Enable ( <i>Strobe</i> )
7	D0	I/O	Data <i>LSB</i>
8	D1	I/O	Data
9	D2	I/O	Data
10	D3	I/O	Data
11	D4	I/O	Data
12	D5	I/O	Data
13	D6	I/O	Data
14	D7	I/O	Data <i>MSB</i>



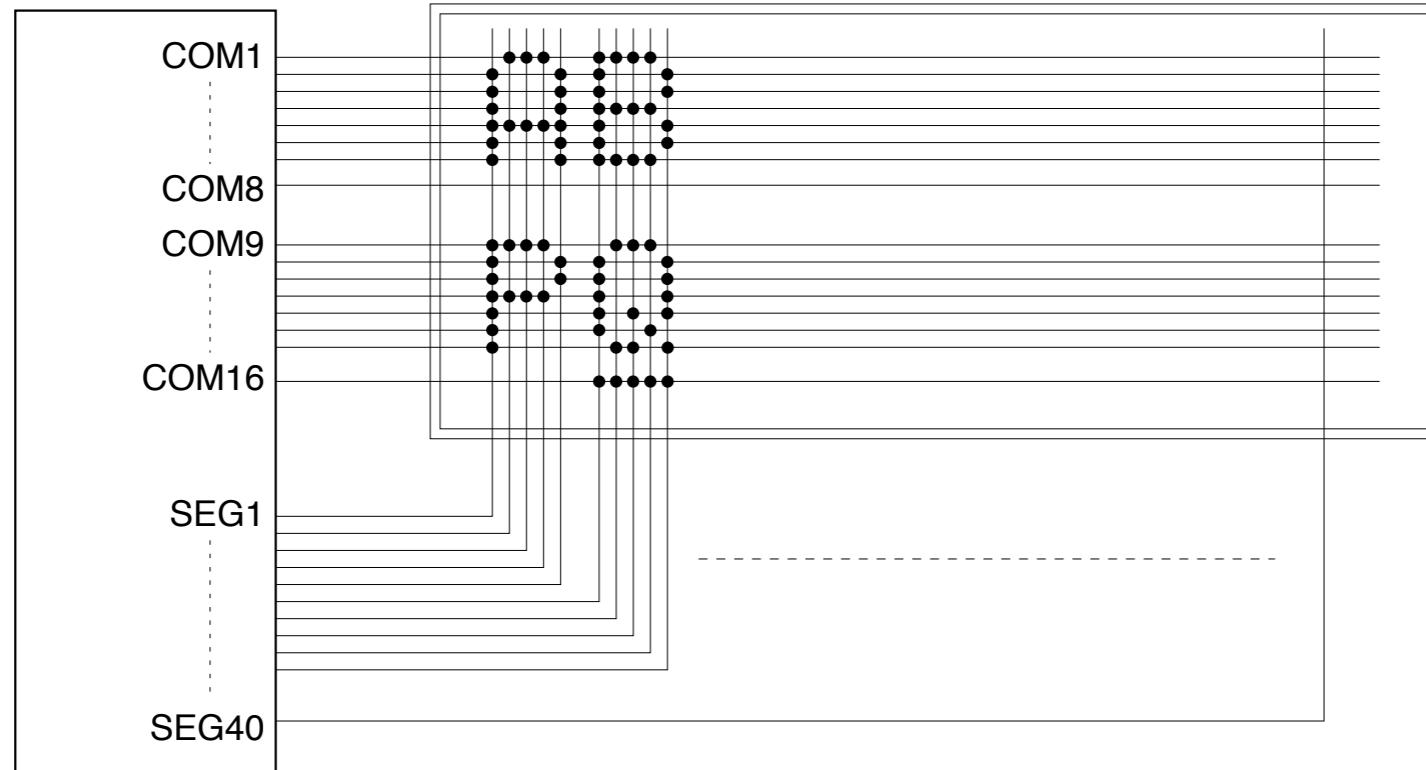
# Liquid Cristal Display



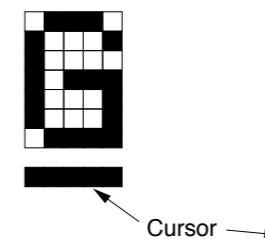
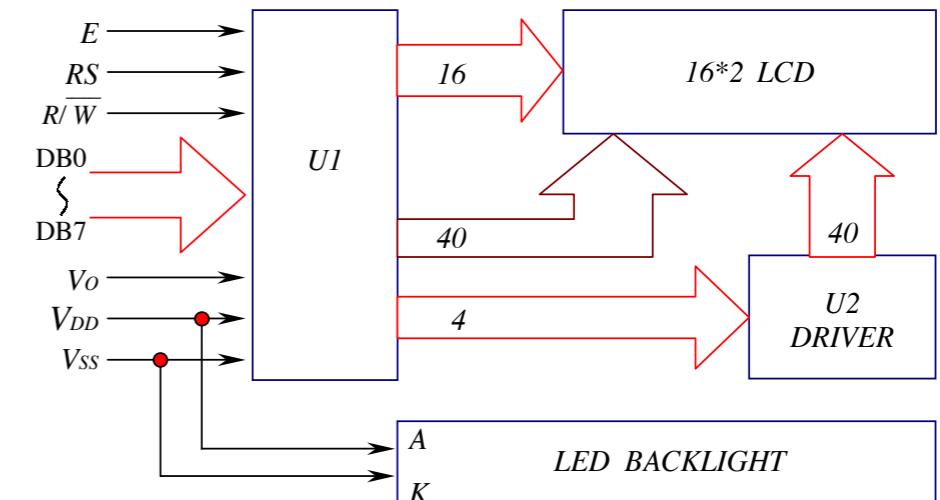
# Liquid Cristal Display



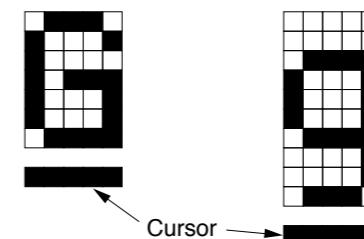
HD44780



Example of a  $5 \times 8$  dot, 8-character  $\times$  2-line display (1/5 bias, 1/16 duty cycle)

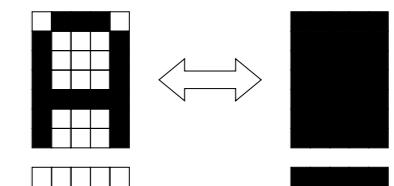


5  $\times$  8 dot character font  
Cursor



5  $\times$  10 dot character font  
Cursor

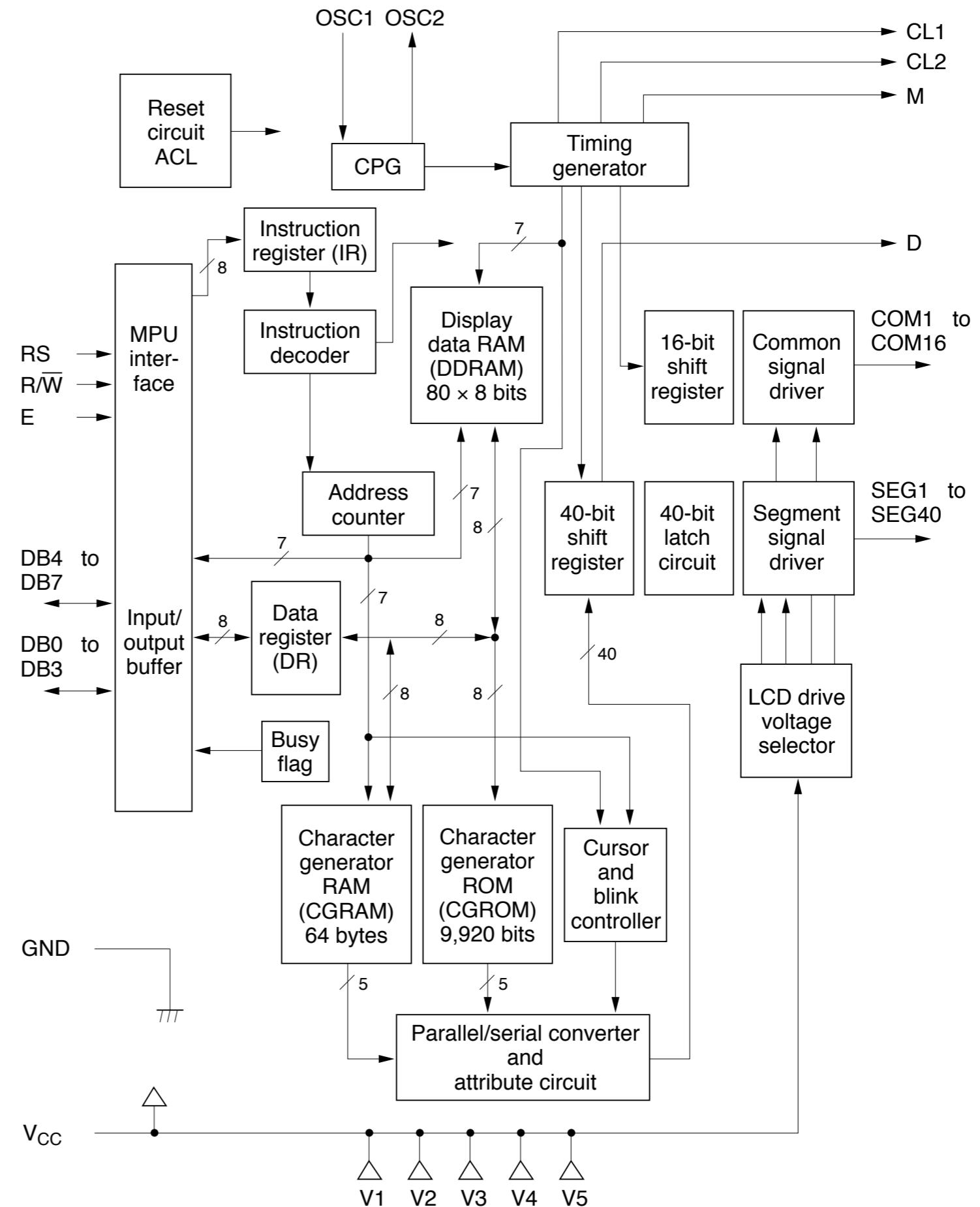
Cursor display example



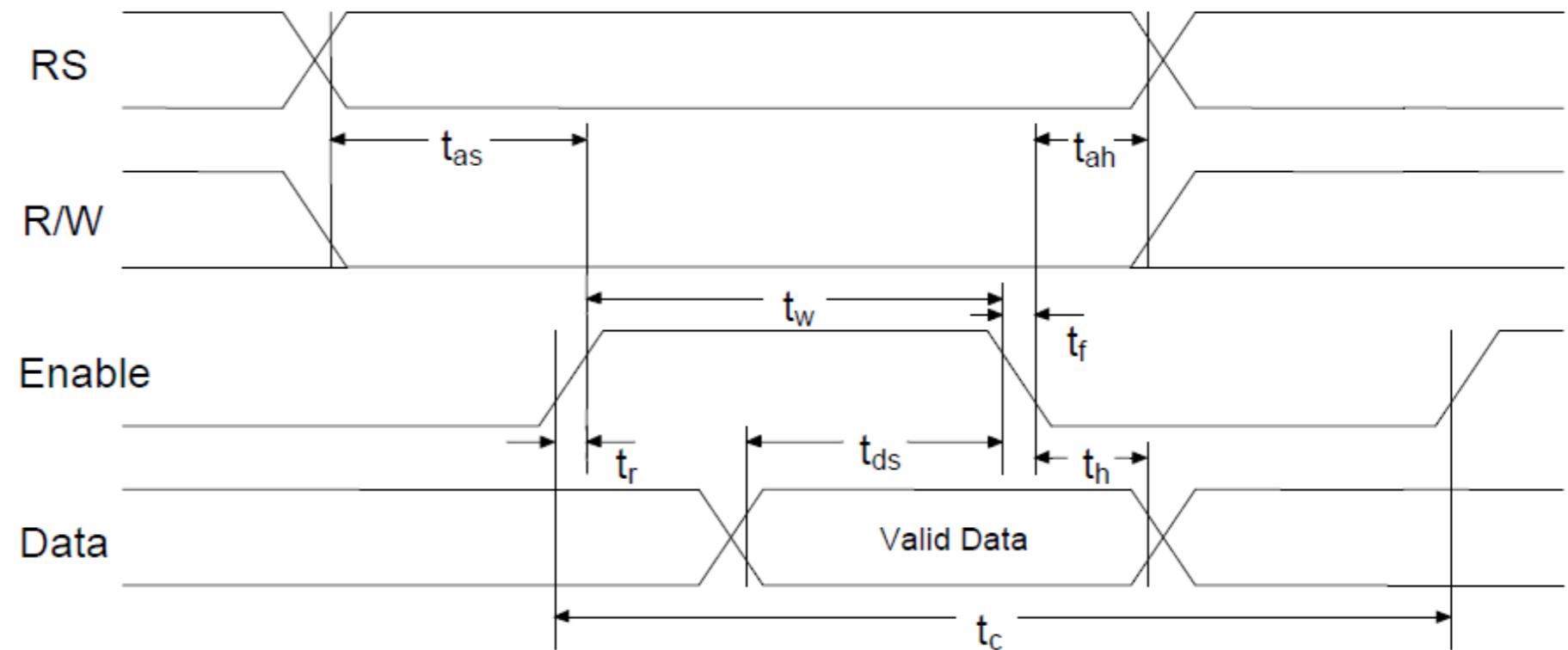
Alternating display

Blink display example

# LCD



# LCD

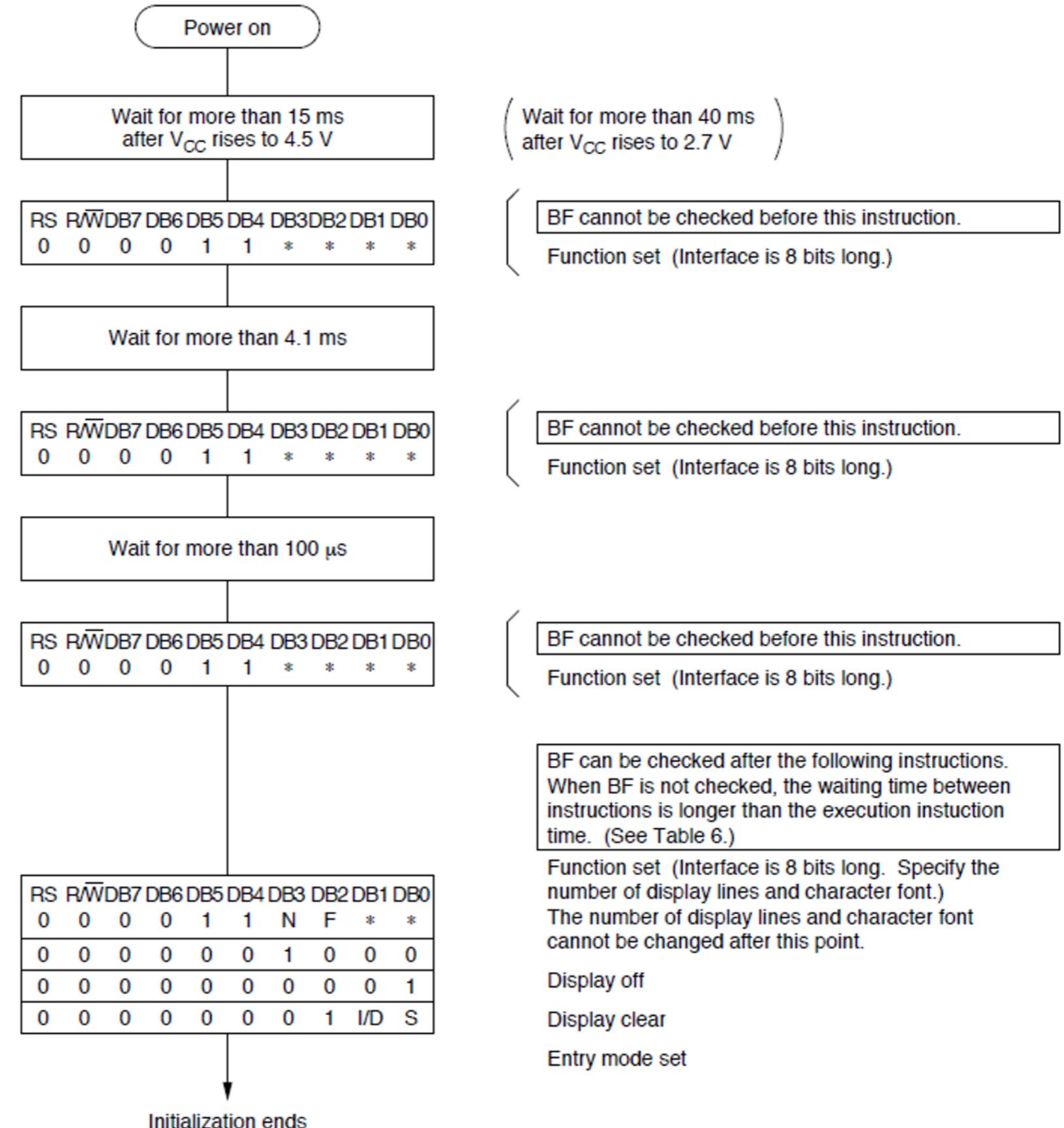


**Write cycle**

Parameter	Symbol	Min <sup>(1)</sup>	Typ <sup>(1)</sup>	Max <sup>(1)</sup>	Unit
Enable Cycle Time	$t_c$	500	-	-	ns
Enable Pulse Width (High)	$t_w$	230	-	-	ns
Enable Rise/Fall Time	$t_r, t_f$	-	-	20	ns
Address Setup Time	$t_{as}$	40	-	-	ns
Address Hold Time	$t_{ah}$	10	-	-	ns
Data Setup Time	$t_{ds}$	80	-	-	ns
Data Hold Time	$t_h$	10	-	-	ns

*Note <sup>1</sup> The above specifications are a indication only. Timing will vary from manufacturer to manufacturer.*

# LCD



# LCD



Display position

	1	2	3	4	5		39	40
	00	01	02	03	04	.....	26	27
	40	41	42	43	44	.....	66	67

DDRAM address  
(hexadecimal)

Instruction	Code										Execution Time (max) (when $f_{cp}$ or $f_{osc}$ is 270 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.
Return home	0	0	0	0	0	0	0	0	1	—	Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DDRAM contents.
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).
Set CGRAM address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM address. CGRAM data is sent and received after this setting.
Set DDRAM address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM address. DDRAM data is sent and received after this setting.
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.
Write data to CG or DDRAM	1	0	Write data						Writes data into DDRAM or CGRAM.		37 µs $t_{ADD} = 4 \mu s^*$
Read data from CG or DDRAM	1	1	Read data						Reads data from DDRAM or CGRAM.		37 µs $t_{ADD} = 4 \mu s^*$
I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5 × 10 dots, F = 0: 5 × 8 dots BF = 1: Internally operating BF = 0: Instructions acceptable										DDRAM: Display data RAM CGRAM: Character generator RAM ACG: CGRAM address ADD: DDRAM address (corresponds to cursor address) AC: Address counter used for both DD and CGRAM addresses	Execution time changes when frequency changes Example: When $f_{cp}$ or $f_{osc}$ is 250 kHz, $37 \mu s \times \frac{270}{250} = 40 \mu s$

Note: — indicates no effect.

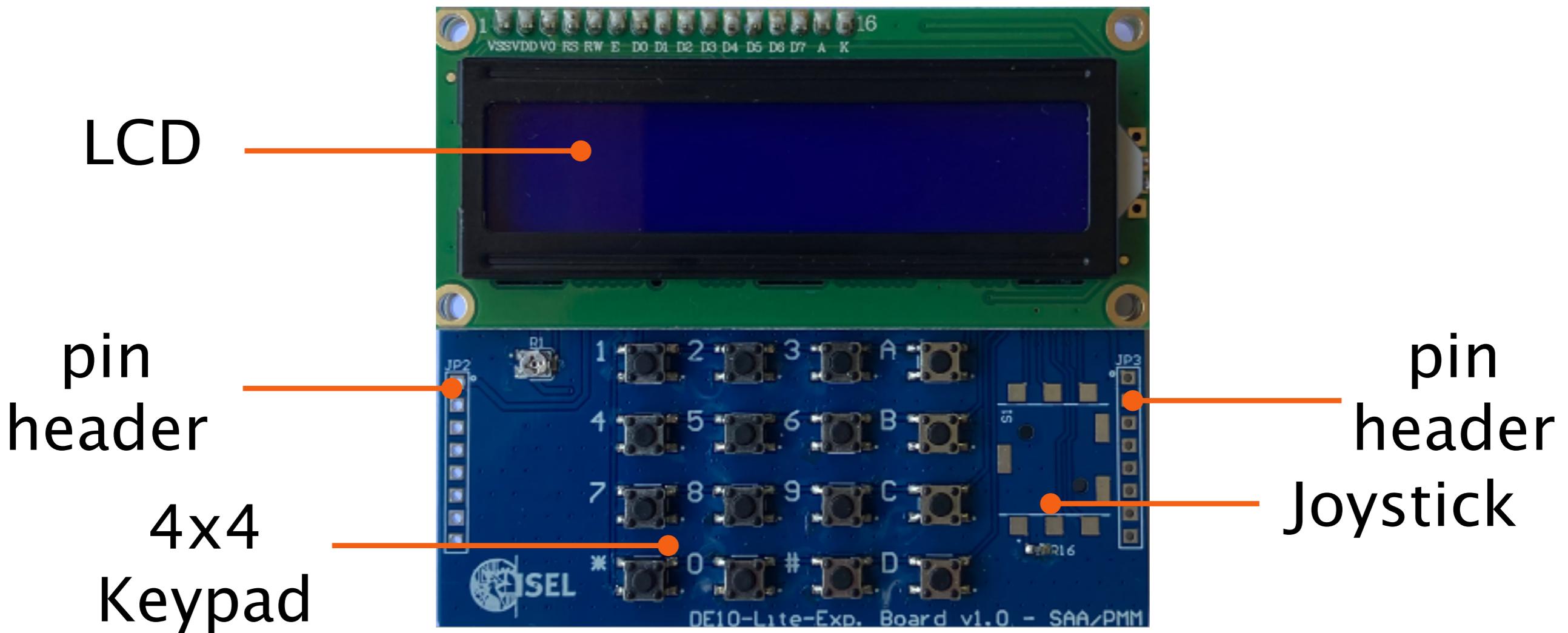
\* After execution of the CGRAM/DDRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In Figure 10,  $t_{ADD}$  is the time elapsed after the busy flag turns off until the address counter is updated.

# LCD



```
LCD { // Escreve no LCD usando a interface a 8 bits.  
    private const val LINES = 2, COLS = 16; // Dimensão do display.  
    // Escreve um byte de comando/dados no LCD em série  
    private fun writeByteSerial(rs: Boolean, data: Int) ...  
    // Escreve um byte de comando/dados no LCD  
    private fun writeByte(rs: Boolean, data: Int) ...  
    // Escreve um comando no LCD  
    private fun writeCMD(data: Int) ...  
    // Escreve um dado no LCD  
    private fun writeDATA(data: Int) ...  
    // Envia a sequência de iniciação para comunicação a 8 bits.  
    fun init() ...  
    // Escreve um carácter na posição corrente.  
    fun write(c: Char) ...  
    // Escreve uma string na posição corrente.  
    fun write(text: String) ...  
    // Envia comando para posicionar cursor ('line':0..LINES-1 , 'column':0..COLS-1)  
    fun cursor(line: Int, column: Int) ...  
    // Envia comando para limpar o ecrã e posicionar o cursor em (0,0)  
    fun clear() ...  
}
```

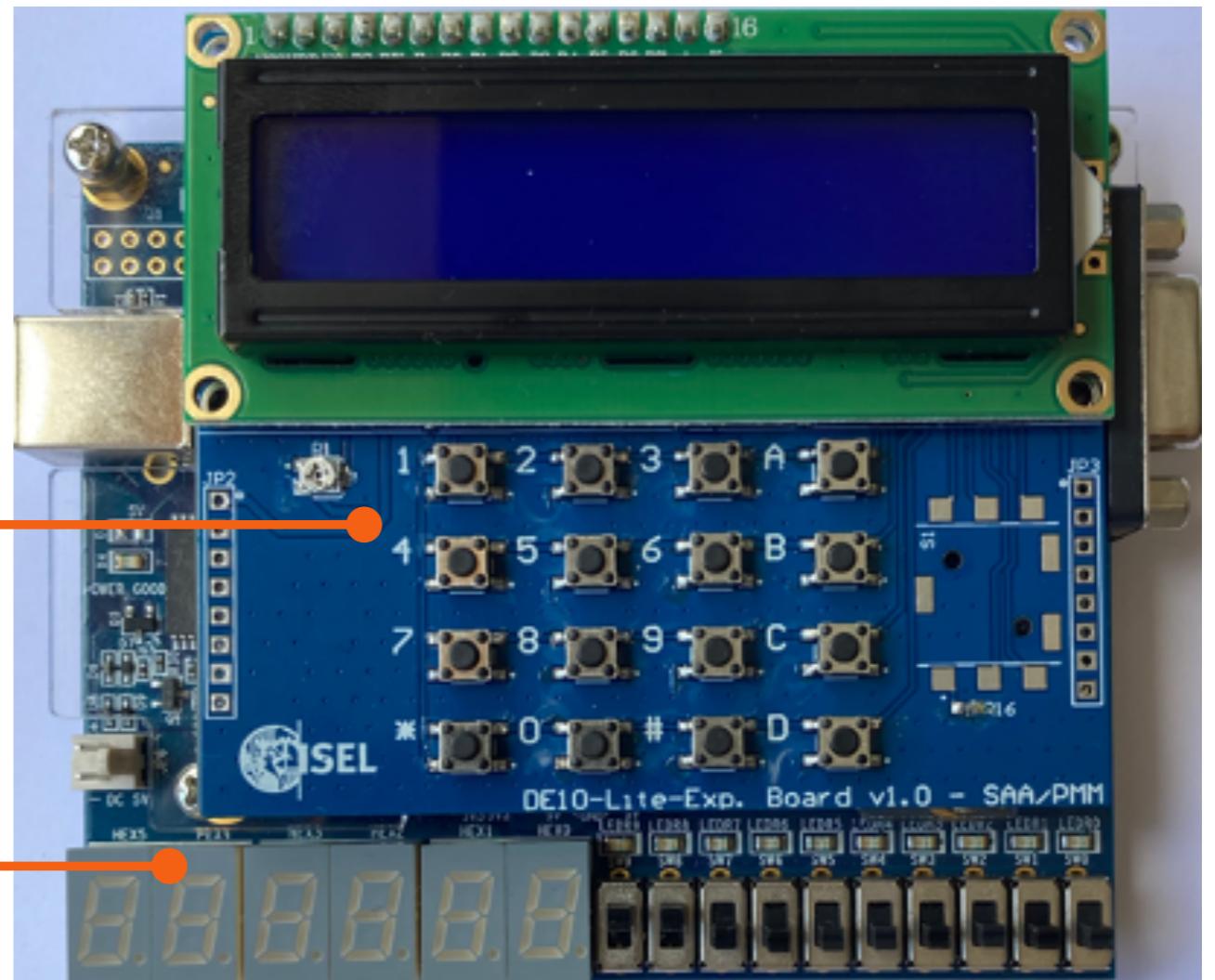
# DE10-Lite Exp. Board v1.0



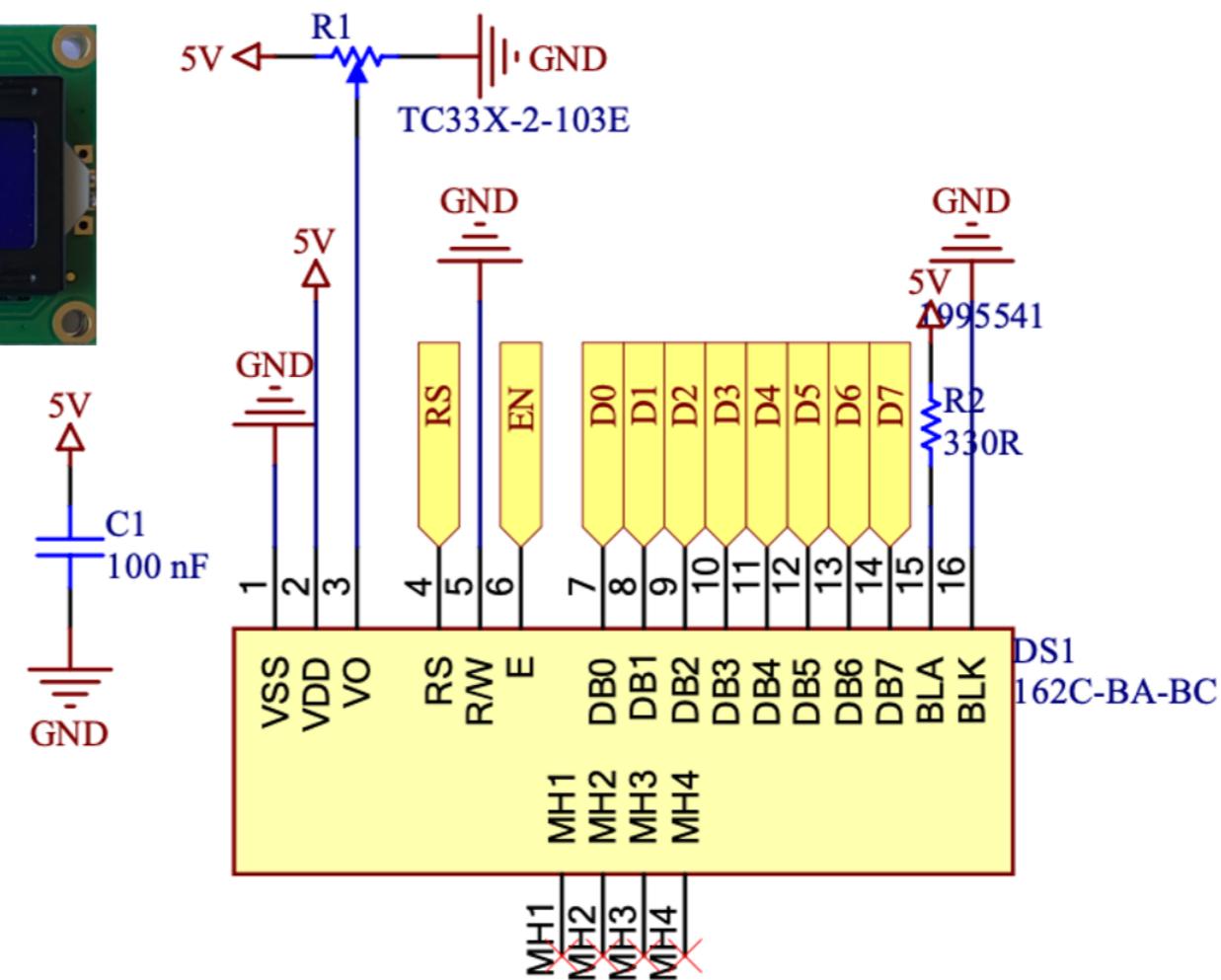
# DE10-Lite Exp. Board v1.0

Expansion  
board

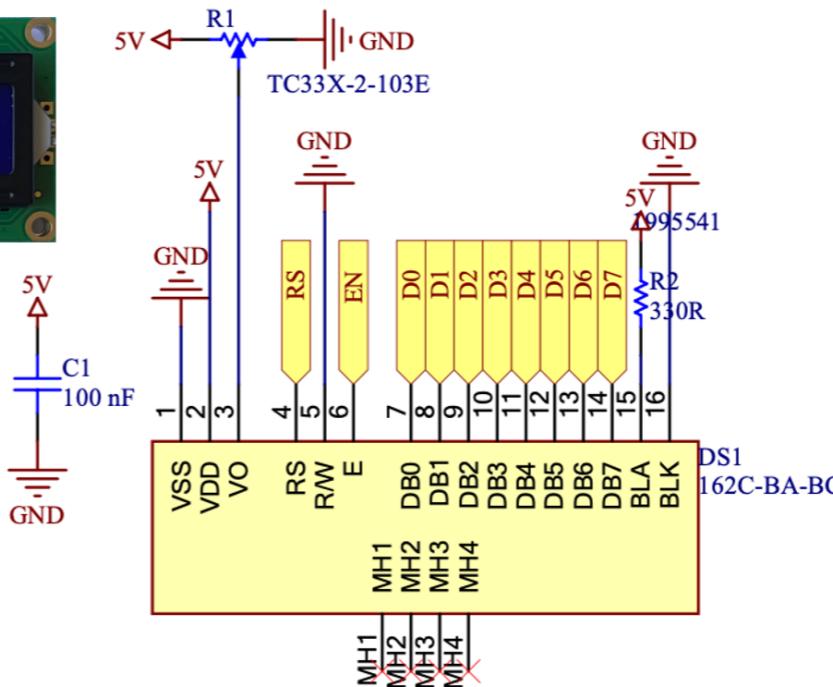
DE10-Lite  
development  
board



# DE10-Lite Exp. Board v1.0



# DE10-Lite Exp. Board v1.0



Signal Name	FPGA Pin No.	Description	I/O Standard
LCD_RS	PIN_W8	RS	3.3-V LVTTL
LCD_EN	PIN_V5	Enable	3.3-V LVTTL
LCD_DATA[0]	PIN_AA15	D0	3.3-V LVTTL
LCD_DATA[1]	PIN_W13	D1	3.3-V LVTTL
LCD_DATA[2]	PIN_AB13	D2	3.3-V LVTTL
LCD_DATA[3]	PIN_Y11	D3	3.3-V LVTTL
LCD_DATA[4]	PIN_W11	D4	3.3-V LVTTL
LCD_DATA[5]	PIN_AA10	D5	3.3-V LVTTL
LCD_DATA[6]	PIN_Y8	D6	3.3-V LVTTL
LCD_DATA[7]	PIN_Y7	D7	3.3-V LVTTL