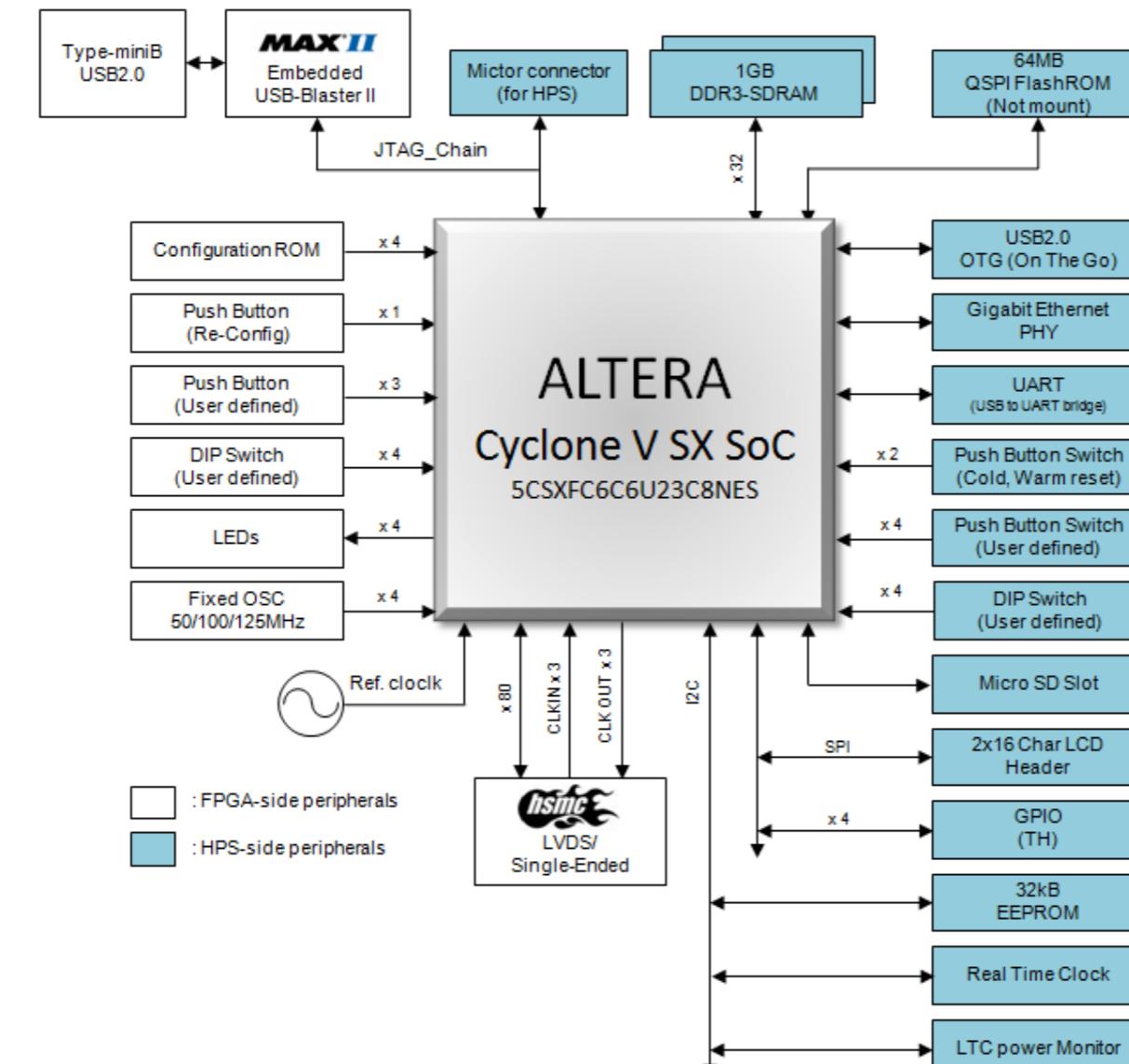


# Helio Board



PAGE	DESCRIPTION
1	Block Diagram
2	FPGA Package Top
3	Cyclone V SoC Bank 3 & 4
4	Cyclone V SoC Bank 5 & 6
5	Cyclone V SoC Bank 7
6	Cyclone V SoC Transceivers & Clocks
7	PLL
8	Cyclone V SoC Configuration
9	JTAG
10	DDR3
11	HSMC
12	Ethernet PHY & RJ45
13	QSPI Flash & Reset Circuit
14	USB 2.0 OTG & Micro SD Card
15	User I/O ,RTC
16	UART
17	On-Board USB Blaster II
18	Power Monitor
19	Power1 - DC Input, 1.1V
20	Power2 - 3.3V
21	Power3 - 1.5V, DDR
22	Power4 - 2.5V, 5V, 1.8V
23	Power5 - 3.3V_EXT
24	Cyclone V SoC Power
25	Cyclone V SoC Capacitor
26	History

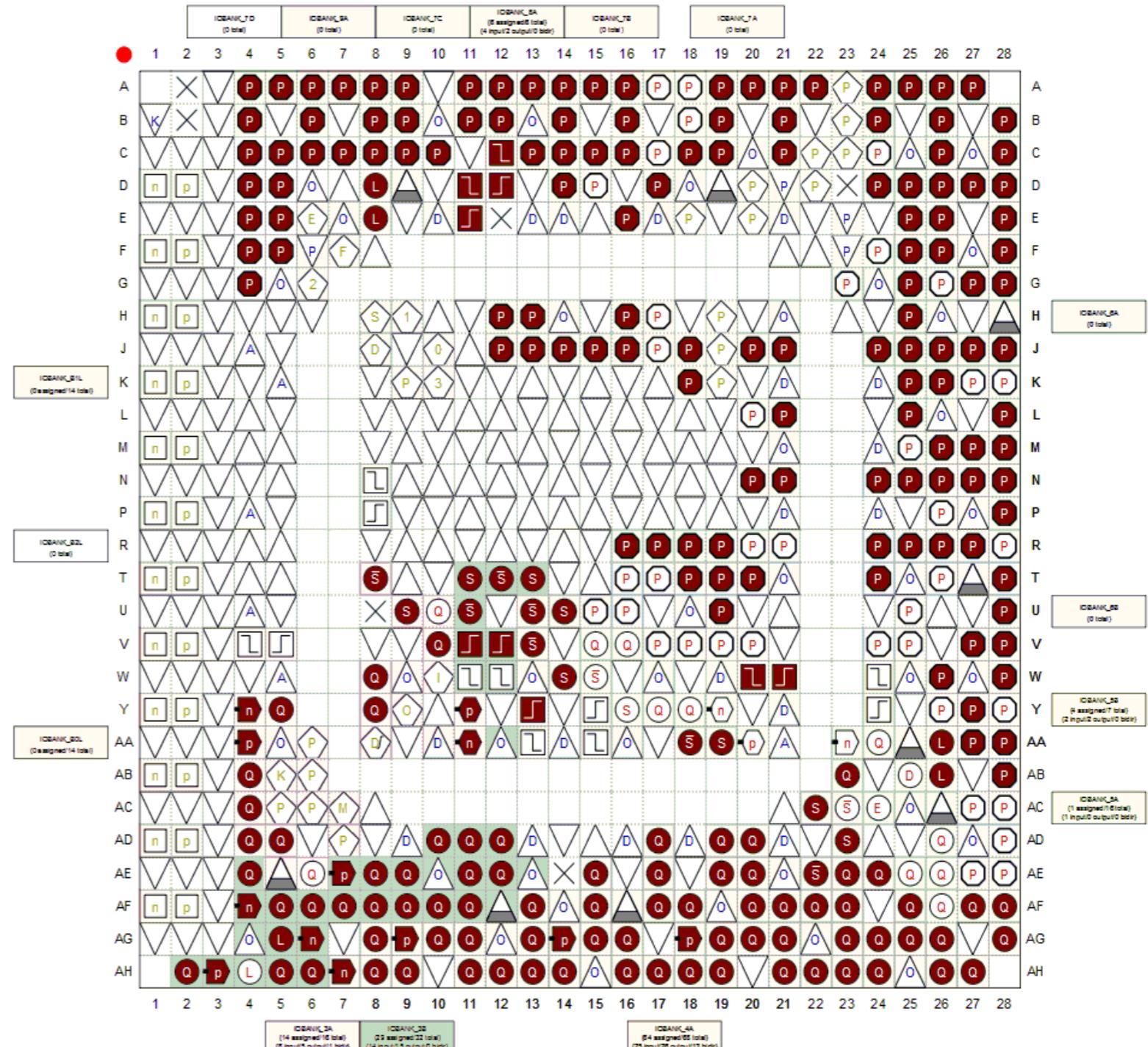
Designed NOV. 20, 2013	 <b>ALTIMA Corporation</b> 1-5-5, Shin-Yokohama, Kouhoku-ku, Yokohama, 222-8563 JAPAN		
Drawn NOV. 20, 2013			
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# FPGA Package Top View

Top View - Wire Bond

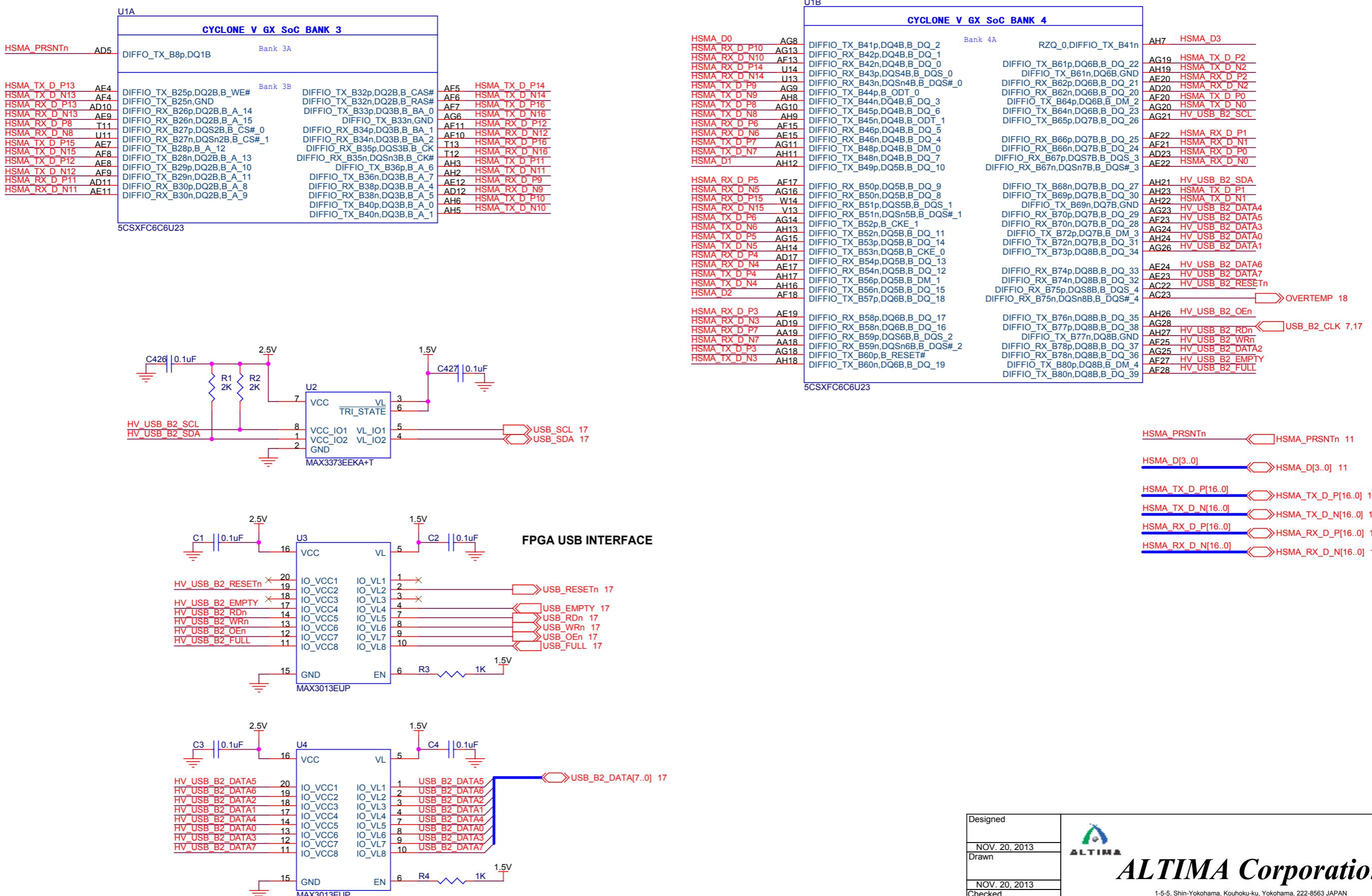
Cyclone V - 5CSXFC6C6U23C8ES

I/O Bank Usage					
I/O Bank	Usage	VCCIO Voltage	VREF Voltage	VCCPD Voltage	
1 B2L	0 / 0 ( -- )	--	--	--	
2 B1L	0 / 14 ( 0 % )	--	--	--	
3 B0L	0 / 14 ( 0 % )	--	--	--	
4 3A	14 / 16 ( 88 % )	2.5V	--	2.5V	
5 3B	29 / 32 ( 91 % )	2.5V	--	2.5V	
6 4A	64 / 68 ( 94 % )	2.5V	--	2.5V	
7 5A	2 / 16 ( 13 % )	2.5V	--	2.5V	
8 5B	4 / 7 ( 57 % )	2.5V	--	2.5V	
9 6B	23 / 45 ( 51 % )	1.5V	0.75V	2.5V	
10 6A	46 / 57 ( 81 % )	1.5V	0.75V	2.5V	
11 7A	13 / 19 ( 68 % )	3.3V	--	3.3V	
12 7B	21 / 22 ( 95 % )	3.3V	--	3.3V	
13 7C	12 / 12 ( 100 % )	3.3V	--	3.3V	
14 7D	14 / 14 ( 100 % )	3.3V	--	3.3V	
15 8A	6 / 6 ( 100 % )	2.5V	--	2.5V	



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# Cyclone V SoC Bank 3 & 4

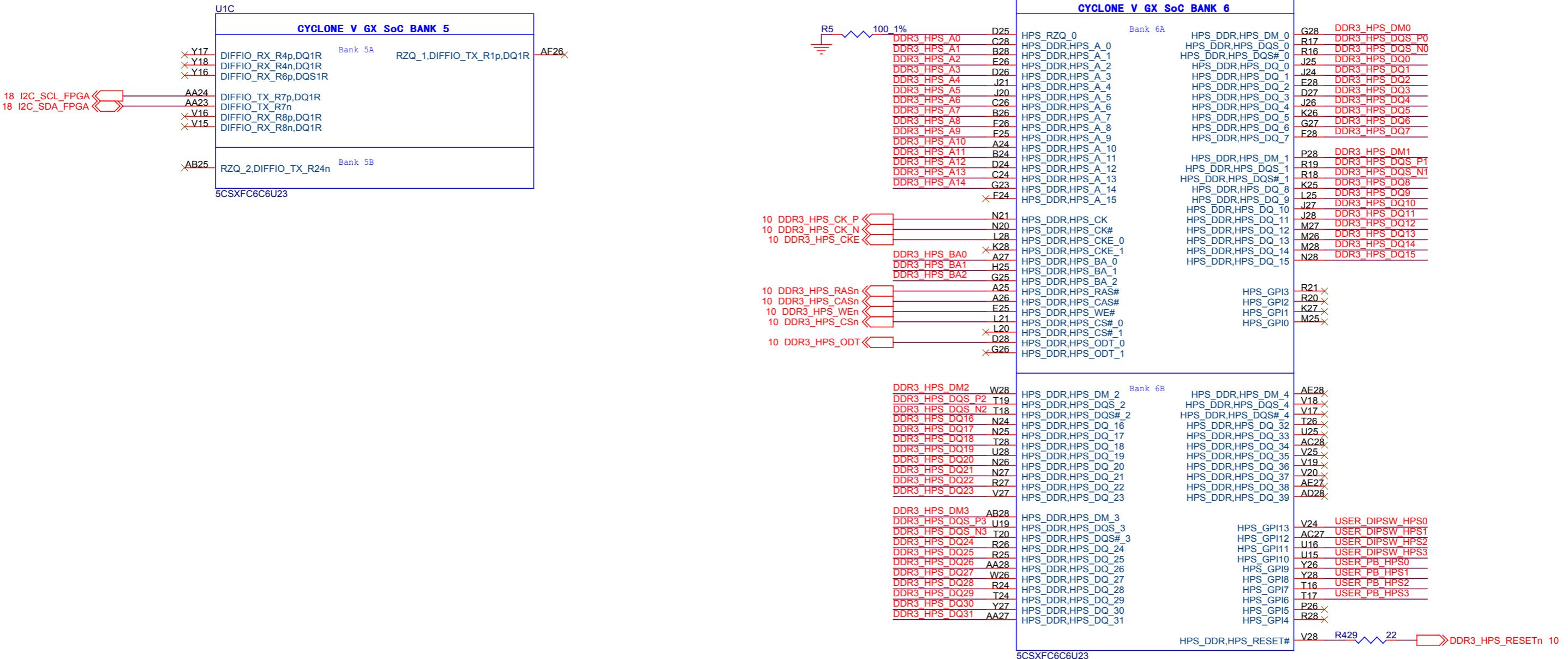


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NOV. 20, 2013			
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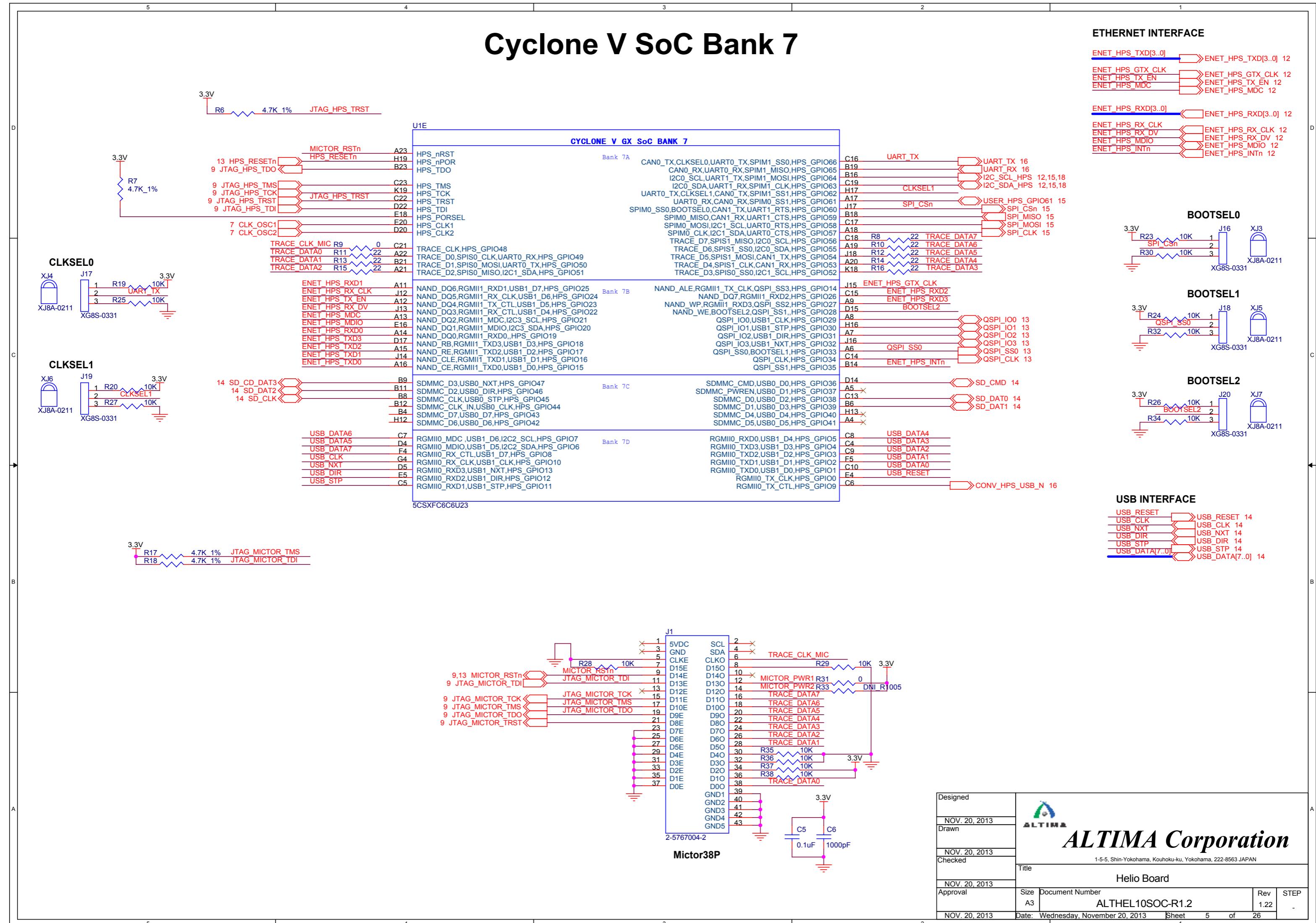
# Cyclone V SoC Bank 5, 6



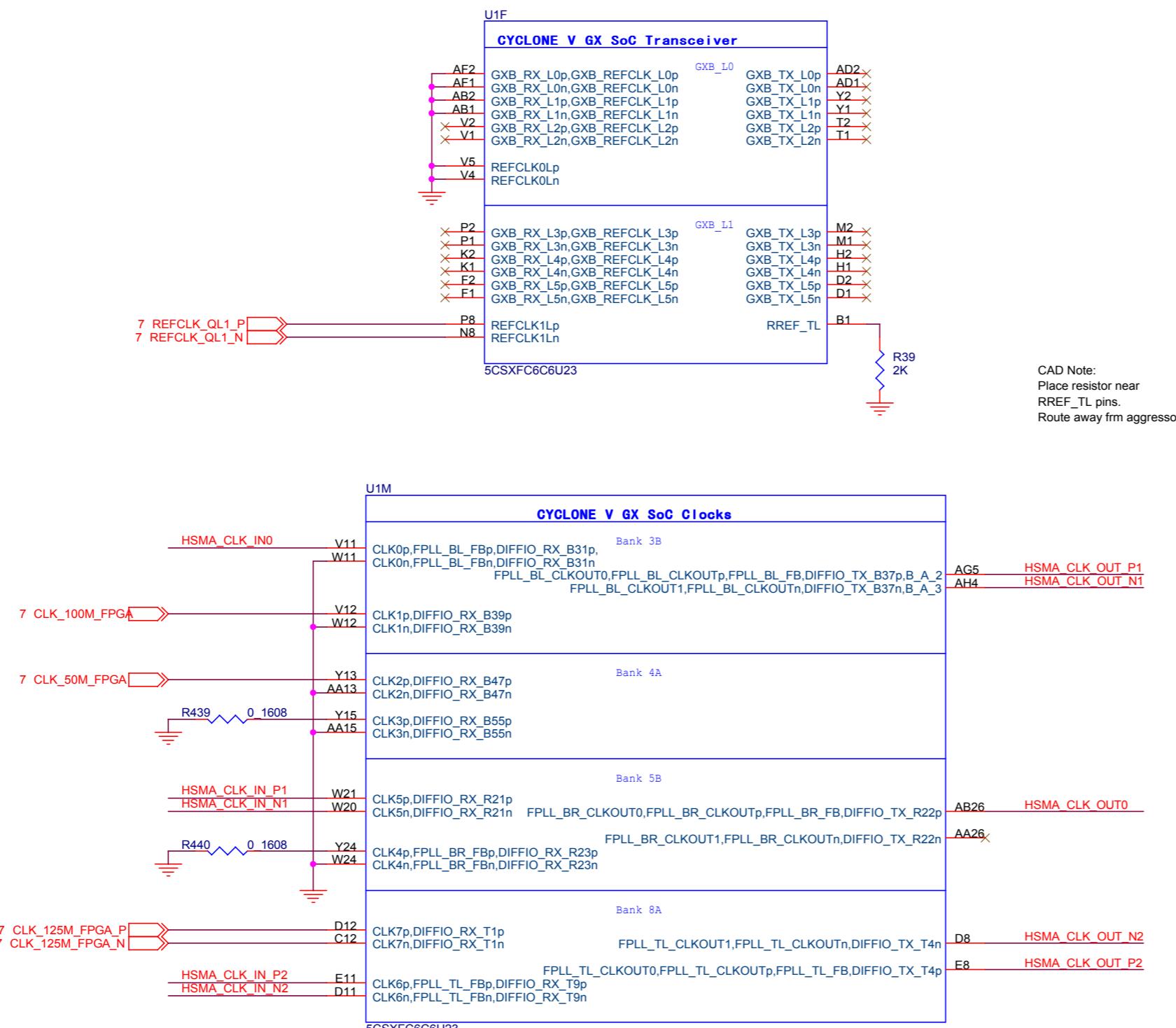
DDR3\_HPS\_A[14..0] → DDR3\_HPS\_A[14..0] 10  
 DDR3\_HPS\_BA[2..0] → DDR3\_HPS\_BA[2..0] 10  
 DDR3\_HPS\_DQS\_P[3..0] → DDR3\_HPS\_DQS\_P[3..0] 10  
 DDR3\_HPS\_DQS\_N[3..0] → DDR3\_HPS\_DQS\_N[3..0] 10  
 DDR3\_HPS\_DQ[31..0] → DDR3\_HPS\_DQ[31..0] 10  
 DDR3\_HPS\_DM[3..0] → DDR3\_HPS\_DM[3..0] 10

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Drawn			
Checked	Title <b>Helio Board</b>		
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NOV. 20, 2013	NOV. 20, 2013	NOV. 20, 2013	NOV. 20, 2013

# Cyclone V SoC Bank 7



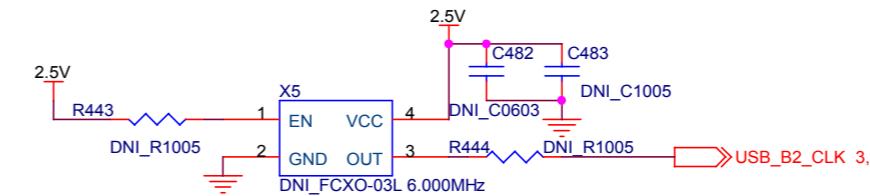
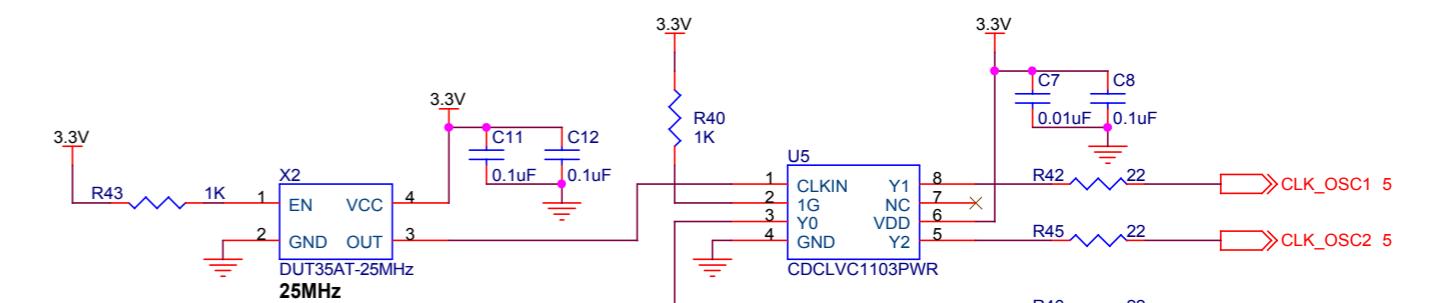
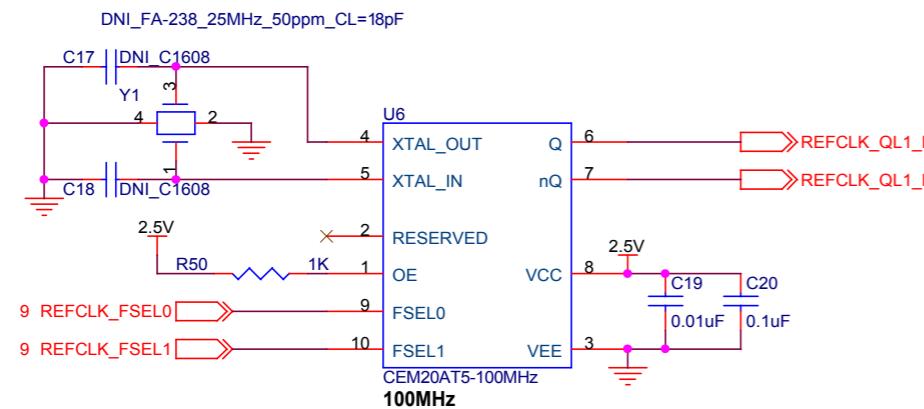
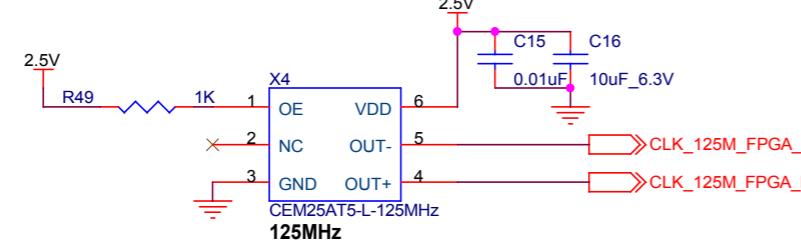
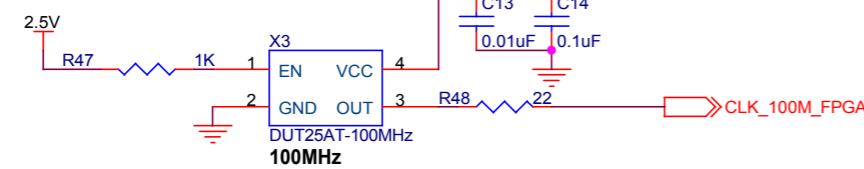
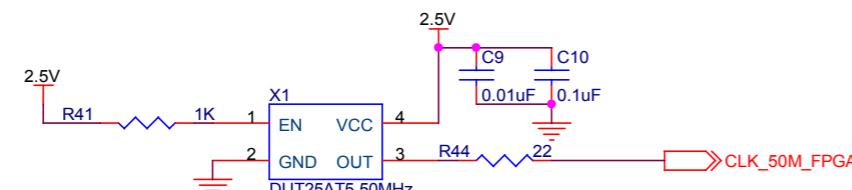
# Cyclone V SoC Transceivers & Clocks



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NOV. 20, 2013			
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NOV. 20, 2013			
Checked	NOV. 20, 2013		
NOV. 20, 2013			
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HSMA_CLK_OUT0	HSMA_CLK_OUT0_11
HSMA_CLK_OUT_P[2..1]	HSMA_CLK_OUT_P[2..1]_11
HSMA_CLK_OUT_N[2..1]	HSMA_CLK_OUT_N[2..1]_11
HSMA_CLK_IN0	HSMA_CLK_IN0_11
HSMA_CLK_IN_P[2..1]	HSMA_CLK_IN_P[2..1]_11
HSMA_CLK_IN_N[2..1]	HSMA_CLK_IN_N[2..1]_11

# PLL



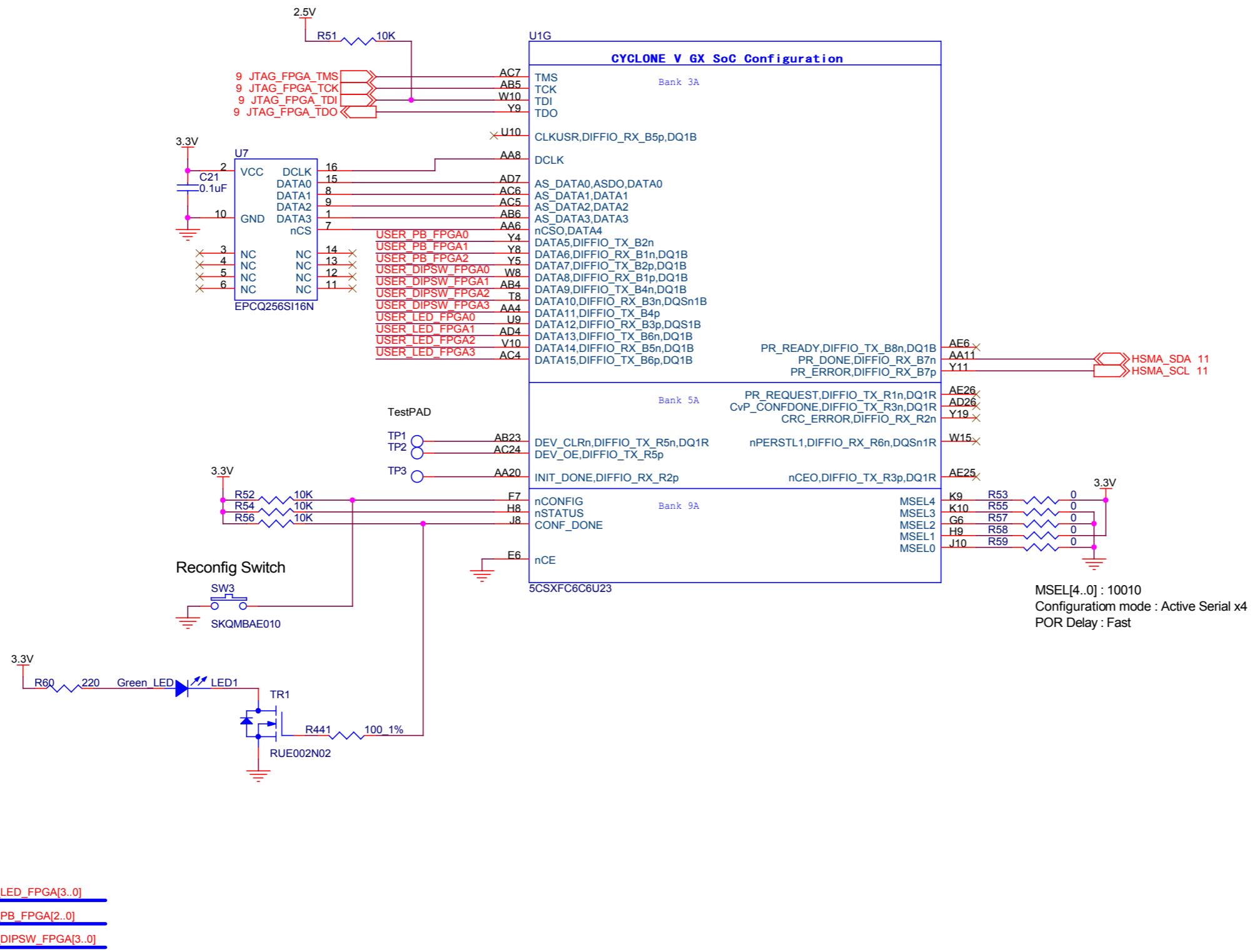
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Checked	NOV. 20, 2013		
Approved	NOV. 20, 2013		
Title	Helio Board		
Size	Document Number	Rev	STEP
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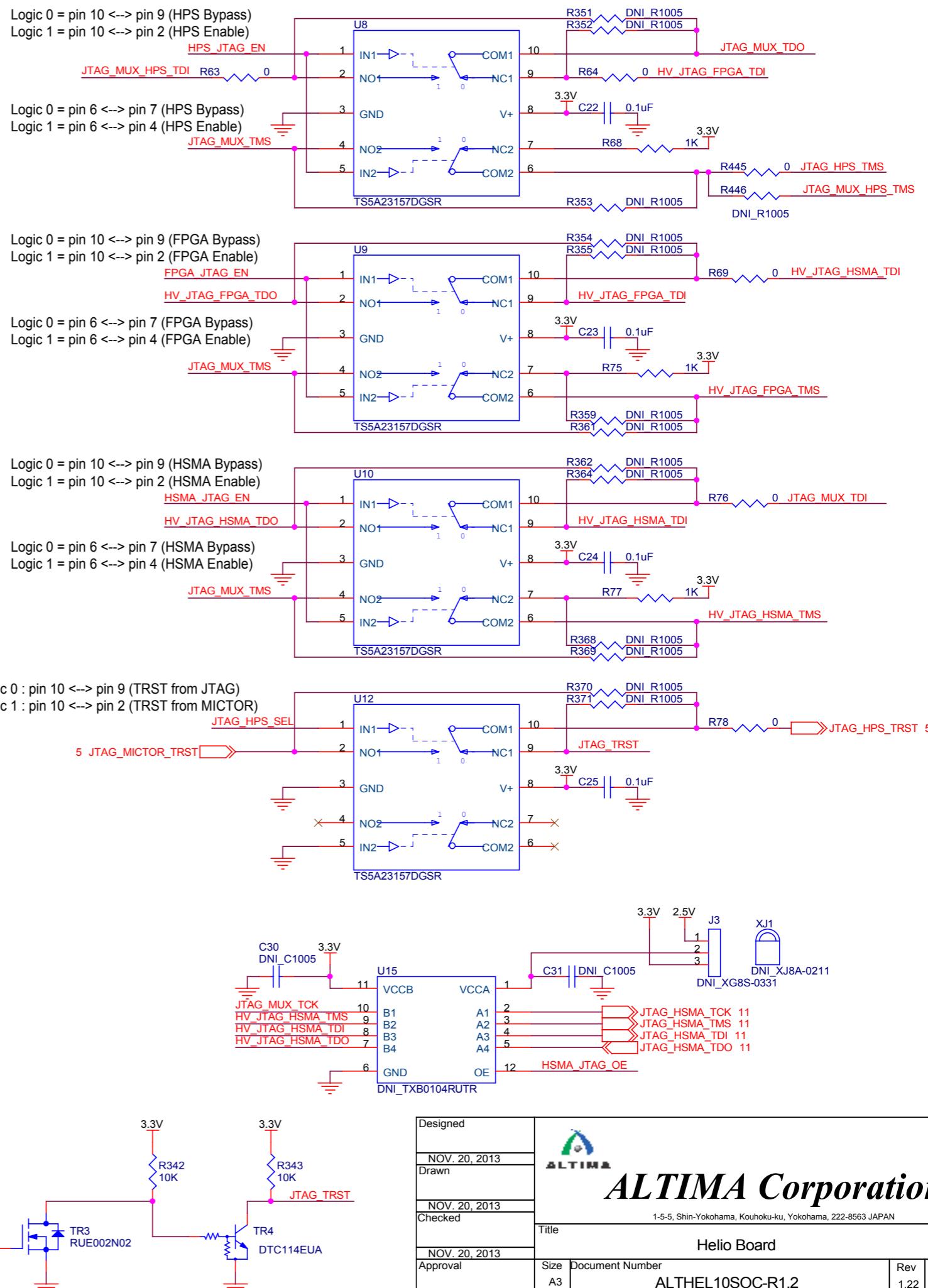
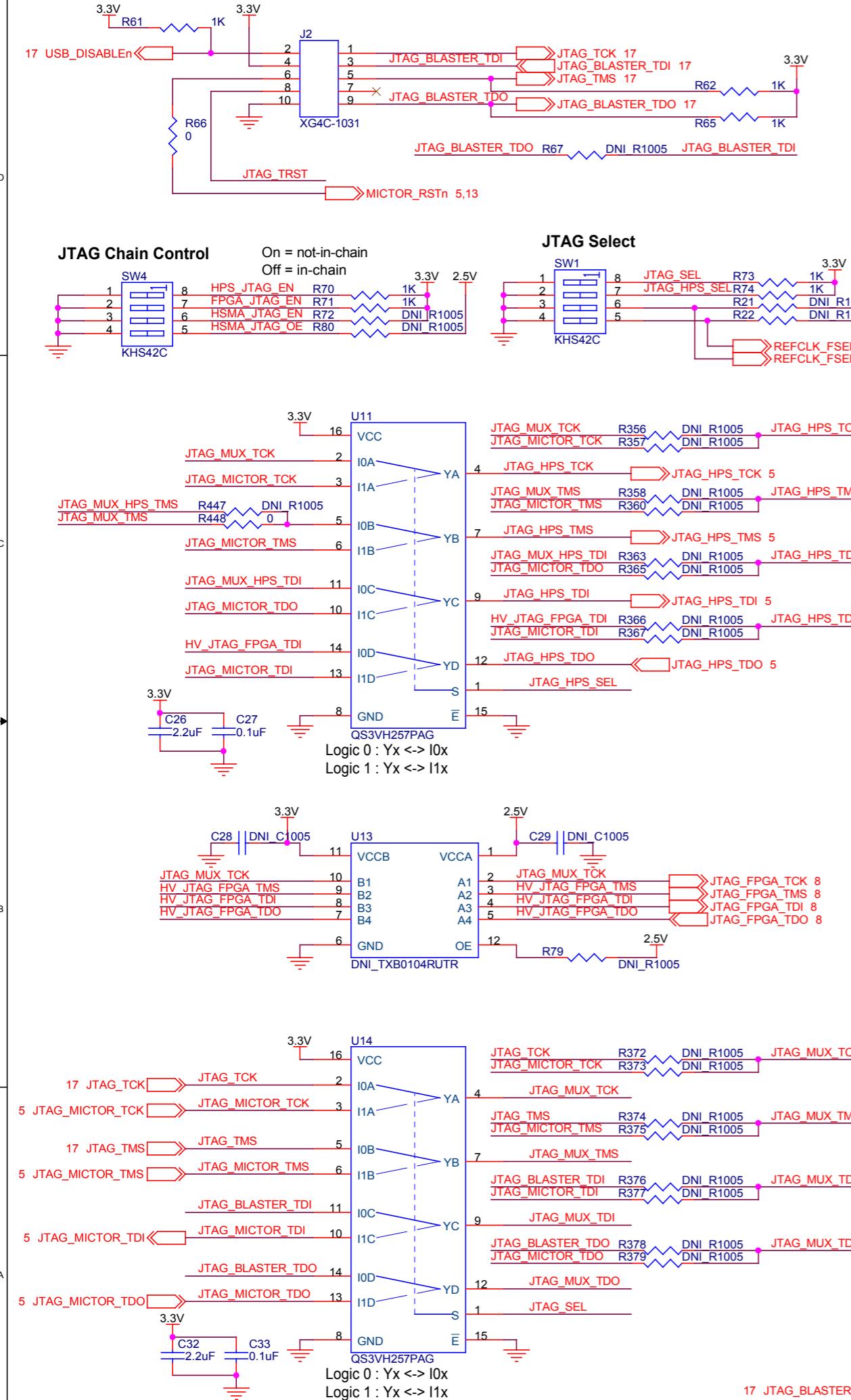
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# Cyclone V SoC Configuration

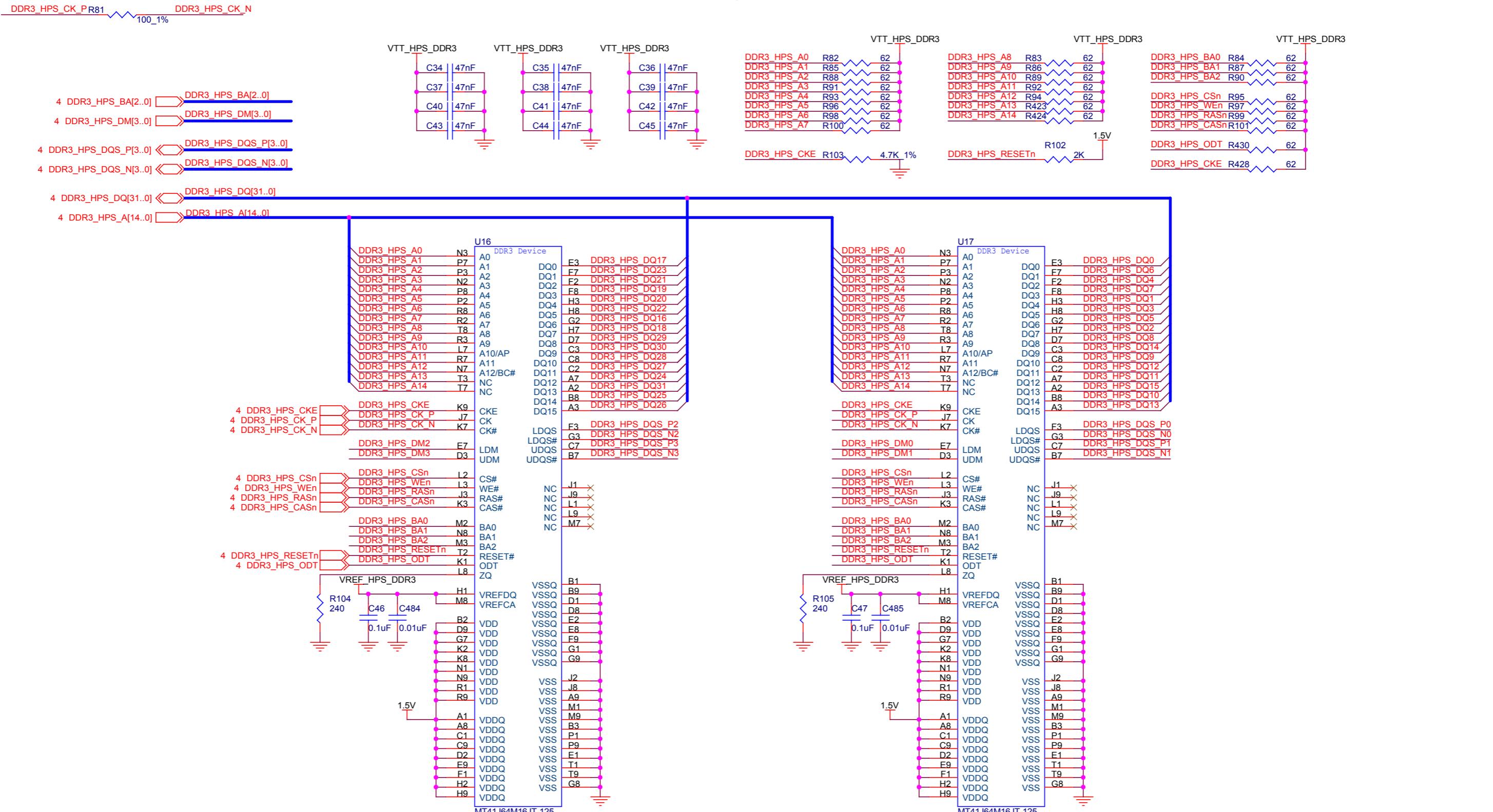


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Approved	Size A3	Document Number ALTHEL10SOC-R1.2	Rev 1.22
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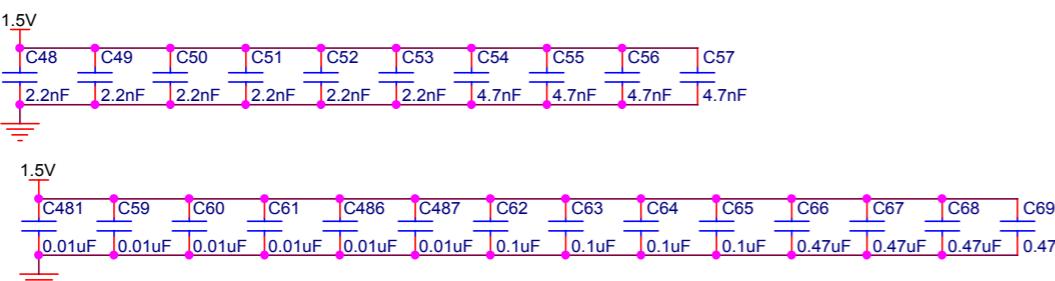
# JTAG



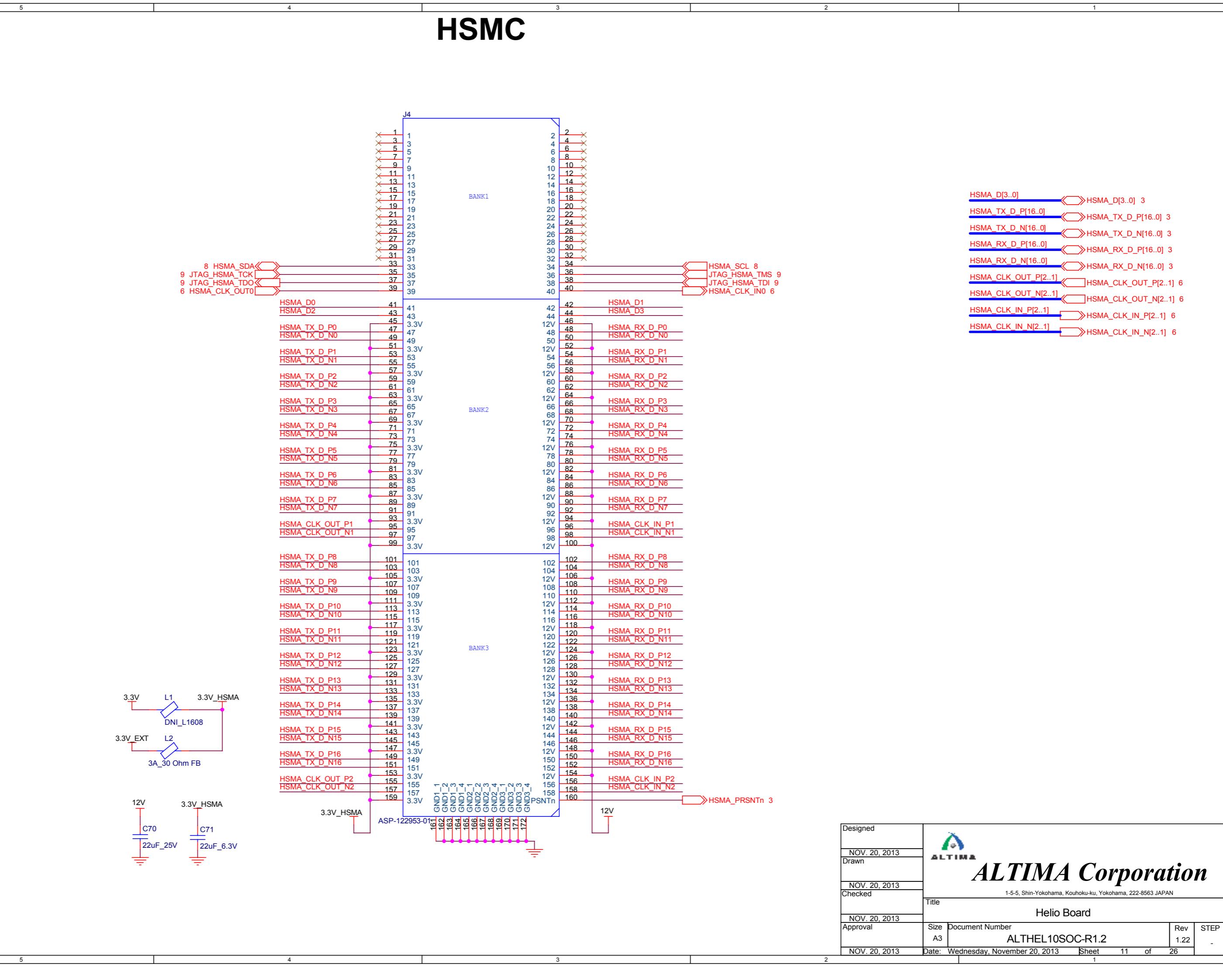
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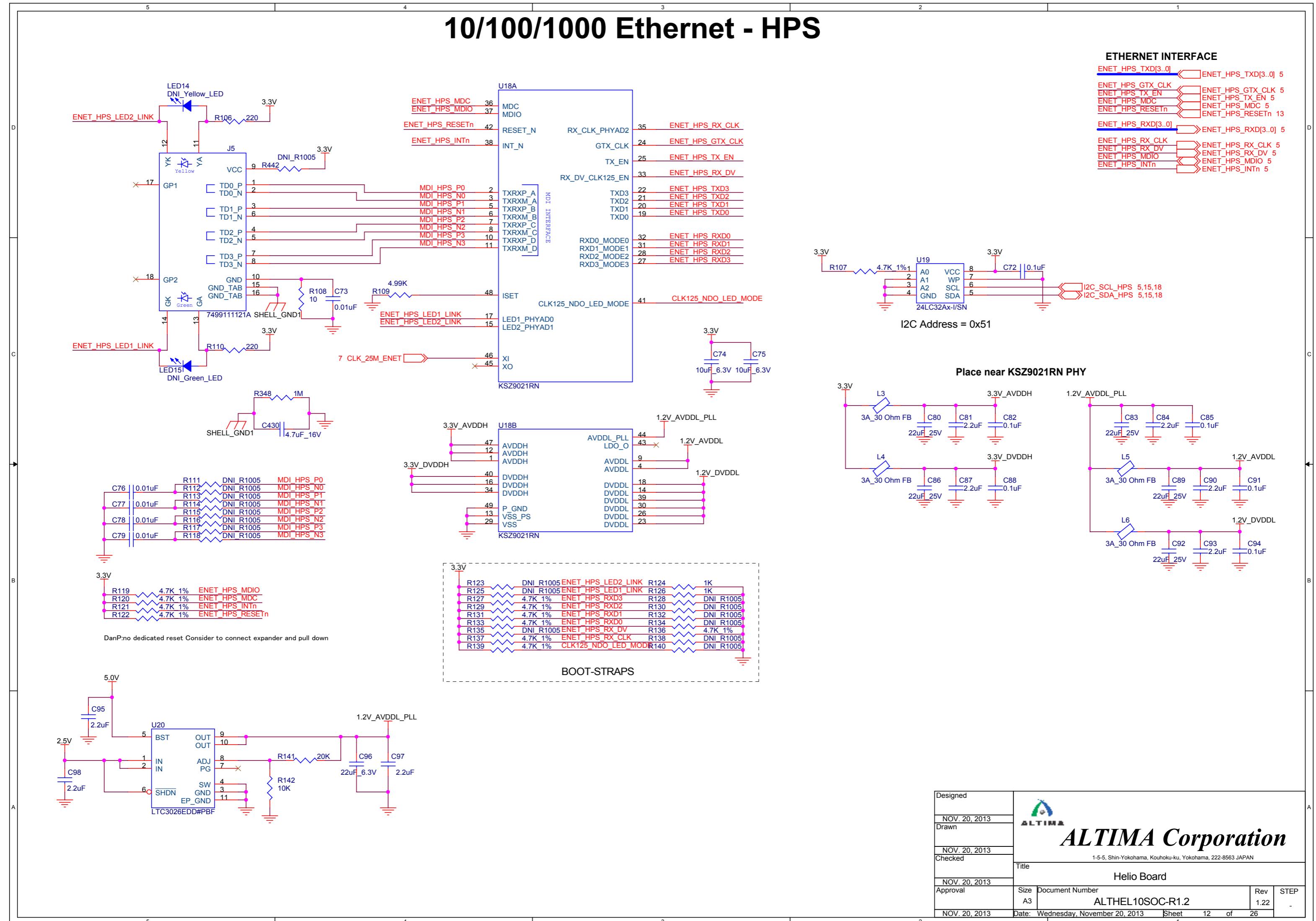
1Gbit : MT41J64M16JT-125  
2Gbit : MT41J128M16JT-125  
4Gbit : MT41J256M16RE-125



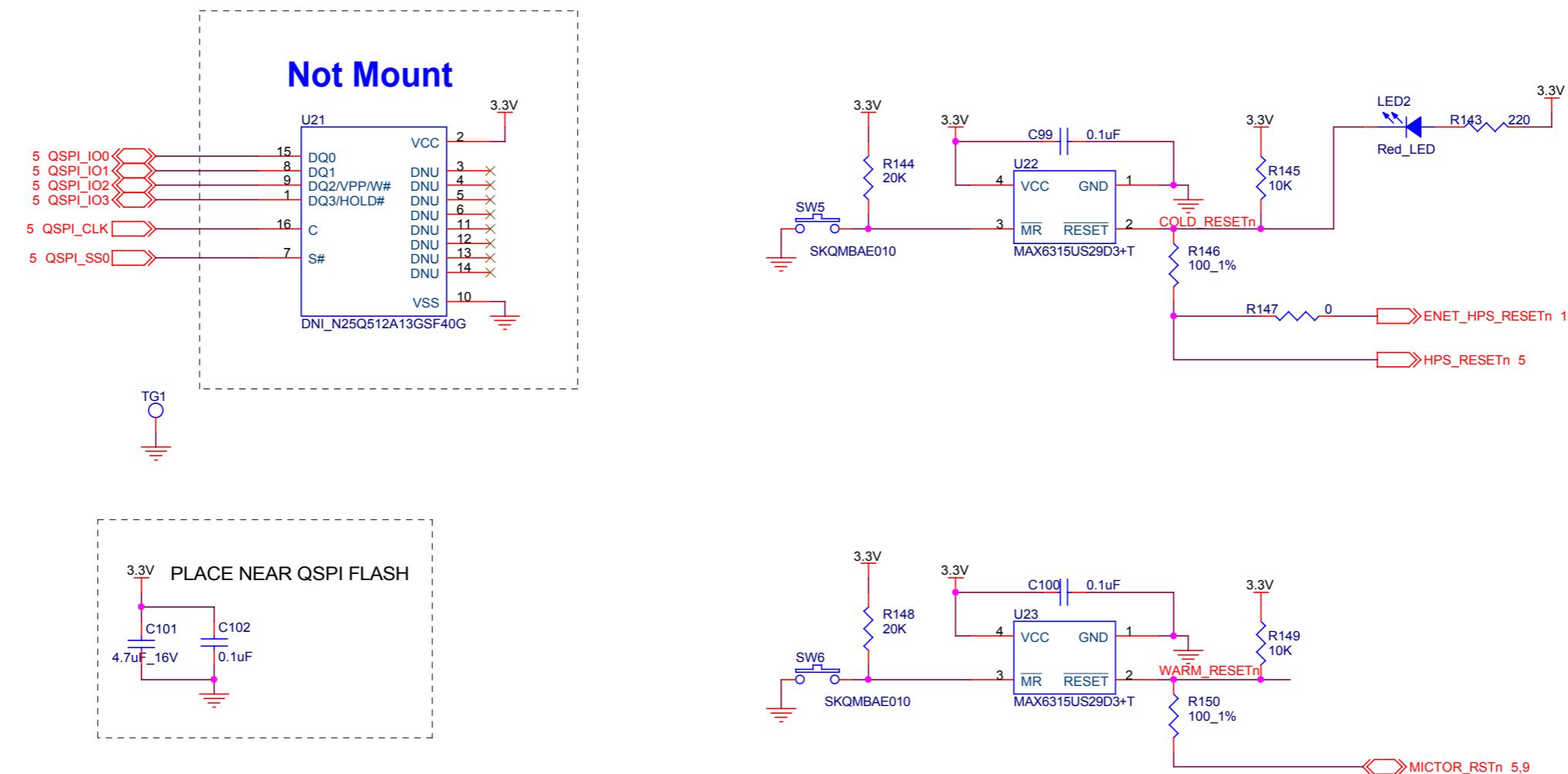
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NOV. 20, 2013			
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A3	ALTHEL10SOC-R1.2		
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# 10/100/1000 Ethernet - HPS

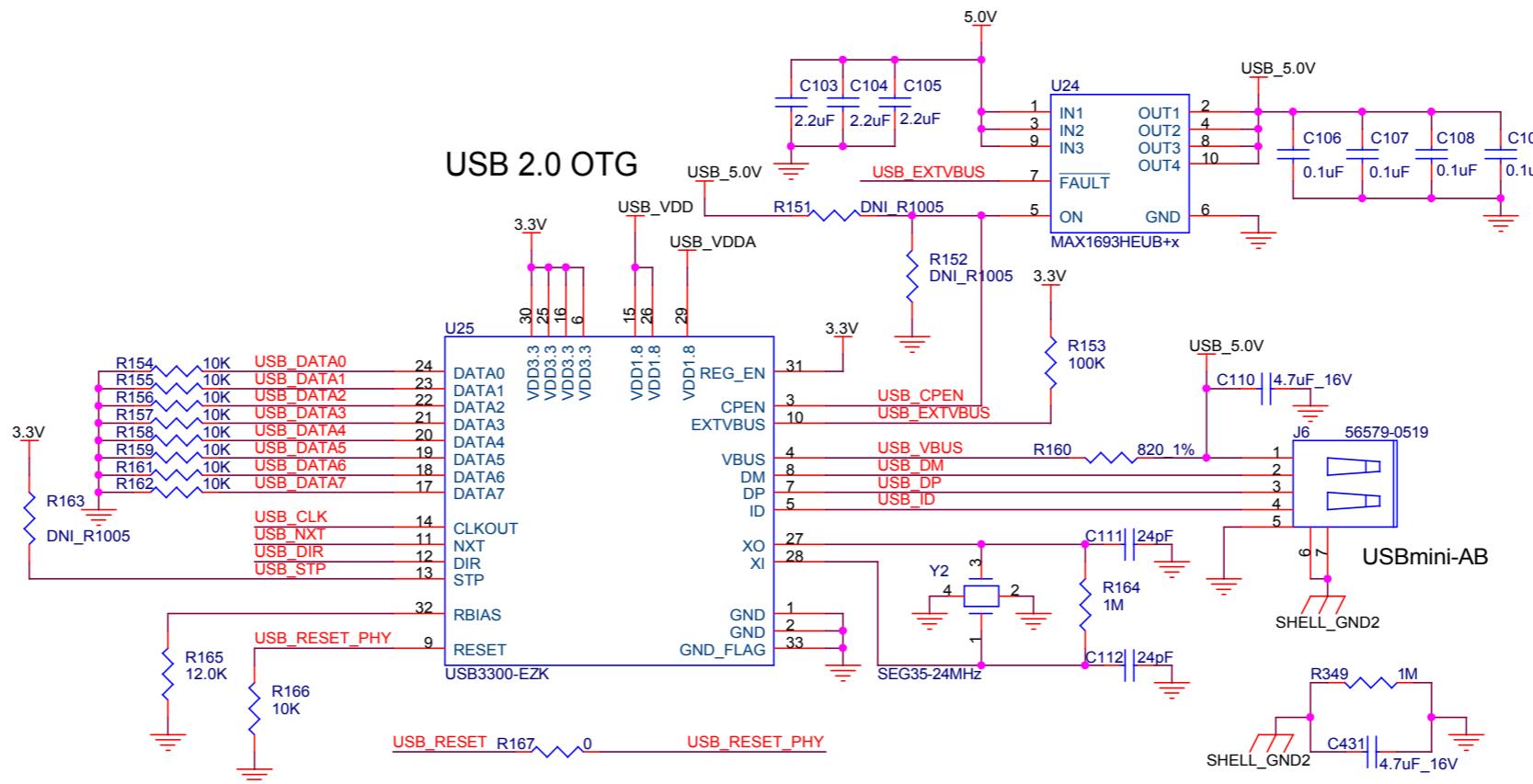


# QSPI Flash & Reset Circuit



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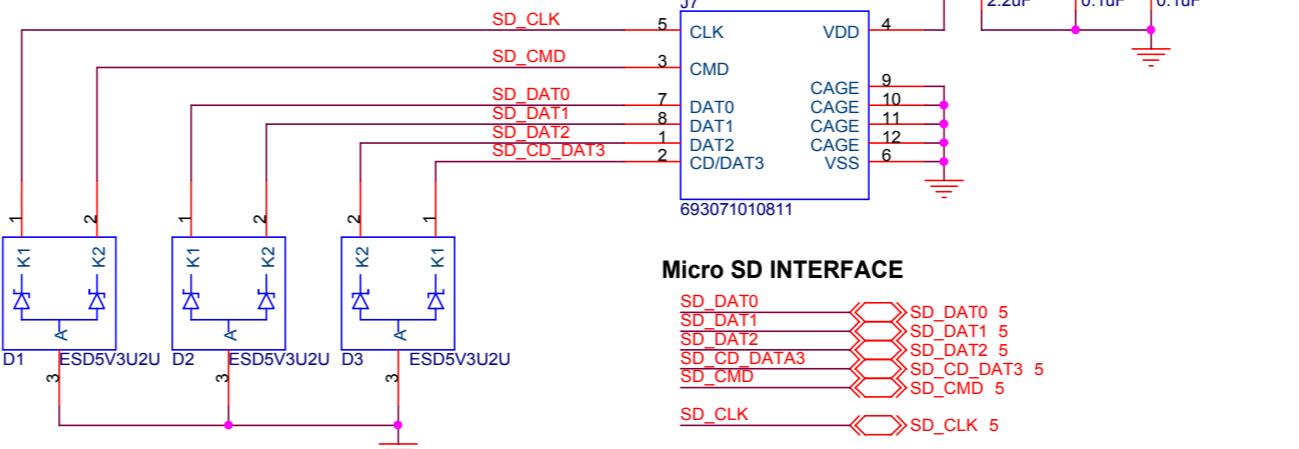
# USB 2.0 OTG, Micro SD Card



## USB INTERFACE

5 USB\_RESET → USB\_RESET  
 5 USB\_CLK → USB\_CLK  
 5 USB\_NXT → USB\_NXT  
 5 USB\_DIR → USB\_DIR  
 5 USB\_STP → USB\_STP  
 5 USB\_DATA[7:0] → USB\_DATA[7:0]

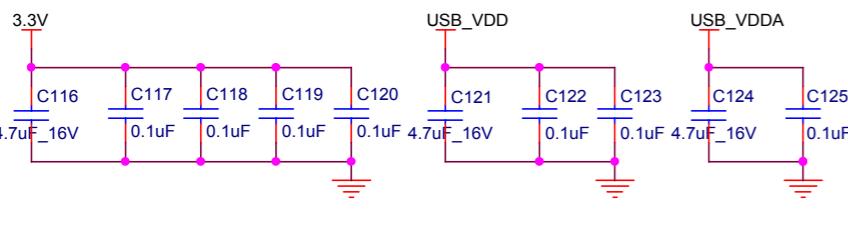
## Micro SD Card



## Micro SD INTERFACE

SD\_DAT0 → SD\_DAT0 5  
 SD\_DAT1 → SD\_DAT1 5  
 SD\_DAT2 → SD\_DAT2 5  
 SD\_CD\_DATA3 → SD\_CD\_DATA3 5  
 SD\_CMD → SD\_CMD 5  
 SD\_CLK → SD\_CLK 5

## PLACE NEAR USB3300



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Title

Helio Board

Size

A3

Document Number

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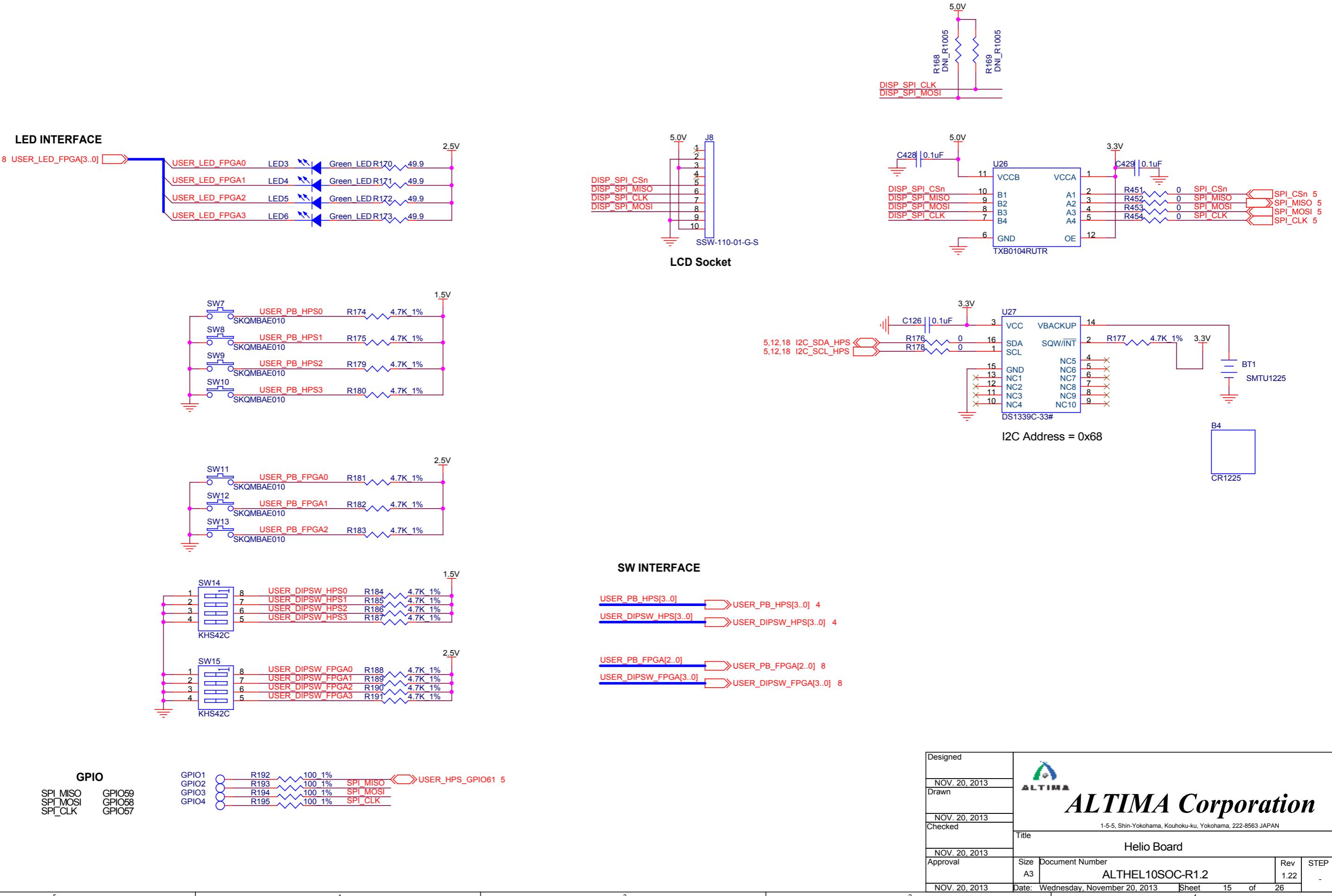
Rev

1.22

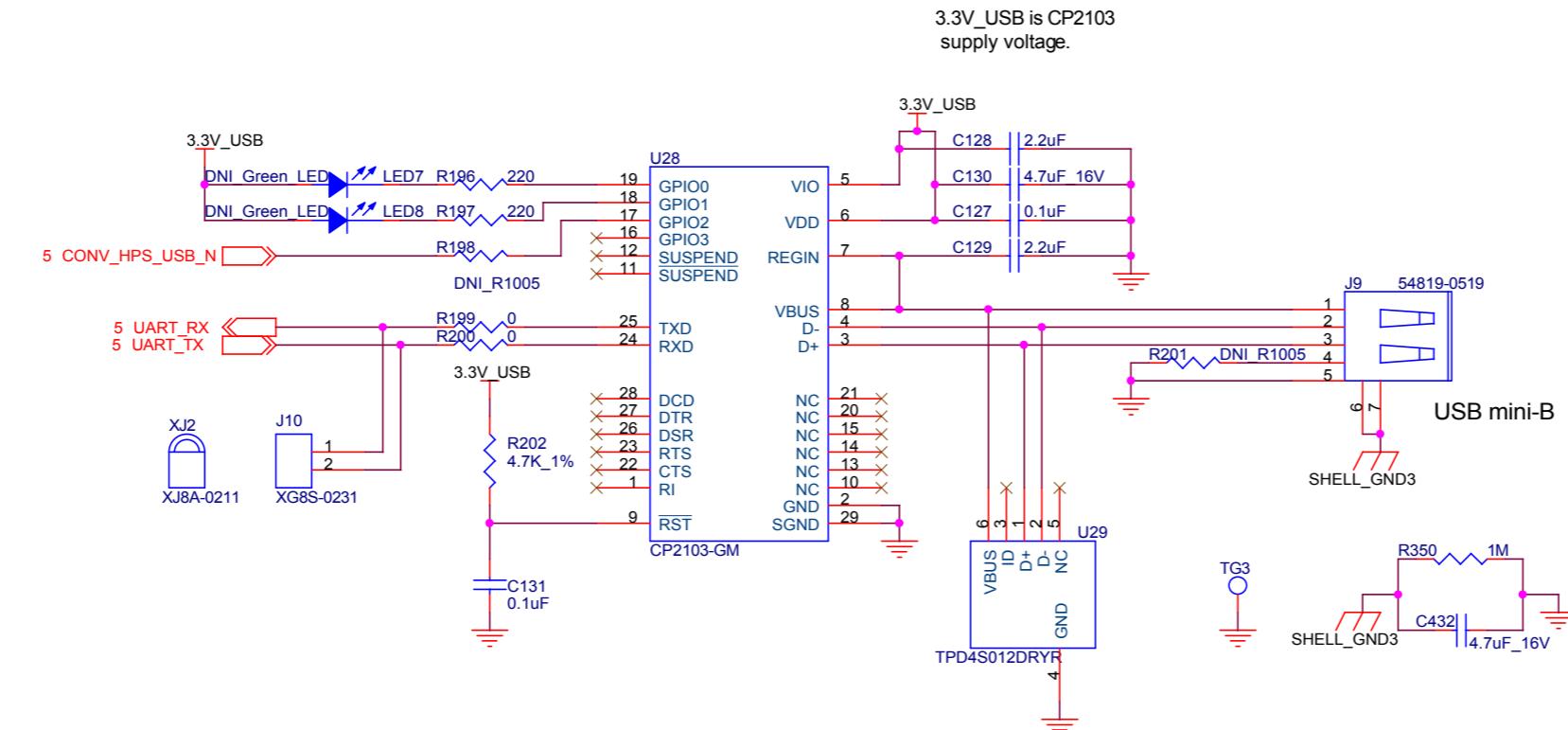
STEP

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# User I/O, RTC

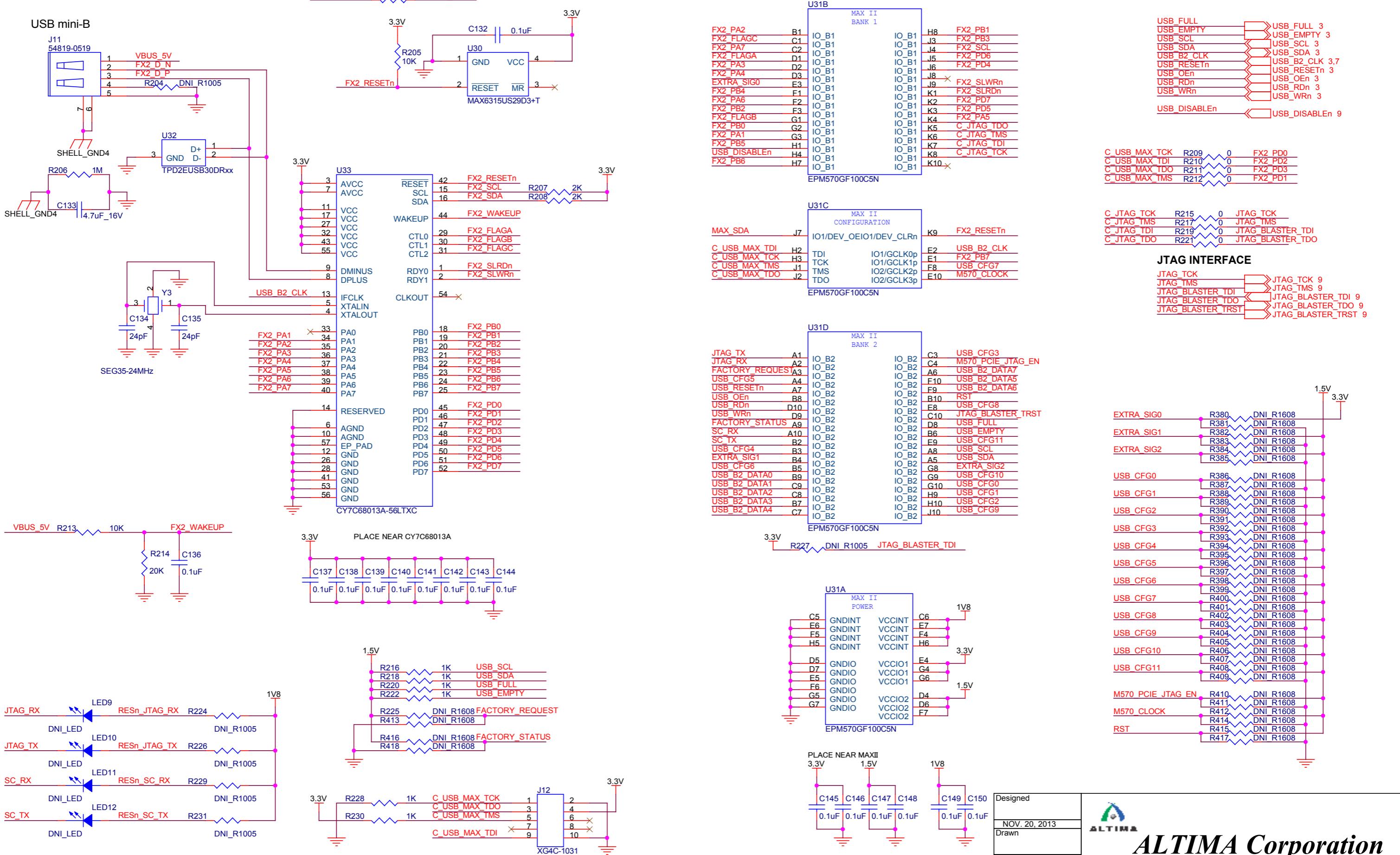


# UART

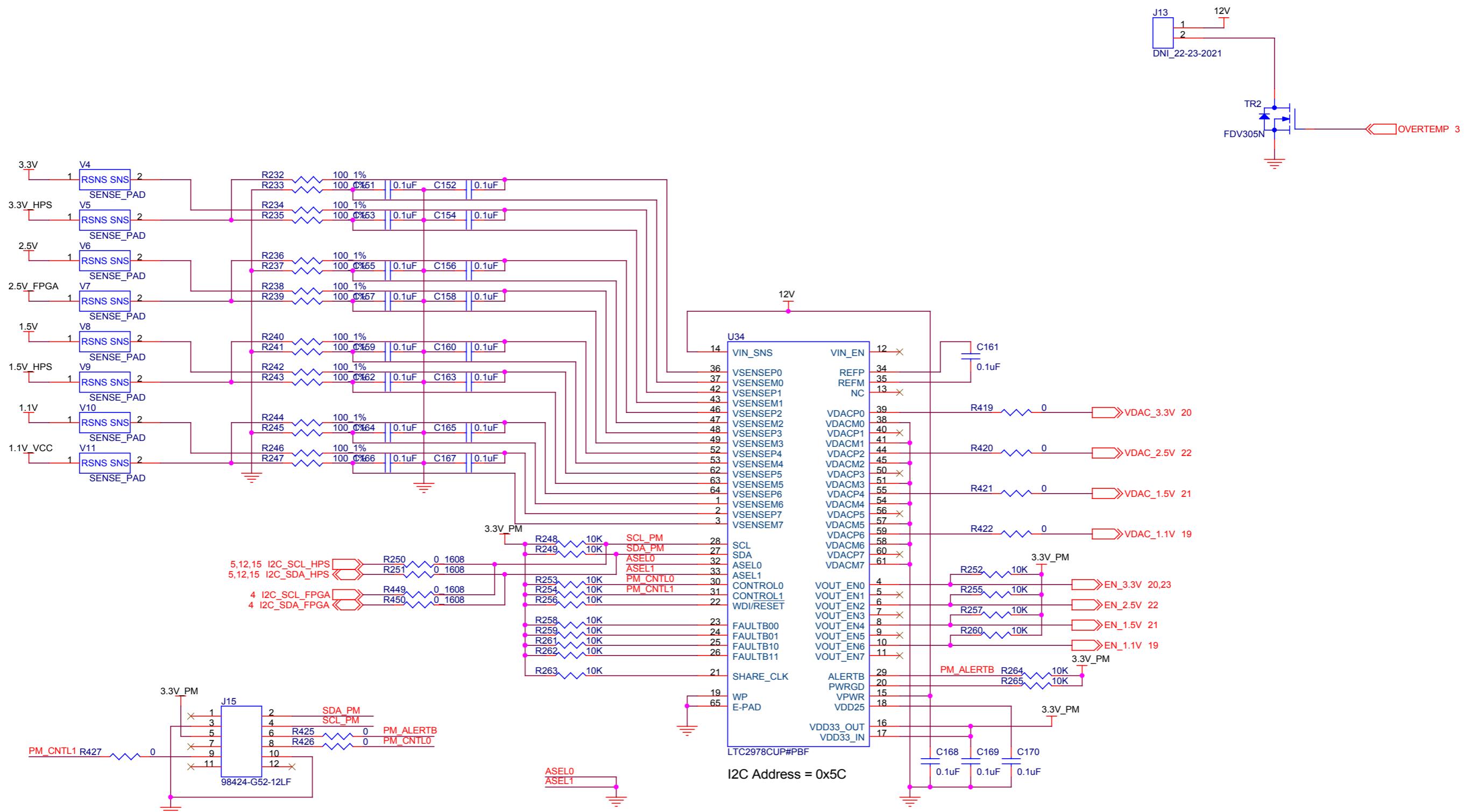


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# On-Board USB BlasterII

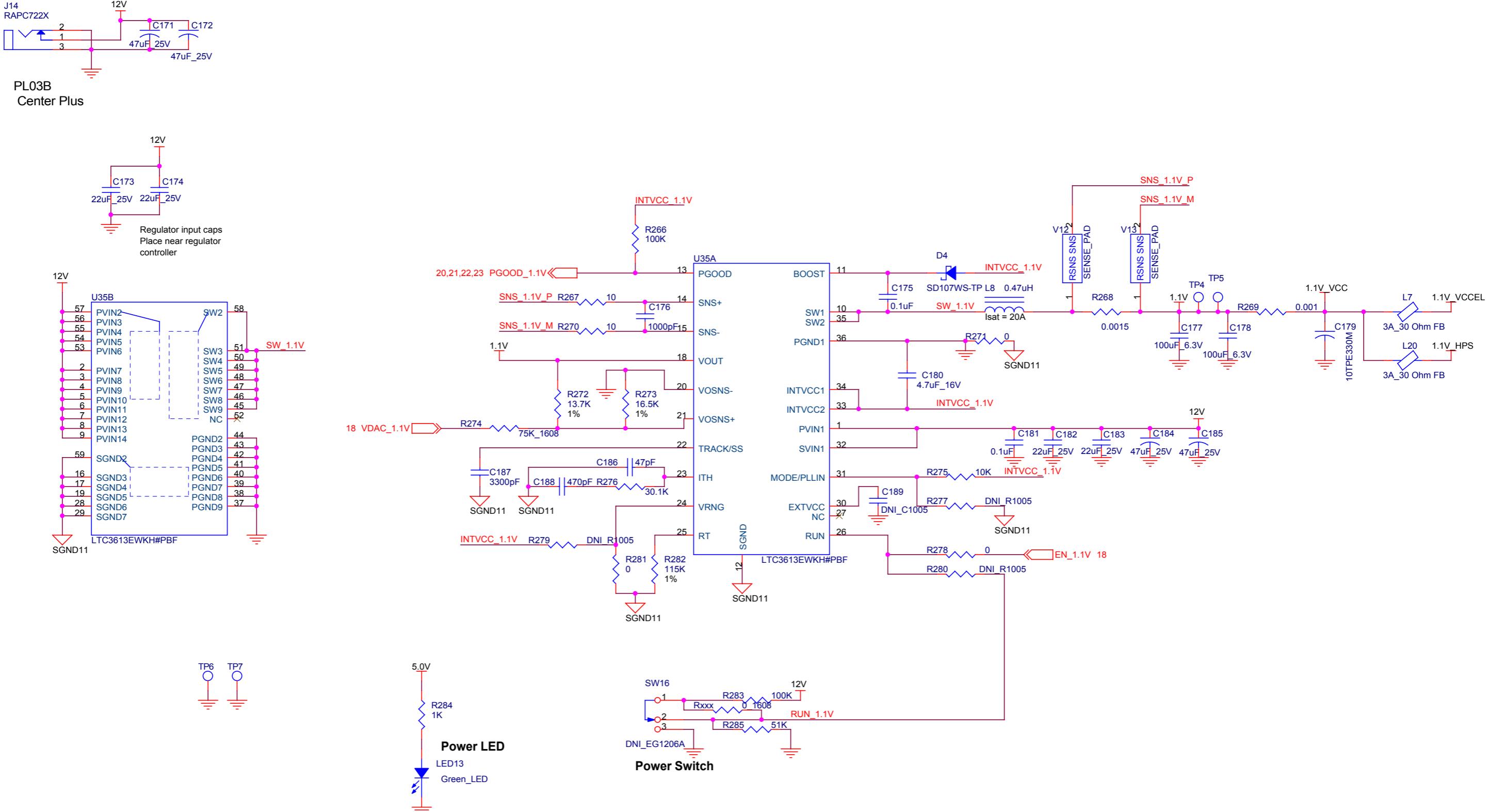


# Power Monitor



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# Power 1 - DC Input, 1.1V



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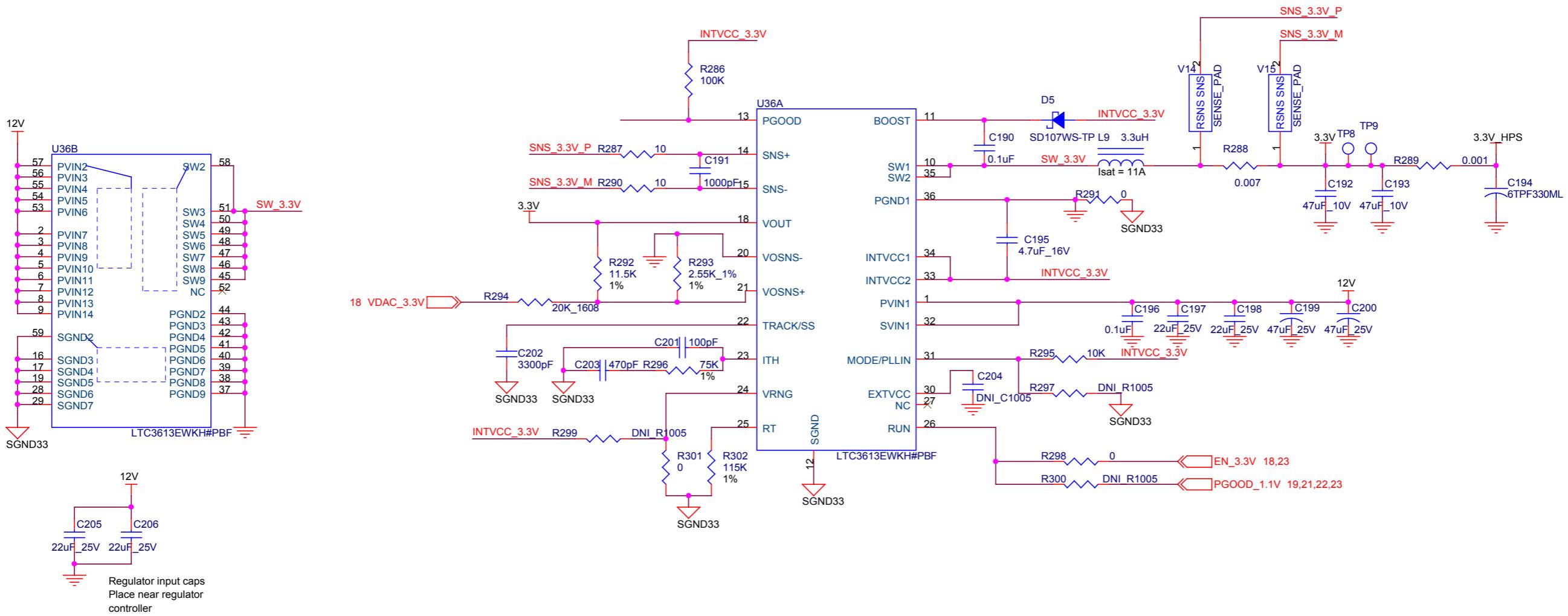
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Helio Board

Size Document Number  
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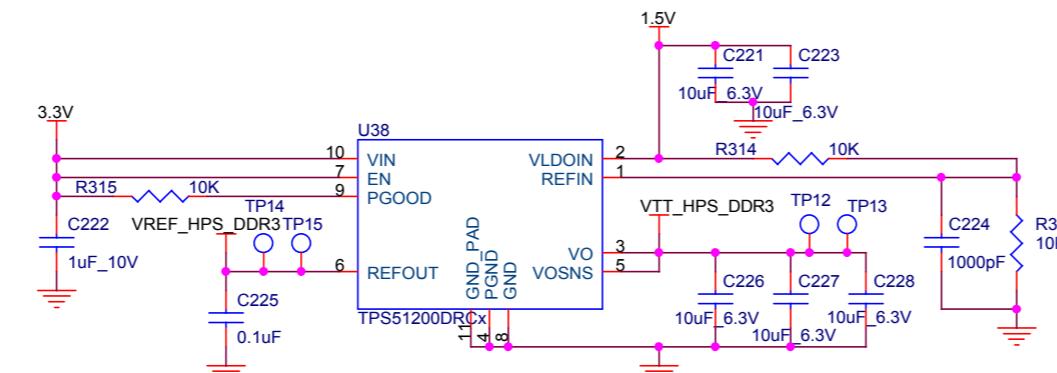
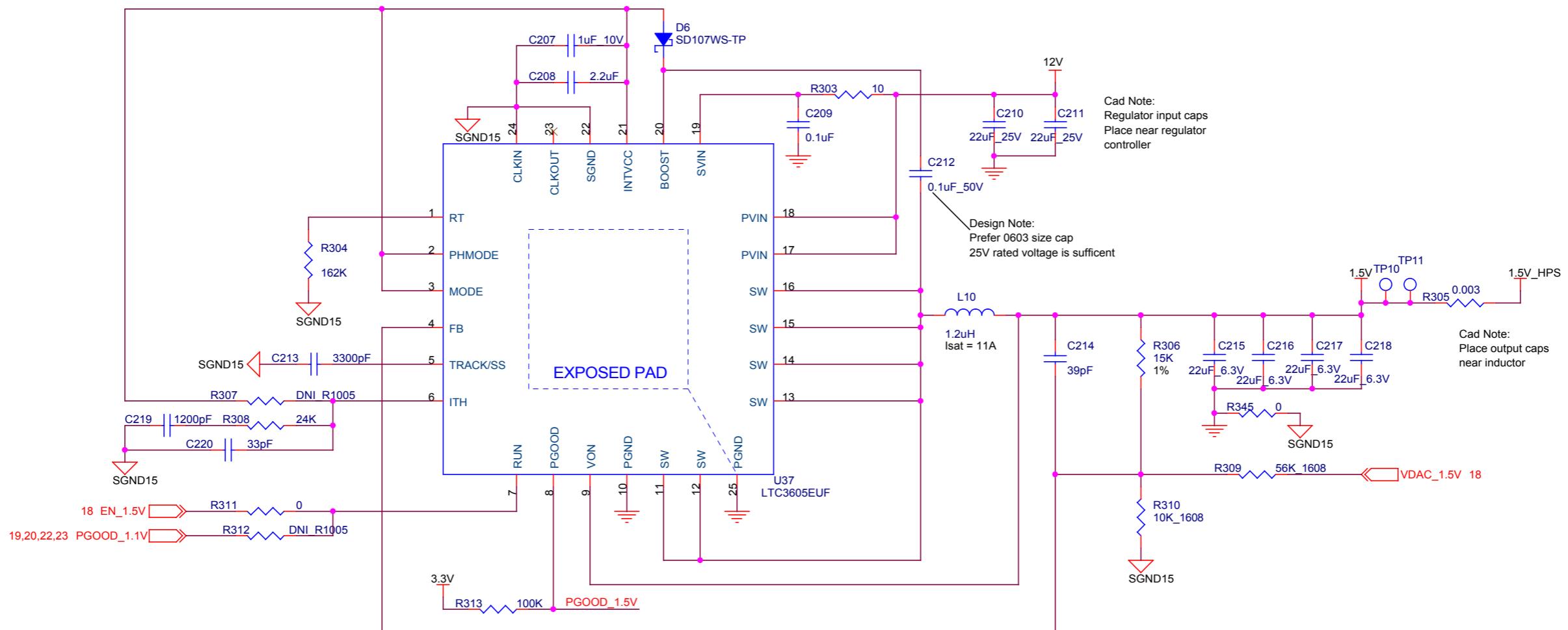
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# Power 2 - 3.3V



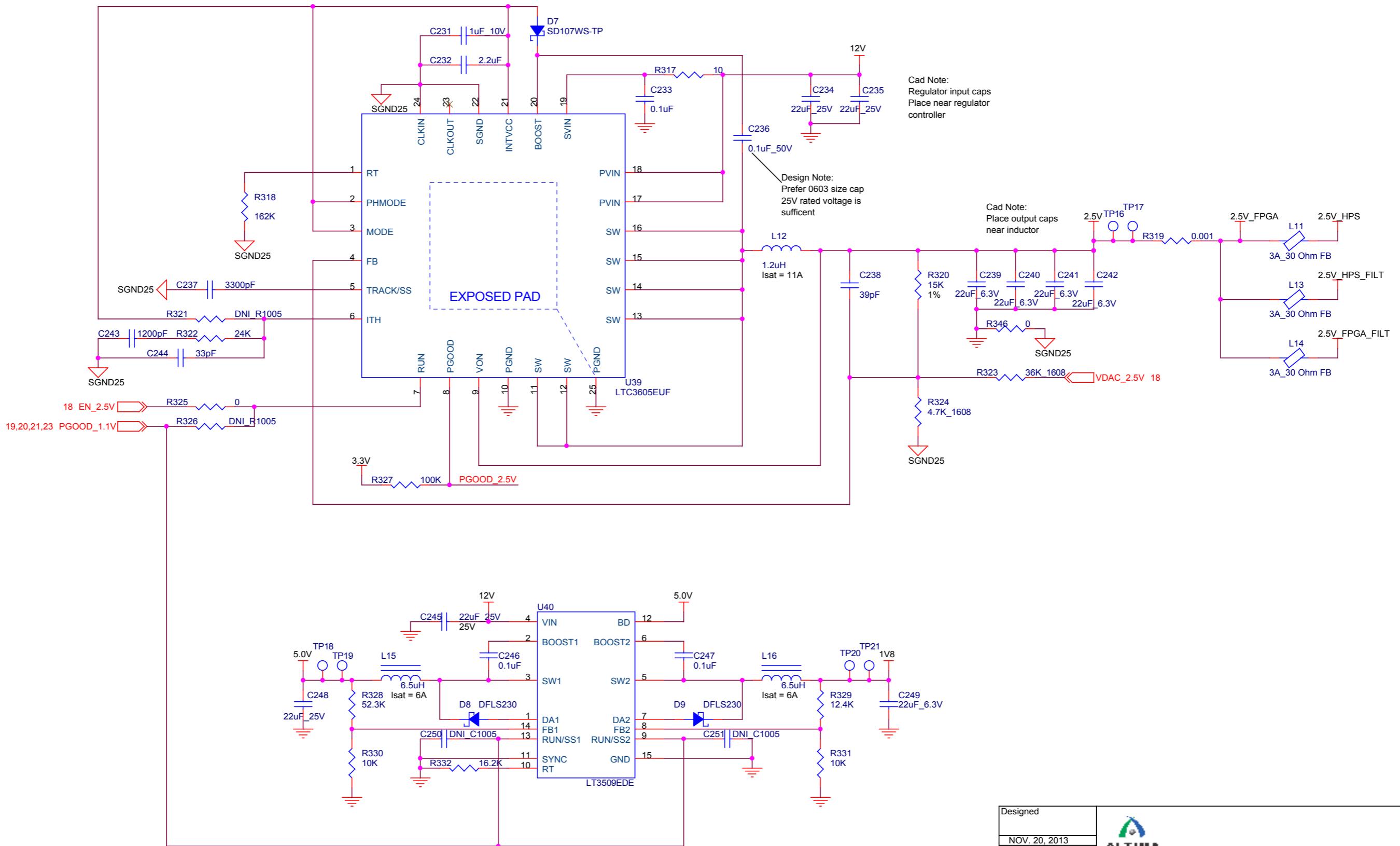
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# Power3 - 1.5V, DDR3 VREF & VTT



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# Power4 - 2.5V, 5V, 1.8V



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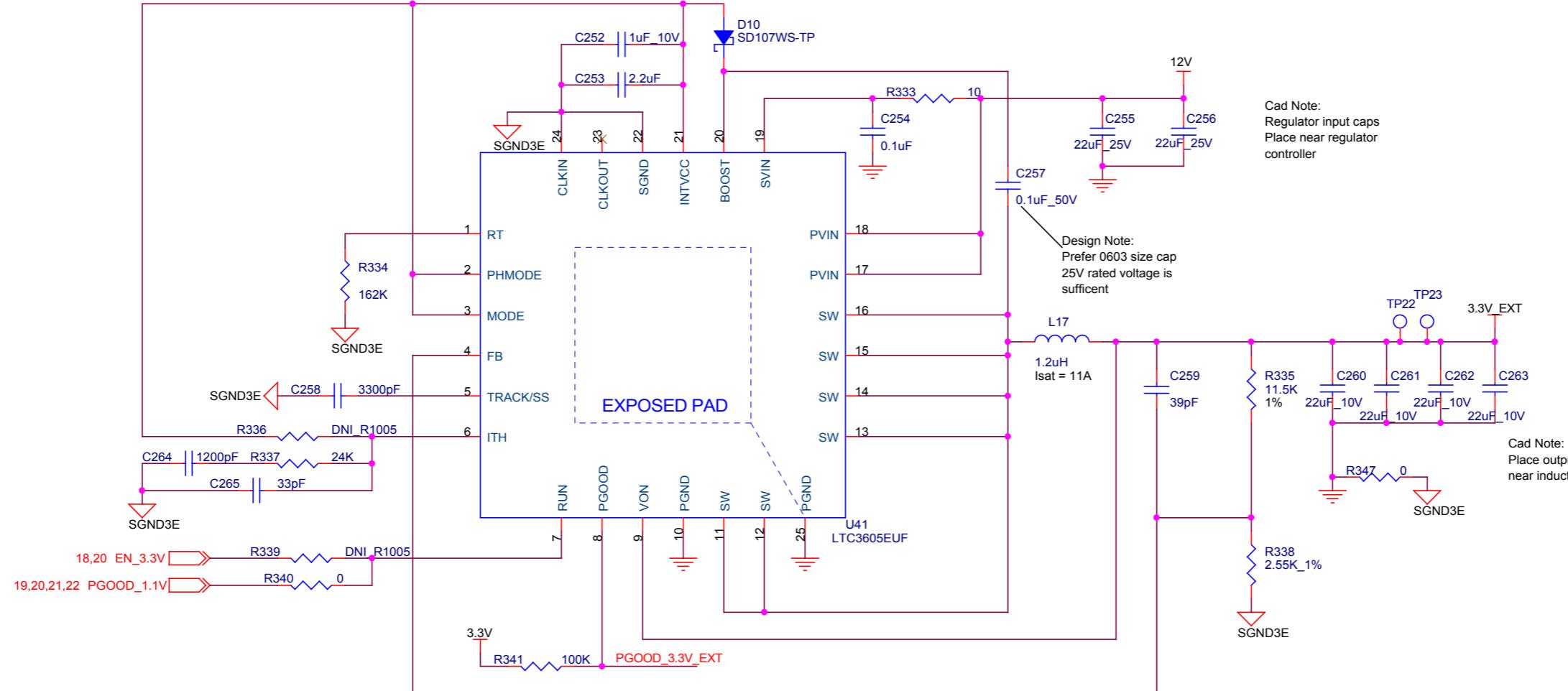
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Title

Helio Board

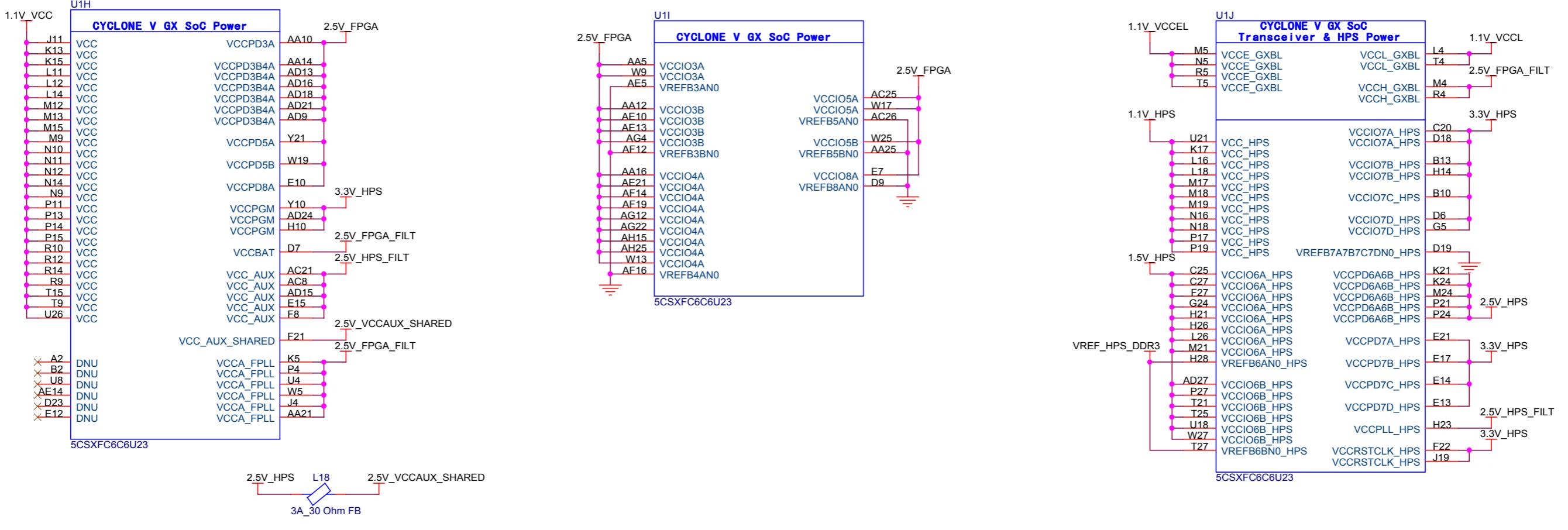
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A3	ALTHEL10SOC-R1.2	1.22	-

# Power5 - 3.3V\_EXT



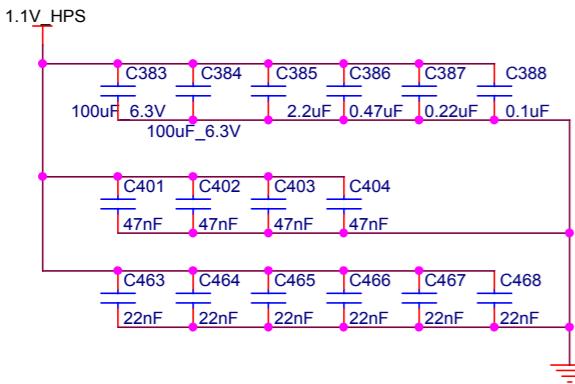
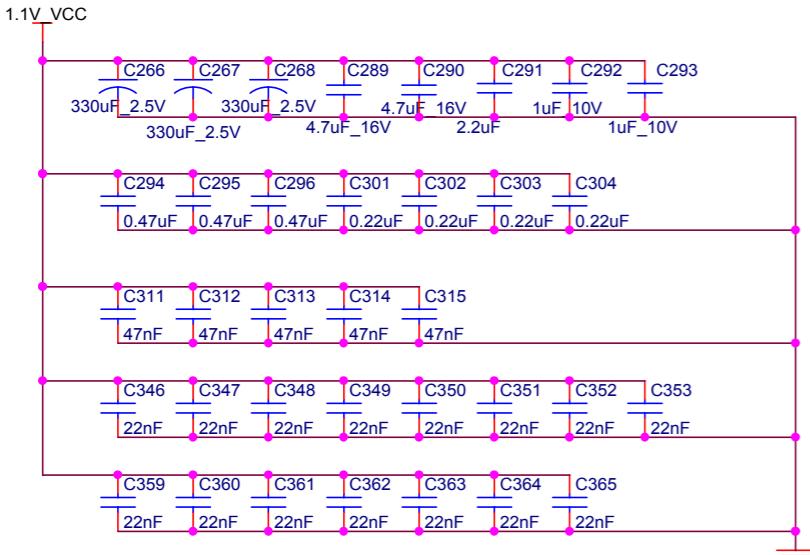
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# Cyclone V SoC Power



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# Decoupling

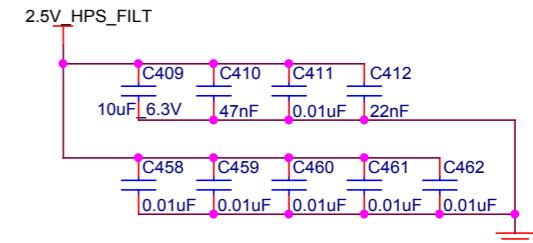
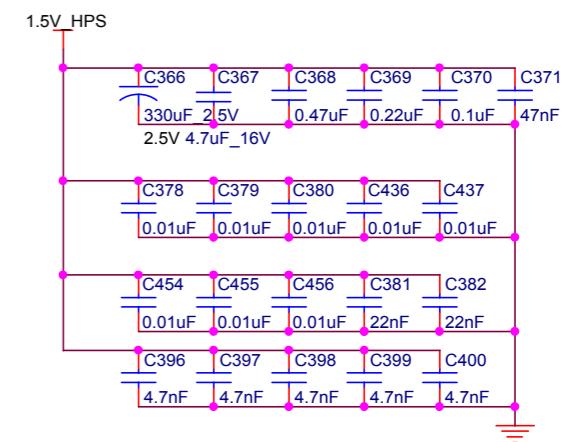
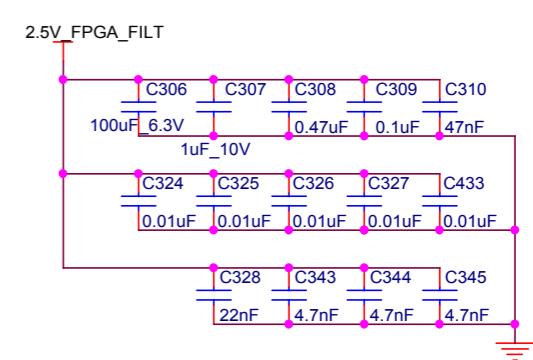
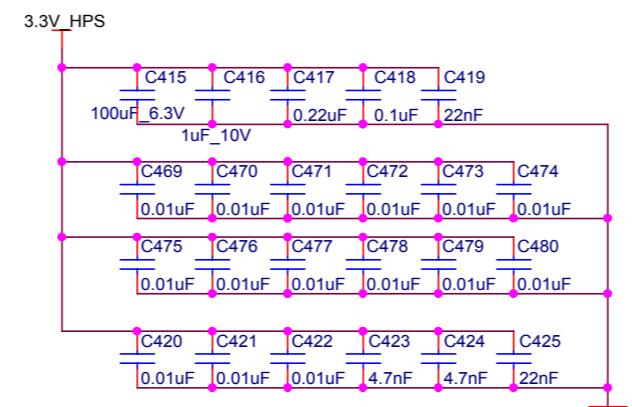
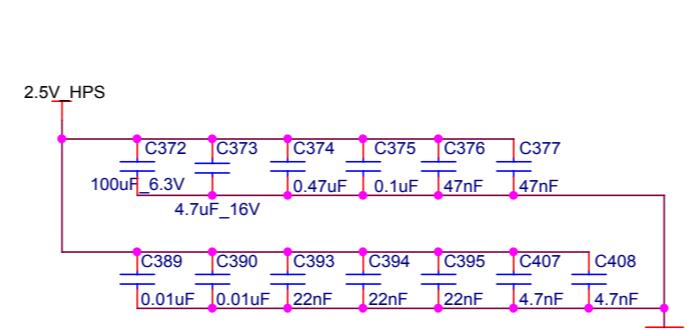
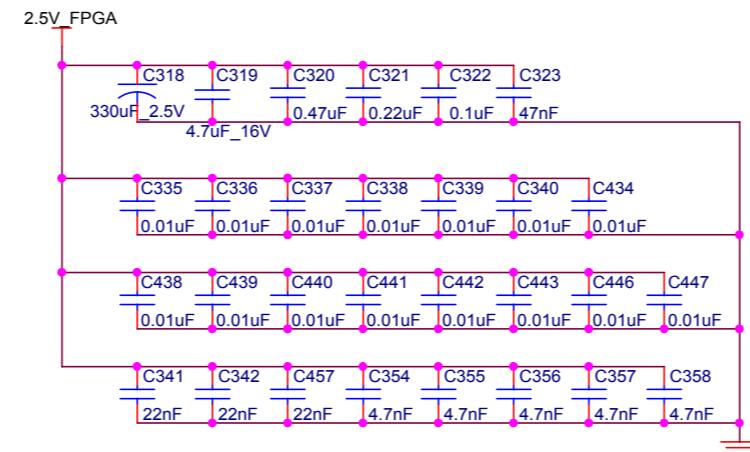
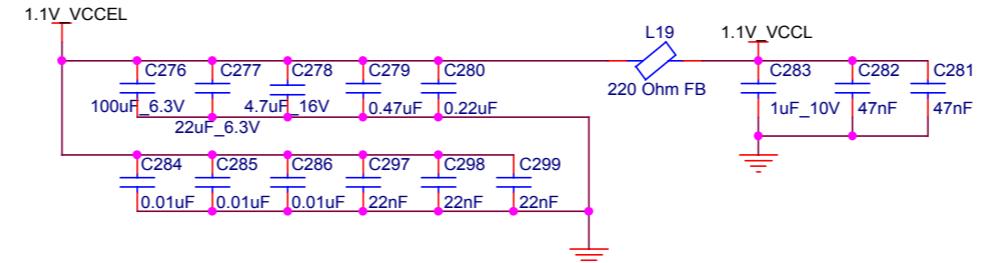


2.5V\_VCCAUX\_SHARED

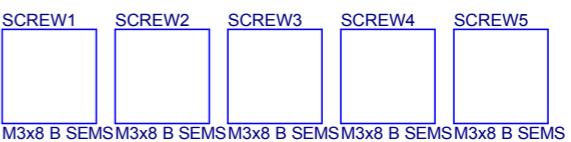
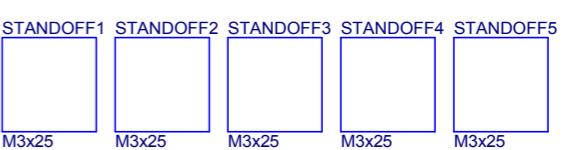
C413, C414, 1uF\_10V, 4.7uF\_16V

VREF\_HPS\_DDR3

C488, 0.01uF



47nF, 0.01uF,  
22nF, 4.7nF caps  
are place near the  
pin of the FPGA



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# History

REV	DATE	PAGES	DESCRIPTION
0.0		All	INITIAL REVISION A RELEASE
0.1	01/23/2013		Add Bypass Cap Add C426-C429 Modify JTAG(TRST) Line Add R344-R343, TR3, TR4, R223 Add I2C Connector Add J15
0.2	01/24/2013		Package change U33 CY7C68013A VBGA56 to QFN56 U15,U13 MAX13042E UCSP12 to TDFN14 Add Component LED14,15 Replace char " " to " " Change Component TP4-TP6
0.3	01/25/2013	Page 25 Page 13 Page 19-23 Page 12,14, 16,17 Page 9 Page 17	Change net 1.5HPS to 1.5V_HPS Add GND net C101, C102 Separate GND Add R345-R347 Separate Shell GND Add R348-R350, C430-C432  Add bypass Circuit Add R351-R379 Add Jumper R Add R380-R418
0.4	01/28/2013	Page 15 Page 15,17 Page 5 Page 3	Change Component BT1 SMTU2032 to SMTU1225, B4 CR2032 to CR1225 Change Component U22,U23 MAX811 to MAX6315 R145,R149,R205 100K to 10K Change net J1-34pin Logic 0 to Logic 1 Change Component R1,R2 10K to 2K
0.5	01/28/2013	Page 22 Page 21 Page 12  Page 5  Page 9 Page 17 Page 18 Page 16	Change Value R324 4.7K_1% to 4.7K_1608 Change Value R310 10K to 10K_1608 Change net Boot Strap Signal GTX_CLK to RX_CLK Change net U20 SHDN Pin Pullup 5.0V to 2.5V Change Boot Sel Change SW2 to J16,J18,J20 Change SW1 to J17,J19 Switch Add SW1 to J17,J19 Change Dipsw Change SW4 KHS62C to KHS42C Move from SW1 Change MAXII setting line Change DNI_R1005 to DNI_R1608 Change R418 1K to 1K_1608 Add 0 ohm Add R419-R422 Change Component Change U28 CP2104 to CP2103
0.6	01/28/2013	Page 12 Page 10	Change Component U12 LTC3026EDD-1 to LTC3026EDD C95 0.1uF to 2.2uF Add DDR3 Address DDR3_HPS_A13, DDR3_HPS_A14 Add R423, R424
0.6a	01/29/2013	Page 7	Change Component X4 4MA to CL20VBC C7,C9,C13,C15,C19 0.1uF to 0.01uF
0.6b	01/29/2013	Page 19 Page 15 Page 25,10	Add Component L20 Change net LED3-LED6 Change Component Cap Size 1005 to 0603
0.6c	01/29/2013	Page 18-24	Change net Remove C229,C230
0.6d	01/29/2013	Page 18	Change connector pin assign Add R445-R447
0.6e	01/30/2013	Page 9 Page 4,10 Page 21-23 Page 7,14,18	Change Component U12,U15 MAX13042 to TXB0104 Add Component R428,R429,R430 Change Component L10,L12,L17 PCMC053T-1R2MN to PCMB053-1R2MS Change x'tal CL 12pF to 24pF
0.6f	01/31/2013	Page 6,11	Add Component R431-R440
0.6g	01/31/2013	Page 8	Change Component TR1 DTC114EUA to RUE002N02 Add R441
0.6h	01/31/2013	Page 6,3 Page 10	Pin Swap HSMC Add Component C481
0.6j	02/01/2013	Page 6,3 Page 12 Page 7	Pin Swap HSMC Change Component R111-R118 49.9 to DNI_1005 Add R442 Add OSC ADD X5,R443,C482,C483,R444
0.6k	02/01/2013	Page 18 Page 10 All Page 14,3	Change net J15.5 NC to 3.3V_PM Change net Swap DDR DQ bus Rename Ref TP4-6 to TG1-3 Pin Swap D1,D2, HSMC
0.6m	02/02/2013	Page 17 Page 9	Change power net Pullup 2.5V to Pullup 3.3V Add 0ohm jumper R445-R448 U11.14 JTAG_FPGA_TDI to HV_JTAG_FPGA_TDI Modify net
0.6n	02/04/2013	Page 9 Page 4,18 Page 5,15 Page 10	Modify net U15.12 connects to SW4.5 Modify net U34.I2C bus connects to FPGA I/O Change net SPI bus connects to LCD module Change net Swap DDR DQ bus
0.6p	02/05/2013	Page 15	Add Component R451-R454
0.6q	02/05/2013	Page 4,10	Change Component R428 10 to 51 Move Page4 to 10
0.6r	02/05/2013	Page 10,4	Change Component DDR Terminal R 51 to 62 Dump R 10 to 22
0.6s	02/06/2013	Page 25 Page 10,25	FPGA Adjust a quantity of bypass cap DDR Adjust a quantity of bypass cap
0.6t	02/07/2013	Page 18-23	Change Component R232-R247, C188, C203, R276, R296, C201, C192, C193, C260-C263, L8, R268, R288
1.0	02/23/2013	Page 14	Change Component R167 DNI to 0 Board Release
1.1	03/04/2013	Page 17 Page 22 Page 9 Page 18	Change Component J12 DNI_XG4C-1031 to XG4C-1031 Change net Connect U40.13, U40.9 to PGOOD_1.1V Do Not Insert Component U13, U15, C28-C31, R79, J3, XJ1, R72, R80 Change Component R449, 450 DNI to 0
1.1a	03/04/2013	Page 19-23 Page 15	Add Component Add Check Land TP6 to TP23 Remove Component B1 to B3

REV	DATE	PAGES	DESCRIPTION
1.1b	03/07/2013	Page 19-23 Page 15 Page 17	Change Value Change CheckLand to TP at even number Reference from TP4 to TP23. Change Value Change TH_GPIO to DNI_TH_GPIO. Rotate Component Rotate Y3 to 90deg.
1.1c	03/08/2013	Page 7	Change Component X5 16MHz to 6MHz
1.1d	03/11/2013	Page 19 Page 20 Page 7	Not Connect U35 52pin Not Connect. Not Connect U36 52pin Not Connect. Fix Component X5 FCXO-03L 6.000MHz
1.1e	03/25/2013	Page 7 Page 9 Page 15 Page 17 Page 18	Not Mount Component X5,R443,R444,C482,C483,Y1,C17,C18 Not Mount Component R21,R22 Not Mount Component R168,R169 Not Mount Component LED9-LED12,R224-R226,R229,R231 Not Mount Component R419-R422
1.2	05/01/2013	Page 1 All	Change block diagram Change Title block
1.21	09/13/2013	Page 18-23	Change Value R419-R422, R278, R280, R298, R300, R311, R312, R325, R326, SW16
1.22	11/20/2013	All	Change/Remove Comment

Designed	 <p><b>ALTIMA Corporation</b> 1-5-5, Shin-Yokohama, Kouhoku-ku, Yokohama, 222-8563 JAPAN</p>		
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