Reference Manual

Mpression Helio Board

Revision 1.4

2015/12/09

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1. For Ensuring Safe Use

Be sure to follow the instructions given in this Manual which are intended to prevent harm to the user and others as well as material damage.

1.1 Legend

Danger	Indicates an imminent hazardous situation which if not avoided will result in death or serious injury.
Warning	Indicates a potentially hazardous situation which if not avoided could result in death or serious injury.
Caution	Indicates a potentially hazardous situation which if not avoided may result in minor or moderate injury or in property damage.

1.2 Cautions

Danger	Make sure to use the AC adapter (included in package) that is specified in this Manual. Using an AC adapter not meeting the specifications described in this Manual will cause the kit to emit heat, explode, or ignite.
Warning	Do not apply strong impacts or blows to the kit. Doing so may cause the kit to emit heat, explode, or ignite, or the equipment in the kit to fail or malfunction. This may also cause fire.
	Do not put the main unit or the AC adapter in cooking appliances such as microwave ovens, or high-pressure containers. Doing so might cause the main unit or AC adapter to emit heat, explode, ignite, or emit smoke, or its parts to break or warp.
	Do not wrap the main unit that is in use with cloth or other materials that are likely to allow heat to build up inside the wrapping. This will cause heat to build up inside the wrapping which may cause the main unit to ignite or malfunction.
	When disposing of the main unit, do not dispose of it along with general household waste. Throwing the main unit into fire may cause it to explode. Dispose of the main unit following the laws, regulations, and ordinances governing waste disposal. Do not use the kit in places subject to extremely high or low temperatures or severe temperature changes. Doing so may cause the kit to fail or to malfunction. Always be sure to use the kit in a temperatures ranging from 5°C to 35°C and a humidity range of 0% to 85%.

Warning (Continued from previous page)	Do not pull the power supply cable with excessive force or place heavy items on it. Do not damage, break, bundle, or tamper with the power supply cable. Damaged parts of the power supply cable might cause a short circuit resulting in fire or accidents involving electrical shock.
	Do not unplug the power plug with wet or moist hands. This might cause injuries or equipment malfunctions or failures due to electrical shock.
	Plug the power plug securely into the outlet. If the power plug is not securely plugged into the outlet, it may cause accidents involving electrical shock or fire due to heat emitted.
	Do not connect many electrical cords to a single socket or connect an AC adapter to an outlet that is not rated for the specified voltage. Failing to do so may cause the equipment to malfunction or fail, or lead to accidents involving electrical shock or fire due to heat emitted.
	Periodically remove any dust accumulated on the power plug and around the outlet (socket). Do not use a power plug with dust accumulated on it because doing so will lead to insulation failure due to moisture which may lead to fire. Remove any dust on the power plug and around the outlet with dried cloth.
	Do not place any containers such as cups or vases filled with water or other liquid on this Board. If this Board is exposed to water or other liquids it may cause the Board to malfunction or lead to accidents involving electrical shock. If you spilled water or other liquid on this Board, immediately stop using the Board, turn off the power, and unplug the power plug. If you have any requests for repairs or technical consultation, please contact the Manufacturer.
Caution	Do not place the kit on unstable places such as shaky stands or tilted locations. Doing so may cause injuries or cause this Board to malfunction if the Board should fall.
	Do not attempt to use or leave the kit in places subject to strong direct sunlight or other places subject to high temperatures such as in cars in hot weather. Doing so might cause the kit to emit heat, break, ignite, run out of control, warp, or malfunction. Also, some parts of the equipment might emit heat causing burn injuries.
	Unplug the power supply cable when carrying out maintenance of devices in which the main unit is embedded. Failure to do so may lead to accidents involving electrical shock.
	Do not place this Board in locations where excessive force is applied to the Board. Failure to do so may cause the PC board to warp, leading to breakage of the PC board, missing parts or malfunctioning parts.
Caution (Continued from previous page)	When using the kit together with expansion boards or other peripheral devices, be sure to carefully read each of their manuals and to use them correctly. Manufacturer does not guarantee the operation of specific expansion boards or peripheral devices when used in conjunction with this Board unless they are specifically mentioned in this Manual or their successful operation with this

	Board has been confirmed in separate documents.
	Be sure to turn off the power switch when moving this Board to connect to other devices. Failure to do so may cause this Board to fail or lead to accidents involving electrical shock.
	Do not clean this Board by using a rag containing chemicals such as benzine or thinner. Failure to do so will likely to cause this Board to deteriorate. When using a chemical cloth be sure to comply with any directions or warnings.
	Do not immediately turn on the power if you find that water or moisture had condensed onto the main unit after removing the board from the package. Condensation might occur on this Board when taking it out of the box, if the board is cool yet the room temperature is warm. Do not apply power to the Board while water or moisture has condensed on it because the moisture may cause the Board to break or may shorten the service life of the parts. When you first take this Board out of the box be sure to leave it at room temperature for a while before using it. If condensation or moisture has occurred on this Board, first wait for the moisture to fully evaporate before installing or connecting the Board to other devices.
	Do not disassemble, dismantle, modify, alter, or recycle parts unless they are clearly described as customizable in this Manual. Although this kit is customizable, if parts not specified in this Manual as customizable are modified in any way, then the overall product operation cannot be guaranteed. Please consult with Manufacturer beforehand if you wish to customize or modify any parts that are not described in this Manual as customizable.

1.3 Manufacturer Information

The Manufacturer of this product is:

Macnica, Inc. | Strategic Technology Group
Mpression
1-6-3 Shin-Yokohama, Kouhoku-ku, Yokohama, 222-8561 Japan
http://www.m-pression.com
Please contact through web site.

2. Unboxing

Package Components

This product consists of the following board and peripherals. Please make sure all components listed below are included.

Table 2-1-1. Packing list

Customer letter	
The Helio board	
microSD card	
USB Standard-A to Mini-B plug cable	
AC adaptor (Output 12V/3.8A)	
This Reference Manual	Download these files from Web site described in the Customer letter.
The Helio board circuit diagram	
FPGA sample design	

If there is any question or doubt about the packaged product, contact your local distributor.

3. The Helio Board Hardware Descriptions

3.1 Overview

This document describes the hardware features of the Helio board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

Main CORE of the Helio board is Altera® Cyclone® V SoC. Altera Cyclone V SoC include the Hard Processor System (HPS) with integrated ARM® Cortex™-A9MPCore processor.

One High-speed Mezzanine Card (HSMC) connector is available to add additional functionalities via a variety of HSMCs available from various partners.

For more information on the following topics, refer to the respective documents:

- As for Cyclone V device family, refer to the Cyclone V Device Handbook.
- For HSMC Specification, refer to the High Speed Mezzanine Card (HSMC) Specification.

3.2 Key Components

The Helio board features the following key component blocks:
Key components are listed in Table 3-2-1.

Table 3-2-1. Key components

	Supplier	Function Name	Part number
CPU	Altera	SoC with FPGA	5CSXFC6C6U23C8NES(*1) 5CSXFC5C6U23C7N(*2)
Configuration ROM	Altera	Configuration device	EPCQ256SI16N
CPLD	Altera	On-board USB-Blaster® II	EPM570GF100C5N
ROM	Microchip	EEPROM	24LC32A
RAM	Micron	DDR3-SDRAM	MT41J256M16RE
Ethernet	Micrel	Gigabit Ethernet PHY	KSZ9021RN
USB	SMSC(Microchip)	OTG USB PHY	USB3300-EZK
	Cypress	USB PHY for USB-Blaster II	CY7C68013A-56BAXC
Real Time Clock	MAXIM	I2C Real time clock	DS1339C-33#
UART	Silicon Labs	USB to UART bridge	CP2103GM
Connector	TE Connectivity	Mictor for HPS	2-5767004-2
	Samtec	HSMC	ASP-122953-01

Note: *1) 5CSXFC6C6U23C8NES was mounted in the Helio board Rev1.3 or earlier.
*2) 5CSXFC5C6U23C7N is mounted in the Helio board Rev1.4 or later.

3.3 Block Diagram

Figure 3-3-1 shows a block diagram of the Helio board.

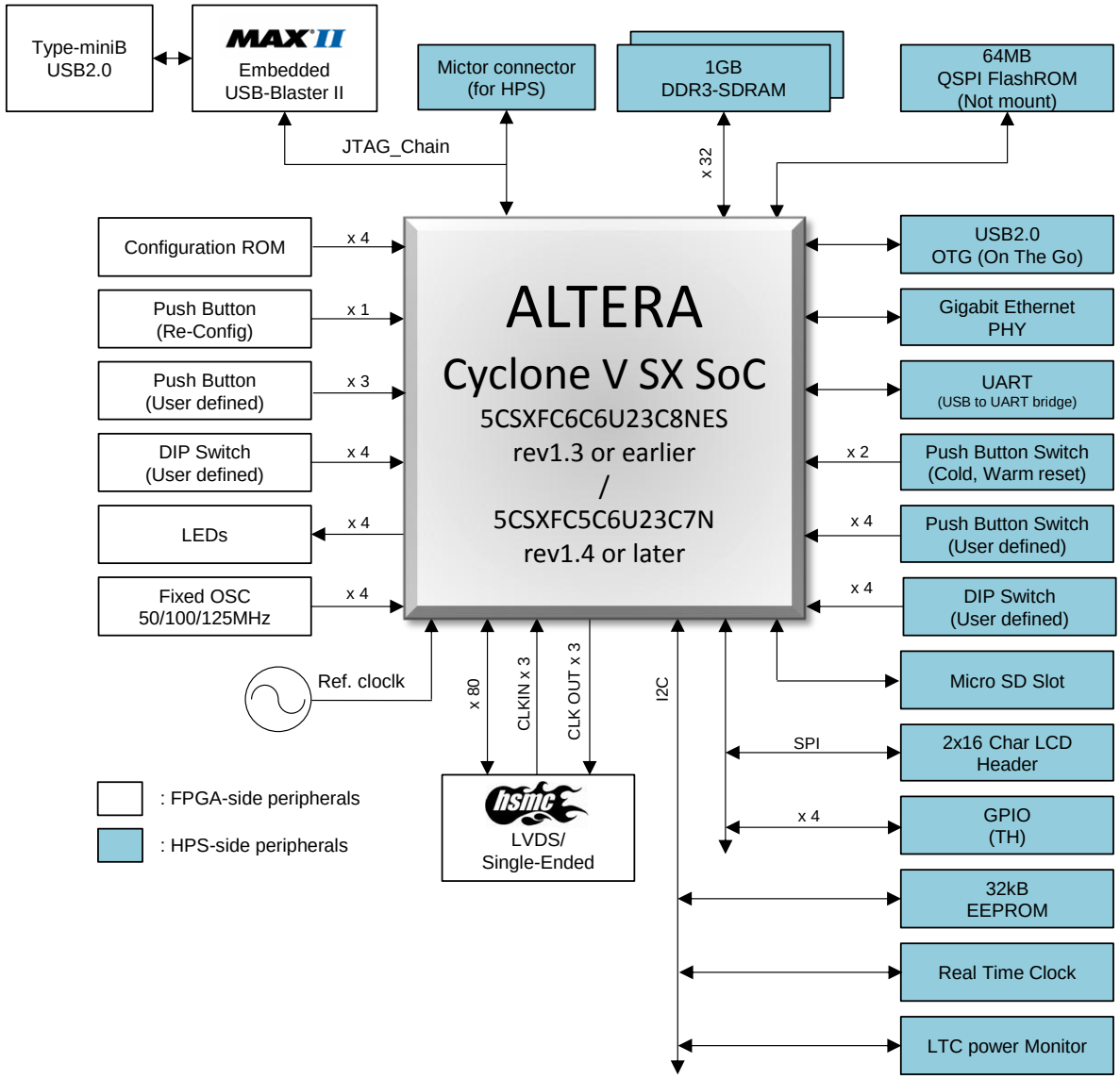

Figure 3-3-1. The Helio board Block Diagram

Board Specification

Table 3-3-1. Board specification

PCB Size	Height	Width
	100mm	167mm
PCB thickness	1.6mm	
Layer number	8 Layers	

4. The Helio board Components

4.1 Board Overview

This section provides an overview of the Helio board Figure 4-1-1 shows a top view of the board.

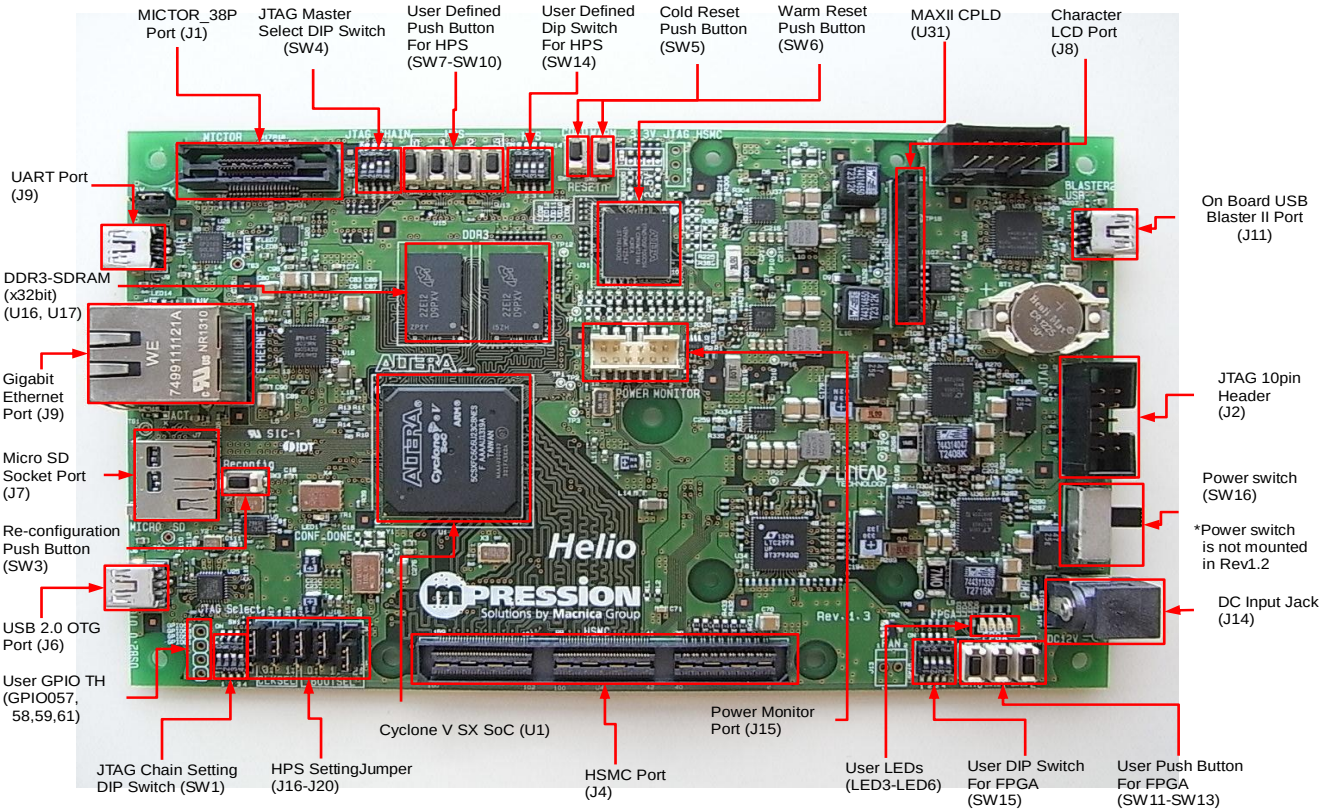

Figure 4-1-1. Board top view

Table 4-1-1 describes the components and lists their corresponding board references.

Table 4-1-1. Board components

Board Reference	Type	Description
Featured Devices		
U1	SoC	Cyclone V SoC, 5CSXFC6C6U23C8NES or 5CSXFC5C6U23C7N, 672-pin UBGA. 5CSXFC6C6U23C8NES was mounted in the Helio board Rev1.3 or earlier. 5CSXFC5C6U23C7N is mounted in the Helio board Rev1.4 or later.

U31	CPLD	MAX® II CPLD, EPM570GF100C5N, 100-pin FBGA
Configuration, Status, and Setup Elements		
J2	JTAG 10pin header	Provides access to the JTAG chain and disables the embedded USB-Blaster II when using an external USB-Blaster cable.
SW1	JTAG chain control DIP Switch	Remove or include devices in the active JTAG chain.
SW4	JTAG master select DIP Switch	Select master I/F of JTAG chain, and master I/F for HPS.
J11	USB type-B connector	USB interface for FPGA programming and debugging thorough the embedded USB-Blaster II JTAG via a type-B cable.
J16, J17, J18, J19, J20	HPS setting Jumper switch	Selects for the HPS boot source, and the clock mode.
SW3	Re-configuration push button	FPGA reconfigured by the configuration ROM (EPCQ) when pushed SW3.
SW5	Cold reset push button	Cold reset: HPS and Ethernet are reset when pushed SW5.
SW6	Warm reset push button	Warm reset: Only HPS is reset when pushed SW6.
LED1	Configuration done LED	Illuminates when the FPGA is configured.
LED2	Cold reset LED	Illuminates when the HPS is Cold reset.
LED7	UART Transmit LED	Blink when there is UART data to transmit.
LED8	UART Receive LED	Blink when there is data on the UART receive buffer.
LED14	Ethernet LINK LED	Illuminates when the Ethernet linked.
LED15	Ethernet ACT LED	Illuminates when the Ethernet activity.
Clock Circuitry		
U6	100-MHz oscillator	100.000-MHz crystal oscillator for the GXB reference clock.
X1	50-MHz oscillator	50.000-MHz crystal oscillator for general purpose logic.
X2	25-MHz oscillator	25.000-MHz crystal oscillator for the HPS primary and secondary clock.
X3	100-MHz oscillator	100.000-MHz crystal oscillator for general purpose logic.
X4	125-MHz oscillator	125.000-MHz crystal oscillator for general purpose logic.
General User Input / Output		
LED3, LED4, LED5, LED6	User LEDs	Four user LEDs. Illuminates when driven low.
SW7, SW8, SW9, SW10	User push button for HPS	Four user push buttons. Connected to the GPIO on the HPS.
SW11, SW12, SW13	User push button for FPGA	Three user push buttons. Connected to the IO of the FPGA.
SW14	User DIP switch for HPS	Four-bit DIP switch. Connected to the GPIO of the HPS.
SW15	User DIP switch for FPGA	Four-bit DIP switch. Connected to the IO of the FPGA.
GPIO1, GPIO2, GPIO3, GPIO4	User GPIO	Four GPIO through holes. Connected to the GPIO of the HPS.
Memory Devices		
U16, U17	DDR3-SDRAM	1GB DDR3-SDRAM (Two 512MB DDR3): Connected to HPS with a 32-bit data bus.
U21	QSPI-Flash memory	64MB QSPI NOR Flash memory: Connected to HPS. HPS support serial, Dual, Quad I/O SPI protocols. Note: QSPI FlashROM was not mounted in the Helio board.
U7	FPGA configuration ROM	Serial or quad-serial FPGA configuration in devices that support active serial ASx1 or ASx4 configuration schemes. 256-Mbit.
U19	EEPROM	32-kbit I2C Serial EEPROM. Connected to HPS
Communication Ports		

J1	Mictor connector	The ARM DSTREM or third party debugger is able to connect to Mictor connector.
J4	HSMC port	Provides 84CMOS or 17LVDS channels per the HSMC specification.
J5	Gigabit Ethernet port	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Micrel KSZ9021RL and the HPS-based Ethernet MAC in RGMII mode.
J6	USB 2.0 OTG port	USB mini-AB connector which provides a USB2.0 Hi-Speed and OTG protocol via a SMSC USB3300 and the HPS-based USB2.0 LINK in ULPI.
J7	Micro SD socket	Micro SD socket which provides a Micro SD via the HPS-based SD/SDIO/MMC flash controller.
J9	UART port	USB mini-B connector which provides a USB-serial via a Silicon Labs CP2103 and the HPS-based UART.
J11	On-Board USB-Blaster II port	USB mini-B connector which provides the FPGA configuration via a Cypress CY7C68013A and an Altera MAXII CPLD.
Display Interface		
J16	Character LCD	Connector that interfaces to a provided 16character x2 line LCD module along with two standoffs.
Power Supply		
J14	DC input jack	Accepts a 12-V DC power supply.
SW16	Power switch	SW16 is the slide switch for power supply ON/OFF. (**However, SW16 is not mounted on the Helio Rev1.2 board. The power supply of the Helio Rev1.2 board is supplied by connecting an AC adapter.**)

4.2 Featured Device: Cyclone V SoC

Cyclone V SoC 5CSXFC6C6U23CNES and 5CSXFC5C6U23C7N device in a 672-pin UBGA package is surface-mounted on the Helio board.
Table 4-2-1 describes the features of the Cyclone V SoC 5CSXFC6C6U23C and 5CSXFC5C6U23C device.

Table 4-2-1. Cyclone V SoC Features

Device	ALMs	Equivalent LEs	M10K RAM Blocks	Total RAM (Kbits)	18-bit x 18-bit multipliers	PLLs	Transceivers	ARM Cortex-A9	Pakage Type
5CSXFC6C6U23C	41,509	110,000	557	5,570	224	FPGA 6 HPS 3	6	Dual-core	672-pin UBGA
5CSXFC5C6U23C	32,075	85,000	397	3972	174	FPGA 6 HPS 3	6	Dual-core	672-pin UBGA

4.2.1 I/O Resources

The Cyclone V SoC 5CSXFC6C6U23CNES and 5CSXFC5C6U23C7N device has 342 user I/Os and six transceiver channels. Table 4-2-2 lists the Cyclone V SoC device I/O pin count and usage by function on this board.

Table 4-2-2. Cyclone V SoC Device I/O Pin Count

Function	I/O Standard	I/O Count	Special Pins
DDR3-SDRAM	1.5-V SSTL	80	HPS, One differential x4 DQS pin
QSPI FlashROM	3.3-V CMOS	6	HPS
USB2.0 OTG port	3.3-V CMOS	12	HPS
UART	3.3-V CMOS	2	HPS
RTC & EEPROM	3.3-V CMOS	2	HPS (I2C)
Character LCD	3.3-V CMOS	4	HPS
Gigabit Ethernet port	3.3-V CMOS	15	HPS
Push buttons	3.3-V CMOS	2	HPS
Dip switches	3.3-V CMOS	4	HPS
GPIO	3.3-V CMOS	4	HPS
HSMC port	2.5-V CMOS + LVDS	91	17 LVDS, I2C
On-board USB-Blaster II	1.5-V	17	-
Push buttons	2.5-V CMOS	5	User defined, Re-config for FPGA
Dip switches	2.5-V CMOS	4	User defined
LEDs	2.5-V CMOS	4	User defined
Clock or Oscillators	2.5V CMOS + LVDS + PCML	16	
Total I/O Used:		268	

4.3 JTAG Configuration

This section describes configuration methods of FPGA and HPS supported by the Helio board. The Helio board supports the following three configuration methods:

- On-board USB-Blaster II is the default method for configuring the FPGA/HPS using the Quartus® II Programmer/the ARM DS-5™ Altera Edition in JTAG mode with the supplied USB cable.
- Mictor connector is the default method for debugging the HPS using the In-Circuit Emulator in JTAG mode.

External USB-Blaster for configuring the FPGA/HPS using an external USB-Blaster that connects to the JTAG chain header (J2).

4.3.1 HPS debugging and FPGA Programming over On-board USB-Blaster II

This configuration method is implemented using USB-mini type-B connector (J11), a USB 2.0 PHY device (U33), and an Altera MAX II CPLD EPM570GF100C5N (U31). Connect the USB cable directly to the USB-Blaster II port of the Helio board.
HPS can be debugged via ARM DS-5 Altera Edition. And FPGA can be programmed via Quartus II programmer. The On-board USB-Blaster II is normally masters of the JTAG chain. Figure 4-3-1 illustrates the JTAG chain.

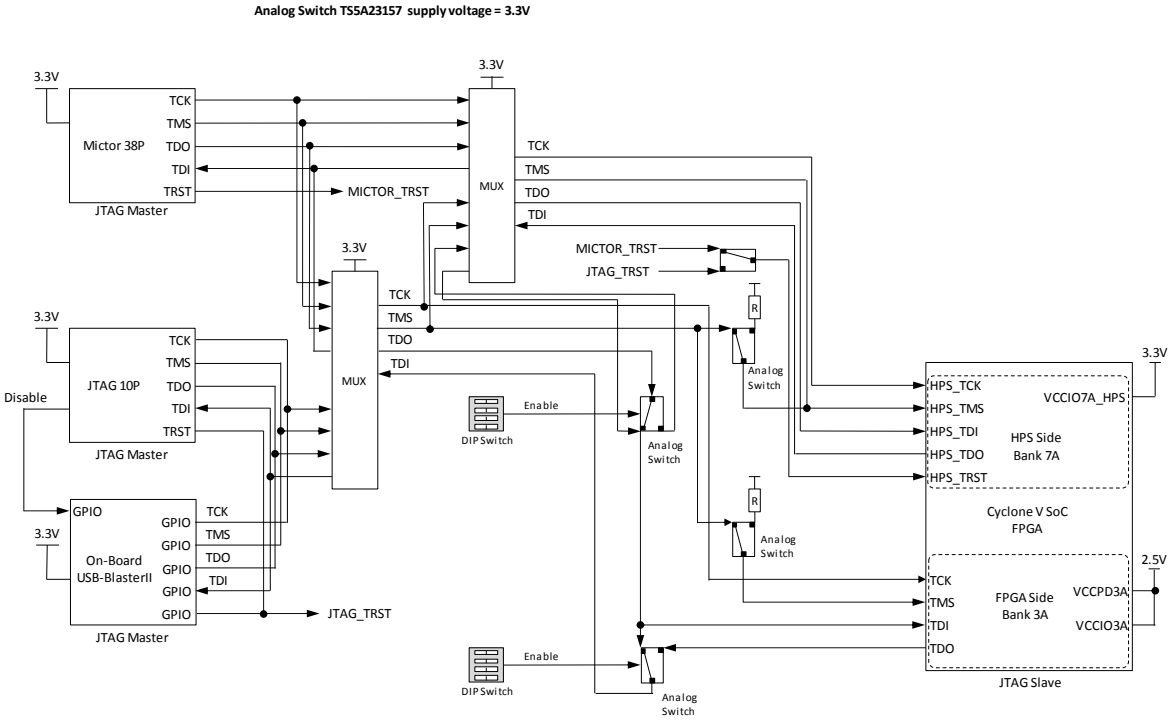

Figure 4-3-1. JTAG Chain

The JTAG setting control DIP switch (SW1, SW4) controls the Analog Switch and the Multiplexer shown in Figure 4-3-1. Refer to 4.5.1 JTAG settings DIP switch if you want to confirm detail settings for JTAG setting DIP switches.

- Stable operation of the On-board USB-Blaster II
  The On-board USB-Blaster II has a default clock frequency for TCK (JTAG) or DCLK (Active Serial programming) of 24MHz. The frequency may be changed to lower frequencies where stable operation and timing does not allow operation at 24MHz.

  - Workaround / Fix
    The following command as the Embedded Command Shell may be used to change the clock frequency of the On-board USB-Blaster II:

    $ jtagconfig --setparam 1 JtagClock <frequency>

    <frequency> is the desired TCK or DCLK frequency. 24M, 16M and 6M are supported.

  - Get clock frequency command

    $ jtagconfig –getparam 1 JtagClock

4.3.2 HPS debugging over Mictor connector for In-Circuit Emulator

Mictor connector (J1) is the connector that has JTAG and Trace data 8-bit bus for HPS debugging with In-Circuit Emulator of ARM coretex-A9.
JTAG and Trace data 8-bit bus of HPS is connected to Mictor connector when JTAG setting DIP switch SW1-[2] was OFF. Refer to 4.5.1 JTAG settings DIP switchif you want to confirm detail settings for JTAG setting DIP switches.
Table 4-3-1 shows the Mictor connector pin assignments.

Table 4-3-1. Mictor Connector Pin Assignments

Board Reference(J4)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
6	TRACE_CLK_MIC	3.3-V	C21	Trace Clock
9	MICTOR_RSTn	3.3-V	A23	HPS Reset
11	JTAG_MICTOR_TDI	3.3-V	D22	JTAG Data Input
15	JTAG_MICTOR_TCK	3.3-V	H22	JTAG Clock
16	TRACE_DATA7	3.3-V	C18	Trace Data Bit 7
17	JTAG_MICTOR_TMS	3.3-V	A29	JTAG Mode Select
18	TRACE_DATA6	3.3-V	A19	Trace Data Bit 6
19	JTAG_MICTOR_TDO	3.3-V	B23	JTAG Data Output
20	TRACE_DATA5	3.3-V	J18	Trace Data Bit 5
21	MICTOR_TRST	3.3-V	C22	JTAG Reset
22	TRACE_DATA4	3.3-V	A20	Trace Data Bit 4
24	TRACE_DATA3	3.3-V	K18	Trace Data Bit 3
26	TRACE_DATA2	3.3-V	A21	Trace Data Bit 2
28	TRACE_DATA1	3.3-V	B21	Trace Data Bit 1
38	TRACE_DATA0	3.3-V	A22	Trace Data Bit 0

4.3.3 FPGA Programming over External USB-Blaster

The JTAG header (J2) provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. To prevent contention between the JTAG masters, the On-board USB-Blaster II is automatically disabled when you connect an external USB-Blaster to the JTAG chain through the JTAG header (J2). Table 4-3-2 lists the JTAG header pin assignment.

Table 4-3-2. JTAG header Pin Assignments

Board Reference (J2)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
1	JTAG_TCK	3.3-V	—	JTAG Clock
2	USB_DISABLEn	3.3-V	—	On-board USB-Blaster II disable when JTAG header is used, the On-board USB-Blaster II JTAG interface cannot be used.
3	JTAG_BLASTER_TDI	3.3-V	—	JTAG Data from device
4	3.3V	—	—	3.3V Power
5	JTAG_TMS	3.3-V	—	JTAG Mode Select
6	MICTOR_RSTn	3.3-V	—	Mictor Reset Signal Input
7				
8	JTAG_TRST	3.3-V	—	JTAG Reset
9	JTAG_BLASTER_TDO	3.3-V	—	JTAG Data to device
10	GND	—	—	Ground

4.4 Status Elements

The Helio board includes status LEDs. This section describes the status elements. Table 4-4-1 lists the LED board references, name, and functional descriptions.

Table 4-4-1. Board-Specific LEDs

Board Reference	Schematic Signal Name	I/O Standard	Description
LED1	CONF_DONE(Inverted)	3.3-V	Green LED. Illuminates when FPGA is successfully configured.
LED2	COLD_RESETn	3.3-V	Red LED. Illuminates when cold_reset is asserted.
LED13	5.0V (Power)	5.0-V	Green LED. Illuminates when 5.0V power is active.

4.5 Setup Elements

The Helio board includes some of setup elements. This section describes the following setup elements:

- JTAG settings DIP switch
- HPS operation mode setting Jumper
- HPS reset push button
- Program configuration push button
- MSEL pins settings

4.5.1 JTAG settings DIP switch

The JTAG setting control DIP switch (SW1, SW4) remove or include devices in the active JTAG chain and select JTAG master interface. Table 4-5-1, Table 4-5-2 lists the switch controls and its descriptions.

Table 4-5-1. JTAG Setting Control DIP Switch (SW1)

Board Reference	Schematic Signal Name	I/O Standard	Description	Default
SW1-1	JTAG_SEL	3.3-V	JTAG master interface select: ON : Select On-board USB-Blaster II or JTAG 10pin Header OFF : Select MICTOR connector	ON
SW1-2	JTAG_HPS_SEL	3.3-V	Cyclone V SoC HPS JTAG Master Select: ON : Select On-board USB-Blaster II or JTAG 10pin Header OFF : Select MICTOR connector	ON
SW1-[3:4]	-	-	This switch has to set ON when normal operation.	ON

Table 4-5-2. JTAG Setting Control DIP Switch (SW4)

Board Reference	Schematic Signal Name	I/O Standard	Description	Default
SW4-1	HPS_JTAG_EN	3.3-V	Remove or include HPS side in the active JTAG chain: ON : Bypass Cyclone V SoC HPS Side OFF : Cyclone V SoC HPS Side in-chain	OFF
SW4-2	FPGA_JTAG_EN	3.3-V	Remove or include FPGA side in the active JTAG chain: ON : Bypass Cyclone V SoC FPGA Side OFF : Cyclone V SoC FPGA Side in-chain	OFF
SW4-[3:4]	-	-	This switch has to set ON when normal operation.	ON

4.5.2 HPS operation mode settings Jumper

The HPS operation mode setting Jumpers are Jumper for the Cyclone V SoC HPS side BSEL[2:0] and CSEL[1:0]. Table 4-5-3 shows the HPS operation mode setting Jumper.

Table 4-5-3. HPS operation mode setting Jumper

Board Reference	Schematic Signal Name	I/O Standard	Description
J16	SPI_CSn (BOOTSEL0)	3.3-V	boot select BSEL0: Jumper setting: 1-2 short / 2-3 short BSEL0: High(1) / Low(0) Default: 1-2 short
J18	QSPI_SS0 (BOOTSEL1)	3.3-V	boot select BSEL1: Jumper setting: 1-2 short / 2-3 short BSEL1: High(1) / Low(0) Default: 2-3 short
J20	BOOTSEL2	3.3-V	boot select BSEL2: Jumper setting: 1-2 short / 2-3 short BSEL2: High(1) / Low(0) Default: 1-2 short
J17	UART_TX (CLKSEL0)	3.3-V	clock select CSEL0: Jumper setting: 1-2 short / 2-3 short CSEL0: High(1) / Low(0) Default: 2-3 short
J19	CLKSEL1	3.3-V	clock select CSEL1: Jumper setting: 1-2 short / 2-3 short CSEL1: High(1) / Low(0) Default: 2-3 short

For more information on the BSEL and CSEL of HPS, refer to the following document:

- Booting and Configuration of Cyclone V SoC HPS, refer to the cv_5400A.

4.5.3 HPS reset push button

The HPS reset push button, COLD_RESETn (SW5) and WARM_RESETn (SW6), are input to the Cyclone V SoC HPS_PORn and HPS_nRST pin. Table4-5-4 lists the button controls and its descriptions.

Table 4-5-4. Reset push button

Board Reference	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
SW5	COLD_RESETn	3.3-V	H19	Cold reset is Power-ON reset to the HPS and Ethernet PHY. Resets all HPS logic that can be reset.
SW6	WARM_RESETn	3.3-V	A23	Warm reset is system reset of HPS block. Only affects the system reset domain, which allows debugging (including trace) to operate through the warm reset.

Figure 4-5-1 illustrates the Reset tree.

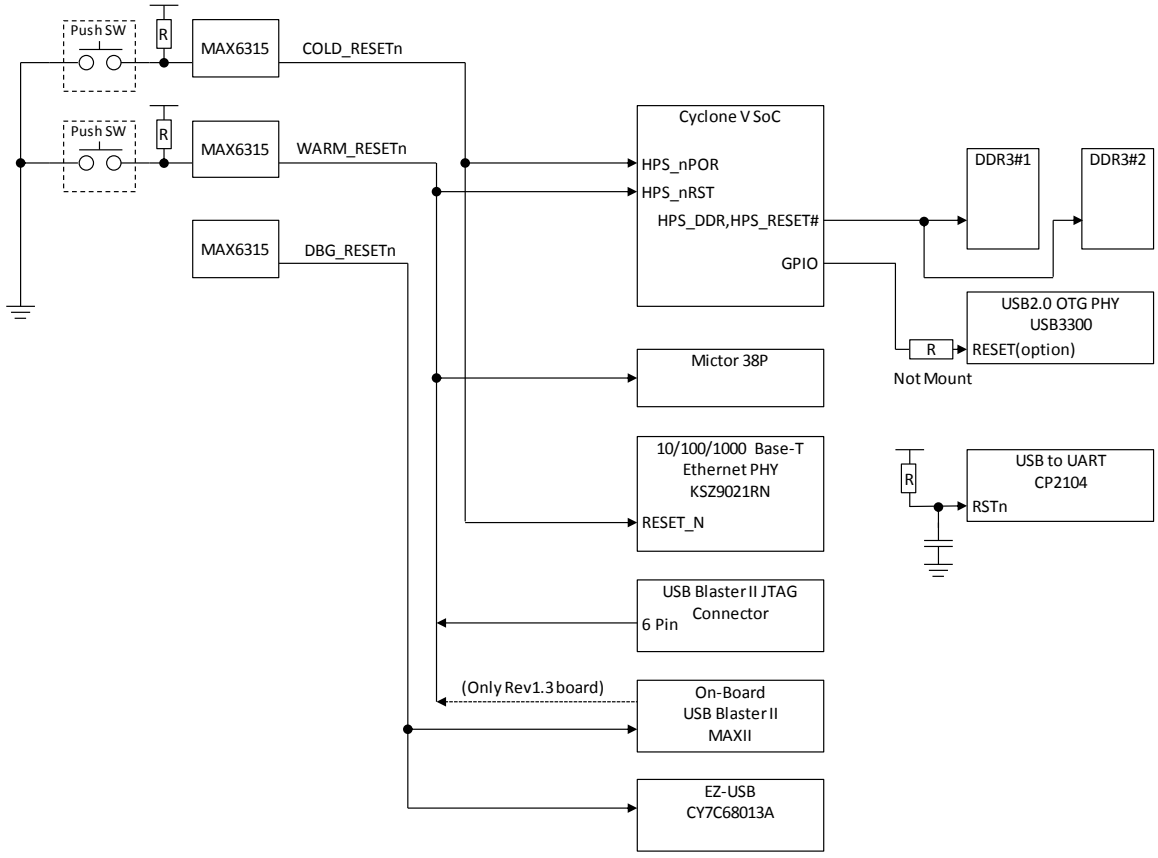

Figure 4-5-1. Reset tree on the Helio board

4.5.4 Program configuration push button

The program configuration push button, nCONFIG (SW3), is an input to the Cyclone V SoC nCONFIG pin. This input forces a FPGA reconfiguration from the EPCQ memory. Table 4-5-5 lists the switch control and its description.

Table 4-5-5. Program configuration push button

Board Reference	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
SW3	nCONFIG	3.3-V	F7	Reconfiguration Switch. Push this button when FPGA is required configuration again.

4.5.5 MSEL pins Settings

In the Helio board, the MSEL pins of the Cyclone V SoC are set as follows.

Table 4-5-6. MSEL pins Setting

MSEL[4..0]	Configuration mode	POR Delay
10010	Active serial (AS) x4	Fast

4.6 Clock Circuitry

This section describes the board's clock inputs and outputs.

4.6.1 On board Oscillators

The Helio board includes oscillators with a frequency of 25-MHz, 50-MHz, 100-MHz and 125-MHz. Figure 4-6-1 shows the default frequencies of all external clocks going to the Helio board.

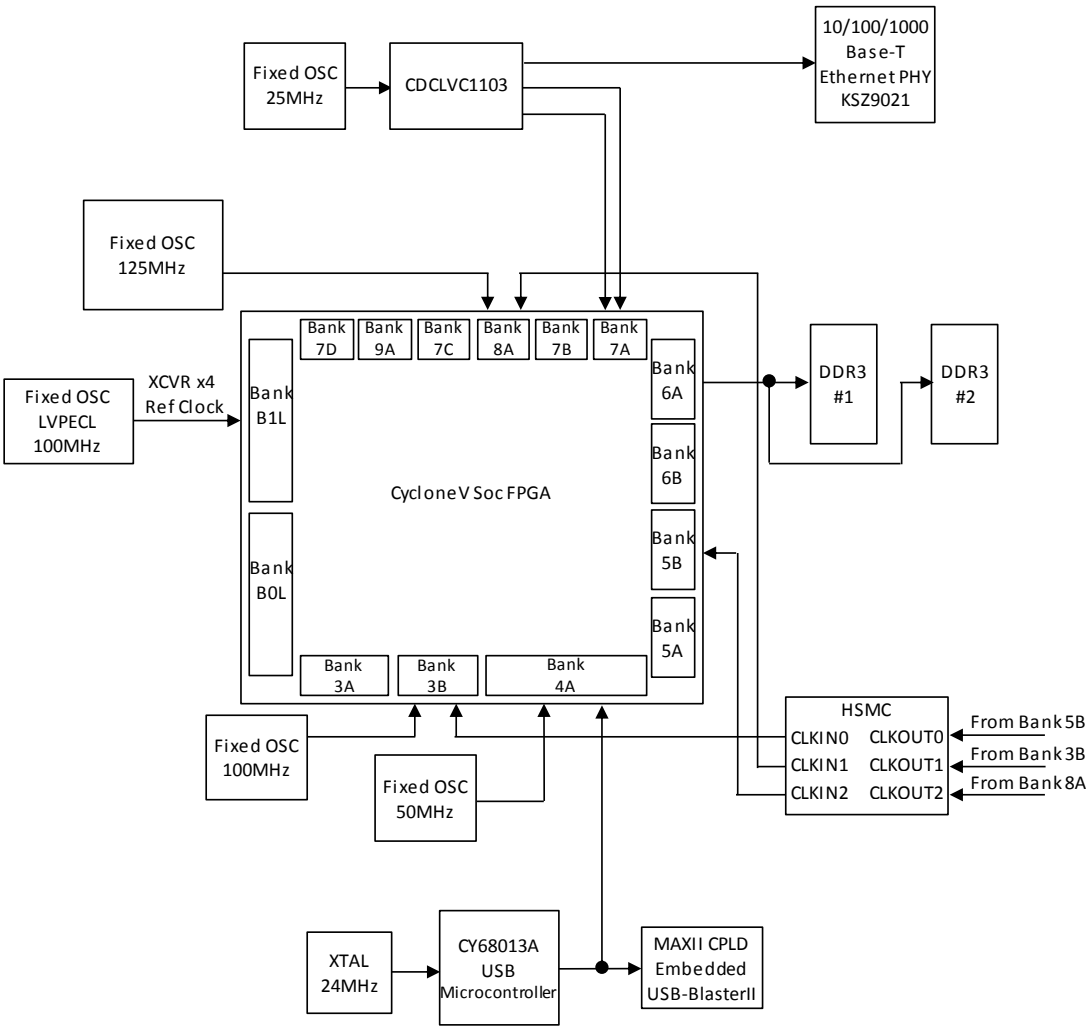

Figure 4-6-1. The Helio board Clocks

Table 4-6-1 lists the oscillators, its I/O standard, and voltages required for the Helio board.

Table 4-6-1. On-board Oscillators

Source	Schematic Signal Name	Frequency	I/O Standard	Cyclone V SoC Pin Number	Application
X1	CLK_50M_FPGA	50.000 MHz	2.5V CMOS	Y13	User
X2	CLK_OSC1	25.000 MHz	3.3V CMOS	F20	HPS Master Clock
	CLK_OSC2	25.000 MHz	3.3V CMOS	D20	HPS Sub Clock
	CLK_25M_ENET	25.000 MHz	3.3V CMOS	—	Ethernet PHY
X3	CLK_100M_FPGA	100.000 MHz	2.5V CMOS	V12	User
X4	CLK_125M_FPGA_P	125.000 MHz	LVDS	D12	Transceiver re-config
	CLK_125M_FPGA_N	125.000 MHz	LVDS	C12	Transceiver re-config
U6	REFCLK_QL1_P	100.000 MHz	LVPECL	P8	Transceiver reference
	REFCLK_QL1_N	100.000 MHz	LVPECL	N8	Transceiver reference

4.6.2 Off-board inputs / outputs

The Helio board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification. Table4-6-2 lists the clock inputs for the Helio board.

Table 4-6-2. Off-board Clock inputs

Source	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
HSMC	HSMA_CLK_IN0	2.5V CMOS	V11	Single-ended input from the installed HSMC cable or board.
HSMC	HSMA_CLK_IN_P1	LVDS/LVCMOS	E11	LVDS input from the installed HSMC cable or board. Can also support 2x LVCMOS inputs.
	HSMA_CLK_IN_N1	LVDS/LVCMOS	D11	
HSMC	HSMA_CLK_IN_P2	LVDS/LVCMOS	W21	LVDS input from the installed HSMC cable or board. Can also support 2x LCMOS inputs.
	HSMA_CLK_IN_N2	LVDS/LVCMOS	W20	

Table 4-6-3 lists the clock outputs for the Helio board.

Table 4-6-3. Off-board Clock outputs

Source	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
HSMC	HSMA_CLK_OUT0	2.5V CMOS	AB26	FPGA CMOS output(or GPIO)
HSMC	HSMA_CLK_OUT_P1	LVDS/LVCMOS	AG5	LVDS output. Can also support 2x LVCMOS outputs.
	HSMA_CLK_OUT_N1	LVDS/LVCMOS	AH4	
HSMC	HSMA_CLK_OUT_P2	LVDS/LVCMOS	E8	LVDS output. Can also support 2x LVCMOS outputs.
	HSMA_CLK_OUT_N2	LVDS/LVCMOS	D8	

4.7 General User Input / Output

This section describes the user I/O interfaces to the FPGA, including the push buttons, DIP switches, LEDs, and character LCD.

4.7.1 User-Defined push button

The Helio board includes seven user-defined push buttons. Board references SW11, SW12 and SW13 are push buttons for controlling FPGA logic of Cyclone V SoC FPGA. Board references SW7 through SW10 are push buttons to inputs to HPS_GPI on the Cyclone V SoC HPS.
Table 4-7-1 shows user-defined push button schematic signal names and their corresponding Cyclone V SoC device pin numbers.

Table 4-7-1. User-Defined Push Buttons Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
SW11	USER_PB_FPGA0	2.5-V	Y4	User-defined push buttons
SW12	USER_PB_FPGA1	2.5-V	Y8	
SW13	USER_PB_FPGA2	2.5-V	Y5	
SW7	USER_PB_HPS0	1.5-V	Y26	Connect to HPS_GPI9
SW8	USER_PB_HPS1	1.5-V	Y28	Connect to HPS_GPI8
SW9	USER_PB_HPS2	1.5-V	T16	Connect to HPS_GPI7
SW10	USER_PB_HPS3	1.5-V	T17	Connect to HPS_GPI6

4.7.2 User-Defined DIP Switch

Board references SW14 and SW15 are two four-pin DIP switches. These switches are user-defined. When the switch is in the OFF position, logic 1 is selected. When the switch is in the ON position, logic 0 is selected. There are no board-specific functions for these switches.
Table 4-7-2 shows the user-defined DIP switch schematic signal names and their corresponding Cyclone V SoC device pin numbers.

Table 4-7-2. User-Defined DIP Switch Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
SW15-1	USER_DIPSW_FPGA0	2.5-V	W8	User-defined DIP switch that connects to the FPGA
SW15-2	USER_DIPSW_FPGA1	2.5-V	AB4	
SW15-3	USER_DIPSW_FPGA2	2.5-V	T8	
SW15-4	USER_DIPSW_FPGA3	2.5-V	AA4	
SW14-1	USER_DIPSW_HPS0	1.5-V	V24	Connected to HPS_GPI13
SW14-2	USER_DIPSW_HPS1	1.5-V	AC27	Connected to HPS_GPI12
SW14-3	USER_DIPSW_HPS2	1.5-V	U16	Connected to HPS_GPI11
SW14-4	USER_DIPSW_HPS3	1.5-V	U15	Connected to HPS_GPI10

4.7.3 User-Defined LEDs

The Helio Board includes general user-defined LEDs. Board references LED3 through LED6 are user-defined LEDs. For example, status and debugging signals are driven to the LEDs from Cyclone V SoC FPGA logic. Driving logic 0 on the I/O port turns the LED on while driving logic 1 turns the LED off. There are no board-specific functions for these LEDs.
Table 4-7-3 shows the general LED schematic signal names and their corresponding Cyclone V SoC device pin numbers.

Table 4-7-3. User-Defined LED Schematic Names and Functions

Board Reference	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
LED3	USER_LED_FPGA0	2.5-V	U9	User-defined LED
LED4	USER_LED_FPGA1	2.5-V	AD4	
LED5	USER_LED_FPGA2	2.5-V	V10	
LED6	USER_LED_FPGA3	2.5-V	AC4	

4.7.4 Character LCD

The Helio board has 10pin receptacle header to connect Display Module NHD -0216K3Z – NSW-BBW-V3 (made by Newhaven Display International, Inc.).
The SPI signal interface of Cyclone V SoC HPS on this board shifts a 5.0V level for connection with Display Module.
Table 4-7-4 lists the LCD connector pin assignments and their corresponding Cyclone V SoC device pin numbers.

Table 4-7-4. LCD connector Pin Assignments, Schematic Signal Names and Functions

Board Reference (J8)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
1	N.C.	—	—-	Not connected
2	GND	—	—	Ground
3	5.0V	-	-	5.0V Power
4	N.C.	—	—-	Not connected
5	DISP_SPI_CSn (5.0V)	3.3-V	J17	SPI Slave Select
6	DISP_SPI_MISO (5.0V)	3.3-V	B18	SPI Master In Slave Out Data
7	DISP_SPI_CLK (5.0V)	3.3-V	A18	SPI Clock
8	DISP_SPI_MOSI (5.0V)	3.3-V	C17	SPI Master Out Slave In Data
9	GND	—	—	Ground
10	5.0V	—	—	5.0V Power

For more information of the Display Module, refer to the following web site:

- NHD-0216K3Z-NSW-BBW-V3 specification, refer to newhavendisplay.com/

4.7.5 Debug Header

The Helio board includes four debug through hole for debug purposes. Cyclone V SoC HPS GPIO route directly to the through hole for the debugging, or quick verification.
Table 4-7-5 lists the debug through hole pin assignments, signal names, and functions.

Table 4-7-5. Debug Through-Hole Pin Assignments, Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
GPIO1	USER_HPS_GPIO61	3.3-V	A17	Connected to HPS_GPIO61
GPIO2	USER_HPS_GPIO59	3.3-V	B18	Connected to HPS_GPIO59 *
GPIO3	USER_HPS_GPIO58	3.3-V	C17	Connected to HPS_GPIO58 *
GPIO4	USER_HPS_GPIO57	3.3-V	A18	Connected to HPS_GPIO57 *

*Note: When LCD module interface is used, GPIO interface cannot be used.

4.8 Components and Interfaces

This section describes the Helio board's communication ports and interface relative to the Cyclone V SoC device. The Helio board supports the following communication ports:

- 10/100/1000 Ethernet
- HSMC
- USB2.0 OTG
- UART
- SD
- I2C

4.8.1 10 / 100 / 1000 Ethernet

The Helio board supports 10/100/1000 base-T Ethernet using an external Micrel KSZ9021RL PHY and HPS Ethernet MAC function. The PHY-to-MAC interface is RGMII interface. The Ethernet function must be provided in the Cyclone V SoC HPS (MAC) for typical networking applications. The Micrel KSZ9021RL PHY uses 3.3-V and 1.2-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator.
Figure 4-8-1 shows the RGMII interface between the HPS (MAC) and Micrel KSZ9021RL PHY.

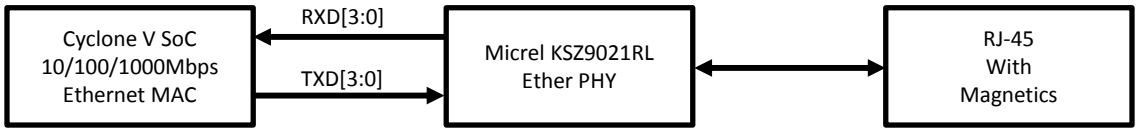

Figure 4-8-1. RGMII Interface between HPS (MAC) and Micrel KSZ9021RL PHY

Table 4-8-1 shows the Ethernet PHY interface pin assignments.

Table 4-8-1. Ethernet PHY Pin assignments, Signal Names and Functions

Board Reference (U18)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
24	ENET_GTX_CLK	3.3-V	J15	125-MHz RGMII transmit clock
38	ENET_HPS_INTn	3.3-V	B14	Management bus interrupt
17	ENET_HPS_LED1_LINK	3.3-V	—	Programmable LED1 output
18	ENET_HPS_LED2_LINK	3.3-V	—	Programmable LED2 output
36	ENET_HPS_MDC	3.3-V	A13	Management bus data clock
37	ENET_HPS_MDIO	3.3-V	E16	Management bus data
42	ENET_HPS_RESETn	3.3-V	—	Device reset
35	ENET_HPS_RX_CLK	3.3-V	J12	RGMII receive clock
32	ENET_HPS_RXD0	3.3-V	A14	RGMII receive data bus
31	ENET_HPS_RXD1	3.3-V	A11	RGMII receive data bus
28	ENET_HPS_RXD2	3.3-V	C15	RGMII receive data bus
27	ENET_HPS_RXD3	3.3-V	A9	RGMII receive data bus
33	ENET_HPS_RX_DV	3.3-V	J13	RGMII receive data valid
19	ENET_HPS_TXD0	3.3-V	A16	RGMII transmit data bus

20	ENET_HPS_TXD1	3.3-V	J14	RGMII transmit data bus
21	ENET_HPS_TXD2	3.3-V	A15	RGMII transmit data bus
22	ENET_HPS_TXD3	3.3-V	D17	RGMII transmit data bus
25	ENET_HPS_TX_EN	3.3-V	A12	RGMII transmit enable
2	MDI_HPS_P0	3.3-V	—	Media dependent interface
3	MDI_HPS_N0	3.3-V	—	Media dependent interface
5	MDI_HPS_P1	3.3-V	—	Media dependent interface
6	MDI_HPS_N1	3.3-V	—	Media dependent interface
7	MDI_HPS_P2	3.3-V	—	Media dependent interface
8	MDI_HPS_N2	3.3-V	—	Media dependent interface
9	MDI_HPS_P3	3.3-V	—	Media dependent interface
10	MDI_HPS_N3	3.3-V	—	Media dependent interface

4.8.2 HSMC

The Helio board supports a HSMC interface. The HSMC interface also supports a full SPI4.2 interface (17 LVDS channels), three input and output clocks, as well as SMB signals. The LVDS channels can be used for CMOS signaling or LVDS.

The HSMC is an Altera-developed open specification, which allows you to expand functionality of the Helio board through the addition of daughter cards.
For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the High Speed Mezzanine Card (HSMC) Specification manual.

The HSMC connector has a total of 172 pins, including 88 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is the 0.5 mm-pitch QSH/QTH of high-speed, board-to-board connectors supplied by Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

Figure 4-8-2 shows the bank arrangement of signals with respect to the Samtec connector's three banks.

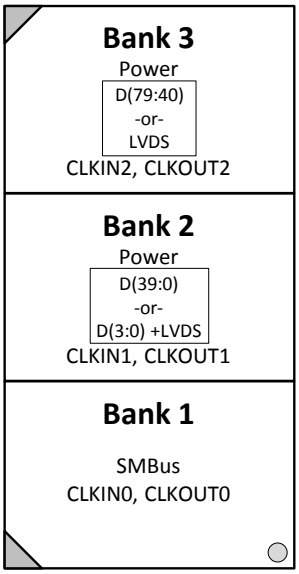

Figure 4-8-2. HSMC Signal and Bank Diagram

The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

As noted in the High Speed Mezzanine Card (HSMC) Specification manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 4-8-2 shows the HSMC interface pin assignments, signal names, and functions.

Table 4-8-2. HSMC Interface Pin Assignments, Schematic Signal Names and Functions

Board Reference (J4)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
17	—	—	—	—
18	—	—	—	—
19	—	—	—	—
20	—	—	—	—
21	—	—	—	—
22	—	—	—	—
23	—	—	—	—
24	—	—	—	—
25	—	—	—	—
26	—	—	—	—
27	—	—	—	—
28	—	—	—	—
29	—	—	—	—
30	—	—	—	—
31	—	—	—	—
32	—	—	—	—

33	HSMA_SDA	2.5-V CMOS	AA11	Management serial data
34	HSMA_SCL	2.5-V CMOS	Y11	Management serial clock
35	—	—	—	—
36	—	—	—	—
37	—	—	—	—
38	—	—	—	—
39	HSMA_CLK_OUT0	2.5-V CMOS	AB26	Dedicated CMOS Clock output
40	HSMA_CLK_IN0	2.5-V CMOS	V11	Dedicated CMOS Clock input
41	HSMA_D0	2.5-V CMOS	AG8	CMOS I/O bit 0
42	HSMA_D1	2.5-V CMOS	AH12	CMOS I/O bit 1
43	HSMA_D2	2.5-V CMOS	AF18	CMOS I/O bit 2
44	HSMA_D3	2.5-V CMOS	AH7	CMOS I/O bit 3
47	HSMA_TX_D_P0	LVDS or 2.5-V	AF20	LVDS TX bit 0 or CMOS bit 4
48	HSMA_RX_ D_P0	LVDS or 2.5-V	AD23	LVDS RX bit 0 or CMOS bit 5
49	HSMA_TX_ D_N0	LVDS or 2.5-V	AG20	LVDS TX bit 0n or CMOS bit 6
50	HSMA_RX_ D_N0	LVDS or 2.5-V	AE22	LVDS RX bit 0n or CMOS bit 7
53	HSMA_TX_ D_P1	LVDS or 2.5-V	AH23	LVDS TX bit 1 or CMOS bit 8
54	HSMA_RX_ D_P1	LVDS or 2.5-V	AF22	LVDS RX bit 1 or CMOS bit 9
55	HSMA_TX_ D_N1	LVDS or 2.5-V	AH22	LVDS TX bit 1n or CMOS bit 10
56	HSMA_RX_ D_N1	LVDS or 2.5-V	AF21	LVDS RX bit 1n or CMOS bit 11
59	HSMA_TX_ D_P2	LVDS or 2.5-V	AG19	LVDS TX bit 2 or CMOS bit 12
60	HSMA_RX_ D_P2	LVDS or 2.5-V	AE20	LVDS RX bit 2 or CMOS bit 13
61	HSMA_TX_ D_N2	LVDS or 2.5-V	AH19	LVDS TX bit 2n or CMOS bit 14
62	HSMA_RX_ D_N2	LVDS or 2.5-V	AD20	LVDS RX bit 2n or CMOS bit 15
65	HSMA_TX_ D_P3	LVDS or 2.5-V	AG18	LVDS TX bit 3 or CMOS bit 16
66	HSMA_RX_ D_P3	LVDS or 2.5-V	AE19	LVDS RX bit 3 or CMOS bit 17
67	HSMA_TX_ D_N3	LVDS or 2.5-V	AH18	LVDS TX bit 3n or CMOS bit 18
68	HSMA_RX_ D_N3	LVDS or 2.5-V	AD19	LVDS RX bit 3n or CMOS bit 19
71	HSMA_TX_ D_P4	LVDS or 2.5-V	AH17	LVDS TX bit 4 or CMOS bit 20
72	HSMA_RX_ D_P4	LVDS or 2.5-V	AD17	LVDS RX bit 4 or CMOS bit 21
73	HSMA_TX_ D_N4	LVDS or 2.5-V	AH16	LVDS TX bit 4n or CMOS bit 22
74	HSMA_RX_ D_N4	LVDS or 2.5-V	AE17	LVDS RX bit 4n or CMOS bit 23
77	HSMA_TX_ D_P5	LVDS or 2.5-V	AG15	LVDS TX bit 5 or CMOS bit 24
78	HSMA_RX_ D_P5	LVDS or 2.5-V	AF17	LVDS RX bit 5 or CMOS bit 25
79	HSMA_TX_ D_N5	LVDS or 2.5-V	AH14	LVDS TX bit 5n or CMOS bit 26
80	HSMA_RX_ D_N5	LVDS or 2.5-V	AG16	LVDS RX bit 5n or CMOS bit 27
83	HSMA_TX_ D_P6	LVDS or 2.5-V	AG14	LVDS TX bit 6 or CMOS bit 28
84	HSMA_RX_ D_P6	LVDS or 2.5-V	AF15	LVDS RX bit 6 or CMOS bit 29
85	HSMA_TX_ D_N6	LVDS or 2.5-V	AH13	LVDS TX bit 6n or CMOS bit 30
86	HSMA_RX_ D_N6	LVDS or 2.5-V	AE15	LVDS RX bit 6n or CMOS bit 31
89	HSMA_TX_ D_P7	LVDS or 2.5-V	AG11	LVDS TX bit 7 or CMOS bit 32
90	HSMA_RX_ D_P7	LVDS or 2.5-V	AA19	LVDS RX bit 7 or CMOS bit 33
91	HSMA_TX_ D_N7	LVDS or 2.5-V	AH11	LVDS TX bit 7n or CMOS bit 34
92	HSMA_RX_ D_N7	LVDS or 2.5-V	AA18	LVDS RX bit 7n or CMOS bit 35
95	HSMA_CLK_OUT_P1	LVDS or 2.5-V	AG5	LVDS or CMOS clock out 1 or CMOS bit 36
96	HSMA_CLK_IN_P1	LVDS or 2.5-V	W21	LVDS or CMOS clock in 1 or

				CMOS bit 37
97	HSMA_CLK_OUT_N1	LVDS or 2.5-V	AH4	LVDS or CMOS clock out 1n or CMOS bit 36
98	HSMA_CLK_IN_N1	LVDS or 2.5-V	W20	LVDS or CMOS clock in 1n or CMOS bit 37
101	HSMA_TX_ D_P8	LVDS or 2.5-V	AG10	LVDS TX bit 8 or CMOS bit 38
102	HSMA_RX_ D_P8	LVDS or 2.5-V	T11	LVDS RX bit 8 or CMOS bit 39
103	HSMA_TX_ D_N8	LVDS or 2.5-V	AH9	LVDS TX bit 8n or CMOS bit 40
104	HSMA_RX_ D_N8	LVDS or 2.5-V	U11	LVDS RX bit 8n or CMOS bit 41
107	HSMA_TX_ D_P9	LVDS or 2.5-V	AG9	LVDS TX bit 9 or CMOS bit 42
108	HSMA_RX_ D_P9	LVDS or 2.5-V	AE12	LVDS RX bit 9 or CMOS bit 43
109	HSMA_TX_ D_N9	LVDS or 2.5-V	AH8	LVDS TX bit 9n or CMOS bit 44
110	HSMA_RX_ D_N9	LVDS or 2.5-V	AD12	LVDS RX bit 9n or CMOS bit 45
113	HSMA_TX_ D_P10	LVDS or 2.5-V	AH6	LVDS TX bit 10 or CMOS bit 46
114	HSMA_RX_ D_P10	LVDS or 2.5-V	AG13	LVDS RX bit 10 or CMOS bit 47
115	HSMA_TX_ D_N10	LVDS or 2.5-V	AH5	LVDS TX bit 10n or CMOS bit 48
116	HSMA_RX_ D_N10	LVDS or 2.5-V	AF13	LVDS RX bit 10n or CMOS bit 49
119	HSMA_TX_ D_P11	LVDS or 2.5-V	AH3	LVDS TX bit 11 or CMOS bit 50
120	HSMA_RX_ D_P11	LVDS or 2.5-V	AD11	LVDS RX bit 11 or CMOS bit 51
121	HSMA_TX_ D_N11	LVDS or 2.5-V	AH2	LVDS TX bit 11n or CMOS bit 52
122	HSMA_RX_ D_N11	LVDS or 2.5-V	AE11	LVDS RX bit 11n or CMOS bit 53
125	HSMA_TX_ D_P12	LVDS or 2.5-V	AE8	LVDS TX bit 12 or CMOS bit 54
126	HSMA_RX_ D_P12	LVDS or 2.5-V	AF11	LVDS RX bit 12 or CMOS bit 55
127	HSMA_TX_ D_N12	LVDS or 2.5-V	AF9	LVDS TX bit 12n or CMOS bit 56
128	HSMA_RX_ D_N12	LVDS or 2.5-V	AF10	LVDS RX bit 12n or CMOS bit 57
131	HSMA_TX_ D_P13	LVDS or 2.5-V	AE4	LVDS TX bit 13 or CMOS bit 58
132	HSMA_RX_ D_P13	LVDS or 2.5-V	AD10	LVDS RX bit 13 or CMOS bit 59
133	HSMA_TX_ D_N13	LVDS or 2.5-V	AF4	LVDS TX bit 13n or CMOS bit 60
134	HSMA_RX_ D_N13	LVDS or 2.5-V	AE9	LVDS RX bit 13n or CMOS bit 61
137	HSMA_TX_ D_P14	LVDS or 2.5-V	AF5	LVDS TX bit 14 or CMOS bit 62
138	HSMA_RX_ D_P14	LVDS or 2.5-V	U14	LVDS RX bit 14 or CMOS bit 63
139	HSMA_TX_ D_N14	LVDS or 2.5-V	AF6	LVDS TX bit 14n or CMOS bit 64
140	HSMA_RX_ D_N14	LVDS or 2.5-V	U13	LVDS RX bit 14n or CMOS bit 65
143	HSMA_TX_ D_P15	LVDS or 2.5-V	AE7	LVDS TX bit 15 or CMOS bit 66
144	HSMA_RX_ D_P15	LVDS or 2.5-V	W14	LVDS RX bit 15 or CMOS bit 67
145	HSMA_TX_ D_N15	LVDS or 2.5-V	AF8	LVDS TX bit 15n or CMOS bit 68
146	HSMA_RX_ D_N15	LVDS or 2.5-V	V13	LVDS RX bit 15n or CMOS bit 69
149	HSMA_TX_ D_P16	LVDS or 2.5-V	AF7	LVDS TX bit 16 or CMOS bit 70
150	HSMA_RX_ D_P16	LVDS or 2.5-V	T13	LVDS RX bit 16 or CMOS bit 71
151	HSMA_TX_ D_N16	LVDS or 2.5-V	AG6	LVDS TX bit 16n or CMOS bit 72
152	HSMA_RX_ D_N16	LVDS or 2.5-V	T12	LVDS RX bit 16n or CMOS bit 73
155	HSMA_CLK_OUT_P2	LVDS or 2.5-V	E8	LVDS or CMOS clock out 2 or CMOS bit 74
156	HSMA_CLK_IN_P2	LVDS or 2.5-V	E11	LVDS or CMOS clock in 2 or CMOS bit 75
157	HSMA_CLK_OUT_N2	LVDS or 2.5-V	D8	LVDS or CMOS clock out 2n or CMOS bit 76

158	HSMA_CLK_IN_N2	LVDS or 2.5-V	D11	LVDS or CMOS clock in 2n or CMOS bit 77
160	HSMA_PSNTN	2.5-V CMOS	AD5	HSMC port presence detect

4.8.3 USB2.0 OTG

The Helio board supports USB 2.0 OTG using an external SMSC USB3300 PHY and HPS ULPI LINK function. The PHY-to-LINK interface is ULPI interface. The LINK function must be provided in the Cyclone V SoC HPS for typical USB applications.

Figure 4-8-3 shows the ULPI interface between the HPS (LINK) and SMSC USB3300 PHY.

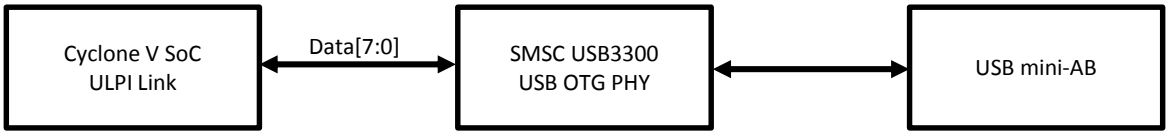

Figure 4-8-3. ULPI Interface between HPS (LINK) and SMSC USB3300 PHY

Table 4-8-3 shows the ULPI interface between the HPS (LINK) and SMSC USB3300 PHY.

Table 4-8-3. USB2.0 PHY Pin Assignments, Signal Names and Functions

Board Reference (U25)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
14	USB_CLK	3.3-V	G4	ULPI Clock
24	USB_DATA0	3.3-V	C10	ULPI Data Bit 0
23	USB_DATA1	3.3-V	F5	ULPI Data Bit 1
22	USB_DATA2	3.3-V	C9	ULPI Data Bit 2
21	USB_DATA3	3.3-V	C4	ULPI Data Bit 3
20	USB_DATA4	3.3-V	C8	ULPI Data Bit 4
19	USB_DATA5	3.3-V	D4	ULPI Data Bit 5
18	USB_DATA6	3.3-V	C7	ULPI Data Bit 6
17	USB_DATA7	3.3-V	F4	ULPI Data Bit 7
12	USB_DIR	3.3-V	E5	ULPI Direction
11	USB_NXT	3.3-V	D5	ULPI Next Data
13	USB_STP	3.3-V	C5	ULPI Stop Data
9	USB_RESET	3.3-V	E4	Optional Active High Reset.

4.8.4 UART

The Helio board supports USB/UART using an external Silicon Labs CP2103 and Cyclone V SoC HPS UART function.

Table 4-8-4 lists the UART interface between the HPS and Silicon Labs CP2103 PHY.

Table 4-8-4. USB to UART IC Pin Assignments, Signal Names and Functions

Board Reference (U28)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
21	UART_RX	3.3-V	B19	UART Receive
20	UART_TX	3.3-V	C16	UART Transmit
12	CONV_HPS_USB_N	3.3-V	C6	T.B.D.

- *Note: Install the CP2103 device driver in PC for the console beforehand when you use UART port. Download the latest CP2103 device driver from the following Web sites.
  CP210x USB to UART Bridge VCP Drivers

- J10 header
  In the Helio board, J10 is header for UART loop back test. Do not short J10 header at normal operation.

4.8.5 SD

The Helio board supports microSD card interface using Cyclone V SoC HPS SD function.
Table 4-8-5 lists the microSD card interface between the HPS and microSD Socket.

Table 4-8-5. SD Pin Assignments, Signal Names and Functions

Board Reference (J7)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
5	SD_CLK	3.3-V	B8	SDMMC Clock out
3	SD_CMD	3.3-V	D14	SDMMC Command Line
7	SD_DAT0	3.3-V	C13	SDMMC Data Bit 0
8	SD_DAT1	3.3-V	B6	SDMMC Data Bit 1
1	SD_DAT2	3.3-V	B11	SDMMC Data Bit 2
2	SD_CD_DAT3	3.3-V	B9	SDMMC Data Bit 3

**: The microSD circuit of The Helio board is not a recommended circuit of the SD specifications. When you make an evaluation board, you should confirm the SD Specifications.

4.8.6 I2C

The Helio board supports I2C Interface using Cyclone V SoC HPS I2C function.
Table 4-8-6 lists the I2C Interface pin assignments, signal names, and functions.

Table 4-8-6. I2C Pin Assignments, Signal Names and Functions

Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
I2C_SCL_HPS	3.3-V	B16	I2C Clock
I2C_SDA_HPS	3.3-V	C19	I2C Data
I2C_SCL_FPGA	2.5-V	AA24	I2C Clock
I2C_SDA_FPGA	2.5-V	AA23	I2C Data

Table 4-8-7 lists the I2C connected devices.

Table 4-8-7. I2C connected devices

Board Reference	Type	Device Address	Description
U19	24LC32A	0x51	EEPROM
U27	DS1339C-33	0x68	RTC
U34	LTC2978	0x5C	Power Monitor IC

4.9 Memory

This section describes the Helio board's memory interface support and also their signal names, types, and connectivity relative to the Cyclone V SoC. The Helio board has the following memory interfaces:

- DDR3-SDRAM
- QSPI FlashROM (QSPI device is not mounted. Only interface is supported.)
- EEPROM

4.9.1 DDR3-SDRAM

The Helio board supports two 32Meg x 16 x 8 banks interfaces for high-speed sequential memory access. User can use hard memory controller (HPS on the top edge of the FPGA) to run DDR3 SDRAM memory. 32-bit data bus comprises of two x16 devices.
Table 4-9-1 and 4-9-2 lists DDR3-SDRAM pin assignments, signal names and functions. The signal names and types are relative to the Cyclone V SoC HPS in terms of I/O setting and direction.

Table 4-9-1. DDR3 Device #1 Pin Assignments, Schematic Signal Names and Functions

Board Reference (U17)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
N3	DDR3_HPS_A0	1.5V-SSTL Class I	C28	Address bus
P7	DDR3_HPS_A1	1.5V-SSTL Class I	B28	Address bus
P3	DDR3_HPS_A2	1.5V-SSTL Class I	E26	Address bus
N2	DDR3_HPS_A3	1.5V-SSTL Class I	D26	Address bus
P8	DDR3_HPS_A4	1.5V-SSTL Class I	J21	Address bus
P2	DDR3_HPS_A5	1.5V-SSTL Class I	J20	Address bus
R8	DDR3_HPS_A6	1.5V-SSTL Class I	C26	Address bus
R2	DDR3_HPS_A7	1.5V-SSTL Class I	B26	Address bus
T8	DDR3_HPS_A8	1.5V-SSTL Class I	F26	Address bus
R3	DDR3_HPS_A9	1.5V-SSTL Class I	F25	Address bus
L7	DDR3_HPS_A10	1.5V-SSTL Class I	A24	Address bus
R7	DDR3_HPS_A11	1.5V-SSTL Class I	B24	Address bus
N7	DDR3_HPS_A12	1.5V-SSTL Class I	D24	Address bus
T3	DDR3_HPS_A13	1.5V-SSTL Class I	C24	Address bus
T7	DDR3_HPS_A14	1.5V-SSTL Class I	G23	Address bus
M2	DDR3_HPS_BA0	1.5V-SSTL Class I	A27	Bank Address bus
N8	DDR3_HPS_BA1	1.5V-SSTL Class I	H25	Bank Address bus
M3	DDR3_HPS_BA2	1.5V-SSTL Class I	G25	Bank Address bus
L2	DDR3_HPS_CSn	1.5V-SSTL Class I	L21	Chip select
L3	DDR3_HPS_Wen	1.5V-SSTL Class I	E25	
J3	DDR3_HPS_RASn	1.5V-SSTL Class I	A25	Row address select
K3	DDR3_HPS_CASn	1.5V-SSTL Class I	A26	Column address select
K9	DDR3_HPS_CKE	1.5V-SSTL Class I	L28	
J7	DDR3_HPS_CLK_P	Differential 1.5-V SSTL Class I	N21	Differential clock

K7	DDR3_HPS_CLK_N	Differential 1.5-V SSTL Class I	N20	Differential clock
E7	DDR3_HPS_DM0	1.5V-SSTL Class I	G28	Write mask byte lane
D3	DDR3_HPS_DM1	1.5V-SSTL Class I	P28	Write mask byte lane
H8	DDR3_HPS_DQ0	1.5V-SSTL Class I	J25	Data bus byte lane 0
H7	DDR3_HPS_DQ1	1.5V-SSTL Class I	J24	Data bus byte lane 0
E3	DDR3_HPS_DQ2	1.5V-SSTL Class I	E28	Data bus byte lane 0
H3	DDR3_HPS_DQ3	1.5V-SSTL Class I	D27	Data bus byte lane 0
F7	DDR3_HPS_DQ4	1.5V-SSTL Class I	J26	Data bus byte lane 0
F8	DDR3_HPS_DQ5	1.5V-SSTL Class I	K26	Data bus byte lane 0
G2	DDR3_HPS_DQ6	1.5V-SSTL Class I	G27	Data bus byte lane 0
F2	DDR3_HPS_DQ7	1.5V-SSTL Class I	F28	Data bus byte lane 0
C8	DDR3_HPS_DQ8	1.5V-SSTL Class I	K25	Data bus byte lane 1
B8	DDR3_HPS_DQ9	1.5V-SSTL Class I	L25	Data bus byte lane 1
D7	DDR3_HPS_DQ10	1.5V-SSTL Class I	J27	Data bus byte lane 1
A7	DDR3_HPS_DQ11	1.5V-SSTL Class I	J28	Data bus byte lane 1
C2	DDR3_HPS_DQ12	1.5V-SSTL Class I	M27	Data bus byte lane 1
C3	DDR3_HPS_DQ13	1.5V-SSTL Class I	M26	Data bus byte lane 1
A3	DDR3_HPS_DQ14	1.5V-SSTL Class I	M28	Data bus byte lane 1
A2	DDR3_HPS_DQ15	1.5V-SSTL Class I	N28	Data bus byte lane 1
F3	DDR3_HPS_DQS_P0	Differential 1.5-V SSTL Class I	R17	Data strobe P byte lane 0
G3	DDR3_HPS_DQS_N0	Differential 1.5-V SSTL Class I	R16	Data strobe N byte lane 0
C7	DDR3_HPS_DQS_P1	Differential 1.5-V SSTL Class I	R19	Data strobe P byte lane 1
B7	DDR3_HPS_DQS_N1	Differential 1.5-V SSTL Class I	R18	Data strobe N byte lane 1
K1	DDR3_HPS_ODT	1.5V-SSTL Class I	D28	On-die termination enable
L8	DDR3_HPS_ZQ	—	—	ZQ impedance calibration

Table 4-9-2. DDR3 Device #2 Pin Assignments, Schematic Signal Names and Functions

Board Reference (U16)	Schematic Signal Name	I/O Standard	Cyclone V SoC Pin Number	Description
N3	DDR3_HPS_A0	1.5V-SSTL Class I	C28	Address bus
P7	DDR3_HPS_A1	1.5V-SSTL Class I	B28	Address bus
P3	DDR3_HPS_A2	1.5V-SSTL Class I	E26	Address bus
N2	DDR3_HPS_A3	1.5V-SSTL Class I	D26	Address bus
P8	DDR3_HPS_A4	1.5V-SSTL Class I	J21	Address bus
P2	DDR3_HPS_A5	1.5V-SSTL Class I	J20	Address bus
R8	DDR3_HPS_A6	1.5V-SSTL Class I	C26	Address bus
R2	DDR3_HPS_A7	1.5V-SSTL Class I	B26	Address bus
T8	DDR3_HPS_A8	1.5V-SSTL Class I	F26	Address bus
R3	DDR3_HPS_A9	1.5V-SSTL Class I	F25	Address bus
L7	DDR3_HPS_A10	1.5V-SSTL Class I	A24	Address bus
R7	DDR3_HPS_A11	1.5V-SSTL Class I	B24	Address bus

N7	DDR3_HPS_A12	1.5V-SSTL Class I	D24	Address bus
T3	DDR3_HPS_A13	1.5V-SSTL Class I	C24	Address bus
T7	DDR3_HPS_A14	1.5V-SSTL Class I	G23	Address bus
M2	DDR3_HPS_BA0	1.5V-SSTL Class I	A27	Bank Address bus
N8	DDR3_HPS_BA1	1.5V-SSTL Class I	H25	Bank Address bus
M3	DDR3_HPS_BA2	1.5V-SSTL Class I	G25	Bank Address bus
L2	DDR3_HPS_CSn	1.5V-SSTL Class I	L21	Chip select
L3	DDR3_HPS_Wen	1.5V-SSTL Class I	E25	
J3	DDR3_HPS_RASn	1.5V-SSTL Class I	A25	Row address select
K3	DDR3_HPS_CASn	1.5V-SSTL Class I	A26	Column address select
K9	DDR3_HPS_CKE	1.5V-SSTL Class I	L28	
J7	DDR3_HPS_CLK_P	Differential 1.5-V SSTL Class I	N21	Differential clock
K7	DDR3_HPS_CLK_N	Differential 1.5-V SSTL Class I	N20	Differential clock
E7	DDR3_HPS_DM2	1.5V-SSTL Class I	W28	Write mask byte lane
D3	DDR3_HPS_DM3	1.5V-SSTL Class I	AB28	Write mask byte lane
H8	DDR3_HPS_DQ16	1.5V-SSTL Class I	N24	Data bus byte lane 0
H7	DDR3_HPS_DQ17	1.5V-SSTL Class I	N25	Data bus byte lane 0
E3	DDR3_HPS_DQ18	1.5V-SSTL Class I	T28	Data bus byte lane 0
H3	DDR3_HPS_DQ19	1.5V-SSTL Class I	U28	Data bus byte lane 0
F7	DDR3_HPS_DQ20	1.5V-SSTL Class I	N26	Data bus byte lane 0
F8	DDR3_HPS_DQ21	1.5V-SSTL Class I	N27	Data bus byte lane 0
G2	DDR3_HPS_DQ22	1.5V-SSTL Class I	R27	Data bus byte lane 0
F2	DDR3_HPS_DQ23	1.5V-SSTL Class I	V27	Data bus byte lane 0
C8	DDR3_HPS_DQ24	1.5V-SSTL Class I	R26	Data bus byte lane 1
B8	DDR3_HPS_DQ25	1.5V-SSTL Class I	R25	Data bus byte lane 1
D7	DDR3_HPS_DQ26	1.5V-SSTL Class I	AA28	Data bus byte lane 1
A7	DDR3_HPS_DQ27	1.5V-SSTL Class I	W26	Data bus byte lane 1
C2	DDR3_HPS_DQ28	1.5V-SSTL Class I	R24	Data bus byte lane 1
C3	DDR3_HPS_DQ29	1.5V-SSTL Class I	T24	Data bus byte lane 1
A3	DDR3_HPS_DQ30	1.5V-SSTL Class I	Y27	Data bus byte lane 1
A2	DDR3_HPS_DQ31	1.5V-SSTL Class I	AA27	Data bus byte lane 1
F3	DDR3_HPS_DQS_P2	Differential 1.5-V SSTL Class I	T19	Data strobe P byte lane 0
G3	DDR3_HPS_DQS_N2	Differential 1.5-V SSTL Class I	T18	Data strobe N byte lane 0
C7	DDR3_HPS_DQS_P3	Differential 1.5-V SSTL Class I	U19	Data strobe P byte lane 1
B7	DDR3_HPS_DQS_N3	Differential 1.5-V SSTL Class I	T20	Data strobe N byte lane 1
K1	DDR3_HPS_ODT	1.5V-SSTL Class I	D28	On-die termination enable
L8	DDR3_HPS_ZQ	—	—	ZQ impedance calibration

4.9.2 QSPI Flash ROM

The Helio board supports using Cyclone V SoC HPS QSPI function a 512Mbit Quad-SPI flash device for non-volatile storage of user code space. (**However, QSPI Flash ROM is not mounted on Helio board.**)
Table4-9-3 shows the Quad-SPI flash device pin assignments, signal names functions. The signal names and types are relative to the Cyclone V SoC HPS in terms of I/O setting and direction.

Table 4-9-3. Quad-SPI Flash Pin Assignments, Schematic Signal Names and Functions

Board Reference (U21)	Schematic Signal Name	I/O Standard	Cyclone V Soc Pin Number	Description
16	QSPI_CLK	3.3-V	C14	QSPI Clock
15	QSPI_IO0	3.3-V	A8	QSPI Data IO Bit 0
8	QSPI_IO1	3.3-V	H16	QSPI Data IO Bit 1
9	QSPI_IO2	3.3-V	A7	QSPI Data IO Bit 2
1	QSPI_IO3	3.3-V	J16	QSPI Data IO Bit 3
7	QSPI_SS0	3.3-V	A6	QSPI Slave Select 0

Note: Macnica doesn't guarantee the operation when you mounted QSPI Flash ROM to this product.

4.9.3 EEPROM

The Helio board supports using Cyclone V SoC HPS I2C function a 32kbit EEPROM device for MAC Address of Ethernet. Refer to 4.8.6 I2C if you want to confirm detail EEPROM.

4.10 Power Supply

You can power up the development board from a laptop-style DC power input. The input voltage must be in the range of 12V. The DC voltage is then stepped down to various power rails used by the board components and installed into the HSMC connectors.
Table 4-10-1 outlines the allowable power inputs.

Table 4-10-1. Power Inputs

Power Source	Voltage (V)	Current (A)	Maximum Wattage (W)
DC input from AC Adaptor	12.0	3.8	45.6

⚠ **Danger**	Make sure to use the AC adapter (included in package) that is specified in this Manual. Using an AC adapter not meeting the specifications described in this Manual will cause the kit to emit heat, explode, or ignite.

⚠ **Danger**	HSMC 12V terminals are supplied 12V when AC adapter is connected to J14 of the Helio Rev1.2 board. Do not connect AC adapter to The Helio Rev1.2 board when HSMC daughter card is connected to HSMC connector.

4.10.1 Power Distribution System

Figure 4-10-1 shows the power distribution system on the Helio board. Regulator inefficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

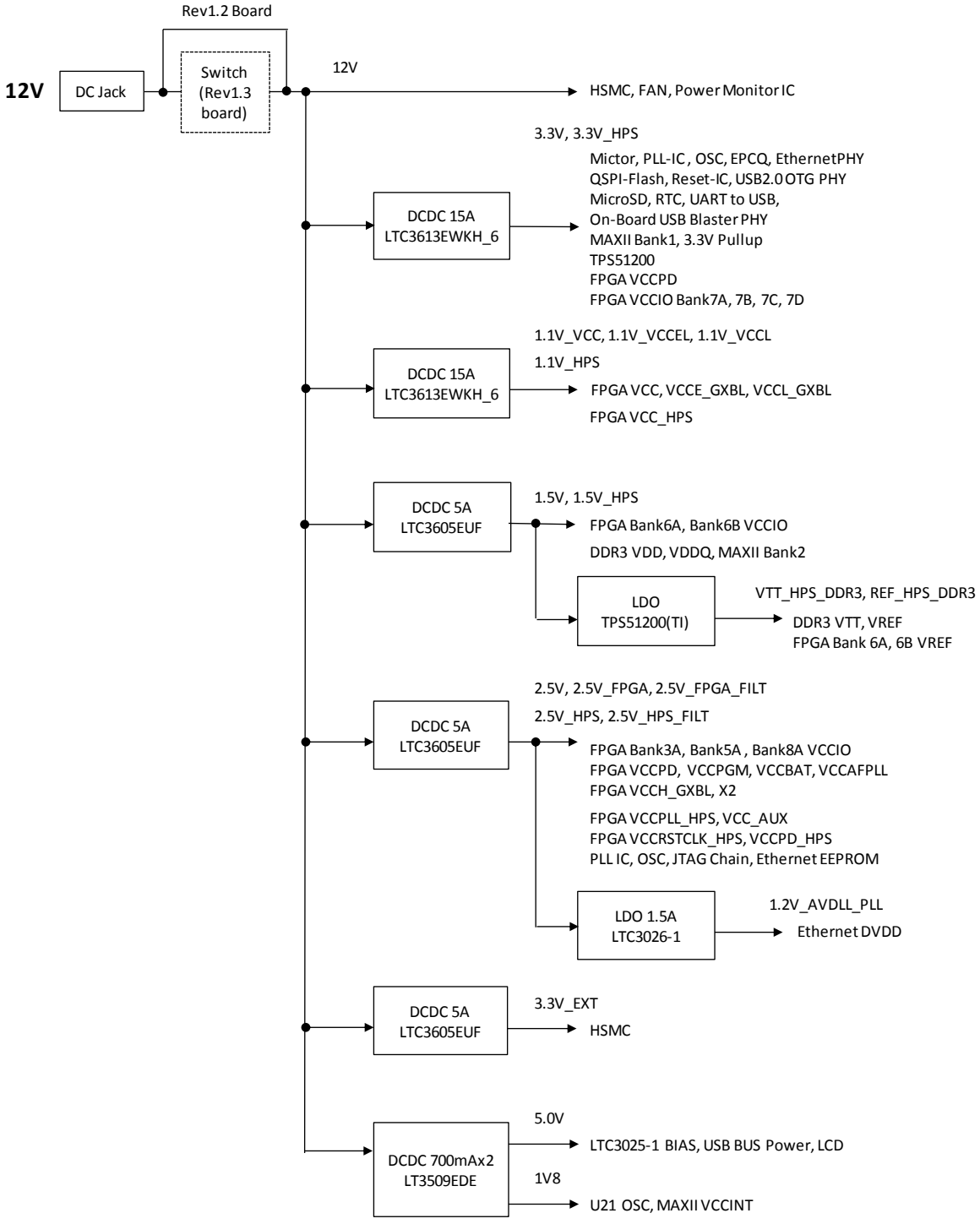

Figure 4-10-1. Power Distribution System

5. Document Revision History

Date	Revision	Changes
April 24, 2013	0.1	• Document created
Nov 19, 2013	1.0	• Changed to Mpression template
Dec 9, 2013	1.1	• Changed the doc format
Sep 1, 2014	1.2	• Added the explanation of the 5CSXC5 device
Nov 16, 2015	1.3	• Fixed default BSEL setting(0x4 -> 0x5) • Added the explanation of the SD interface
Dec 09, 2015	1.4	• Added the explanation of On-board USB-Blaster II