Top EMC08

Integration Guide

Version #: 1.0

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Version Control

Revision	Authors	Date	Comments
0.1	Vinícius Amaral	28/sep/2010	Initial Version
1.0	Thiago Santos	11/oct/2010	Power section and Synthesis section updated.

Table of Contents

1 Introduction

EMC08 project is an 8-bit Microcontroller internal IP that could be used in future projects that require, embedded DIGITAL, AMS, RF and DSP blocks as part of the automotive system application.

The 8-bit Microcontroller has a CPU optimized for control applications, extensive Boolean processing capabilities, 4K bytes of on-chip program memory (ROM) address space, 128 bytes of on-chip data RAM, 32 bidirectional and 8 unidirectional and individually addressable I/O lines, three 24-bit timer/counters, full-duplex UART, vector interrupt structure with two priority levels.

The Analog blocks are basically 8-bit digital to analog converter and low noise 2.4 GHz RF Transceiver and Receiver digital wireless protocol based. The DSP will act as a baseband processing stage, which means it will be in charge of performing several algorithms for both the transmitter and the receiver.

This Integration Guide is focused on Digital module. The Analog and DSP modules will not be part of this team development, they are considered separated IPs which can be integrated in the SoC. However, there are two essentials analog sub-modules that are necessary to digital operation:

- Phase Locked Loop – PLL
- Power On Reset

The main clock can be provided by an external crystal oscillator, or optionally, can be used the 20MHz Low-Jitter Oscillator, an analog block. The PLL provides the clock used for memories and Power On Reset provides a reliable start up of the digital core. Other analog blocks are optionally too, as well as DSP module.

The following picture shows a case which the Digital/AMS/RF/DSP modules are all integrated:

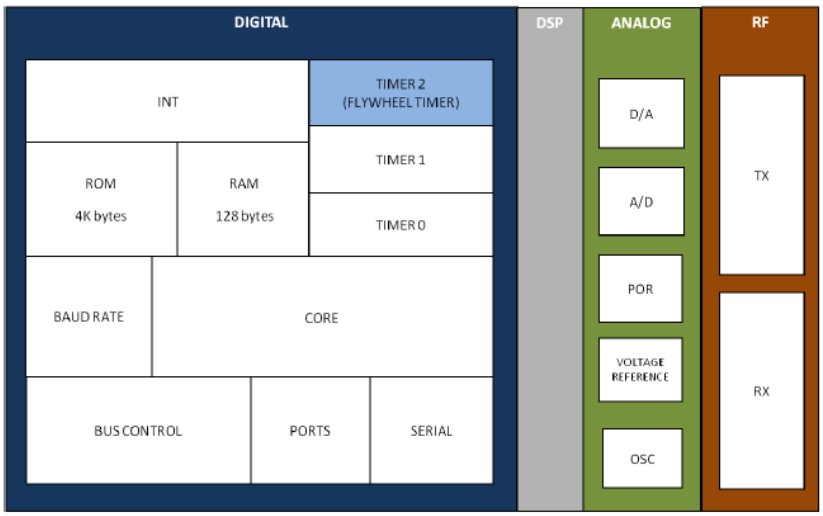

Figure 1 - EMC08 Digital/AMS/RF/DSP Modules

2 Interface Specification

A top module block diagram is shown in the following figure, with input and output connections and block internal interfaces.

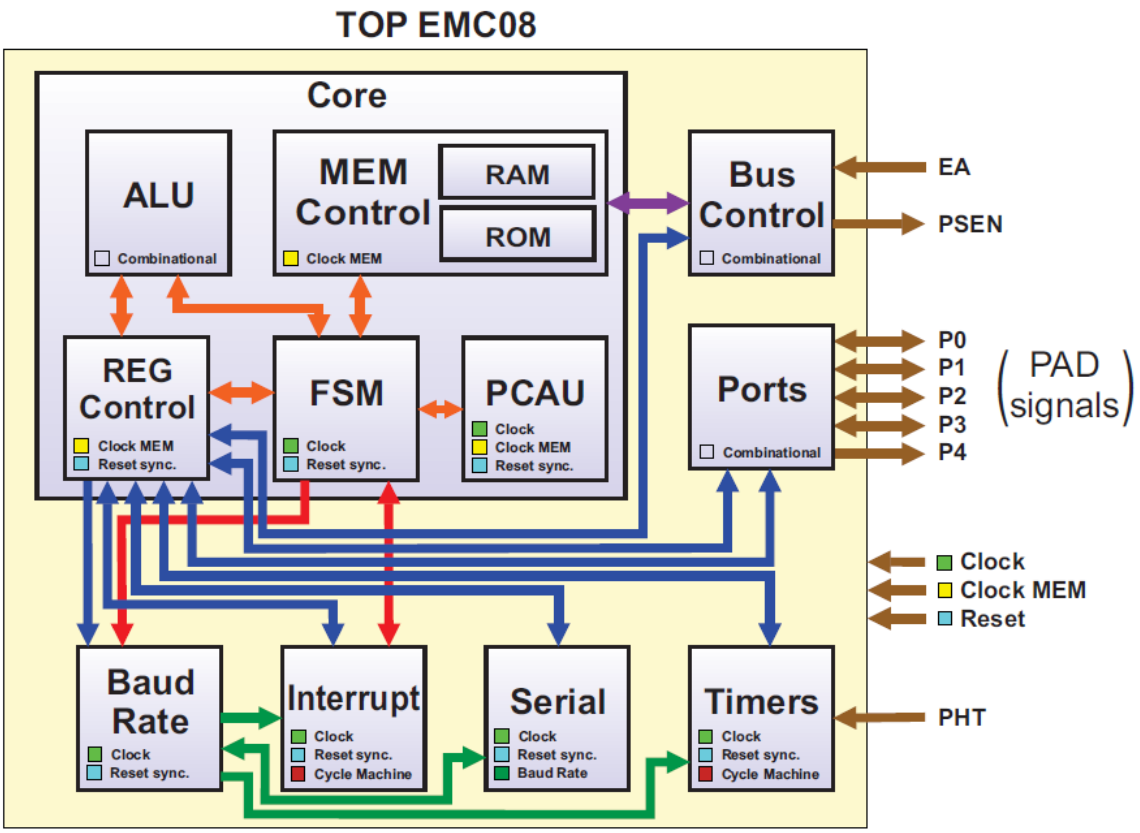

Figure 2 - EMC08 Digital block diagram

The next table describes all inputs and outputs and their reset states.

Input / Output	Description	Reset state
top_clock_i	A main clock of 20 MHz. This clock is input of top module and is distributed for all sequential blocks	-
top_clock_mem_i	A derived and synchronous clock for memories of 40 MHz.	-
top_reset_i	A synchronous (referenced to main clock) reset signal. Reset signal is low active.	-
top_p[0:3]_y_i	Output of I/O bi-directional buffer and input of Ports module.	-
top_p[0:3]_en_o	Enable for Input of I/O bi-directional buffer. It is low active.	11111111h
top_p[0:4]_a_o	Input of I/O bi-directional buffer and output of Ports module.	0000000h
top_pht_i	External chip input of Digital Flywheel Tooth sensor to Timer 2.	-
top_ea_b_i	External chip input for external memory access enable.	-
top_psen_b_o	External chip output for program store enable	High Level
top_test_mode_i	External chip input for test mode enable. Active High	-
top_scan_enable_i	External chip input for scan enable. Active High.	-
top_vcc	Digital Supply Voltage	-
top_vss	Digital Ground	-

Table 1 – Inputs and outputs specifications

2.1 Clocking

The digital module uses four domains of clock:

top_clock_i: A main clock of 20 MHz. This clock is input of top module and is distributed for all sequential blocks. This signal comes from Low-Jitter Oscillator analog block, or, if this analog block is not being used, from the external crystal oscillator.

top_clock_mem_i: A derived and synchronous clock for memories. PLL analog block will send this signal to core with twice the clock frequency. It was chosen to use this clock because the memories are very fast, and there are a lot of instructions that needs many reads and writes operations. As is not possible change the main clock frequency because it is a project specification, the design team opts to use another clock domain to control memories. So, it is possible make read or write memory operations in each semi-clock period.

top_cycle_machine: The cycle machine is an internal clock signal produced by Baud Rate digital module and sent to Interrupt and Timers modules. Each instruction of instruction set can be performed in one or two cycles of cycle machine. One cycle machine has two periods of main clock.

top_baud_rate_trans: Baud rate transition signal is an internal clock signal, derived from main clock too, and it is a 16 times faster than Baud rate signal. It is generated by Baud Rate digital module and is sent to Serial module only. This clock signal is variable and can assume a multiple value of clock period.

The following figure illustrates the relation between the three fixed clock domains.

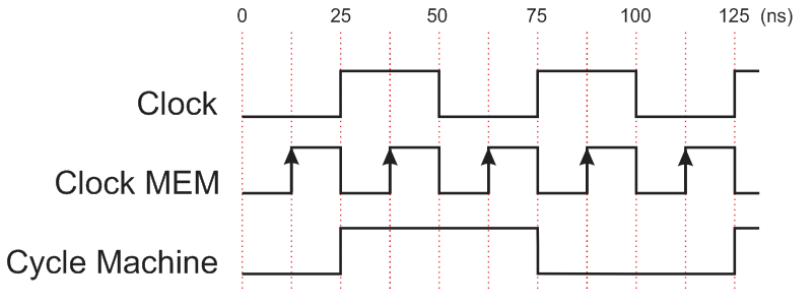

Figure 3 - Relation between fixed clock domains

The top_cycle_machine internal signal is used as data by Interrupt module and as clock by Timers module. The top_baud_rate_trans internal signal is used as data and as clock by Serial module.

2.2 Interface Timing

To be defined.

2.3 Scan Wrapper

Not applicable.

3 Power Consumption

The power consumption was estimated during the synthesis with RTL Compiler. The synthesis tool uses statistical toggle rates for analyze power consumption on each net of the component. It was

used three different libraries to estimate power consumption: slow, typical and fast libraries. Table 2 shows the libraries and the tool used. Table 3 describes characteristics of each PVT case and Table 4 presents the results of power consumption.

Tool Used	Cadence RTL Compiler. Version 7.2
Clock Frequencies	Main Clock: 20MHz Memory Clock: 40MHz
Libraries	DCELLS_MOSLP_slow_1_62_125C.lib DCELLS_MOSLP_typ_1_80_25C.lib DCELLS_MOSLP_fast_1_98_m40C.lib

Table 2 –Synthesis Tools and Libraries

PVT Corners

Process	slow	typical	fast
Temperature	125° C	25° C	-40° C
Voltage	1,62 V	1,80 V	1,98 V

Table 3 –PVT Corner Cases

Estimated Power

PVT Corner	slow	typical	fast
Dynamic Power	3,759 mW	4,835 mW	6,601 mW
Leakage Power	2478,125 nW	40,148 nW	2,545 nW

Table 4 – Power Consumption Analysis

4 Module Configurability

The module on its main functionality doesn't have any configurable issue. The test mode inputs and outputs are the only properties that can be modified. The configurable properties are: Scan Enable pin, Test Mode pin, Scan Chain Input and Output pins, number of scan chains and scan style.

By default, the pins are tied respectively to *top_scan_enable_*i, *top_test_mode_i*, *ports P0/P1, ports P2/P4*. There are sixteen predefined scan chains, configured to use muxed scan devices. These values can be changed in the synthesis script by modifying the following lines:

```
set_attr dft_scan_style muxed_scan
define_dft shift_enable -active high -create_port top_scan_enable_i
define_dft test_mode -active high -create_port top_test_mode_i

define_dft scan_chain -name emc_chain_01 -sdi top_p0_y_i[0] -shared_output -sdo top_p2_a_o[0]
define_dft scan_chain -name emc_chain_02 -sdi top_p0_y_i[1] -shared_output -sdo top_p2_a_o[1]
define_dft scan_chain -name emc_chain_03 -sdi top_p0_y_i[2] -shared_output -sdo top_p2_a_o[2]
define_dft scan_chain -name emc_chain_04 -sdi top_p0_y_i[3] -shared_output -sdo top_p2_a_o[3]
define_dft scan_chain -name emc_chain_05 -sdi top_p0_y_i[4] -shared_output -sdo top_p2_a_o[4]
define_dft scan_chain -name emc_chain_06 -sdi top_p0_y_i[5] -shared_output -sdo top_p2_a_o[5]
define_dft scan_chain -name emc_chain_07 -sdi top_p0_y_i[6] -shared_output -sdo top_p2_a_o[6]
define_dft scan_chain -name emc_chain_08 -sdi top_p0_y_i[7] -shared_output -sdo top_p2_a_o[7]
define_dft scan_chain -name emc_chain_09 -sdi top_p1_y_i[0] -shared_output -sdo top_p4_a_o[0]
define_dft scan_chain -name emc_chain_10 -sdi top_p1_y_i[1] -shared_output -sdo top_p4_a_o[1]
define_dft scan_chain -name emc_chain_11 -sdi top_p1_y_i[2] -shared_output -sdo top_p4_a_o[2]
define_dft scan_chain -name emc_chain_12 -sdi top_p1_y_i[3] -shared_output -sdo top_p4_a_o[3]
define_dft scan_chain -name emc_chain_13 -sdi top_p1_y_i[4] -shared_output -sdo top_p4_a_o[4]
```

```
define_dft scan_chain -name emc_chain_14 -sdi top_p1_y_i[5] -shared_output -sdo top_p4_a_o[5]
define_dft scan_chain -name emc_chain_15 -sdi top_p1_y_i[6] -shared_output -sdo top_p4_a_o[6]
define_dft scan_chain -name emc_chain_16 -sdi top_p1_y_i[7] -shared_output -sdo top_p4_a_o[7]
```

5 Synthesis

The synthesis process was made with Cadence RTL Compiler 7.2 using the synthesis flow showed up in the figure below.

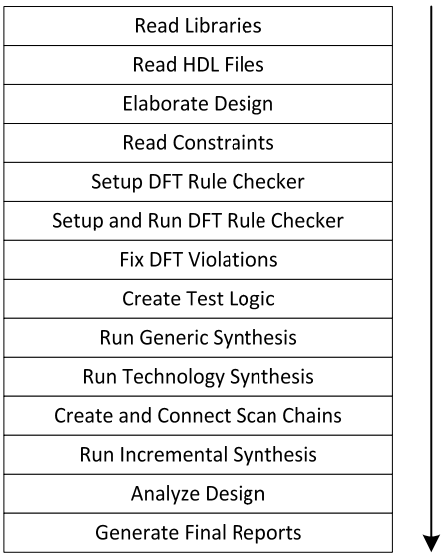

Figure 4 - Synthesis Flow

The synthesis flow was run in three different PVT corners: slow, typical and fast. For a preliminary timing analysis the constraints were defined only for the clocks, based on the PLL specifications, described in SOW.

Main Clock	
Period	50ns
Waveform	50% Duty Cycle
Rise and Fall Time	1ns
Uncertainty	1ns
Input Capacitance	1 pF
Memory Clock	
Period	25 ns
Waveform	50% Duty Cycle
Rise and Fall Time	1 ns
Uncertainty	1 ns
Input Capacitance	1 pF

Table 5 – Clock Constraints

The critical path start and end points, and the calculated slack for each PVT corner are shown below:

- `PVT Corner: slow`

```
-------------------------------------------------------------
Cost Group   : 'C2C' (path_group 'C2C')
Timing slack :       5ps
Start-point  : CORE_INSTANCE/pcau/pcau_pc_o_reg[6]/CN
End-point    : CORE_INSTANCE/fsm/fsm_op_aux_2_reg[2]/D
-------------------------------------------------------------
```

- PVT Corner: typical

```
-------------------------------------------------------------
Cost Group   : 'C2C' (path_group 'C2C')
Timing slack :       0ps
Start-point  : CORE_INSTANCE/pcau/pcau_pc_o_reg[6]/CN
End-point    : CORE_INSTANCE/fsm/fsm_op_aux_2_reg[0]/D
-------------------------------------------------------------
```

- PVT Corner: fast

```
-------------------------------------------------------------
Cost Group   : 'C2C' (path_group 'C2C')
Timing slack :       1ps
Start-point  : CORE_INSTANCE/pcau/pcau_pc_o_reg[7]/CN
End-point    : CORE_INSTANCE/fsm/fsm_op1_reg[1]/D
-------------------------------------------------------------
```

The DFT analysis showed that 662 of the 748 existents Flip-Flops are scannable. The non-scannable flops are those who use clocks generated by the Baud Rate module. These clocks are running only when the device is under normal operation, so these flops can't be included on the standard scan chains. Sixteen scan chains were created, using ports P0 and P1 as scan input and P2 and P4 as scan output. More details of the DFT can be found on the DFT Guide and DFT reports.

The complete script used to synthesize the design and the obtained reports are available at:

- Script: EMC08/digital_A/top/synthesis/scripts/top_synth.tcl
- Reports: EMC08/digital_A/top/synthesis/reports/

6 Block Technology Dependency

The Table 6 provides a list of all instantiated cells and a brief description of each one of them. This list represents the result obtained on the typical PVT corner synthesis.

Cell	Number of Instances	Description
AN211X0	53	2-Input AND into 3-Input NOR
AN21X0	148	2-Input AND into 2-Input NOR
AN21X1	1	2-Input AND into 2-Input NOR
AN221X0	138	2x2-Input AND into 3-Input NOR
AN222X0	76	3x2-Input AND into 3-Input NOR
AN22X0	193	2x2-Input AND into 2-Input NOR
AN311X0	7	3-Input AND into 3-Input NOR
AN31X0	28	3-Input AND into 2-Input NOR
AN321X0	39	3-Input AND, 2-Input AND into 3-Input NOR
AN32X0	31	3-Input, 2-Input AND into 2-Input NOR
AN33X0	7	2x3-Input AND into 2-Input NOR
AND2X0	193	2-Input AND
AND2X1	2	2-Input AND
AND2X2	1	2-Input AND
AND3X0	40	3-Input AND
AND4X0	4	4-Input AND
AND5X0	3	5-Input AND

AND6X0	16	6-Input AND
AO211X0	17	2-Input AND into 3-Input OR
AO21X0	102	2-Input AND into 2-Input OR
AO221X0	159	2-Input AND into 2-Input OR
AO221X1	1	2x2-Input AND into 3-Input OR
AO222X0	89	3x2-Input AND into 3-Input OR
AO22X0	434	2x2-Input AND into 2-Input OR
AO311X0	4	3-Input AND into 3-Input OR
AO31X0	10	3-Input AND into 2-Input OR
AO321X0	14	3-Input AND, 2-Input AND into 3-Input OR
AO32X0	37	3-Input, 2-Input AND into 2-Input OR
AO33X0	6	2x3-Input AND into 2-Input OR
DFRQX0	61	Posedge Single Q D-Flip-Flop
EN2X0	90	2-Input XNOR
EN3X0	6	3-Input XNOR
EO2X0	38	2-Input XOR
EO3X0	10	3-Input XOR
FAX0	58	Full Adder
HAX0	49	Half Adder
INX0	586	Inverter
INX1	4	Inverter
LOGIC0	5	Constant Logic 0
MU2IX0	39	2:1 Inverting Multiplexer
MU2X0	23	2:1 Multiplexer
NA2I1X0	188	2-Input NAND with 1 Inverted Input
NA2I1X1	2	2-Input NAND with 1 Inverted Input
NA2X0	711	2-Input NAND
NA2X1	38	2-Input NAND
NA2X2	5	2-Input NAND
NA3I1X0	33	3-Input NAND with 1 Inverted Input
NA3I2X0	2	3-Input NAND with 2 Inverted Inputs
NA3X0	99	3-Input NAND
NA3X1	1	3-Input NAND
NA5I2X2	1	5-Input NAND with 2 Inverted Inputs
NA6I1X0	1	6-Input NAND with 1 Inverted Input
NA6I3X0	1	6-Input NAND with 3 Inverted Inputs
NA6X0	7	6-Input NAND
NO2I1X0	274	2-Input NOR with 1 Inverted Input
NO2I1X1	22	2-Input NOR with 1 Inverted Input
NO2I1X2	2	2-Input NOR with 1 Inverted Input
NO2X0	466	2-Input NOR
NO2X1	8	2-Input NOR
NO3I1X0	54	3-Input NOR with 1 Inverted Input
NO3I2X0	3	3-Input NOR with 2 Inverted Inputs
NO3X0	53	3-Input NOR
NO5I2X0	1	5-Input NOR with 2 Inverted Inputs
NO6I2X0	1	6-Input NOR with 1 Inverted Input
NO6X0	3	6-Input NOR
OA211X0	11	2-Input OR into 3-Input AND
OA21X0	40	2-Input OR into 2-Input AND
OA221X0	9	2x2-Input OR into 3-Input AND
OA222X0	3	3x2-Input OR into 3-Input AND
OA22X0	8	2x2-Input OR into 2-Input AND

OA311X0	1	3-Input OR into 3-Input AND
OA31X0	3	3-Input OR into 2-Input AND
OA321X0	1	3-Input OR, 2-Input OR into 3-Input AND
OA32X0	2	3-Input OR, 2-Input OR into 2-Input AND
ON211X0	76	2-Input OR into 3-Input NAND
ON21X0	213	2-Input OR into 2-Input NAND
ON21X1	1	2-Input OR into 2-Input NAND
ON221X0	78	2x2-Input OR into 3-Input NANA
ON222X0	13	3x2-Input OR into 3-input NAND
ON22X0	54	2x2-Input OR into 2-Input NAND
ON311X0	7	3-Input OR into 3-input NAND
ON31X0	19	3-Input OR into 2-input NAND
ON321X0	18	3-Input OR, 2-Input OR into 3-Input NAND
ON32X0	17	3-Input OR, 2-Input OR into 2-Input NAND
ON33X0	7	2x3-Input OR into 2-Input NAND
OR2X0	102	2-Input OR
OR2X1	1	2-Input OR
OR2X2	1	2-Input OR
OR3X0	12	3-Input OR
OR3X1	1	3-Input OR
OR3X2	1	3-Input OR
OR4X0	3	4-Input OR
OR5X0	10	5-Input OR
OR6X0	6	6-Input OR
ROM4096X8	1	ROM 4096 x 8 Bits
SDFFQX0	60	Negedge Single Q D-Flip-Flop with Scan
SDFFQX1	8	Negedge Single Q D-Flip-Flop with Scan
SDFFQX2	1	Negedge Single Q D-Flip-Flop with Scan
SDFFX0	1	Negedge D-Flip-Flop with Scan
SDFRQX0	582	Posedge Single Q D-Flip-Flop with Scan
SDFRQX1	6	Posedge Single Q D-Flip-Flop with Scan
SDFRQX2	2	Posedge Single Q D-Flip-Flop with Scan
SDFRX0	19	Posedge D-Flip-Flop with Scan
SPRAM128X8	1	SPRAM 128 x 8 Bits

Table 6 – List of Instantiated Cells

The bidirectional pads used in this project requires especial ties “hi” and “lo” to work correctly. These pads have four configuration inputs, EN, PI, PDEN and PUEN, that must be set as showed in the table below:

Function	EN	PI	PDEN	PUEN
Input	HI	LOW	HI	LOW
Output	LOW	X	X	X

Table 7 – Bidirectional Pads Configuration

To a correct work, the pins PI, PDEN and PUEN must be hard tied respectively to LOW, HI and LOW logic levels. This way, the configuration is made just through the top_p[3:0]_en_o outputs. Port p4 uses a output pad.

7 Physical Properties

7.1 Introduction

The physical process adopted for EMC08 project is the XFAB 0.18 µm Modular CMOS process family: XC018. For this process family, two main modules exist:

MOSLP: Low Power MOS module, single polysilicon, 3 metals. The number of masks is 17 and it can be used for 1.8V NMOS/PMOS & resistors applications.

MOSST: Standard MOS module, single polysilicon, 3 metals. The number of masks is 17 and it can be used for 1.8V NMOS/PMOS & resistors applications.

The memories used in this project are XFAB 0.18 µm IPs. The characteristic of each memory used is described below:

ROM: 4096 x 8 bits Standard CMOS ROM Memory Module, 4 metals.

RAM: 128 x 8 bits Standard CMOS SPRAM Memory Module, 4 metals.

7.2 Library

The following standard cell library was used for this project:

- X-FAB xc018 MOSLP ISOMOS Digital Core Library, standard, 1.62V, 125C.

The table below shows the main characteristics of library adopted.

File	**D_CELLS_MOSLP_slow_1_62V_125C.lib**
Description	Synopsys technology library xc018 MOSLP Digital Core Library, low power PVT = slow process, 1.62V, 125C
Technology	xc018, MOSLP: Low Power MOS module
Library version	V 2.2.0, May 08 2008

Table 8 – Library characteristics

7.3 Floor Plan

To be defined.

7.4 VC Shielding

To be defined.

7.5 Net Shielding

To be defined.

7.6 Net Dimensions

To be defined.

7.7 Placement

To be defined.

7.8 Layers

The adopted library, XFAB 0.18 µm, provides from 3 to 6 metal layers, that can be chosen according to the project needs. For this project, 6 layers are going to be used. The description of the available layers can be found in the following LEF files provided in the design kit.

Number of Layers	LEF Files Location
3 metal layers	/ddk/XFABC018/cadence/xc018/LEF/xc018_m3_FE
4 metal layers	/ddk/XFABC018/cadence/xc018/LEF/xc018_m4_FE
5 metal layers	/ddk/XFABC018/cadence/xc018/LEF/xc018_m5_FE
6 metal layers	/ddk/XFABC018/cadence/xc018/LEF/xc018_m6_FE

Table 9 – List of LEF (Layout Exchange Format) Files

7.9 Size and Area

The synthesized area and the number of gates of each module are indicated in the following table. This area represents only the core of the VC and does not include pads.

The equivalent gates count was made based on the area of a standard 2-Input NAND cell, NA2X1, which area is 9.2232 µm².

Instance	Cell Area (µm²)	Net Area (µm²)	Number of Gates	Equivalent Gates
EMC_TOP	262849	9177	6197	28499
CORE	82288	6249	4420	8922
TIMERS	21530	972	888	2334
SERIAL	7707	354	311	835
BAUD_RATE	7077	351	276	767
INTERRUPT	4286	225	213	464
BUS_CONTROL	464	2	38	50
MEMORIES	139023	0	2	15073

Table 10 – Synthesized Area and Gates

7.10 Design Rule Checks

To be defined.

7.11 LVS

To be defined.

7.12 Power and Ground

The I/O library used is specified for 1.8V core supply and 3.3V I/O supply and three VDD and GND rails pairs. They are named as follows:

- Logic array VDD and GND, which supply power to the core of the chip.
- Output buffer VDDO and GNDO, which supply power to the I/O cell output buffers and ESD protection structures.
- Input buffer VDDR and GNDR, which supply the I/O cell input buffers. These supply rails can be completely isolated for low noise operation.

All cells used inside top module must be supplied with the same voltage of 1.8 V by VDD and GND logic array. I/O bidirectional cells use all three rails pairs.

Recommend 4 or 8 mA output buffers.

8 Floating Node Analysis

To be defined.

8.1 Critical Nets

The main critical nets to the functionality of the block and its description are listed in the following table

Net	Description
top_clock	System clock
top_clock_mem	Memory clock
top_reset	System reset
core_reset	Internal reset to sub modules
baud_rate_cm	Cycle machine clock to sub modules
baud_rate_br	Clock to serial transmission
baud_rate_br_trans	Auxiliary clock to serial transmission
core_sfr_read, core_sfr_write	Control signals to SFR read and write operations
core_rom_read	Control signal to ROM memory read
core_ram_read, core_ram_write	Control signals to RAM memory read and write operations

Table 11 – Critical Nets