REVIEW	***1***
Project: EMC08 - Digital	**Author:** Thiago Santos
Subject: Project Definitions	**Date:** 18/08/2010
Local: Digital A lab	**Team Leader:** Vinícius Amaral

Participants:

Name	Group	Name	Group
Vinícius		Eloi	
Jonatas		Inácio	
Thiago		Dino	
Valéria		Julierme	
Pedro		Gabriela	
Hugo			
Marcelo			
Felipe			
Liz			
Harney			

Issues Discussed:

Item	Actions	Responsible	Date
1	**Verilog Code Convention presented** - file must be sent to redmine.	Vinicius, Pedro, Thiago	18/08
2	**Specman Code Convention** - to be defined	Dino, Harney	20/08
3	**Cycle Machine Policy** Every module receives a cycle machine cycle (block_name_cm_i) from Baud Rate module, with 50% of duty cycle.	Thiago, Pedro, Dino	-
4	**SFR Read Policy** Machine Cycle high level	Thiago, Pedro, Vinícius	-
5	**SFR Write Policy** Machine Cycle Falling Edge (1 clock cycle)	Thiago, Pedro, Vinícius	-
6	**Cycle Machine** Initial definition: 4 Clock Cycles for cycle machine To be confirmed latter	Thiago, Pedro, Vinícius	20/08
7	**Define "Block not Completed Verified"** Post an issue in redmine	Vinícius	18/08
8	**Bus Control Function** Remains out of Core and with same functions Reason: core needs 1 CM to read/write in SFR regs.	Jonatas, Gabriela	

Related Documents:	EMC08_digA_verilog_conventions.pdf		

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