DAT105 Computer Architecture
Study Period II, 2017
Department of Computer Science and Engineering
Chalmers University of Technology, Göteborg, Sweden

Laboratory Assignment 1 - Competition
Exploring the Impact of Cache Hierarchy on Processor Performance

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Target:
This part of the lab assignment is designed as a competition among lab groups. Similar to the main assignment, the target is to design a cache architecture that maximizes the performance. The focus is on the data cache.

Applications:
The application is a matrix multiplication:

$$A \times B = C$$

Each matrix has a size of 200×200 double integers. There is a technique called blocked matrix multiplication that improves cache performance by improving the locality. You are provided two applications: "blocked_matrix_mult_1block" and "blocked_matrix_mult_4block". The former performs the calculation as a one single block i.e. a normal matrix multiplication. The latter divides each matrix into blocks of size 100×100 elements and then performs the blocked calculation[1].

Description:
You start with the base configuration provided for the lab1-competition. Using the insights you gained from the main lab assignment and the information about the applications, you should find an optimum configuration for each application that maximizes the performance.
You should only change the configuration of the level1 data cache. However, to have a more realistic trade-off, you must also change the cache access latency according to the following table:

Cache size	≤8KB	≤64KB	≤512KB	≤4MB	≤8MB
Latency (cycles)	1	2	3	4	5

Results:
You should write a 1 page report similar to the main assignment. You can also have a 1 page appendix if you want. You will upload the report along with the two final configuration files on pingpong

Deadline:
The same as the main assignment1

[1] You can find more information about this on the internet