UNIVERSIDADE FERDERAL DE CAMPINA GRANDE

Training in Digital Microelectronics – Functional Verification (UVM) and Design

Professor: Sr.Marcos Morais and Sr.Elmar Melcher

Weekly report

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1. OBJETIVO

Solve design and verification problems using the knowledge taught during training. Using the SystemVerilog HDL Language.

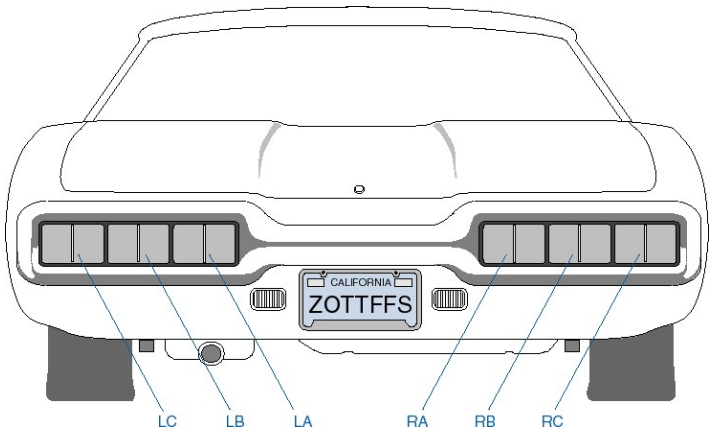
2. FERRAMENTAS UTILIZADOS

- X2GO - Client
- XCELIUM
- REDHAT
- Arquivo UVM_Steps.tgz

3. PROJECT THUNDERBIRD TURN SIGNAL

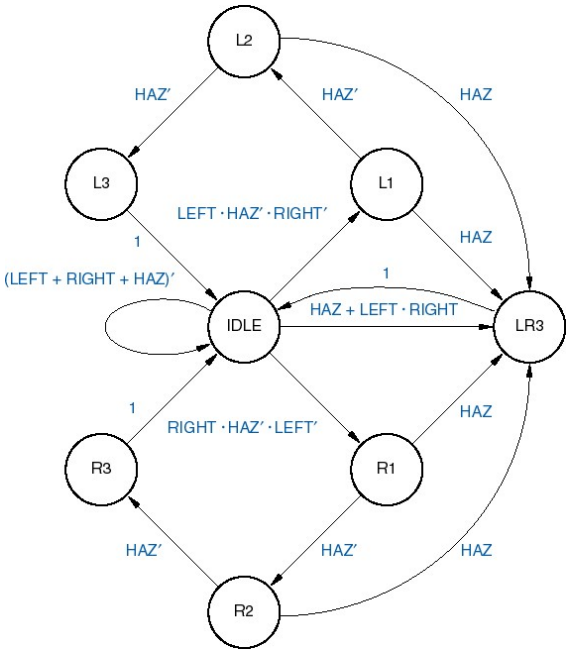
I designed a finite state machine in SystemVerilog to control the taillights of a 1965 Ford Thunderbird. There were three lights on each side that operate in sequence to indicate the direction of a turn. The sequence was designed to complete even when the button was released during it. If none of the buttons or both left and right button were pressed in initial states, no lights were turned on.

Figura 1 – THUNDERBIRD lights



Fonte: personal archive

Figura 2 – FSM, State Diagram



Fonte: Acervo pessoal

- **Use enumerated types for the states**
- **Use time value suffixes for time values and assume a complete(uninterrupted) turning sequence should take two seconds**
- **User parameters and local parameters where/if appropriate**
- **In the testbench print the name of the state the FSM is in at every statechange**

4. Simulation

My simulation only test the state since that's the only part of the circuit which involves conditional adapatative logic.

5. Conclusion

The codes can be found at:
https://github.com/pedrohfmacedo/hardware_project/tree/main/project_01