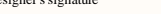


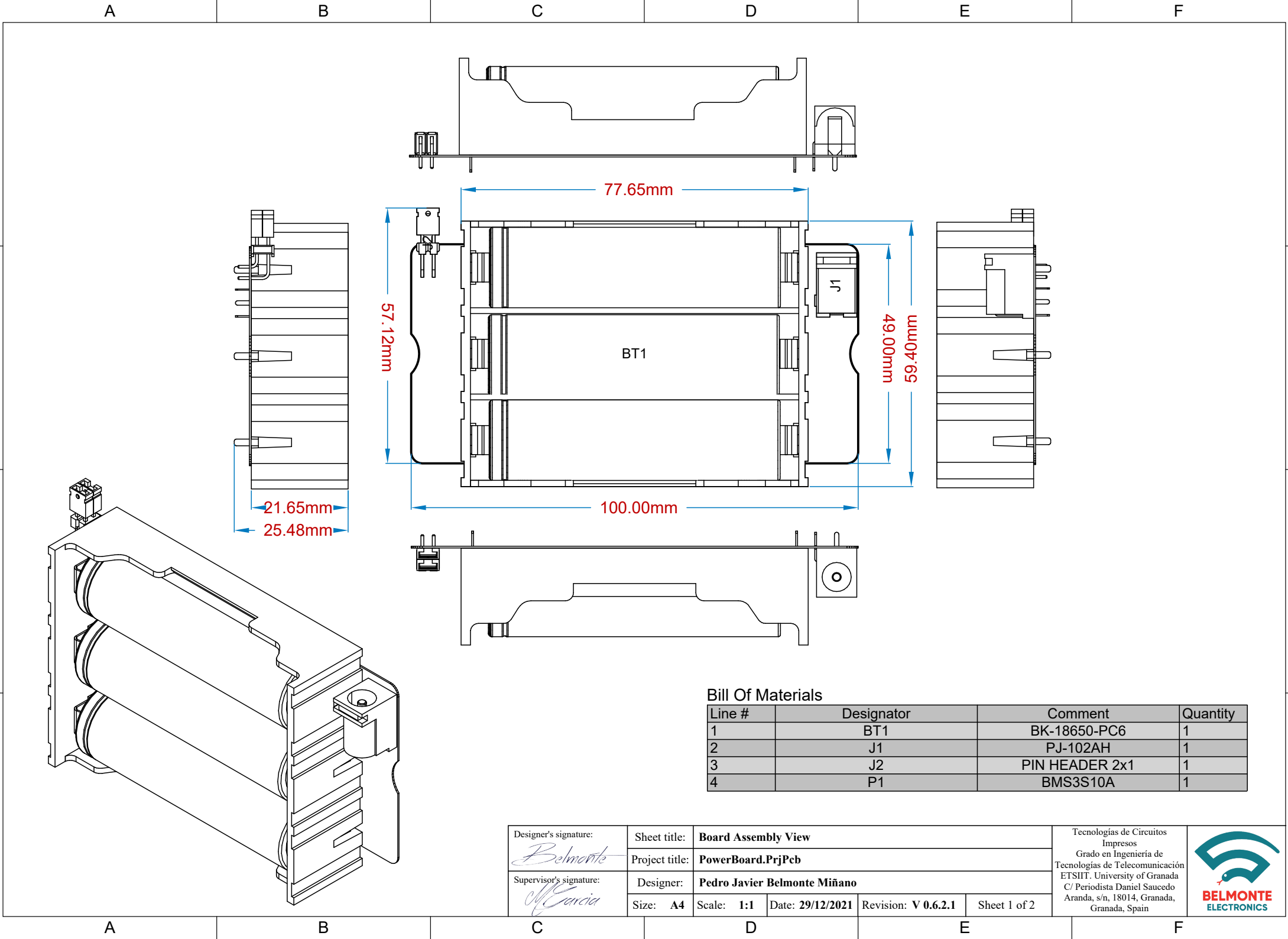


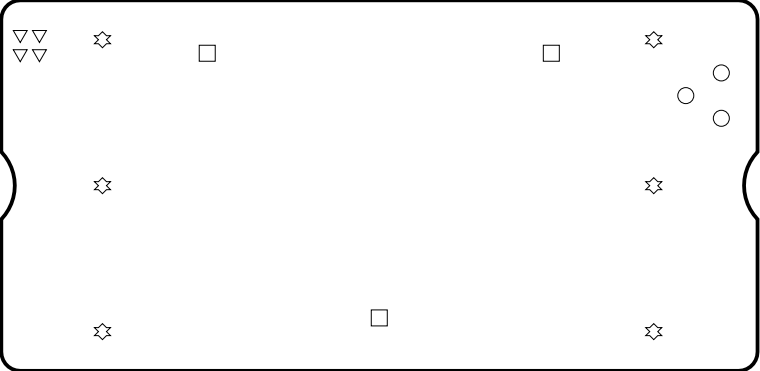
Designer's signature 	Sheet title: <b>Bottom Board</b>			<div>Tecnologías de Circuitos Impresos Grado en Ingeniería de Tecnologías de Telecomunicación ETSIT. University of Granada C/ Periodista Daniel Saucedo Aranda, s/n, 18014, Granada, Granada, Spain</div> 
	Project title: <b>Balancing Robot</b>			
Supervisor's signature 	Designer: <b>Pedro Javier Belmonte Miñano</b>			
	Date: <b>29/12/2021</b>	Revision: <b>V 0.6.2.1</b>	Sheet 1 of 1	



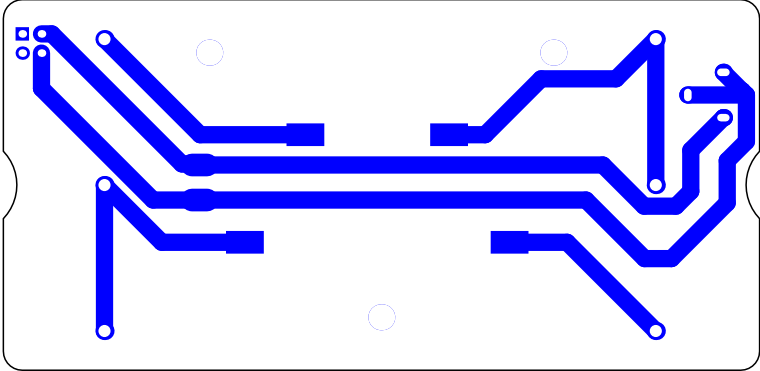
Top Layer



Drill Drawing View



Bottom Layer



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
○	3	1.00mm	Plated	
▽	4	1.02mm	Plated	
☆	6	1.60mm	Plated	
□	3	3.44mm	Plated	
	16 Total			

