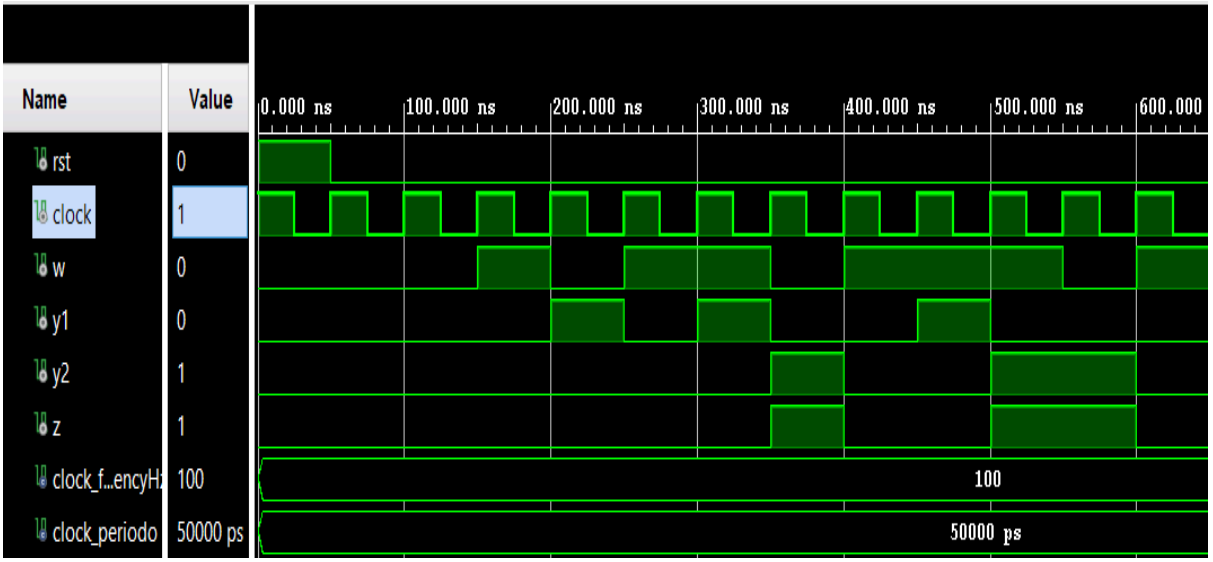
01.
Arquivos VHDL'S

02.



03.
a)

	PRÓXIMO ESTADO								
ESTADO	W=0	W=1	R1 Out	R1 In	R2 Out	R2 In	R3 Out	R3 In	Done
A	A	B	0	1	0	0	1	0	1
B	C	C	0	0	1	0	0	1	0
C	A	A	1	0	0	1	0	0	0

b)

	ATUAL		W=0	w=0	w=1	w=1
	y1	y2	y1	y2	y1	y2
A	0	0	0	0	0	1
B	0	1	1	0	1	0
C	1	0	0	0	0	0
–	1	1	–	–	–	–

c)

Y1:

	y1y2	y1y2	y1y2	y1y2
	00	01	11	10
W=0	0	1	–	0
W=1	0	1	–	0

Y2:

	y1y2	y1y2	y1y2	y1y2
	00	01	11	10
W=0	0	0	–	0
W=1	1	0	–	0

d)

e)