Folha 3

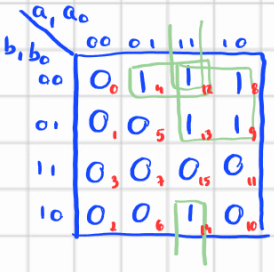
2

b) XOR, é apenas construido com a mesma porta lógica (NAND) mas é mais lento

3

a_1	a_0	b_1	b_0	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

SoP: $\overline{a_1}\, a_0\, \overline{b_1}\, b_0 + a_1\, \overline{a_0}\, \overline{b_1}\, \overline{b_0} + a_1\, \overline{a_0}\, \overline{b_1}\, b_0 + a_1\, a_0 \overline{b_1}\, \overline{b_0} + a_1\, a_0\, \overline{b_1}\, b_0 + a_1\, a_0\, b_1\, \overline{b_0}$



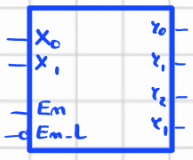
$F = a_1\, \overline{b_1} + a_0\, \overline{b_1}\, \overline{b_0} + a_1\, a_0\, \overline{b_0}$

6

$S = a \oplus b \oplus cin$

$Cout = ab + a\,cin + b\,cin$

7



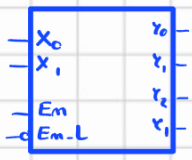
Em	Em_L	X_1	X_0	Y_3	Y_2	Y_1	Y_0
0	X	X	X	0	0	0	0
1	1	X	X	0	0	0	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	1	0	0	0

$Y_0 = Em\, \overline{Em\_L}\, \overline{X_1}\, \overline{X_0}$

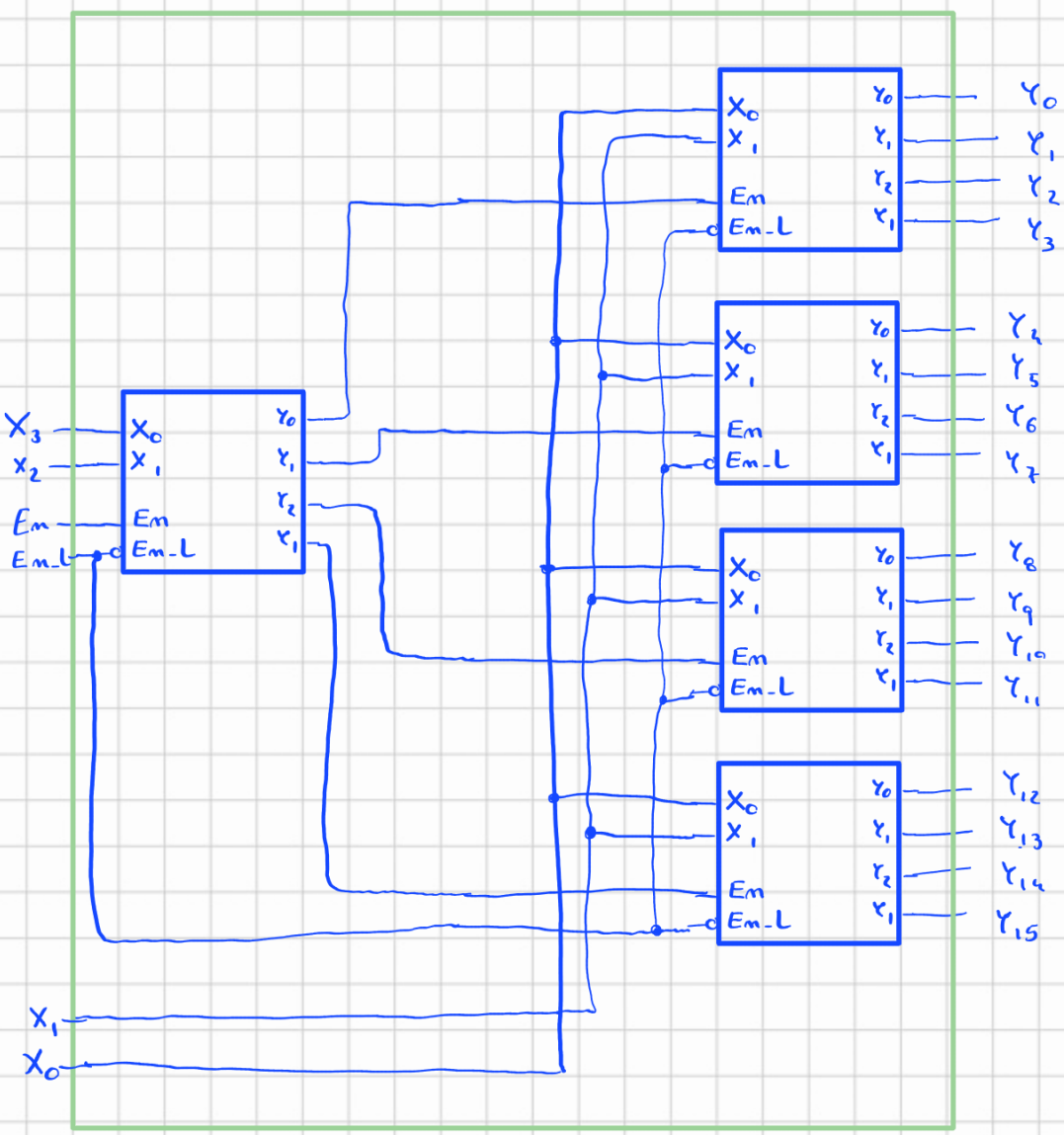
$Y_1 = Em\, \overline{Em\_L}\, \overline{X_1}\, X_0$

$Y_2 = Em\, \overline{Em\_L}\, X_1\, \overline{X_0}$

$Y_3 = Em\, \overline{Em\_L}\, X_1\, X_0$



X_3	X_2	X_1	X_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0																1
0	0	0	1															1	
0	0	1	0														1		
0	0	1	1													1			
0	1	0	0												1				
0	1	0	1											1					
0	1	1	0										1						
0	1	1	1									1							
1	0	0	0								1								
1	0	0	1							1									
1	0	1	0						1										
1	0	1	1					1											
1	1	0	0				1												
1	1	0	1			1													
1	1	1	0		1														
1	1	1	1	1															



$f(A,B,C,D) = \bar{A}BC + AD + AC$

$\bar{A}BC$: 011 → 0110 ou 0111

AD: 01 → 0001 - 1, 0011 - 3, 0101 - 5, 0111 - 7

AC: 01 → 0010 - 2, 0011 - 3, 0110 - 6, 0111 - 7

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1