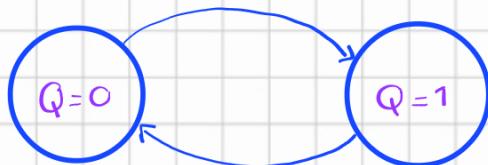


Folha 4

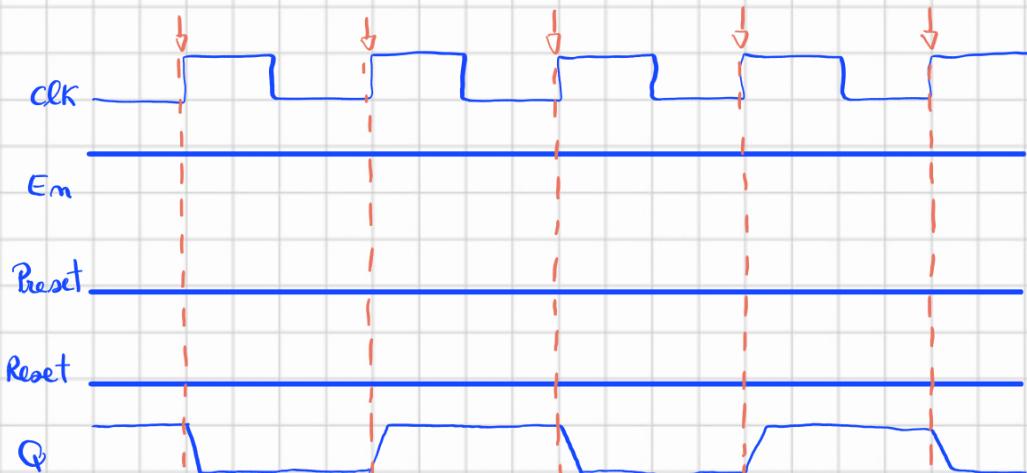
1

a)



Em	Preset	Reset	Q_{ant}	Q	Q
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	1	1	1
1	0	0	1	1	0
1	0	1	0	0	0
1	1	0	1	0	0
1	1	1	1	1	1

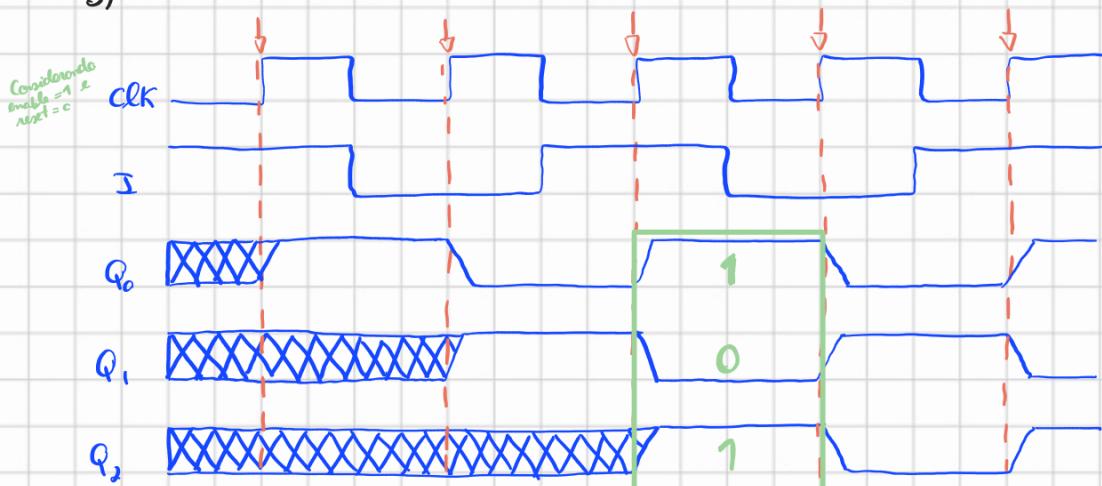
b)



2

a) A saída Q_{ant} será igual à saída Q_m quando o clock transita de 0 para 1

b)



(com 3 ciclos de

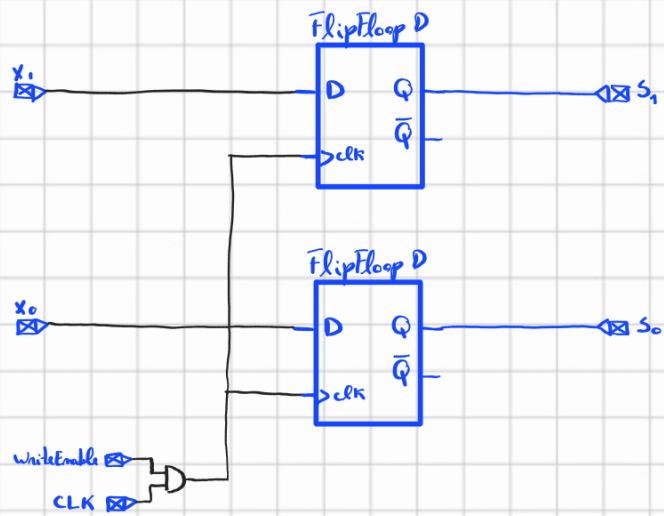
c) Porque a cada transição de 0 para 1 do clock os bits das saídes Q_0, Q_1, Q_2 transitam para a direita, e na entrada Q_0 entra I

clock consigo $Q_0 = 1$

e $Q_1 = 0$ e $Q_2 = 1$

3

a)

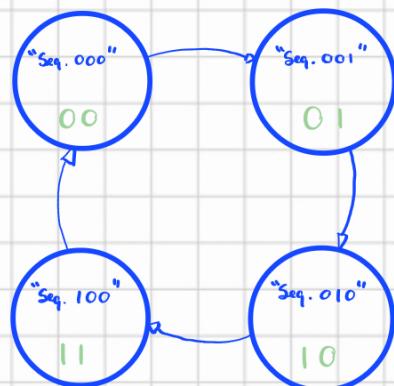


4

4.1

P1

4 estados $\Rightarrow \lceil \log_2 4 \rceil = 2$ bits de estado



P2

Estado - Atual		Estado - Seguinte	
Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

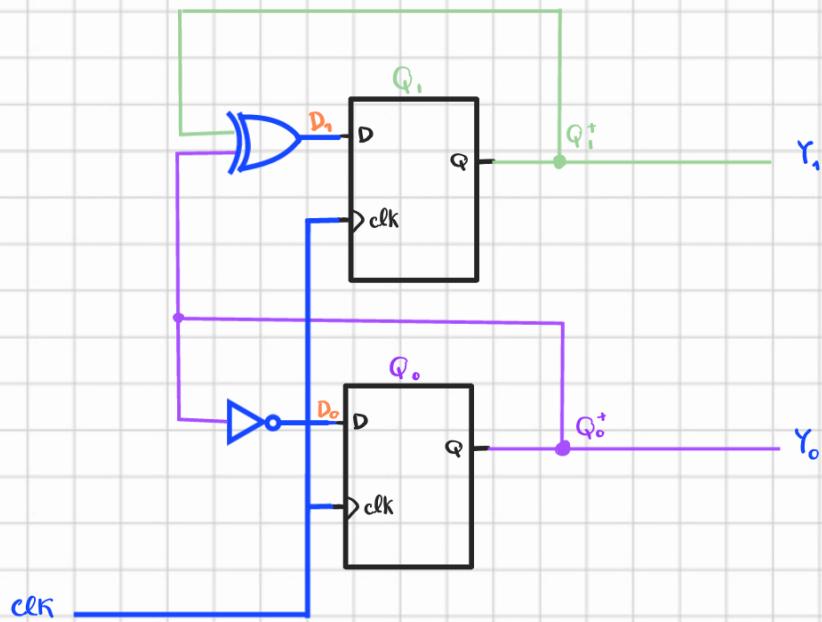
P3

Estado - Atual		Entradas D	
Q_1	Q_0	D_1	D_0
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

P4

$$D_1 = Q_1 \oplus Q_0$$

$$D_0 = \overline{Q_0}$$



P5

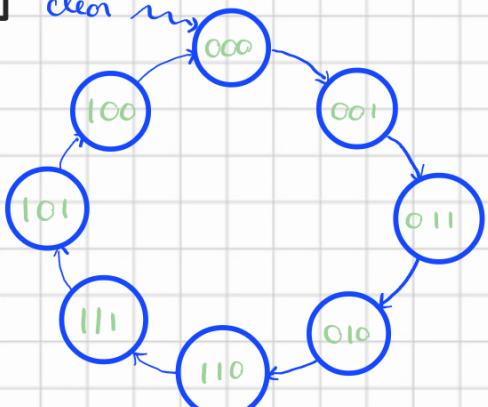
Estado - Atual		Saídos		
Q1	Q0	S2	S1	S0
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

$$S_2 = Q_1 Q_0$$

$$S_1 = Q_1 \overline{Q_0}$$

$$S_0 = \overline{Q_1} Q_0$$

4.2

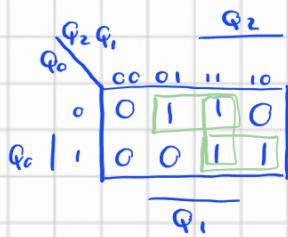


8 estados \Rightarrow 3 bits de estado

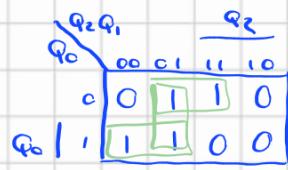
a)

Estado - Atual			Estado - Seguinte		
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	1

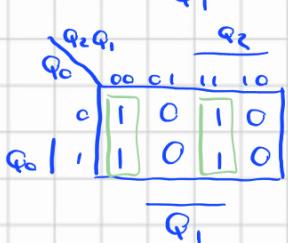
Estado - Atual			Entradas D		
Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	1



$$D_2 = Q_1 \overline{Q}_0 + Q_2 Q_0$$

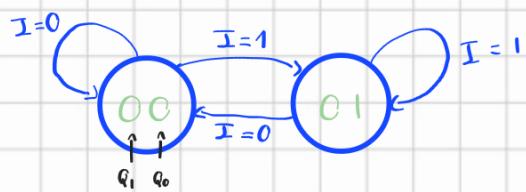


$$D_1 = Q_1 \overline{Q}_0 + \overline{Q}_2 Q_0$$



$$D_0 = \overline{Q}_1 \overline{Q}_2 + Q_1 Q_2 = \overline{Q}_1 \oplus Q_2$$

5



Nota: como o circuito começa
no estado 00, o estado 11 e 10 nunca
vai ser atingido.