

Introduction to Digital Systems

Part III (Sequential Components)

2022/2023

Sequential Logic Fundamentals and Basic Circuits

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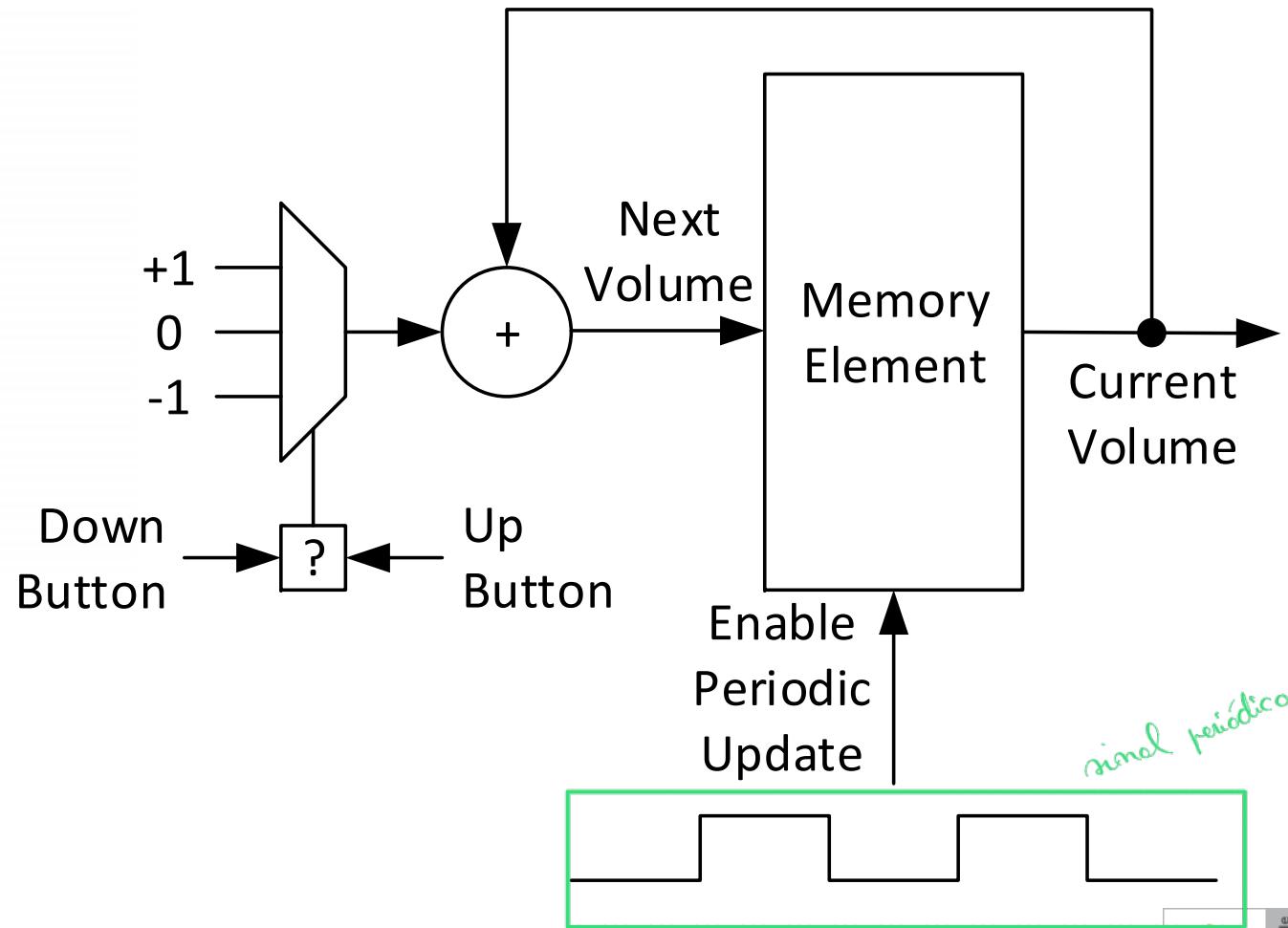
Lecture Contents

- Sequential logic circuits fundamentals
 - Motivation and concepts
- Sequential logic basic circuits (memory elements built with ordinary gates and feedback loops)
 - S-R Latch
 - D Latch
 - D Flip-flop



Figures and most content extracted from: John F. Wakerly, “Digital Design – Principles and Practices”, 4 ed., Pearson – Prentice Hall, 2006 (chapter 7). Reading chapter 7 (4th ed.) or chapter 10 (5th ed.) is highly recommended.

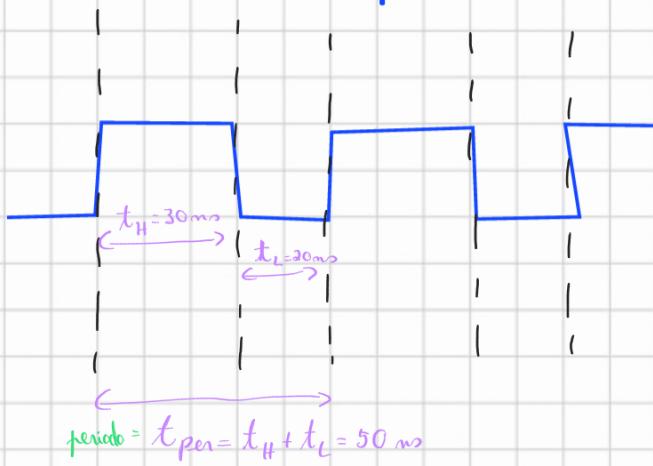
Sequential Circuit Example



Introduction

- **Combinational** logic circuit
 - Is one whose outputs depend only on its current inputs
- **Sequential** logic circuit
 - Is one whose outputs depend not only on its current inputs, but also on the past sequence of inputs, possibly far back in time
- **State** of a sequential circuit
 - Is a collection of state variables whose values at any one time contain all the information about the past, necessary to account for the circuit's future behavior
- N-bit state variable: 2^N maximum number of states

Sinal periódico



$$\text{freq} = \frac{1}{t_{per}} = \frac{1}{50 \text{ ms}} = \frac{1}{50 \times 10^{-3} \text{ s}} = \frac{10^3}{50} \text{ Hz} = \frac{10^3 \times 10^6}{50} \text{ Hz} = 20 \text{ MHz}$$

$$\text{ms} \longleftrightarrow \text{MHz} \Rightarrow \frac{1000}{\text{ms}}, \text{ e.g. } \frac{100\%}{5\%} = \frac{100}{5} = 20 \text{ MHz}$$

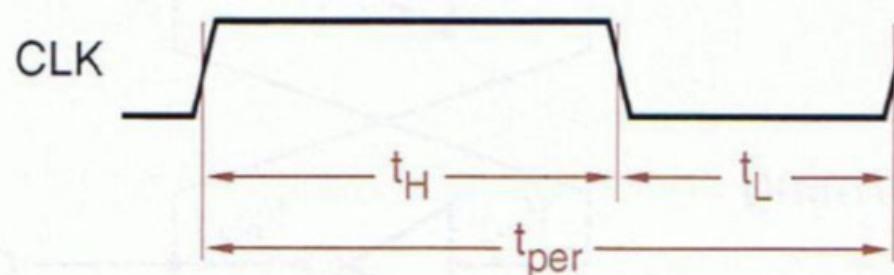
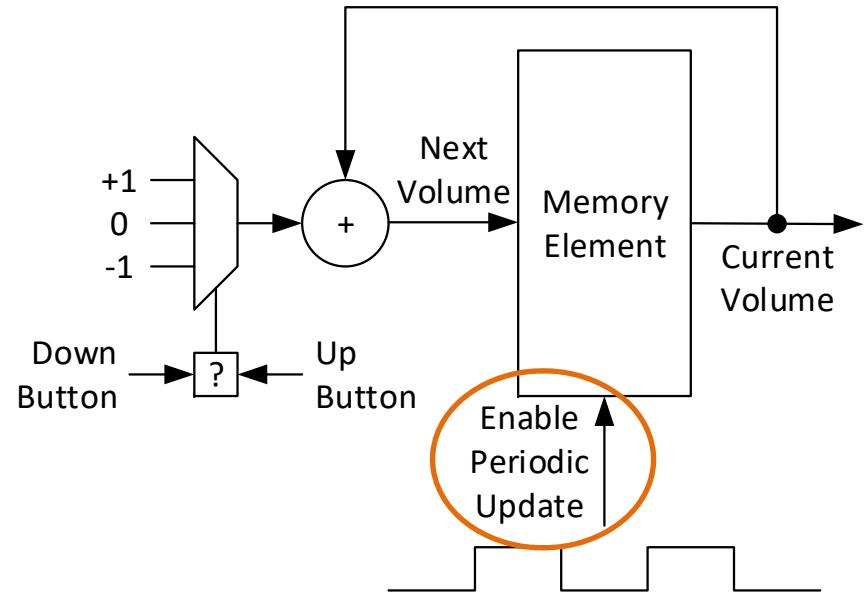
% de tempo que está ativo

$$\text{duty cycle} = \frac{t_H}{t_{per}} \times 100\% = \frac{30 \text{ ms}}{50 \text{ ms}} \times 100\% = 60\%$$



Clock Signals

- State changes of most sequential circuits occur at times specified by a free-running clock signal
- Active high / active low clock signals



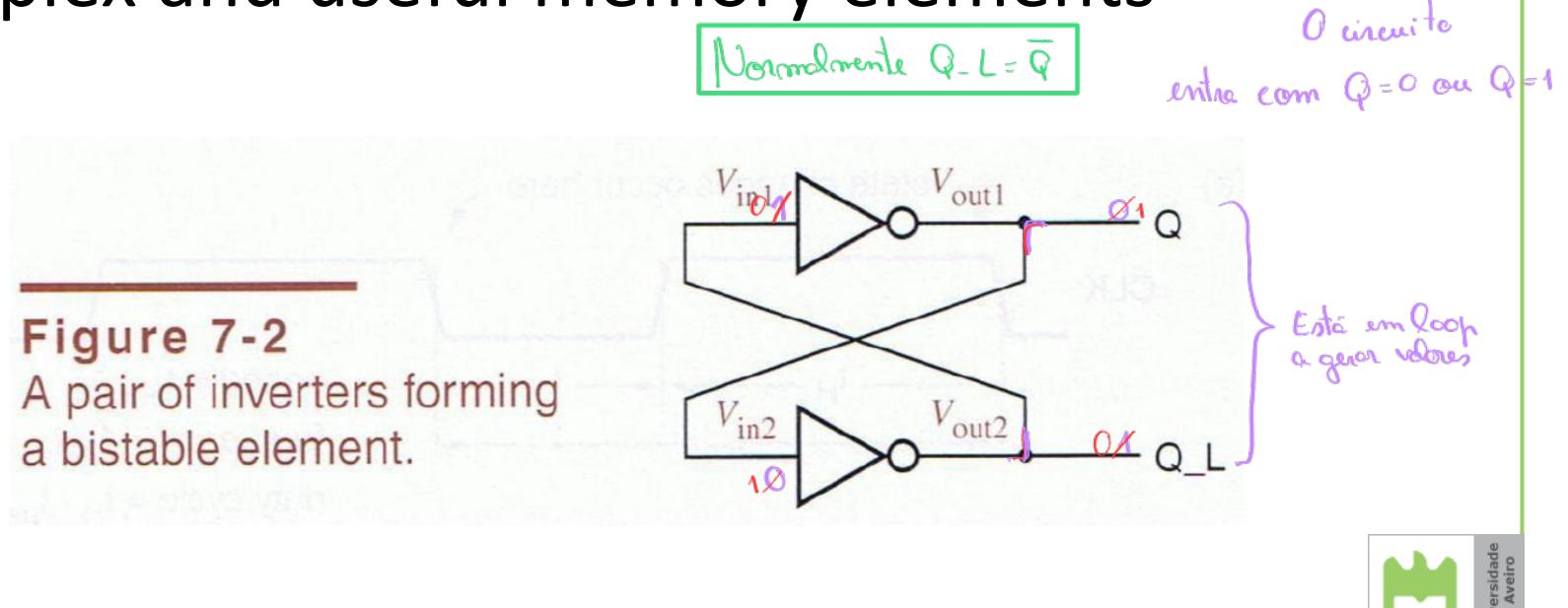
$$\begin{aligned} \text{period} &= t_{per} \\ \text{frequency} &= 1 / t_{per} \\ \text{duty cycle} &= t_H / t_{per} \end{aligned}$$

Figure 7-1
Clock signals:

Bi - estavel

Bistable Element (Basic Structure)

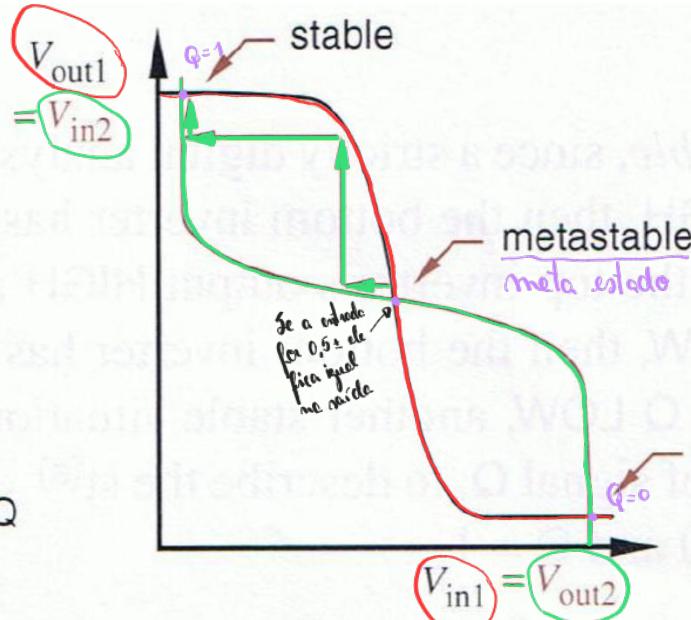
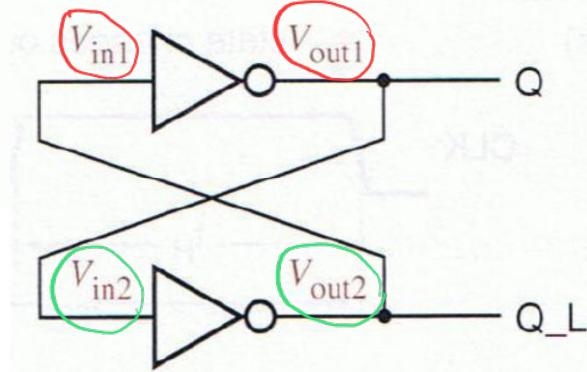
- No inputs and therefore no way of controlling or changing its state (random set at power up)
- Only illustrative but serves the basis for more complex and useful memory elements



Bistable Element (Analog Analysis)

Figure 7-3

Transfer functions for inverters in a bistable feedback loop.



Transfer function:

$$V_{out1} = T(V_{in1})$$

$$V_{out2} = T(V_{in2})$$

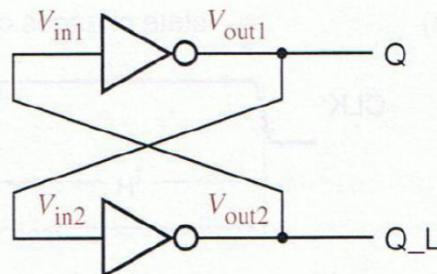
$$\begin{aligned} V_{in1} &= V_{out2} \\ &= T(V_{in2}) \\ &= T(T(V_{in1})) \\ &= T(T(T(V_{in1}))) \end{aligned}$$

3 equilibrium points: 2 stable and 1 metastable

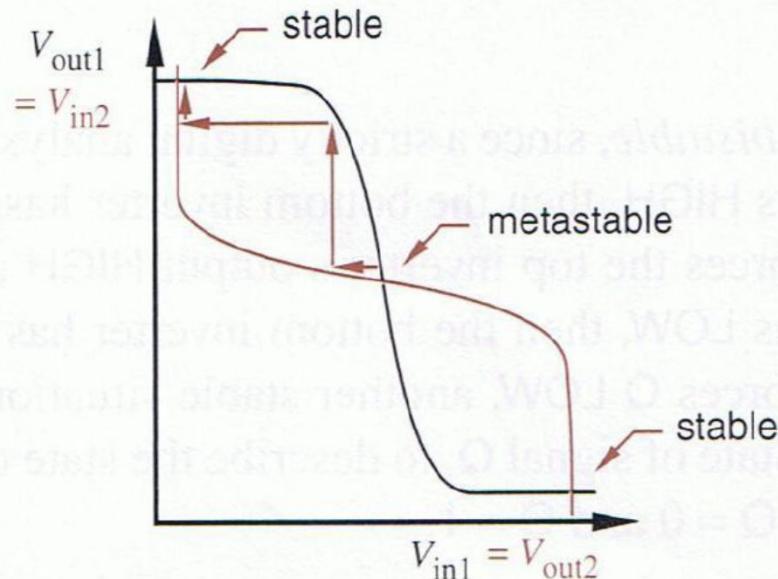
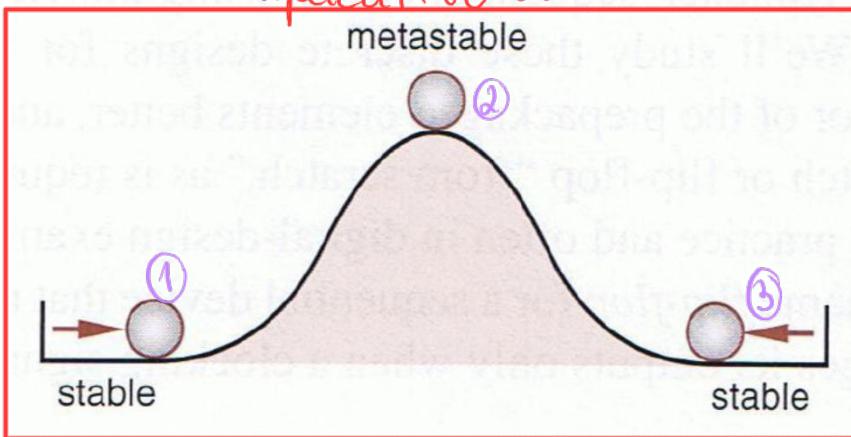
Metastability

Figure 7-3

Transfer functions for inverters in a bistable feedback loop.



Explicativo !!!



Transfer function:

$$V_{out1} = T(V_{in1})$$

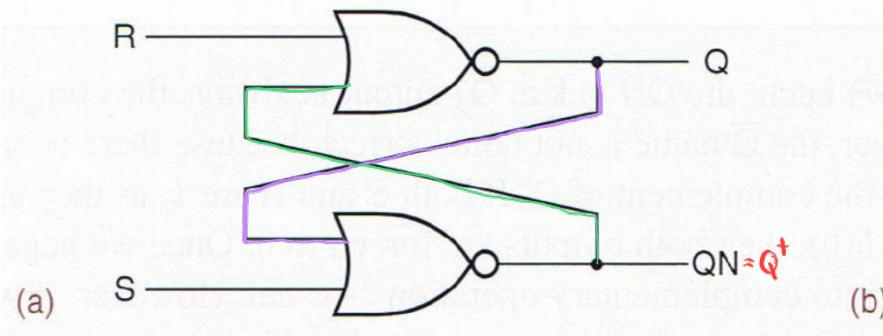
$$V_{out2} = T(V_{in2})$$

Figure 7-4
Ball and hill analogy for
metastable behavior.

Effects of noise and circuit
impairments on metastability

S-R Latch

(Structure and Function Table)



S	R	Q	$QN \approx Q^t$
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

Figure 7-5
S-R latch: (a) circuit design using NOR gates; (b) function table.

São iguais
Problema
Se o utilizador mudar o S e o R para 0, o sistema não estabiliza.
Fica 1/0/1/0/1/0...

Nota: ignoramos um pouco o QN como uma saída!

$Q^t \rightarrow$	Q^s	00	01	11	10
0	SR	0	0	X	1
1		1	1	0	X

$Q^t = S + \bar{R}Q$
Equação característica

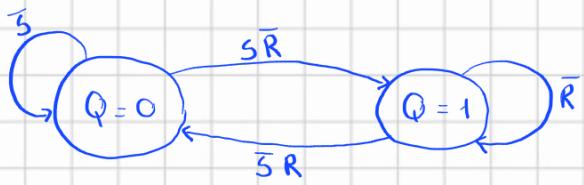
Tabela de Estados

S	R	Q	Q^t	Próximo Q (Q^t ou Q^* ou QN)
0	0	0	0	HOLD (mantém o estado)
0	0	1	1	
0	1	0	0	RESET (estabiliza em 0) Rativo
0	1	1	0	
1	0	0	1	SET (estabiliza em 1) Sativo
1	0	1	1	
1	1	0	X	
1	1	1	X	NOT ALLOWED !

Tabela de excitação

Q	Q^t	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Diagrama de estados - 2 estados ($Q=0$ v $Q=1$)



S-R Latch (Operation/Timing Diagrams)

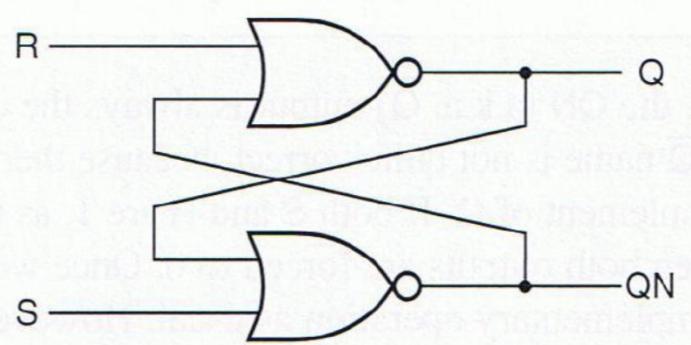
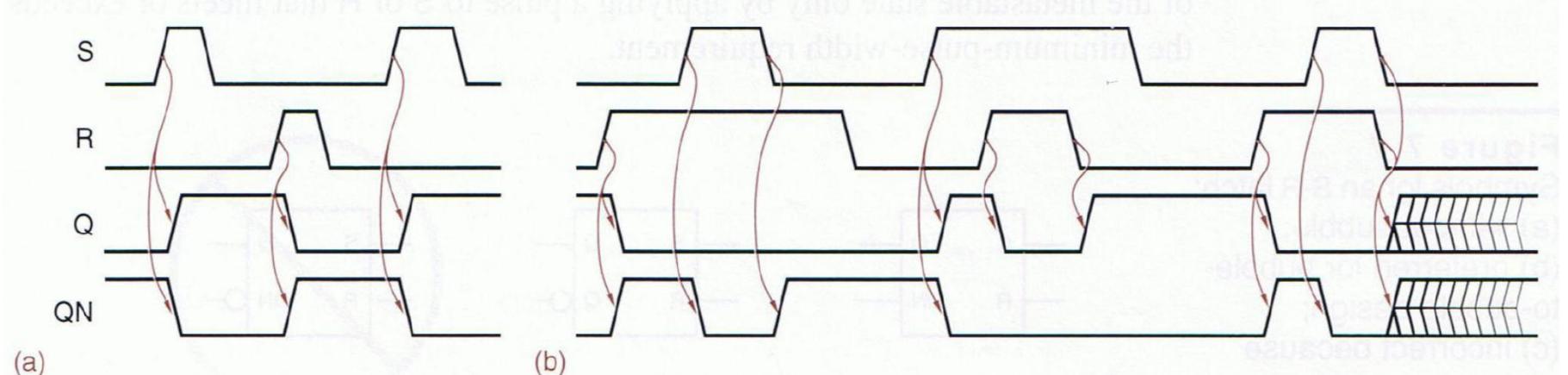
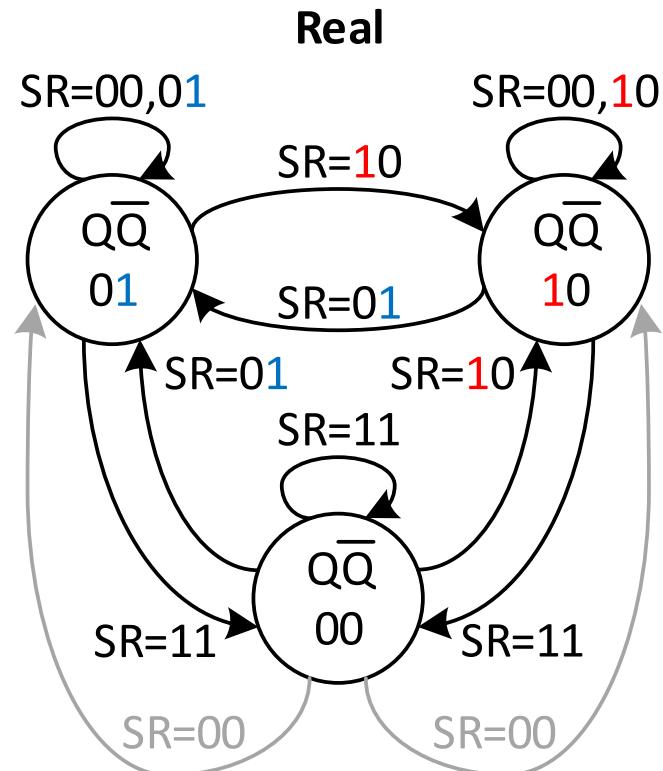
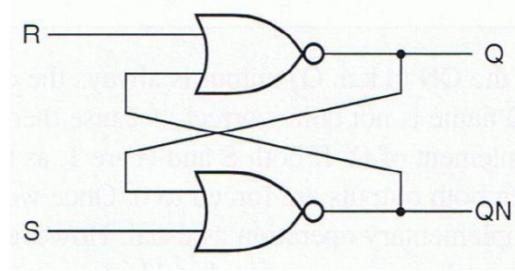
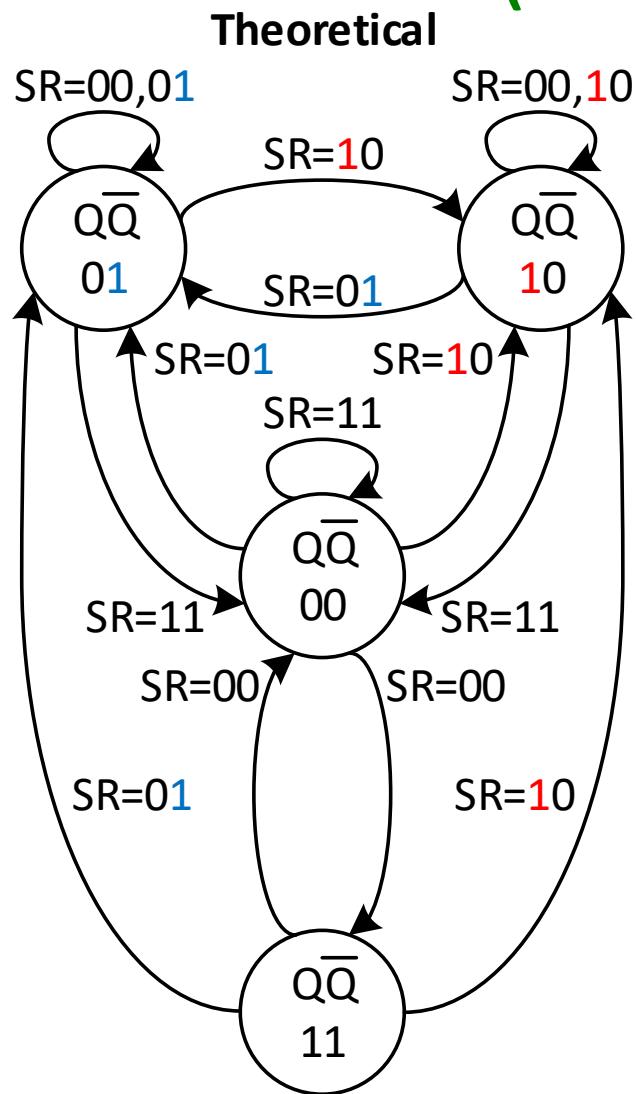


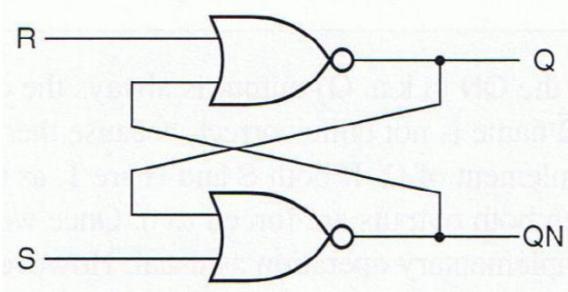
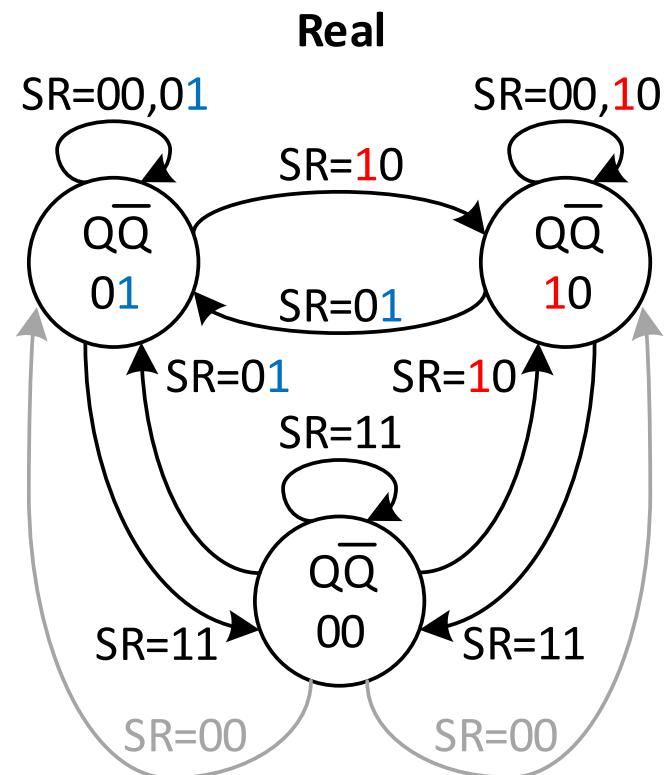
Figure 7-6 Typical operation of an S-R latch: (a) “normal” inputs; (b) S and R asserted simultaneously.



S-R Latch (State Diagram)



S-R Latch (Characteristic Equation)



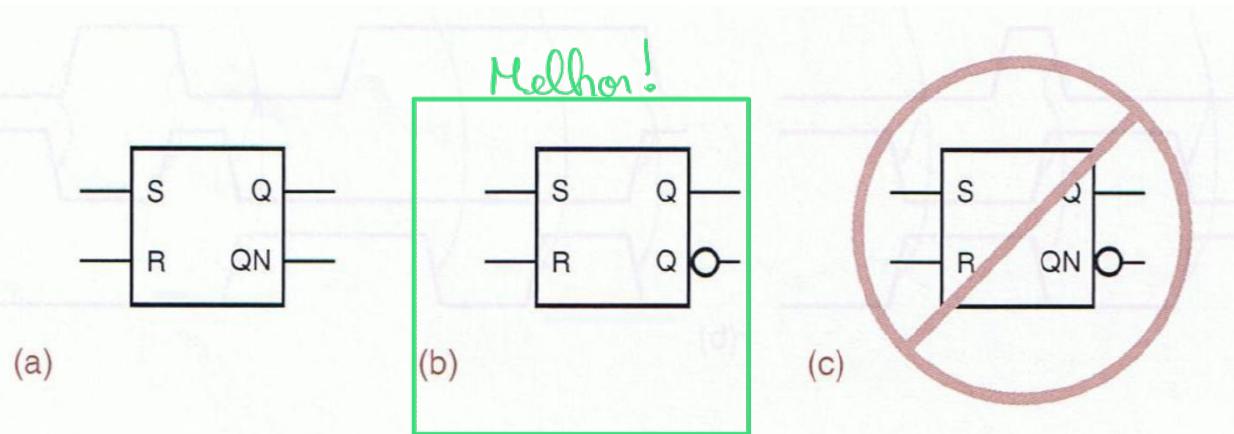
SR	00	01	11	10
Q	0	0	X	1
Q̄	1	0	X	1

$$Q^+ = S + Q \cdot \bar{R}$$

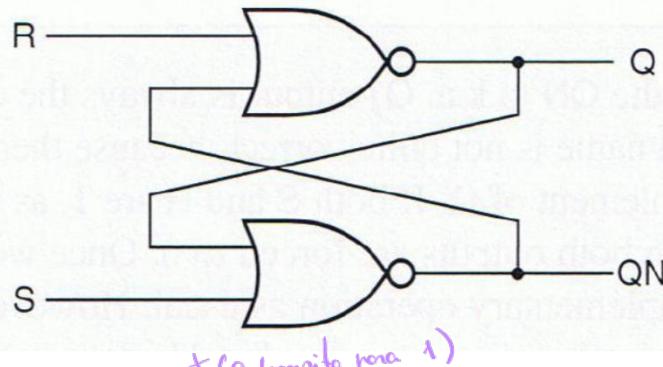
S-R Latch (Symbol)

Figure 7-7

Symbols for an S-R latch:
(a) without bubble;
(b) preferred for bubble-to-bubble design;
(c) incorrect because of double negation.



S-R Latch (Timing Parameters)



- t_{pLH} – propagation time LOW-to-HIGH
- t_{pHL} – propagation time HIGH-to-LOW
- $T_{pw(min)}$ – minimum pulse width

Non-determinism/metastability due to violation of $T_{pw(min)}$

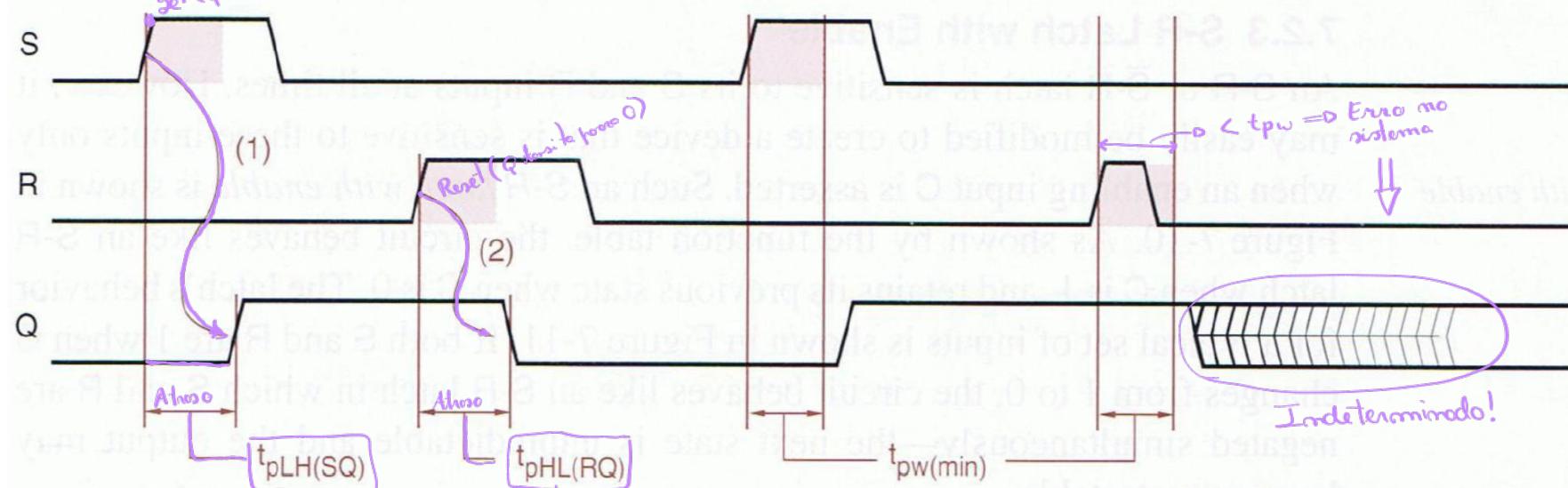
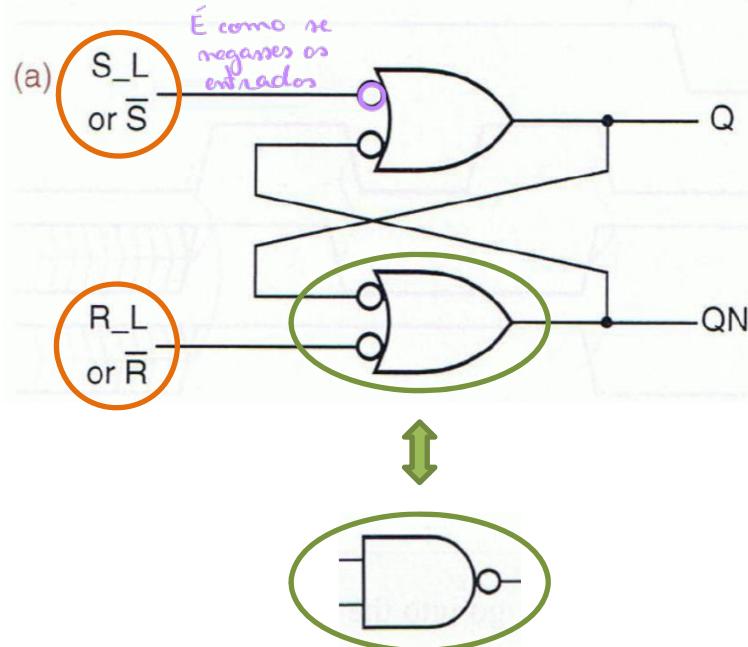


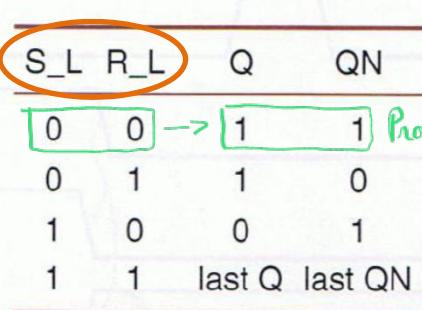
Figure 7-8 Timing parameters for an S-R latch.

S-R Latch (with NAND Gates)

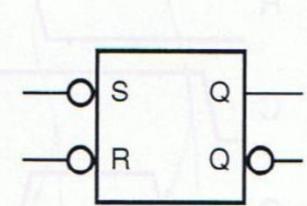
- Entradas negados

Figure 7-9 $\overline{S}\text{-}\overline{R}$ latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.



(b) 

\overline{S}_L	\overline{R}_L	\overline{Q}	\overline{Q}_N
0	0	1	1
0	1	1	0
1	0	0	1
1	1	last \overline{Q}	last \overline{Q}_N



S-R Latch with Enable (C)

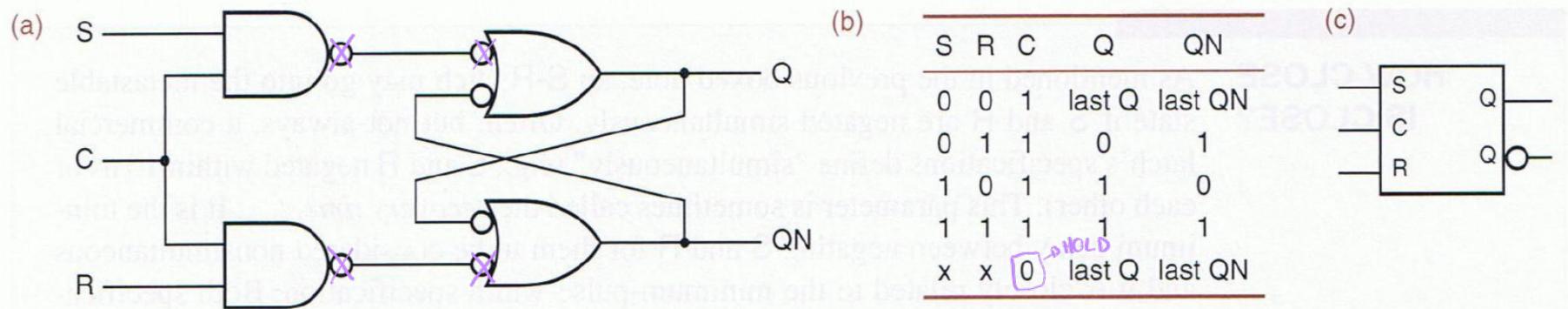


Figure 7-10 S-R latch with enable: (a) circuit using NAND gates; (b) function table; (c) logic symbol.

S-R Latch with Enable (Operation)

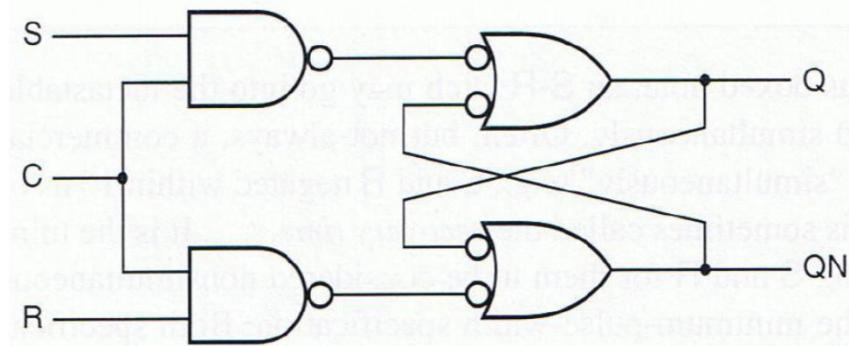
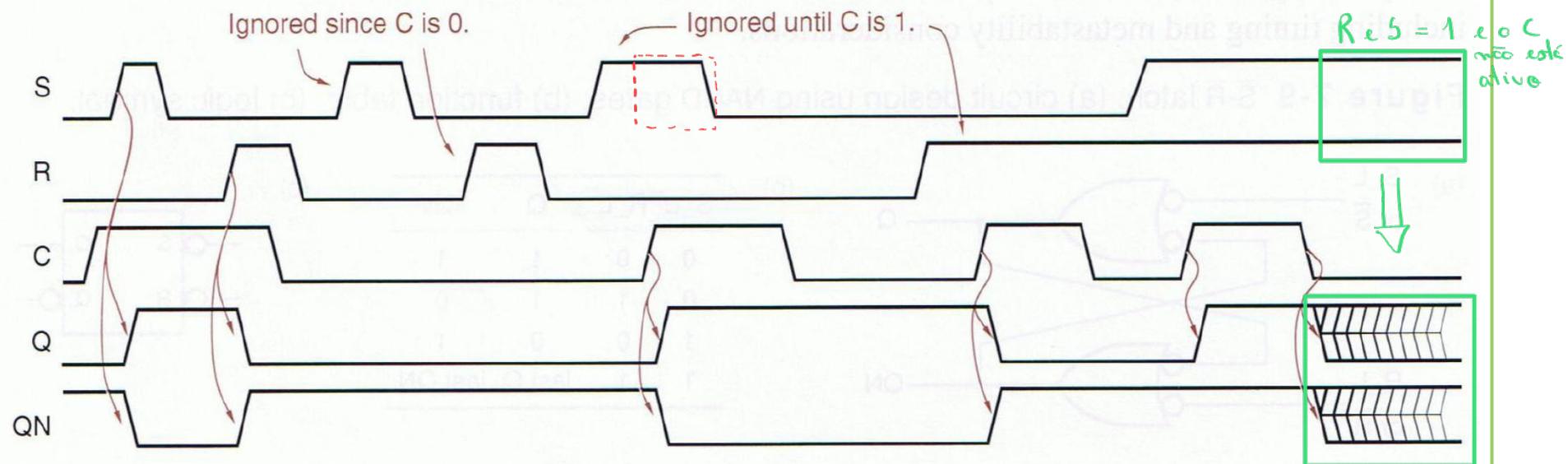


Figure 7-11 Typical operation of an S-R latch with enable.



Latch D

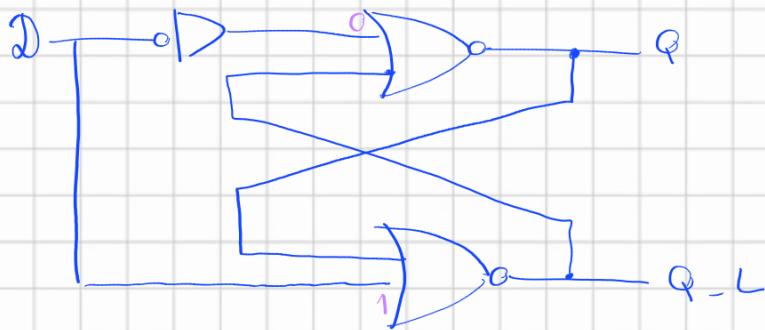


Tabela de estados

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

$Q^+(D, Q) = D$

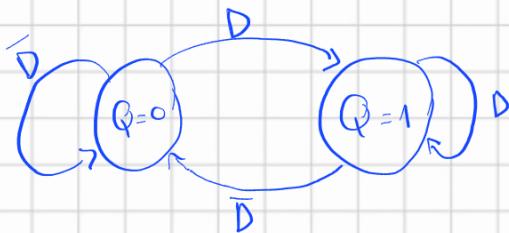
Reset

Set

Tabela de excitação

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

Diagrama de estado



D Latch (Structure and Operation)

→ Com enable (clock)

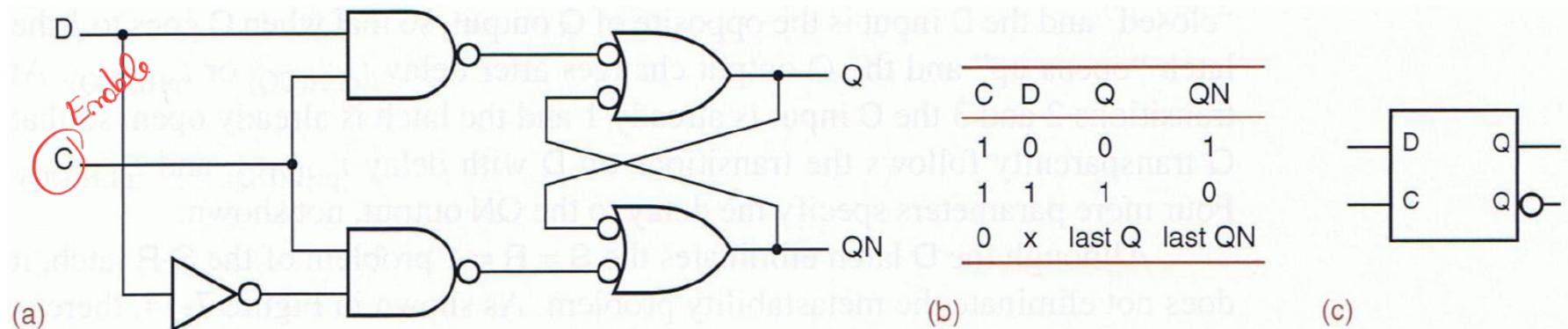


Figure 7-12 D latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.

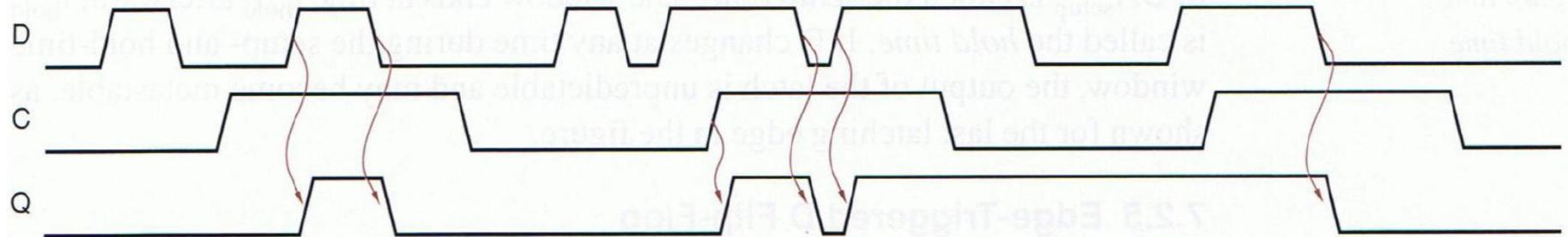
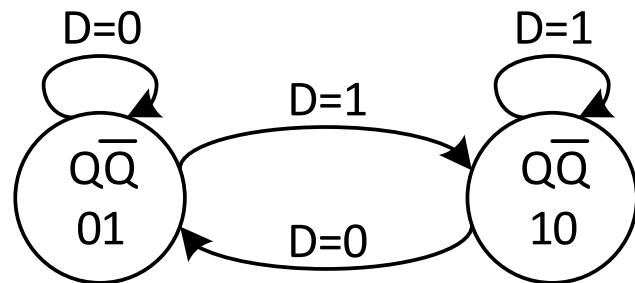
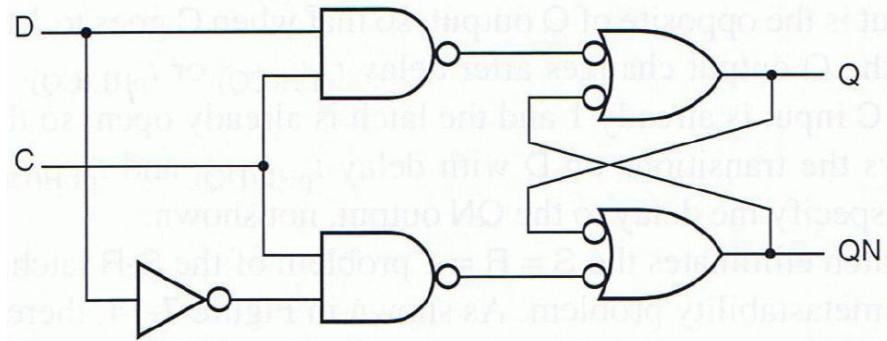


Figure 7-13 Functional behavior of a D latch for various inputs.

D Latch

(State Diagram and Characteristic Equation)



A truth table showing the characteristic equation $Q^+ = D$. The table has four columns corresponding to the inputs D, \bar{C} , \bar{Q} , and $\bar{Q}N$. The rows show the resulting output Q for all combinations of inputs.

D	\bar{C}	\bar{Q}	Q
0	0	1	0
0	1	0	0
1	0	0	1
1	1	1	1

$$Q^+ = D$$

D Latch (Timing Parameters)

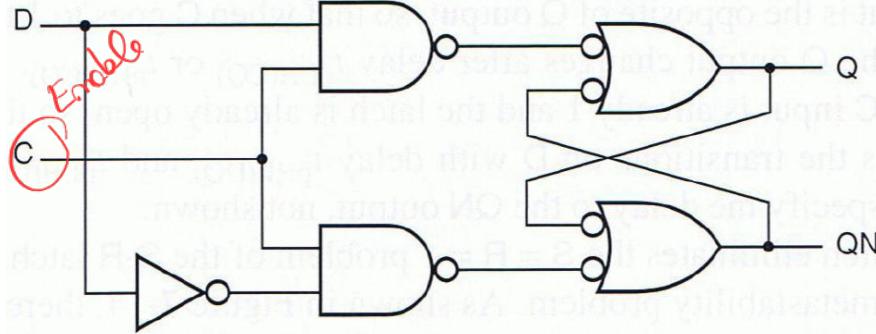
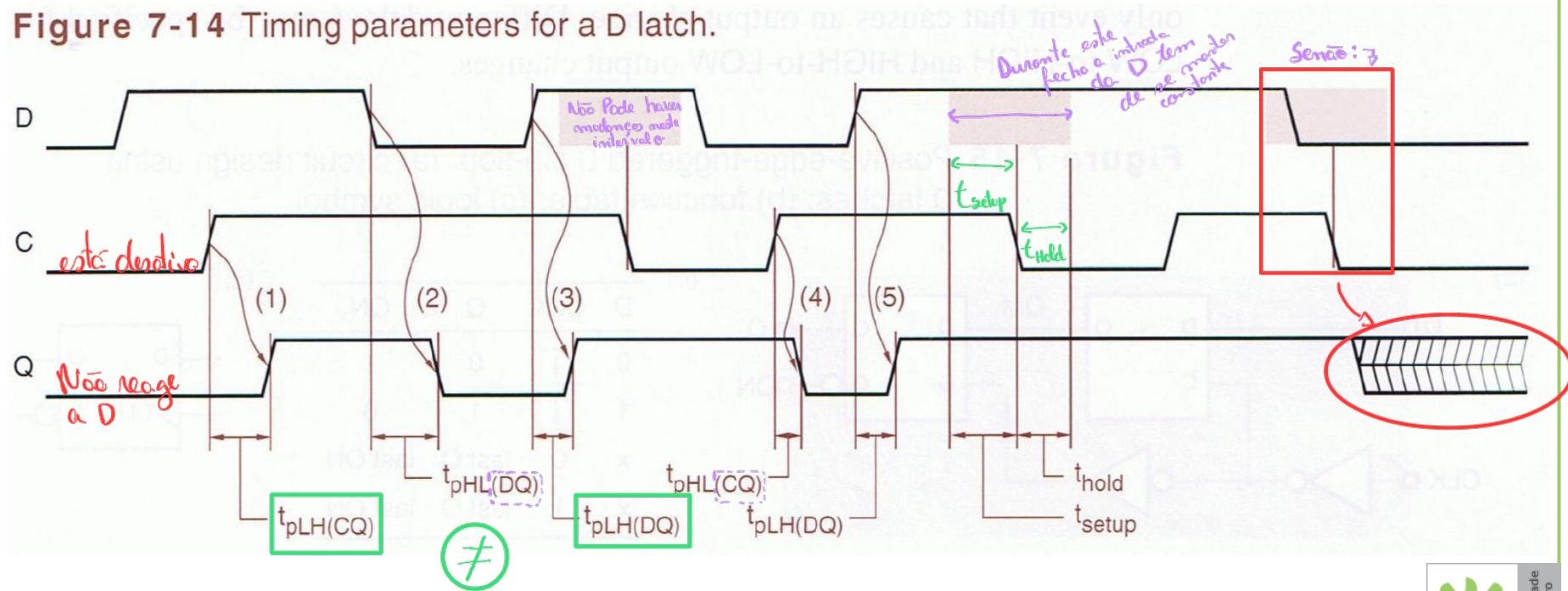
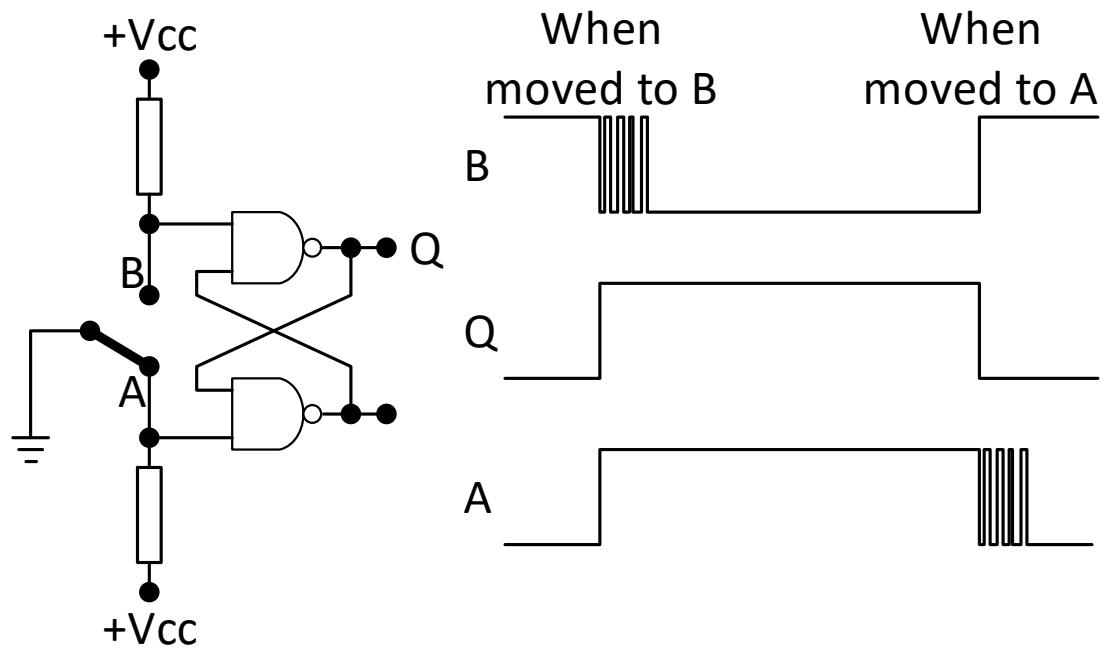
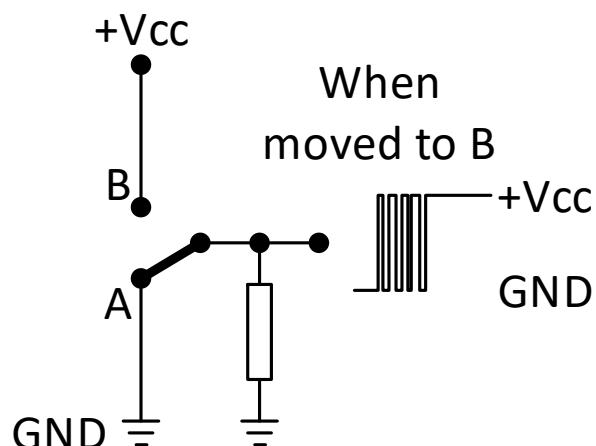


Figure 7-14 Timing parameters for a D latch.

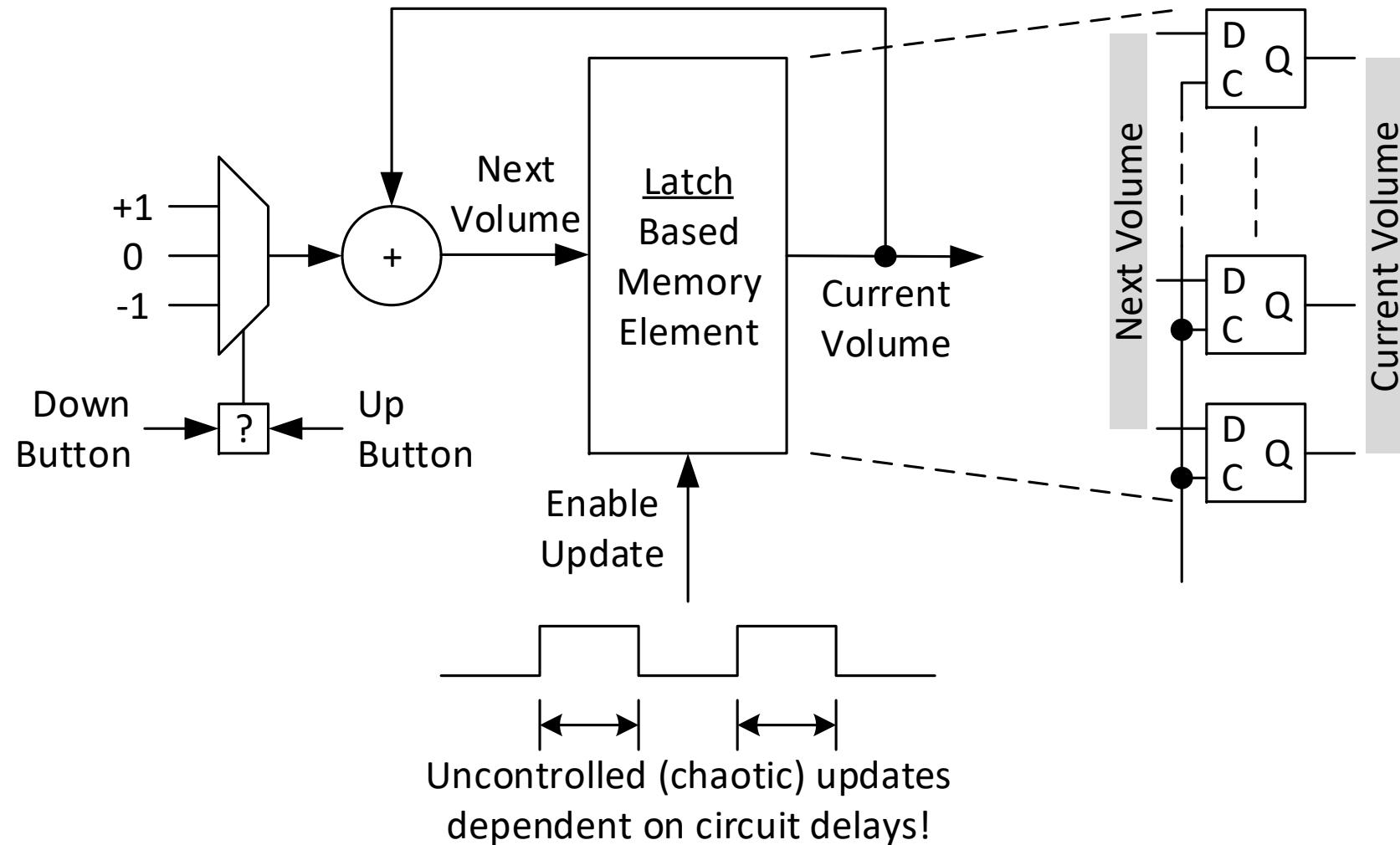


Application Example of an S-R Latch

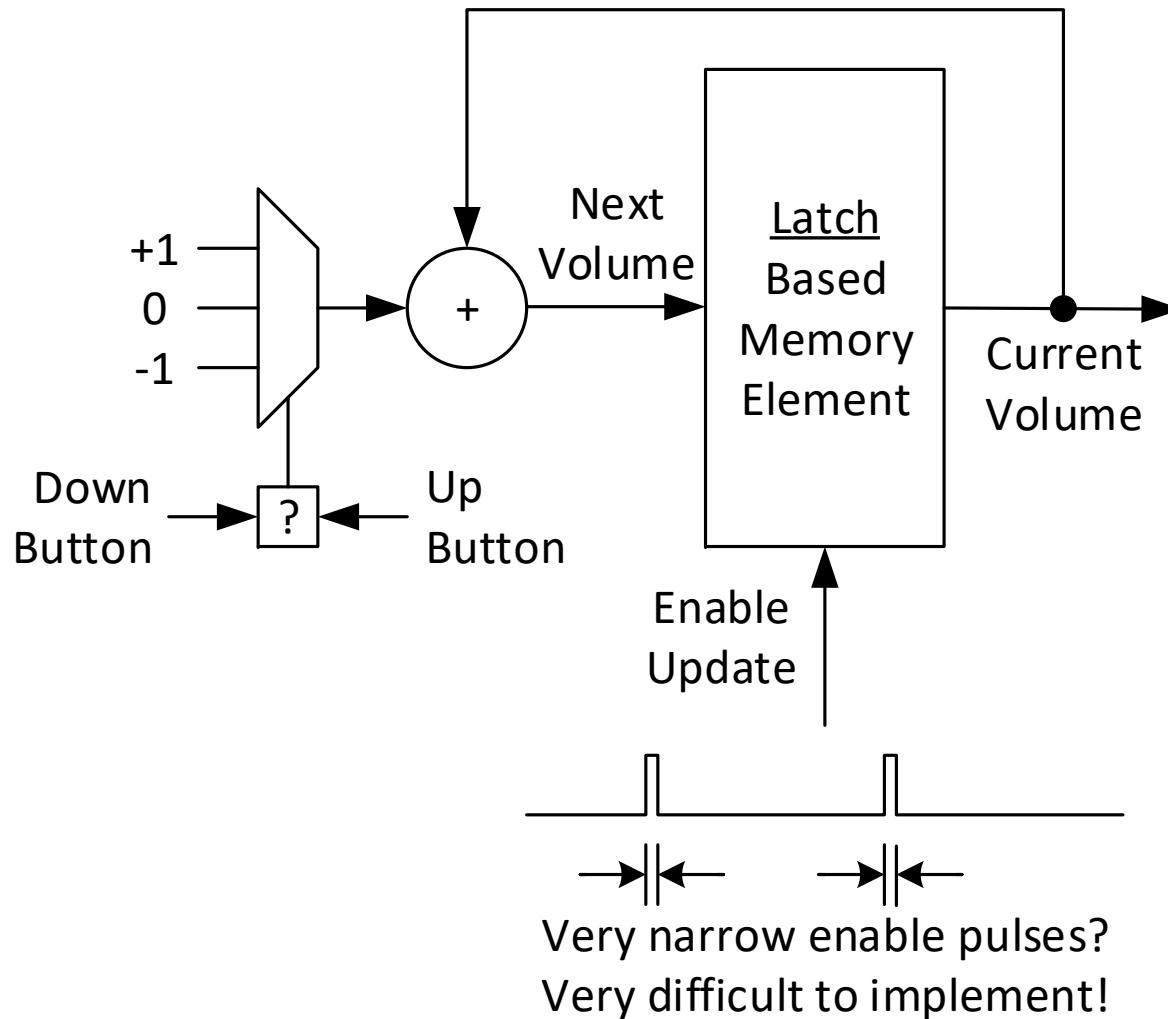
Debounce mechanical switches



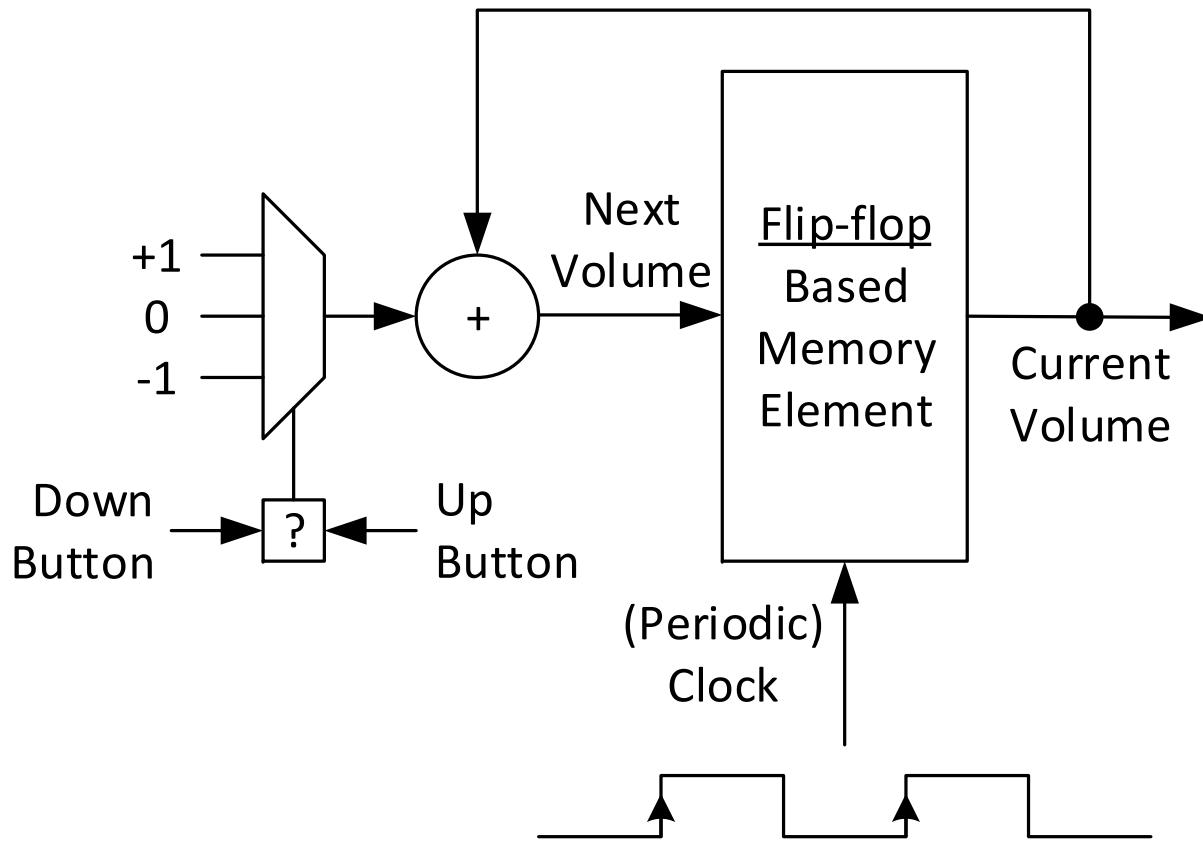
Latch Limitations/Issues



Possible Solution? Unfeasible!



A Feasible Solution



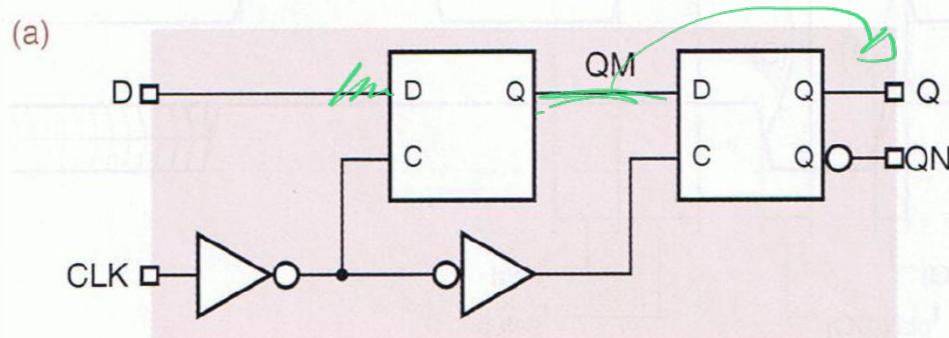
Periodic updates triggered by
one of the edges (rising or
falling) of a clock signal

Positive-edge-triggered D Flip-flop

Por de latch D

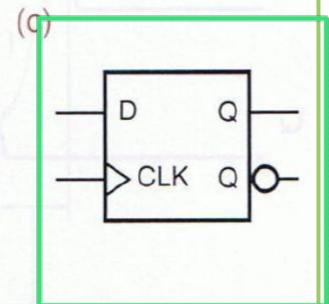
- Latches are not used frequently but are a building block for flip-flops

Figure 7-15 Positive-edge-triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.



(b)

D	CLK	Q	QN
0	0	0	1
1	1	1	0
x	0	last Q	last QN
x	1	last Q	last QN



flip - flop D



Estratégia para entender

São díuos concelos:

- 1 tem de estar fechada e outra aberta



Note: Positive-edge-triggered D flip-flop

$$\text{clk} = 0 \quad | \quad \text{clk} = 1$$

→ Deixa entrar a informação e mantém a saída → Mantém a informação e abre a saída

③ Momentos em que pode haver mudanças na

clk

udongos na
aída ①

6

1

1

1

→ Q M

D Q
clk

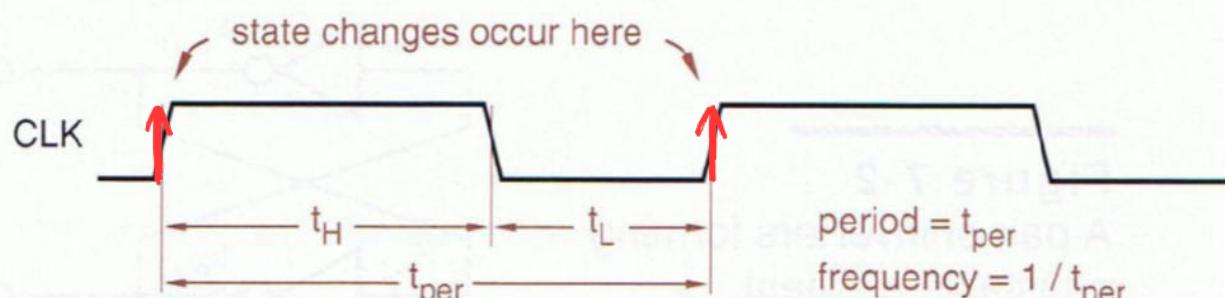
Ativo com
clk a 1

A hand-drawn diagram of a rectangle. The top-left vertex is labeled 'D' and the top-right vertex is labeled 'Q'. The bottom-left vertex is labeled 'O' and has a red arrow pointing towards it from the left, with the word 'clk' written next to it.

ativo com
clk a 0

Clock Signals (revisited)

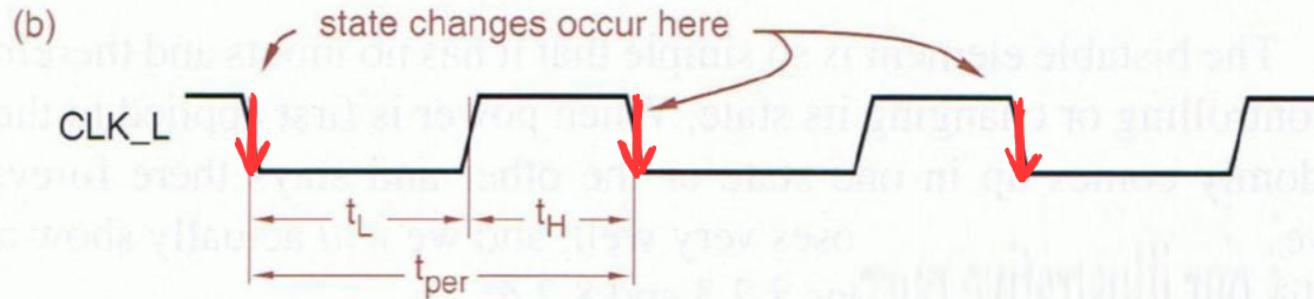
(a)



Positive - edge ...

$$\begin{aligned} \text{period} &= t_{per} \\ \text{frequency} &= 1 / t_{per} \\ \text{duty cycle} &= t_H / t_{per} \end{aligned}$$

(b)



Negative - edge ...

Figure 7-1
Clock signals:
(a) active high;
(b) active low.

Positive-edge-triggered D Flip-flop (Functional Behavior / Operation)

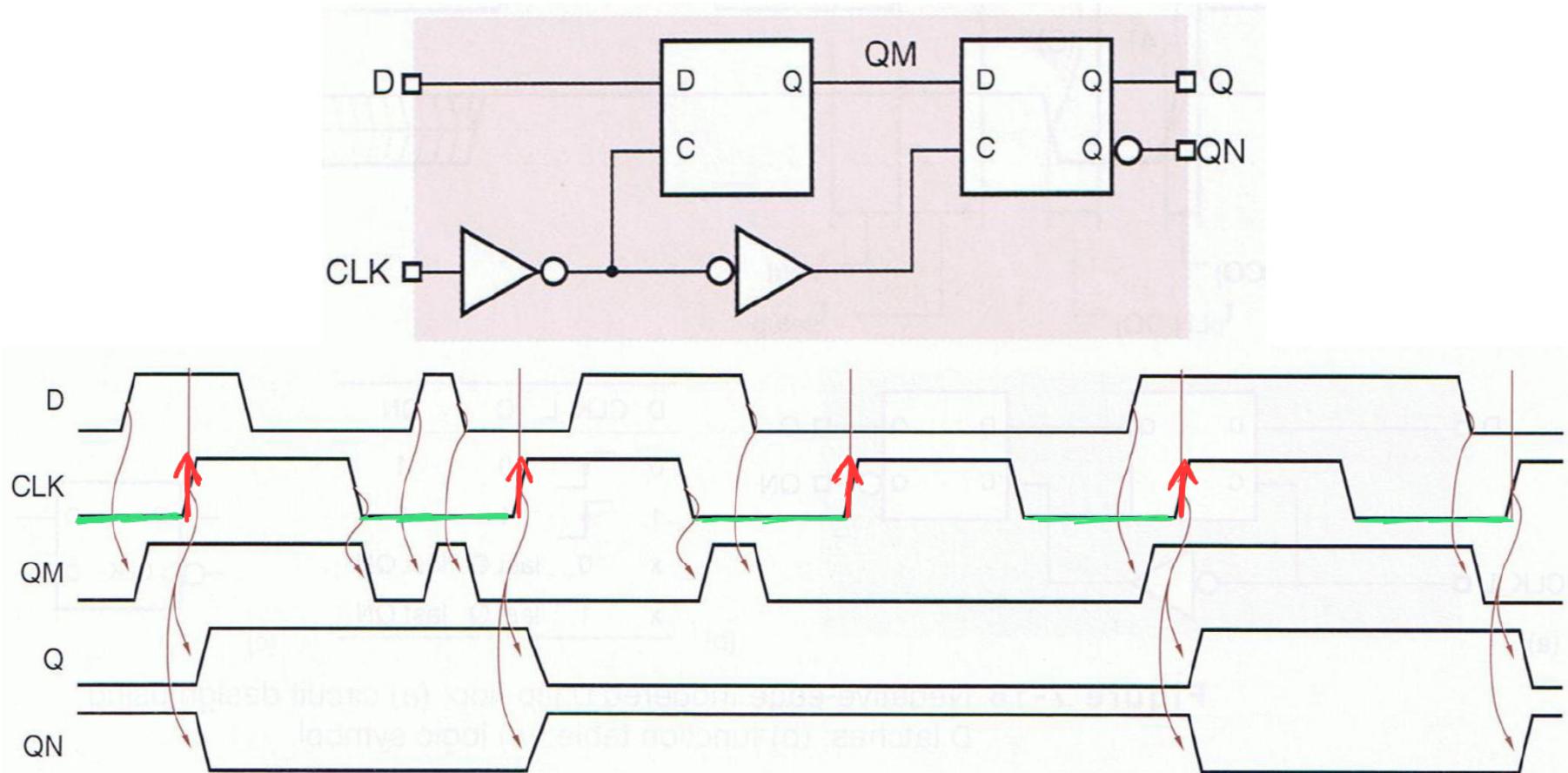
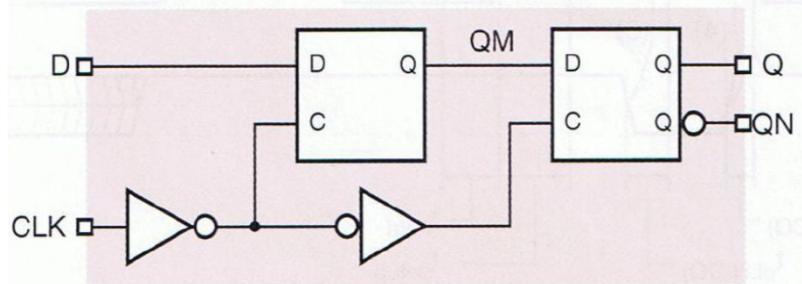


Figure 7-16 Functional behavior of a positive-edge-triggered D flip-flop.

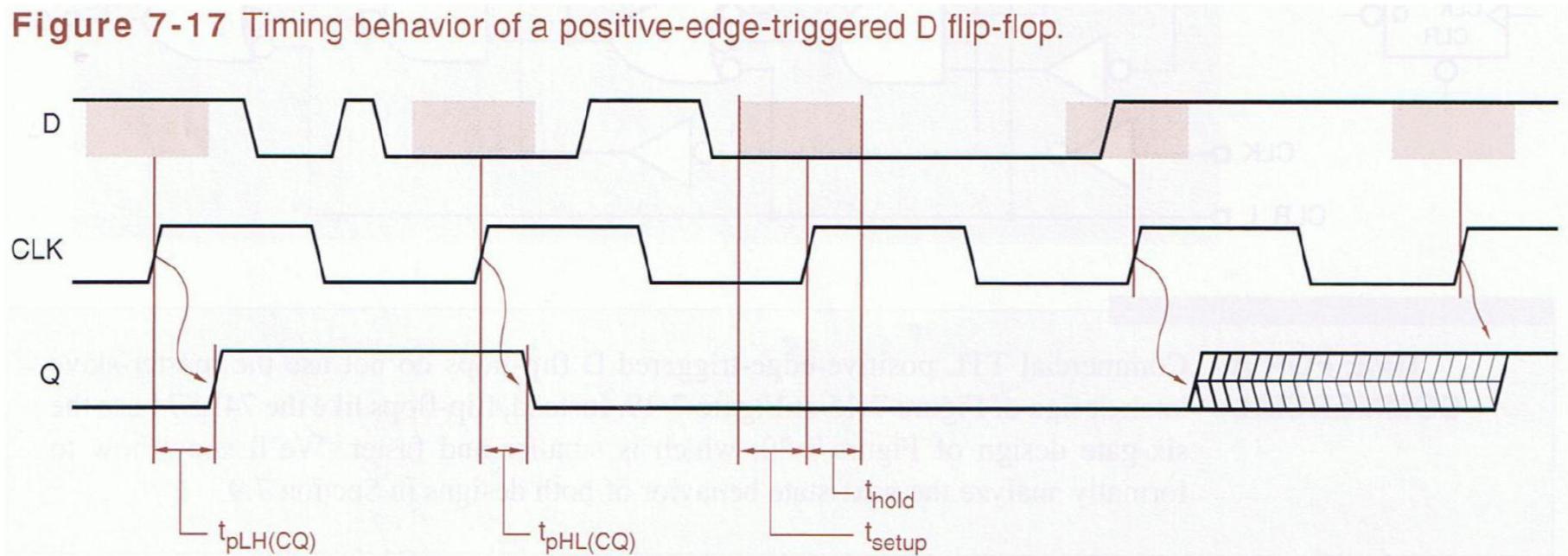
Positive-edge-triggered D Flip-flop (Timing Behavior)



- t_{pLH} – propagation time LOW-to-HIGH
- t_{pHL} – propagation time HIGH-to-LOW
- t_{setup} – setup time
- t_{hold} – hold time

Non-determinism/metastability due to violation of t_{setup} and/or t_{hold}

Figure 7-17 Timing behavior of a positive-edge-triggered D flip-flop.



Negative-edge-triggered D Flip-flop

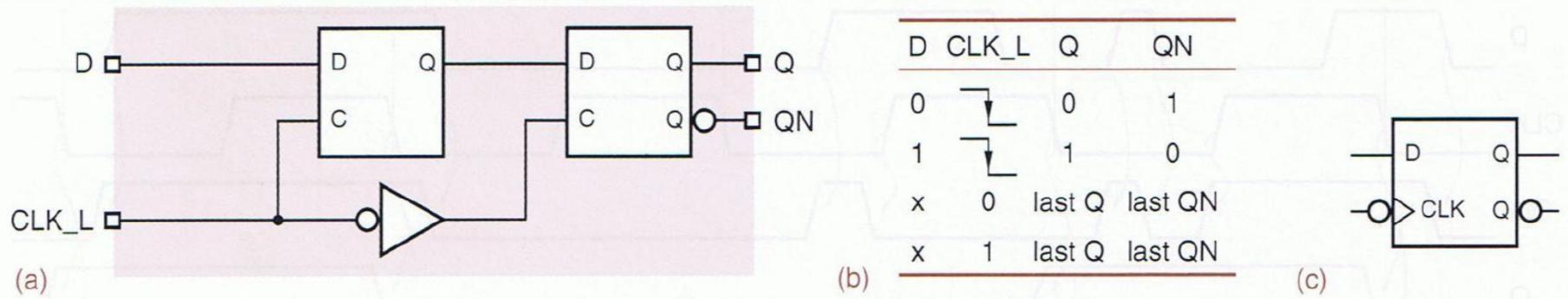
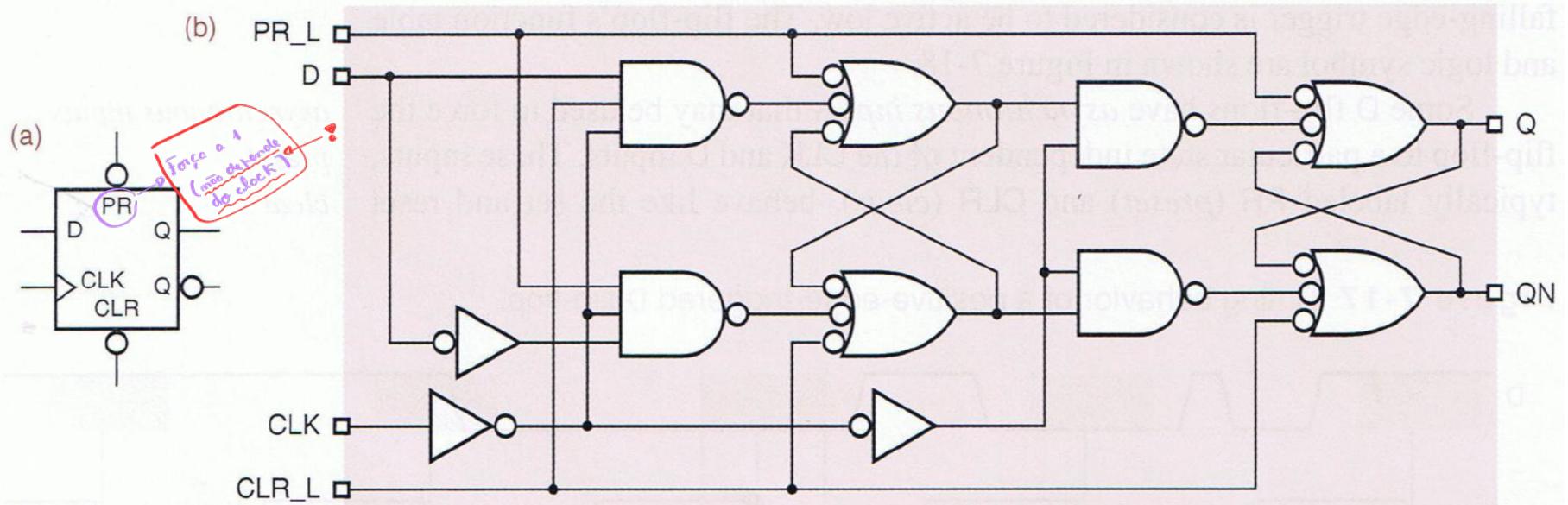


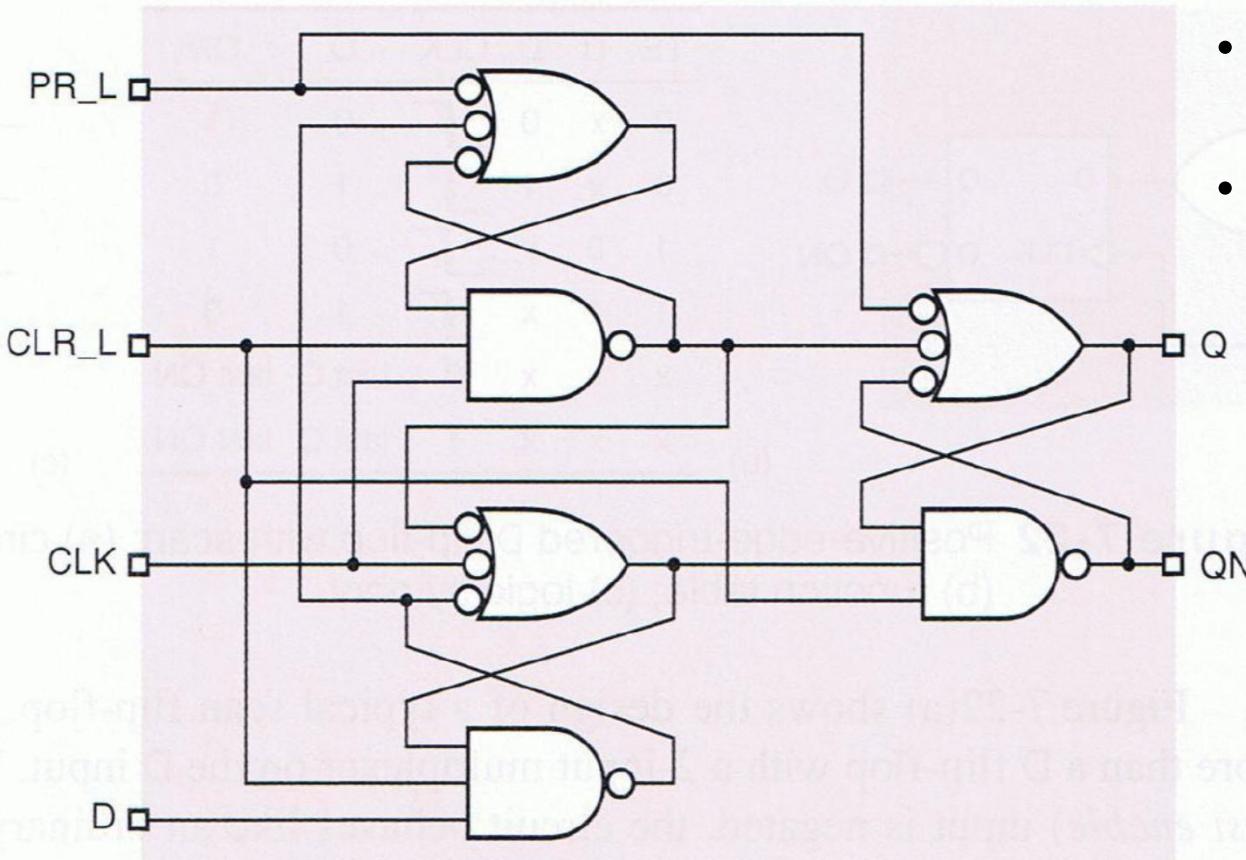
Figure 7-18 Negative-edge triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.

Positive-edge-triggered D Flip-flop with Preset and Clear

Figure 7-19 Positive-edge-triggered D flip-flop with preset and clear:
(a) logic symbol; (b) circuit design using NAND gates.



Positive-edge-triggered D Flip-flop (7474 Commercial Integrated Circuit)

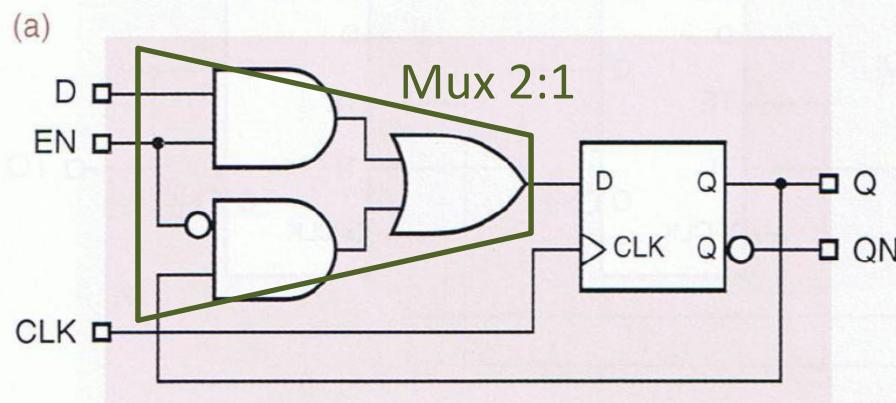


- 6 gates instead of 8 gates + inverters
- To be analyzed later...

Figure 7-20
Commercial circuit for
a positive-edge-
triggered D flip-flop
such as 74LS74.

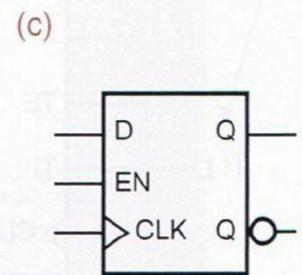
Positive-edge-triggered D Flip-flop with Enable

Figure 7-21 Positive-edge-triggered D flip-flop with enable: (a) circuit design; (b) function table; (c) logic symbol.



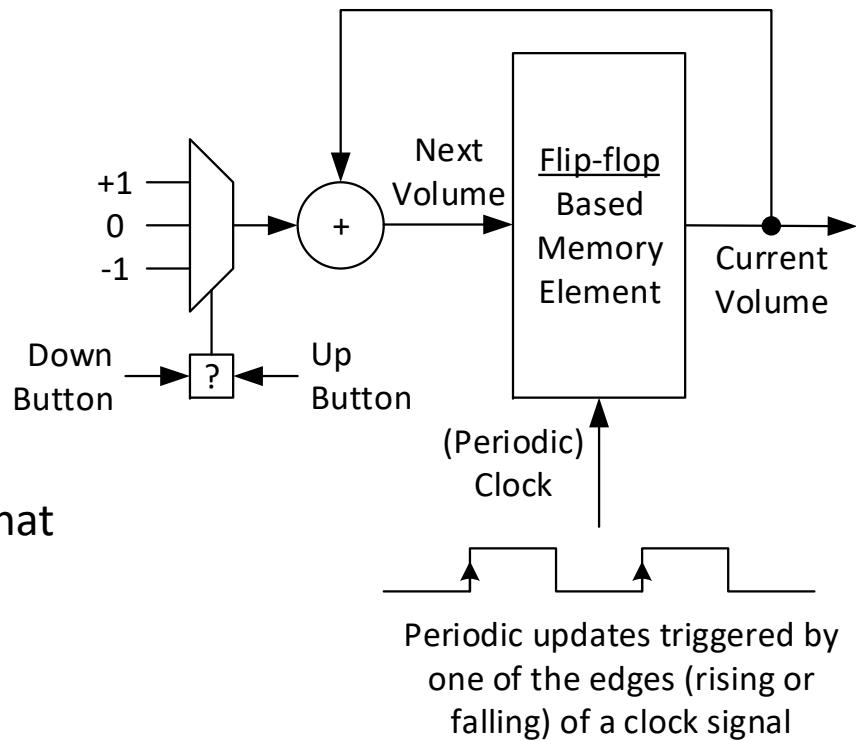
(b)

D	EN	CLK	Q	QN
0	1	0	0	1
1	1	1	1	0
x	0	0	last Q	last QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN



Exercise

- Design the complete logic diagram of the volume control system based on positive-edge-triggered D Flip-flops with enable (assume 16 levels of volume).
- Component budget
 - Flip-flops
 - Adder
 - Mux 2:1
 - Logic gates
- From the usability point of view, what could be the clock frequency?
- How to force a predefined volume level (e.g. half scale) at power up?



Conclusion

- At the end of this lecture and corresponding lab, it is fundamental to know and understand the structure, operation and timing behavior of basic sequential logic circuits (latches and flip-flops)
- Plan for the next lectures
 - Analysis of sequential circuits (Finite State Machines) and timing aspects
 - Synthesis of sequential circuits (Finite State Machines)
 - Standard sequential circuits
 - Registers and shift registers
 - Counters
 - Iterative vs. sequential circuits

Reading chapter 7 (4th ed.) or chapter 10 (5th ed.) of John F. Wakerly, "Digital Design – Principles and Practices", Pearson – Prentice Hall, is highly recommended.