

# Introduction to Digital Systems

## Part III (Sequential Components)

2022/2023

Analysis of Clocked Synchronous  
Finite State Machines

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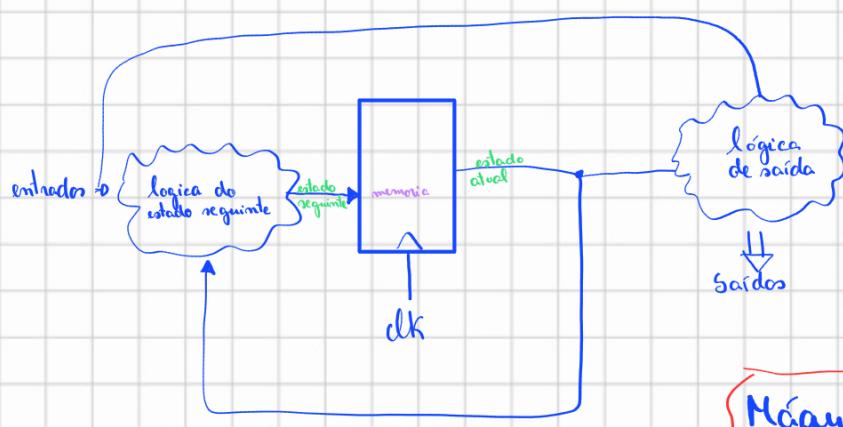
# Lecture Contents

- Analysis of Clocked Synchronous Finite State Machines
  - Typical structure
    - Mealy machine
    - Moore machine
    - Next state and output logic
  - State, transition and output tables
  - State diagrams
  - Timing analysis

Figures and most content extracted from: John F. Wakerly,  
“Digital Design – Principles and Practices”, 4 ed., Pearson –  
Prentice Hall, 2006 (chapter 7). Reading chapter 7 (4<sup>th</sup> ed.) or  
chapter 10 (5<sup>th</sup> ed.) is highly recommended.

# Clocked Synchronous Finite State Machines

- Why?
  - “Finite State Machine” (FSM)
  - “Clocked”
  - “Synchronous”
- State change at clock “tick”

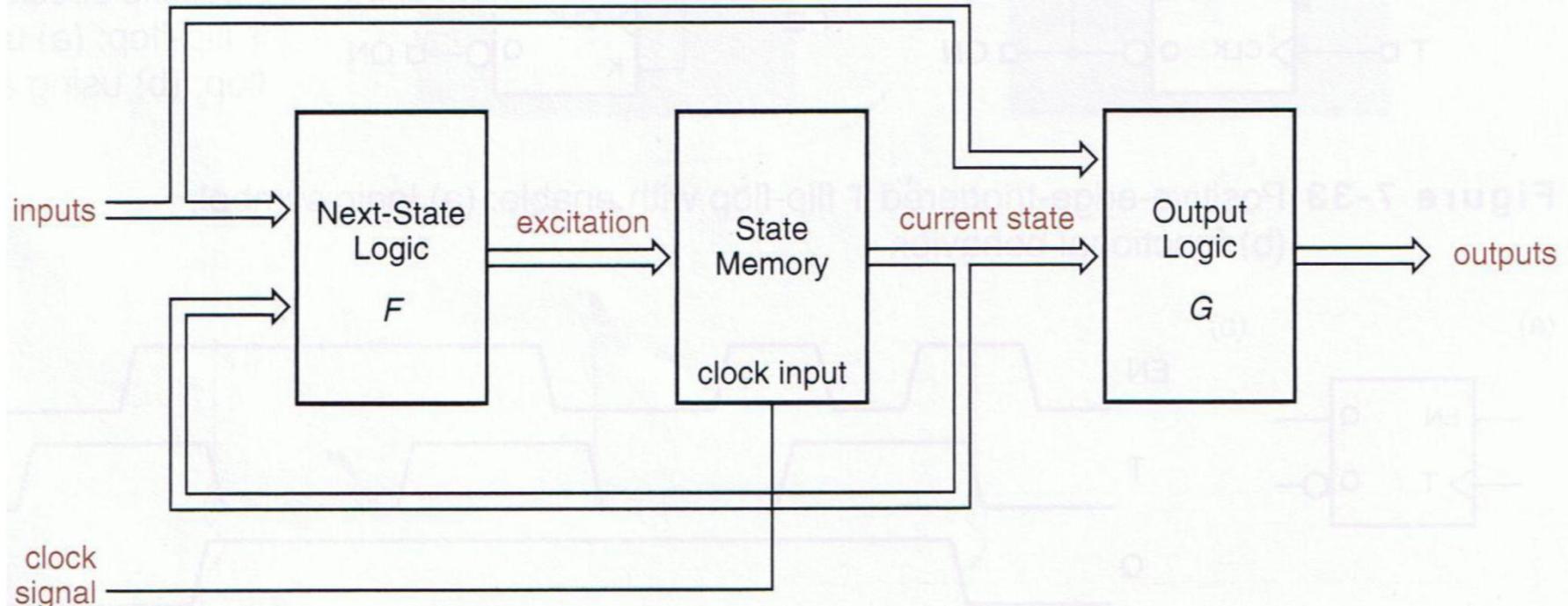


Máquina de Moore  
de Mealy

- Não depende de entradas
- Depende dos estados

# FSM Structure (Mealy Machine)

Figure 7-35 Clocked synchronous state-machine structure (Mealy machine).

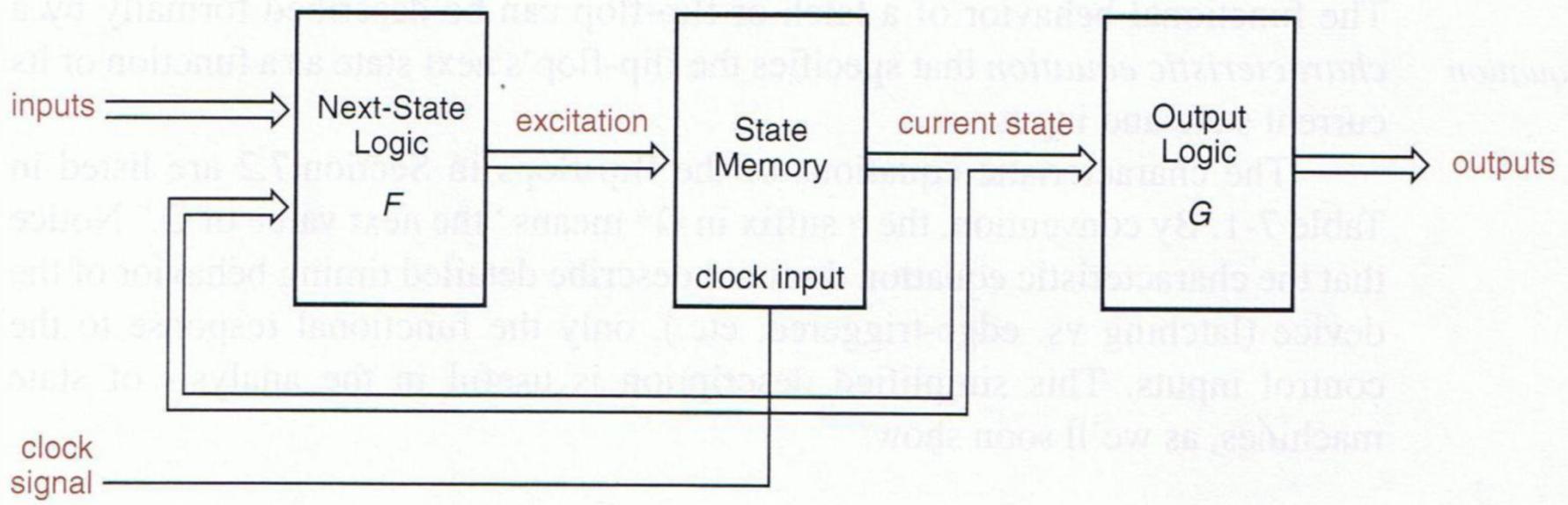


$$\text{next state} = F(\text{current state}, \text{inputs})$$

$$\text{outputs} = G(\text{current state}, \text{inputs})$$

# FSM Structure (Moore Machine)

Figure 7-36 Clocked synchronous state-machine structure (Moore machine).



$$\text{next state} = F(\text{current state}, \text{inputs})$$

$$\text{outputs} = G(\text{current state})$$

# Latches and Flip-flops

## Characteristic Equations

- Characteristic Equation – what is the next state depending on current state and input(s)?

<i>Device Type</i>	<i>Characteristic Equation</i>
S-R latch	$Q^* = S + R' \cdot Q$
D latch	$Q^* = D$
Edge-triggered D flip-flop	$Q^* = D$
D flip-flop with enable	$Q^* = EN \cdot D + EN' \cdot Q$

**Table 7-1**  
Latch and flip-flop  
characteristic  
equations.

# Clocked Synchronous FSM Analysis

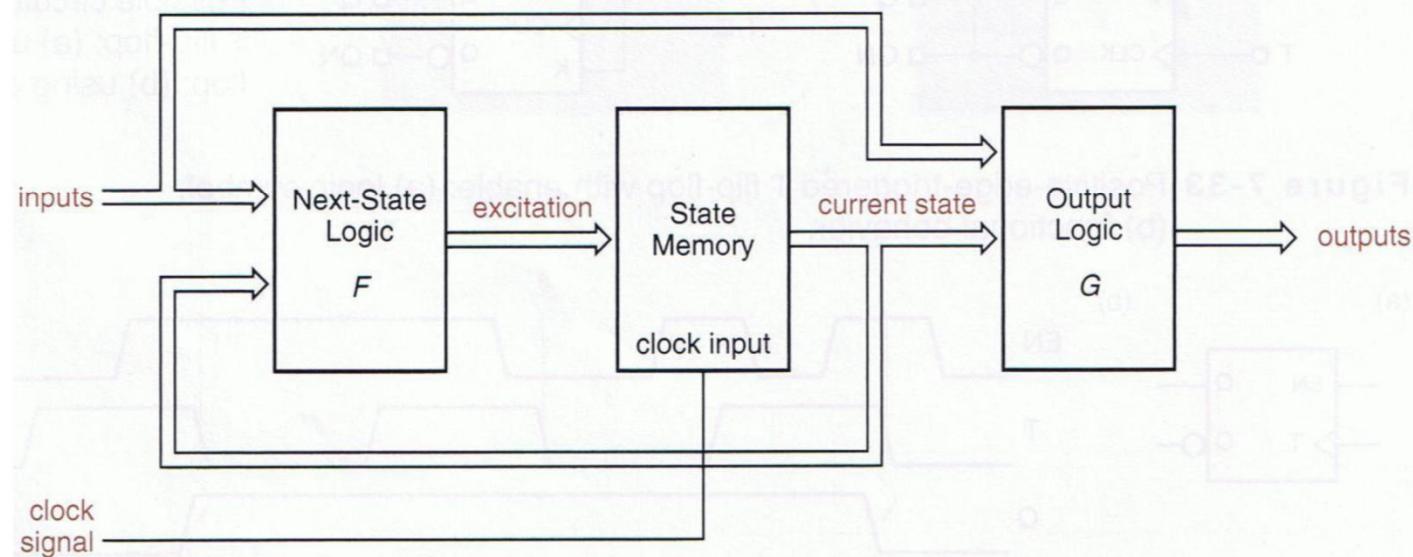
The analysis of a clocked synchronous state machine has three basic steps:

1. Determine the next-state and output functions  $F$  and  $G$ .
2. Use  $F$  and  $G$  to construct a *state/output table* that completely specifies the next state and output of the circuit for every possible combination of current state and input.
3. (Optional) Draw a *state diagram* that presents the information from the previous step in graphical form.

*state/output table*

*state diagram*

**Figure 7-35** Clocked synchronous state-machine structure (Mealy machine).



# Example of an FSM Logic Circuit

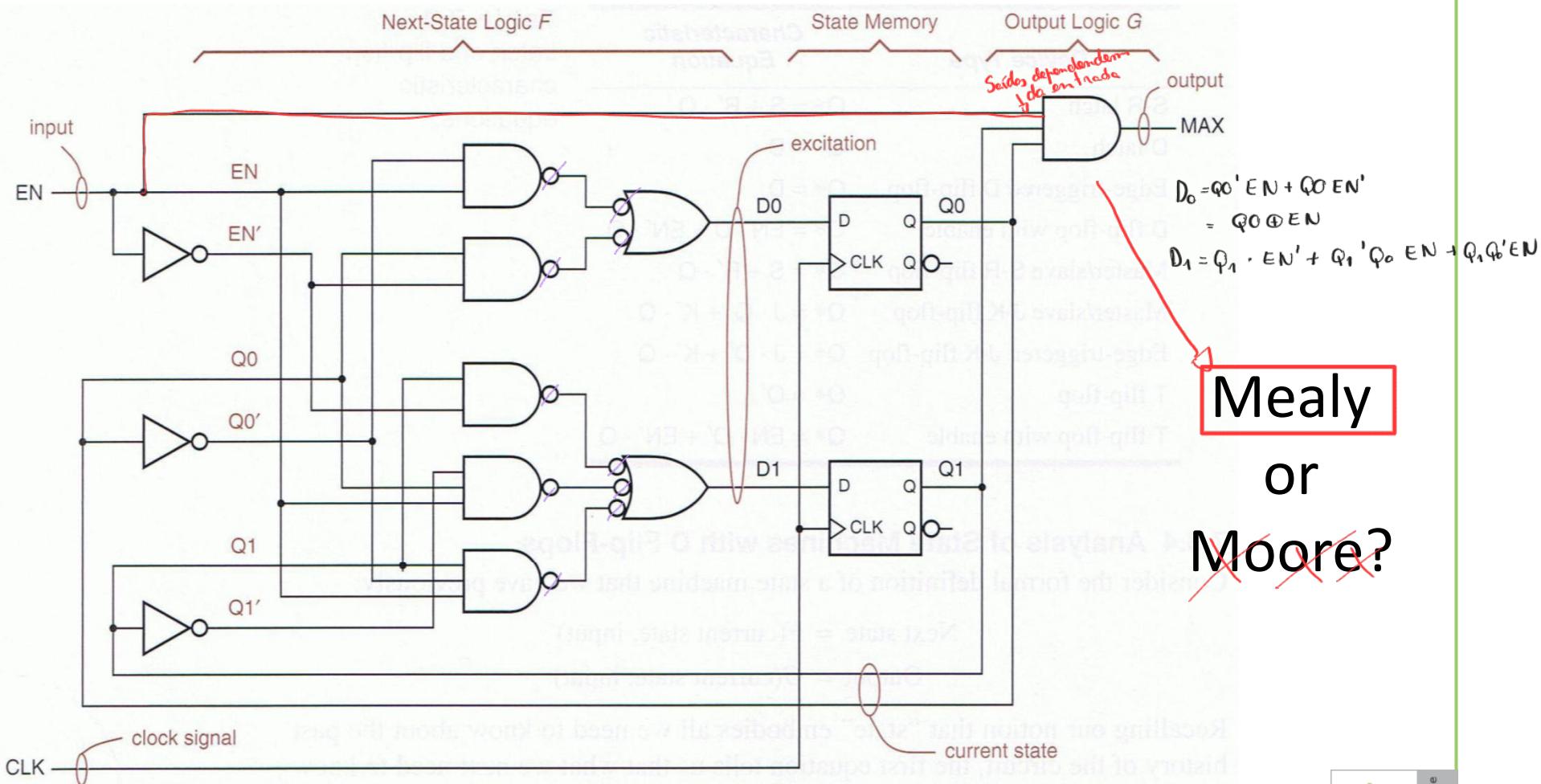


Figure 7-38 Clocked synchronous state machine using positive-edge-triggered D flip-flops.

# Example of an FSM Logic Circuit

## Excitation equations

$$Q_0^+ = Q_0 \cdot EN' + Q_0' \cdot EN$$

$$Q_1^+ = Q_1 \cdot EN' + Q_1' \cdot Q_0 \cdot EN + Q_1 \cdot Q_0' \cdot EN$$

$$= \overline{EN} \cdot Q_1 + EN \cdot (Q_1 \oplus Q_0)$$

## Characteristic equations

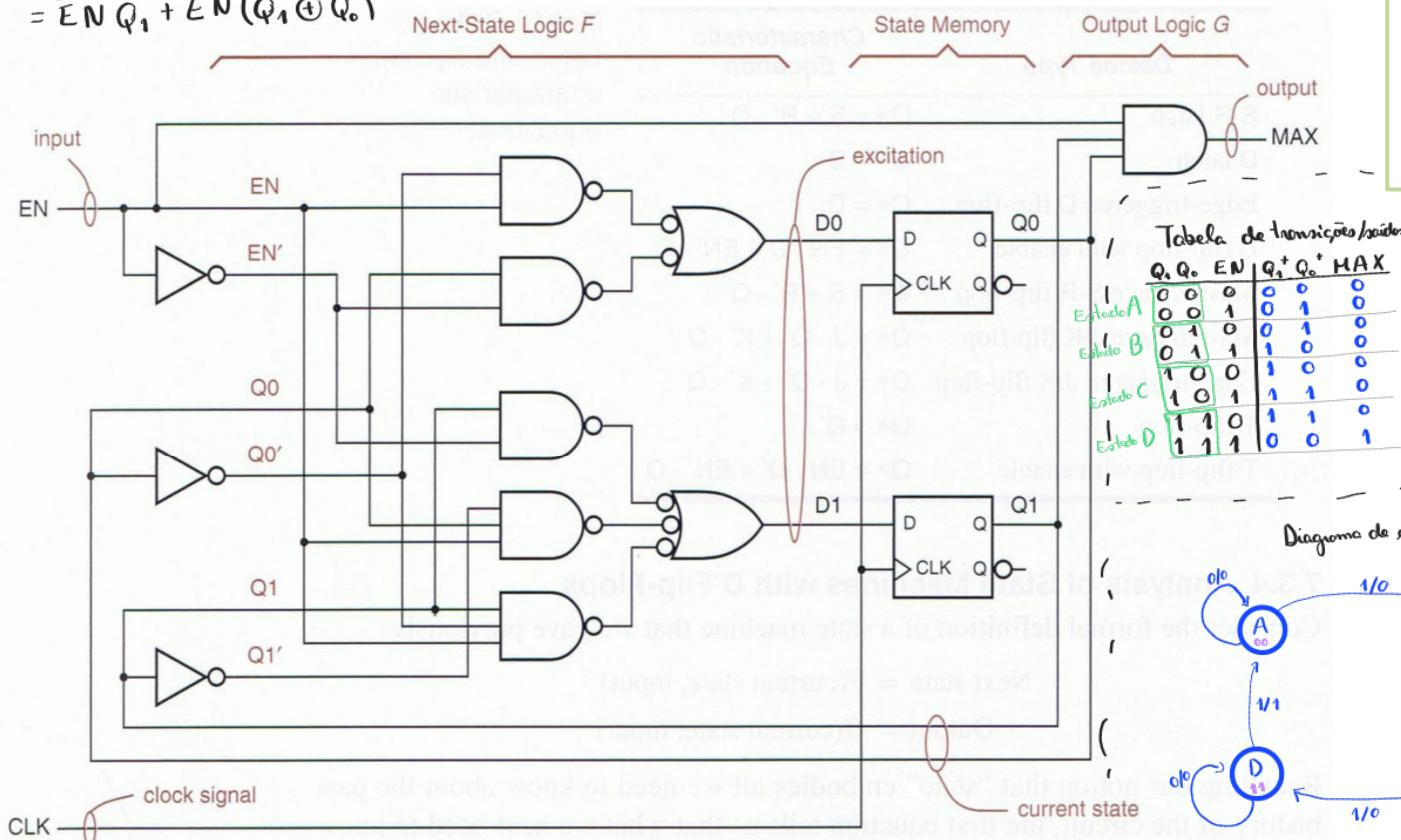
$$Q_0^* = D_0$$

$$Q_1^* = D_1$$

## Transition equations

$$Q_0^* = Q_0 \cdot EN' + Q_0' \cdot EN$$

$$Q_1^* = Q_1 \cdot EN' + Q_1' \cdot Q_0 \cdot EN + Q_1 \cdot Q_0' \cdot EN$$



## Output(s) equation(s)

$$MAX = Q_1 \cdot Q_0 \cdot EN$$

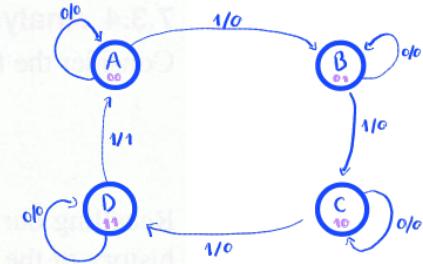
Tabela de transições/saídas

$Q, Q'$	$EN$	$Q_1^+, Q_0^+, MAX$	
		$Q_1^+$	$Q_0^+$
Estado A	0 0	0	0
Estado A	0 0	0	1
Estado B	0 1	0	1
Estado B	0 1	1	0
Estado C	1 0	1	0
Estado C	1 0	1	1
Estado D	1 1	0	1
Estado D	1 1	0	0

Tabela de entradas/saídas

$Q$	$EN$	$Q'$	$MAX$
A	0	A	0
A	1	B	0
B	0	B	0
B	1	C	0
C	0	C	0
C	1	D	0
D	0	D	0
D	1	A	1

Diagrama de estados



Legenda:  $EN/MAX$

Figure 7-38 Clocked synchronous state machine using positive-edge-triggered D flip-flops.



# Transition, State and State/Output Tables

Transition equations

$$Q_0^* = Q_0 \cdot EN' + Q_0' \cdot EN$$

$$Q_1^* = Q_1 \cdot EN' + Q_1' \cdot Q_0 \cdot EN + Q_1 \cdot Q_0' \cdot EN$$

Output(s)  
equation(s)

$$MAX = Q_1 \cdot Q_0 \cdot EN$$

What is the purpose of the circuit and the role of its inputs and outputs?

		EN	
<i>Q<sub>1</sub></i>	<i>Q<sub>0</sub></i>	0	1
00	00	01	
01	01	10	
10	10	11	
11	11	00	
		Q <sub>1*</sub> Q <sub>0*</sub>	

		EN	
		S	0
<i>S</i>		0	1
A	A	B	
B	B	C	
C	C	D	
D	D	A	
		S*	

		EN	
<i>S</i>		0	1
A	A, 0	B, 0	
B	B, 0	C, 0	
C	C, 0	D, 0	
D	D, 0	A, 1	
		S*, MAX	

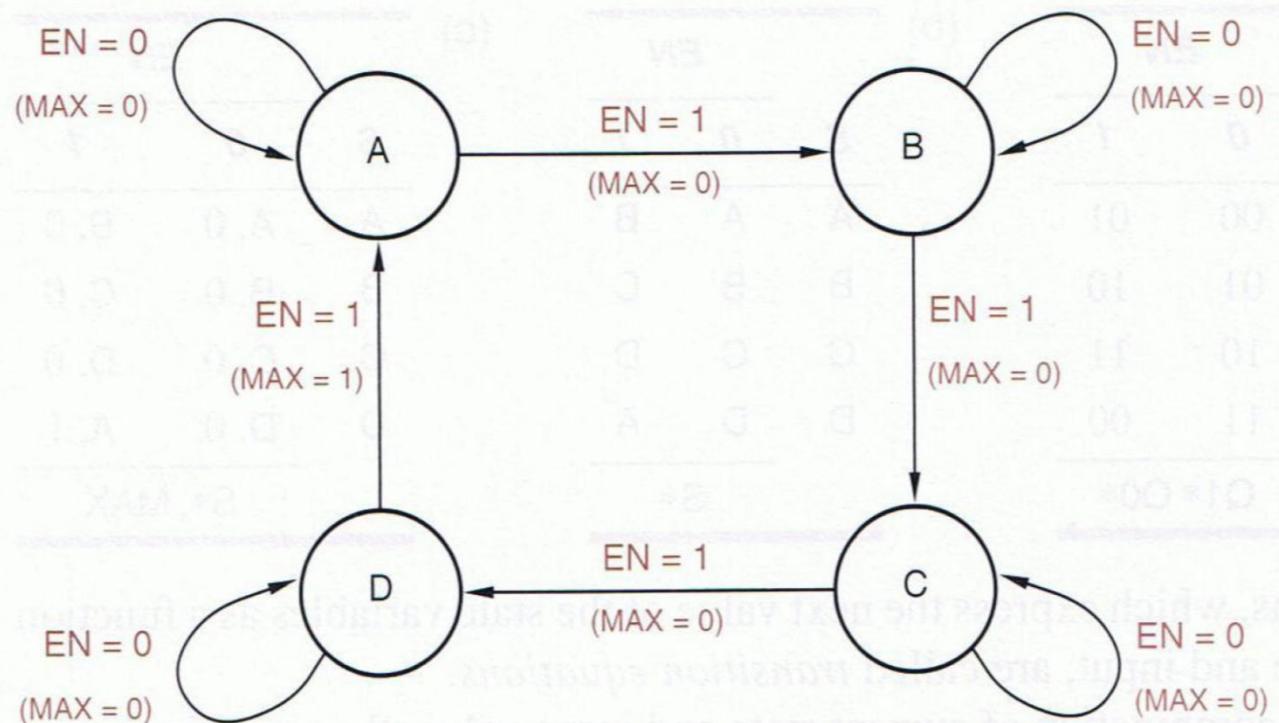
Table 7-2

Transition, state, and state/output tables for the state machine in Figure 7-38.

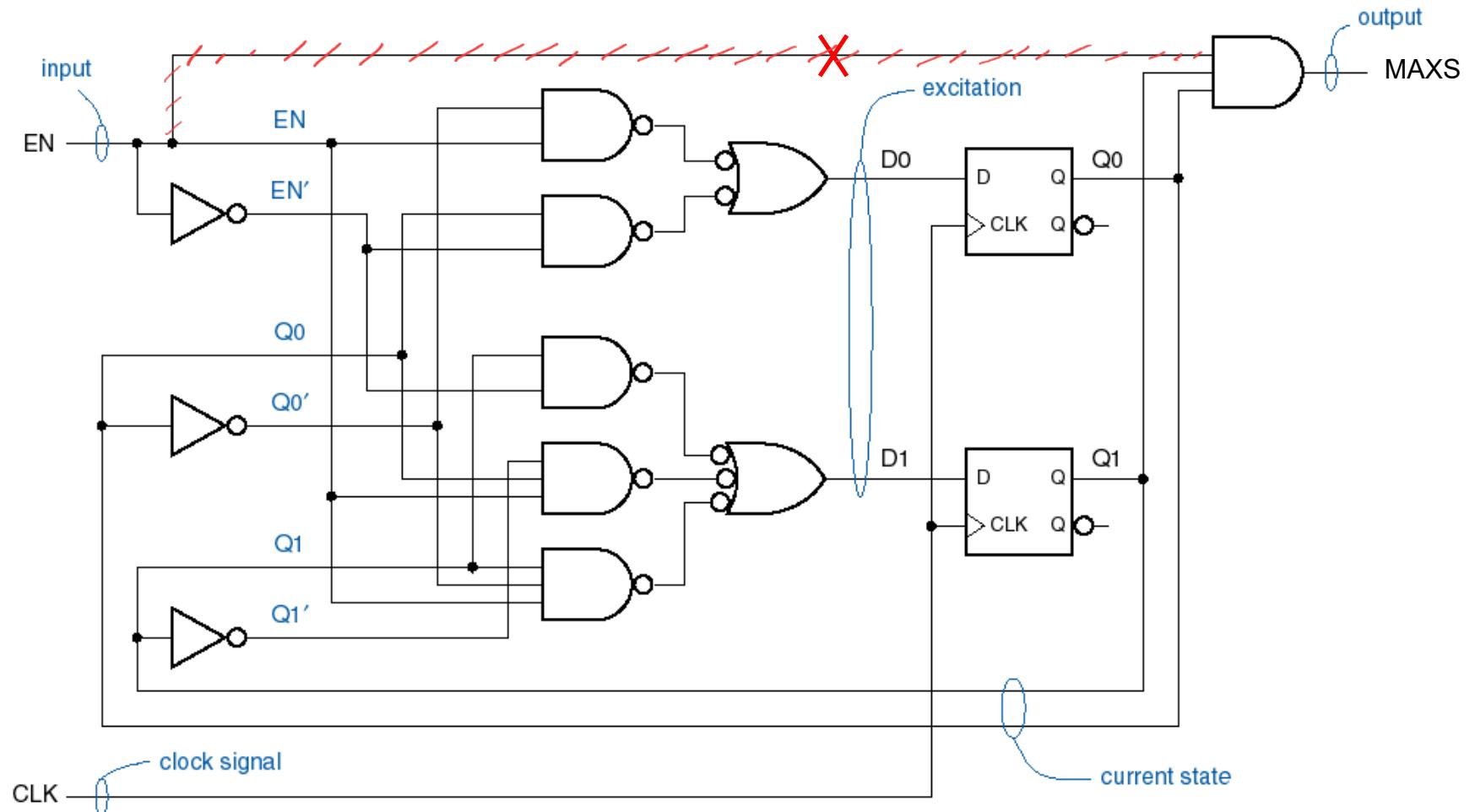
# State Diagram for a Mealy Machine

s	EN	
	0	1
A	A, 0	B, 0
B	B, 0	C, 0
C	C, 0	D, 0
D	D, 0	A, 1
S*, MAX		

**Figure 7-39**  
State diagram  
corresponding to the  
state machine of  
Table 7-2.



# Outputs in a Moore Machine



$$\text{MAXS} = Q_0 \cdot Q_1$$

Tabela de transições/saídos

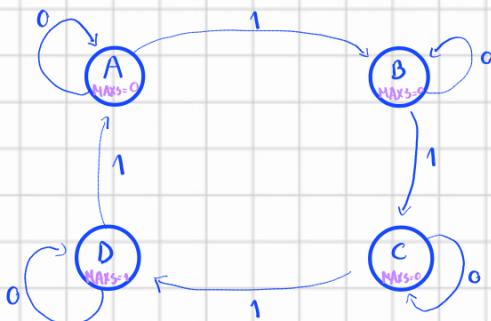
	$Q_1, Q_0$	EN	$Q_1^+, Q_0^+$	MAX	MAXS
Estado A	0 0	0	0 0	0	0
	0 0	1	0 1	0	0
	0 1	0	0 1	0	0
	0 1	1	1 0	0	0
Estado B	1 0	0	1 0	0	0
	1 0	1	1 1	0	0
	1 1	0	1 1	0	0
	1 1	1	1 1	0	1
Estado C	1 0	0	1 1	0	1
	1 0	1	1 1	0	0
	1 1	0	1 1	0	1
	1 1	1	0 0	1	1
Estado D	1 1	0	0 0	1	1
	1 1	1	0 0	1	1

Tabela de entradas/saídos

$Q$	EN	$Q'$	MAX	MAXS
A	0	A	0	0
A	1	B	0	0
B	0	B	0	0
B	1	C	0	0
C	0	C	0	0
C	1	D	0	0
D	0	D	0	1
D	1	A	1	1

Não depende  
de EN → Máquina  
de Moore

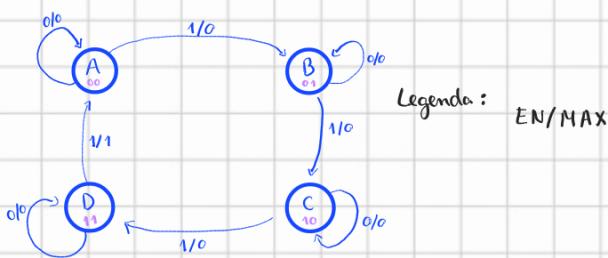
Diagrama de estados



É diferente de  
máquina de Mealy

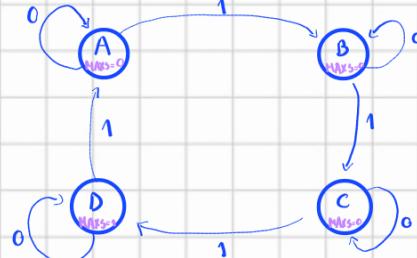
## Diagrama temporal (sem atraso !)

Mealy

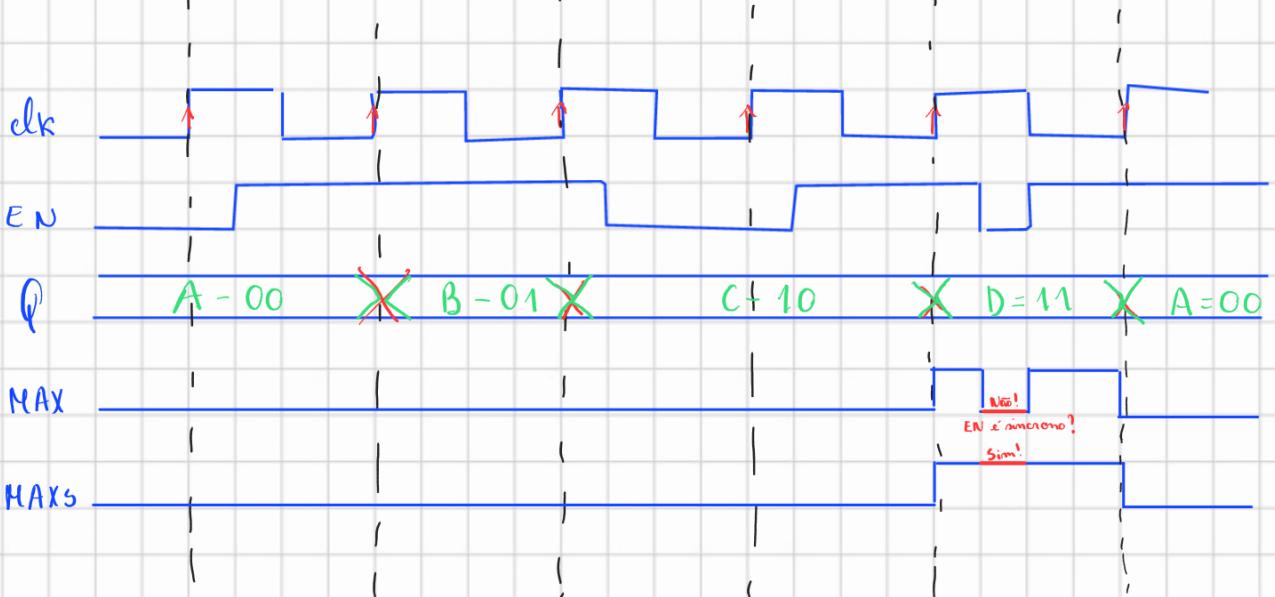


Legenda: EN/MAX

Moore



Legenda: EN



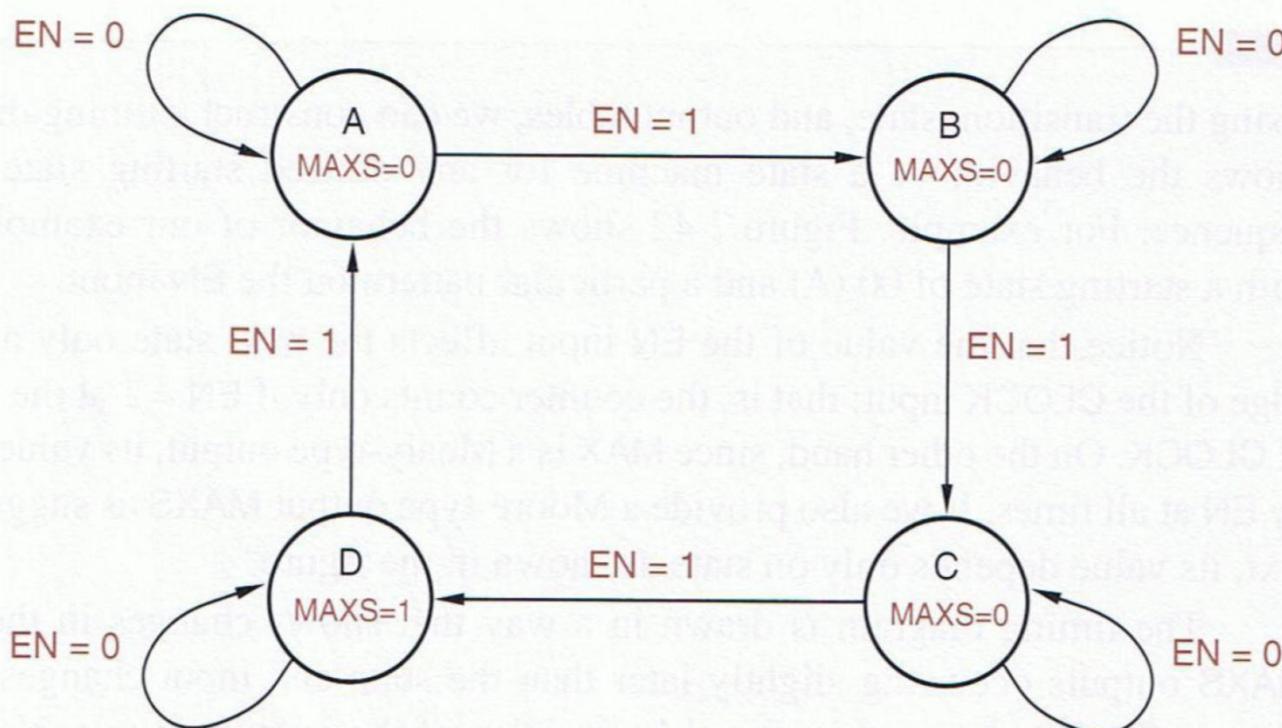
# Outputs in a Moore Machine

**Table 7-3**  
State/output table for  
a Moore machine.

S	EN		MAXS
	0	1	
A	A	B	0
B	B	C	0
C	C	D	0
D	D	A	1

S\*

# State Diagram for a Moore Machine



EN		MAXS
S	0	1
A	A	B
B	B	C
C	C	D
D	D	A
		S*

**Figure 7-40**  
State diagram  
corresponding to the  
state machine of  
Table 7-3.

# Redrawn Logic Diagram

Transition equations

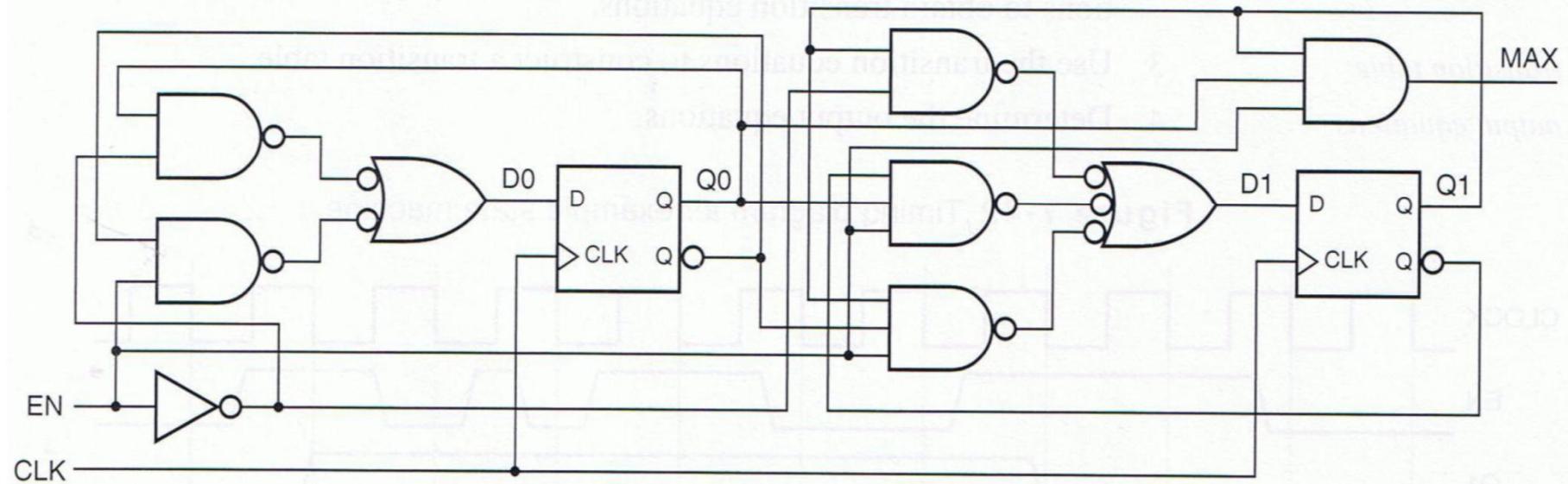
$$Q0^* = Q0 \cdot EN' + Q0' \cdot EN$$

$$Q1^* = Q1 \cdot EN' + Q1' \cdot Q0 \cdot EN + Q1 \cdot Q0' \cdot EN$$

Output(s)  
equation(s)

$$MAX = Q1 \cdot Q0 \cdot EN$$

Figure 7-41 Redrawn logic diagram for a clocked synchronous state machine.



# Timing Diagram

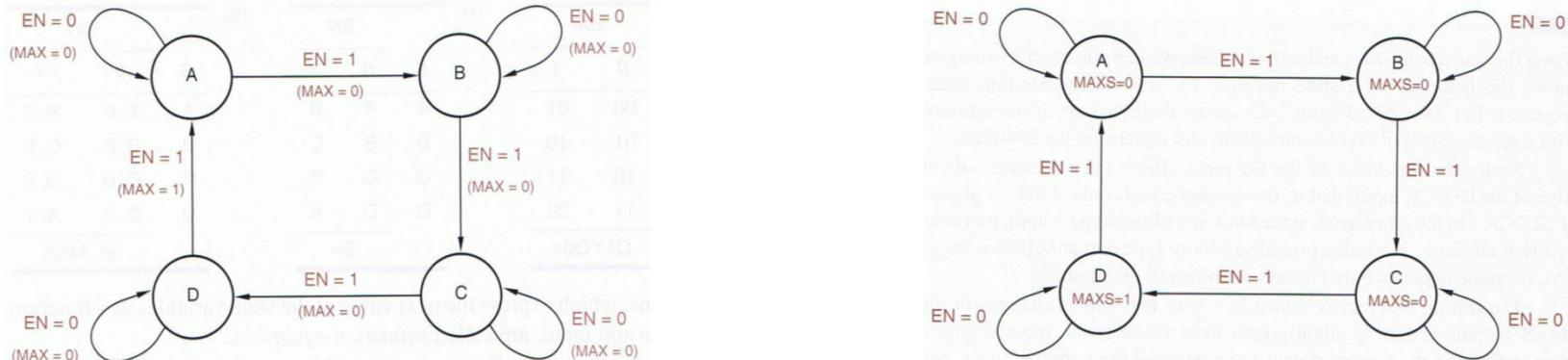
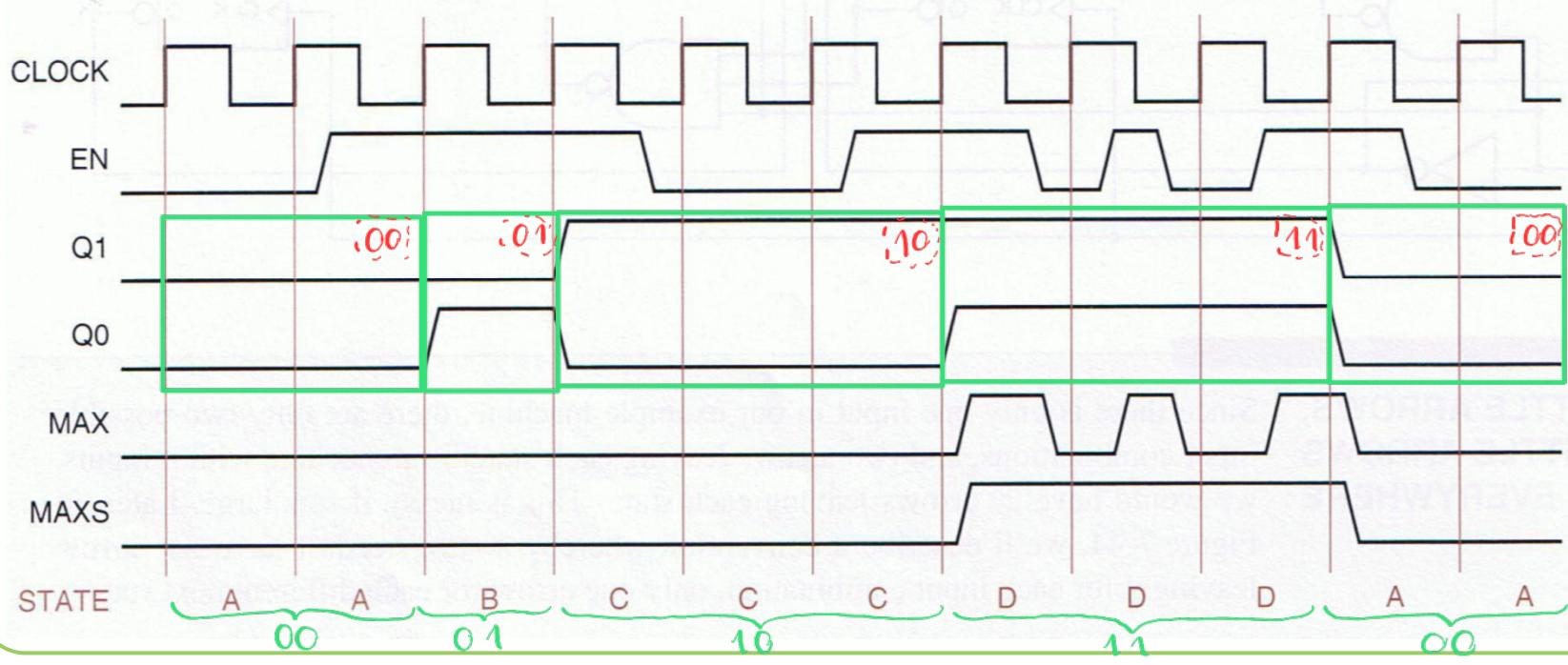
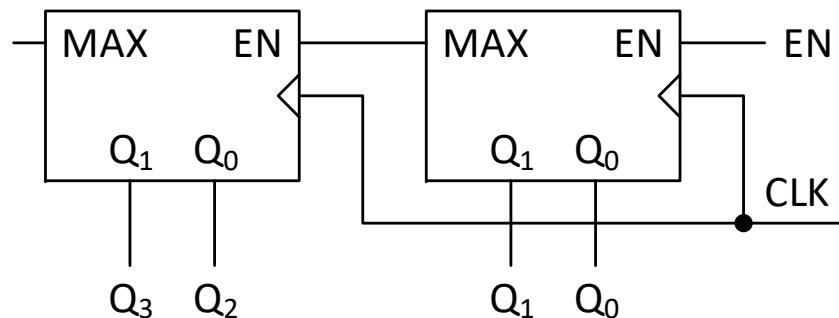


Figure 7-42 Timing diagram for example state machine.



# Cascading Two Counters

Using MAX output



Using MAXS output

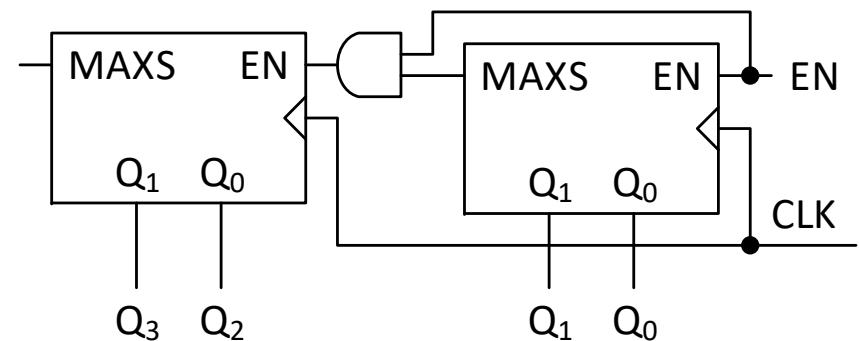
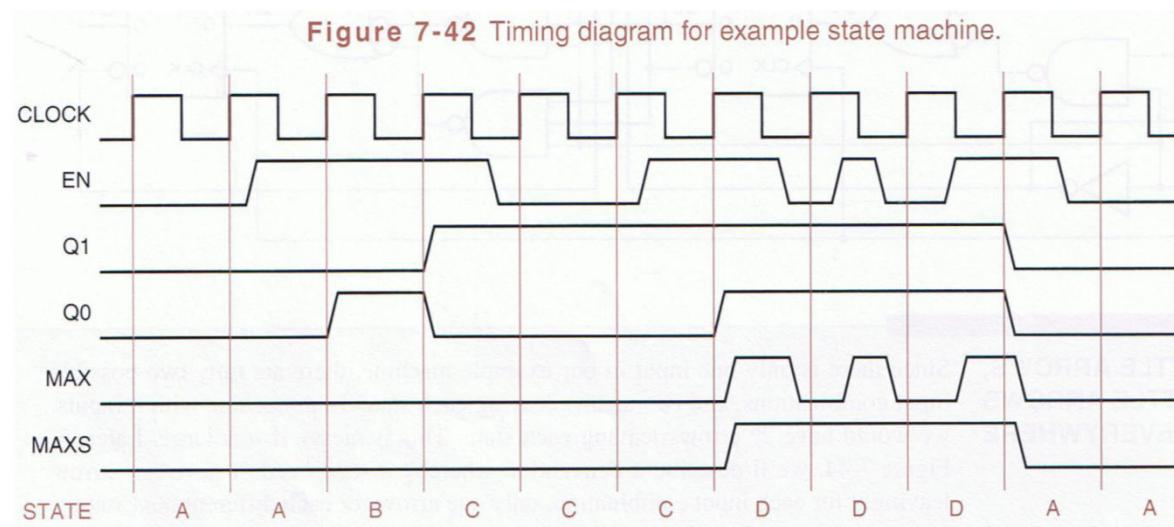


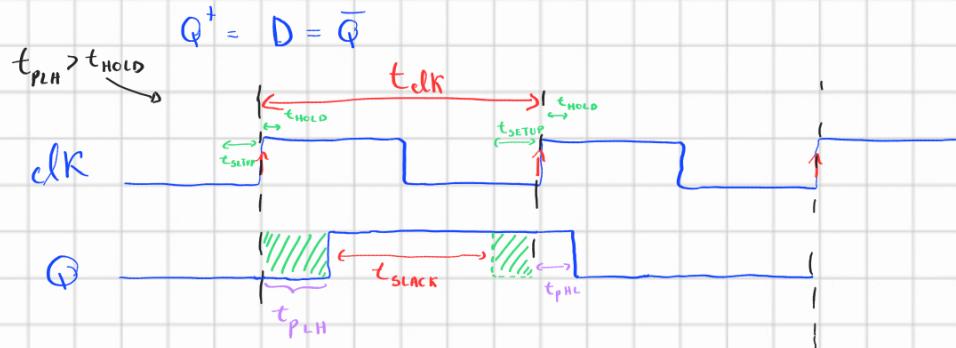
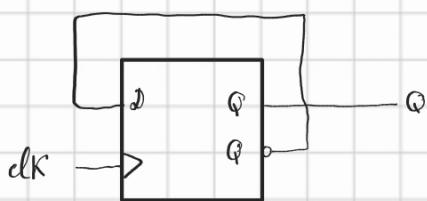
Figure 7-42 Timing diagram for example state machine.



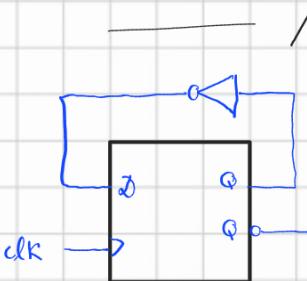
# Timing Analysis

- Purpose
  - Obtain all the circuit delays with the aim of determine the maximum operating frequency
- Ideal vs. real circuits
  - Real circuits exhibit propagation, setup and hold times
  - In ideal circuits all these timing parameters are zero
- Simplifications
  - Single clock domain fully synchronous circuits
  - Flip-flop “hold time” lower than both propagation times ( $T_{pLH}$  and  $T_{pHL}$ )

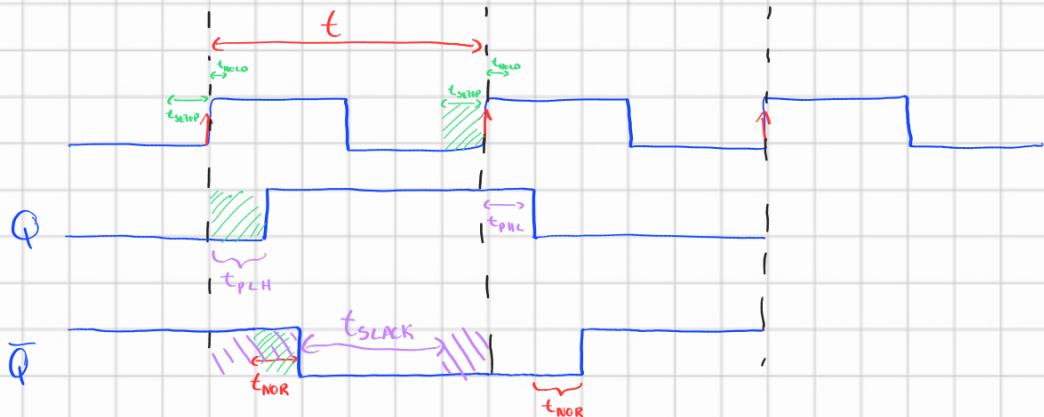
Exemplo:



$$t_{min} = t_{SETUP} + \max(t_{PLH}, t_{PHL})$$



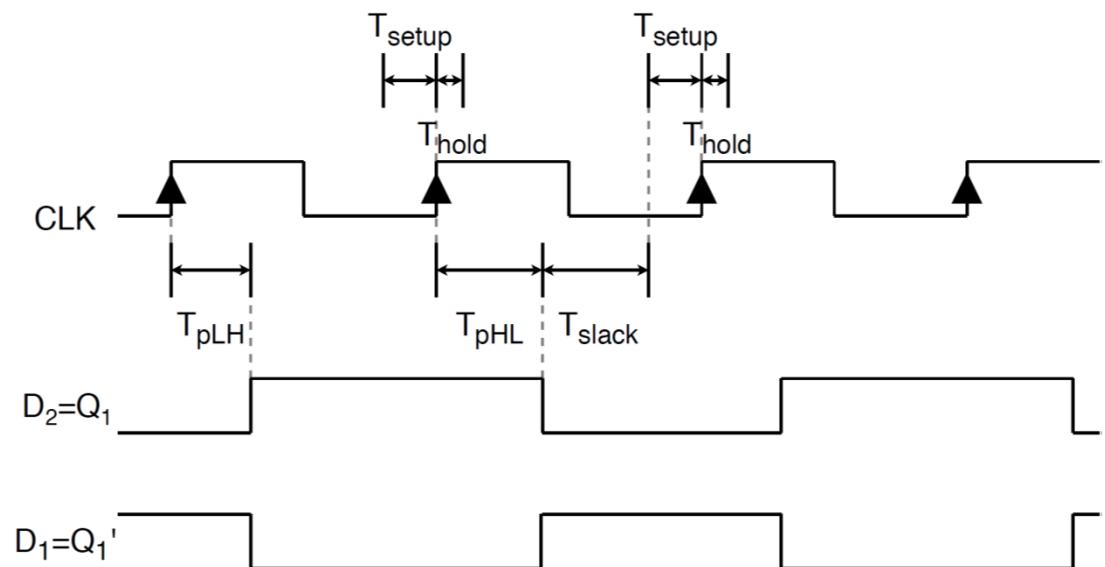
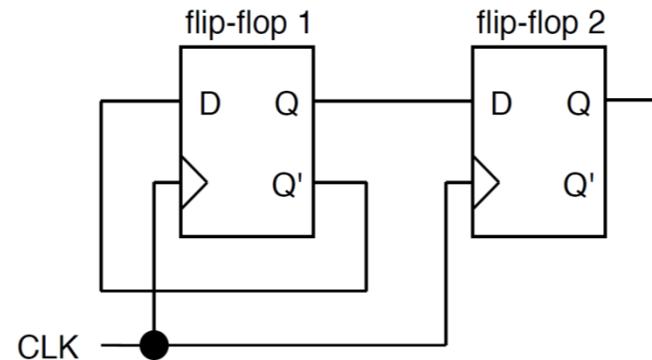
$$Q^+ = D = \bar{Q}$$



$$t_{min} = t_{SETUP} + \max(t_{PLH}, t_{PHL}) + t_{NOR}$$

# Timing Analysis - A Simple Example

- Flip-flop(s) without combinatorial logic in between / in the feedback path
- What is the maximum operating frequency / minimum period of CLK?



$T_{min}$  when  $T_{slack} = 0$

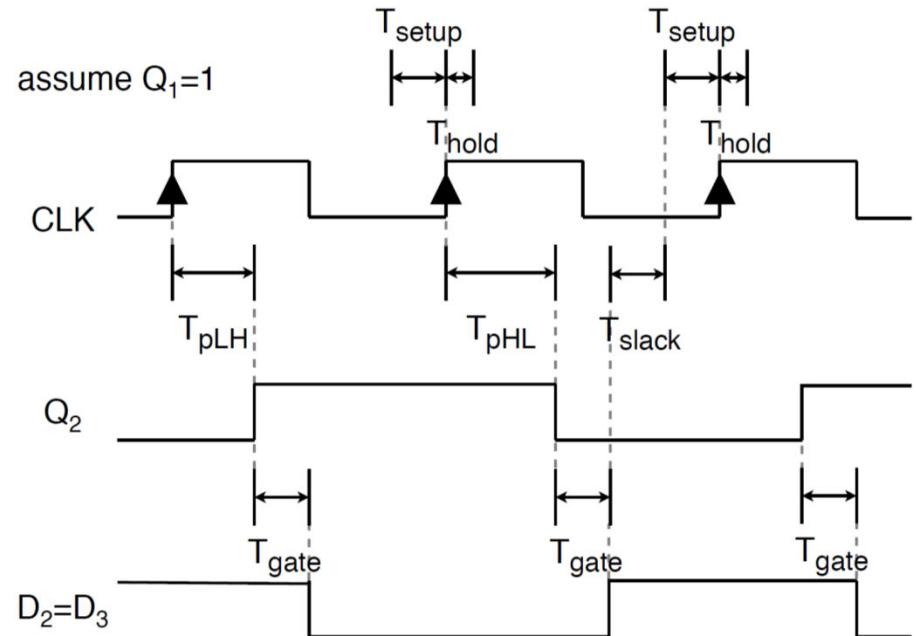
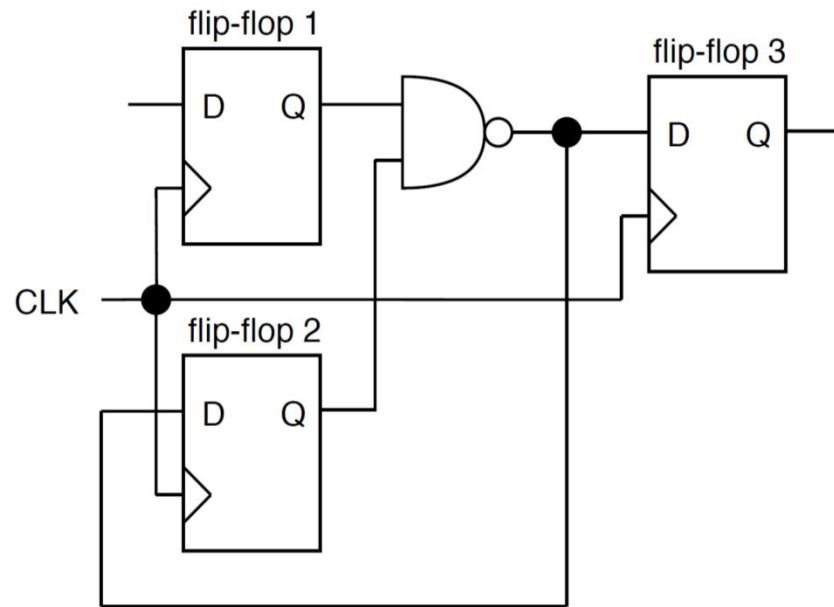
$$T_{min} = \max(T_{pHL}, T_{pLH}) + T_{setup}$$

$$f_{max} = \frac{1}{T_{min}}$$



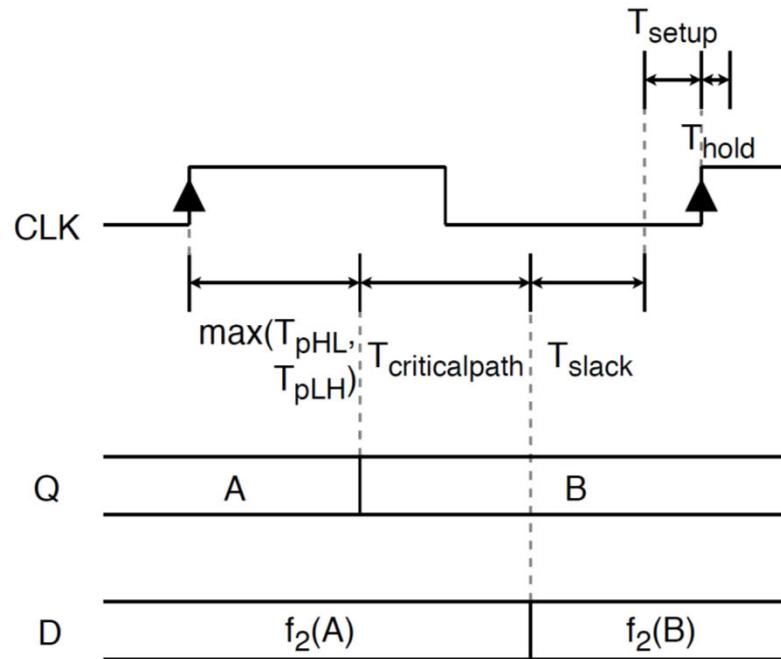
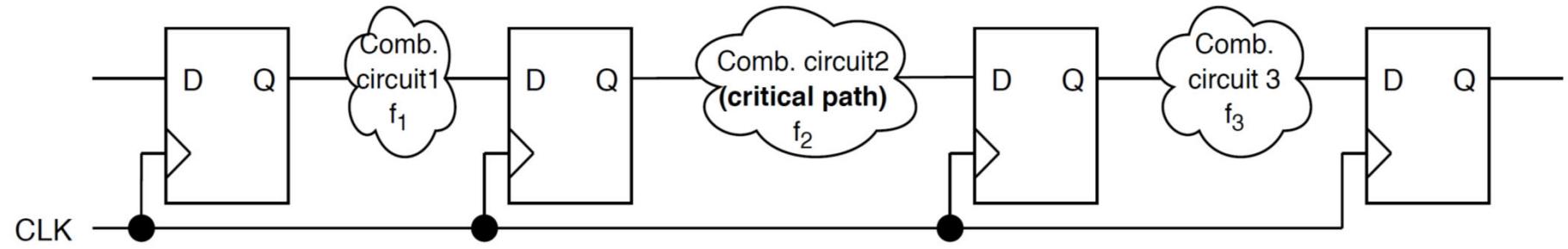
# Timing Analysis - Another Example

- Flip-flop(s) with simple logic gate in between / in the feedback path
- What is the maximum operating frequency / minimum period of CLK?



$$T_{min} \text{ when } T_{slack} = 0 \quad T_{min} = \max(T_{pHL}, T_{pLH}) + T_{gate} + T_{setup} \quad f_{max} = \frac{1}{T_{min}}$$

# Synchronous Circuit General Structure



What is the maximum operating frequency / minimum period of CLK?

$$T_{min} \text{ when } T_{slack} = 0$$

$$T_{min} = \max(T_{pHL}, T_{pLH}) + \boxed{T_{criticalpath}} + T_{setup}$$

O mais lento!

$$f_{max} = \frac{1}{T_{min}}$$

# FSM Timing Analysis

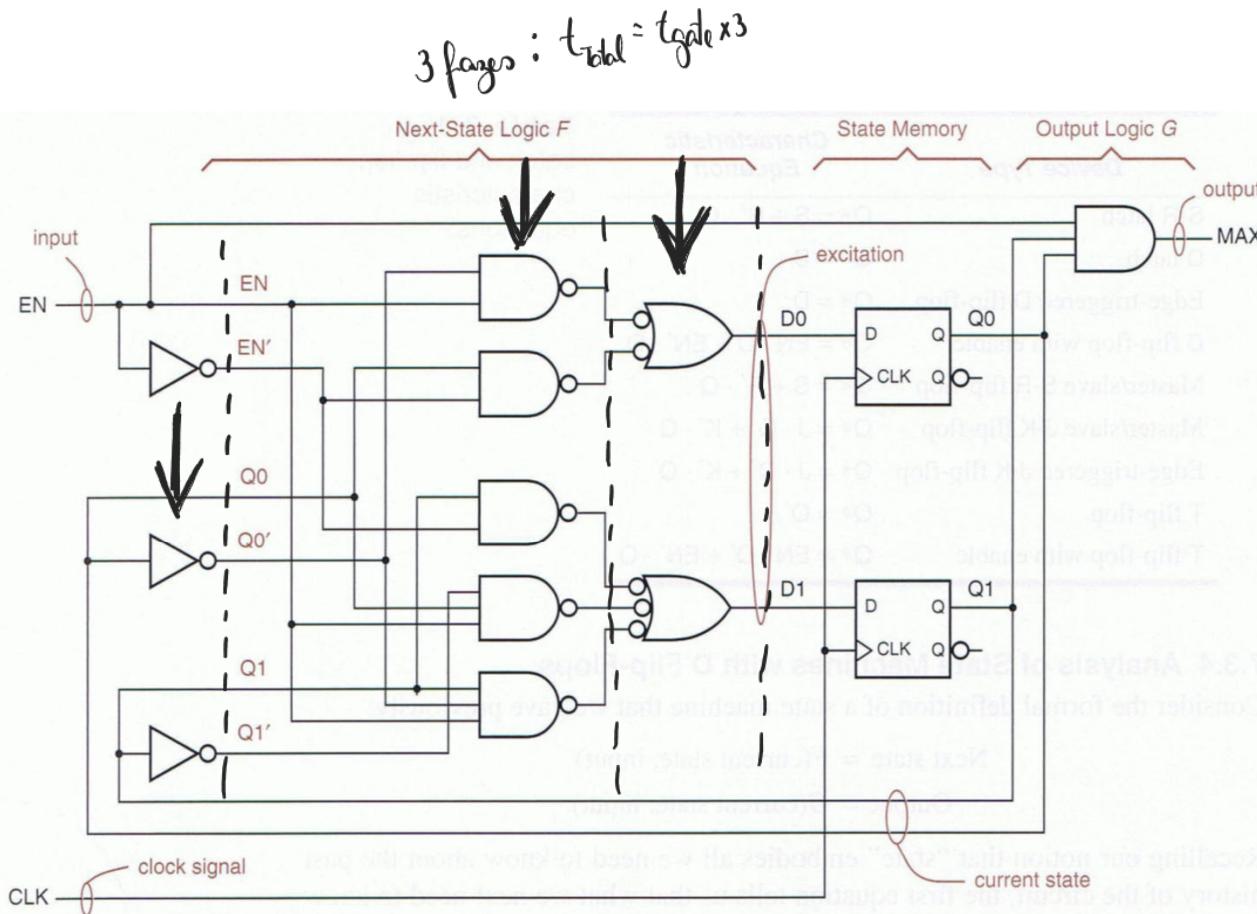


Figure 7-38 Clocked synchronous state machine using positive-edge-triggered D flip-flops.

Só vai funcionar  
se o tick for maior

$$T_{\min} = ? \quad 5 + 3 + (4 \times 3) = 8 + 12 = 20 \text{ ns}$$

$$f_{\max} = ? \frac{1}{20 \text{ ns}} = \frac{100 \text{ MHz}}{20 \text{ ns}} = 50 \text{ MHz}$$

Consider:

$$T_{pHL} = 4 \text{ ns} \quad t_{pLH} > t_{pHL}$$

$$T_{pLH} = 5 \text{ ns}$$

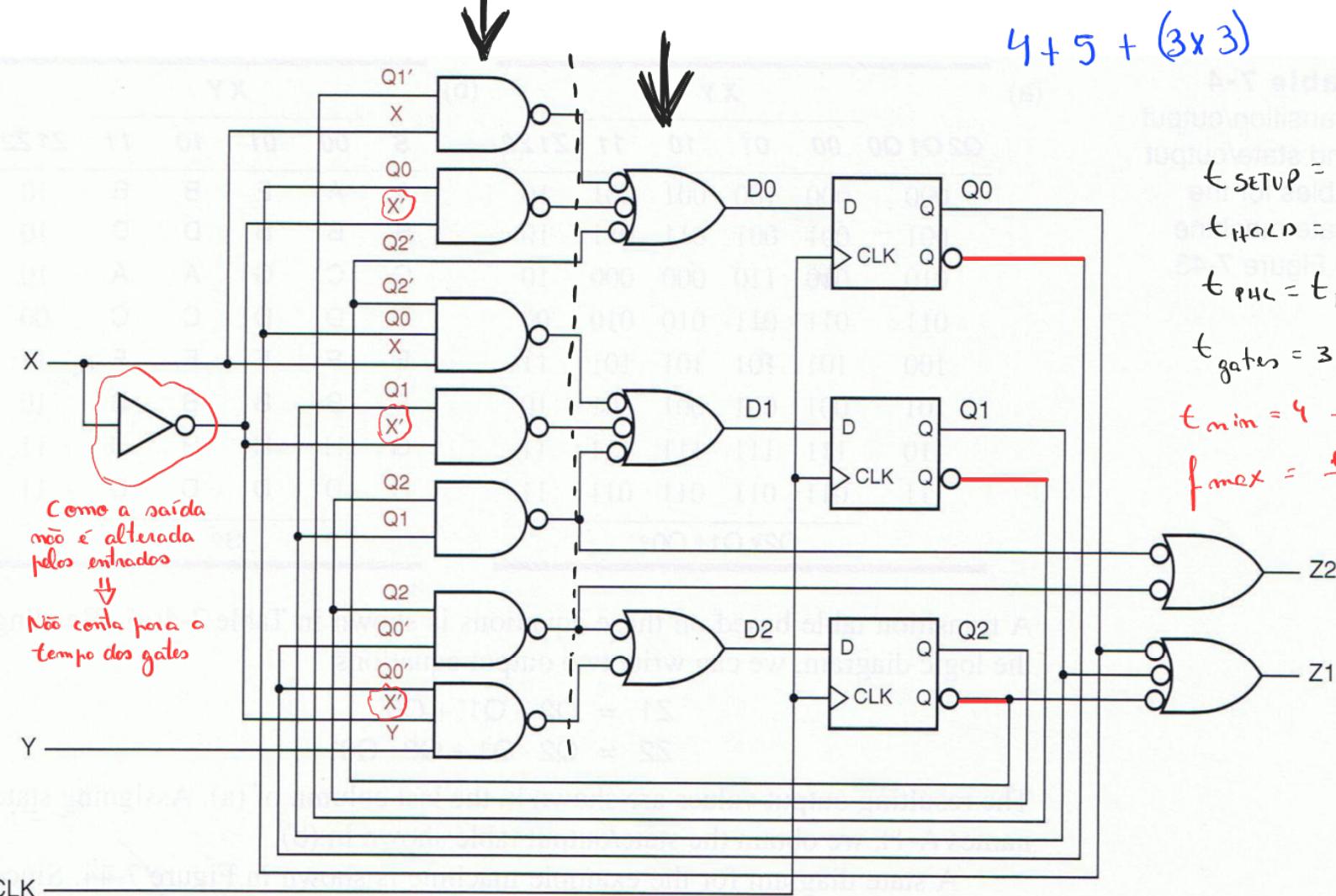
$$T_{\text{setup}} = 3 \text{ ns}$$

$$T_{\text{hold}} = 1 \text{ ns}$$

$$T_{\text{gate}} = 4 \text{ ns}$$

(assume that all gates exhibit the same delay)

# Another FSM Example



$$4+5+(3\times 3)$$

$$t_{\text{SETUP}} = 4 \text{ ms}$$

$$t_{\text{fold}} = 2 \text{ ms}$$

$$t_{\text{PUL}} = t_{\text{PLH}} = 5 \text{ ms}$$

$$t_{gates} = 3 \text{ ms}$$

$$f_{\text{min}} = 4 + 5 + 6 = 15$$

$$f_{\text{max}} = \frac{1000}{15} \approx 66 \text{ MHz}$$

**Figure 7-43** A clocked synchronous state machine with three flip-flops and eight states.

# Another FSM Example

## Excitation Equations

$$D_0 = Q_1' \cdot X + Q_0 \cdot X' + Q_2$$

$$D_1 = Q_2' \cdot Q_0 \cdot X + Q_1 \cdot X' + Q_2 \cdot Q_1$$

$$D_2 = Q_2 \cdot Q_0' + Q_0' \cdot X' \cdot Y$$

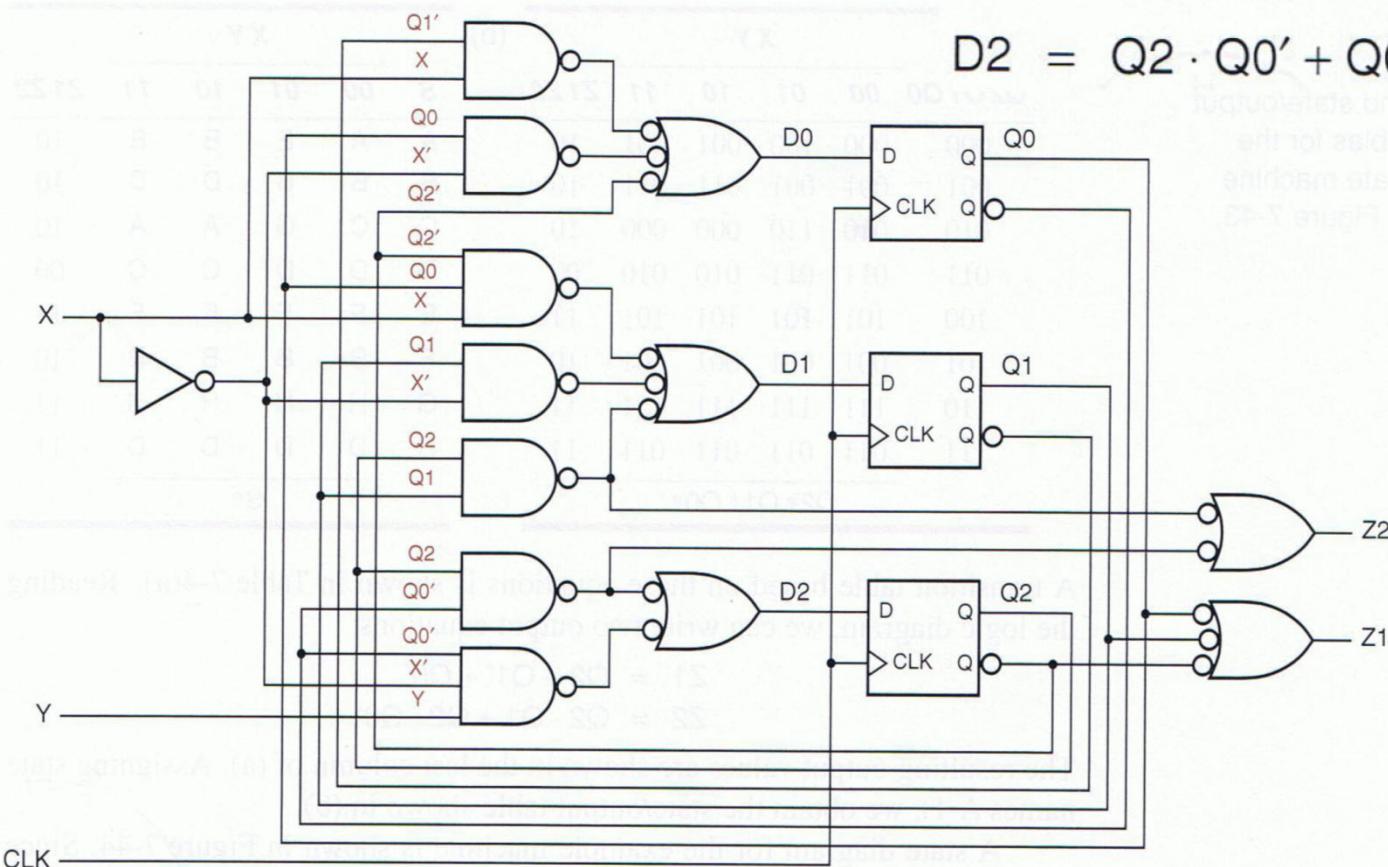


Figure 7-43 A clocked synchronous state machine with three flip-flops and eight states.

# Another FSM Example

## Transition Equations

$$Q0^* = Q1' \cdot X + Q0 \cdot X' + Q2$$

$$Q1^* = Q2' \cdot Q0 \cdot X + Q1 \cdot X' + Q2 \cdot Q1$$

$$Q2^* = Q2 \cdot Q0' + Q0' \cdot X' \cdot Y$$

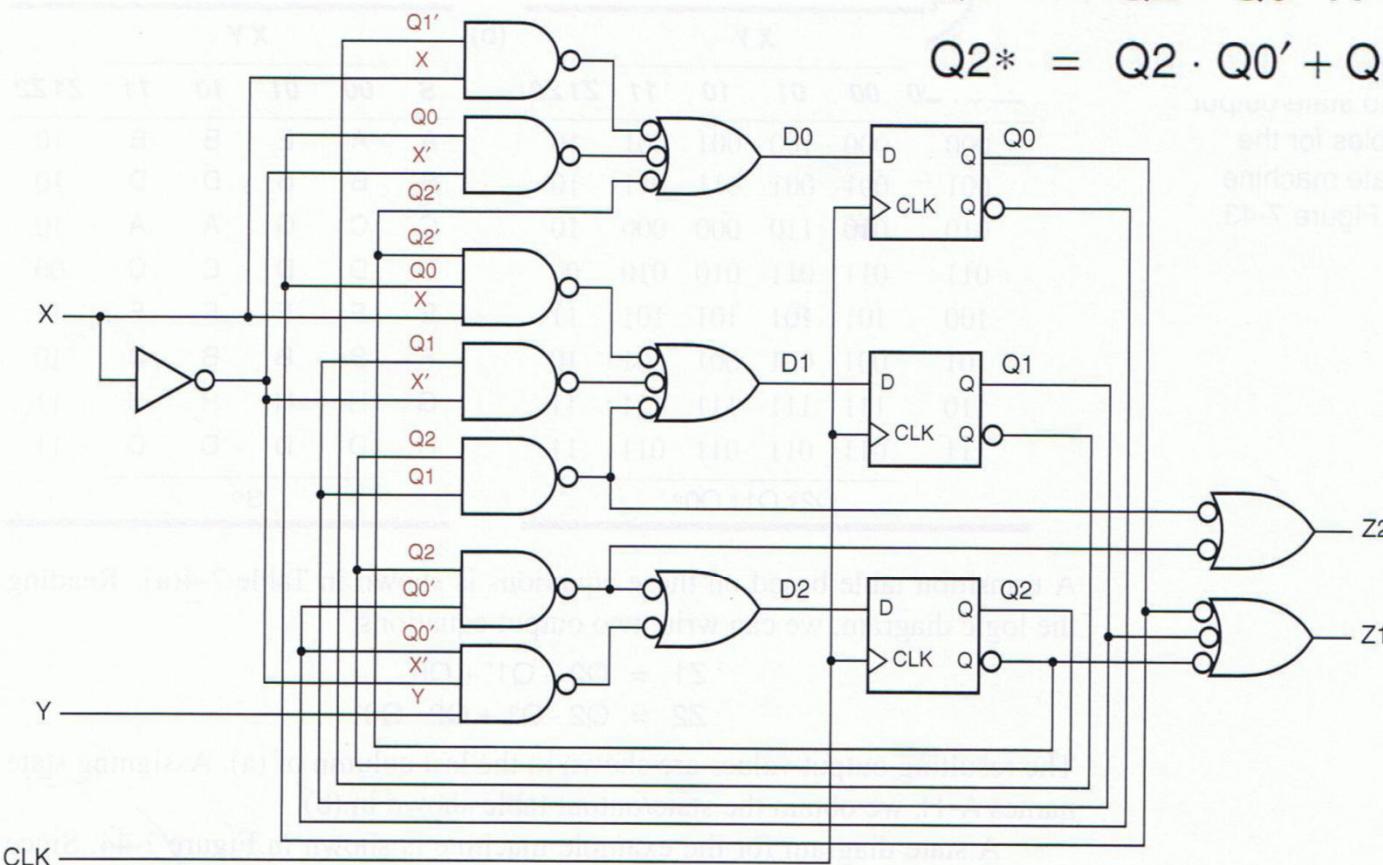


Figure 7-43 A clocked synchronous state machine with three flip-flops and eight states.

# Another FSM Example

## Output Equations

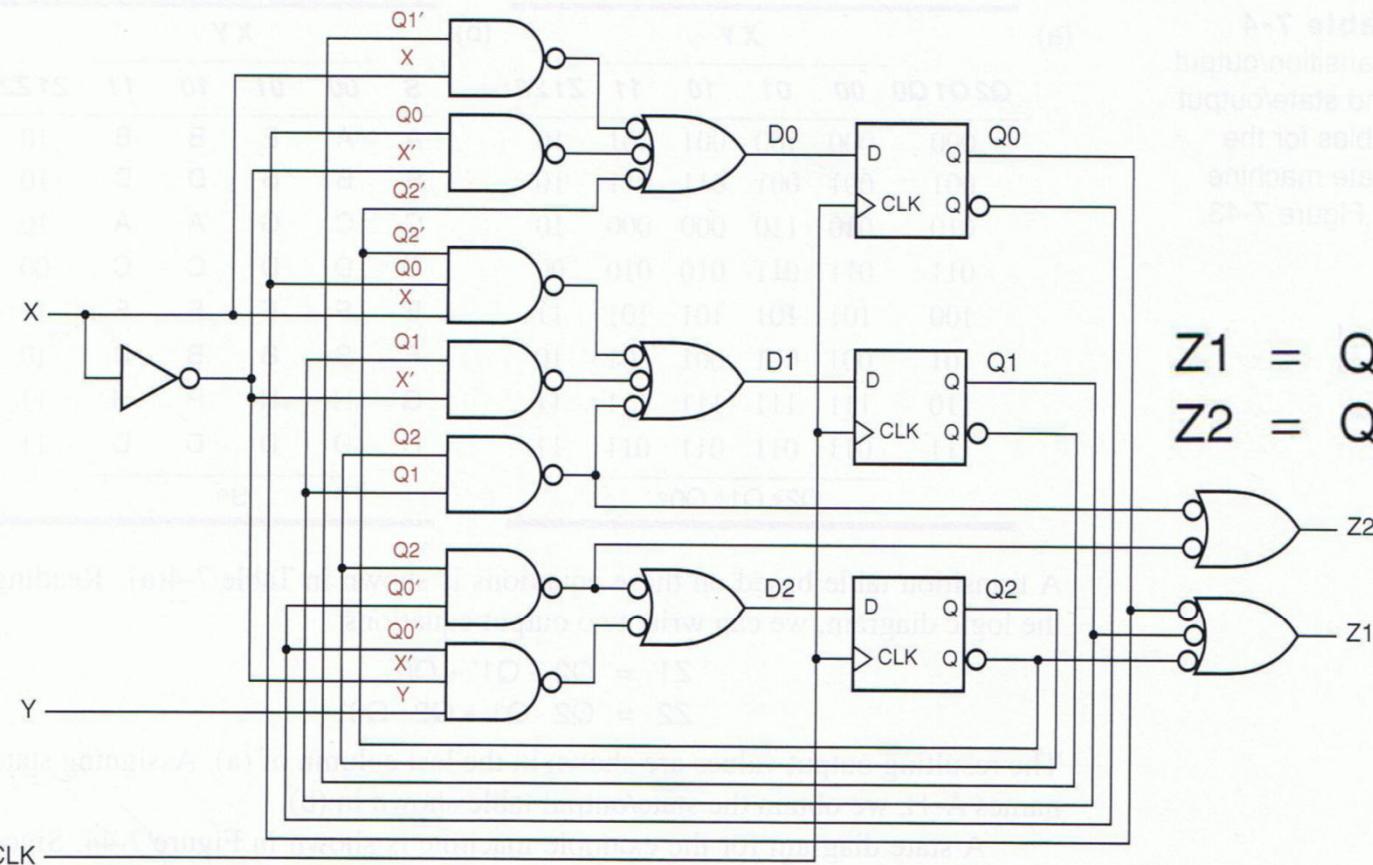


Figure 7-43 A clocked synchronous state machine with three flip-flops and eight states.

# Another FSM Example – Transition / Output and State / Output Tables

$$Q_0^* = Q_1' \cdot X + Q_0 \cdot X' + Q_2$$

$$Q_1^* = Q_2' \cdot Q_0 \cdot X + Q_1 \cdot X' + Q_2 \cdot Q_1$$

$$Q_2^* = Q_2 \cdot Q_0' + Q_0' \cdot X' \cdot Y$$

$$Z_1 = Q_2 + Q_1' + Q_0'$$

$$Z_2 = Q_2 \cdot Q_1 + Q_2 \cdot Q_0'$$

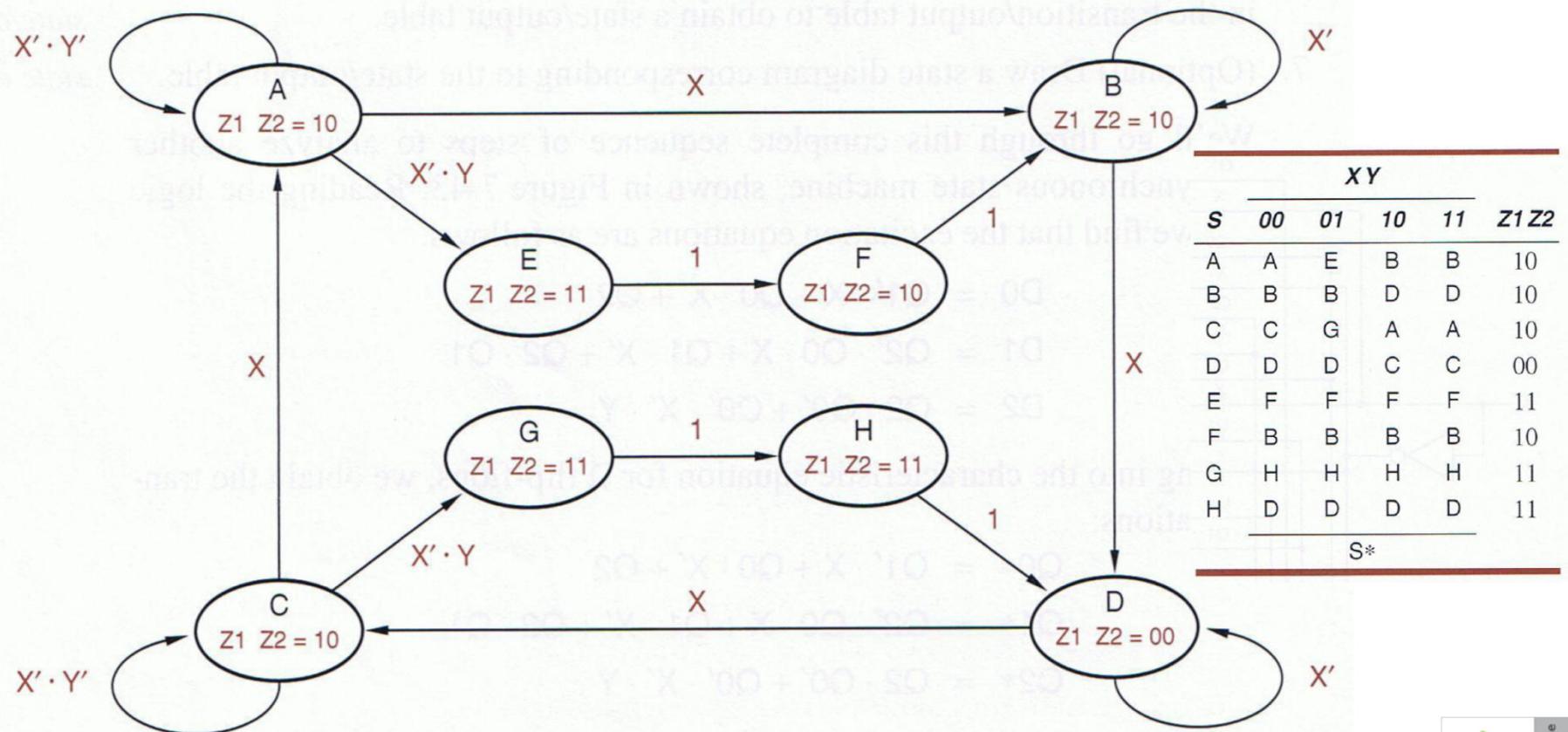
**Table 7-4**  
Transition/output  
and state/output  
tables for the  
state machine  
in Figure 7-43.

			XY							
			Q2	Q1	Q0	00	01	10	11	Z1 Z2
			000	000	100	001	001	10		
			001	001	001	011	011	10		
			010	010	110	000	000	10		
			011	011	011	010	010	00		
			100	101	101	101	101	11		
			101	001	001	001	001	10		
			110	111	111	111	111	11		
			111	011	011	011	011	11		
			Q2* Q1* Q0*				S*			

# Another FSM Example

## State Diagram

**Figure 7-44** State diagram corresponding to Table 7-4.



# Conclusion

- At the end of this lecture and corresponding lab, it is fundamental to know how to analyse sequential circuits described by finite state machines and implemented with D type flip-flops, including functional/behavioral and timing aspects
- Plan for the next lectures
  - Synthesis of sequential circuits (Finite State Machines)
  - Standard sequential circuits
    - Registers and shift registers
    - Counters
  - Iterative vs. sequential circuits

Reading chapter 7 (4<sup>th</sup> ed.) or chapter 10 (5<sup>th</sup> ed.) of John F. Wakerly, "Digital Design – Principles and Practices", Pearson – Prentice Hall, is highly recommended.