README

Location of SOF file: Located at the lab1_template_de1soc folder and is named Basic_Organ_Solution.SOF

Status: Lab is working as expected. The DE1_Soc generates all 8 frequencies correctly according to the audio data shown in line 2 of the Signal Tap LCD. Also, in line 2 of signal tap the position of switches is displayed in hexadecimal. The LED was built using an FSM and it works as expected bouncing back and forward, changing states every second.

Simulation: I have provided a folder called Model_sim, where all the testbenches are located. I tested 3 modules: couter (clock divider module using a counter logic), frequency generator (selection of the frequencies generated by the clock divider) , and FSMLED (finite machine logic for the LED). The files for these modules and its corresponding testbenches are : couter: clk.sv & clk_tb.sv, frequency generator : frequency_gen.sv & frequency_gen_tb.sv, FSMLED: FSM_LED.sv & FSM_tb.sv. All these files are in a model sim project called LAB1. I have also included the wave files for clk_divider: clk_div_wave.do and for frequency_generator: wave_freq_gen.do. For simplicity I have also added the screenshots in this file.

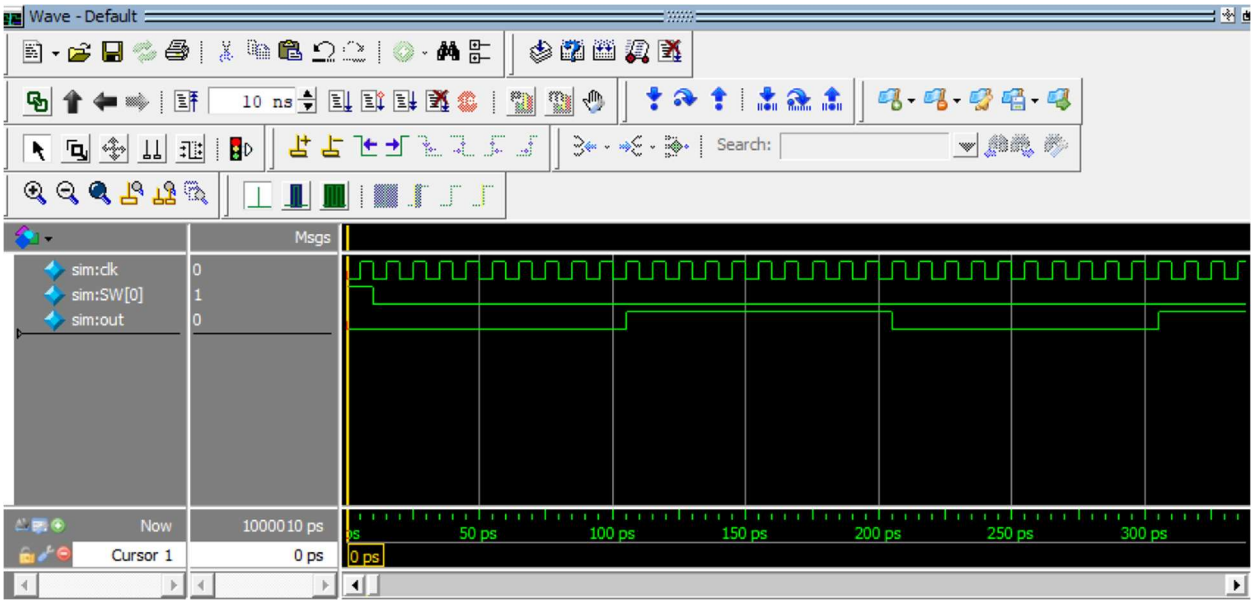

Figure 1

Clk_tb.sv: It shows the clock being divided by 10, where the output changes the output from 1 to 0 every 10 positive edges of the clock

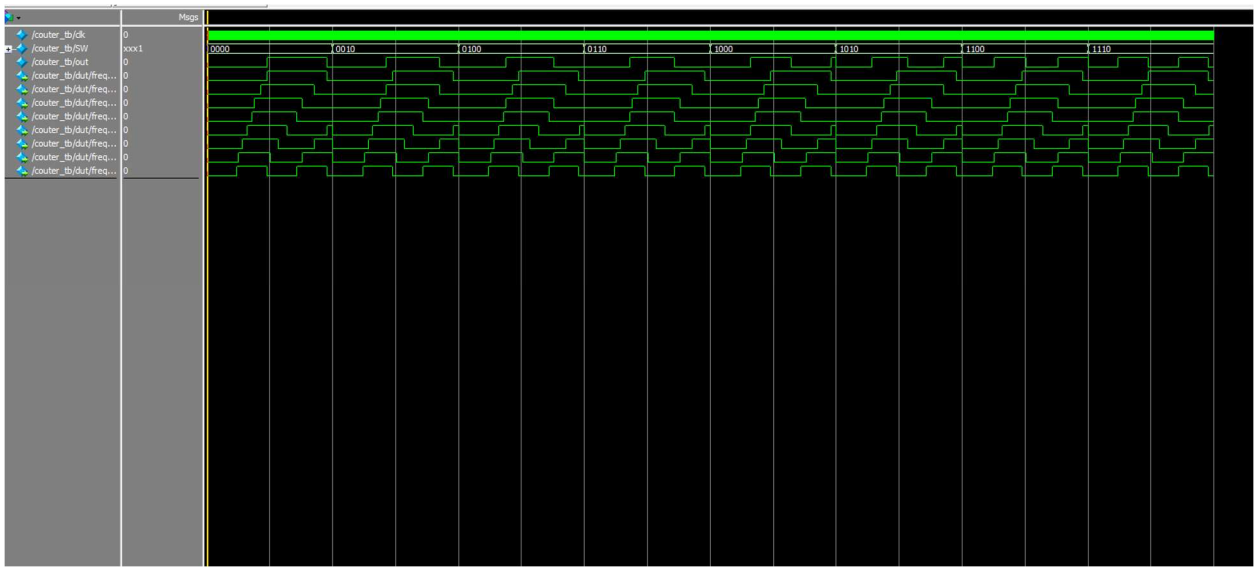

Figure 2

Frequency_gen_tb.sv: It shows that every time that the SW(switch) changes its value it changes the frequency. The bottom 8 frequencies are the output of different clock dividers and the Switch is selecting witch one is going to the output.

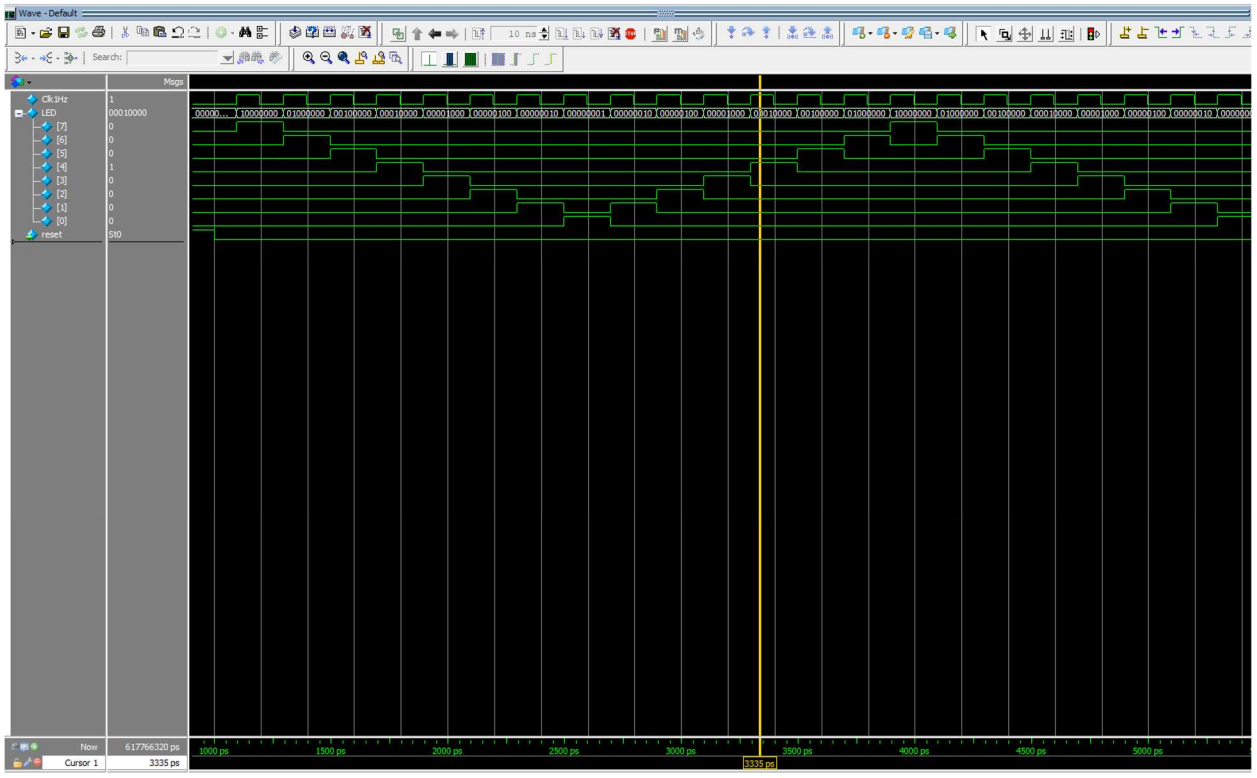

Figure 2

FSM_tb.sv: This shows the change of the states synchronized to the clock cycle and also its possible to visualize that the output is going back and forward with its value.