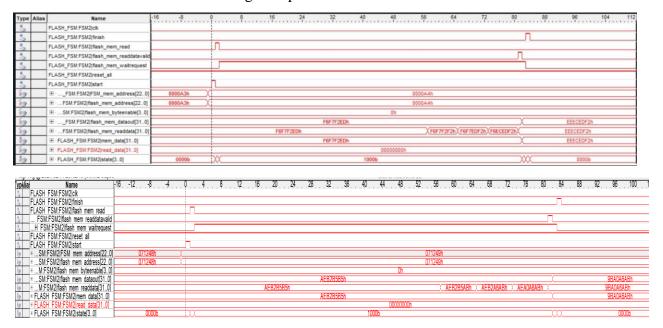
Location of SOF file: Located at the lab2_template_de1soc folder and is named simple_ipod_solution.SOF

Status: Lab is working as expected. The DE1_Soc plays the song and repeats after the song ends, Keys 0, 1 and 2 speed up, slows down and reset the speed respectively and the key D from the keyboard stops the music while key E starts the music, however keys b and f were not implemented.

Simulation: I have provided a folder called Model_sim, where all the testbenches are located. My lab is composed of three FSMs to output the music. The first FSM is the address handle fsm(ADDR_FSM.sv) that basically loops through all the addresses of the music and sends to the next fsm once every address. The second FSM handles the FLASH memory, where it sends the received address and ouputs the received flash memory data. And finally, the third one divides the 32 bit address into 2 and sends the most significant bits to the audio signal.

1. Flash FSM simulation and signal tap

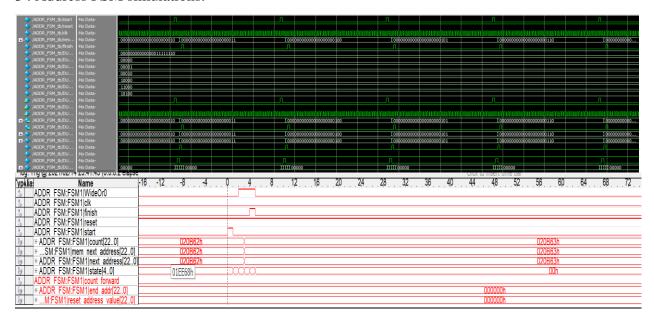


2. Audio signal FSM simulations and signal tap

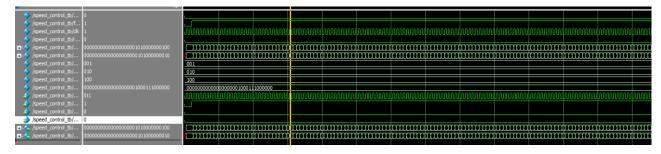
4 /audio frm tb/dk	lo			_								_		_		_	-	_		_	
// /audio_fsm_tb/reset																	1				
/audio_fsm_tb/start							1				1		1								
// /audio_frm_tb/DUT/done_count	0									1		1									
- /audio_fsm_tb/data	00000100000001	00000100000001	01000000111	1111111	0																
/sudio_fsm_tb/finish	0											1									
- /audio_fsm_tb/audio_signal	00001000	00000000	[00000]	000	00000	1000	100000	1000	(000000	1000	100000	1000	000000	000	000000	. 1000	00000	. 1000.	. 100000.	. 1000.	00000
/audio_fsm_tb/DUT/idle	0000	0000																			
/audio_fsm_tb/DUT/send_upper_data	0001	0001																			
/audio_fsm_tb/DUT/send_lower_data	0010	0010																			
/audio_fsm_tb/DUT/waiting	9100	0100															1				
/audio_fsm_tb/DUT/finished	1000	1000																			
/audio_fsm_tb/f0UT/dk	St0									_				_							
/audio_fim_tb/DUT/reset	St1																				
/audio_fsm_tb/DUT/start	St0						1		1		1										
Jaudio_fsm_tb/OUT/data	00000100000001	00000100000001	d1000000111	1111111	0																
4 /audio_fsm_tb/DUT/finish	0																_				
// /audio_fsm_tb/DUT/audio_signal	00001000	00000000	[000000]	000	00000	1000	100000	1000	100000	2000	(000000	1000	00000	000	000000	. 1000	00000	. [000.	. 100000.	. 1000.	(00000)
// /audio_fsm_tb/DUT/send_upp	0																				
// /audio_fsm_tb/(DUT/send_low)																					
/audio_fem_tb/fXUT/wait_logic																					
- / /audio_fsm_tb/DUT/lowerdata	00001000	00001000																			
- /audio_fsm_tb/DUT/upperdata	00000011	00000011																			
- /audio_fsm_tb/DUT/audio_data	00001000	00000000	[00000 Y	000	00000	1000	100000	1000	100000	1000	[000000	1000	100000	(000	100000.	. 1000.	000000	. 1000.	. 1000000.	1000	. 100000 I
/audio_fsm_tb/DUT/state	0000	0000	0100	0000	0100	I 0000	10100	0000	X 0 100	0000	10100	0000	0100	00000	0100	0000	10100	0000	0100	X 0000	0100
/audio_fon_tb/DUT/Clock_228Hz	×																				
/ Jaudio_fsm_tb/DUT/count	00000	00000		00000		00000		(00000		000000		00000		0000		00000		0000	0		0

Type	Alias	Name	-990Value 989	-1024	-512	0	512	1024	1536	2048	2560	3072	3584	4096	4608	5120	5632	6144	6656	7168
*		Audio_fsm:FSM3 clk	0													10	17	100		
*		Audio_fsm:FSM3 done_count	0																	
*		Audio_fsm:FSM3 finish	0																	
*5		Audio_fsm:FSM3 reset	1																	_
*		Audio_fsm:FSM3 start	0																	
3		Audio_fsm:FSM3 audio_data[70]	EAh		EAh			EBh					E3h				DDh			E2h
8		Audio_fsm:FSM3[audio_signat[70]	EAh		EAh			EBh					E3h				DDh			E2h
19		Audio_fsm:FSM3[count[12_0]	0		0								0							0
59		Audio_fsm:FSM3[data[310]	E3EBEAE1h	E	3EBEAE1h					EBEAE	3DEh						DDDF	2E7h		
19		Audio_fsm:FSM3[state[30]	0000ь		0000b			0100b					0000ь				0100b			0000b
59		① Audio_fsm:FSM3[M[190]	008E0h									008E0h								
19		(+) Audio_fsm:FSM3(count[190]	OOh				00h													

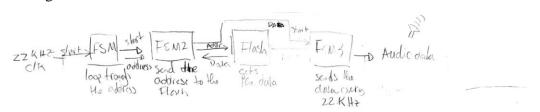
3 . Address FSM simulations.

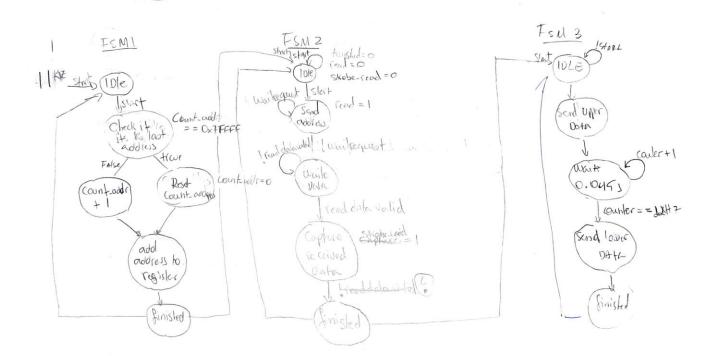


4 Speed control simulation



Before starting the lab I built this schematic.





And at the end the overall schematic is:

