4.2.2 Special Definition

Term	Definition
NW	N-WELL
PW	P-WELL
RW	NW hole in DNW
MOS	Transistor structure consisting of a source, a drain, and a gate
NMOS	N type MOS
PMOS	P type MOS
SR_DOD	Dummy OD
SR_DPO	Dummy PO
DMn	Dummy Metal
DMn_O	OPC dummy metal. The rules of DMn_O are the same as real metal, Mn
CHIP	GDS EXTENT or GDS bounding box
Seal-ring enhanced zone	The region between the seal-ring and Chip_Boundary
ENDCAP	The PO extension of a transistor gate in the width direction onto the field
CB	Passivation opening for wire bond design
CBD	Passivation opening for flip chip design
RV	Redistribution VIA for connecting AP-MD with Mtop
CB2_FC	Passivation 2 opening for flip chip
CB2_WB	Passivation 2 opening for wire bond
AP	Al pad metal layer after CB or CBD in Cu process
AP RDL	Al pad redistribution layer
PM	Polyimide opening
UBM	Under bump metallurgy
A~B	A ≤ rule value ≤ B
PRL	Parallel run length
Line-end (end)	Layer edge width ≤ W μm [edge formed by 2 consecutive 90-90 degree convex corners] W value is defined in each layer
Run	Layer edge except Layer line-end edge
Lower_Metal/VIA	Intermediate under layer of metal/VIA EX: Lower_Metal of VIA3 is M3. Lower_VIA of VIA3 is VIA2.
Upper_Metal/VIA	Intermediate upper layer of metal/VIA EX: Upper_Metal of M2 is M3. Upper_VIA of M2 is VIA2.