

# Power Supply Noise Reduction

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An introduction into the basics of power supply noise reduction using supply bypassing and decoupling.

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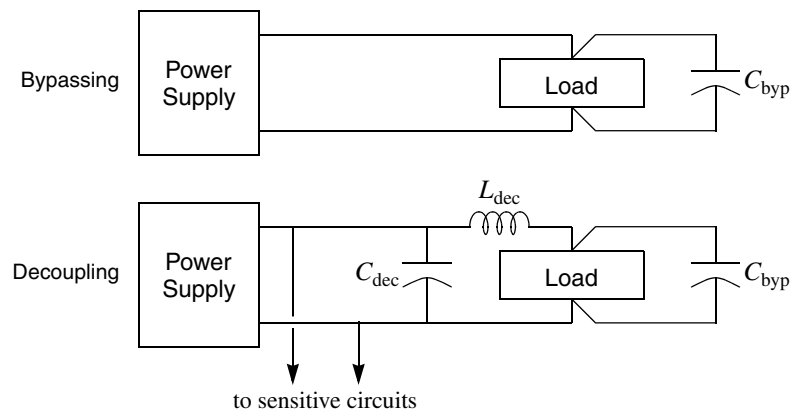
## 1 Introduction

Many of the problems that appear out of Murphy's box upon transforming a design from the mythical world of textbooks and SPICE to the real world emanate from the non-ideal power supply. Real power supplies can cause noise and spurious oscillations that can force the designer into a frustrating glitch hunt. Rules of thumb can usually be applied successfully to simple problems, but a little understanding and forethought will usually provide clean solutions to even the more obscure problems. With this paper, I hope to provide the understanding of some of the dynamics of power distribution. The forethought is up to you.

## 2 Definitions

Bypassing and decoupling are often poorly understood and poorly applied. Many designers believe bypassing and decoupling are synonymous. They are not; they are distinct concepts and each is a solution to a different problem (see Figure 1).

FIGURE 1 *Bypassing and decoupling.*



**Bypassing** is the reduction of high frequency current flow in a high impedance path by shunting that path with a bypass, usually a capacitor (in this case,  $C_{byp}$ ). Bypassing is used to reduce the noise current on power supply lines.

**Decoupling** is the isolation of two circuits on a common line. The decoupling network is usually a low pass filter and the isolation is rarely equal in both directions. Decoupling is used to prevent transmission of noise from one circuit to another. In the figure a bypass capacitor,  $C_{byp}$ , is shown along with the decoupling circuit,  $L_{dec}$  and  $C_{dec}$ . This is because in practice bypassing is always used when decoupling.

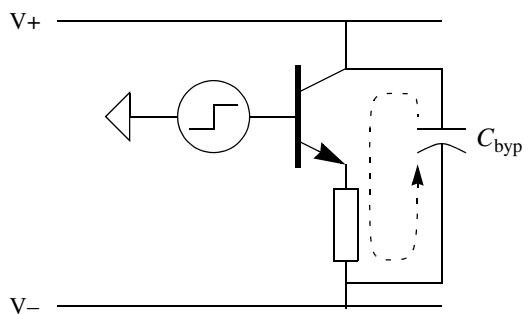
Most circuits require bypassing, not decoupling. Using decoupling techniques to accomplish bypassing will give disappointing, if not disastrous, results. Complete understanding of both concepts is vital. We begin with bypassing.

### 3 Bypassing

Due to the finite bandwidth of all voltage regulators, their output impedance increases with frequency. This can be modeled as an inductor in series with the output. Typical values lie between 1  $\mu\text{H}$  and 2  $\mu\text{H}$  for a linear three terminal regulator. The output impedance of switching regulators varies widely and should be measured for each case. The interconnecting leads add about 20 nH per inch. When an active load is connected, the time varying current demand creates a noise voltage across these inductors. This noise voltage can be reduced in only two ways: reduce the rate of change of the current ( $di/dt$ ) passing through the inductor, or reduce the inductance. Bypassing reduces the rate of change of the current through the inductor.

In bypassing, a secondary, high frequency low impedance path (a capacitor) is provided for the varying currents from the load that shares as little inductance as possible with the power supply leads. The key to successful bypassing is to properly determine the flow of current from a load and to supply a return path that is not common with any other part of the circuit (see Figure 2). The bypass path must be a significantly lower impedance at the frequency of interest than the power supply leads. It is always better to use many small parallel capacitors than one large one. This is because the equivalent series inductance does not vary significantly with capacitance. The parallel bypass paths achieved with the small capacitors results in a much lower total inductance.

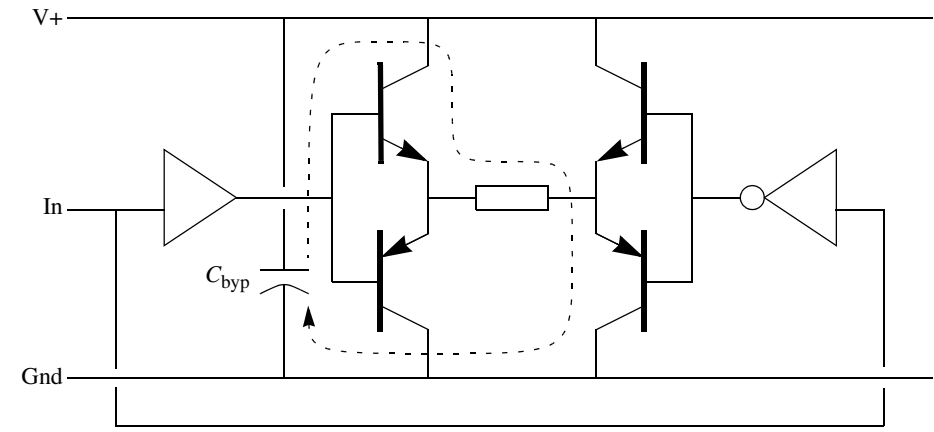
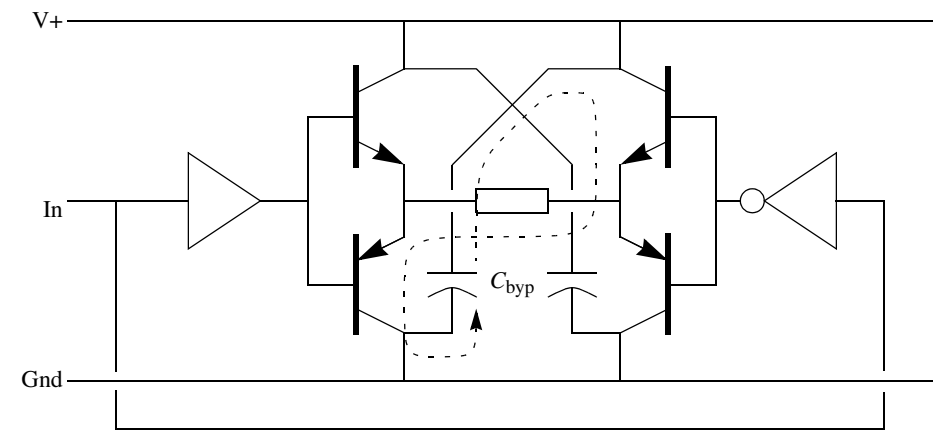
FIGURE 2 Proper bypassing.



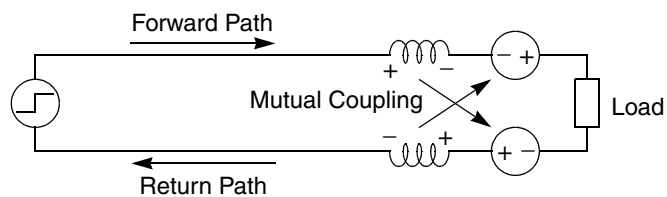
Care must be taken when determining the return current path. It is often not obvious at first glance as demonstrated in Figure 3. In this case the standard bypassing is applied, which causes a current to flow in the ground and supply leads, which generates a noise voltage. In Figure 4, this situation is remedied.

### 4 Reducing Inductance

As mentioned above, one way to reduce the noise voltage developed in the power supply inductance is to reduce that inductance. To reduce the inductance of a linear regulator, you can either increase its bandwidth or decrease its open loop output impedance. Both are really not options unless you design your own regulator. There are also two methods for decreasing the inductance of the power supply bus. One is to decrease its self inductance, and the other is to increase the mutual coupling to its return path. A wire's self

FIGURE 3 *Improper bypassing. Bypass current runs through shared supply lines.*FIGURE 4 *Proper bypassing.*

inductance can be reduced by decreasing its length, increasing its radius (a small effect) or running multiple isolated wires.

FIGURE 5 *Cancellation of inductance using mutual coupling.*

The benefit of increased mutual coupling is illustrated in Figure 5. The coupling between the forward and return paths cause the voltage generated in the self-inductance of one path to be cancelled by the voltage induced from the coupling from the other path. With perfect coupling also comes perfect cancellation and zero effective inductance. To increase the mutual coupling between paths requires decreasing the distance

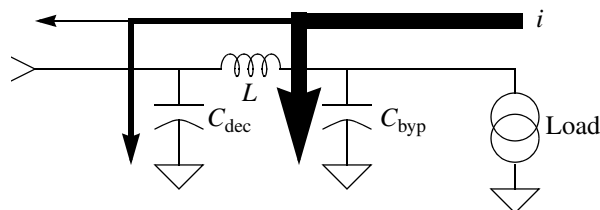
between them or increasing their width. It is best to place the forward and return paths as close as possible. Using supply planes, as opposed to supply traces, along with a ground plane, causes this to happen naturally.

When using two layer boards, it is difficult to lay out power supply planes. The second best technique is to use a power grid combined with a ground plane. This reduces the self inductance of the supply by running many isolated traces to the load. This technique can be very successfully applied on digital boards. On analog boards, even this is difficult to do, especially when isolation between circuits is required. In this case, the preferred method is to structure the supply  $C_{dec}$  like a tree. This minimizes the length, and hence the inductance, of the supply  $C_{dec}$ . Avoid long serial, or “daisy chained” power supply traces.

## 5 Decoupling

When it is desired to isolate one circuit from the noise of another, you should reduce the amount of shared supply trace between them. If that is not sufficient, decoupling should be used. Decoupling decreases noise transmission in two ways (see Figure 6). First, since decoupling always consists of a high impedance element in series with the supply line, it assists the bypassing; assuring that the noise current will flow through the low impedance bypass element rather than the supply. Second, it acts as a low pass filter so that the high-frequency content of any current that does pass through the series element will be attenuated, making it more likely that the regulator will be able to react and keep the supply voltage stable.

FIGURE 6 Current paths in a typical decoupling network.



The series element may either be a resistor (when DC voltage drop is not a problem), or an inductor, or both. Sometimes even a parallel resonant tank circuit may be used if the noise is concentrated at one frequency.

When choosing component values for a decoupling network, two parameters are important. First, of course, is isolation versus frequency. Second, and often overlooked, is the impedance seen by the load. This is important because a large output impedance will cause the load noise current to be translated into a large noise voltage. Typically, a large series inductor will be chosen to give good isolation. This then requires a large bypass capacitor in order to keep the output impedance at a reasonable level. Therefore the decoupling network becomes large and expensive. For both economy and size, the smallest inductance that gives the required isolation should be used. It is sometimes possible to get good isolation, low output impedance, and small component values by using a multi section ladder filter rather than a single series inductor. This allows the cutoff

frequency of the filter to increase while keeping the isolation high at the frequency of interest. This relaxes the requirements on the bypass capacitor.

When using the circuit in Figure 6, care must be taken to assure that there is negligible noise on the power supply side. If not,  $C_{dec}$  will couple the noise on to ground, possibly creating more problems than you started with.

## 6 Damping

The more experienced among us may realize that there are serpents in this Garden of Eden. When we added this bypass capacitors to the stray inductance, the power supply became an under damped resonant circuit. This leads to ringing and noise peaking on the supplies, which may end up on the output. Often times, this problem is severely aggravated by the use of LC decoupling networks. For example, consider the decoupling network shown in Figure 7. When a 20 mA step is applied, the resulting ringing had a peak amplitude of over 500 mV and a time constant for the decay of over 40  $\mu$ S. It is clear that care must be taken in designing bypassing and decoupling networks to minimize transient response amplitude and provide damping. Transient response can roughly be predicted with

$$V_{peak} = I_{peak} \sqrt{\frac{L}{C}} \text{ for } Q \gg 1 \quad (1)$$

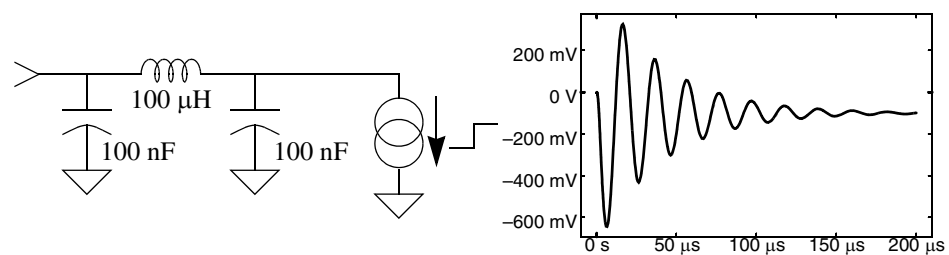
where for parallel RCL

$$Q = \sqrt{\frac{R^2 C}{L}} \text{ and } \tau = 2RC \quad (2)$$

and for series RCL

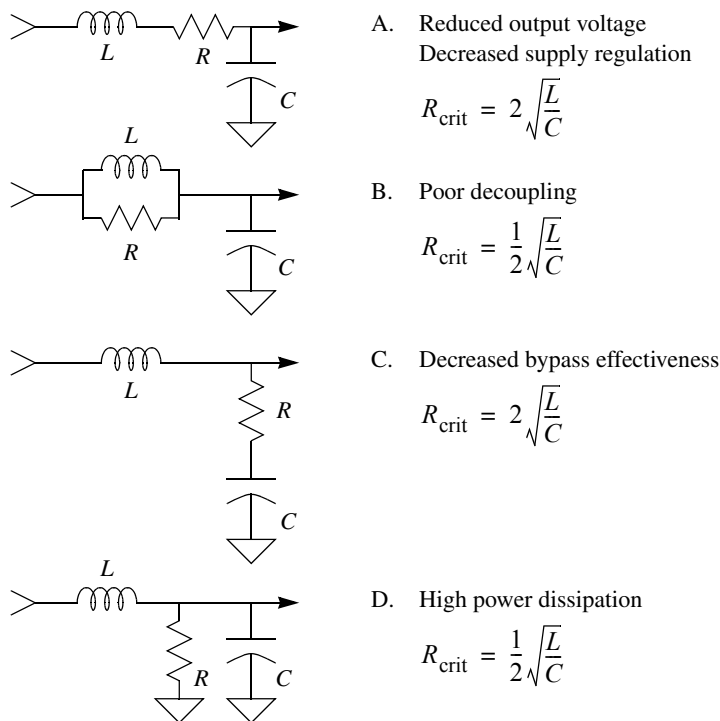
$$Q = \sqrt{\frac{L}{R^2 C}} \text{ and } \tau = 2\frac{L}{R} \quad (3)$$

FIGURE 7 A decoupling network and its measured response to a 20 mA current step.



There are several techniques for providing damping, as shown in Figure 8. The damping that gives the best isolation and the lowest output impedance at high frequencies is method A. Unfortunately it suffers from a high DC series resistance, which reduces output voltage and supply regulation. Methods B and D are usually unacceptable. This leaves C as the preferred damping method when low DC output resistance is required. The problem with C is its high frequency output impedance. By adding series resistance to the bypass capacitor, the amplitude and high frequency components of the transient

FIGURE 8 Several methods for damping decoupling networks along with the value of the resistor needed for critical damping.



response to the load are increased. The amplitude of the critically damped response is twice that of the undamped. When the resistive parasitics in the components are not enough to provide proper damping, careful consideration should be given to whether the advantages of damping outweigh the disadvantages.

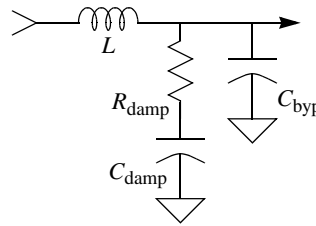
It is not necessary to provide damping for every bypass capacitor; rather a single large capacitor should be added to each board and damping provided for that capacitor. This is shown in Figure 9. The single large capacitor must be at least 16 times larger than the sum of all of the high speed bypass capacitance connected to the supply to completely dominate in the damping resistor calculation. If the capacitor is large, and the inductor is small, then often times the equivalent series resistance (ESR) of the capacitor will be large enough to damp the network. With this approach, we have in effect switched to method D, but we added a large DC blocking capacitor in series with the damping resistor to avoid the excess power dissipation problem.

It is necessary that both the series RCL network consisting of  $L$ ,  $R_{\text{damp}}$ , and  $C_{\text{damp}}$ , and the parallel RCL network consisting of  $L$ ,  $R_{\text{damp}}$ , and  $C_{\text{byp}}$  be properly damped. This requires that both

$$R_{\text{damp}} > 2\sqrt{\frac{L}{C_{\text{damp}}}} \quad (4)$$

and

FIGURE 9 The preferred approach for providing damping to a decoupling network.



$$R_{\text{damp}} < \frac{1}{2} \sqrt{\frac{L}{C_{\text{byp}}}} \quad (5)$$

However, the requirement that  $C_{\text{damp}} > 16C_{\text{byp}}$  assures that a value of  $R_{\text{damp}}$  exists that satisfies both (4) and (5). Choosing a larger ratio between  $C_{\text{damp}}$  and  $C_{\text{byp}}$  results in a range of resistor values satisfying both inequalities. This is valuable if for no other reason that the value of  $R_{\text{damp}}$  can only be specified to within some finite tolerance. In addition, it also happens that if  $C_{\text{damp}}$  is chosen large enough, its ESR will likely satisfy both (4) and (5); eliminating the need to add an additional discrete resistor to implement  $R_{\text{damp}}$ .

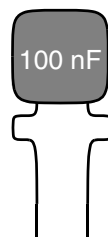
When damping decoupling networks like the one in Figure 7, it is usually a good idea to assure that both sides of the network are damped. Damping is typically provided on the power supply side by the large electrolytic capacitors at the output of the regulators.

## 7 The Recipe

I have found that the following procedure works well when designing power supply noise reduction networks.

1. Identify all high derivative ( $di/dt$ ) current sources and sinks and identify their return paths. Often there exist multiple paths, all of which must be bypassed. For example, and op-amp sources current from the positive supply, and sinks current from the negative supply. A good limit for the maximum  $di/dt$  for a total board is 10 mA/ $\mu$ S.
2. During layout, place the forward path as close as possible (on opposite sides of the board) to the return path and maximize the trace width to minimize inductance by mutual coupling. If possible, lay out power supply busses in a grid or a plane. Avoid long serial supply traces.
3. Bypass all high derivative ( $di/dt$ ) current sources and sinks with capacitors that work well at the frequencies of interest. Ceramic capacitors are good for this application because they are inexpensive, small, and work well at high frequencies. Avoid capacitors with formed leads (see Figure 10) because of their large equivalent series inductance (ESL).
4. If needed, choose the decoupling elements based on required isolation and frequency response requirements. If using a simple series inductor, its value should be as small as possible. Avoid high-Q inductors, in this application low-Q is desirable.
5. Choose a damping resistor and capacitor that satisfy (4) and (5). Use (5) to choose the resistor and (4) to choose the capacitor. Be sure to include the capacitor ESR as

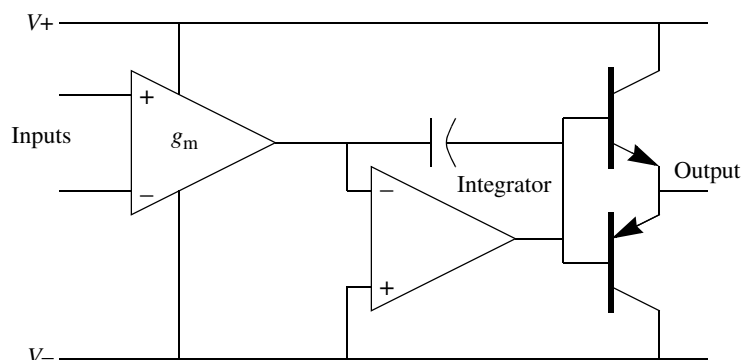


FIGURE 10 *Capacitor with formed leads.*

part of the total damping resistance. When using (4) to compute the resistance needed for critical damping include the effective output inductance of the regulator, the parasitic inductance of the wiring, and the effective series inductance of the capacitor along with the decoupling inductance. Attempt to choose a capacitor large enough so that the ESR provides adequate damping. Tantalum electrolytic capacitors usually work well in this role. If the ESR of the capacitor is not large enough to critically damp the network, then additional resistance should be added to the large capacitor.

## 8 Operational Amplifiers

Op amps can be quite sensitive to noise on the power supply, and it is informative to look at how op amps are designed in order to get a better feel for why they are sensitive and what to do about it. Figure 11 shows the block diagram of a typical ( $\mu A741$ ) op amp.

FIGURE 11 *Block diagram of a  $\mu A741$  operational amplifier.*

Notice that the integrator has its non-inverting input referred to the negative supply. This means that any high frequency noise that exists on the negative supply gets coupled to the output. In other words, if the negative supply voltage changes abruptly, the integrator will force the output to follow the change. When the entire amplifier is embedded in a global feedback loop, the error signal at the input will tend to restore the output, but the recovery will be limited by the settling time of the amplifier. As a result, an amplifier of this type may have outstanding low frequency power supply rejection, but the negative

supply rejection is fundamentally limited at high frequencies, approaching zero at frequencies above the closed loop bandwidth.

Due to parasitics in the amplifier, the power supply rejection of the positive supply also deteriorates with frequency, but this is less severe than what occurs with the negative supply. This causes an asymmetrical pulse response. Typically, a positive-going pulse edge will have a response determined mainly by the amplifier whereas a negative-going pulse edge will have a response due to both the amplifier and the power supply. To solve this problem, both bypassing and decoupling can be used. With an op amp, it is better to use small resistors (10-50  $\Omega$ ) rather than inductors as decoupling elements to avoid resonances. The good low frequency power supply rejection will take care of the low frequency voltage drops due to the resistor. This, of course, assumes that the application can tolerate the reduced range of compliance.

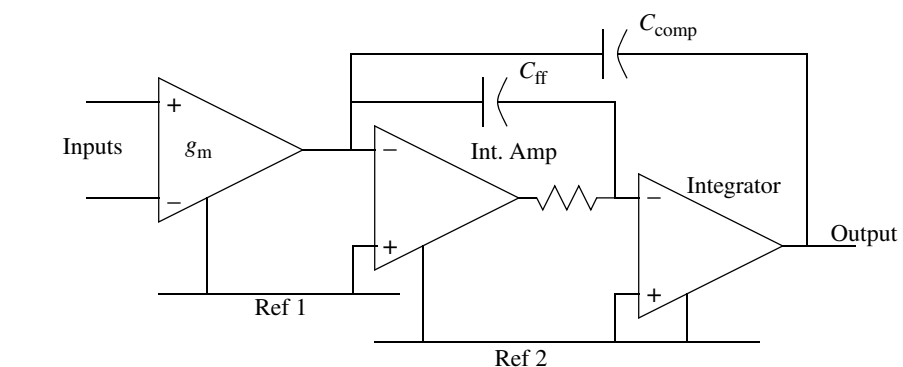
In Figure 11, a secondary feedback loop exists that is not widely recognized in which signal is fed back from the collector of the output PNP transistor through the negative supply rail and into the non-inverting input of the integrator. The dynamics of this path are dependent on both the load and the negative supply impedance. When the supply looks inductive, it tends to destabilize the amplifier. A capacitive load will aggravate the situation. Bypassing the negative supply will help alleviate this problem. Note that neither a high speed op amp nor fast signals are required for this problem to appear.

It is not uncommon for the integrator input to be referred to the positive supply instead of the negative supply (LM308). In this case, concern for the supplies should be reversed.

## 9 Feed Forward

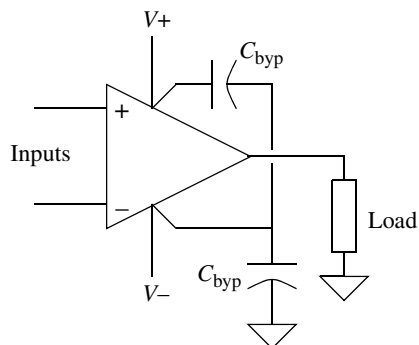
Many high speed op amps use a technique called feed forward to achieve their bandwidth. In a feed forward op amp, the slow PNP level shift stage is bypassed with a capacitor to provide an alternate high speed path. A block diagram of a feed forward amplifier is shown in Figure 12. Notice that the intermediate amp (level shifter) and the integrator are referred to different nodes. For example, the LM318 and OP05 have the intermediate amp referred to the positive supply while the integrator is referred to the negative supply.

FIGURE 12 A feed forward amplifier.



This means that any signal appearing between the two supplies is effectively inserted in the integrator loop. This problem can usually be minimized by tying the two supplies together with a bypass capacitor, as in Figure 13.

FIGURE 13 Bypassing a feed forward amplifier.



## 10 Conclusion

Clean supplies are essential for low noise, stable, and clean designs and they are not difficult to achieve. A little effort taken during circuit board layout can save a lot of time and minimize the possibility of your supplies ringing like the “Avon Lady”.

### 10.1 If You Have Questions

If you have questions about what you have just read, feel free to post them on the *Forum* section of *The Designer's Guide Community* website. Do so by going to [www.designers-guide.org/Forum](http://www.designers-guide.org/Forum).

## Acknowledgements

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