Final Project
Introduction of Integrated Circuit Design
(January 2023)

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***Abstract* – In this report, we'll explain our design of ROM(Read-Only Memory) macro, which include ROM array, 7-to-128 decoder, D-flip flop(DFF), Multiplexer(MUX), sense amplifier(SA) and timing control logic.**

Index Terms – Read only memory (ROM), D-flip flop (DFF), Decoder, Multiplexer (MUX), Sense Amplifier (SA).

I. INTRODUCTION

A 128 x 16 bits ROM array macro is consisted of 128 word lines(WLs) and 16 bit lines(BLs), and the input is the address of memory cell(A<9:0>), the outputs are the stored values of memory cells(DOUT<1:0>).

At first, DFFs will stored the value of inputs(A<9:0>). After the clock rise, word line is chosen by A<9:3>, which is implemented by 7-to-128 x-decoder. Bit lines is chosen by A<2:0>, which is implemented by 3-to-8 y-decoder and MUXs. The difference of chosen BLs signal and Vref will be amplified by SAs, and output will be latched by two D-latches connected with outputs of SAs. Meanwhile, all of the timing control signal are produced by timing control logic.

II. CIRCUIT STRUCTURE

A. D Flip-Flops(DFFs)

We use 10 DFFs to store the input values, 7 DFFs is for the word lines x-decoder, and the other 3 is for bit lines y-decoder. While the clock rise, DFFs will read in the input value, and then hold it until the next clock rising edge.

Here we add 7 AND gates at the word line output stage, the inputs of AND gate is Q (value stored in DFF) and WL_EN1. WL_EN1 is a control signal to prevent Q from transporting while CLK = 0, and it is generated by timing control logic. The output of AND gates will serve as input (IN and INB) for 7-to-128 decoder.

B. x-Decoder (7-to-128 decoder)

X-decoder help us choose the WL we want to read. It receives the input signals from DFF and AND gates, which is A<3:9> and AB<3:9>. Depends on the input, it'll generate 128 rows of outputs (WL<0:127>), and only one output will be 1, the others are 0, these outputs will be sent into ROM array.

To be noticed, When the x-decoder is in standby mode (WL_EN1 = 0), the input of x-decoder is 0000000. As the result, WL<0> will be 1, which will discharge the BLs. So we add an AND gate between decoder and ROM array, its inputs is PRE_B (a control signal generated by timing control) and WL<0>, when PRE_B = 0, the input of the first row of ROM array will also be 0. In this way, we can make sure the BLs won't be discharge by first row when we are charging BLs.

C. y-decoder and 8-to-1MUXs

y-decoder is a 3-to-8 decoder, it receives the input signals from DFF, which is A<0:2> and AB<0:2>. It performs similar functionality as x-decoder, and will send the outputs (Y-sel<0:7>) to 8-to-1 MUXs.

8-to-1 MUXs is shared by 8 bit lines, so with 16 bit lines in total, we'll have 2 8-to-1 MUXs, generate 2 output (DL<0:1>) respectively.

8-to-1 MUXs is constructed by 8 transmission gates, their inputs is 8 BLs form ROM array, all the outputs is connected. Control signal Y_sel is received by gates, when Y_sel = 1, the transmission gate will open and the voltage of chosen BL will flow in. Among 8 BLs, only one will be chosen.

D. Sense Amplifiers and D-Latches

Sense amplifier receive the input signal form MUXs (DL<0:1>), and compare it with reference voltage. If the BL voltage is at least one input offset voltage lower than Vref, SA will amplify the difference and output 0 or 1 rail-to-rail signal.

There is a problem that if we connect output of SA directly to DOUT<0:1>, the DOUT signal cannot sustain until the next clock edge. It's because our SAEN control signal is a delay of clock signal, while SAEN = 0, the output of SA will be pre-charge to VDD, causing DOUT return to 1 during clk = 0 period, then we cannot measure the access time of reading 1.

In order to solve this problem, we connect two clocked D-latch to the output of SA, whose control signal is SAEN. When SAEN = 1, the output of SA can transport to DOUT, but when SAEN = 0, D-latch will hold the original DOUT, so that DOUT won't be affected by the pre-charge period of SA.

E. Timing control

Timing control logic generates all of the control signal we need in the macro, including CLKB, WL_EN1, PRE_B, and SAEN.

WL_EN1 is used to make sure all of the inputs of x-decoder is 0 when WL_EN1 = 0. PRE_B is an initialization signal for BLs, it is sent to 16 pre-charge PMOS, which is connect to 16 BLs. When PRE_B = 0, the conducting path from VDD to BLs is open, all of the bit lines are pre-charge to VDD, so that in the read period afterward, the bit lines can be discharge. These three control signal is important, because we need to make sure the initial state of WLs and BLs are correct, such that the reading process can be properly implemented.

SAEN is a signal controlling the sensing period of SA. And it's also a main factor for reading correctness. If the SAEN rise too early, the voltage of BL may not be low enough, which will cause the false output result.

All of the timing control signals mentioned above are delays of clock signal. This is implemented by delay chain, which is constructed by even stages of inverter.

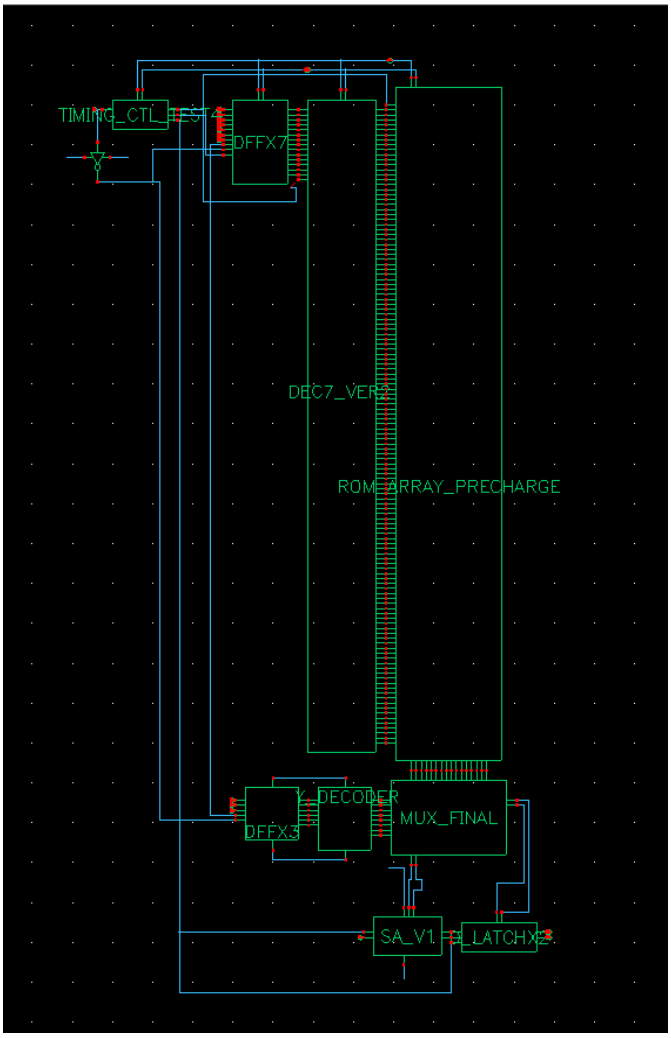

Fig. 1 Schematic of 128 x 16 ROM macro.

III. PRE-SIMULATION RESULT

We construct the whole ROM array macro circuit by composer and run the simulation of each small block first. After we make sure all of the instance work correctly, we connect it together and run the simulation of whole macro.

In order to achieve the best access time. we spend most of the time to test timing control logic. Also, we change the structure of timing control significantly after we run the post-sim, so the delay of pre-sim is actually much larger than the original one. Pre-simulation result is shown as below.

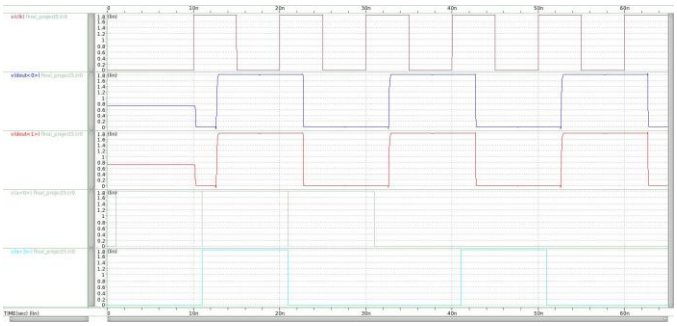

Fig. 2 Waveform of TT 25 corner in pre-sim.

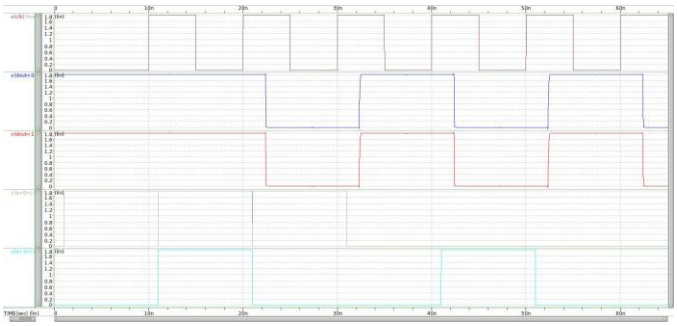

Fig. 3 Waveform of FF 25 corner in pre-sim.

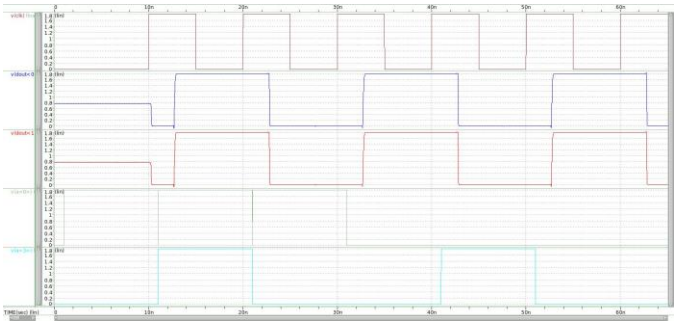

Fig. 4 Waveform of FS 25 corner in pre-sim.

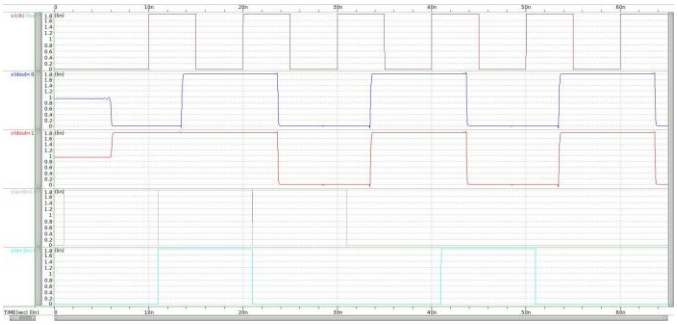

Fig. 5 Waveform of SF 25 corner in pre-sim.

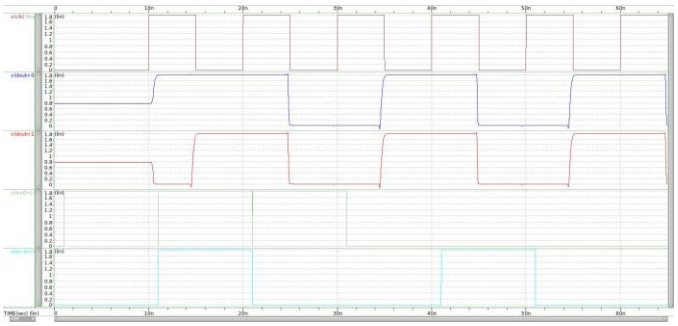

Fig. 6 Waveform of SS 25 corner in pre-sim.

TABLE I
PRE-SIMULATION RESULT

Corner	Access Time (ns)	Avg. Power (uW)
TT 25	2.7175	473.4753
FF 25	2.3775	498.4758
FS 25	2.7650	478.0446
SF 25	3.6075	506.6594
SS 25	4.7475	502.5042

IV. POST-SIMULATION RESULT

After we finish the layout, we pass DRC check and LVS check. Then we extract the PEX model, which conclude the parasitic R + C + CC effect.

We find out that our output delay is too large. The reason is that SAEN rise too early such that the voltage of BL hasn't drop to the enough input offset level. To solve this problem, we try to add more delay chain and change the sizing of SA. Finally, we successfully create a version of circuit that can meet the spec. But the trade-off is long access time compare with the original version. The post-simulation result is shown as below.

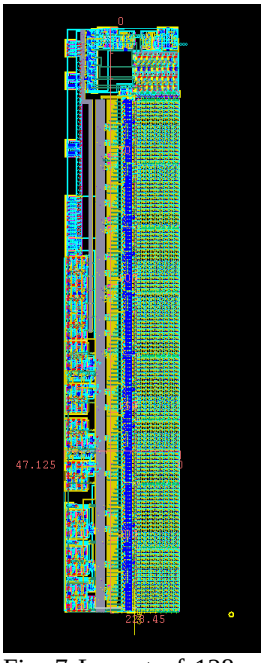

Fig. 7 Layout of 128 x 16 ROM macro. Area = 47.125um x 228.45um = 10765.7062um^2.

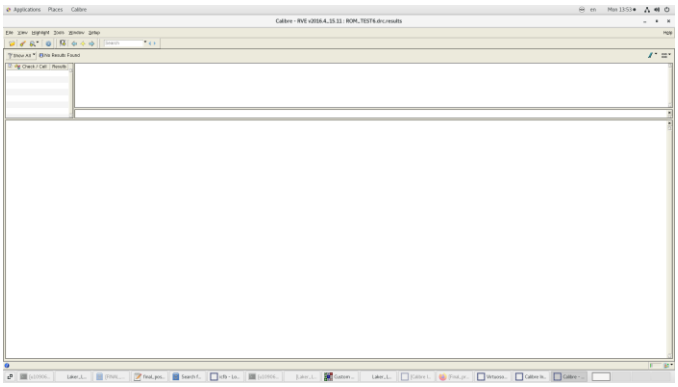

Fig. 8 DRC check result.

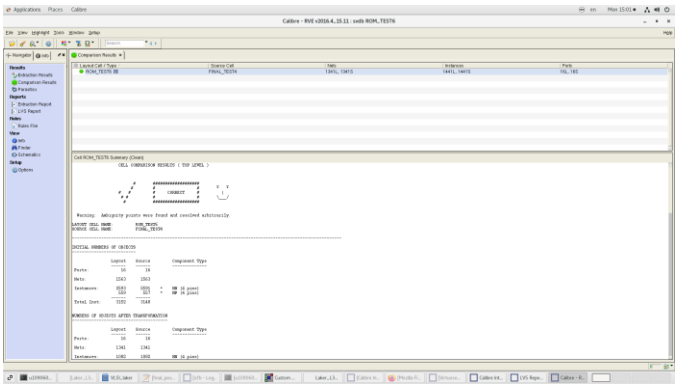

Fig. 9 LVS check result.

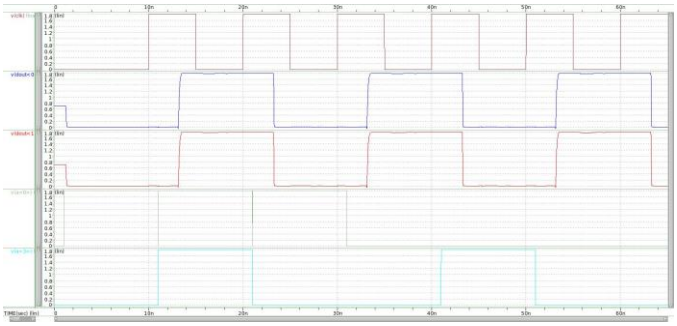

Fig. 10 Waveform of TT 25 corner in post-sim.

TABLE II
POST-SIMULATION RESULT

Corner	Access Time (ns)	Avg. Power (uW)
TT 25	3.2525	807.5757

FoM = (access time^2) x (power) x (area)
= (3.2525^2) x (807.5757) x (10765.7062)
= 91973005.07 ns^2 · uW · um^2

V. CONCLUSION

Form the final project, we have learned the ability to complete the work step by step. And realized that it's really important to sketch the plan before starting. This project also give as more insight into the working scheme of ROM macro and the importance of post-simulation result.

[1] Pre-simulation .sp file: final_postv3.sp
[2] Post-simulation .sp file: final_project5.sp
[3] .spi file (without PEX extraction): FINAL_TEST4.spi
[4] .spi file (with PEX extraction): ROM_TEST6.pex.spi, ROM_TEST6.pex.spi.pex, ROM_TEST6.pex.spi.ROM_TEST6.pxi
[5] Layout file: ROM_TEST6.gds