Uppsala University

Bachelor's Thesis

Static Multi-Versioning for Efficient Prefetching

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Abstract

Faculty for Science and Technology
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Bachelor of Computer Science

Static Multi-Versioning for Efficient Prefetching

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The Thesis Abstract is written here (and usually kept to just this page). The page is kept centered vertically so can expand into the blank space above the title too...

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Abbreviations

CFG Control Flow Graph

DAE Decoupled Access-Execute

Physical Constants

Speed of Light $c = 2.997\ 924\ 58 \times 10^8\ \mathrm{ms}^{-\mathrm{S}}$ (exact)

Symbols

a	distance	m
P	power	W (Js^{-1})
ω	angular frequency	rads^{-1}

Chapter 1

Introduction

General introduction...

1.1 Background

- Decreased power consumption through DVFS
  - Power equation
  - Breakdown of Dennard scaling
- Decoupled access/execute
  - Finding tasks suitable for optimisation
  - Breaking them down in small enough chunks
  - Creating the access version

1.2 Approach

- Multiple access versions
  The idea is to generate more than one access version. These are to be generated from different rule sets. The generated access versions are evaluated in a runtime system in order to determine which version that produces the best results for a specific task. That version is selected to be used for that task while others may use different access versions if they prove to be better.

Chapter 2

Related Work

- Fix the code [1]
- Towards More Efficient Execution [2]
- Polyhedral model and affine code
  (Not strictly required for this thesis.)

Chapter 3

Methodology

A few introductory words...

3.1 Access phase generation

When generating the access phase there are three goals to keep in mind: inserting prefetches at suitable locations; preserving the Control Flow Graph (CFG), including all instructions it depends on; and removing all side effects. The task to be converted into Decoupled Access-Execute (DAE) is first copied to create separate access and execute phases that can be run sequentially. Once this has been done the instructions that are required to be in the access phase are identified and prefetches are inserted. Other instructions are removed.

3.1.1 Control Flow Graph skeleton

To find out which instructions that must be kept in order to leave the CFG in a working state following steps are taken in order to create the set K of instructions to be kept:

Algorithm 3.1. Finding instructions forming the CFG skeleton.

1. Find all instructions that directly defines the CFG, i.e. branch instructions, and add them to K.
2. Pick an instructions I from K and find all instructions that produces a value that I instructions requires in order to execute.

3. If I is a load instruction, find all store instructions that could be causing the value to that I later reads and add them to K. (See below, in Algorithm 3.2, for details on how to find these stores.)

4. Repeat steps 2 and 3 until no choice of I will cause further instructions to be added to K.

When searching for stores causing the value of a load the reversed Control Flow Graph is used in order to easily find predecessors of basic blocks. Starting with the load instruction I in focus, which uses the address A, the following algorithm is used to produce the set S of potential sources:

Algorithm 3.2. Finding potential sources for a load instruction I.

1. If I has already been visited, stop.

2. If I is a store instruction with address B, perform following:

   (a) If A and B alias with some certainty, add I to S.

   (b) If A and B alias without doubt, stop.

3. If I is the first instruction in its basic block, apply this algorithm to each predecessor basic block starting with their last instruction as I. Once the algorithm has stopped for each of the predecessors, stop also this instance. (Observe that all instances share the set S and the list of visited instructions.)

4. Let the instruction that occurs immediately before I be denoted I instead and start over from step 1.

Observe that steps 2a and 2b require an alias analysis (not described here) to be performed. The wording "alias with some certainty" describes a minimum which can mean anything from "cannot be proven not to alias" to "alias without doubt". Depending on the strictness of the interpretation different results may follow.

At this point all instruction that must be kept are known. If any of these instructions may cause side effects on data used outside of the access phase the task must be disqualified from DAE in order not to affect the results of the program in any way. Disqualification will occur when any function calls or stores touching memory not guaranteed to be local are part of K.

3.1.2 Prefetches

The purpose of the prefetches, and the access phase in general, is to bring data into the cache to be ready for use once the execute phase takes over. As the phases do not share local data it is only useful to prefetch global variables. Furthermore, if a load is present in the access phase (because it is required to compute a control flow decision or the address of a prefetch) it is not prefetched to avoid the overhead of accessing the same data twice, once with the prefetch and once with the load.

When a prefetch is inserted it is also necessary to make sure that all instructions required to compute the address A in question is present in the access version. To find the set D of such dependency instructions following algorithm is used:

Algorithm 3.3. Finding dependencies of an address A.

1. If A is produced by an instruction, add it to D, otherwise stop.
2. Follow steps 2-4 from Algorithm 3.1 using D in place of K.

Upon inserting a prefetch, itself and the content of D should be added to K.

As with the CFG skeleton it is possible to run into situations where computing the address for a prefetch require modification to externally visible memory. If this is the case the prefetch, and D, are not added to K in order to keep the correctness of the program.

When a prefetch instruction is inserted is should not be added at the location of the load it replaces but rather as soon as the pointer address is available. This is in order to enable more aggressive dead code elimination.

3.2 Multiversioning

When applying multiversioning more than one version of the access phase are created. In each access version the instructions making up the CFG skeleton are identified as described in Section 3.1.1. The difference between the versions is the policy used when selecting which loads that are going to be prefetched.

The rules used in this paper, to decide if a prefetch is inserted in the access version, are based upon the number of indirections required to calculate the address of where to prefetch from. A threshold is set for each of the access versions. If the number of indirections required for a prefetch exceed the threshold (or otherwise violates the rules

mentioned in Section 3.1.2) the prefetch is not allowed to be in that particular access version.

3.2.1 Indirection measure

Indirections are a measure of how many intermediate loads that are required to compute an address. There are several conceivable ways to define the level of indirection for a load or prefetch. Different variant may use different rules to define what intermediate loads that are counted toward the indirection measure, in what way they are counted, and whether or not indirection counts are independent between different loads and prefetches.

The definition of the indirection measure used here follows following algorithm to find the number of indirections required to compute an arbitrary address A (used by a load or prefetch):

Algorithm 3.4. Finding the number of indirections for an address A.

1. Find the set D of dependencies for A using Algorithm 3.3.
2. Count all load instructions present in D. The result of the count is the level of indirections.

With this approach to measure the indirection level both situations when an address has to be loaded and when data, such as an index, is required from memory are covered. (Pointer dereferences and array accesses in C illustrates these circumstances). Another consequence of counting all loads among the dependency instructions of an address without discrimination is that every level of indirection does not have to be represented among the dependencies.

Figure 3.1 illustrates an example where the origin load depends on six other loads. There are however no intermediate load with exactly three or four indirections as some loads depends on more than one other load. This phenomenon may lead to situations where an access version with a threshold of four indirections may be exactly the same as the one with a threshold of three (and two in this particular example) while the version with a maximum of five indirections is different.

3.3 Evaluation

This section could possibly be moved to the experiments chapter.

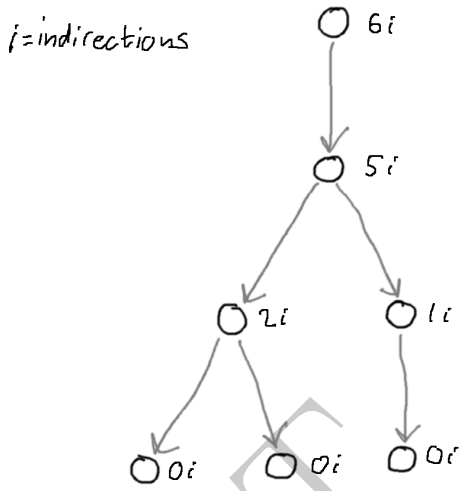

FIGURE 3.1: Tree of indirections illustrating that not all indirection levels have to be present. (A crude placeholder.)

- Running
  - Each access version independently
  - Four instances on four individual cores
  - Once on low and once on high frequency
- Measurement
  - Energy estimation

TODO:

- Evaluation model
  - Power model
  - Measurement method
- Environment setup
  - LLVM 3.4
  - SPEC CPU2006

Chapter 4

Experiments

... or Evaluation

Chapter 5

Conclusion

Appendix A

Appendix Title Here

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Bibliography

[1] A. Jimborean, K. Koukos, V. Spiliopoulos, D. Black-Schaffer, and S. Kaxiras. Fix the code. don't tweak the hardware: A new compiler approach to voltage-frequency scaling. In *GCO'14*, February 2014.

[2] K. Koukos, D. Black-Schaffer, V. Spiliopoulos, and S. Kaxiras. Towards more efficient execution: A decoupled access-execute approach. In *ICS'13*, June 2013.