

# Investigate and Reduce Capacitive Couplings in a Flyback Adapter with a DC-Bus Filter to Reduce EMI

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**Abstract**— In consumer electronics, high power density power adapters are designed to minimize the adapter size. As a result, the components are getting very close and the near field coupling issue tends to be severe. This compromises the performance of EMI filters, especially at high frequencies. This paper investigates near field capacitive couplings and the reduction techniques in a high power-density power adapter with a DC-bus filter. The parasitic capacitive coupling theory is developed and parasitic coupling capacitances are experimentally extracted. The CM noise model with parasitic capacitive couplings is developed and the techniques to reduce the CM noise due to parasitic capacitive couplings are explored. Simulation and experiments were conducted to verify the analysis and the proposed techniques.

**Index Terms**—active clamp Flyback converter, capacitive coupling, DC-bus filter, shielding, parasitic capacitance cancellation.

## I. INTRODUCTION

Increasing the switching frequency of power converters helps to increase their power density. However, high switching frequency can cause severe HF electromagnetic interference (EMI) noise. Therefore, EMI filters with good high frequency (HF) performance are desired in high power-density power converter design.

Near field coupling has been identified as a significant factor that limits the HF performance of EMI filters [1]. In consumer electronics, the components in a high power-density AC/DC power adapters are very close to each other, so the near field coupling could be significant. Moreover, in order to improve power efficiency, in some designs, the EMI filter is located on DC bus [8] instead of on AC line. It will be discussed in this paper later that DC-bus filters tend to have capacitive coupling issues.

Conventionally, there're two different near field couplings: inductive coupling and capacitive coupling. Many literatures focus on the analysis and reduction of inductive couplings [1-4, 21-29] including those between two equivalent series inductances (ESL) of a pair of capacitors [1][2], between a filter inductor and a capacitor's ESL [1][3], between a capacitor's ESL and its adjacent PCB trace loop [1][29] and between two PCB trace loops [1][4]. For EMI filters with multiple components, the couplings could be complicated. In [1][2][23][25][27], the inductive couplings in a CLC  $\pi$ -filter are identified and reduced. In [21][26][28], the couplings in an LCL

T-filter are analyzed. For more complicated filter structures, 3D finite element analysis (FEA) can help to extract the parasitic coupling parameters in an EMI filter [22][23][26].

On the other hand, not many literatures address the capacitive coupling. In [5], the capacitive coupling between the metal foils of two bulk capacitors is identified. However, the techniques to extract and reduce the parasitic capacitance were not further investigated. In [6][21][28][30], the capacitive couplings due to the PCB traces across an LCL T-filter are explored. In order to mitigate the couplings, PCB slits and shielding are applied to reduce and bypass the noise current [6][21][31][33]. The technique was verified within a filter, but the performance when used in a converter was not presented.

In [7], the capacitive coupling between the PCB traces across an inductor is investigated by the same authors of this paper. By improving the PCB layout or applying the parasitic capacitance cancellation technique, the capacitive coupling can be greatly reduced. The techniques are going to be further explored and improved in this paper. Also, in existing literatures, the investigation focuses on the capacitive coupling among components carrying low noise voltages. In this paper, it is found that the capacitive coupling between the conductors or components with high pulsating voltages and sensitive nodes could be more important.

The paper is organized as follows. In section II, the CM noise models of an active-clamp Flyback adapter with an AC-line or a DC-bus EMI filter are developed and compared without any capacitive couplings included. The CM noise of the converter with an AC-line or a DC-bus EMI filter is also measured and compared. In section III, the capacitive couplings are identified and the coupling mechanism is studied. The parasitic coupling parameters are also extracted for the development of CM noise model. In section IV, different capacitive coupling reduction techniques, such as parasitic capacitance cancellation and shielding techniques, are investigated to reduce the CM EMI due to capacitive couplings. Simulation and experiments were conducted to verify the proposed techniques.

## II. CM NOISE MODELS OF AN ACTIVE CLAMP FLYBACK ADAPTER WITH AN AC-LINE OR DC-BUS FILTER

### A. Active Clamp Flyback Adapters with an AC-line or DC-bus Filter

Fig. 1 shows an active clamp Flyback adapter with a conventional AC-line EMI filter line impedance stabilization networks (LISNs). The low line and high line input voltages are 120V/60Hz AC and 240V/50Hz AC, respectively. The output voltage is 20V DC, and the output power is 65W. The converter

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has a switching frequency of 150kHz.  $S_2$  and  $C_{Cl}$  are active clamp components used to improve converter's power efficiency. A CM inductor  $L_{CM}$  (700 $\mu$ H) with two fully coupled windings is placed at the AC input and a Y-capacitor  $C_Y$  (470pF) is placed across the primary ground (PGND) and secondary ground (SGND) to reduce CM EMI noise. An LC filter, which is composed of a DM inductor  $L_{DM}$  (300 $\mu$ H) and an X-capacitor  $C_X$  (0.47 $\mu$ F) on AC line, reduces the differential mode (DM) EMI noise. The SGND of the adapter is floating.  $C_{SG}$  represents the parasitic capacitance between SGND and the earth ground.  $C_{SG}$  is measured as around 10pF.

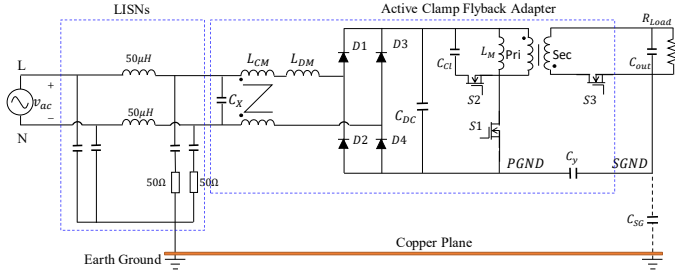


Fig. 1. An AC/DC active clamp Flyback adapter with an AC-line filter.

Because the diode bridge turns on/off at 50/60Hz, the AC input current of the adapter has large line-frequency current ripples, which result in a large RMS and peak current. Therefore, the winding power loss of the CM and DM inductors could be significant. Furthermore, the X-capacitor  $C_X$  needs to meet the AC-line safety requirement EN60950. Therefore, a film capacitor should be used. The film capacitor has large size due to its low permittivity. In order to improve the power efficiency and power density of the adapter, a DC-bus filter [8] can be applied in Fig. 2. In Fig. 2, the EMI filter is moved from AC line to DC bus. Since the AC-line current ripple due to the diode bridge is mostly filtered out by the bulk electrolytic capacitor  $C_{DC}$  (82 $\mu$ F), the current flowing through the inductors  $L_{CM}$  and  $L_{DM}$  is almost a constant DC current. Since the peak current in a DC-bus inductor is greatly reduced, the DM inductor is to be saturated at a higher current than an AC-line inductor. Therefore, a smaller magnetic core can be used for  $L_{DM}$ . Also, the RMS current in a DC-bus inductor is smaller than that in an AC-line inductor, so the winding power loss in a DC-bus inductor is smaller than that of an AC-line inductor. Moreover, ceramic capacitors can be used as the DM capacitance  $C_{DM}$  (0.47 $\mu$ F) without the limitation of the same safety standard as required for AC-line filters. Due to its high permittivity, the size of ceramic capacitors on DC bus is much smaller than that of film capacitors on AC line even the capacitance derating due to DC-bus voltage bias is considered.

In order to show the advantages of the DC-bus filter, the size and power loss of the inductors and capacitors in an AC-line filter are compared with those in a DC-bus filter for a 65W Flyback adapter in TABLE I. In TABLE I, by employing a DC-bus filter, the EMI filter size reduces by 84% and the power loss reduces by 775mW, which indicates the adapter has more than 1% efficiency improvement. The DC-bus filter is therefore preferred for many high power-density designs.

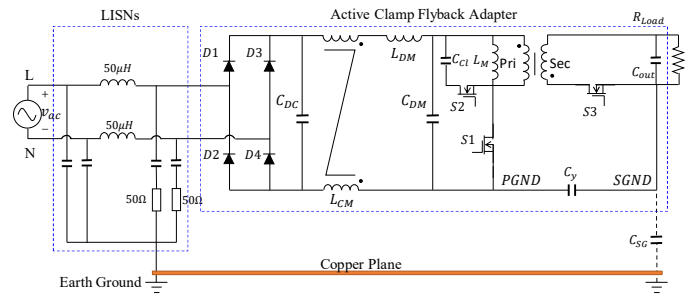


Fig. 2. An AC/DC active clamp Flyback adapter with a DC-bus filter.

TABLE I. COMPARISON OF THE SIZE AND POWER LOSS OF AN AC-LINE FILTER AND A DC-BUS FILTER IN A 65W FLYBACK ADAPTER

EMI Filter Components		Characteristics of Filter Components		
		Value	Size (mm <sup>3</sup> )	Loss <sup>a</sup> (mW)
AC Line	Ferrite Toroid Core: $L_{CM}$	$L=700\mu$ H DCR=203m $\Omega$	120	292
	High Flux Core: $L_{DM}$	$L=300\mu$ H DCR=383m $\Omega$	1370	552
	Safety Film Capacitor: $C_X$	$C=0.47\mu$ F ESR=20m $\Omega$	2900	<1
	Total		4390	844
DC Bus	Ferrite Toroid Core: $L_{CM}$	$L=700\mu$ H DCR=203m $\Omega$	120	32.5
	High Flux Core: $L_{DM}$	$L=300\mu$ H DCR=160m $\Omega$	435	25.6
	Ceramic Capacitor: $C_{DM}$	$C=0.47\mu$ F*2 <sup>b</sup> ESR=20m $\Omega$ /2	71.3*2	10.3
	Total		698	68.4

a. The power loss is calculated when the input voltage is 120V AC and the output is 65W (full load).

b. When using a ceramic capacitor with DC bus bias voltage, a 50% capacitance derating is needed based on the guideline on the datasheet. So, in actual design, two parallel 0.47 $\mu$ F capacitors are used.

### B. CM Noise Model for Active Clamp Flyback Adapters

For CM noise analysis in conducted EMI frequency range from 150kHz to 30MHz, the impedances of the line and neutral of the AC power line between the diode-bridge and LISNs can be ignored. It is assumed that the CM impedance of LISNs is approximately 25 $\Omega$  [9] within the conducted EMI range. The CM inductance of the coupled CM inductor  $L_{CM}$  is equal to the single winding's inductance  $L_{CM}$ . The impedance of the diode-bridge can be ignored [11] even when it is off for CM EMI analysis because its 50pF junction capacitance is much larger than  $C_{SG}$ . The equivalent series resistance (ESR) and the equivalent series inductance (ESL) of the bulk capacitor  $C_{DC}$  is 0.8 $\Omega$  and 20nH, respectively. Because of this, the impedance of  $C_{DC}$  is below 5 $\Omega$  in the conducted EMI range, which is much smaller than the impedance of  $L_{CM}$  or  $C_{SG}$ , so  $C_{DC}$  can be considered as short circuit for EMI analysis. Similarly,  $C_X$  (ESR=20m $\Omega$ , ESL=2.5nH) in Fig. 1,  $C_{DM}$  (For a single 0.47 $\mu$ F ceramic capacitor, ESR=20m $\Omega$ , ESL=1.5nH) in Fig. 2, and the output capacitor  $C_{out}$  (ESR=8m $\Omega$ , ESL=5nH) can also be considered as short circuit for EMI analysis [9].

In Figs. 1 and 2, based on substitution theory, S1 can be replaced with a voltage source  $V_{S1}$  which has the same voltage waveform as the MOSFET drain to source voltage; S2 and S3 can be replaced with current sources  $I_{S2}$  and  $I_{S3}$  which have the

exact same current waveforms as the MOSFET currents [13]. Another important component in CM noise analysis is the transformer which is a 4-port component. Thanks to the research in [12], the transformer's interwinding parasitic capacitance can be represented with a two-capacitor model for CM noise analysis. The impedance of  $L_{DM}$  can be ignored in CM noise analysis because of the full coupling between  $L_{CM}$ 's two windings. Based on the analysis above, the circuit in Figs. 1 and 2 can be represented with the model shown in Fig. 3(a).

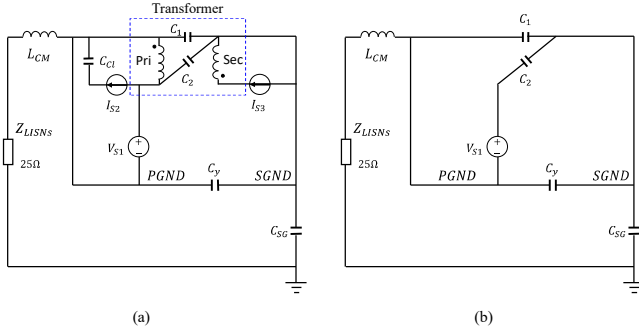


Fig. 3. (a) CM noise model with substitution theory applied, (b) CM noise model with superposition theory applied.

Superposition theory can be applied to simplify the model in Fig. 3 (a). Based on superposition theory, the effect of a voltage/current source on CM EMI can be analyzed by shorting other voltage sources and disconnecting other current sources. Based on this, it was found that, only the noise generated by  $V_{S1}$  flows through LISNs [10]. As a result,  $I_{S2}$  and  $I_{S3}$  can be removed from the model. Furthermore, both transformer windings are in parallel with the voltage source  $V_{S1}$  thus they can be removed as shown in Fig. 3(b). Based on the transformer capacitance extraction technique introduced in [12],  $C_1$  and  $C_2$  are extracted as 107pF and -2.1pF. It should be noted that  $C_2$  is an equivalent capacitance in the transformer model and its value can be either positive or negative [10][12]. The transformer has been optimized for CM noise reduction based on the transformer design technique in [10], so  $C_2$  is small.

Based on Thevenin equivalence, the circuit between PGND and SGND can be modeled with an equivalent capacitance  $C_{Eq}$  and an equivalent voltage source  $V_{Eq}$  in (1) and (2). The final model is shown in Fig. 4.  $V_{CM}$  is the CM voltage drop on LISNs. It should be noted that the CM noise models for the circuits in Fig. 1 and Fig. 2 are identical, which indicates that theoretically, the location of the EMI filter, either on the AC line side or DC bus side, does not change the CM noise model.

$$V_{Eq} = \frac{C_2}{C_1 + C_2 + C_y} V_{S1} \quad (1)$$

$$C_{Eq} = C_1 + C_2 + C_y \quad (2)$$

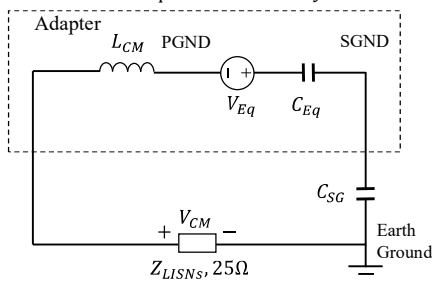


Fig. 4. Final CM noise model of an active clamp Flyback adapter.

### C. CM Noise of a Power Adapters with an AC-line or DC-bus Filter

The CM EMI noise of power adapters with an AC-line or a DC-bus EMI filter was measured in Fig. 5. The input voltage is 240V AC, which represents the worst case for CM EMI noise since the switching voltage  $V_{S1}$  is the highest. In the measurement, all component values in two adapters are identical. The model in Fig. 4 does not include any parasitic couplings. Based on this model, the CM noise should be equal for the two adapters. However, in Fig. 5, the adapter with an AC-line filter meets the conducted EMI standard, whereas the CM noise of the adapter with a DC-bus filter is 15dB higher than the noise with the AC-line filter at high frequencies. It is higher than the EMI standard EN55022. It indicates there are issues which have not been identified and investigated for DC-bus filter implementation.

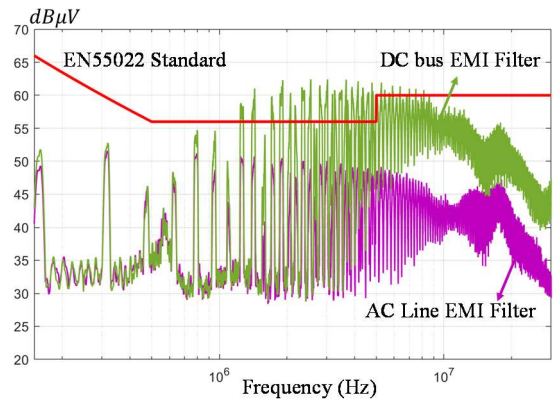


Fig. 5. Measured CM EMI noise of Flyback adapters with an AC-line filter or a DC-bus filter.

## III. IDENTIFICATION AND ANALYSIS OF THE NEAR FIELD CAPACITIVE COUPLINGS

### A. Capacitive Couplings in an Active Clamp Flyback Converter with an AC-line Filter

The undesired capacitive couplings usually happen between conductors with different voltages, especially between the sensitive nodes and noisy nodes. In order to identify the capacitive couplings of the converter in Fig. 1, voltage nodes are identified as shaded areas in Fig. 6 (a). The adapter's physical layout is in Fig. 6 (b). In Fig. 6, node  $N_A$  is between the EMI filter and the LISNs on the AC line. The diode bridge, DM inductor  $L_{DM}$ , bulk electrolytic capacitor  $C_{DC}$  and DC bus PCB traces can be defined as node  $N_C$  for the convenience of noise analysis although the diode may not be always on. As analyzed previously, for CM noise, because of the fully coupled two windings on  $L_{CM}$ ,  $L_{DM}$  almost has no voltage drop, so it is included in  $N_C$ . Node  $N_D$  is the voltage pulsating node. It includes not only the connection between the transformer and the drain of the MOSFET S1 but also the effects of the transformer primary winding as it has gradient and time varying voltages.

In Fig. 6, node  $N_A$  is at the output of the EMI filter, so the noise at  $N_A$  should be very low. Any significant capacitive couplings from the noisy nodes to  $N_A$  may significantly increase the noise at  $N_A$ . Because of this,  $N_A$  is identified as sensitive node. On the other hand, node  $N_D$  is identified as noisy



node. Node  $N_C$  includes PGND, so the capacitive coupling  $C'_{CD}$  from node  $N_D$  to  $N_C$  is equivalently in parallel with MOSFET S1, as a result, it does not contribute to the CM noise on LISNs. On the other hand, the capacitive coupling  $C'_{AC}$  between the node  $N_C$  and  $N_A$  can reduce the performance of the EMI filter, so it is important. Similarly, the capacitive coupling  $C'_{AD}$  between noisy node  $N_D$  and sensitive node  $N_A$  is also important if the coupling effect is significant. The induced current  $i'_{AD}(s)$  due to  $C'_{AD}$  can be approximated as

$$i'_{AD}(s) \approx sC'_{AD}V_{S1}(s) \quad (3)$$

where  $V_{S1}(s)$  is the drain to source voltage of S1 as shown in Fig. 3. A detailed analysis on this approximation will be given in section III D. From (3), the induced current is proportional to  $C'_{AD}$ .

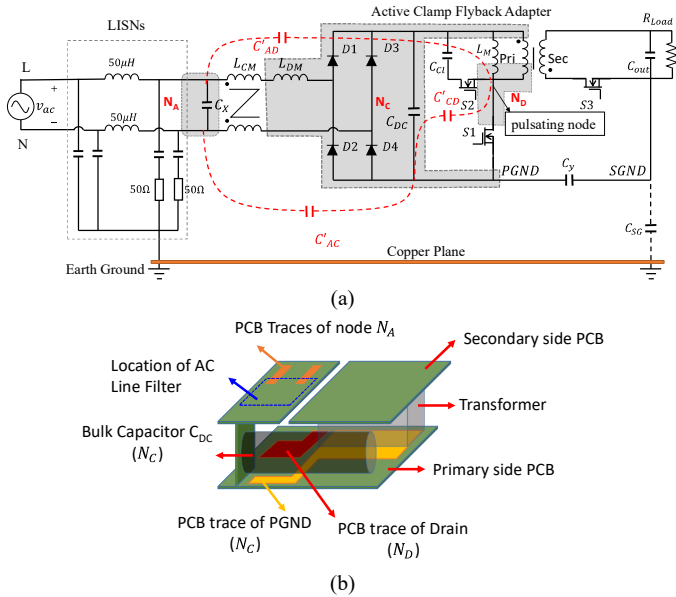


Fig. 6. (a) Voltage nodes and capacitive couplings in an AC/DC active clamp Flyback adapter with an AC-line filter and LISNs, (b) physical layout.

### B. Capacitive Couplings in an Active Clamp Flyback Converter with a DC-bus Filter

For the active clamp Flyback converter with a DC-bus filter in Fig. 2, the voltage nodes are identified in Fig. 7 (a). The adapter's physical layout in Fig. 7 (b) is similar to that in Fig. 6 (b) for AC-line filter case. Node  $N_B$  includes bulk capacitor  $C_{DC}$ , the diode bridge and the PCB traces connected to them. It is the output of the EMI filter, so it is a sensitive node. Node  $N_C$  includes DM capacitor  $C_{DM}$  and  $L_{DM}$  and the PCB traces connected to them. Similar to that in Fig. 6,  $L_{DM}$  is included in node  $N_C$  because it almost has no voltage drop for CM current due to the full coupling between the two windings of  $L_{CM}$ . Node  $N_D$  is a voltage pulsating node same as in Fig. 6.

There are capacitive coupling  $C_{BD}$ ,  $C_{BC}$  and  $C_{CD}$  between any two nodes. Different from the active clamp Flyback converter with an AC-line EMI filter in Fig. 6, bulk electrolytic capacitor  $C_{DC}$  is now in sensitive node. Any capacitive couplings to  $C_{DC}$  could be significant due to its large size.  $C_{BC}$  is the parasitic capacitance between node  $N_B$  and  $N_C$ . The coupling between electrolytic capacitor  $C_{DC}$  and node  $N_C$  may contribute to a big part of  $C_{BC}$  because of the small distance between  $C_{DC}$  and PGND in Fig. 7 (b).  $C_{CD}$  can be ignored as it is in parallel with MOSFET S1.  $C_{BD}$  is the capacitive coupling between the voltage pulsating node  $N_D$  and node  $N_B$ . It could be

significant due to the large size of electrolytic capacitor  $C_{DC}$ . Similar to (3), the induced current  $i_{BD}(s)$  due to  $C_{BD}$  can be derived as

$$i_{BD}(s) \approx sC_{BD}V_{S1}(s) \quad (4)$$

From (4), the induced current is proportional to  $C_{BD}$ .

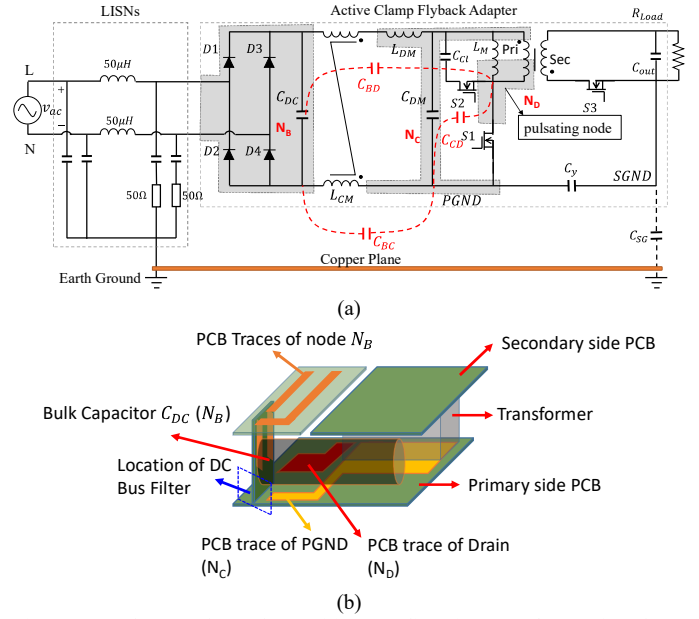


Fig. 7. (a) Voltage nodes and capacitive couplings in an AC/DC active clamp Flyback adapter with a DC-bus filter and LISNs, (b) physical layout.

### C. Measurement and Analysis of the Capacitive Couplings

For the Flyback converter with an AC-line filter in Fig. 6,  $C'_{AC}$ ,  $C'_{AD}$  and  $C'_{CD}$  can be extracted using a vector network analyzer (VNA) in Fig. 8 (a) based on the technique in [17]. In Fig. 8 (a), the two-port S-parameters is measured with  $N_C$  as reference,  $N_A$  and  $N_D$  as two ports. The  $\pi$  capacitance network can be derived from the measured S-parameters and all three capacitances can be extracted. It should be pointed out that, the contribution of the gradient voltage on transformer primary winding to  $C'_{AD}$  has been included in the measurement as the voltage excitation on port 1 is added to the transformer primary winding and this voltage is a gradient voltage on the primary winding.  $C'_{AC}$  is extracted as 1.9pF. Compared with the 1pF equivalent parallel winding capacitance (EPC) and 2.6k $\Omega$  equivalent parallel resistance (EPR) of  $L_{CM}$ ,  $C'_{AC}$  has limited influence to  $L_{CM}$ 's HF performance. Because of the long distance between  $N_A$  and  $N_D$  in Fig. 6 (b), the  $C'_{AD}$  is extracted as only 0.026pF. As the magnitude of  $V_{S1}$  at the fundamental switching frequency is around 300V, based on (3), the induced CM current  $i'_{AD}(s)$  is 7.4 $\mu$ A at fundamental switching frequency. If all of this current flows through LISNs, the voltage drop on 25 $\Omega$  LISNs is 44dB $\mu$ V. It is much smaller than the EMI limit EN55022 (66dB $\mu$ V for Quasi-peak), so its effect can be ignored. As stated previously,  $C_{DC}$  is an electrolytic capacitor which has a big metal shell equivalently connected to its negative terminal for the EMI noise as the capacitance between the metal shell and the negative terminal is measured as 0.8 $\mu$ F. Part of  $C'_{AC}$  and  $C'_{CD}$  is due to  $C_{DC}$ 's metal shell. In the physical layout in Fig. 6 (b), capacitor  $C_{DC}$  is right on the PGND copper plane, so there is a large parasitic capacitance  $C'_{p,dc}$  between the metal shell and the PGND in Fig. 8 (b), but it does not contribute to CM noise.

On the other hand, for the active clamp Flyback converter with a DC-bus filter, with the layout as in Fig. 7 (b), because the parasitic capacitance  $C_{p,dc}$  between  $C_{DC}$  and PGND is significant, it greatly contributes to  $C_{BC}$  as in Fig. 9.  $L_{CM}$ 's performance is thus greatly degraded. Fig. 10 shows the measurement setup for  $C_{BC}$ ,  $C_{BD}$  and  $C_{CD}$ , and the comparison of the measured impedance curves for  $C'_{AC}$ ,  $C_{BC}$  and CM inductor  $L_{CM}$ . In Fig. 10 (a), the two-port S-parameters is measured with  $N_C$  as reference,  $N_B$  and  $N_D$  as two ports. Similar to the case with an AC-line filter, the contribution of the gradient voltage on transformer primary winding to  $C_{BD}$  has been included in the measurement as the voltage excitation on port 1 is added to the transformer primary winding as a gradient voltage. The  $\pi$  capacitance network can be derived from the measured S-parameters and all three capacitances can be extracted. The extracted  $C_{BC}$  is 10.4pF. The noise below 400kHz in Fig. 10 (b) is due to the background noise as the magnitude of signal is too small below 400kHz. In Fig. 10 (b), comparing with 1.9pF  $C'_{AC}$  in AC-line filter case, 10.4pF  $C_{BC}$  can reduce the impedance  $L_{CM}$  above 5MHz.  $C_{p,dc}$  is also extracted as 9pF which contributes to the most of  $C_{BC}$ . When extracting  $C_{p,dc}$ ,  $C_{DC}$  is disconnected from the circuit but keeps at the same position.  $L_{CM}$  and the PCBs at the left side of  $C_{DC}$  are also removed (the top left and the vertical boards in Fig. 7(b)). The distance between  $C_{DC}$  and the PGND is kept unchanged. The capacitance between the negative terminal  $C_{DC}$  and PGND is measured as  $C_{p,dc}$ . It should be noted that the location of  $C_{DM}$  has little influence on  $C_{BC}$  since the size of  $C_{DM}$  is very small. The measured capacitance between  $C_{DM}$  and  $C_{DC}$  when they are adjacent to each other is only 0.3pF, so it can be ignored compared to  $C_{BC}$ .

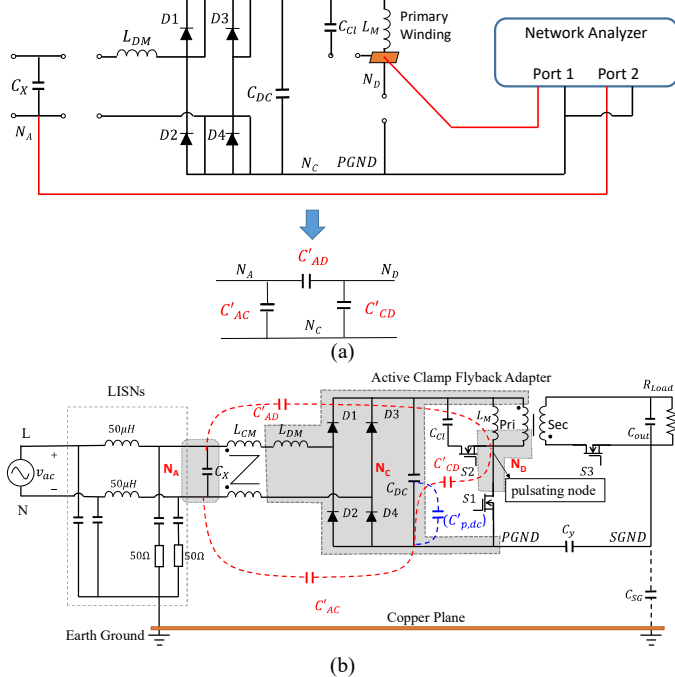


Fig. 8. (a) Measurement setup for  $C'_{AC}$ ,  $C'_{AD}$  and  $C'_{CD}$ , (b) the parasitic capacitance  $C'_{p,dc}$  between the metal shell of the electrolytic capacitor  $C_{DC}$  and PGND does not contribute to CM noise.

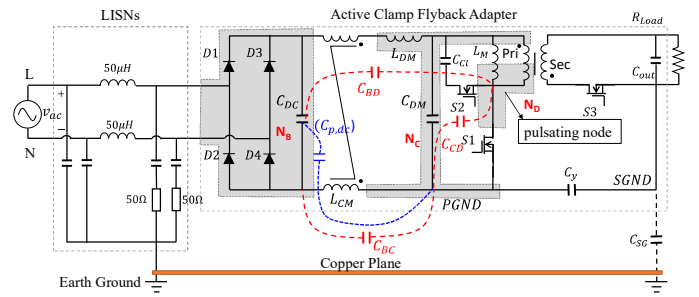


Fig. 9. The parasitic capacitance  $C'_{p,dc}$ , which is part of  $C'_{BC}$ , between the metal shell of the electrolytic capacitor  $C_{DC}$  and PGND degrades  $L_{CM}$ 's performance.

Different from the  $C'_{AD}$  in Fig. 6,  $C_{BD}$  cannot be ignored because it is much larger than  $C'_{AD}$  due to the parasitic capacitance between the big metal shell of  $C_{DC}$  and node  $N_D$ . The extracted  $C_{BD}$  is 0.31pF. Based on (4), the induced CM current  $i_{BD}(s)$  due to  $C_{BD}$  is 88μA at fundamental switching frequency. If all of this current flow through LISNs, its voltage drop on 25Ω LISNs is 66dBμV. It reaches the EMI limit EN55022 (66dBμV for Quasi-peak), so its effect cannot be ignored. This conclusion also holds for high order switching harmonics based on (4).

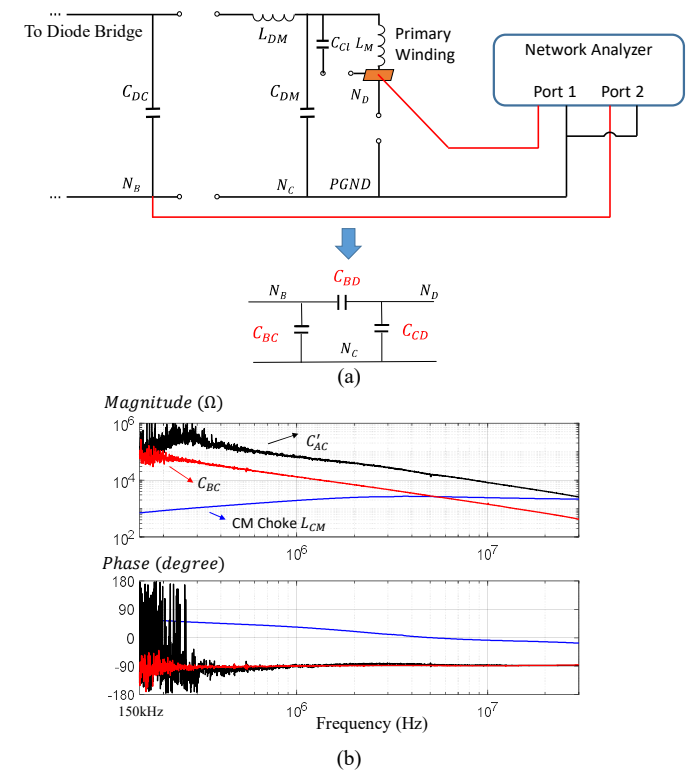


Fig. 10. (a) Measurement setup for  $C'_{BC}$ ,  $C'_{BD}$  and  $C'_{CD}$ , (b) comparison of the measured impedances of the CM inductor  $L_{CM}$ ,  $C'_{AC}$ , and  $C'_{BC}$ .

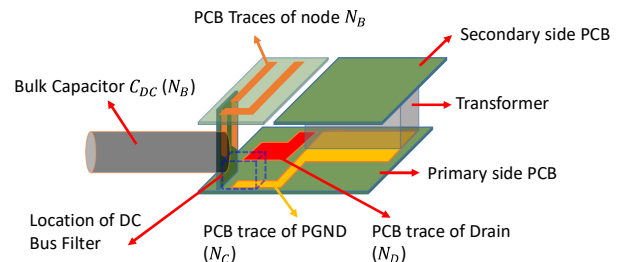


Fig. 11. Place the bulk capacitor away from the primary side PCB.

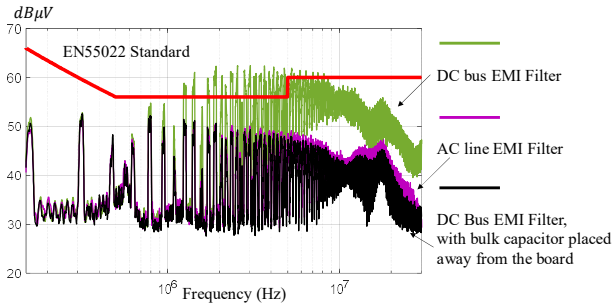


Fig. 12. Comparison of the CM noise of the adapter with the bulk capacitor placed away from the primary side board and the original CM noise.

In order to verify the effects of capacitive couplings due to the large metal shell of  $C_{DC}$  on CM noise, an experiment is conducted in Fig. 11. The bulk capacitor  $C_{DC}$  was moved away from the PGND by mounting it on the outside of the adapter. Based on the measurements,  $C_{BD}$  is greatly reduced from 0.31pF to 0.023pF and  $C_{p,dc}$  is greatly reduced from 9pF to 0.7pF. The CM noise is measured and compared with the original power adapters with an AC-line or DC-bus filter in Fig. 12. In Fig. 12, after the  $C_{DC}$  was moved far away from PGND, the CM noise with a DC-bus filter is reduced to a level almost the same as that with an AC-line filter and it meets the EMI standard. Despite this, it will be shown later that  $C_{BD}$  and  $C_{BC}$  actually play inverse roles on HF CM EMI.

#### D. CM Noise Analysis with Capacitive Couplings

The CM noise model in Fig. 3 (b) for the active clamp Flyback converter with a DC-bus filter can be improved in Fig. 13 with capacitive couplings and  $L_{CM}$ 's EPR and EPC included.

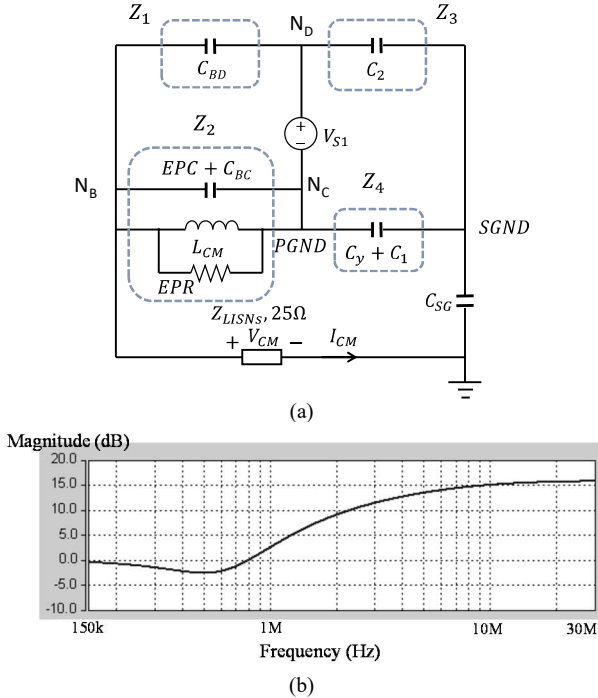


Fig. 13. (a) CM equivalent circuit with a DC-bus filter and capacitive couplings, (b) simulated difference of the voltage transfer gains of the DC-bus and the AC-line filters.

The circuit in Fig. 13 (a) is a Wheatstone bridge with  $V_{S1}$  as the source. The actual CM noise flowing through LISNs is due to the unbalance of the Wheatstone bridge [18]. In the bridge, branch  $Z_1$  is  $C_{BD}=0.31\text{pF}$ . Branch  $Z_2$  includes

$EPC+C_{BC}=11.4\text{pF}$ ,  $L_{CM}=700\mu\text{H}$  and  $EPR=2.6\text{k}\Omega$  in parallel. Branch  $Z_3$  is  $C_2=2.1\text{pF}$ . Branch  $Z_4$  is  $C_y+C_1=470\text{pF}+107\text{pF}$ . Therefore,  $|Z_1|$  and  $|Z_3|$  are much larger than  $|Z_2|$  and  $|Z_4|$  respectively. Based on the theory of Wheatstone bridge with large impedance ratio [20], the CM noise can be greatly reduced even the bridge is unbalanced. The low frequency voltage transfer gain  $\text{Gain}_{LF}$  from  $V_{S1}(s)$  to  $V_{CM}(s)$  can be derived as,

$$\text{Gain}_{LF} = \frac{V_{CM}}{V_{S1}} = \frac{Z_{LISNs} \left( \frac{Z_2}{Z_1 + Z_2} - \frac{Z_4}{Z_3 + Z_4} \right)}{Z_{LISNs} + Z_{CSG} + \frac{Z_1 Z_2}{Z_1 + Z_2} + \frac{Z_3 Z_4}{Z_3 + Z_4}} \approx \frac{Z_{LISNs}}{Z_{CSG}} \left( \frac{Z_2}{Z_1} - \frac{Z_4}{Z_3} \right) \approx -Z_{LISNs} \frac{s C_{SG} C_2}{C_y + C_1} \quad (5)$$

where  $Z_{CSG}$  is the impedance of  $C_{SG}(10\text{pF})$ . It should be noted that since  $Z_{LISNs}$  ( $25\Omega$ ) is much smaller than  $Z_{CSG}$  in the conducted EMI range, when deriving the CM current  $I_{CM}$  flowing through  $Z_{LISNs}$ ,  $Z_{LISNs}$  is ignored. This approximation is also applied in the rest of the paper.

From (5), LF CM noise is mostly determined by  $C_2$  and  $C_{SG}$ . At high frequencies, the impedance of  $EPC+C_{BC}$  is smaller than that of  $L_{CM}$  and  $EPR$  in parallel. As a result, the unbalance and CM noise is determined by all parasitic capacitances in the Wheatstone bridge. The HF voltage transfer gain  $\text{Gain}_{HF}$  can be derived as,

$$\text{Gain}_{HF} = \frac{V_{CM}}{V_{S1}} \approx \frac{Z_{LISNs} \left( \frac{s C_{BD}}{C_{BC} + EPC} - \frac{s C_2}{C_y + C_1} \right)}{\frac{1}{C_{SG}} + \frac{1}{C_{BC} + EPC} + \frac{1}{C_y + C_1}} \approx Z_{LISNs} \frac{s C_{SG} C_{BD}}{C_{BC} + EPC + C_{SG}} \quad (6)$$

In (6), based on the extracted capacitances above, the bridge is unbalanced (numerator is not zero). The approximation in (6) holds because  $C_y$  is much larger than other capacitances. It is shown that for the unbalanced bridge, HF CM noise is proportional to  $C_{BD}$ . On the other hand, increasing  $C_{BC}$  actually helps reduce HF CM EMI. From (6), the HF EMI reduction in Fig. 12 after moving  $C_{DC}$  away from the primary side PCB is therefore due to the fact that the reduction of the numerator due to the reduction of  $C_{BD}$  is much more than the reduction of the denominator due to the reduction of  $C_{BC}$ .

The boundary frequency  $f_B$  between low frequencies and high frequencies mentioned above can be approximately derived based on the analysis of the transfer gain of Fig. 13 (a), as shown in (7).

$$f_B \approx \frac{1}{2\pi \sqrt{L_{CM} \sqrt{(EPC + C_{BC} + C_{SG}) \left[ EPC + C_{BC} - \frac{C_{BD}}{C_2} (C_1 + C_y) \right]}}} \quad (7)$$

In (7),  $f_B$  is calculated as 890kHz. In order to validate the derivation from (5) to (7), a simulation is conducted in Saber. The values of the components in the simulation are the same as the extracted in this section. Fig. 13(b) shows the simulated difference between the transfer gains of the DC-bus filter and the AC-line filter based on Fig. 13 (a). In the simulation, the transfer gain of the AC-line filter was simulated after changing  $C_{BD}$  and  $C_{BC}$  in Fig. 13 (a) to  $C'_{AD}$  and  $C'_{AC}$ . In Fig. 13(b), the gain difference between the two filters matches the difference of the measured noise in Fig. 12, which also validated the model and the analysis. It is shown that the DC-bus filter becomes

worse after  $f_B$  because  $C_{BD}$  begins to play a role in the balance of the bridge. Before  $f_B$ , the CM noise is mainly determined by transformer parasitics.

#### IV. TECHNIQUES TO REDUCE CM EMI DUE TO CAPACITIVE COUPLINGS

##### A. CM Noise Reduction with Single Shielding Technique

For the active clamp Flyback converter with a DC-bus filter, from (6), if  $C_{BD}$  can be eliminated, HF CM noise can be greatly reduced. In order to eliminate  $C_{BD}$ , a copper foil was used in Fig. 14 (a) to shield  $C_{DC}$  from node  $N_D$  and the PGND copper plane on PCB. The copper foil is grounded to PGND, so it is part of node  $N_C$ . The equivalent circuit with the copper foil shielding is shown in Fig. 14(b). In Fig. 14(b), with the copper shielding applied, there is a parasitic capacitance  $C_{SD}$  between node  $N_D$  and the shielding (node  $N_C$ ), and a parasitic capacitance  $C_{BS}$  between  $C_{DC}$  (node  $N_B$ ) and the shielding (node  $N_C$ ).  $C_{BS}$  was measured as 30pF. The  $C_{BD}$  in Fig. 13 is equivalently eliminated in Fig. 14(b).  $C_{SD}$  does not contribute to CM noise as it is in parallel with  $V_{S1}$ .

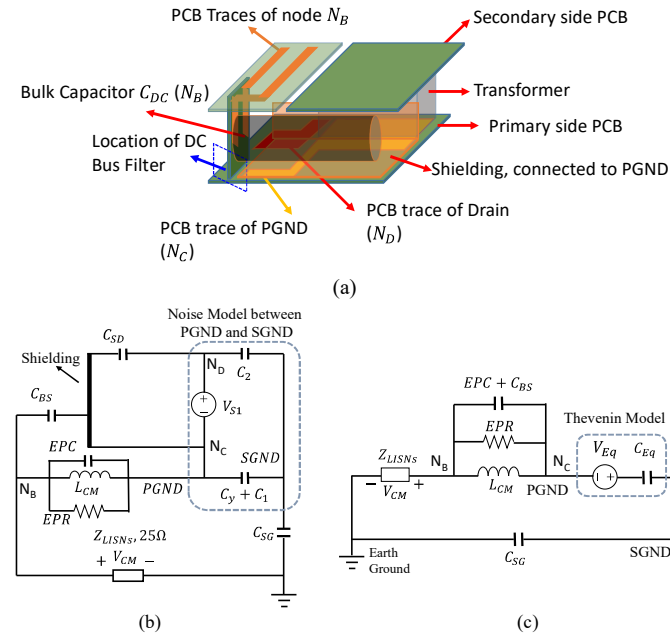


Fig. 14. (a) Apply a copper shielding to reduce the capacitive coupling due to the metal shell of electrolytic capacitor  $C_{DC}$ , (b) equivalent circuit, (c) CM noise model of a power adapter with the copper shielding.

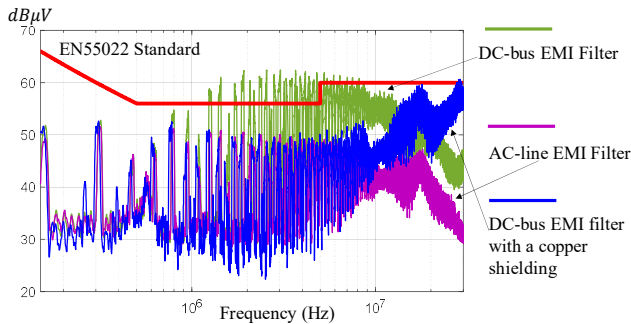


Fig. 15. Measured CM EMI noise with a copper shielding to eliminate the parasitic capacitive coupling between the metal shell of electrolytic capacitor  $C_{DC}$  and node  $N_D$ .

The equivalent circuit between PGND and SGND is therefore similar to the model shown in Fig. 3(b). As a result,

Fig. 14(b) is simplified to Fig. 14(c), where  $V_{Eq}$  and  $C_{Eq}$  are defined in (1) and (2). In Fig. 14(c), it is obvious that  $C_{BS}+EPC$  will degrade CM inductor HF performance. Fig. 15 shows the measured CM EMI noise with the shielding. In Fig. 15, with the copper shielding, the EMI noise between 1MHz and 12MHz is reduced by up to 13dB, and it is close to the EMI performance with an AC-line filter below 10MHz. The measured CM EMI is still higher than the EMI standard around 16MHz and 30MHz due to large  $C_{BS}$  based on Fig. 14 (b).

##### B. CM Noise Reduction with Capacitance Cancellation

To further reduce the CM EMI with single shielding technique so as to meet EMI standard at high frequencies, the other techniques should be explored. In [15][16][19][32][34], the parasitic winding capacitance cancellation techniques are proposed to cancel the EPC of an inductor.

Since  $C_{BS}$  is parallel to EPC, the winding capacitance cancellation technique can be explored to cancel  $C_{BS}+EPC$  in Fig. 14. As shown in Fig. 16, for an inductor with EPC, a cancellation capacitor  $C_{Can}$  which is equal to  $4EPC$  is connected between the tap of the two fully coupled windings on the inductor and the ground. The EPC can be canceled because a negative capacitance equal to  $-EPC$  is generated in parallel with EPC. The turn ratio of the two windings can be 1:1 or 1:n (if 1:n, the cancellation capacitance would be  $(n+1)^2EPC/n$ ). 1:1 turn ratio can easily achieve high coupling coefficient with bifilar winding structure, which is critical for HF EPC cancellation and improving CM inductor's HF performance [16][19], so it will be used here. The issue of applying the technique to  $L_{CM}$  is that there is no earth ground in the power adapter to connect  $C_{Can}$  when two-prong power plugs are used in these power adapters.

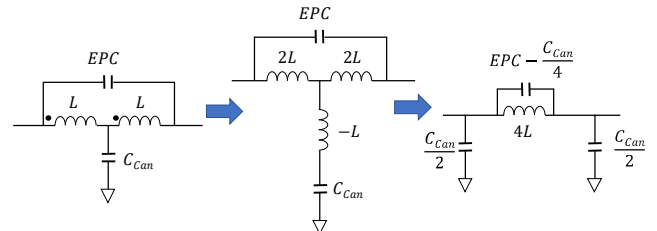


Fig. 16. Winding capacitance EPC cancellation for a CM inductor.

Further investigation on Fig. 16 discloses that  $C_{Can}$  is not necessarily connected to the earth ground because as long as  $C_{Can}$  is connected to the returning path of the CM noise current, for example, SGND in Fig. 14 (b), the cancellation principle still holds. This is because the network transformation in Fig. 16 is still correct even  $C_{Can}$  is not connected to the earth ground.

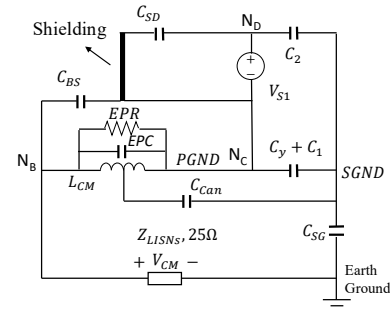


Fig. 17. Improve inductor performance by canceling  $EPC+C_{BS}$ .

Fig. 17 shows using this cancellation technique to cancel



$C_{BS}+EPC$  based on Fig. 14. A cancellation capacitor  $C_{Can}$  is connected between the center tap of one winding of the CM inductor and SGND. Fig. 18 shows the equivalent circuit. If  $C_{Can}$  is equals to  $4(EPC+C_{BS})$ ,  $EPC+C_{BS}$  is canceled. Because  $C_{Can}$  (to discuss later) and  $C_{SG}(10pF)$  is much smaller than  $C_{Eq}$ , which is  $C_1+C_y+C_2=575pF$ , based on Fig. 18, the voltage transfer gain  $Gain_{Can}$  after  $EPC+C_{BS}$  is canceled is given by (8), where  $V_{Eq}$  is defined in (1).

$$Gain_{Can} = \frac{V_{CM}}{V_{Eq}} \approx \frac{Z_{LISNs} C_{SG}}{C_{SG} + \frac{C_{Can}}{2}} \frac{s \left( C_{SG} + \frac{C_{Can}}{2} \right) \left( \frac{SL_{CM}}{EPR} + 1 \right)}{s^2 \left( C_{SG} + \frac{C_{Can}}{2} \right) L_{CM} + \frac{SL_{CM}}{EPR} + 1} \quad (8)$$

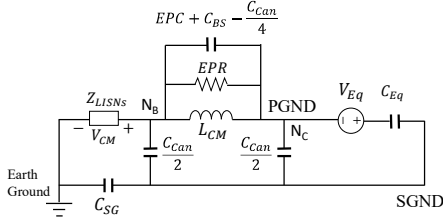


Fig. 18. CM noise model of a power adapter with capacitance cancellation.

It is shown in Fig. 18 that, with the cancellation technique,  $EPC+C_{BS}$  can be canceled. At the same time, the two resultant capacitances  $C_{Can}/2$  work as part of the CM filter for CM noise reduction. Because the two windings of  $L_{CM}$  are fully coupled, connecting  $C_{Can}=4(EPC+C_{BS})$  to the center tap of one winding gives the similar performance to that by connecting two  $C_{Can}=2(EPC+C_{BS})$  to the center taps of two windings respectively, where  $EPC$  is the total winding capacitance of the coupled two windings and it is equal to twice of the winding capacitance of one winding.

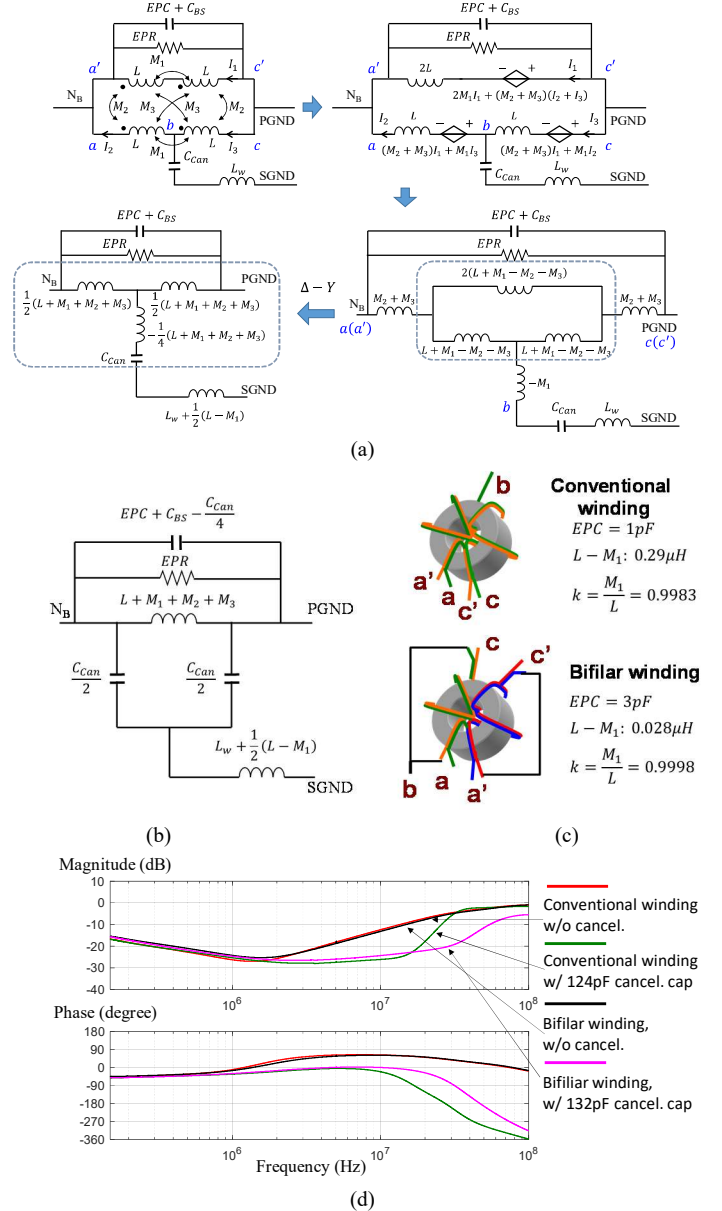
The circuit realization and analysis of this are shown in Fig. 19(a). As aforementioned, for CM analysis, the two windings of the CM inductor are in parallel. Therefore, the  $EPC$  and  $EPR$  of two windings are combined for simplification in Fig. 19(a). Due to the symmetrical winding structure, the mutual inductances can be defined as  $M1$  between winding halves in the same winding and  $M2$  or  $M3$  between winding halves in the different windings. A cancellation capacitor is connected to the center tap of one winding. In experiments, a wire is used to connect the capacitor to SGND. The length of the wire is 5cm and its inductance  $L_w$  is measured as 60nH. The ESL of the cancellation capacitor is only 2nH, which is much smaller than  $L_w$ , therefore, the ESL can be ignored. After decoupling the mutual inductances in Fig. 19(a), it is shown that  $M2$  and  $M3$  will not influence the HF performance of the cancellation, whereas  $M1$  and  $L_w$  will. The model in Fig. 19(a) can be further transformed into Fig. 19(b) with a similar method to that in Fig. 16. It is obvious that when the impedance of  $L_w+1/2(L-M1)$  is much smaller than  $C_{Can}$ , the cancellation technique works. After the resonance frequency  $f_r$ , which is expressed in (9), the cancellation technique will be ineffective.

$$f_r = \frac{1}{2\pi \sqrt{C_{Can} \left[ L_w + \frac{1}{2}(L - M_1) \right]}} \quad (9)$$

In order to increase  $M1$  so as to increase  $f_r$ , a bifilar winding structure is applied in Fig. 19(c) to improve the coupling of the winding halves in the same winding. In Fig. 19(c), the measured  $L-M1$  of the bifilar winding is much smaller than that of the

conventional winding structure. Therefore, HF performance can be greatly improved. The comparison of the measured S21 with 50Ω source and load impedances before and after applying the cancellation technique to these two winding structures is shown in Fig. 19(d). A simulation is also conducted in Saber to compare the transfer gains of the two cases in Fig. 19(e). Obviously, the effective frequency range of bifilar structure is wider than that of the conventional winding. The simulation results in Fig. 19(e) match the measured results in Fig. 19(d).

The comparison of the measured CM noise with the original DC-bus filter, with copper shielding added in Fig. 14 and further with winding capacitance cancellation technique in Fig. 19 is shown in Fig. 20. It is shown that, with capacitance cancellation technique and the bifilar winding structure, HF CM EMI can be further reduced by up to 15dB.





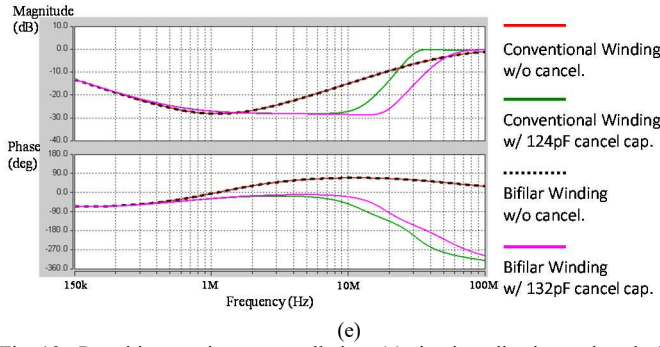


Fig. 19. Parasitic capacitance cancellation: (a) circuit realization and analysis with mutual inductance decoupling, (b) equivalent  $\pi$  model of (a), (c) winding structures of parasitic capacitance cancellation, (d) measured transfer gains w/ and w/o cancellation, (e) simulated transfer gains w/ and w/o cancellation.

The advantage of capacitance cancellation is that not only EPC but also the parasitic capacitance across the CM inductor is cancelled. The drawback is that since the cancellation capacitor is across PGND and SGND, it must meet safety requirements. Using one  $C_{Can}=4(EPC+C_{BS})$  on one of the two fully coupled windings instead of using two  $C_{Can}=2(EPC+C_{BS})$  on two fully coupled windings separately can improve safety (1 capacitor's failure rate is lower than that of 2 capacitors) and reduce cost.

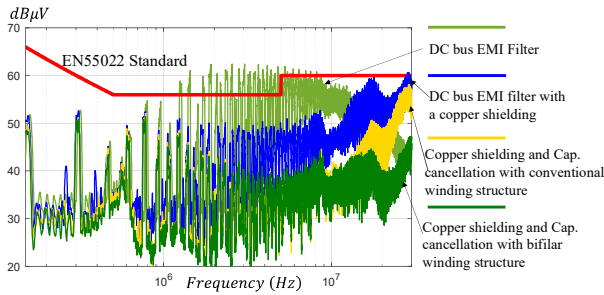


Fig. 20. Comparison of the measured CM noise.

### C. CM Noise Reduction with Double Shielding Technique

The single shielding technique in Fig. 14 can be further improved to reduce HF CM EMI with a double shielding technique in Fig. 21. In Fig. 21 (a), shielding 1 is close to  $C_{DC}$  and connected to the SGND. Shielding 2 is under shielding 1 and above PCB PGND. It is connected to PGND and shields nodes N<sub>C</sub> and N<sub>D</sub> from shielding 1. The equivalent circuit is shown in Fig. 21 (b).  $C_{BS1}$  is the parasitic capacitance between node N<sub>B</sub>, where  $C_{DC}$  is located, and shielding 1.  $C_{BS1}$  is connected to SGND via shielding 1. The measured  $C_{BS1}$  is 30pF.  $C_{SS}$ , the parasitic capacitance between two shielding, was measured as 6.2pF.  $C_{SS}$  is equivalently in parallel with  $C_y+C_1$  and can be ignored because it is much smaller than  $C_y+C_1$ .  $C_{DS2}$  is the parasitic capacitance between node N<sub>D</sub> and shielding 2 and it is in parallel with  $V_{S1}$ , so it can be ignored too.

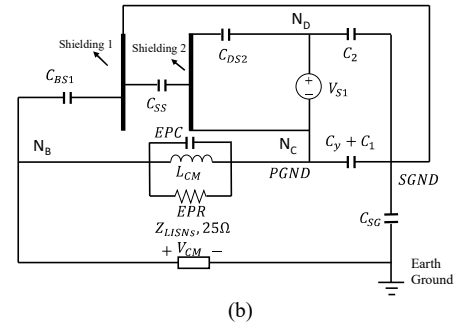
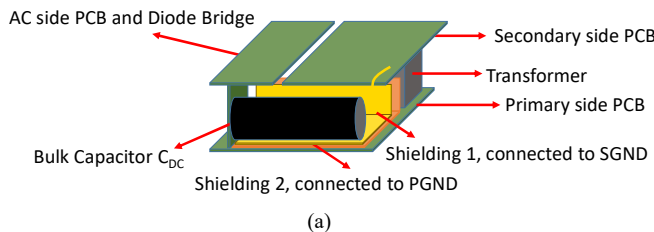


Fig. 21. (a) Physical realization of double shielding and (b) equivalent circuit.

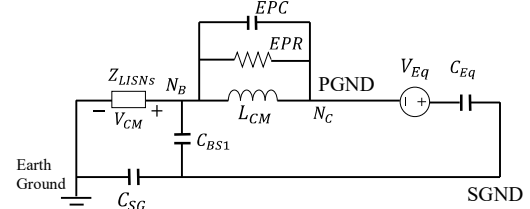


Fig. 22. Reduced CM equivalent circuit of an active clamp Flyback adapter with a DC-bus filter and double shielding technique.

The reduced equivalent circuit is shown in Fig. 22. As discussed above, in Fig. 22,  $C_{SS}$  is ignored, and  $C_{BS1}$  work as part of the CM filter, which helps to reduce HF CM noise. The  $C_{BS}$  in Fig. 14 has been eliminated. And the voltage gain  $Gain_{DS}$  is given by (10), where  $V_{Eq}$  is defined in (1).

$$Gain_{DS} = \frac{V_{CM}}{V_{Eq}} \approx \frac{Z_{LISNs} C_{SG}}{C_{SG} + C_{BS}} \frac{s(C_{SG} + C_{BS}) \left( \frac{SL_{CM}}{EPR} + 1 \right)}{s^2(C_{SG} + C_{BS1})L_{CM} + \frac{SL_{CM}}{EPR} + 1} \quad (10)$$

Based on Fig. 10, the impedance of CM inductor is mostly dominated by EPR at high frequencies, so small EPC (1pF) can be ignored in deriving (10) from Fig. 22. Comparing (8) and (10), both techniques have the similar performance. The only difference is  $C_{Can}/2$  in (8) is replaced with  $C_{BS1}$  in (10). Fig. 23 shows the comparison of the measured CM noise.

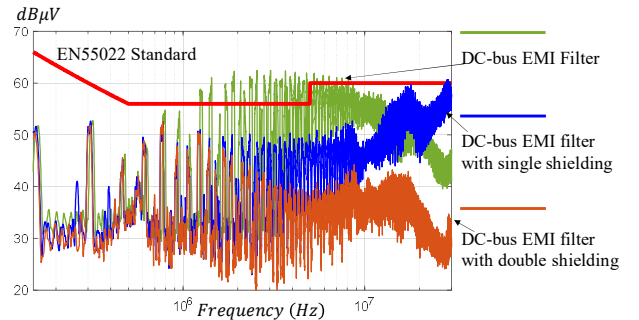


Fig. 23. Measured CM noise of an active clamp Flyback adapter with a DC-bus filter and double shielding technique.

In Fig. 23, comparing with the single shielding technique, the double shielding technique can further reduce the HF CM noise above 2MHz and meet the EMI standard because of the elimination of  $C_{BS}$  in single shielding implementation and the utilization of  $C_{BS1}$  as CM filter components. In this case, because 30pF  $C_{BS1}$  is much larger than 10pF  $C_{SG}$ , based on Fig. 22,  $C_{BS1}$  has positive effects on the reduction of EMI.

The general rule of shielding design is that its shape and size should cover the facing areas between the  $C_{DC}$  and PGND, between the  $C_{DC}$  and pulsating PCB traces, between the  $C_{DC}$  and transformer windings. It should be noted that for safety reason, both copper shielding and the bulk capacitor  $C_{DC}$  should be

covered with insulation tapes. The two shielding should have the same size and shape. The shielding performance is not susceptible to the distance between the capacitor and the shielding as long as the facing area mentioned above is fully covered by the shielding and the distance between  $C_{DC}$  and the shielding is much smaller than shielding size because the electric field fringing effect is minimized under that condition, which results in the minimized capacitive couplings between  $C_{DC}$  and PGND, between  $C_{DC}$  and pulsating PCB traces, and between  $C_{DC}$  and transformer windings.

It should be noted that for power adapters, typically a bridge rectifier is employed at the AC input. As analyzed previously, a DC-bus EMI filter helps to reduce the size and the power loss of the EMI filter. However, the effects of capacitive coupling tends to be significant in the converter, so the techniques proposed in this paper are applicable to general AC/DC adapters with a diode bridge rectifier and a DC-bus filter.

## V. CONCLUSIONS

In the paper, the capacitive couplings within active clamp Flyback converters are investigated. The important capacitive couplings in an active clamp Flyback converter with DC-bus filter are first identified. The capacitive couplings are then extracted using a VNA. The CM noise model which includes capacitive couplings are developed. Based on the developed models, the effects of capacitive couplings on CM EMI is analyzed. Techniques to reduce the CM noise due to capacitive couplings are developed. Experiments were conducted to validate the proposed theory and techniques. It is found that the electrolytic capacitor on DC bus can significantly contribute to the capacitive couplings and therefore increase CM noise in an active clamp Flyback converter with a DC-bus filter. Shielding and parasitic capacitance cancellation techniques are effective to reduce the CM EMI.

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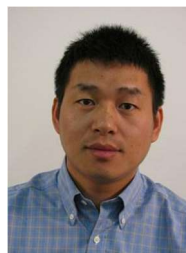
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