Investigating a Guard Trace Ring to Suppress the Crosstalk due to a Clock Trace on a Power Electronics DSP Control Board

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***Abstract*—The grounded guard trace ring is usually utilized to suppress the interference in high-speed printed circuit boards or IC packages. Although the guard ring can reduce crosstalk, its performance is greatly affected by the effectiveness of its design. This paper first investigates the mechanism of the crosstalk cancelation with a grounded guard ring. The paper then discusses and analyzes several grounding patterns based on a lumped circuit model. The analysis applies to the applications where the dimensions of PCB traces are smaller than 5% of the wavelength at the highest frequency. It is found that the best grounding patterns for the guard trace ring is to ground its two ends instead of using multipoint grounding within the concerned frequency range from 10 to 200 MHz in this paper. The theoretical analysis and the developed technique are verified by electromagnetic field distribution plots and the four-ports scattering parameters that are simulated in ANSYS HFSS 3-D electromagnetic simulation software. Experiments were finally conducted to validate the analysis and the proposed technique.**

***Index Terms*—Clock trace, crosstalk, EMI, grounding, guard trace ring, inductive coupling.**

I. Introduction

In the digital signal processor (DSP) control board of a power electronics system, the crosstalk, whose mechanism has been explained in [1]–[6], from high *di/dt* traces or high *dv/dt* nodes may seriously degrade the performance of the DSP board. There are three critical signal traces which can cause the near field coupling and radiated EMI in the DSP control board. They are clock traces, data buses and certain I/O traces. The clock signal is one of the worst offenders due to its large amplitudes and high frequency harmonics. The control board in Fig. 1 consists of a DSP controller and a complex programmable logic device. They are synchronized with a clock signal. The near-field crosstalk usually happens between the long clock trace and I/O traces which are routed along the clock trace. Due to the large number of I/O traces, the crosstalk could be very serious.

Conventionally, the long clock trace is routed with a grounded trace ring. The grounded trace ring is supposed to shield the near EM field between the clock trace and other critical signal traces on the printed circuit board (PCB) [2], [3]. The grounded trace ring is also called guard ring or guard trace. For simplification, the guard ring will be used in this paper. The effectiveness of a grounded guard ring for the suppression of crosstalk between two adjacent transmission lines have been verified in the literature [4]. However, the theory for the modeling of a guard ring including the number and position of grounding vias and the technique to improve guard rings have not been well established. It has been subject to many online discussions in the PCB signal integrity community. There is also a lack of analytical work to address this topic [5], [7]–[11], [13].

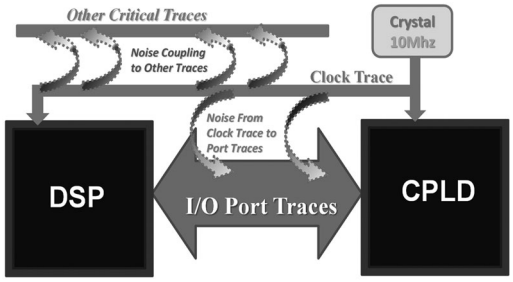

Fig. 1. Crosstalk due to clock traces in a DSP control board of a power electronics system.

This paper aims to contribute to this theme by analyzing the mechanism of crosstalk reduction with guard rings and presenting the theoretical analysis for the number and position of the grounding vias on the guard rings.

A clock trace with a guard ring on a PCB board will be presented in Section II. The equivalent circuit model for the clock trace together with its guard ring is developed. The crosstalk due to the clock trace is analyzed from the aspects of capacitive coupling and inductive coupling. Based on the analysis of the developed model, the grounding pattern to improve the performance of the guard ring is proposed. It will be shown that comparing with other multipoint grounding patterns, the guard ring grounded at its two ends gives the best near magnetic field shielding without sacrificing the effectiveness of electric field shielding. The technique to improve guard ring's performance is developed.

Due to the high power operation of the investigated power inverter system, the power inverter's switching frequency is only several kHz. DSP does not need to have very high clock frequency to process power control. 10-MHz clock frequency is a typical frequency used for the DSP in the power inverter system under investigation. Because of this, this paper will only analyze

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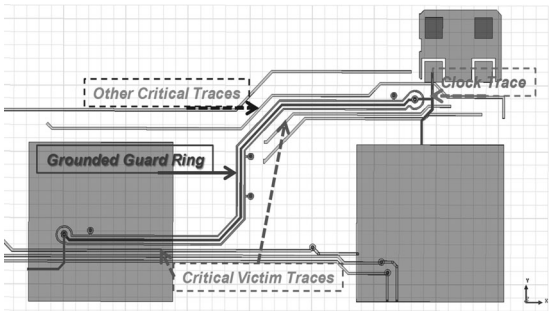

Fig. 2. Clock trace with a grounded guard ring.

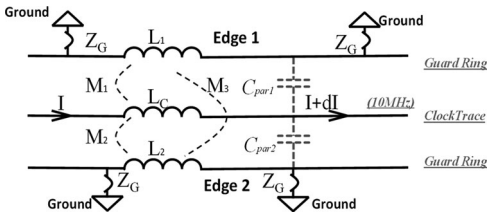

Fig. 3. Equivalent circuit model of a clock trace and its guard ring.

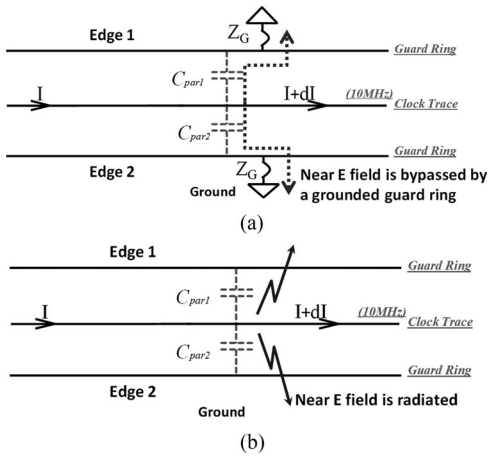

Fig. 4. Mechanism of near electric field shielding with a guard ring: (a) grounded guard ring and (b) ungrounded guard ring.

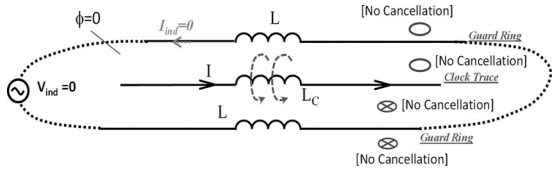

Fig. 5. Floating guard ring cannot shield near magnetic field.

the near field crosstalk within the concerned frequency range from 10 to 200 MHz, where the dimensions of PCB traces are smaller than 5% of the wavelength (λ) at the highest frequency.

In Sections III and IV, the theoretical analysis and the proposed technique for the guard ring are validated with both full-wave 3-D electromagnetic field simulations and crosstalk experiments. The simulation and experimental results show that the proposed technique can greatly reduce the near field crosstalk from a clock trace.

II. Modeling and Analysis of a Guard Ring

It is assumed that the dimensions of the traces under investigation are smaller than 0.05λ [12] within concerned frequency range (10–200 MHz), so lumped parameters can be used for all the analysis. In this paper, the trace length is 4–6.5 cm and 0.05λ at 200 MHz is 7.5 cm, so the condition is met.

A. Guard Ring of a Clock Trace

In Fig. 2, on a four-layer PCB in the control system of a power electronic system, the crosstalk due to undesired capacitive, inductive or conductive coupling from one unshielded noisy trace to other traces is always affecting circuit performance. In Fig. 1, one of the most susceptible traces is I/O traces because they are close to the high frequency clock trace. The grounded guard ring is routed around the clock trace to reduce these undesired couplings.

To investigate the mechanism of the reduction of near field couplings with a guard ring, a circuit model is developed in Fig. 3 for a clock trace with a guard ring. The inductor L_C is the inductance of the clock trace which generates the near magnetic field. L_1 and L_2 are the inductance of the edge 1 and edge 2 of the guard ring. The inductance M_1, M_2 and M_3 are the mutual inductance among the clock trace and the two edges of the guard ring. The capacitance $C_{\rm par1}$ and $C_{\rm par2}$ are the capacitance between the clock trace and two edges of the guard ring. Z_G is the grounding impedance. The shielding mechanism will be analyzed from the aspects of capacitive coupling and inductive coupling between the clock trace and the guard ring.

B. Capacitive Coupling Reduction With a Guard Ring

The grounded guard ring can partially shunt the electric (E) field from the clock trace to the ground with the help of capacitance $C_{\rm par1}$ and $C_{\rm par2}$. The green dash line in Fig. 4(a) shows the current paths. On the other hand, for an ungrounded guard ring, the near E field radiates to the air and easily couples to surrounding critical traces as shown in Fig. 4(b).

One of the objectives of grounding a guard ring is therefore to shield near E field by shunting it to ground. Because of this, an ungrounded guard ring cannot shield E field. As the impedances of $C_{\rm par1}$ and $C_{\rm par2}$ are usually much higher than those of the guard ring and the grounding vias, decreasing grounding impedance Z_G cannot significantly improve the E field shielding performance. Because of this, multipoint grounding may not greatly improve the E field shielding effectiveness unless the guard ring is very long.

C. Inductive Coupling Reduction With a Guard Ring

The inductive coupling (crosstalk) is also very important in the design of high speed digital circuits. In Fig. 5, the clock trace carries high *di/dt* currents (10-MHz clock signal) which generate high near magnetic (H) field. The generated H field contaminates other critical traces nearby on the board.

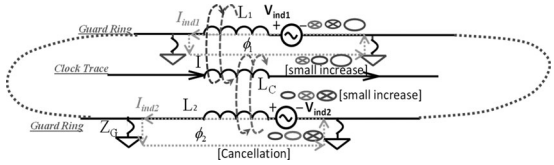

Fig. 6. Guard ring with two-point grounding on each edge can partially shield near magnetic field from a clock trace.

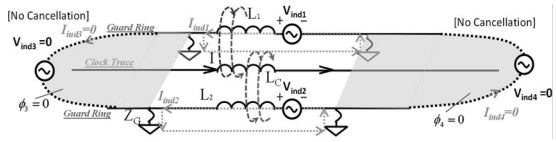

Fig. 7. Guard ring on the two sides of the grounding loops has no magnetic field cancelation performance.

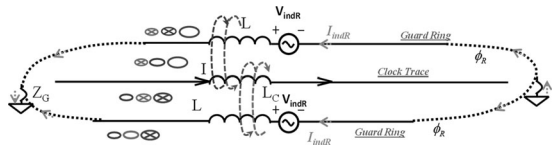

Fig. 8. Improve a guard ring's performance by moving grounding points to the two ends.

A floating guard ring is shown in Fig. 5. In Fig. 5, the direction and magnitude of the H field are represented with blue circle and blue cross. The bigger the circle is; the larger the magnitude is. The crossed circle means the direction of the H field is into the paper and the blank circle means the H field is out from the paper. The blue dashed arrows in the figure represent the magnetic flux generated by the clock trace.

Because the guard ring is symmetrical to the clock trace, the net magnetic flux linkage ϕ to the guard ring is zero as shown in the figure. As a result, the induced voltage $V_{\rm ind}$ is zero as given by (1); so does the induced current $i_{\rm ind}$. Because $i_{\rm ind}$ is zero, the guard ring cannot generate an H field to cancel that from the clock trace so it cannot shield near magnetic field.

$$V_{\rm ind} = \frac{d\phi}{dt} = 0. \tag{1}$$

The guard ring is grounded from both edge 1 and edge 2 through vias in Fig. 6. Each edge uses a two-points grounding. The inductances of the guard ring between the two grounding vias are L_1 and L_2 for edge 1 and edge 2, respectively. The grounding impedance of each grounding path is Z_G. Two loops are shown in the figure. The loop 1 includes L_1, two $Z_G s$ and the ground. The loop 2 includes L_2, two $Z_G s$ and the ground. As shown by the dashed blue arrows in the figure, the near magnetic field generated from the clock trace links the two loops. The linkages $\phi_{1,2}$ are not zero. As a result, the voltages $V_{\rm ind1}$, $V_{\rm ind2}$ and the currents $I_{\rm ind1}$, $I_{\rm ind2}$ are induced in the loops. $V_{\rm ind1}$, $V_{\rm ind2}$ and $I_{\rm ind1}$, $I_{\rm ind2}$ are given by (2) to (4).

$$V_{\rm ind1,2} = \frac{d\phi_{1,2}}{dt} \tag{2}$$

$$I_{\rm ind1} = \frac{V_{\rm ind1}}{Z_{L1} + 2Z_G} \tag{3}$$

$$I_{\rm ind2} = \frac{V_{\rm ind2}}{Z_{L2} + 2Z_G}. \tag{4}$$

The $I_{\rm ind1}$ and $I_{\rm ind2}$ generate a reverse H field to partially cancel the H field from the clock trace as shown by the purple and red dashed arrows in the figure. The directions and magnitudes of the H field generated from clock trace and two loops are represented with colored circles and crosses. As shown in the figure, the H field outside of the guard ring is greatly reduced. The H field inside the guard ring is slightly increased because the distance to two loops are different.

Since the induced currents are much smaller than the currents on the clock trace, the cancelation performance can be improved by increasing $I_{\rm ind1}$ and $I_{\rm ind2}$. The bigger $I_{\rm ind1}$ and $I_{\rm ind2}$ are, the better the cancelation is. Reducing the impedances of the guard ring and the grounding paths can improve the performance. However, the guard ring structure in Fig. 6 does not give the best performance since there is no H field cancelation on the two sides of the loops as illustared in Fig. 7.

In Fig. 7, for the shaded regions on the two sides of the ring loop, because the guard ring is symmetrical to the clock trace, the net flux linkage $\phi_{3,4}$ is zero. As a result, the net induced voltages $V_{\rm ind3,4}$ are zero which leads to a zero induced currents $I_{\rm ind3,4}$ and therefore there is no H field cancelations. This is described by (5) and (6).

$$V_{\rm ind3,4} = \frac{d\phi_{3,4}}{dt} = 0 \tag{5}$$

$$I_{\rm ind3,4} = 0. \tag{6}$$

D. Optimization of a Guard Ring

Based on the analysis, to improve a guard ring's H field shielding performance, the grounding points can be moved and merged to the two ends of the guard ring as shown in Fig. 8. In Fig. 8, the induced voltages and currents are equal in the two loops between the two edges of the guard ring and the ground.

The induced voltage $V_{{\rm ind}R}$ and current $I_{{\rm ind}R}$ are given by (7) and (8).

$$V_{{\rm ind}R} = \frac{d\phi_R}{dt} \tag{7}$$

$$I_{{\rm ind}R} = \frac{V_{{\rm ind}R}}{Z_L + 4Z_G}. \tag{8}$$

In (7), ϕ_R is the flux linkage in one loop. The $4Z_G$ in denominator is due to the fact that $2I_{{\rm ind}R}$ flows through $Z_G s$. It is obvious that decreasing loop impedance can increase induced currents therefore improves the cancelation performance. The guard ring's magnetic field shielding performance can be characterized with mutual inductances in Fig. 9.

In Fig. 9, L_V is the inductance of a victim trace. $V_{{\rm ind}V}$ is the induced voltage due to the clock trace and the guard ring. All the mutual inductances between any two self-inductances are shown in the figure. It is assumed that the mutual inductances

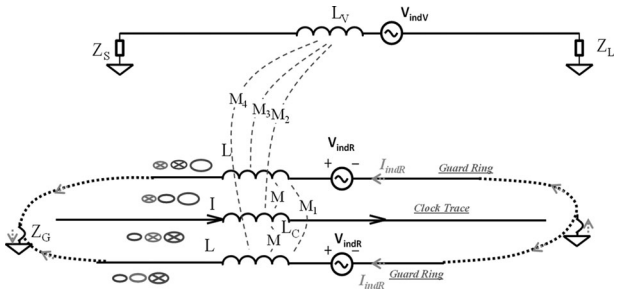

Fig. 9. Characterization of magnetic field shielding with mutual inductances.

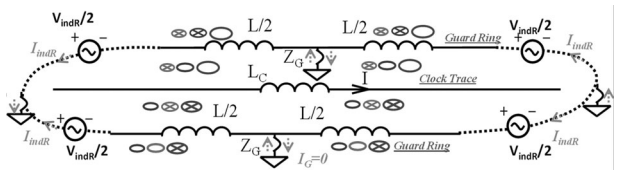

Fig. 10. Two more grounding points in the middle of the guard ring do not improve its performance of shielding magnetic field.

and self-inductances meet the condition (9).

$$L, L_C, L_V >> M, M_1, M_2, M_3, M_4 \tag{9}$$

. The induced currents on the guard ring is therefore

$$I_{\mathrm{ind}R} \approx \frac{M}{L+4L_G} I. \tag{10}$$

The induced voltage on the victim trace is therefore

$$\begin{aligned} V_{\mathrm{ind}V} &\approx j\omega M_2 I - j\omega(M_3+M_4) I_{\mathrm{ind}R} \\ &\approx j\omega \left[M_2 - \frac{M(M_3+M_4)}{L+4L_G} \right] I = j\omega M_{eq} I \end{aligned} \tag{11}$$

where

$$M_{eq} = M_2 - \frac{M(M_3+M_4)}{L+4L_G}. \tag{12}$$

In (11), M_{eq} is an equivalent mutual inductance between the clock trace and the victim trace. The smaller the M_{eq} is, the better the guard ring's shielding performance is. From (12), increasing the mutual inductance *M* between the guard ring and the clock trace or decreasing the guard ring loop inductance $L + 4L_G$ can improve a guard ring's shielding performance.

E. Discussion

As discussed, moving the grounding points to the two ends of the guard ring can greatly improve its performance. The question is if more grounding points on the guard ring can further improve its performance? Fig. 10 shows two more grounding points added to the middle of the guard ring.

As shown in Fig. 10, because the guard ring and the clock trace are symmetrical to the two middle grounding points, the net currents flowing from the guard ring to the ground through the two middle grounding vias are zero. As a result, it does not improve the guard ring's magnetic field shielding performance. The induced voltages and currents inside the guard ring are still given by (7) and (8). It has also been analyzed previously

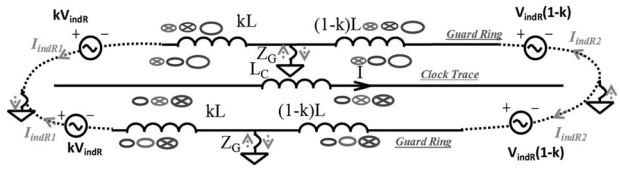

Fig. 11. Two more grounding points on the guard ring do not improve its performance of shielding magnetic field.

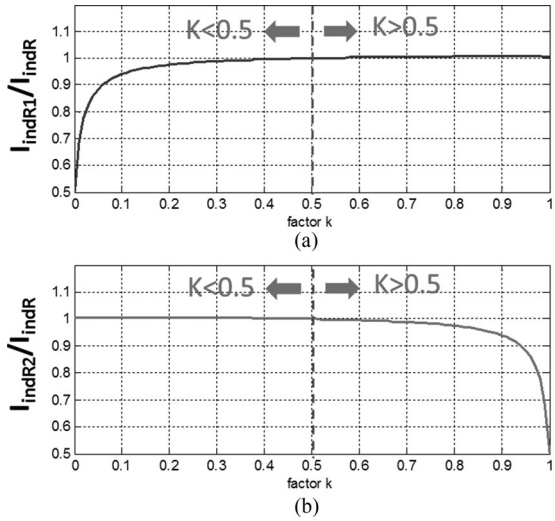

Fig. 12. Induced currents in the guard ring reduces when two more grounding vias are added to both edges: (a) current ratio on the left fraction and (b) current ratio on the right fraction.

that the multipoint grounding may not improve the electric field shielding performance since the impedances of $C_{\mathrm{par}}s$ are much bigger than Z_L and Z_G within the concerned frequency range unless the clock trace is very long.

If the two added grounding points are not in the middle of the guard ring but at the same position on each edge as shown in Fig. 11, the factor *k* can be used to represent the location of the grounding points on the edge of the guard ring. $k = 0$ means the grounding points are at the left end. $k = 1$ means the grounding point is at the right end. $k = 0.5$ means the grounding point is in the middle. The induced voltage on the left fraction of the guard ring is proportional to the length of the guard ring; therefore, it is proportional to *k*. So does the inductance. On the right fraction, they are proportional to *1–k* instead.

The current ratios of the induced currents $I_{\mathrm{ind}R1}$ and $I_{\mathrm{ind}R2}$ with one more grounding point added to each edge to $I_{\mathrm{ind}R}$ with only two grounding points at the two ends as a function of *k* are given by (13) and (14). L_G and *L* can be extracted using ANSYS HFSS 3-D.

$$\frac{I_{\mathrm{ind}R1}}{I_{\mathrm{ind}R}} = \frac{[(1+k)L_G + k(1-k)L][L+L_G]}{3L_G^2 + k(1-k)L^2 + 2L_G L} \tag{13}$$

$$\frac{I_{\mathrm{ind}R2}}{I_{\mathrm{ind}R}} = \frac{[(2-k)L_G + k(1-k)L][L+L_G]}{3L_G^2 + k(1-k)L^2 + 2L_G L}. \tag{14}$$

Their current ratio curves are shown in Fig. 12. It is shown that the induced currents are reduced if $k < 0.5$ and almost

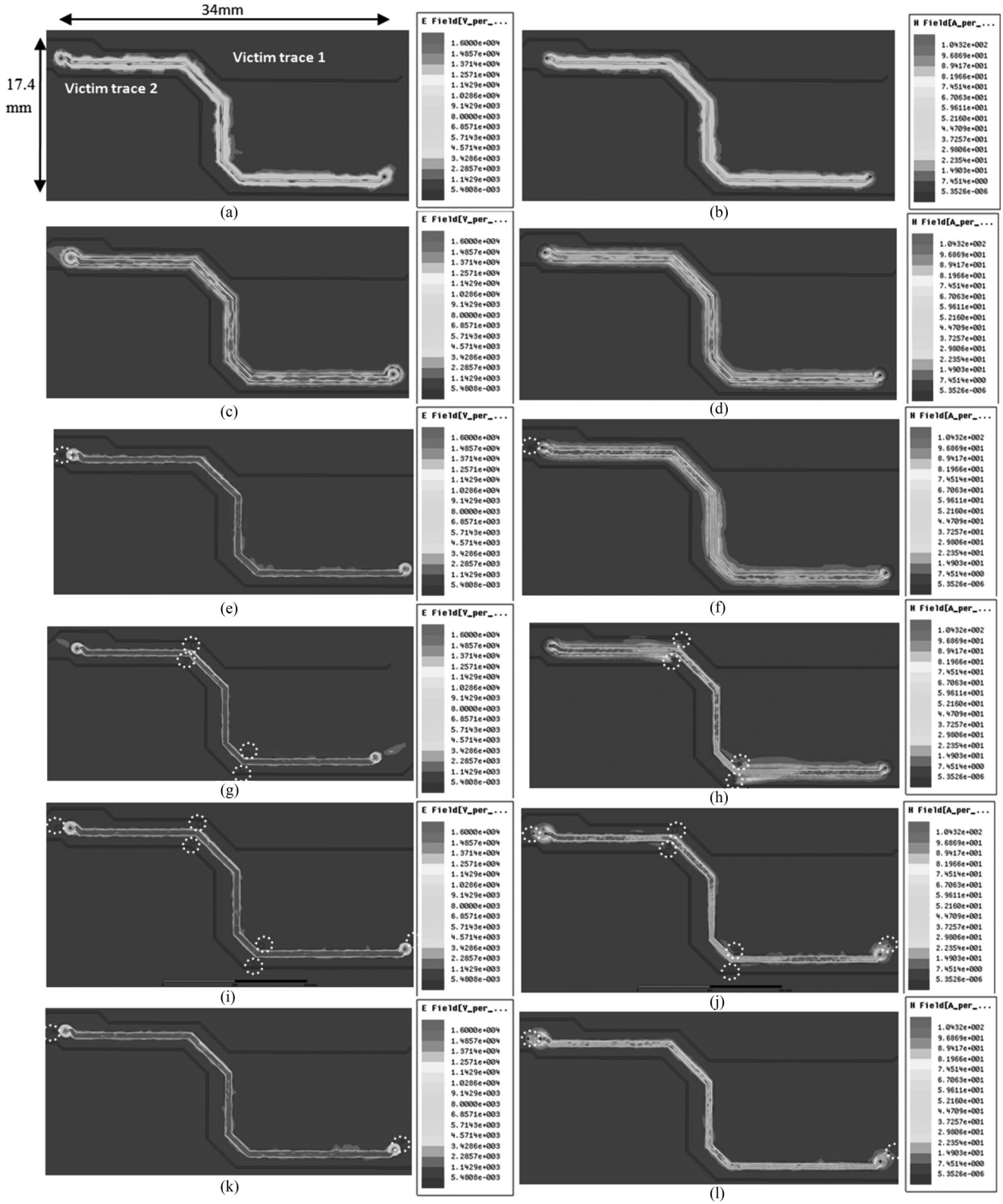

Fig. 13. Simulated E field [V/m] and H field [A/m] distributions (the grounding vias are highlighted with dash circles). (a)–(b) E and H field distributions without guard rings. (c)–(d) E and H field distributions with a floating guard ring. (e)–(f) E and H field distributions with a guard ring grounded by one via at source end. (g)–(h) E and H field distributions with a guard ring grounded by four vias in the middle. (i)–(j) E and H field distributions with a guard ring grounded by six vias (four vias in the middle and two vias at both ends). (k)–(l) E and H field distributions with a guard ring grounded by two vias at both ends only.

unchanged if $k > 0.5$. Because the induced current is reduced on the side with $k < 0.5$, the overall performance of the guard ring is degraded. Because of this, more grounding vias may degrade the guard ring's performance of shielding H field.

III. Simulation Verification for the Developed Theory and Technique

To verify the analysis, a full-wave 3-D electromagnetic simulation was carried out in software ANSYS HFSS. The clock trace with a guard ring was simulated based on a four-layer PCB. The simulated model includes two wiring layers, a power plane and a ground plane. Two victim signal traces (victim trace 1 and 2) are also included. Fig. 13 shows the simulated E and H fields on the same plane as the clock trace with different guard rings at 10-MHz clock frequency. The dimensions of the investigated area are also shown in the figures. The distance between the guard ring and the clock trace is 0.23 mm. The width of the clock and victim traces is 0.2 mm and the width of the guard ring trace is 0.15 mm.

Six cases were simulated. For the first case in (a), (b), no guard ring is presented. The second case (c), (d) has a floating guard ring. For the third case (e), (f), the guard ring has a one-point grounding. For the fourth case (g), (h), the guard ring has a four-points grounding in the middle but not at the two ends. For the fifth case (i), (j), the guard ring has a six-point grounding: two at the two ends and four in the middle. For the sixth case (k), (l), the guard ring is grounded at the two ends only. The E and H fields outside of the guard ring are to be investigated.

In the simulations, the material of PCB board is FR4 glass epoxy and the PCB traces are copper. The completed PCB board was developed in the simulator.

From the Fig. 13(a) and (d), the floating guard ring has no shielding effects on either E or H field. This agrees with the analysis in Section II. In Fig. 13(e) and (f), the guard ring with one point grounding can shield E field but not H field. It agrees with the analysis previously since the grounding can shunt part of E field to the ground. In Fig. 13(g) and (h), four-point grounding in the middle of the guard ring can only shield the H field between the two grounding points on each edge. The H field outside of the four-point grounding region is not reduced. The E field distribution is almost the same as the one-point grounding. These agree with the previous analysis. In Fig. 13(i) and (j), two more grounding vias are added to the two ends of the guard ring. E field has no improvement and H field is reduced on the two sides. In Fig. 13(k) and (l), only the two ends of the guard ring are grounded. Compared with Fig. 13(i) and (j), the H field in the whole length range is reduced. E field is almost the same as the single-point grounding. These simulation results validate the analysis in Section II.

The simulated crosstalk curves from the clock trace to victim traces for difference cases in Fig. 13 are shown in Figs. 14 and 15. One more case was simulated for eight grounding vias. The concerned frequency is from clock frequency 10 to 200 MHz as explained in Section I. In Fig. 14, the crosstalk curves between the clock trace and the victim trace 2 are compared for both near end (NEXT) and far end (FEXT). In Fig. 15, the crosstalk curves between the clock trace and the victim trace 1 are compared for both near end (NEXT) and far end (FEXT).

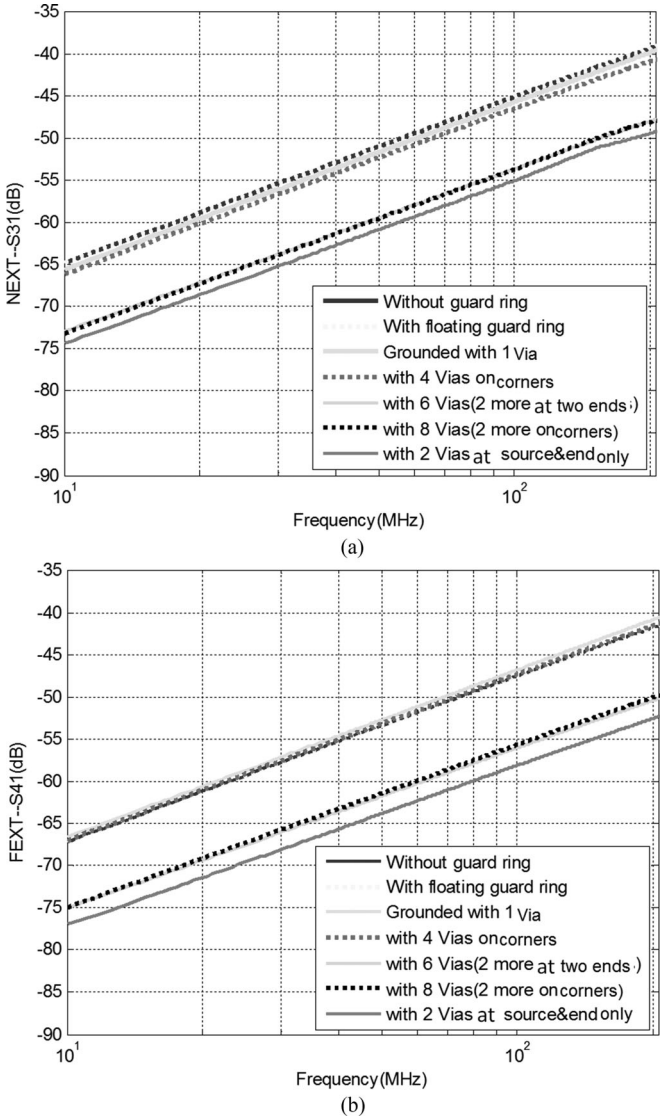

Fig. 14. HFSS simulation results: NEXT and FEXT crosstalk magnitude in dB between the clock trace and the victim trace 2: (a) NEXT plot and (b) FEXT plot.

The simulated crosstalk curves agree with the results in Fig. 13. From Figs. 14 and 15, the guard ring grounded at the two ends gives the lowest crosstalk. A 10–15 dB crosstalk reduction is achieved compared with that without guard rings. More grounding points do not improve the performance. On the other hand, the crosstalk may be even worse if the guard ring is not properly grounded. In the concerned frequency range 10–200 MHz, the simulated crosstalk is proportional to frequency as (11) predicted.

IV. Experimental Verification for the Developed Theory and Technique

Experiments were conducted for the same layouts as used in the simulations. Fig. 16(a) and (b) shows the PCB layouts and the measurement setup used in the experiments. Same as that

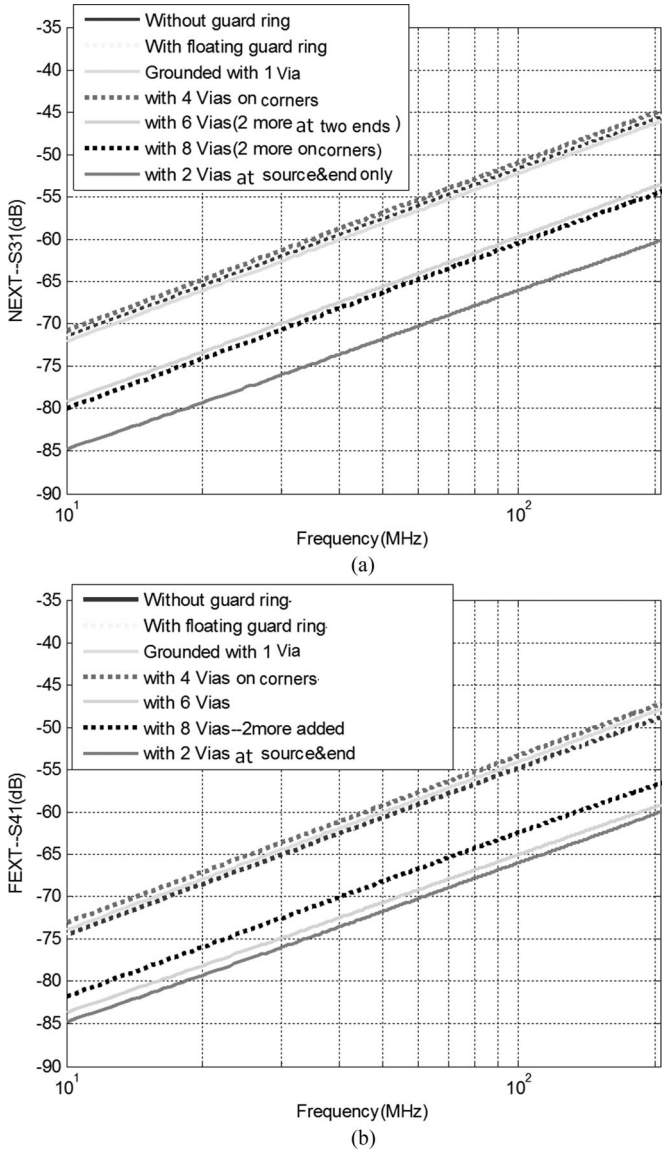

Fig. 15. HFSS simulation results: NEXT and FEXT crosstalk magnitude in dB between the clock trace and the victim trace 1. (a) NEXT plot and (b) FEXT plot.

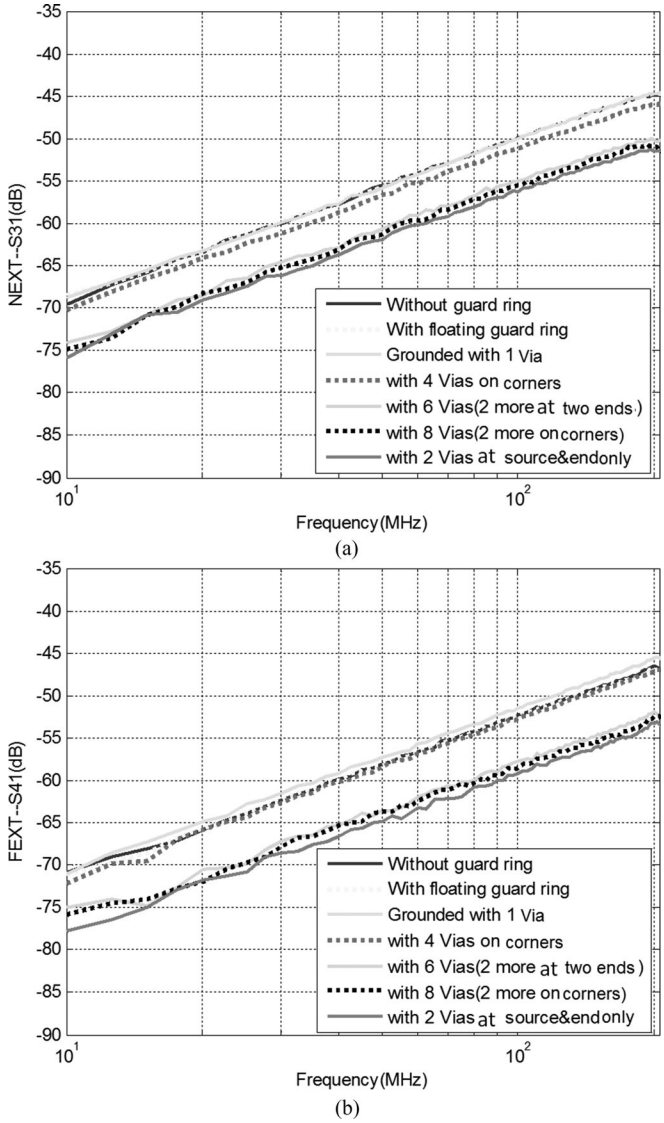

Fig. 17. Measured crosstalk curves (dB) between the clock trace and the victim trace 2: (a) NEXT plot and (b) FEXT plot.

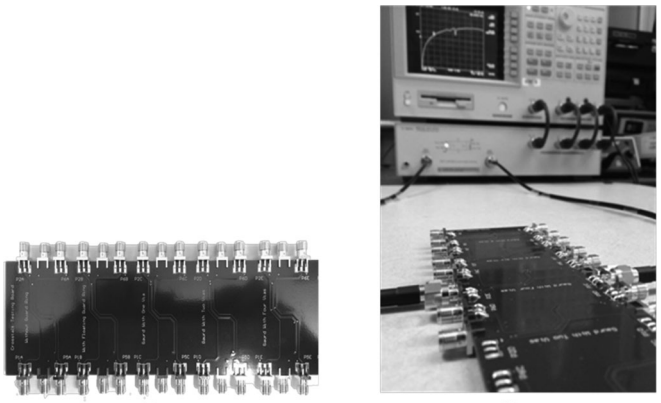

Fig. 16. (a) PCB layout and (b) measurement setup.

in the simulations, the distance between the guard ring and the clock trace is 0.23 mm; and there are victim traces 1 and 2 near the clock trace.

An Agilent 4395A network analyzer is used for the crosstalk (S-parameters) measurement. The measured frequency range is from 10 to 200 MHz.

The measured crosstalk curves from the clock trace to victim traces for difference cases are shown in Figs. 17 and 18. They are correspondent to the cases in Figs. 14 and 15.

In Figs. 17 and 18, both the near end crosstalk (NEXT) curves and far end crosstalk (FEXT) crosstalk curves from the clock trace to the victim traces 2 and 1 are compared. In Fig. 18, the crosstalk magnitude at low frequencies is smaller than the resolution of the network analyzer; as a result, network analyzer's background noise is observed in the measurement results from 10 to 20 MHz. The conclusion from the

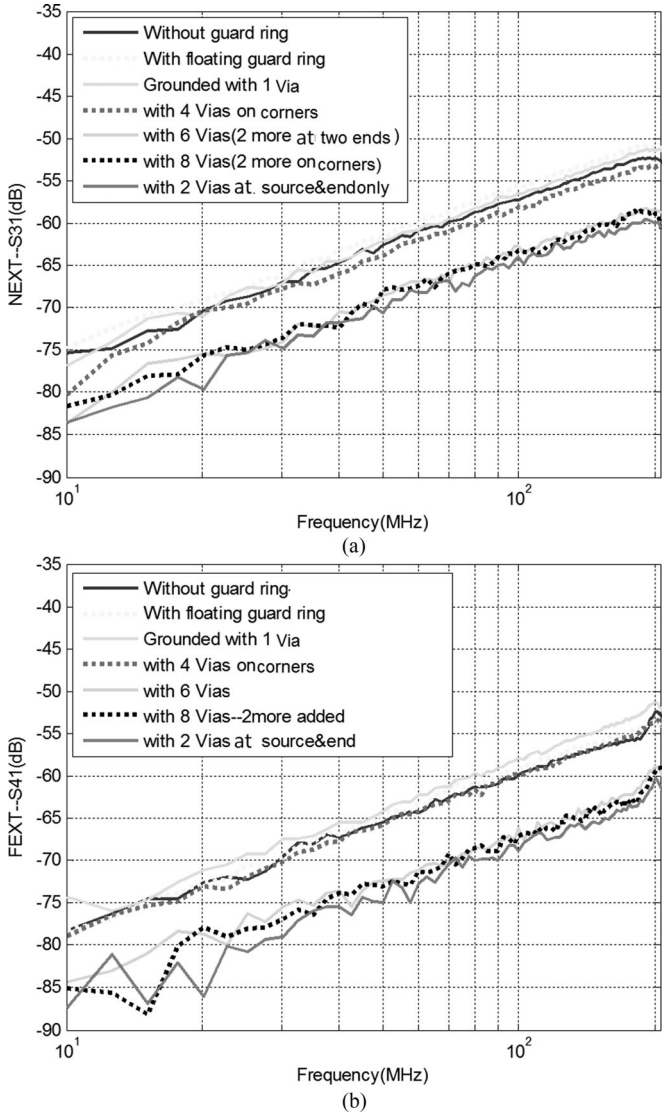

Fig. 18. Measured crosstalk curves (dB) between the clock trace and the victim trace 1: (a) NEXT plot and (b) FEXT plot.

measured results in Figs. 17 and 18 is the same as that from the simulated results in Figs. 14 and 15. It is shown that the guard ring grounded at the two ends gives the lowest crosstalk. A 7–11 dB crosstalk reduction is achieved compared with that without guard rings. In the concerned frequency range, the measured crosstalk is proportional to frequency as (11) pre-dicted.

For the investigated prototypes, the calculated per unit inductance and capacitance of the victim and clock traces are 4.5 nH/cm and 0.7 pF/cm, respectively. The length of the clock trace is 4.5 cm. The length of the victim trace 1 and the victim trace 2 is 5.0 and 6.5 cm, respectively. Compared with 50-Ω source and load impedances used in S-parameter measurement in Figs. 17 and 18, the effects of these capacitance and inductance on the crosstalk can be ignored for the concerned frequency range, 10 to 200 MHz. Because of this, based on the measured crosstalk $S_{\mathrm{Crosstalk}}$ and the principle of S-parameter

TABLE I
EXTRACTED EQUIVALENT MUTUAL INDUCTANCE

M_{eq} (nH)	No Ring	Floating Ring	Ring w/ 1 via	Ring w/ 2 vias	Ring w/ 4 vias	Ring w/ 6 vias	Ring w/ 8 vias
Victim 1 (NEXT)	0.263	0.263	0.250	0.094	0.202	0.119	0.129
Victim 1 (FEXT)	0.190	0.188	0.196	0.056	0.162	0.076	0.071
Victim 2 (NEXT)	0.533	0.522	0.518	0.252	0.468	0.296	0.273
Victim 2 (FEXT)	0.447	0.392	0.432	0.181	0.381	0.213	0.209

measurement, the equivalent mutual inductance M_{eq} between the clock trace and the victim traces can be approximately given by

$$M_{\mathrm{eq}} \approx \frac{50\Omega \times |S_{\mathrm{Crosstalk}}|}{\pi f}. \tag{15}$$

In (15), f is the frequency at which the crosstalk $S_{\mathrm{Crosstalk}}$ is measured. Based on (15) and Figs. 17 and 18, the equivalent mutual inductance between the clock trace and victim traces is extracted in Table I.

In Table I, the guard ring grounded at both ends always gives the lowest equivalent mutual inductance. It is found that with the help of the guard ring grounded at both ends, for the near end, M_{eq} is reduced from 0.263 nH to 94 pH for victim trace 1 and from 0.533 to 0.252 nH for victim trace 2. For the far end, M_{eq} is reduced from 0.190 nH to 56 pH for victim trace 1 and from 0.447 to 0.181 nH for victim trace 2. The performance of the guard ring is therefore quantified.

The simulated, measured and calculated NEXT and FEXT curves are compared for victim trace 2 in Fig. 19(a) and (b). In Fig. 19(a) and (b), two cases are compared. For the first case, the clock trace has no guard ring. For the second case, the clock trace has a guard ring grounded at its two ends. It is shown that the calculated curves based on the extracted equivalent mutual inductance in Table I match the measured curves for both cases. This is reasonable since the equivalent mutual inductance is extracted based on the measured crosstalk. The simulated curves have 0–5 dB difference from the measured and calculated curves. This difference is acceptable considering the crosstalk ranges from –45 to –85 dB. The difference could be due to small errors of HFSS modeling or the measurement. For victim trace 1, the comparison result is similar to that of victim trace 2. Due to the limited space, the comparison figures are not shown here.

Based on (12), M_{eq} can be further reduced by increasing the mutual inductance *M* between the guard ring and the clock trace. In Fig. 9, reducing the distance between the guard ring and the clock trace can increase *M*. It can therefore further improve the performance of a guard ring. Further simulations and experiments show that when the distance between the guard ring and the clock trace reduces from 0.23 to 0.13 mm, the performance of the guard ring can be further improved by 3 dB (a 30% M_{eq} reduction).

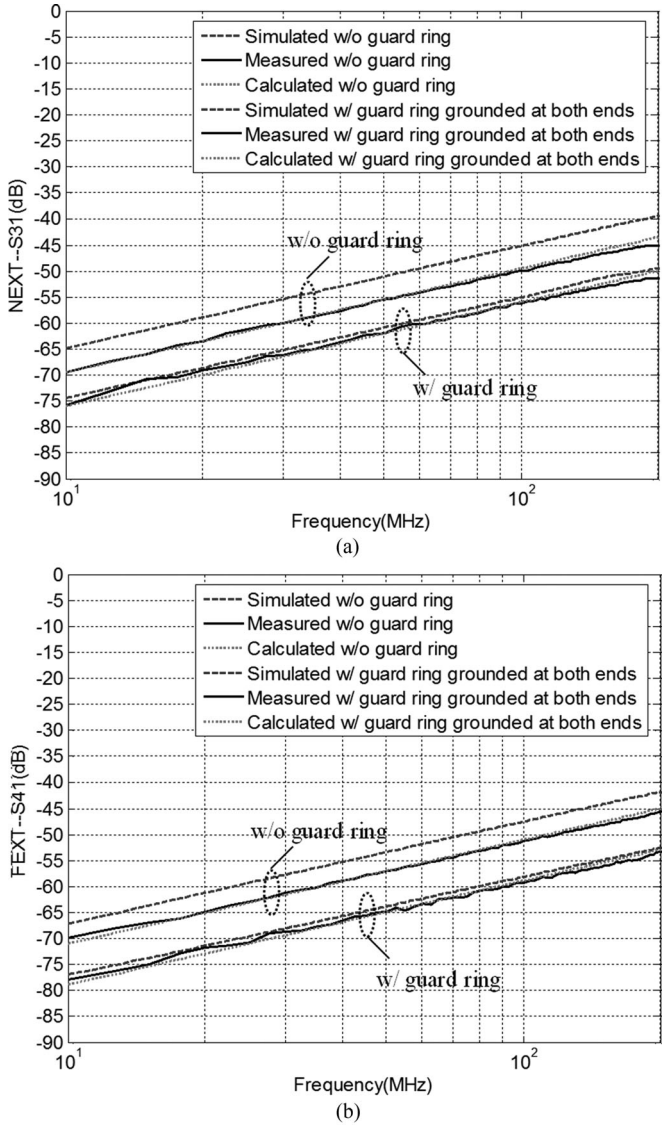

Fig. 19. Comparison of the simulated, measured and calculated crosstalk curves for victim trace 2 with guard ring grounded at two ends and without guard ring: (a) NEXT and (b) FEXT.

V. Conclusion

This paper develops a lumped circuit model for the guard ring of a clock trace for the frequencies at which the dimensions of PCB traces are smaller than 5% of the wavelength. Based on the model, it was found that the guard ring can shield both near electric and near magnetic fields. The paper analyzes the principle of magnetic field shielding in detail. It is found that the best grounding pattern for a guard ring within the concerned frequency range from 10 to 200 MHz in this paper is to ground it at its two ends. Adding more grounding points to the guard ring may not improve its performance. Increasing the mutual inductance between clock trace and the guard ring or reducing the impedance of the guard ring can further improve the performance of the guard ring. The simulated E-H field distributions and crosstalk in HFSS, and the measured crosstalk with a network analyzer for different cases validate the theoretical analysis and the proposed technique of improving the performance of a guard ring.

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