BL0939 datasheet

BL0939 Calibration-free Metrology Chip Data Sheet

Release Notes

Versions	Date	Content	Revisionist
V1.0	2018/06/07	Create	Kang Liao, HCJ
V1.1	2019/12/25	Errata	Kang Liao, HCJ
V1.2	2020/9/7	Errata	Kang Liao, HCJ

Catalog

1 Product Briefing

1.1 Function Introduction

BL0939 is a built-in clock calibration-free power metering chip, suitable for single-phase multi-functional power meters, smart sockets, smart appliances, electric bicycle charging posts and other applications, with high cost performance.

The BL0939 integrates a 3-channel high precision Sigma-Delta ADC to measure 2 currents and 1 voltage simultaneously.

BL0939 can measure current, voltage RMS, active power, active energy and other parameters, can output fast current RMS (for leakage monitoring or overcurrent protection), as well as temperature detection, waveform output and other functions, through the UART/SPI interface output data, can fully meet the smart socket, smart home appliances, single-phase multi-functional power meter, electric bicycle charging pile and electricity information big data It can fully meet the needs of smart socket, smart home appliance, single-phase multifunctional power meter, electric bicycle charging pile and big data collection of electricity consumption information.

BL0939 has a patented anti-submarine design, with reasonable external hardware design, can ensure that the noise power is not counted in the power pulse when there is no current.

1.2 Main features

- Three independent Sigma-Delta ADCs for measuring two currents and one voltage.
- Current RMS range (10mA~35A) @1mohm
- Active power (1w~7700w)@1mohm@220V
- Can output current, voltage RMS, fast current RMS, active power, current and voltage waveform phase angle
- Batch factory gain error less than 1%, peripheral components to meet certain conditions can be free of calibration
- Both current channels are equipped with leakage/overcurrent monitoring function, monitoring threshold and response time can be set
- Voltage over zero signal output
- Built-in waveform register for outputting waveform data for load type analysis
- Integrated temperature sensor to meet the product itself over-temperature monitoring, high

current node preset temperature alarm, ambient temperature measurement and other needs

- Integrated SPI (Encapsulation) Fastest rate support 900KHz)/UART (4800bps) communication method, UART supports multi-chip communication with address (SSOP20L)
- Internal power down monitoring, when it falls below 2.7V, the chip enters reset state.
- Built-in 1.218V reference voltage source
- Built-in oscillation circuit, clock approximately 4MHz
- Chip single operating power supply 3.3V, low power consumption 10mW (typical)
- SSOP20L/SOP16L package

1.3 System Block Diagram

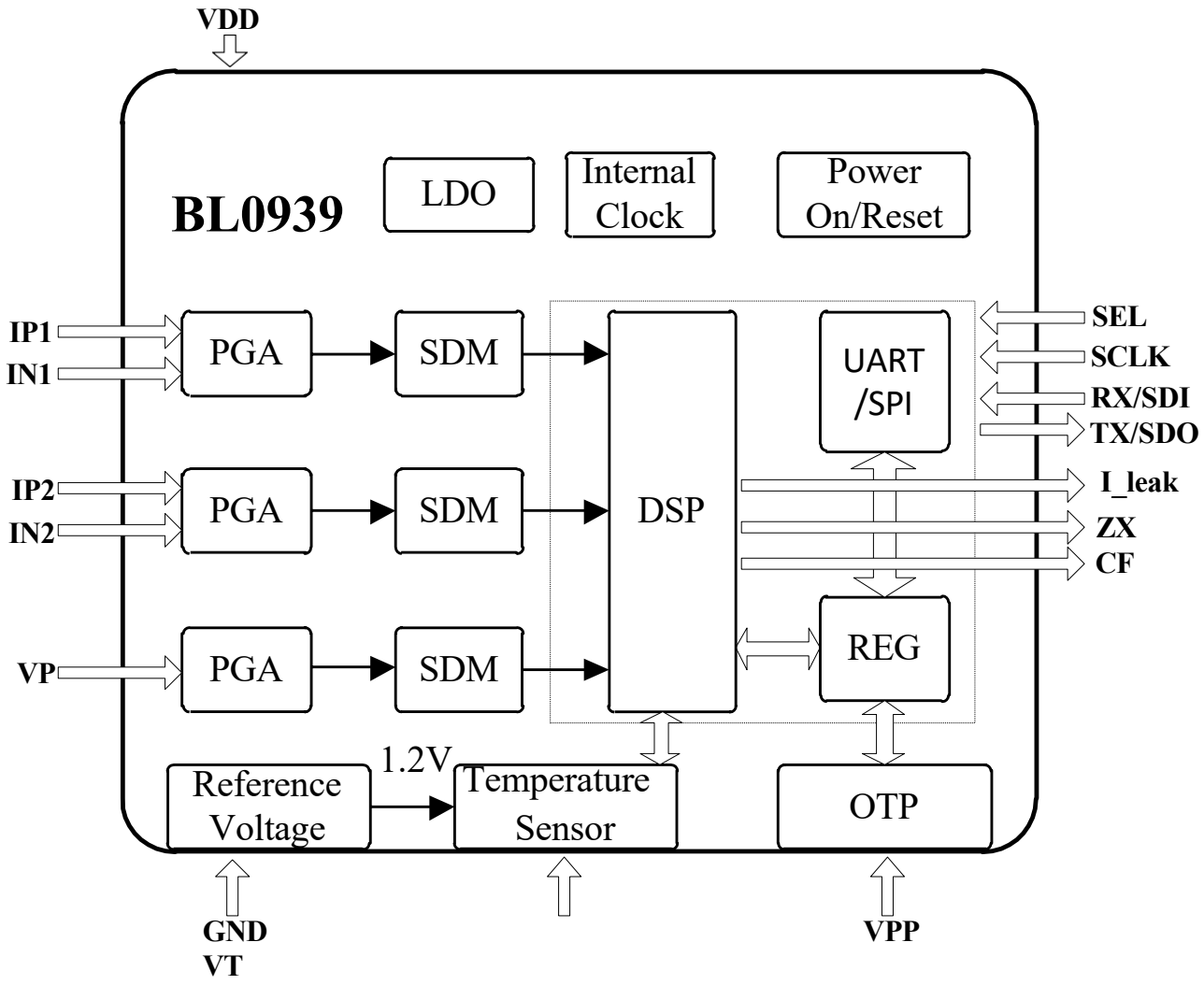
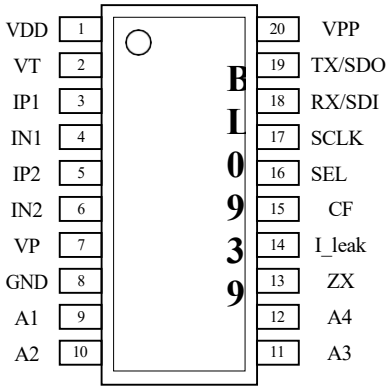


Figure 1

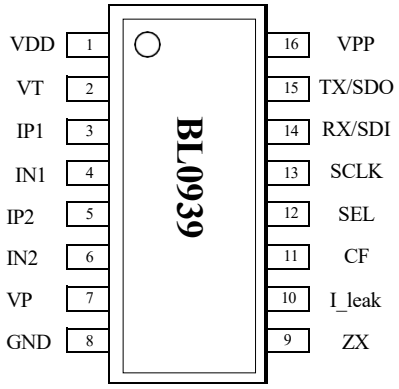
1.4 Package and Pin Description

BL0939 is available in two packages.



SSOP20L

Figure 2



SOP16L

Figure 3

Pin Description (SSOP20L)

Pin No.	Symbols	Description
1	VDD	Power supply (+3.3V)
2	VT	External temperature sensor signal input
3,4	IP1,IN1	Analog input for current A channel, maximum differential voltage of pin ±50mV (35mV rms)
5,6	IP2,IN2	Analog input for current B channel, maximum differential voltage of pin ±50mV (35mV rms)
7	VP	Voltage signal positive input, maximum differential voltage ±100mV (70mV rms)
8	GND	Chip Land
9	A1	UART multi-chip communication mode, used to set the address of the chip, A4/A3/A2/A1 binary code (0000~1111), can set the address 0~15; there is a pull-down resistor inside the pin, hanging is 0 level, the pin is directly connected to VDD is high level. Matching with the device address in UART communication protocol
10	A2	
11	A3	
12	A4	
13	ZX	Voltage over zero indication
14	I_leak	Leakage/overcurrent alarm output for current B channel
15	CF	Electrical energy pulse output, multiplexing function see MODE register description

16	SEL	UART/SPI communication mode selection (0: UART 1: SPI) with internal pull-down resistor 0 level (UART) if overhung, high level (SPI) if the pin is connected directly to VDD
17	SCLK	SPI mode clock input; in UART communication mode, just dangle
18	RX/SDI	UART/SPI multiplexed pins, UART RX/SPI DIN
19	TX/SDO	UART/SPI multiplexing pin, UART TX/SPI DOUT, external pull-up resistor required
20	VPP	Retain, just suspend

Pin Description (SOP16L)

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7	VP	Voltage signal positive input, maximum differential voltage ±100mV (70mV rms)
8	GND	Chip Land
9	ZX	Voltage over zero indication
10	I_leak	Leakage/overcurrent alarm output for current B channel
11	CF	Electrical energy pulse output, multiplexing function see MODE register description
12	SEL	UART/SPI communication mode selection (0: UART 1: SPI) with internal pull-down resistor 0 level (UART) if left open, high level (SPI) if the pin is connected directly to VDD
13	SCLK	SPI clock input, UART communication mode, dangling
14	RX/SDI	UART/SPI multiplexed pins, UART RX/SPI DIN
15	TX/SDO	UART/SPI multiplexing pin, UART TX/SPI DOUT, external pull-up resistor required
16	VPP	Retain, just suspend

1.5 Register List

Address	Name	External Read/ Write	Internal Read/ Write	Bit width	Default Value	Description
Electrical Parameter Register (read-only)						
0x00	IA_FAST_RMS	R	W	24	0x000000	A-Channel Fast RMS, unsigned
0x01	IA_WAVE	R	W	20	0x000000	A channel current waveform register with sign
0x02	IB_WAVE	R	W	20	0x000000	B-channel current waveform register with sign
0x03	V_WAVE	R	W	20	0x000000	Voltage waveform register with sign
0x04	IA_RMS	R	W	24	0x000000	A-channel current RMS register, unsigned
0x05	IB_RMS	R	W	24	0x000000	B-channel current RMS register, unsigned
0x06	V_RMS	R	W	24	0x000000	Voltage RMS register, unsigned
0x07	IB_FAST_RMS	R	W	24	0x000000	B-Channel Fast RMS, unsigned
0x08	A_WATT	R	W	24	0x000000	A-channel active power register, signed
0x09	B_WATT	R	W	24	0x000000	B-channel active power register, signed
0x0A	CFA_CNT	R	W	24	0x000000	A-channel active energy pulse counting, unsigned
0x0B	CFB_CNT	R	W	24	0x000000	B-channel active energy pulse counting, unsigned
0x0C	A_CORNER	R	W	16	0x0000	A channel current and voltage waveform phase angle register
0x0D	B_CORNER	R	W	16	0x0000	B-channel current and voltage waveform phase angle register
0x0E	TPS1	R	W	10	0x000	Internal temperature detection register, unsigned
0x0F	TPS2	R	W	10	0x000	External temperature detection register, unsigned
User operation registers (read and write)						
0x10	IA_FAST_RMS_CTRL	R/W	R	16	0xFFFF	A-Channel Fast RMS Control Register
0x13	IA_RMSOS	R/W	R	8	0x00	Current A channel RMS small signal correction register
0x14	IB_RMSOS	R/W	R	8	0x00	Current B channel RMS small signal

						correction register
0x15	A_WATTOS	R/W	R	8	0x00	A-channel active power small signal correction register
0x16	B_WATTOS	R/W	R	8	0x00	B-channel active power small signal correction register
0x17	WA_CREEP	R/W	R	8	0x0B	Active power anti-submarine register
0x18	MODE	R/W	R	16	0x0000	User mode selection register
0x19	SOFT_RESET	R/W	R	24	0x000000	Reset the user area register when writing to 0x5A5A5A
0x1A	USR_WRPROT	R/W	R	8	0x00	User write protect setting register. After writing to 0x55, use the The user operation register can be written; write other values, the user operation register area is not writable
0x1B	TPS_CTRL	R/W	R	16	0x07FF	Temperature mode control register
0x1C	TPS2_A	R/W	R	8	0x0000	External temperature sensor gain coefficient correction register
0x1D	TPS2_B	R/W	R	8	0x0000	External temperature sensor offset coefficient correction register
0x1E	IB_FAST_RMS _CTRL	R/W	R	16	0xFFFF	B-Channel Fast RMS Control Register

1.6 Special Register Description

1.6.1 User mode selection register

0x18	MODE	Operating mode register		
No.	name	default value	description	
[7:0]	reserved	0b00000000	Reserved	
8	RMS_UPDATE_SEL	0b0	Valid value register refresh time selection Select	0: 400ms 1: 800ms
9	AC_FREQ_SEL	0b0	AC frequency selection	0: 50 Hz 1: 60Hz
10	reserved	0b0	Reserved	
11	CF_SEL	0b0	CF pin output power pulse selection	0: A channel 1: B-channel
12	CF_UNABLE	0b0	CF pin output function selection	0: Electrical energy pulse, MODE [11] Configuration valid 1: Alarm function, TPS_CTRL[14] is configured with Effect
[15:13]	reserved	0b000	Reserved	

1.6.2 Temperature mode control register

0x1B	TPS_CTRL	Temperature mode control register		
No.	name	default value	description	
0x1B	TPS_CTRL	0x07FF	[15] Temperature measurement switch, default 0b0,on Start temperature measurement	0: Open
				1: Close
			[14] Alarm switch, default 0b0,	0: Temperature alarm on
				1: Current A channel overcurrent/leakage alarm Police On
			[13:12] Temperature measurement selection, default 0b00 automatic temperature measurement	00: Automatic temperature measurement
				01: Same as 00
				10: Internal temperature measurement
				11: External temperature measurement
			[11:10] Temperature measurement time interval selection, default 0b01 100ms	00:50ms
				01: 100ms
				10: 200ms
				11: 400ms
			[9:0] External temperature measurement alarm threshold setting The default setting is 0x3FF, no alarm.	TPS2 register value is greater than or equal to report Alarm value, generate alarm

1.7 Performance Indicators

1.7.1 Electrical parameters performance

(VDD = 3.3V, GND = 0V, on-chip reference voltage source, built-in crystal, 25° C, electrical energy measured via CF output)

Measurement items	Symbols	Measurement conditions	Minimum	Typical	Maximum	Unit
Power supply VDD	VDD		3.0		3.6	V
Power consumption	Iop	VDD=3.3V		3		mA
Measurement Range		4000:1 input motion State Range				
Active energy measurement accuracy (Big Signal)		35A~100mA Input Input @ 1mohm sampling resistance		0.2		%
Active energy measurement accuracy (small signal)		100mA~50mA input @ 1mohm sampling Resistance		0.4		%
Active energy measurement accuracy (tiny signal)		50mA~10mA Input Input @ 1mohm sampling resistance		0.6		%
RMS measurement accuracy (Big Signal)		35A~100mA input @ 1mohm sampling Resistance		0.2		%
RMS measurement accuracy (small signal)		100mA~50mA input @ 1mohm sampling Resistance		2		%
RMS measurement accuracy (tiny signal)		50mA~10mA input @ 1mohm sampling Resistance		6		%

Fast RMS response time	50Hz	Can be set to circumferential/ Semi-Circular Wave	10		40	mS
	60Hz		8.3		33	mS
Over-zero signal output delay				571		uS
Measurement error due to phase angle between channels Difference (capacitive)	PF08err	Phase overrun 37 (PF=0.8)			0.5	%
Measurement error due to phase angle between channels Poor (perceptual)	PF05err	Phase lag 60 (PF=0.5)			0.5	%
AC power supply rejection (output frequency) (rate range change)	ACPSRR	IP/N=100mV			0.1	%
DC power supply rejection (output frequency) (rate range change)	DCPSRR	VP/N=100mV			0.1	%

Measurement items	Symbols	Measurement conditions	Minimum	Typical	Maximum	Unit
Analog input level (current)		Current differential input (peak)			50	mV
Analog input level (voltage)		Voltage differential input (peak)			200	mV
Analog Input Impedance				370		kΩ
SEL Pull-down resistor		SEL (drop down)		56.9		kΩ
Analog input bandwidth		(-3dB)		3.5		kHz
Internal voltage reference	Vref			1.218		V
Logic input high		VDD=3.3V±5%	2.6			V
Logic input low		VDD=3.3V±5%			0.8	V
Logic output high		VDD=3.3V±5% IOH=5mA	VDD-0.5			V
Logic output low		VDD=3.3V±5% IOL=5mA			0.5	V

1.7.2 Limit range

(T = 25 ° C)

Projects	Symbols	Extreme values	Unit
Supply Voltage VDD	VDD	-0.3 ~ +4	V
Analog input voltage (with respect to GND)	IP1, IP2, VP	-4 ~ +4	V
Digital input voltage (with respect to GND)	A1~A4, UART_SEL, RX/SDI	-0.3 ~ VDD+0.3	V
Digital output voltage (with respect to GND)	CF, I_Leak, TX/SDO	-0.3 ~ VDD+0.3	V
Operating temperature	Topr	-40 ~ +105	℃
Storage temperature	Tstr	-55 ~ +150	℃

2 Function Description

BL0939 is mainly divided into two blocks: analog signal processing and digital signal processing. The analog part mainly includes three-channel PGA, three-channel Sigma-Delta ADC, internal clock, power on/reset, temperature sensor, LDO and other related modules. The digital part is the digital signal processing module (DSP).

2.1 Current and voltage transient waveform measurement

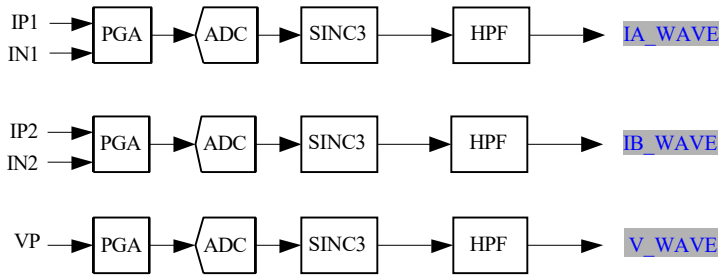


Figure 4

As shown in the figure above, two currents and one voltage are passed through the analog module amplifier (PGA) and high precision analog-to-digital conversion (ADC) to get three 1bit PDMs to the digital module, which passes through the downsampling filter (SINC3), high-pass filter (HPF), channel bias correction and other modules to get the required current waveform data and voltage waveform data (IA_WAVE, IB_WAVE, V_WAVE). IB_WAVE, V_WAVE).

The BL0939 has three high-precision ADCs with double-ended differential signal inputs for current: A current channel IP1/IN1, B current channel IP2/IN2, voltage channel VP.

The acquired load current and voltage waveform data are updated at a rate of 7.8k, and each sample data is a 24bit signed number and stored in the waveform registers (IA_WAVE, IB_WAVE, V_WAVE) respectively. The SPI rate configuration is greater than 375Kbps, and the waveform value of one channel can be read continuously.

Note: register is 24bit, insufficient bits, high bits are zeroed.

Address	Name	External Read/write	Internal Read/write	Bit width	Default Value	Description
0x01	IA_WAVE	R	W	24	0x000000	A-channel current waveform register
0x02	IB_WAVE	R	W	24	0x000000	B-channel current waveform register
0x03	V_WAVE	R	W	24	0x000000	Voltage waveform register

2.2 Active power

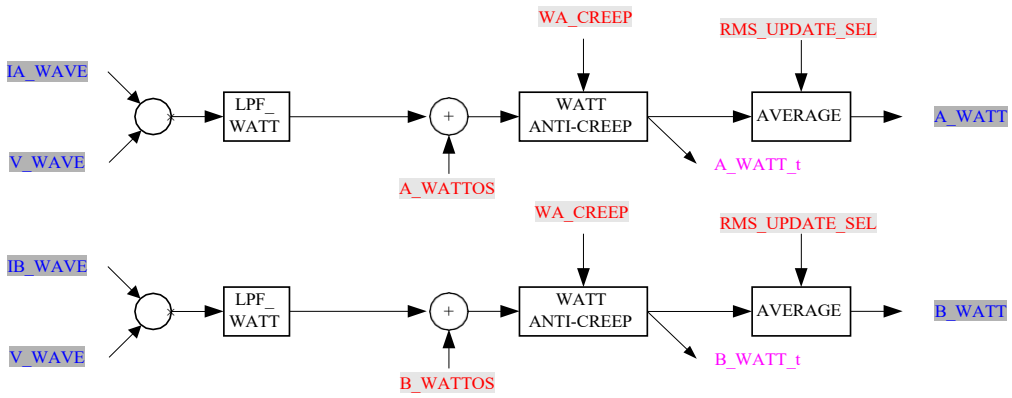


Figure 5

Address	Name	External Read/Write	Internal Read/Write	Bit width	Default Value	Description
0x08	A_WATT	R	W	24	0x000000	A channel active register
0x09	B_WATT	R	W	24	0x000000	B Channel active register

Active power calculation formula: $\frac{4046*I(A)*V(V)*\mathrm{Cos}(\varphi)}{Vref2}$

A/B_WATT =

where $I(A)$, $V(V)$ is the rms value of the channel pin input signal (mV), φ is the phase angle of the I(A), V(V) AC signal, and Vref is the built-in reference voltage with a typical value of 1.218V.

These two registers indicate whether the current active power is positive or negative, Bit[23] is the sign bit, Bit[23]=0, the current power is positive, Bit[23]=1, the current power is negative, in the form of complementary code.

2.3 Active power bias calibration

The BL0939 contains two 8-bit active power bias correction registers (A_WATTOS, B_WATTOS) with a default value of 00H. They remove the active power bias during power metering with data in the form of 2's complement, Bit [7] being the sign bit. The deviations here may originate from board-level noise or crosstalk. The deviation correction allows the value in the active power register to approach 0 in the absence of load.

Address	Name	External Read/write	Internal Read/write	Bit width	Default Value	Description
0x15	A_WATTOS	R/W	R	8	0x00	A-channel power small signal correction register
0x16	B_WATTOS	R/W	R	8	0x00	B-channel power small signal correction register

$$WATTOS = \frac{WATT - WATT0}{8 \times 3.05172}$$

WATT is the active power after correction and WATT0 is the active power before correction.

2.4 Anti-submergence of active power

BL0939 has a patented power anti-submarine function to ensure that the board-level noise power will not accumulate power when there is no current input.

The active anti-submarine threshold register (WA_CREEP) is an 8bit unsigned number, default is 0BH. This value corresponds to the active power register value as shown in the following equation. accumulate.

Address	Name	External Read/Write	Internal Read/Write	Bit width	Default Value	Description
0x17	WA_CREEP	R/W	R	8	0x0B	Active power anti-submarine register

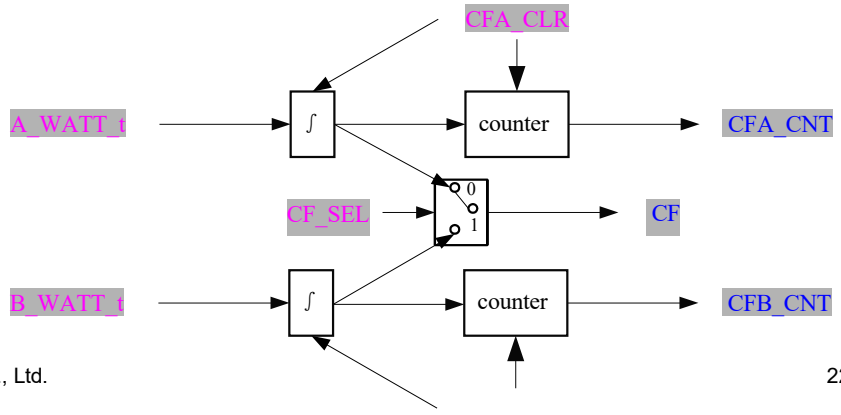
WA_CREEP can be set according to the value of power register A_WATT/B_WATT, their correspondence

$$WA\_CREEP = \frac{WATT}{3.0517578125*8}$$

Note: When the channel is in the anti-submarine state, the current RMS value of the channel is not measured and is also cut to 0.

2.5 Electricity metering

BL0939 provides two channels of electrical energy pulse metering, two channels of active instantaneous power by time integration, can obtain active electrical energy, proportional to the output check pulse CF, CFA_CNT and CFB_CNT registers to store the number of output electrical energy pulse CF, as shown in the figure below.



CFB_CLR

Figure 6

0x18	MODE	Operating mode register	
No.	name	default value	description
10	reserved	0b0	Reserved
11	CF_SEL	0b0	CF pin output power pulse pass Road selection 0: A channel 1: B channel
12	CF_UNABLE	0b0	CF Pin Output Selection 0: Electrical energy pulse MODE[11] configuration is valid 1: Temperature measurement/leakage alarm TPS [14] configuration is valid

First set MODE[12]=0 to select CF pin output power pulse, then set MODE[11] to select output power pulse of A channel or B channel.

Address	Name	External Read/Write	Internal Read/Write	Bit width	Default Value	Description
0x0A	CFA_CNT	R	W	24	0x000000	A-channel active energy pulse counting, unsigned
0x0B	CFB_CNT	R	W	24	0x000000	B-channel active energy pulse counting, unsigned

The active power pulse count corresponds to the power consumption, and the results are stored in two registers, CFA_CNT and CFB_CNT respectively, or the number of pulses can be counted directly from the CF pin through I/O interrupt.

Note: CFA_CNT and CFB_CNT registers are the algebraic and cumulative way of power pulses, i.e. positive work plus, negative work minus.

Cumulative time of each CF pulse $tCF=\frac{1638.4*256}{WATT}$

where WATT is the corresponding active power register value (A_WATT, B_WATT).

2.6 Current and voltage RMS

The RMS values of the three channels, as shown in the figure below, are squared (X^2), low-pass filtered (LPF_RMS), and open-rooted (ROOT) to obtain the instantaneous value of the RMS_t, and then averaged to obtain the average value of the three channels (A_RMS, B_RMS, and V_RMS).

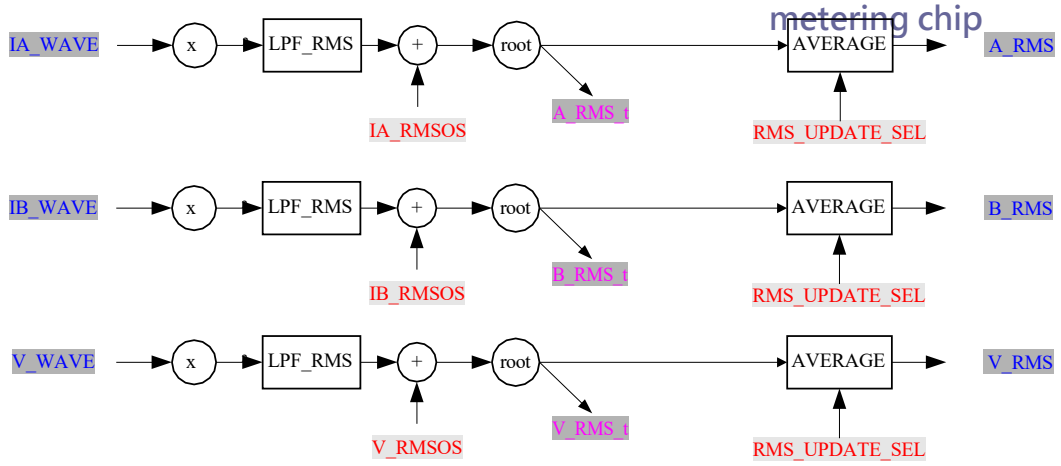


Figure 7

Address	Name	External Read/Write	Internal Read/Write	Bit width	Default Value	Description
0x04	IA_RMS	R	W	24	0x000000	A-channel current RMS register, unsigned
0x05	IB_RMS	R	W	24	0x000000	B-channel current RMS register, unsigned
0x06	V_RMS	R	W	24	0x000000	Voltage RMS register, unsigned

0x18	MODE	Operating mode register		
No.	name	default value	description	
8	RMS_UPDATE_SEL	0b0	Valid value update speed selection	0: 400ms
				1: 800ms

Set MODE[8].RMS_UPDAT_SEL to choose the RMS average refresh time to 400ms or 800ms, default 400ms. when a current channel is in anti-submarine state, the RMS value of this current channel is zero.

Current RMS conversion formula: $\frac{324004*I(A)}{Vref}$
IA/B_RMS =

Voltage RMS conversion formula: V_RMS = $\frac{79931*V(V)}{Vref}$

Vref is the reference voltage and the typical value is 1.218V.

Note: **I(A)** is the input signal **(mV)** between **IP1, IN1 pins** and **V(V)** is the input signal **(mV)** of **VP** pin.

2.7 Current-voltage RMS bias calibration

The BL0939 contains two 8-bit rms bias registers (IA_RMSOS and IB_RMSOS) with a default value of 00H, which adjust for deviations in the rms calculation with data in the form of 2's complement. Such deviations may originate from input noise. The deviation correction allows the value in the rms register to be close to 0 without load.

Address	Name	External Read/Write	Internal Read/Write	Bit width	Default Value	Description
0x13	IA_RMSOS	R/W	R	8	0x00	IA Current RMS small signal correction register
0x14	IB_RMSOS	R/W	R	8	0x00	IB Current RMS Small Signal Correction Register

Calibration formula: $RMSOS = \frac{RMS2-RMS02}{9.3132\times 2^{15}}$

Here RMS0 is the valid value before correction and RMS is the valid value after correction.

2.8 Leakage/overcurrent detection

Both BL0939 A and B channels have fast RMS registers to detect half-periodic or periodical RMS values. This function can be used for leakage or overcurrent detection. The source of the leakage waveform I_WAVE is shown in the block diagram of channel waveform. IA/IB_WAVE_F takes the absolute value and then performs half-periodic or periodical time accumulation, which is selected by FAST_RMS_CTRL[15], and the default value 1 selects periodical accumulation with a maximum response time of 40ms (50Hz) or 33mS (60Hz), note that the x_FAST_RMS register jumps more when the half-cycle is totalized. To distinguish between 50 Hz and 60 Hz half-cycle times (AC_FREQ_SEL).

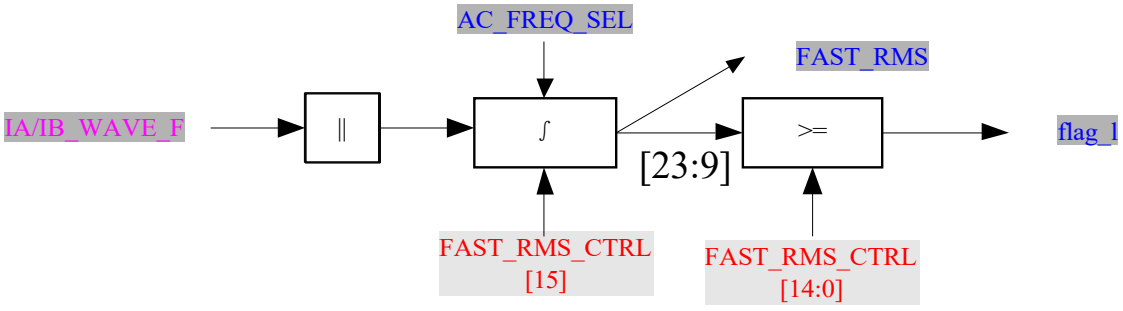


Figure 8

Address	Name	External	Internal	Bit width	Default Value	Description
		Read/Write	Read/Write			
0x10	IA_FAST_RMS_CTRL	R/W	R	16	0xFFFF	A-Channel Fast RMS Control Register
0x1E	IB_FAST_RMS_CTRL	R/W	R	16	0xFFFF	B-Channel Fast RMS Control Register

The two Fast RMS control registers, IA_FAST_RMS_CTRL and IB_FAST_RMS_CTRL, allow you to select the refresh time as half-cycle or cycle and set the fast rms threshold (i.e., leakage or overcurrent threshold).

		Channel Fast RMS Register		
No.	name	default value	description	
0x10	IA_FAST_RMS_CTRL	0xFFFF	[15] A-Channel Fast RMS Register Refresh Time	0: Half-perimeter wave
				1: Zhou Bo
			[14:0] A Channel Fast RMS Threshold	
0x1E	IB_FAST_RMS_CTRL	0xFFFF	[15] B-Channel Fast RMS Register Refresh Time	0: Half-perimeter wave
				1: Zhou Bo
			[14:0] B-Channel Fast RMS Threshold	

0x18	MODE	Operating mode register		
No.	name	default value	description	
9	AC_FREQ_SEL	0b0	AC frequency selection	0: 50 Hz
				1: 60Hz

Set the AC frequency via MODE [9].

Address	Name	External	Internal	position wide	Default Value	Description
		Read/Write	Read/Write			
0x00	IA_FAST_RMS	R	W	24	0x000000	A-Channel Fast RMS, unsigned
0x07	IB_FAST_RMS	R	W	24	0x000000	B-Channel Fast RMS, unsigned

The 24-bit unsigned fast rms register is refreshed according to the circumference or half circumference, and the Bit[23:9] of the FAST_RMS register is compared with the leakage/overcurrent threshold FAST_RMS_CTRL [14:0], if it is greater than or equal to the set threshold, the leakage/overcurrent alarm output indicator pin outputs high.

The B channel leakage/overcurrent alarm output indication pin is I_leak, which can be output directly without configuration.

A channel leakage/overcurrent alarm output indication pin is CF, you need to set MODE[12]=1 first, then set TPS_CTRL[14]=1.

0x18	MODE	Operating mode register		
No.	name	default value	description	
12	CF_UNABLE	0b0	CF Pin Output Selection	0: Electrical energy pulse MODE[11] configuration is valid
				1: Temperature measurement/leakage alarm TPS [14] configuration is valid

0x1B	TPS_CTRL	Temperature mode control register		
No.	name	default value	description	
14	ALERT_CTRL	0b0	Alarm switch	0: Temperature alarm on 1: Current A channel overcurrent/leakage alarm on

The response time of I_leak is up to 2 cycles or 2 half cycles because the fast RMS value is updated on a weekly or semi-periodic basis.

2.9 Phase angle calculation

The BL0939 can be used for phase angle measurements, with the phase angle between the current and voltage of each of the two A/B phases CORNER_A/ CORNER_B indicating the reactive quadrant. The calculation is obtained by the difference of the forward crossing time of the current and voltage, which is updated to the registers CORNER_A/ CORNER_B, respectively, when the current is forward crossing, each register is a 16-bit unsigned number.

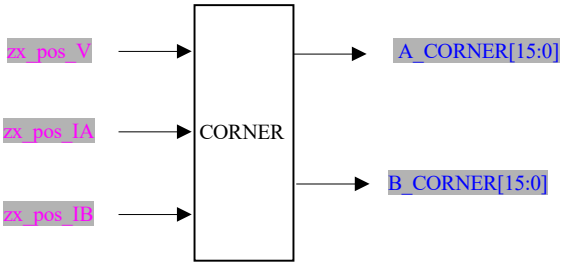


Figure 9

Address	Name	External Read/Write	Internal Read/Write	Bit width	Default Value	Description
0x0C	A_CORNER	R	W	16	0x0000	A channel current and voltage waveform phase angle register
0x0D	B_CORNER	R	W	16	0x0000	B-channel current and voltage waveform phase angle register

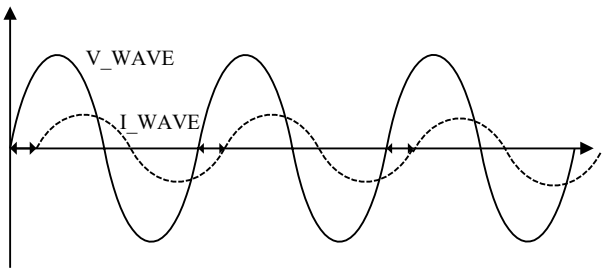


Figure 10

Phase angle conversion formula: Unit is radian

$$\frac{2*pi*A/B\ CORNER*fc}{f0}$$

Where, f_c is the measurement frequency of the AC signal source, default is 50Hz, and f_0 is the sampling frequency, typical value is 1MHz.

2.10 Over-zero detection

The BL0939 provides voltage over-zero detection, and the over-zero signal is output directly from pin ZX. A ZX of zero indicates a positive half-cycle of the waveform, and a ZX of 1 indicates a negative half-cycle of the waveform. The time delay with the actual input signal is 570us.

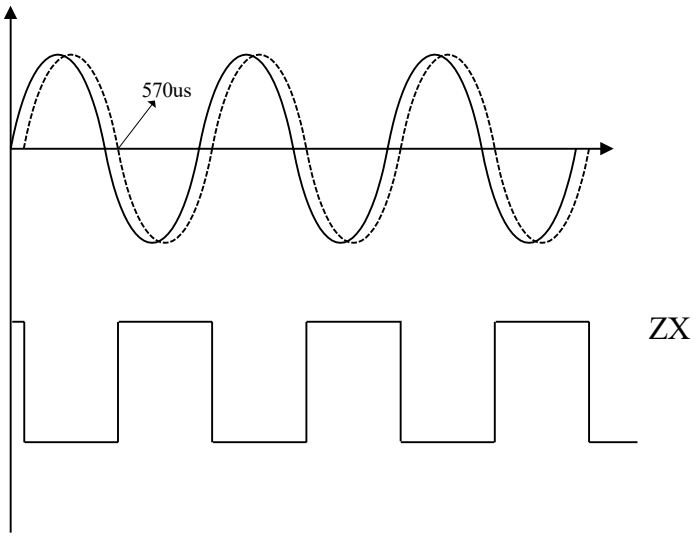


Figure 11

2.11 Temperature measurement

BL0939 provides internal temperature measurement and off-chip temperature measurement.

When external temperature measurement, optional output alarm indication, when the alarm function is turned on, CF pin can be multiplexed to output alarm signal, when TPS2 is greater than or equal to the alarm threshold value, CF pin outputs high level, temperature indication alarm. Exit the alarm indication when the temperature value is lower than the alarm value or when the alarm function is turned off.

0x1B	TPS_CTRL	Temperature mode control register		
No.	name	default value	description	
0x1B	TPS_CTRL	0x07FF	[15] Temperature measurement switch, default 0b0, on Start temperature measurement	0: Open
				1: Close
			[14] Alarm switch, default 0b0,	0: Temperature alarm on
				1: Current A channel overcurrent/ Leakage alarm on
			[13:12] Temperature measurement selection, default 0b00 automatic temperature measurement	00: Automatic temperature measurement
				01: Same as 00
				10: Internal temperature measurement
				11: External temperature measurement
			[11:10] Temperature measurement time interval selection, default 0b01 100ms	00:50ms
				01: 100ms
				10: 200ms
				11: 400ms
			[9:0] External temperature measurement alarm threshold setting The default setting is 0x3FF.	

First set MODE[12]=1, then set TPS_CTRL[14]=0 to enable the CF pin to output external

temperature alarm indication.

0x18	MODE	Operating mode register		
No.	name	default value	description	
12	CF_UNABLE	0b0	CF Pin Output Selection	0: Electrical energy pulse MODE[11] configuration is valid
				1: Temperature measurement alarm TPS [14] configuration is valid

The external and internal temperature readings are stored in two registers, TPS1 and TPS2, respectively.

Address	Name	External	Internal	Bit width	Default Value	Description
		Read/Write	Read/ Write			
0x0E	TPS1	R	W	10	0x0000	Internal temperature value register, unsigned
0x0F	TPS2	R	W	10	0x0000	External temperature value register, unsigned

Internal temperature measurement formula: Tx=(170/448)(TB/2-32)-45

TB is the TPS1 register value.

The external test temperature uses a SAR ADC with a maximum input signal of 0.55*VDD (V) on the VT pin and the TPS2 register value is the corresponding AD Sampling value, full scale 1024.

Address	Name	External Read/write	Internal Read/write	Bit width	Default Value	Description
0x1C	TPS2_A	R/W	R	8	0x00	External temperature sensor gain coefficient A calibration register
0x1D	TPS2_B	R/W	R	8	0x00	External Temperature Sensor Bias Factor B Calibration Register

3 Communication Interface

The register data is sent by 3 bytes (24 bits). If the register data is less than 3 bytes, the unused bits are complemented by 0 to make up the full 3 bytes.

3.1 SPI

- Selected via pin UART_SEL, multiplexed with UART
- From the model
- Half-duplex communication, communication rate can be matched, maximum communication rate 900khz
- 8-bit data transfer, MSB first, LSB second
- Fixed one clock polarity/phase (CPOL=0, CPHA=1)

3.1.1 Working mode

The master device works in Mode1: CPOL=0, CPHA=1, i.e. when idle state, SCLK is at low level, data sending is at the 1st edge, i.e. SCLK jumps from low level to high level, so data sampling is at falling edge and data sending is at rising edge.

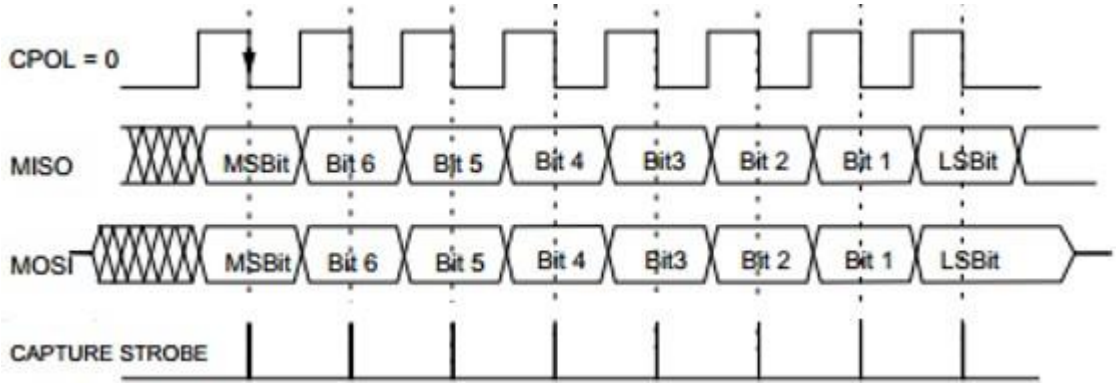


Figure 12

3.1.2 Frame Structure

In communication mode, the 8bit identification byte (0x55) or (0xA5) is sent first, (0x55) is the read operation identification byte and (0xA5) is the write operation identification byte, and then the register address byte is sent to determine the address to access the register (see BL0939 Register List). The following figure shows the data transfer sequence for read

and write operations, respectively. When a frame of data transfer is completed, the BL0939 re-enters communication mode. The number of pulses of SCLK required for each read/write operation is 48 bits.

There are two types of frame structures, each described as follows.

1) Write operation frame

Write operation frame	0xA5	ADDR[7:0]	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

The checksum byte CHECKSUM is((0xA5 + ADDR + DATA_H + DATA_M + DATA_L) & 0xFF) and then inverted by bit. 2) Read operation frame

Read command frame	0x55	ADDR[7:0]

Return Data	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

The checksum byte CHECKSUM is((0x55 + ADDR + DATA_H + DATA_M + DATA_L) & 0xFF) and then inverted by bit. Note: The data is fixed 3 bytes (high byte in front, low byte at the end, if the valid byte of data is less than 3 bytes, the invalid bit is complemented by 0)

3.1.3 Timing of write operations

The serial write sequence is performed in the following manner. The frame identification byte {0xA5} indicates that the data communication operation is to write data, and ADDR is the address of the register to be written to. All remaining bits of the register data are also shifted left at the lower edge of this SCLK (Figure 13).

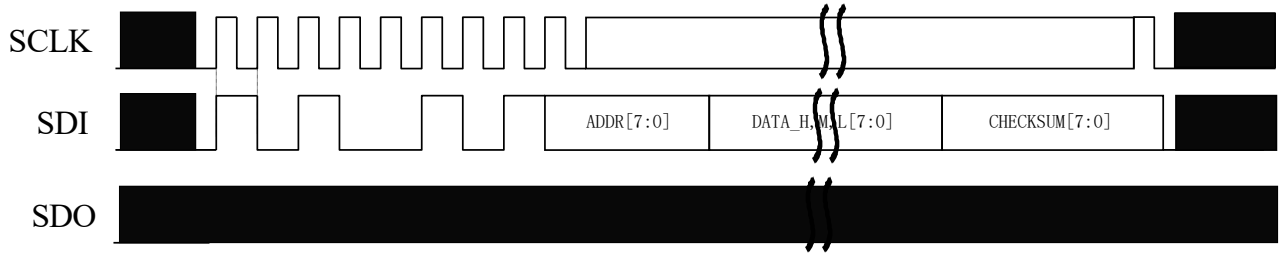


Figure 13

3.1.4 Read Operation Timing

During the data readout operation of the BL0939, on the rising edge of SCLK, the BL0939 shifts the corresponding data out to the SDO logic output pin, and the SDO value remains unchanged for the next time when SCLK is 1, i.e., the external device can sample the SDO value on the next falling edge. The MCU must first send a read command frame during the data readout operation.

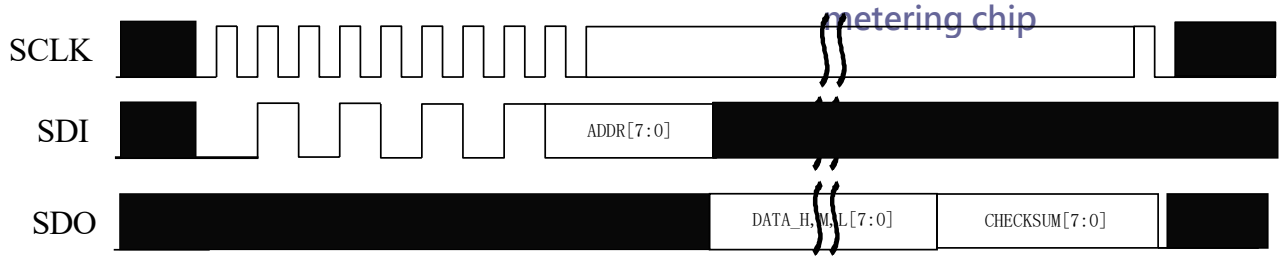


Figure 14

When the BL0939 is in communication mode, the frame identification byte {0x55}, indicates that the data communication operation is reading out data. Then the immediately following byte ADDR is the address of the target register to be read out. the BL0939 starts shifting out the data in the register on the rising edge of SCLK after receiving the register address (Figure 14). All remaining bits of the register data are shifted out on the subsequent rising edge of SCLK. Thus, at the falling edge of SCLK, the external device can sample the SPI output data. Once the readout operation is complete, the serial interface reenters communication mode. At this point, the SDO output enters a high resistance state at the falling edge of the last SCLK signal.

3.1.5 Fault tolerance mechanism for SPI interface

1) The soft reset function of SPI interface can reset the SPI interface individually by sending 6 bytes of 0xFF through SPI interface.

Note: SPI communication does not support chip selection, if you choose 20pin package, you need to connect A4A2 to ground and A3A1 to high level.

3.2 UART

3.2.1 Overview

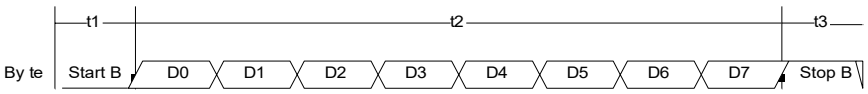
The BL0939 is available with UART communication. the UART interface requires only two low-speed optocouplers for isolated communication. Fixed baud rate 4800bps, N, 8, 1.5, operates in slave mode, half duplex communication.

Both packages with UART communication, 20 pin package with chip select address [A4 A3 A2 A1], can set device address 00~15.

3.2.2 Description

UART port setting: communication baud rate is 4800bps, no parity, stop bit 1.5.

3.2.3 Per Byte Format



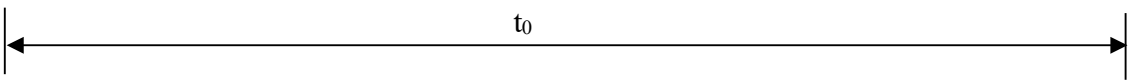
Start bit low duration t1=208us

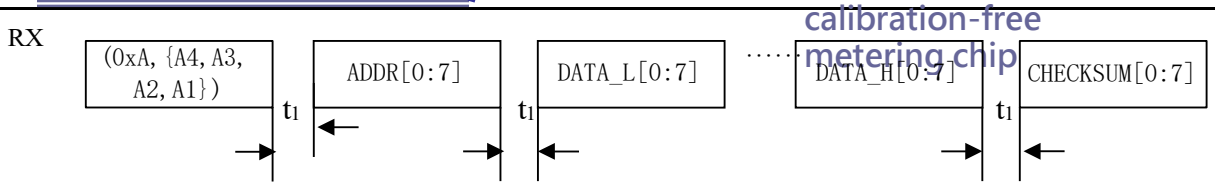
Valid data bit time duration t2=208*8=1664us

Stop bit high duration t3=208us+104us

3.2.4 Write Timing

The host UART write data timing is shown below, the host first sends the command byte (0xA,{A4,A3,A2,A1}), then the register address (ADDR) where the data needs to be written, then sends the data byte in order (low byte before, high byte after, if the data valid byte is less than 3 bytes, the invalid bit is complemented by 0), and finally the checksum byte.





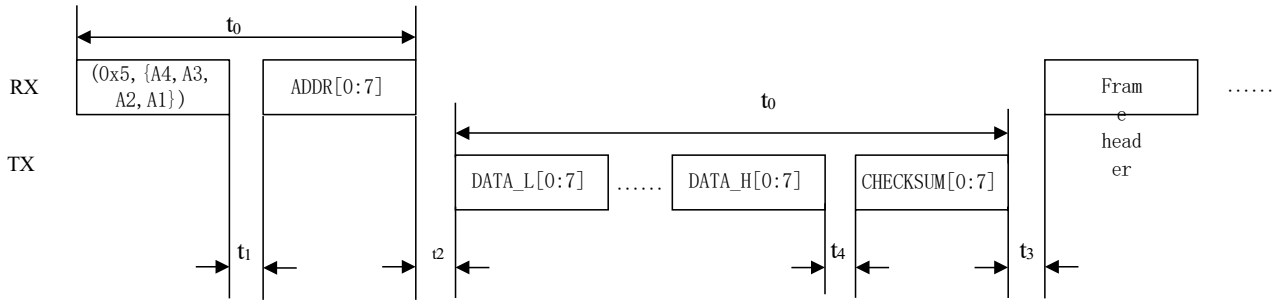
(0xA,{A4,A3,A2,A1}) is the frame identification byte for write operation, if [A4A1]=0101, device address 5, frame identification byte is 0xA5.

ADDR is the internal register address of the BL0939 corresponding to the write operation.

CHECKSUM byte is ((0xA,{A4,A3,A2,A1})+ADDR+Data_L+Data_M+Data_H) & 0xFF) and then inverse by bit. Note: The BL0939-SOP16L device address is 5, i.e. the first byte is 0xA5.

3.2.5 Read Timing

The host UART read data timing is shown below, the host first sends the command byte (0x5,{A4,A3,A2,A1}), then sends the register address (ADDR) to be read, then BL0939 sends the data byte (low byte before, high byte after, if the valid data byte is less than 3 bytes, the invalid bit is complemented by 0), and finally the checksum byte.



(0x5,{A4,A3,A2,A1}) is the frame identification byte of the read operation; if [A4A1]=0101, device address 5, the frame identification byte is 0x55; ADDR is the internal register address of BL0939 corresponding to the read operation.

CHECKSUM bytes as ((0x5,{A4,A3,A2,A1})+ADDR+Data_L+Data_M+Data_H) & 0xFF) and then inverted by bit.

Timing Description

	Description	Min	Type	Max	Unit
t1	MCU interval between sending bytes	0		20	mS
t2	The interval between the end of the MCU transmit register address and the BL0939 transmit byte during the read operation		72		uS

t3	Frame interval time	0.5			uS
t4	BL0939 Interval between sent bytes		116		uS

3.2.6 Packet sending mode

With the command "(0x5,{A4,A3,A2,A1}) + 0xAA", BL0939 returns an all-electric parameter packet. The returned packets are 35

The format is: Packet header (1byte head) Current A Fast RMS (3byte IA_FAST_RMS) Current A RMS (3byte IA_RMS) Current B RMS (3byte IB_RMS) Voltage RMS (3byte V_RMS) Current B Fast RMS (3byte IB_FAST_RMS) A Channel Power Value (3byte A_WATT) B Channel Power Value (3byte B_WATT)

A channel pulse count value (3byte CFA_CNT) B channel pulse count value (3byte CFB_CNT) Internal thermometer measurement value (2byte TPS1 + 1byte 0) External temperature sensor measurement Value (2byte TPS2 + 1byte 0) Checksum value (1byte CHECKSUM)

All-electric parameter package format.

Name	Byte order No.	Content	Name	Byte order No.	Content
Baotou	0	Head (0x55)	B_WATT	19	B_WATT_l
IA_FAST_RMS	1	IA_FAST_RMS_l		20	B_WATT_m
	2	IA_FAST_RMS_m		21	B_WATT_h
	3	IA_FAST_RMS_h	CFA_CNT	22	CFA_CNT_l
IA_RMS	4	IA_RMS_l		23	CFA_CNT_m
	5	IA_RMS_m		24	CFA_CNT_h
	6	IA_RMS_h	CFB_CNT	25	CFB_CNT_l
IB_RMS	7	IB_RMS_l		26	CFB_CNT_m
	8	IB_RMS_m		27	CFB_CNT_h
	9	IB_RMS_h	TPS1	28	TPS1_l
V_RMS	10	V_RMS_l		29	TPS1_m
	11	V_RMS_m		30	0x00
	12	V_RMS_h	TPS2	31	TPS2_l
IB_FAST_RMS	13	IB_FAST_RMS_l		32	TPS2_m
	14	IB_FAST_RMS_m		33	0x00
	15	IB_FAST_RMS_h	checksum	34	checksum
A_WATT	16	A_WATT_l			
	17	A_WATT_m			
	18	A_WATT_h			

checksum=((0x5,{A4,A3,A2,A1}) + 0x55 + data1_l + data1_m + data1_h + ……) & 0xff) and then invert by bit

3.2.7 Protection mechanism for the UART interface

The UART communication of BL0939 provides a timeout protection mechanism, if the interval between bytes exceeds 18.5mS, the UART

The interface is automatically reset.

If the frame identification byte is incorrect or the CHECKSUM byte is incorrect, the frame data is dropped.

UART module reset: The UART module is reset when the RX pin is pulled high after a low level of more than 6.65mS.

4 Order Information

BL0939-X X=SOP16L: SOP16L package

X=SSOP20L: SSOP20L package

5 Package

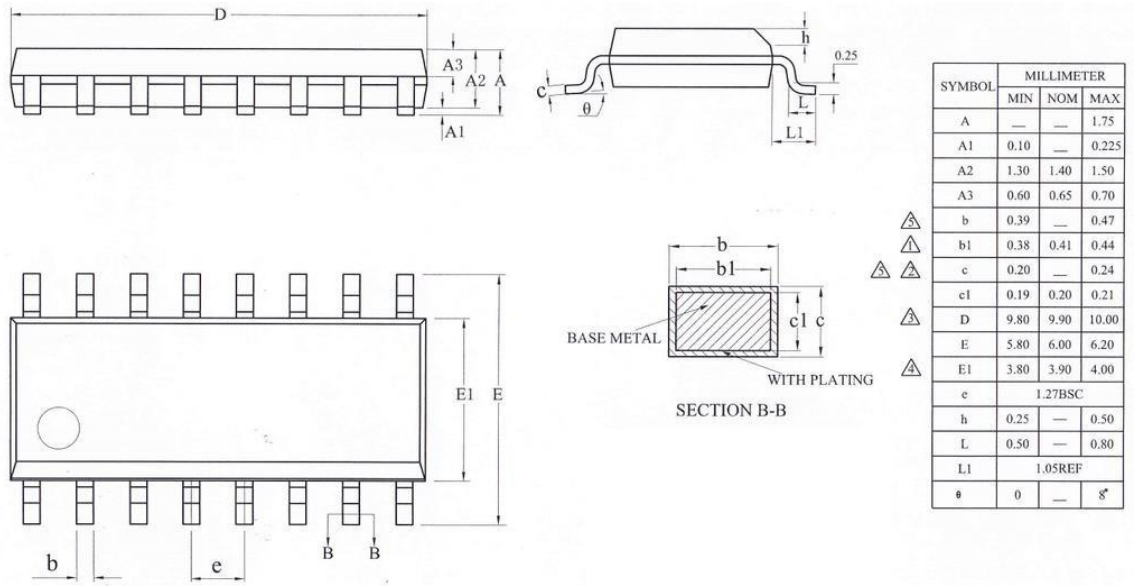
Moisture sensitivity class MSL 3

Warranty period Two years

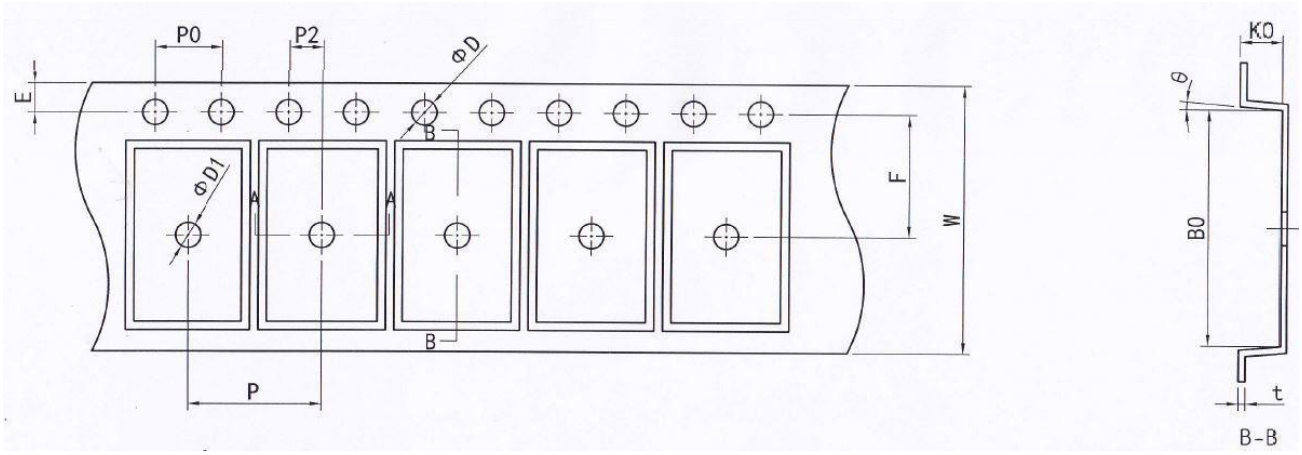
Packaging method Taping packing

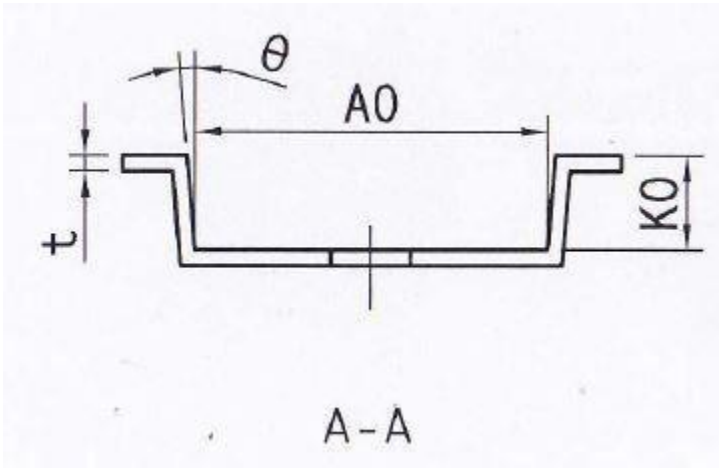
minimum packing 2500

5.1 SOP16L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°





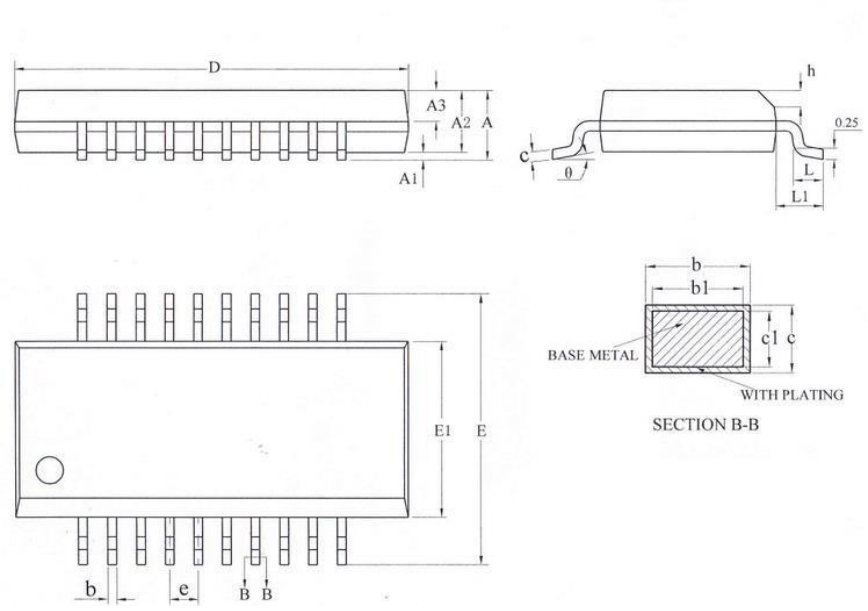
共同尺寸

	外 观	尺 寸(mm)
	E	1.75±0.10
	F	7.50±0.05
⚠1	P2	2.00±0.10
⚠2	D	1.55±0.05
	D1	$1.50^{+0.25}_{-0}$
	P0	4.00±0.10
	10P0	40.0±0.20

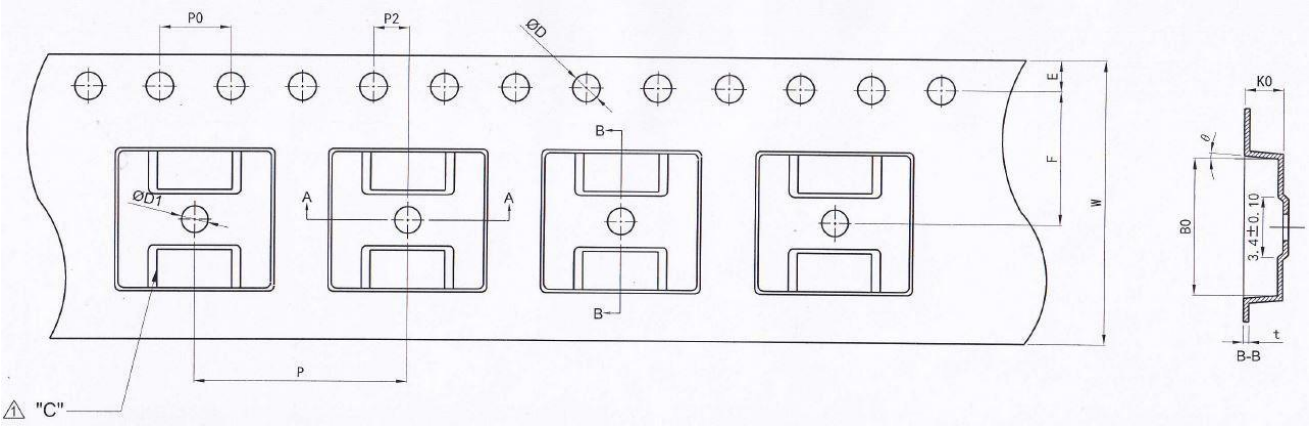
口袋尺寸

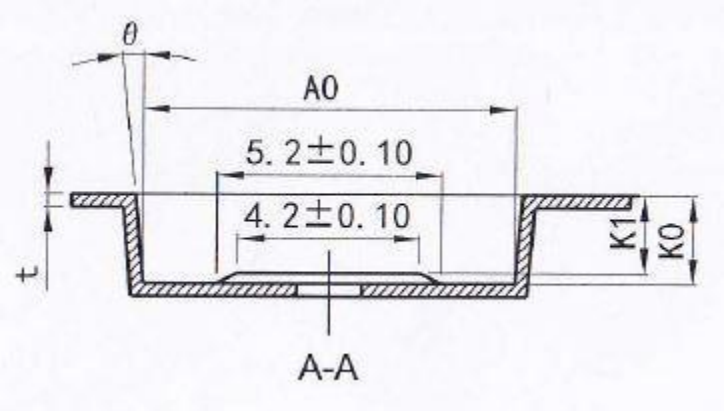
外 观	尺 寸(mm)
W	16.00±0.30
P	8.00±0.10
A0	6.70±0.10
B0	10.40±0.10
K0	2.10±0.10
t	0.30±0.05
θ	5° TYP

5.2 SSOP20L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°





共同尺寸

外 观	尺 寸(mm)
E	1.75±0.10
F	7.50±0.10
P2	2.00±0.10
D	1.55±0.05
D1	$1.5^{+0.25}_{0}$
P0	4.00±0.10
10P0	40.00±0.20

口袋尺寸

外 观	尺 寸(mm)	
W	16.00±0.20	2
P	12.00±0.10	
A0	8.40±0.10	3
B0	7.75±0.10	3
K0	2.50±0.10	3
t	0.30±0.05	
θ	3~5° TYP	
K1	2.10±0.10	3