EE 201C

Homework 1

Wei Wu

Submit code and report to:

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1. References

Capacitance Calculation:

- Formula based
  - T.Sakurai, K.Tamaru, "Simple Formulas for Two- and Three-Dimensional Capacitances," IEEE Trans. Electron Devices ED-30, pp. 183-185
  - F C Wu, S C Wong, P S Liu, D L Yu, F Lin, "Empirical models for wiring capacitances in VLSI", In Proc. IEEE Int. Symp. on Circuits and Systems, 1996
- Table based
  - J. Cong, L. He, A. B. Kahng, D. Noice, N. Shirali and S. H.-C. Yen, "Analysis and Justification of a Simple, Practical 2 1/2-D Capacitance Extraction Methodology", ACM/IEEE Design Automation Conference, June 1997, pp.627-632
- Field solver
  - K. Nabors and J. White, "FastCap: A multipole accelerated 3-D capacitance extraction program", IEEE Trans. Computer-Aided Design, 10(11), 1991.

1. References

Inductance Calculation:

- Table based
  - L. He, N. Chang, S. Lin, and O. S. Nakagawa, "An Efficient Inductance Modeling for On-chip Interconnects", IEEE Custom Integrated Circuits Conference, May 1999.
  - Norman Chang, Shen Lin, O. Sam Nakagawa, Weize Xie, Lei He, "Clocktree RLC Extraction with Efficient Inductance Modeling". DATE 2000
- Circuit model and inductance screening
  - M. Xu and L. He, "An efficient model for frequency-based on-chip inductance," IEEE/ACM International Great Lakes Symposium on VLSI, West Lafayette, Indiana, pp. 115-120, March 2001.
  - Shen Lin, Norman Chang, Sam Nakagawa, "Quick On-Chip Self- and Mutual-Inductance Screen," ISQED, pp.513, First International Symposium on Quality of Electronic Design, 2000.

1. References

Inductance Calculation (cont.):

- PEEC model and Susceptance model
  - A.E. Ruehli, " Inductance calculations in a complex integrate circuit environment," IBM J. Res. Develop., vol. 16, pp. 470-481, Sept. 1972.
  - A. Devgan, H. Ji and W. Dai, "How to Efficiently Capture OnChip Inductance Effects: Introducing a New Circuit Element K," Proc. ICCAD, pp. 150-155, 2000.

- Formulas
  - G. Zhong, and C. Koh. Exact Closed Form Formula for Partial Mutual Inductances of On-Chip Interconnects. ICCD, 2002

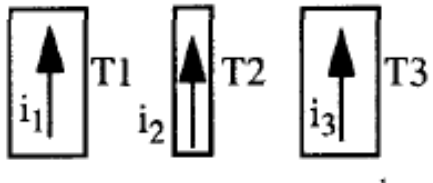
- Field solver
  - M. Kamon, M. J. Tsuk, and J. K. White, "Fasthenry: a multipole-accelerated 3-D inductance extraction program," IEEE Trans. Microwave Theory Tech., pp. 1750 - 1758, Sep 1994.

2. Further Readings

- N. Delorme, M. Belleville, and J. Chilo. Inductance and Capacitance Analytic Formulas for VLSI Interconnects. Electronics letters, 1996
- T. Sakurai. Closed-Form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI's. IEEE Transactions on Electron Devices, 1993
- W. Shi, J. Liu, N. Kakani and T. Yu, "A fast hierarchical algorithm for three-dimensional capacitance extraction", IEEE Trans. CAD, 21(3): 330-336, 2002.
- N. Delorme, M. Belleville, and J. Chilo. Inductance and Capacitance Analytic Formulas for VLSI Interconnects. Electronics letters, 1996
- H. Kim, and C. C. Chen. Be careful of Self and Mutual Inductance Formulae. UW-Madison VLSI-EDA Lab, 2001

3. Example for L_{eff}

- Calculation effective loop inductance (L_{eff}) of signal trace T2



The top view of a coplanar-waveguide

- According to definition of L_{eff} of T2

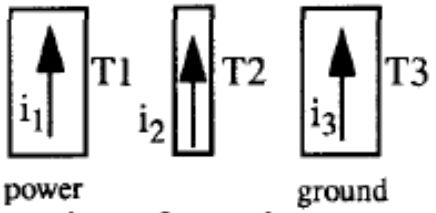
$$\Delta V = L_{eff} \cdot \frac{di_2}{dt} = Lp_{22} \cdot \frac{di_2}{dt} + Lp_{21} \cdot \frac{di_1}{dt} + Lp_{23} \cdot \frac{di_3}{dt}$$
$$-Lp_{11} \cdot \frac{di_1}{dt} - Lp_{12} \cdot \frac{di_2}{dt} - Lp_{13} \cdot \frac{di_3}{dt},$$

- Also, two ground traces have the same voltage drop

$$Lp_{11} \cdot \frac{di_1}{dt} + Lp_{12} \cdot \frac{di_2}{dt} + Lp_{13} \cdot \frac{di_3}{dt}$$
$$= Lp_{13} \cdot \frac{di_1}{dt} + Lp_{23} \cdot \frac{di_2}{dt} + Lp_{33} \cdot \frac{di_3}{dt},$$

- Assume all current returns in this block

- KCL: $i_1 + i_2 + i_3 = 0$



The top view of a coplanar-waveguide

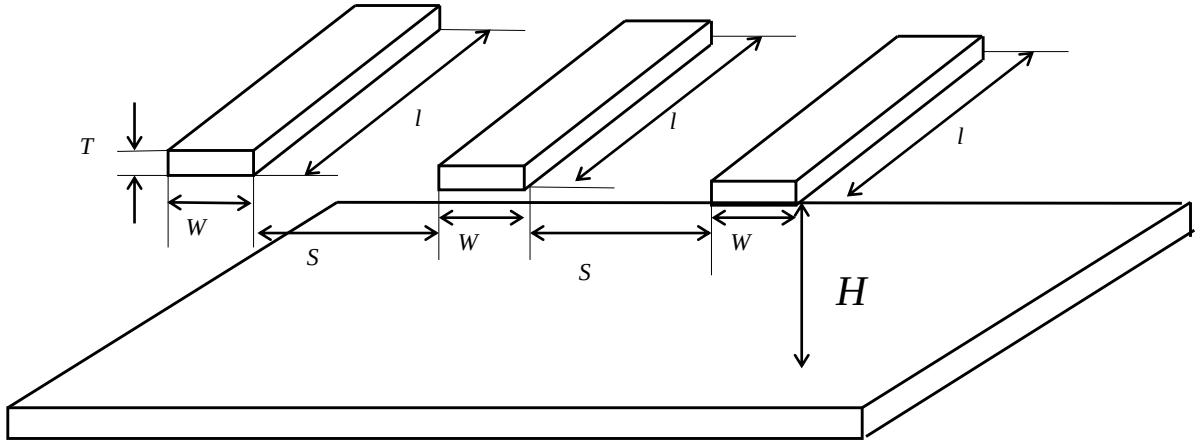
- L_{eff} can be solved as a function of partial inductances

$$L_{eff} = Lp_{22} - 2Lp_{23} + \frac{Lp_{11}}{2} + \frac{Lp_{13}}{2}$$

* L. He, N. Chang, S. Lin, and O. S. Nakagawa, "An Efficient Inductance Modeling for On-chip Interconnects", IEEE Custom Integrated Circuits Conference, May 1999.

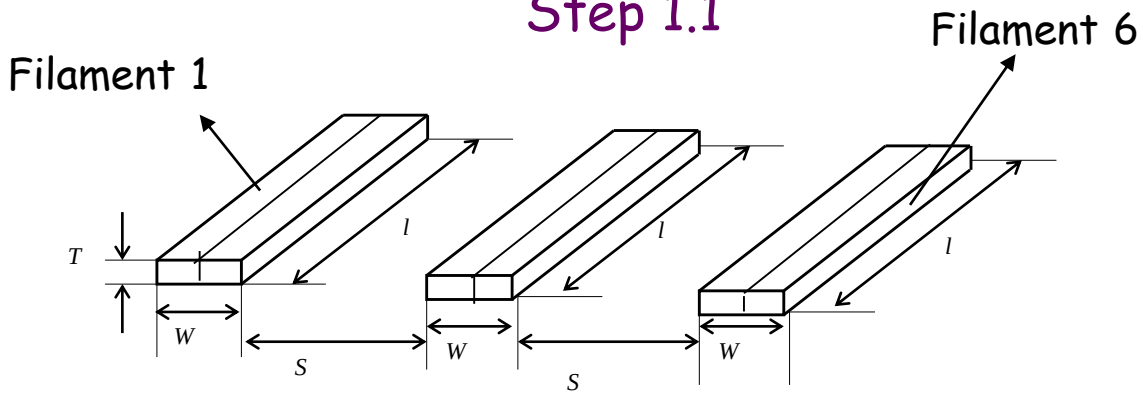
3. Homework (due Feb 1, 2016)

[1] Given three wires, each modeled by at least 2 filaments, find the 3x3 matrix for (frequency-independent) inductance between the 3 wires, along with the capacitance and resistance. We assume that the ground plane has infinite size and is 10 um away for the purpose of capacitance calculation.



- wire width: W=9um, wire thickness: T=6um, wire length: l=9000um,
- wire spacing: S = 15um, distance to ground: H=10um,
- Copper electrical resistivity 0.0175 $\Omega mm^2/m$ (room temperature),
- $\mu = 1.256 \times 10^{-6} H/m$,
- free space $\varepsilon_0 = 8.85 \times 10^{-12} F/m$

Step 1.1



Discretization and L calculation

- Discretize 3 wires into 6 filaments.
- For each filament, calculate its self-inductance with (e.g.)

$$L_{self-L} = \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{W'+T}\right)+\frac{1}{2}+\frac{(W'+T)}{4l}\right]$$

$$W' = W/2$$

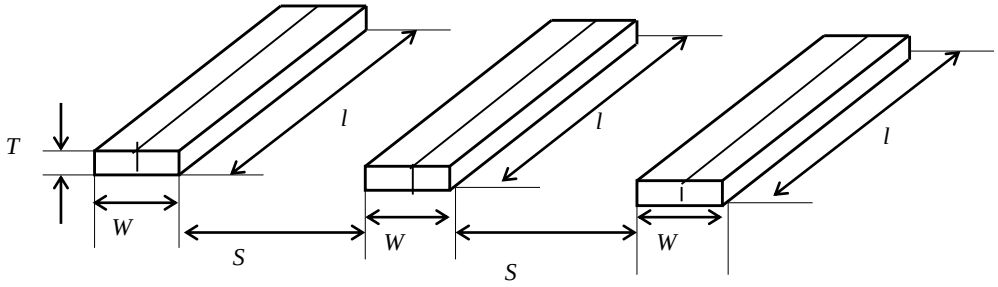
- For each pair of filament, calculate the mutual inductance with (e.g.)

$$L_{mutual-L} = \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{D}\right)-1+\frac{D}{l}\right]$$

- Different filaments and formulae may be used for better accuracy.

Step 1.2

Calculate inductance matrix of three wires



- Mutual Inductance

$$Lp_{km} = \sum_{i=1}^{P} \sum_{i=1}^{Q} Lp_{ij}$$

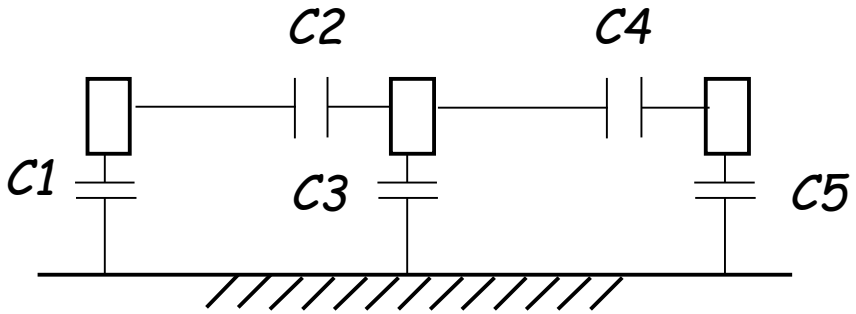
- Lp_{km} is the mutual inductance between conductor T_k and T_m
- Lp_{ij} is the mutual inductance between filament i of T_k and filament j of T_m
- Lp_{ij} can be negative to denote the inverse current direction.

- Self Inductance

- If k=m, Lp_{km} is the self Lp for one conductor

Step 1.3

Capacitance Calculation



C_1 and C_5 equals to average of those for the following two cases:

- single wire over ground
- three parallel wires over ground

Total cap below needs to be split into ground and coupling cap

$$C = \varepsilon\{\frac{w}{h} + 2.977(\frac{t}{h})^{0.232} + [0.229(\frac{w}{s}) + 1.227(\frac{t}{s})^{1.384}](\frac{h}{s})^{0.398}\}$$

Step 1.4

- Resistance Calculation
- Copper electrical resistivity 0.0175 $\Omega mm^2/m$ (room temperature),

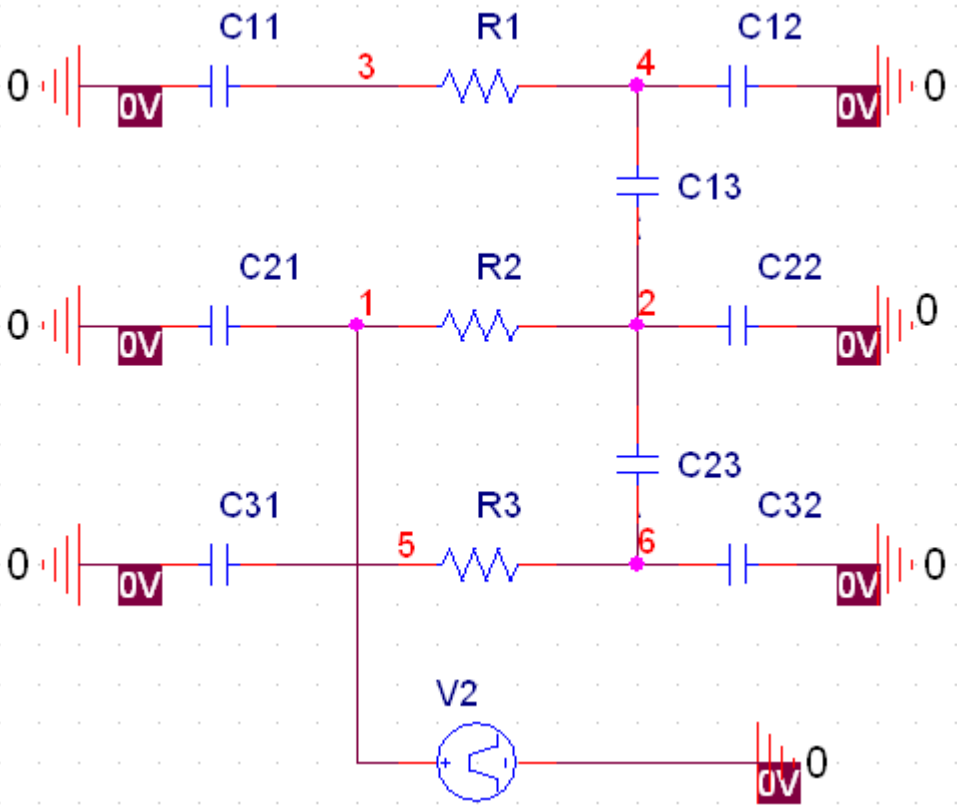
  - l is length of wire
  - A is area of wire's cross section

$$R = \rho \frac{l}{A}$$

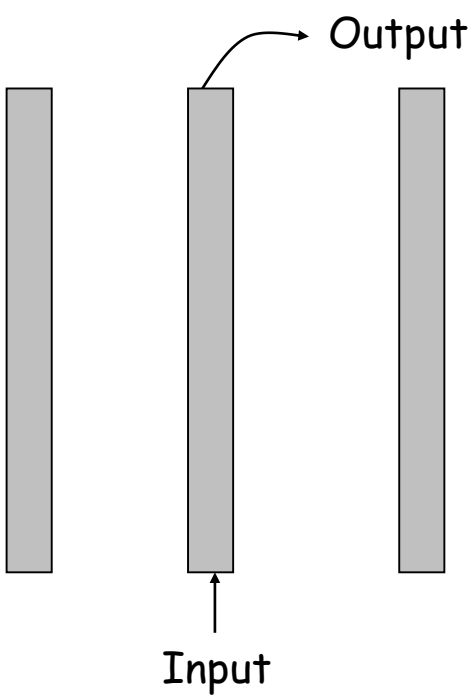
time

[2] Build the RC and RCL circuit models in SPICE netlist for the above wires. (suggest to use matlab script to generate matrix and thus SPICE netlist)

```
*This is RC circuit
VDD 1 0 PULSE(0 1 0 10ps)
C11      3        0        XXXXX
C12      4        0        XXXXX
C21      1        0        XXXXX
C22      2        0        XXXXX
C31      5        0        XXXXX
C32      6        0        XXXXX
C13      4        2        XXXXX
C23      6        2        XXXXX
R1       3        4        XXXXX
R2       1        2        XXXXX
R3       5        6        XXXXX
.op
.TRAN 1ps 50ps
.print all
.plot all
.END
```

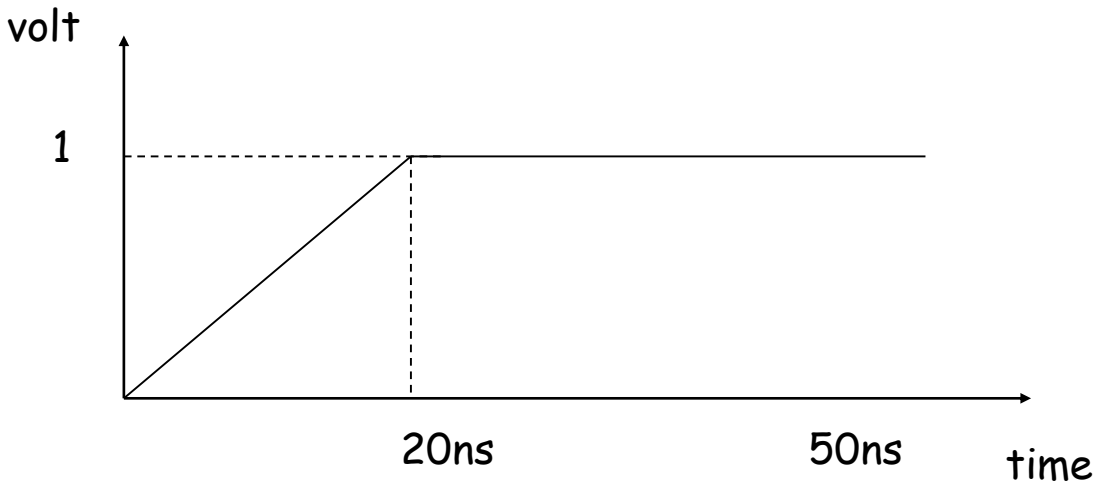


[3] Assume a step function applied at end-end, compare the four waveforms at the far-end for the central wire using SPICE transient analysis for (a) RC and RLC models and (b) rising time is 20ns, or try to use longer rising time.



Suggested Input:

VDD 1 0 PULSE(0 1 0 20ns)



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