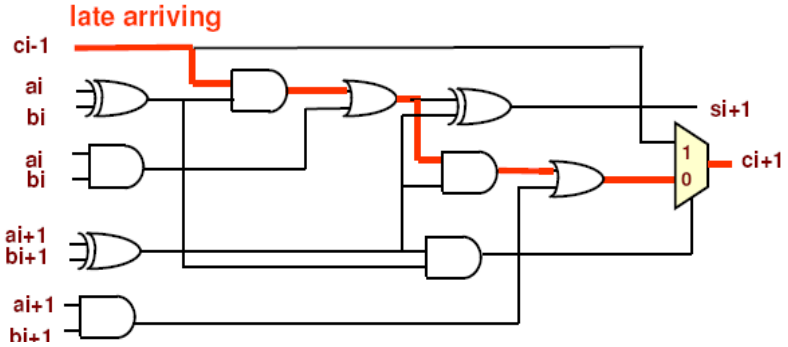
Homework 3 solution

1. With the same circuit, the red critical path has been proved to be false path. Try to find the true critical path for this circuit. Assume unit gate delay in this circuit.



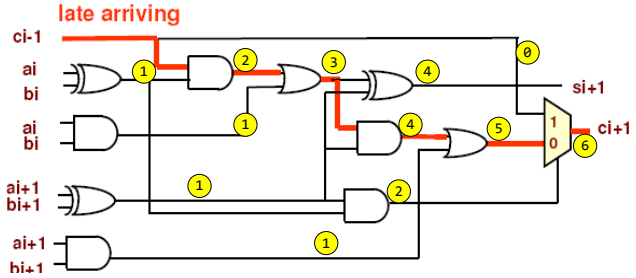
Solution

This circuit is too simple to adopt the algorithm in the reference [1]. For this problem, the methodology is to find the critical path and verify if it is the sensitive path.

1.1. Find critical path:

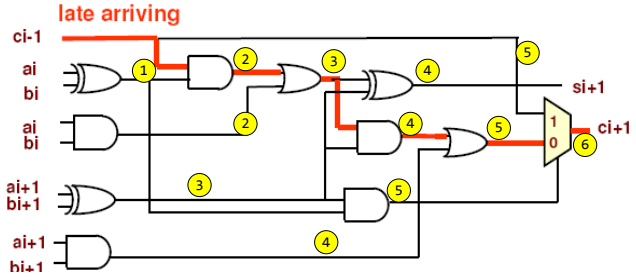
For this circuit, we can first calculate the arrival time (AT) as:

Arrival time (AT):

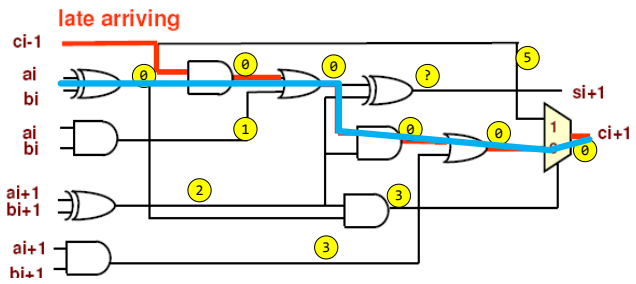


It's obviously that the critical path follows 1,2,3,4,5,6, but here we follow the steps and calculate the required arrival time:

Required Arrival Time (RAT): Assume the RAT of sink point is 6.



Once the AT and RAT are known, then the slack can be represented as:



1.2. Verify the critical path

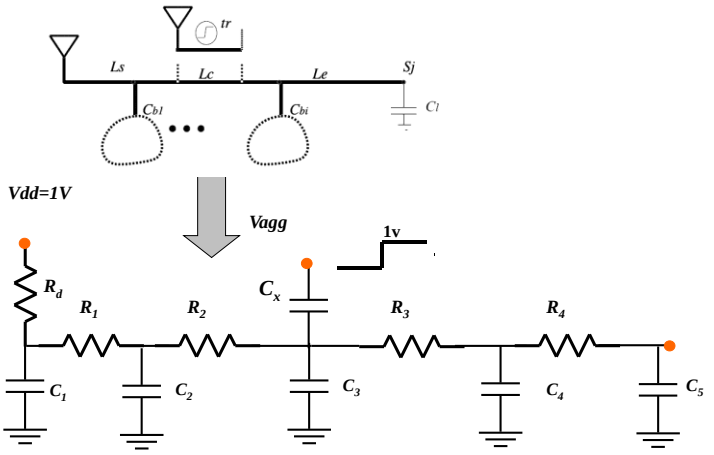
Then, verify whether that path is true path:

The single propagation depends on

$$
\begin{aligned}
& c_{i-1}\&(a_{i+1}\ XOR\ b_{i+1})\&\overline{\left((a_{i+1}\ XOR\ b_{i+1})\&(a_i\ XOR\ b_i)\right)} \\
&= c_{i-1}\&(a_{i+1}\ XOR\ b_{i+1})\&\left(\overline{(a_{i+1}\ XOR\ b_{i+1})}\,|\,\overline{(a_i\ XOR\ b_i)}\right) \\
&= c_{i-1}\&(a_{i+1}\ XOR\ b_{i+1})\&\overline{(a_i\ XOR\ b_i)} \\
&\neq \emptyset
\end{aligned}
$$

So the critical path is a true path.

2. Given the layout of a victim net and an aggressor net above it. Try to calculate noise voltage output & waveform considering crosstalk using the noise model from [aspdac'01] .



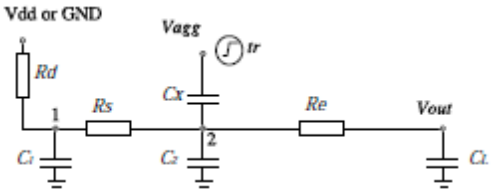
Solution

Compare the solution of [aspdac'01] with hspice model

2.1. Crosstalk noise model:

2.1.1.Add C_{bi} to the C_1, C_2 and C_L.

According to section 2.3 in [aspdac'01], we can incorporate the lumped capacitance to C_1, C_2 and C_L. Then the circuit model in this problem becomes a $2-\pi$ model.



Here C_{b1} and C_{b2} can be divided to C1 and C2.

For C_{b1} (C2), α=R1/(R1+R2) = 0.4, then 0.4*C_{b1} goes to C1, and 0.6*C_{b1} goes to CL;

For C_{b2} (C4), β=R4/(R3+R4)= 6/11, then 6/11*C_{b2} goes to C2, and 5/11*C_{b2} goes to CL;

2.1.2.Calculate the parameters in equivalent $2-\pi$ model

$R_s = R_1 + R_2 = 250\Omega$

$R_e = R_3 + R_4 = 550\Omega$

$C_x = C_x = 5e-14F$

$R_d = R_d = 300\Omega$

$C_1 = C_1 + 0.4 * C_{b1} = 4e-14F$

$C_2 = C_3 + 0.6 * C_{b1} + 5/11 * C_{b2} = 6.091e-14F$

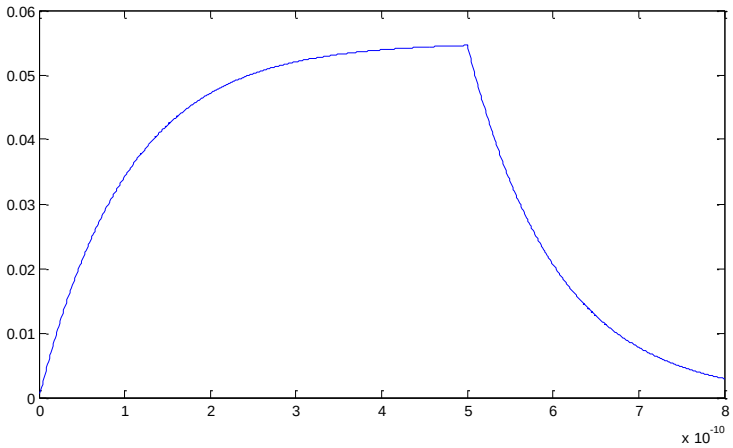
$C_L = C_5 + 6/11 * C_{b2} = 4.21e-14F$

2.1.3.Apply closed form

Then apply the closed form

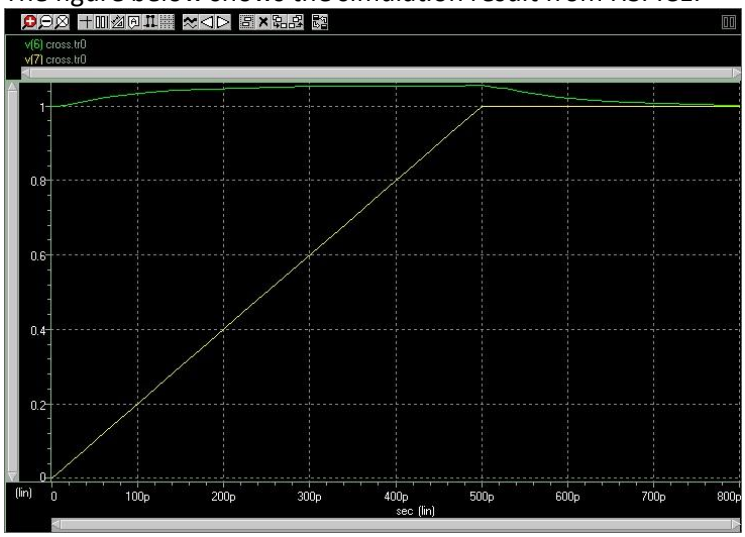
$$V_{out} = \begin{cases} \frac{t_x}{t_v}(1 - e^{-t/t_v}) & 0 \le t \le t_r \\ \frac{t_x}{t_v}(e^{-\frac{t-t_r}{t_v}} - e^{-t/t_v}) & t > t_r \end{cases}$$

Here t_r is $500ps = 5e-12s$,
$t_x = (R_d + R_s) * C_x = 2.75e-11s$
$t_v = (R_d + R_s) * (C_x + C_2 + C_L) + R_e C_L + R_d C_1 = 1.0275e-10s$
(Note: t_x and t_v can also be calculated by the RC delay form the upstream resistance and the distributed Elmore delay of the victim net)
Then, put these values into matlab, the Vout can be plot as:

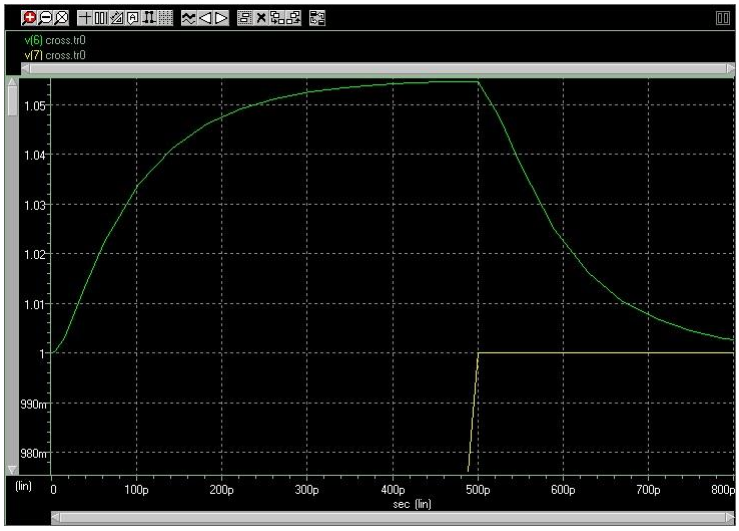


2.2. SPICE result

The figure below shows the simulation result from HSPICE.



If zoom in the figure, it illustrates that the cross talk results in an inference with peak of 0.054V, which is consistent with the close form analysis result.



[1] Chul Rim; Soo-Hyun Kim; Joo-Hyun Park; Myung-Soo Jang; Jin-Yong Lee; Kyu-Myong Choi; Jeong-Taek Kong; , "Fast and practical false-path elimination method for large SoC designs," SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip] , vol., no., pp. 397- 400, 17-20 Sept. 2003

[2] J. Cong, Z. Pan and P. V. Srinivas, "Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization", ASPDAC 2001