Homework 2 (Due Feb. 15)

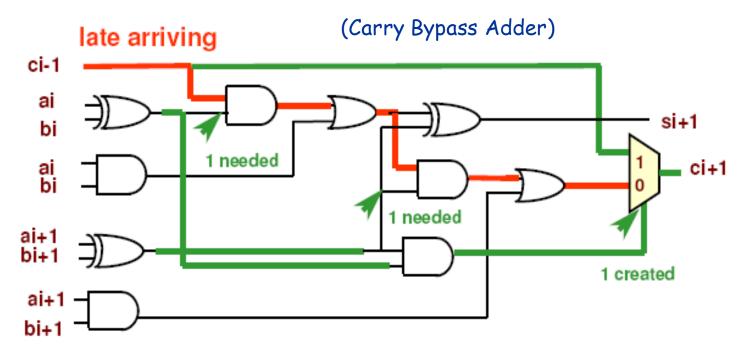
Submit code and report to:

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Email Subject: EE201C_HW2_Name_UID

False Path

False Path: those paths which signals never propagate from PI to PO.



To sensitize red path we need:

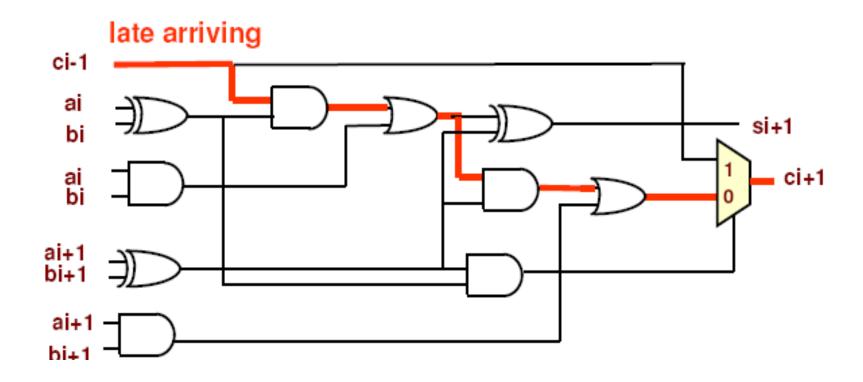
■ ai XOR bi && ai+1 XOR bi+1

But: red path is false

- When above condition is true, MUX selects "1" input, i.e. directly from ci-1
- Instead shorter green paths are sensitized
- Hence, red path is not the critical path of the circuit!

Problem 1

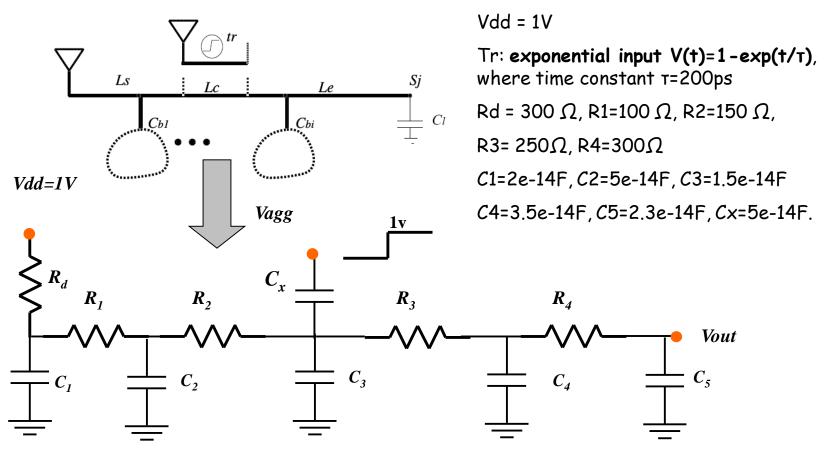
[1] With the same circuit, the red critical path has been proved to be false path. Try to find the true critical path for this circuit. Assume unit gate delay in this circuit.



Problem 2 Crosstalk Noise Calculation

[2] Given the layout of a victim net and an aggressor net above it. Try to calculate (1)noise voltage output in closed-form (2) max output (Vmax) (3) waveform Vout and compare it with HSPICE simulation result.

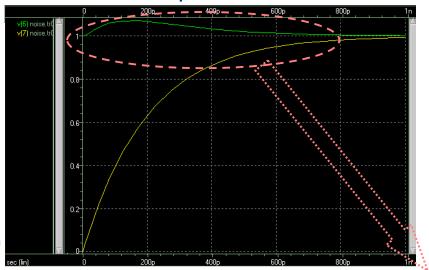
You may refer to the noise model proposed in [aspdac'01]. Note that in [aspdac'01], it uses a step signal as Vagg (equation 3), but Vagg (Tr) is replace by a exponential input in the homework.



[aspdac'01] Jason Cong, David Zhigang Pan, and Prasanna V. Srinivas. 2001. "Improved crosstalk modeling for noise constrained interconnect optimization". In *Proceedings of the 2001 Asia and South Pacific Design Automation Conference* (ASP-DAC '01). Pages: 373-378.

Problem 2 Crosstalk Noise Calculation (cont.)

Compare your calculation with Spice Simulation results



```
.op
.TRAN 1ps 1000ps
```

```
.print all
.plot all
.END
```

