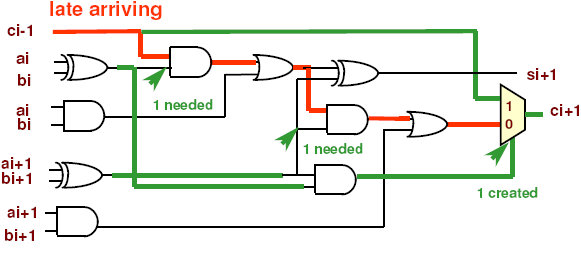
**Homework 2**

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*Problem 1： False Path: those paths which signals never propagate from PI to PO.*

*To sensitize red path we need:*

*ai XOR bi && ai+1 XOR bi+1*

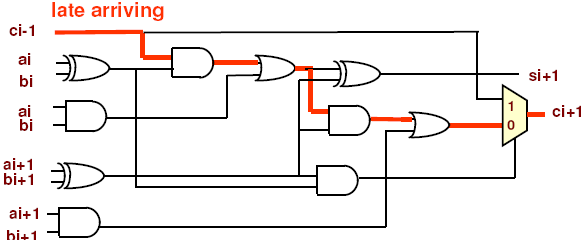
*But: red path is false*

*When above condition is true, MUX selects “1” input, i.e. directly from ci-1*

*Instead shorter green paths are sensitized*

*Hence, red path is not the critical path of the circuit!*

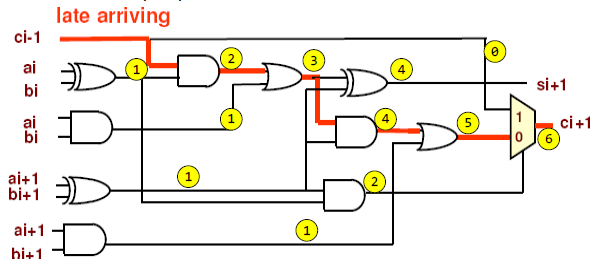
*With the same circuit, the red critical path has been proved to be false path. Try to find the true critical path for this circuit. Assume unit gate delay in this circuit.*



**Solution:**

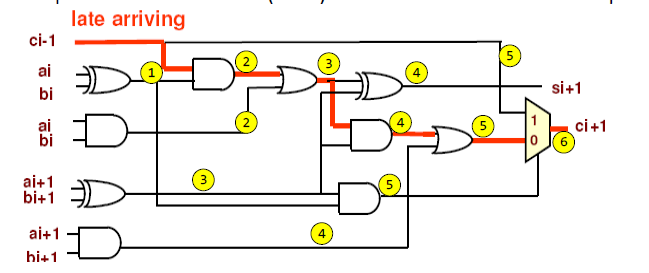
The arrival time is shown in Figure 1.1.

The numbers 1, 2, 3, 4, 5 and 6 mean the delay of the arrival time delay of the path.



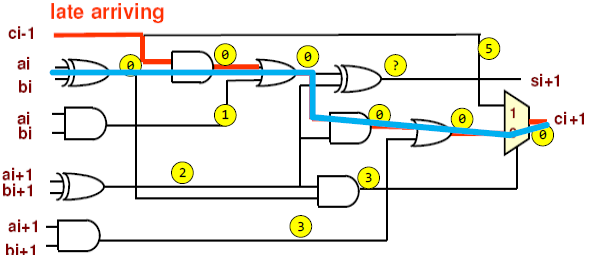
**Figure 1.1 Arrival time analysis**

By the same method, we can define the required arrival time in Figure 1.2.



**Figure 1.2 Required arrival time analysis**

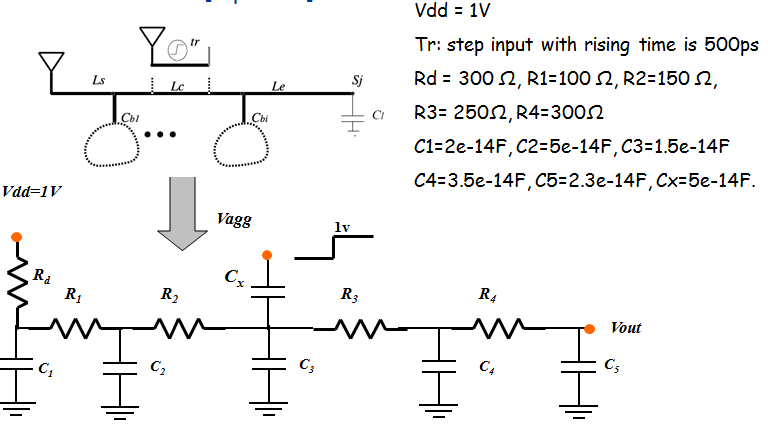
By subtracting the number, we can find the time slack of the circuit in Figure 1.3.



**Figure 1.3 Time slack analysis**

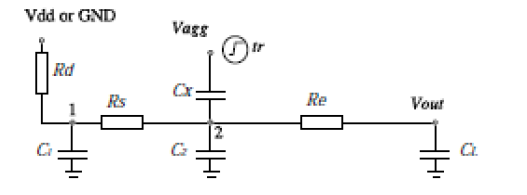
The critical path is the path with zero time slack as the blue solid line depicts in Figure 1.3.

*Problem 2: Given the layout of a victim net and an aggressor net above it. Try to calculate noise voltage output & waveform considering crosstalk using the noise model from [aspdac’01].*



**Solution:**

According to [aspdac’01], we can incorporate the lumped capacitance to , and in Figure 2.1.



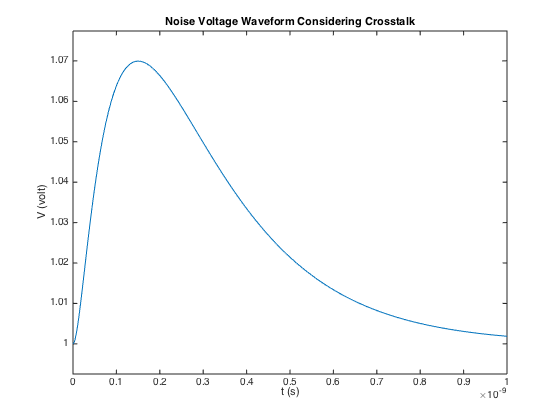
**Figure 2.1 Lumped model**

We can then calculate the parameters of the lumped model as follows:

And we apply the formula:

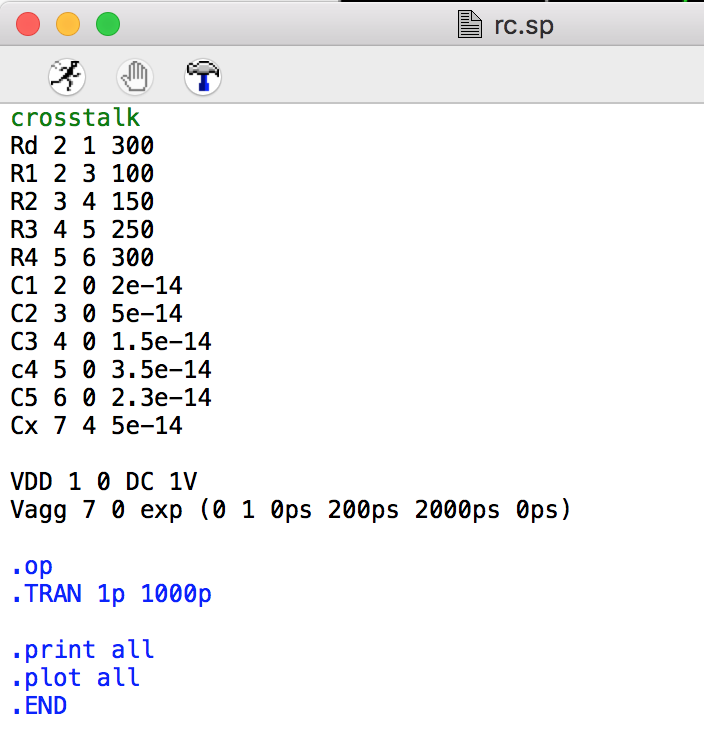
Where

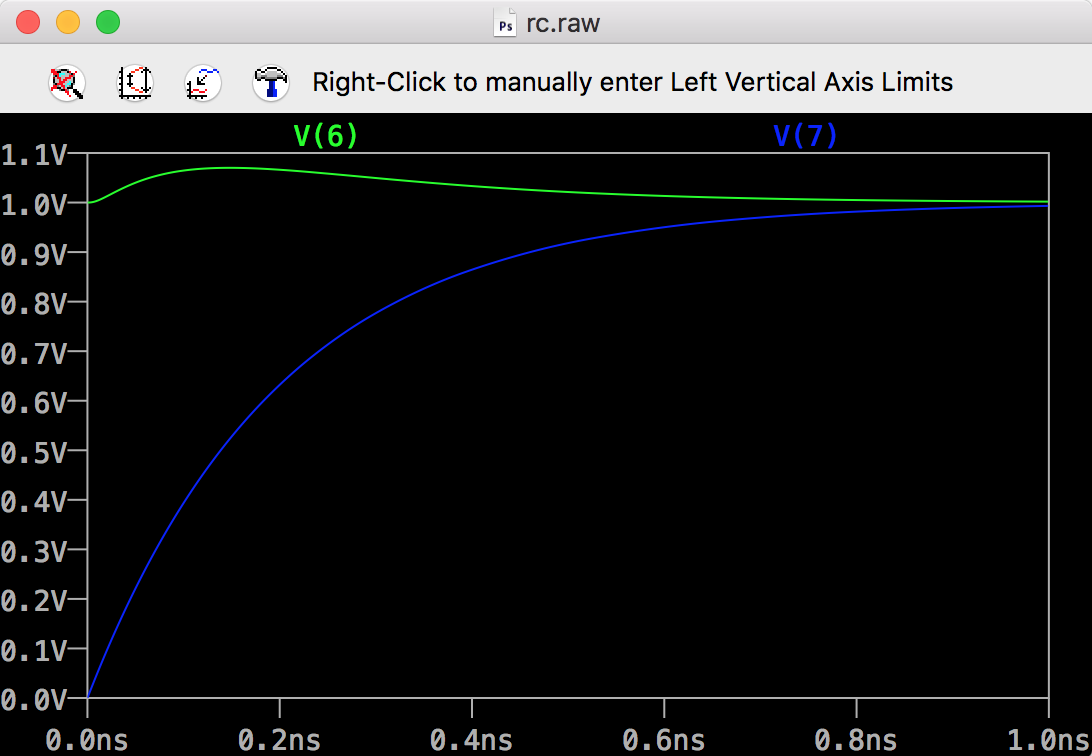
Then we have figure 2.2.

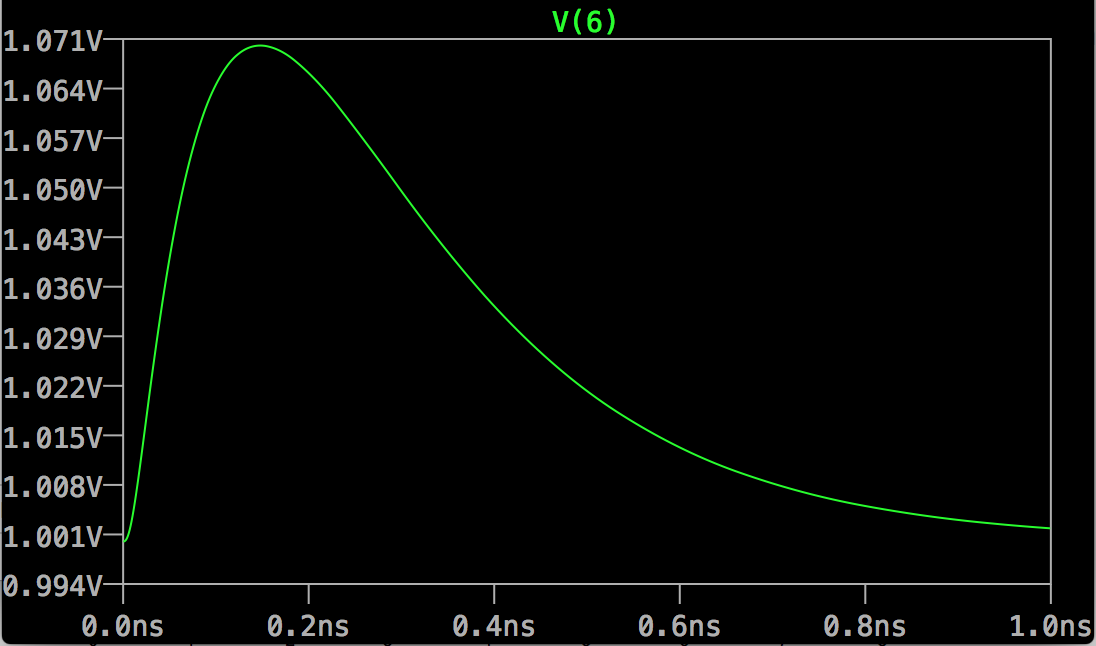


**Figure 2.2 Vout output figure**

If we do the same job in Spice, we can find the same result as Figure 2.3 shows.







**Figure2.3 Spice results**