IEEE Transactions on Computer-Aided Design Donald O. Pederson Best Paper Award

To recognize the best paper published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.

Historical Background:
The IEEE Transactions on Computer-Aided Design Donald O. Pederson Best Paper Award is sponsored by the IEEE Council on EDA and recognizes the best paper published in the Transactions on Computer-Aided Design of Integrated Circuits and Systems publication.

The award is based on the overall quality, the originality, the level of contribution, the subject matter and the timeliness of the research. Anyone who is an author of a paper published in the Transactions on Computer-Aided Design of Integrated Circuits and Systems during the two calendar years preceding the award is eligible for nomination.

Prize:
$500 for each author (maximum of $2,000 per award) and Certificate plaque

Funding:
Funded by the IEEE Council on Electronic Design Automation.

Presentation:
The award will be presented at the ICCAD conference.

Basis for Judging:
General quality, originality, contributions, subject matter, and timeliness.

Eligibility:
Authors of papers published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems during the two calendar years preceding the award. Self Nominations are permitted. Each nominator may only nominate one paper only.

Nomination Details:
Nomination deadline is 28 February of the award year.

View the 2020 Donald O. Pederson Award Committee

Nomination Form:

Nominate for this Award

Recipients

2020

"An Efficient Methodology for Mapping Quantum Circuits to the IBM QX Architectures"
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 38, no. 7, pp. 1226-1236, July 2019

Alwin Zulehner, Alexandru Paler, and Robert Wille

2019

"YodaNN: An Architecture for Ultralow Power Binary-Weight CNN Acceleration"
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 1, pp. 48-60, Jan. 2018

Renzo Andri, Lukas Cavigelli, Davide Rossi, and Luca Benini

2019

"Caffeine: Towards Uniformed Representation and Acceleration for Deep Convolutional Neural Networks"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 38, Issue 11, pp. 2072 - 2085, November 2019

Chen Zhang, Guangyu Sun, Zhenman Fang, Peipei Zhou, Peichen Pan, and Jason Cong

2018

"Majority-Inverter Graph: A New Paradigm for Logic Optimization"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 35, Issue 5, pp. 806 - 819, May 2016

Luca G. Amaru, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli

2017

"Mining Requirements from Closed-Loop Control Models"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 34, Issue 11, pp. 1704 – 1717, November 2015

Xiaoqing Jin, Alexandre Donzé, Jyotirmoy V. Deshmukh, and Sanjit A. Seshia

2016

"Fast Statistical Analysis of Rare Circuit Failure Events via Scaled-Sigma Sampling for High-Dimensional Variation Space"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 34, Issue 7, pp. 1096 - 1109, July 2015

Shupeng Sun, Xin Li, Hongzhou Liu, Kangsheng Luo, and Ben Gu

2015

"Testing of Flow-Based Microfluidic Biochips: Fault Modeling, Test Generation, and Experimental Demonstration"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 33, Issue 10, pp. 1463 - 1475, October 2014

Kai Hu, Feiqiao Yu, Tsung-Yi Ho, and Krishnendu Chakrabarty

2014

"Stochastic Testing Method for Transistor-Level Uncertainty Quantification Based on Generalized Polynomial Chaos"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 32, Issue 10, pp. 1533 - 1545, September 2013

Zheng Zhang, Tarek A. El-Moselhy, Ibrahim M. Elfadel, and Luca Daniel

2013

"Virtual Probe: A Statistical Framework for Low-Cost Silicon Characterization of Nanoscale Integrated Circuits"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 30, Issue 12, pp. 1814 - 1827, December 2011

Wangyang Zhang, Xin Li, Frank Liu, Emrah Acar, and Ronald D. (Shawn) Blanton

2012

"An Analytical Approach for Network-on-Chip Performance Analysis"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 29, Issue 12, pp. 2001-2013, December 2010

Umit Ogras, Paul Bogdan, and Radu Marculescu

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