AN 26.21

USB Device Design Checklist

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INTRODUCTION

The purpose of this application note is to provide a list of items that need to be considered when designing systems that incorporate the following categories of Microchip USB products:

- USB 2.0 Hubs
- USB 3.0 Hubs
- Flash Media Controllers
- Flash Media Controller Hub Combo
- USB Transceivers

The target audience of this document is system engineers and layout professionals who are familiar with industry standard practices. This application note must be used in conjunction with the device data sheet, reference design, and other relevant application notes.

OVERVIEW

This document includes the following chapters:

- Schematic Guidelines
- Layout Guidelines

Each chapter begins with a sub-section on the general design considerations for all products. Subsequent sub-sections detail design considerations for specific product categories and their applications. The order of these lists are arbitrary.

REFERENCES

- Application Notes:
  - AN 18.16, PCB Design Guidelines for USB223x/i & USB225x/i Controllers
  - AN 26.2, Implementation Guidelines for Microchip's USB 2.0 and USB 3.0 Hub Devices
  - AN 18.15, PCB Design Guidelines for QFN and DQFN Packages
  - AN 19.17, ULPI Design Guide
  - WP 2.10, PCB Design for WLCSP BGA Packages
- The data sheet for the respective product(s)
- Applicable USB specifications and ECNs available at usb.org

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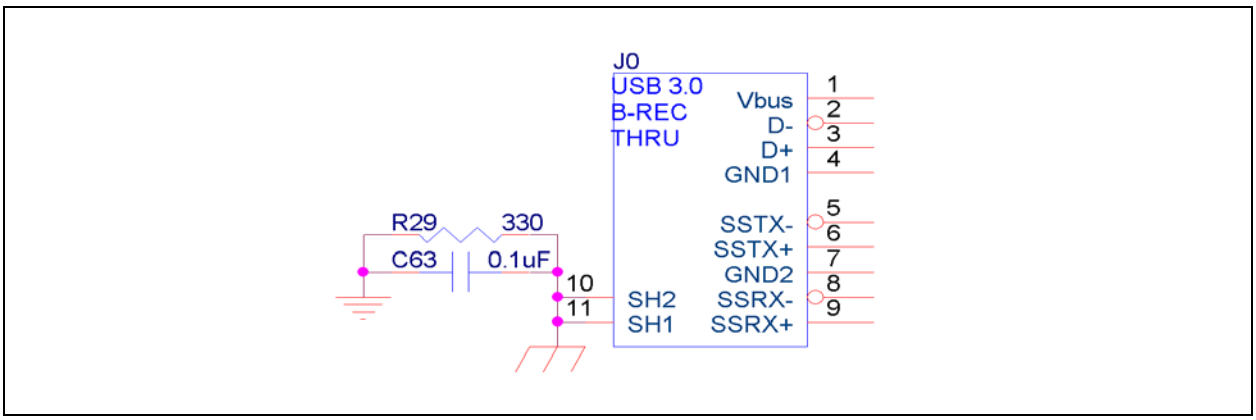
1.0 SCHEMATIC GUIDELINES

1.1 General Considerations

- □ **A.** Confirm the pin-out functions of the schematic symbol of the USB product matches what is provided in the product data sheet.
- □ **B.** For designs with exposed USB connectors, connect the USB cable shield to digital ground with an RC network. Refer to the Microchip AN 26.2 application note for additional details.

FIGURE 1-1: SHIELD TO DIGITAL GROUND CONNECTION



- □ **C.** Ensure that the power rails, such as VDD12 or VDD33, are not noisy and are stable and accurate across all power consumption ranges. Refer to the Microchip AN 26.2 application note and the product data sheets for additional details.
- □ **D.** RESETn should be asserted buy a supervisory circuit when either VDD12 or VDD33 are below their thresholds or asserted under manual or host control. Refer to the Microchip AN 26.2 application note for additional details.
- □ **E.** To use in-system OTP programming through SMBus, SM_DAT should be pulled up with an external resistor and SM_CLK should be pulled down with an external resistor. The programmer pulls SM_CLK up with a resistor when connected to the PCB. Refer to the Microchip AN 26.2 application note for additional details.
- □ **F.** Make sure that the crystal and load capacitors are chosen correctly for proper operation. Refer to the product data sheet for additional details.
- □ **G.** If the Microchip product has internal regulators, place regulator capacitors on the regulator pins as described in the product data sheet.
- □ **H.** Internal regulators of the Microchip product must have the proper input voltage. No external voltage should be applied to the output of these internal regulators. Refer to the product data sheet for additional details.
- □ **I.** Place a 2.2uF capacitor on upstream Vbus to comply with the USB-IF decoupling capacitance requirements with margin for capacitor tolerances. Refer to the USB 2.0 Specification for additional details.
- □ **J.** VBUS_DET should be connected to the upstream VBUS through a resistor divider for stand-alone applications. Embedded applications should actively control this pin with a 3.3V signal. Refer to the Microchip AN 26.2 application note for additional details.
- □ **K.** The Rbias resistor must be the correct value and have, at worst, a 1% tolerance. Refer to the product data sheet for additional information.
- □ **L.** Pins that are identified as no connect should not be connected to any net. Refer to the product data sheet for additional information.
- □ **M.** Ensure that the product is configured correctly by either puling the relevant strap pins up/down appropriately, or via SMBus/I^2C. Refer to the product data sheet for additional information.

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- □ **N.** Ensure that any SPI or EEPROM devices are compatible with the Microchip product. Refer to the product data sheet for additional information.

1.1.1 USB2.0 SIGNALS

- □ **A.** Do not use common mode chokes unless needed. Chokes must have a DIFFERENTIAL IMPEDANCE of 90 ohms. Refer to the Microchip AN 26.2 application note for additional details.

1.1.2 USB 3.0 SIGNALS

- □ **A.** Do not use common mode chokes unless needed. Chokes must have a DIFFERENTIAL IMPEDANCE of 90 ohms. Refer to the Microchip AN 26.2 application note for additional details.
- □ **B.** Do not place ESD protection ICs on SuperSpeed Tx and Rx differential pairs unless proven necessary. Refer to the Microchip AN 26.2 application note for additional details.

1.2 USB Hubs

- □ **A.** The PRT_PWR/PRT_CTL pins should be connected to the USB Power switch IC with an open drain overcurrent signal when using individual port power for exposed downstream ports.
- □ **B.** For downstream embedded devices, the appropriate PRT_PWR or PRT_CTL pin should be connected to the input of the downstream device that controls its enumeration.
- □ **C.** Place a 150uF capacitor on Vbus pin on any exposed downstream ports to comply with the USB-IF requirements with margin for capacitor tolerances. Refer to USB 2.0 Specification.

1.3 Flash Media Signals

- □ **A.** Place a capacitor on CRD_PWR pins with the appropriate value to meet the system requirements.
- □ **B.** Ensure that the flash media card connector’s card detect and write protect switch logic are compatible with the respective inputs to the controller. Refer to the product data sheet for additional information.
- □ **C.** If the flash media card connector’s card detect or write protect switches are connected to the shield, make sure that the shield is connected to ground appropriately.

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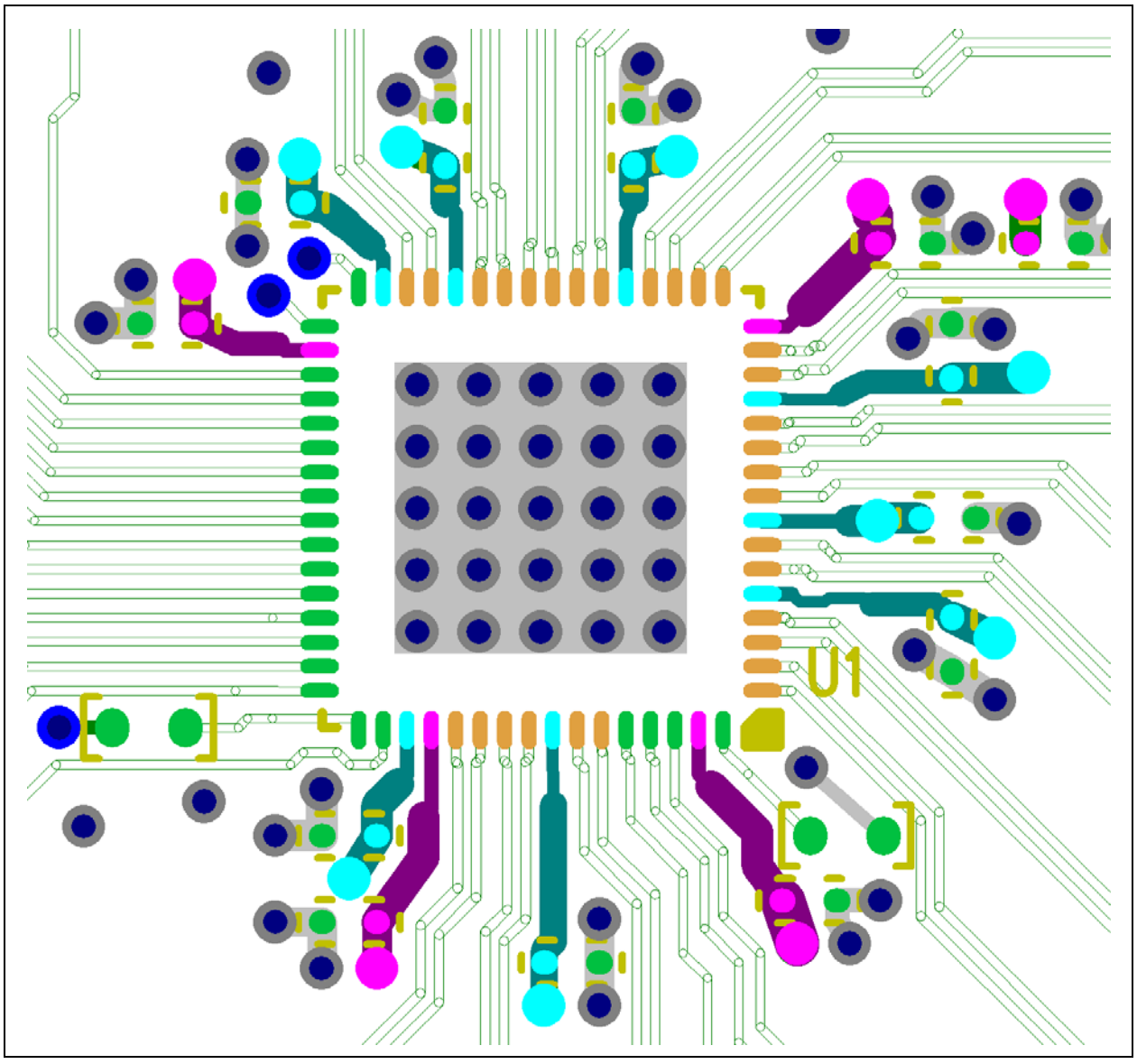
2.0 LAYOUT GUIDELINES

2.1 General Considerations

- □ **A.** Place RBIAS, bypass capacitors, and crystal components close to the respective pins. Refer to the Microchip AN 26.2 application note for additional details.
- □ **B.** Place electrically noisy devices, including switching regulators, far away from the hub circuit, RBIAS, crystal, and USB differential pairs. Refer to the Microchip AN 26.2 application note for additional details.
- □ **C.** Use a thin dielectric between PCB signal-to-plane layers. See AN 26.2 for more information.
- □ **D.** The connection of bypass capacitors to their pins, and to power and ground, must be low inductance (short and very wide traces). Refer to the Microchip AN 26.2 application note for additional details.

FIGURE 2-1: EXAMPLE BYPASS CAPACITOR PLACEMENT AND ROUTING



- □ **E.** Fill the ground flag with vias to the ground plane layer, especially around the periphery of the flag. Refer to the Microchip AN 26.2 application note for additional details.
- □ **F.** RBIAS must be connected to the ground plane nearest to the RBIAS pin on the hub. This return path

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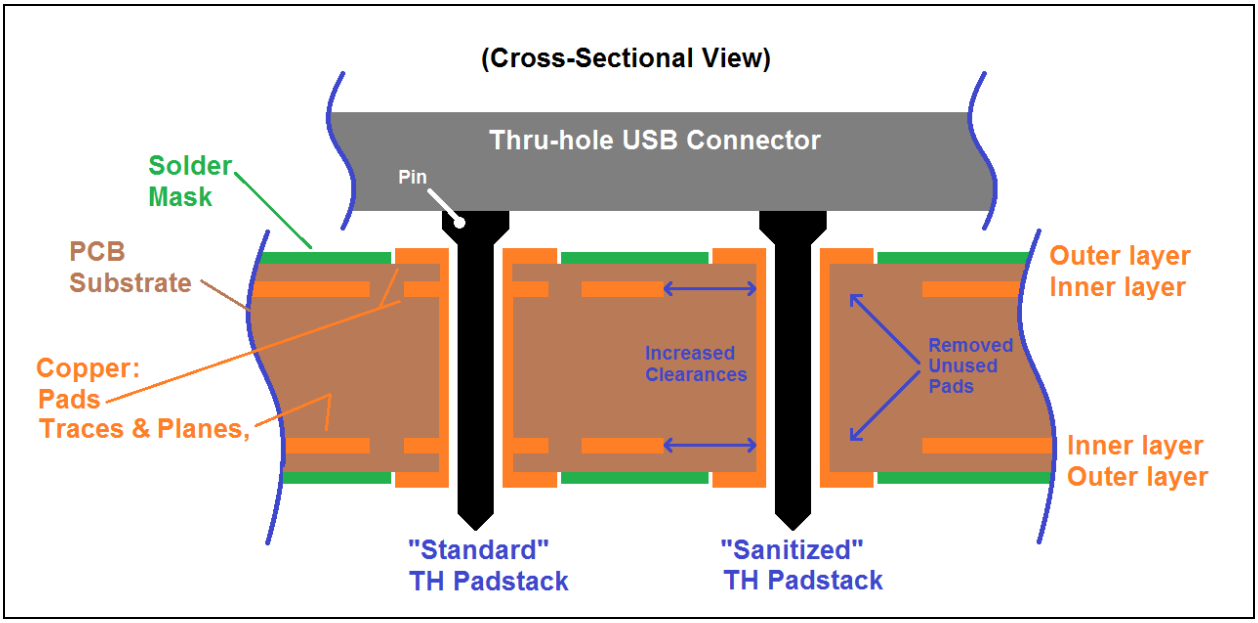
must not be shared with any other components. Refer to the Microchip AN 26.2 application note for additional details.

- **G.** Remove pin pads of through-hole USB connectors on unused layers and increase clearances. Refer to the Microchip AN 26.2 application note for additional details.

FIGURE 2-2: THROUGH HOLE PAD-STACK



- **H.** Use surface mount USB connectors whenever possible. For through hole USB connectors, propagate the USB signals through the end of the through hole pin either by mounting the connector on the opposite side of the PCB or through the use of vias. Refer to the Microchip AN 26.2 application note for additional details.
- **I.** Route foreign traces no closer than 5 times the minimum trace spacing to crystal traces. Refer to the Microchip AN 26.2 application note for additional details.
- **J.** Avoid routing between the ground flag and the pads for a QFN device. Refer to the Microchip AN 18.15 application note for additional details.

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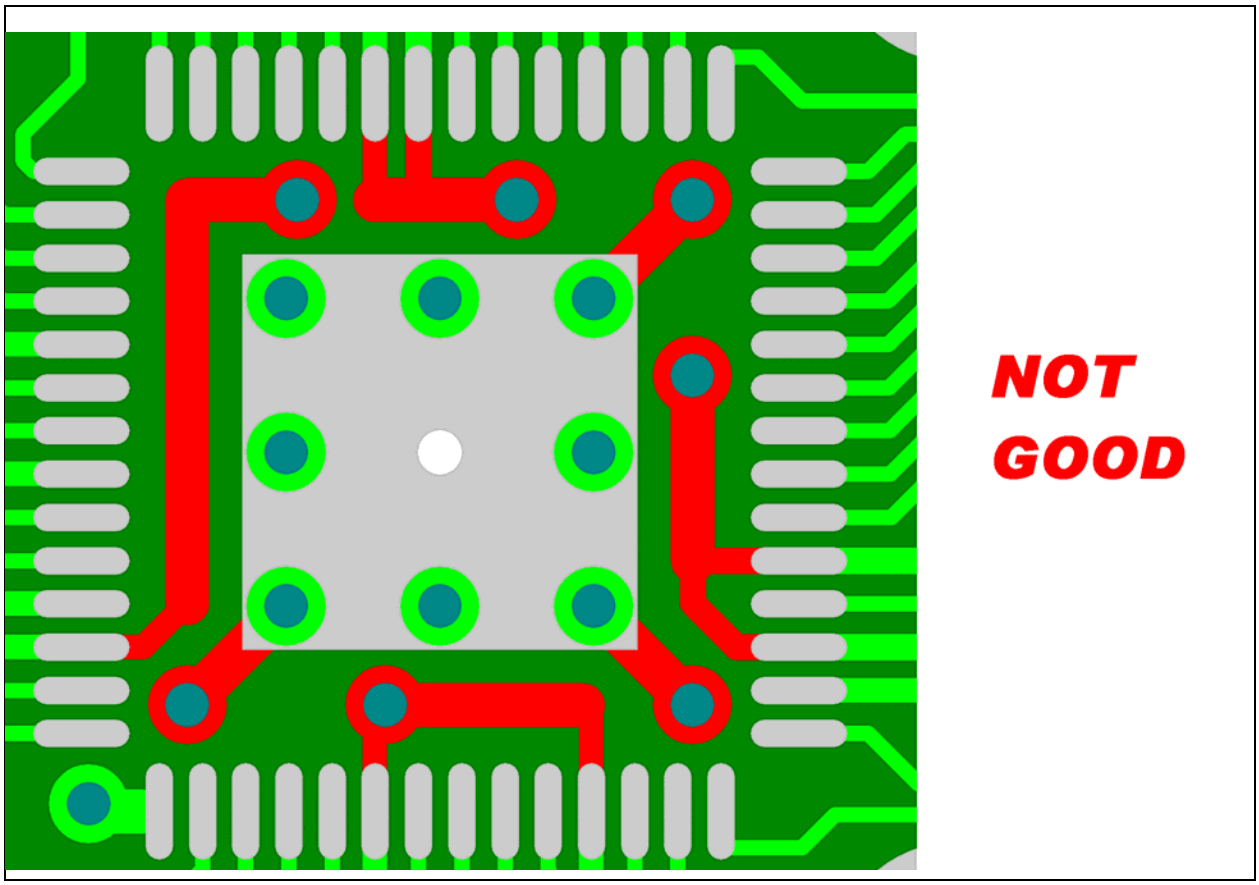
FIGURE 2-3: POOR QFN ROUTING



- □ **K.** Route crystal traces at least 5 times the minimum trace spacing away from other traces. Refer to the Microchip AN 26.2 application note for additional details.
- □ **L.** When using WLCSP products, the land pattern should conform to that described in WP 2.10.

2.1.1 HSIC SIGNALS

High-Speed Inter-Chip USB is a two-wire, single-ended signaling method that uses the USB 2.0 protocols for communication between ICs in a system. The interface is specifically High-Speed. Refer to the *High-Speed Inter-Chip USB Electrical Specification* (USB.org) for details.

- □ **A.** Match the Strobe and Data trace lengths to within 0.5 mm (0.020”).
- □ **B.** The Strobe and Data lines must be 2 – 10 cm (0.79 – 3.94”) long.
- □ **C.** Route Strobe and Data as single-ended traces, NOT as a differential pair.
- □ **D.** Space the Strobe and Data lines at least 0.65 mm (0.025”) from each other and from any other traces.
- □ **E.** Confirm that the characteristic trace impedance (Zchar) is 45 – 55 Ohm.

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2.1.2 USB2.0 SIGNALS

- □ **A.** Maintain a routing spacing to foreign traces of at least 3 times the differential spacing between high speed DP and DM. Refer to the Microchip AN 26.2 application note for additional details.
- □ **B.** The length of SuperSpeed USB differential pair traces must be within 0.13mm of each other. Refer to the Microchip AN 26.2 application note for additional details.
- □ **C.** The differential impedance of USB 2.0 signals (DP and DM) must be 90 ohms +/- 15%. Microchip suggests 90 ohms +/- 10%. Refer to the USB 2.0 specification for additional information.

2.1.3 USB3.0 SIGNALS

Note: Refer to AN 26.2 for more information on these items.

- □ **A.** The differential impedance of USB 3.0 signals (RX+/- & TX+/-) should be 90 ohms +/- 7 ohms. Refer to the USB 3.0 specification for additional information.
- □ **B.** Place 0.1uF SS_TX AC coupling capacitors near the USB connectors.
- □ **C.** Keep SuperSpeed traces as short as possible, on outer layers, and over unbroken ground planes. Traces longer than 6 inches may degrade signal quality.
- □ **D.** Maintain a routing spacing to foreign traces of at least 5 times the differential spacing between SuperSpeed lines.
- □ **E.** Eliminate or minimize the number of vias on USB3.0 signals whenever possible. The +/- signals in the each USB 3.0 differential pair can be swapped for easier routing. See the product data sheet for more information on PortSwap.
- □ **F.** The length of a SuperSpeed USB differential pair traces must be within 0.13mm of each other.

2.2 USB Hubs

- □ **A.** The VBUS path to each downstream port must be wide and have very low impedance.

2.3 Flash Media Signals

Note: Refer to the Microchip AN 18.16 application note for more information on the following items.

- □ **A.** The CRD_PWR traces must be wide enough to not produce a significant voltage drop.
- □ **B.** Unless otherwise specified in the product data sheet, route all time-sensitive media so that they are the same length, +/- 0.5 inches.
- □ **C.** Route all other traces, including other SD interface signals, at least three times the minimum trace spacing away from SD_CLK.
- □ **D.** Route all other traces, including other MS interface signals, at least three times the minimum trace spacing away from MS_CLK.
- □ **E.** Route all other traces, including other CF interface signals, at least three times the minimum trace spacing away from these traces.
- □ **F.** The multiplexed media interface signals must be routed to the connectors with minimal stubs.

2.4 USB Transceivers

- □ **A.** Processors/SoCs vary greatly in their timing specification for the ULPI bus. It is recommended to keep all ULPI traces less than 3 inches. However, consult your processor/SoC vendor for exact specifications.
- □ **B.** If deemed necessary via simulation, place a series termination resistor near the clock source. Refer to the Microchip AN 19.17 application note for additional details.
- □ **C.** Isolate the ULPI signals from adjacent signals and supplies. Refer to the Microchip AN 19.17 application note for additional details.

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APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001863A (11-13-14)	DS00001863A replaces former SMSC version Rev. 1.0 (06-26-13)	
	Section 2.1.1, HSIC Signals	Added section
Rev. 1.0 (06-26-13)	All	Initial Release

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