KSZ9021RL/RN

Gigabit Ethernet Transceiver with RGMII Support

General Description

The KSZ9021RL is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ9021RL provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000Mbps speed.

The KSZ9021RL reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

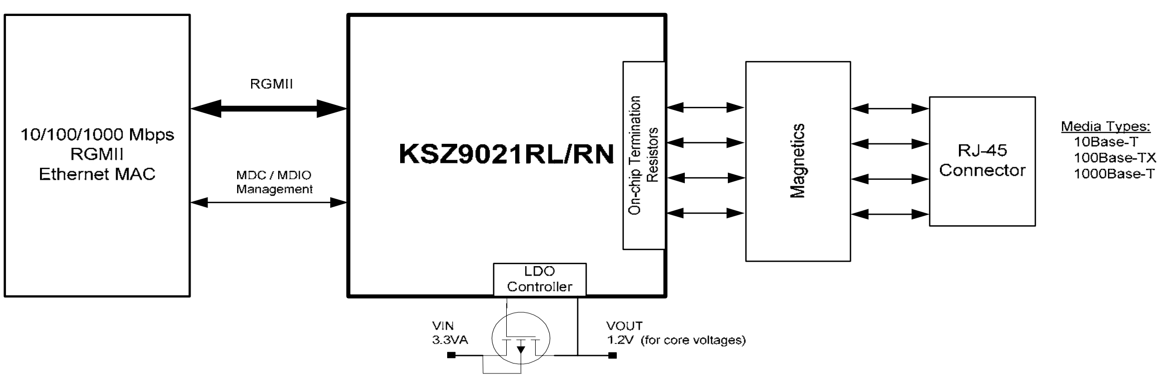
The KSZ9021RL provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9021 I/Os and board. Micrel LinkMD® TDR-based cable diagnostics permit identification of faulty copper cabling. Remote and local loopback functions provide verification of analog and digital data paths.

The KSZ9021RL is available in a 64-pin, lead-free E-LQFP package, and is offered as the KSZ9021RN in the smaller 48-pin QFN package (See Ordering Information).

Features

- Single-chip 10/100/1000Mbps IEEE 802.3 compliant Ethernet Transceiver
- RGMII interface compliant to RGMII Version 1.3
- RGMII I/Os with 3.3V/2.5V tolerant and programmable timings to adjust and correct delays on both Tx and Rx paths
- Auto-negotiation to automatically select the highest link up speed (10/100/100Mbps) and duplex (half/full)
- On-chip termination resistors for the differential pairs
- On-chip LDO controller to support single 3.3V supply operation – requires only external FET to generate 1.2V for the core
- Jumbo frame support up to 16KB
- 125MHz Reference Clock Output
- Programmable LED outputs for link, activity and speed
- Baseline Wander Correction
- LinkMD® TDR-based cable diagnostics for identification of faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and board.
- Loopback modes for diagnostics

Functional Diagram



More Features

- Automatic MDI/MDI-X crossover for detection and correction of pair swap at all speeds of operation
- Automatic detection and correction of pair swap, pair skew and pair polarity
- MDC/MDIO Management Interface for PHY register configuration
- Interrupt pin option
- Power down and power saving modes
- Operating Voltages
  - Core: 1.2V (external FET or regulator)
  - I/O: 3.3V or 2.5V
  - Transceiver: 3.3V
- Available packages
  - 64-pin E-LQFP (10mm x 10mm): KSZ9021RL
  - 48-pin QFN (7mm x 7mm): KSZ9021RN

Applications

- Laser/Network Printer
- Network Attached Storage (NAS)
- Network Server
- Gigabit LAN on Motherboard (GLOM)
- Broadband Gateway
- Gigabit SOHO/SMB Router
- IPTV
- IP Set-top Box
- Game Console
- Triple-play (data, voice, video) Media Center
- Media Converter

Ordering Information

Part Number	Temp. Range	Package	Lead Finish	Description
KSZ9021RL	0°C to 70°C	64-Pin E-LQFP	Pb-Free	RGMII, Commercial Temperature, 64-E-LQFP
KSZ9021RLI (1)	-40°C to 85°C	64-Pin E-LQFP	Pb-Free	RGMII, Industrial Temperature, 64-E-LQFP
KSZ9021RN	0°C to 70°C	48-Pin QFN	Pb-Free	RGMII, Commercial Temperature, 48-QFN
KSZ9021RNI (1)	-40°C to 85°C	48-Pin QFN	Pb-Free	RGMII, Industrial Temperature, 48-QFN

Note:

1. Contact factory for lead time.

Revision History

Revision	Date	Summary of Changes
1.0	1/16/09	Data sheet created.
1.1	10/13/09	Updated current consumption in Electrical Characteristics section. Corrected data sheet omission of register 1 bit 8 for 1000Base-T Extended Status information. Added the following register bits to provide further power saving during software power down: Tri-state all digital I/Os (reg. 258.7), LDO disable (reg. 263.15), Low frequency oscillator mode (reg. 263.8). Added KSZ9021RN device and updated entire data sheet accordingly. Added 48-Pin QFN package information.

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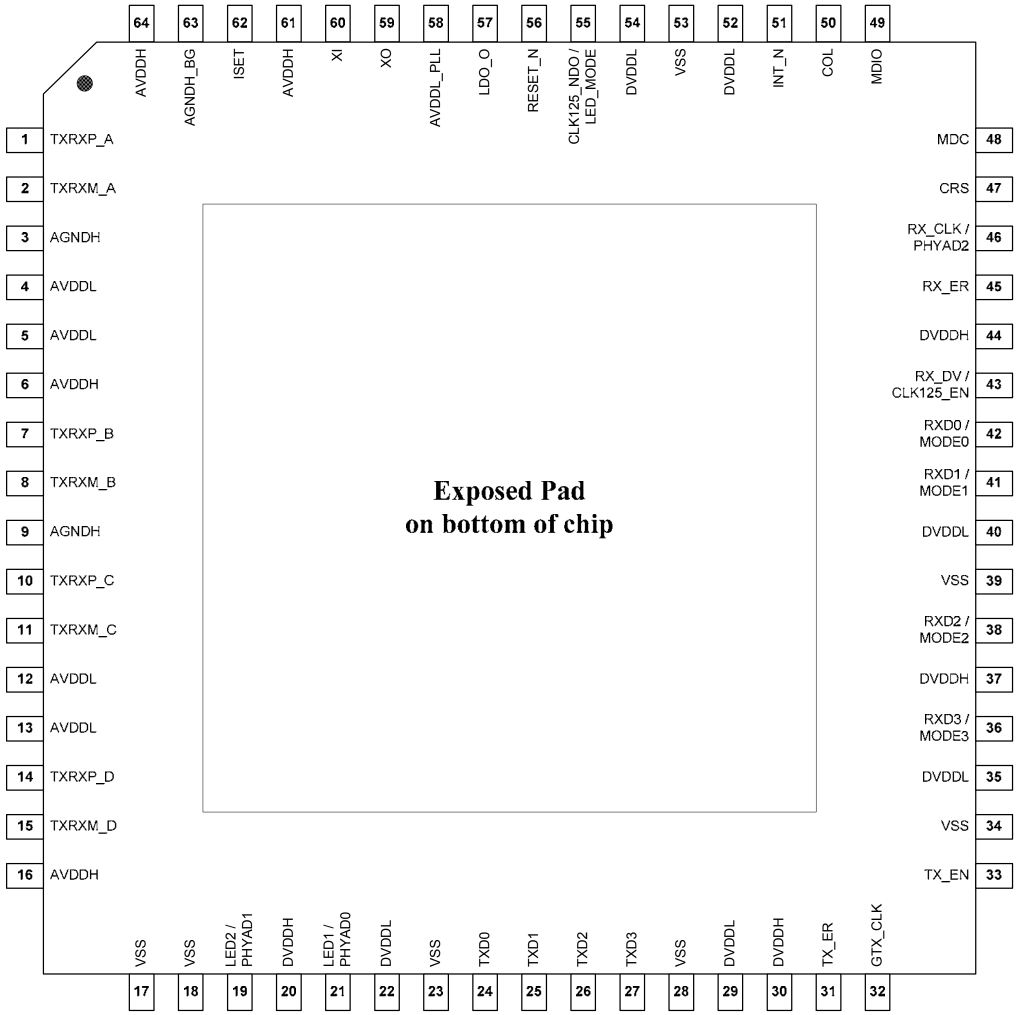
Pin Configuration – KSZ9021RL



64-Pin E-LQFP
(Top View)

Pin Description – KSZ9021RL

Pin Number	Pin Name	Type[(1)]	Pin Function
1	TXRXP_A	I/O	Media Dependent Interface[0], positive signal of differential pair 1000Base-T Mode: TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively.
2	TXRXM_A	I/O	Media Dependent Interface[0], negative signal of differential pair 1000Base-T Mode: TXRXM_A corresponds to BI_DA- for MDI configuration and BI_DB- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_A is the negative transmit signal (TX-) for MDI configuration and the negative receive signal (RX-) for MDI-X configuration, respectively.
3	AGNDH	Gnd	Analog ground
4	AVDDL	P	1.2V analog V_{DD}
5	AVDDL	P	1.2V analog V_{DD}
6	AVDDH	P	3.3V analog V_{DD}
7	TXRXP_B	I/O	Media Dependent Interface[1], positive signal of differential pair 1000Base-T Mode: TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively.
8	TXRXM_B	I/O	Media Dependent Interface[1], negative signal of differential pair 1000Base-T Mode: TXRXM_B corresponds to BI_DB- for MDI configuration and BI_DA- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_B is the negative receive signal (RX-) for MDI configuration and the negative transmit signal (TX-) for MDI-X configuration, respectively.
9	AGNDH	Gnd	Analog ground
10	TXRXP_C	I/O	Media Dependent Interface[2], positive signal of differential pair 1000Base-T Mode: TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_C is not used.
11	TXRXM_C	I/O	Media Dependent Interface[2], negative signal of differential pair 1000Base-T Mode: TXRXM_C corresponds to BI_DC- for MDI configuration and BI_DD- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_C is not used.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>12</td><td>AVDDL</td><td>P</td><td>1.2V analog V_{DD}</td></tr>
<tr><td>13</td><td>AVDDL</td><td>P</td><td>1.2V analog V_{DD}</td></tr>
<tr><td>14</td><td>TXRXP_D</td><td>I/O</td><td>Media Dependent Interface[3], positive signal of differential pair
1000Base-T Mode:
TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively.
10Base-T / 100Base-TX Mode:
TXRXP_D is not used.</td></tr>
<tr><td>15</td><td>TXRXM_D</td><td>I/O</td><td>Media Dependent Interface[3], negative signal of differential pair
1000Base-T Mode:
TXRXM_D corresponds to BI_DD- for MDI configuration and BI_DC- for MDI-X configuration, respectively.
10Base-T / 100Base-TX Mode:
TXRXM_D is not used.</td></tr>
<tr><td>16</td><td>AVDDH</td><td>P</td><td>3.3V analog V_{DD}</td></tr>
<tr><td>17</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>18</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>19</td><td>LED2 /
PHYAD1</td><td>I/O</td><td>LED Output: Programmable LED2 Output /
Config Mode: The pull-up/pull-down value is latched as PHYAD[1] during power-up / reset. See “Strapping Options” section for details.
The LED2 pin is programmed by the LED_MODE strapping option (pin 55), and is defined as follows.

Single LED Mode
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>Link off</td><td>H</td><td>OFF</td></tr>
<tr><td>Link on (any speed)</td><td>L</td><td>ON</td></tr>
</table>

Tri-color Dual LED Mode
<table>
<tr><th rowspan="2">Link / Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>

For Tri-color Dual LED Mode, LED2 works in conjunction with LED1 (pin 21) to indicate 10 Mbps Link and Activity.</td></tr>
<tr><td>20</td><td>DVDDH</td><td>P</td><td>3.3V / 2.5V digital V_{DD}</td></tr>
</table>

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[1]</th><th>Pin Function</th></tr>
<tr><td>21</td><td>LED1 /
PHYAD0</td><td>I/O</td><td>LED Output: Programmable LED1 Output /
Config Mode: The pull-up/pull-down value is latched as PHYAD[0] during power-up / reset. See “Strapping Options” section for details.
The LED1 pin is programmed by the LED_MODE strapping option (pin 55), and is defined as follows.

Single LED Mode
<table><tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No Activity</td><td>H</td><td>OFF</td></tr><tr><td>Activity (RX, TX)</td><td>Toggle</td><td>Blinking</td></tr></table>
Tri-color Dual LED Mode
<table><tr><th rowspan="2">Link / Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr><tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr><tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr><tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr><tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr><tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr><tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr><tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr><tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr></table>
For Tri-color Dual LED Mode, LED1 works in conjunction with LED2 (pin 19) to indicate 10 Mbps Link and Activity.</td></tr>
<tr><td>22</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>23</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>RGMII Mode: RGMII TD0 (Transmit Data 0) Input</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>RGMII Mode: RGMII TD1 (Transmit Data 1) Input</td></tr>
<tr><td>26</td><td>TXD2</td><td>I</td><td>RGMII Mode: RGMII TD2 (Transmit Data 2) Input</td></tr>
<tr><td>27</td><td>TXD3</td><td>I</td><td>RGMII Mode: RGMII TD3 (Transmit Data 3) Input</td></tr>
<tr><td>28</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>29</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>30</td><td>DVDDH</td><td>P</td><td>3.3V / 2.5V digital V_{DD}</td></tr>
<tr><td>31</td><td>TX_ER</td><td>I</td><td>RGMII Mode: This pin is not used and should be left as a no connect.</td></tr>
<tr><td>32</td><td>GTX_CLK</td><td>I</td><td>RGMII Mode: RGMII TXC (Transmit Reference Clock) Input</td></tr>
<tr><td>33</td><td>TX_EN</td><td>I</td><td>RGMII Mode: RGMII TX_CTL (Transmit Control) Input</td></tr>
<tr><td>34</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>35</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
</table>

Pin Number	Pin Name	Type[1]	Pin Function
36	RXD3 / MODE3	I/O	RGMII Mode: RGMII RD3 (Receive Data 3) Output / Config Mode: The pull-up/pull-down value is latched as MODE3 during power-up / reset. See “Strapping Options” section for details.
37	DVDDH	P	3.3V / 2.5V digital V_{DD}
38	RXD2 / MODE2	I/O	RGMII Mode: RGMII RD2 (Receive Data 2) Output / Config Mode: The pull-up/pull-down value is latched as MODE2 during power-up / reset. See “Strapping Options” section for details.
39	VSS	Gnd	Digital ground
40	DVDDL	P	1.2V digital V_{DD}
41	RXD1 / MODE1	I/O	RGMII Mode: RGMII RD1 (Receive Data 1) Output / Config Mode: The pull-up/pull-down value is latched as MODE1 during power-up / reset. See “Strapping Options” section for details.
42	RXD0 / MODE0	I/O	RGMII Mode: RGMII RD0 (Receive Data 0) Output / Config Mode: The pull-up/pull-down value is latched as MODE0 during power-up / reset. See “Strapping Options” section for details.
43	RX_DV / CLK125_EN	I/O	RGMII Mode: RGMII RX_CTL (Receive Control) Output / Config Mode: Latched as CLK125_NDO Output Enable during power-up / reset. See “Strapping Options” section for details.
44	DVDDH	P	3.3V / 2.5V digital V_{DD}
45	RX_ER	O	RGMII Mode: This pin is not used and should be left as a no connect.
46	RX_CLK / PHYAD2	I/O	RGMII Mode: RGMII RXC (Receive Reference Clock) Output / Config Mode: The pull-up/pull-down value is latched as PHYAD[2] during power-up / reset. See “Strapping Options” section for details.
47	CRS	O	RGMII Mode: This pin is not used and should be left as a no connect.
48	MDC	Ipu	Management Data Clock Input This pin is the input reference clock for MDIO (pin 49).
49	MDIO	Ipu/O	Management Data Input / Output This pin is synchronous to MDC (pin 48) and requires an external pull-up resistor to 3.3V digital V_{DD} in a range from 1.0KΩ to 4.7KΩ.
50	COL	O	RGMII Mode: This pin is not used and should be left as a no connect.
51	INT_N	O	Interrupt Output This pin provides a programmable interrupt output and requires an external pull-up resistor to 3.3V digital V_{DD} in a range from 1.0KΩ to 4.7KΩ when active low. Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 14 sets the interrupt output to active low (default) or active high.
52	DVDDL	P	1.2V digital V_{DD}
53	VSS	Gnd	Digital ground
54	DVDDL	P	1.2V digital V_{DD}
55	CLK125_NDO / LED_MODE	I/O	125MHz Clock Output This pin provides a 125MHz reference clock output option for use by the MAC. / Config Mode: The pull-up/pull-down value is latched as LED_MODE during power-up / reset. See “Strapping Options” section for details.

Pin Number	Pin Name	Type[(1)]	Pin Function
56	RESET_N	Ipu	Chip Reset (active low) Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See "Strapping Options" section for more details.
57	LDO_O	O	On-chip 1.2V LDO Controller Output This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip's core voltages. If 1.2V is provided by the system and this pin is not used, it can be left floating.
58	AVDDL_PLL	P	1.2V analog V_{DD} for PLL
59	XO	O	25MHz Crystal feedback This pin is a no connect if oscillator or external clock source is used.
60	XI	I	Crystal / Oscillator / External Clock Input 25MHz +/-50ppm tolerance
61	AVDDH	P	3.3V analog V_{DD}
62	ISET	I/O	Set transmit output level Connect a 4.99KΩ 1% resistor to ground on this pin.
63	AGNDH_BG	Gnd	Analog ground
64	AVDDH	P	3.3V analog V_{DD}
E-PAD	E-PAD	Gnd	Exposed Pad on bottom of chip Connect E-PAD to ground.

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up.
   Ipu/O = Input with internal pull-up / Output.

Strapping Options – KSZ9021RL

Pin Number	Pin Name	Type[(1)]	Pin Function
46 19 21	PHYAD2 PHYAD1 PHYAD0	I/O I/O I/O	The PHY Address, PHYAD[2:0], is latched at power-up / reset and is configurable to any value from 1 to 7. Each PHY address bit is configured as follows: Pull-up = 1 Pull-down = 0 PHY Address bits [4:3] are always set to '00'.
36 38 41 42	MODE3 MODE2 MODE1 MODE0	I/O I/O I/O I/O	The MODE[3:0] strap-in pins are latched at power-up / reset and are defined as follows: (see MODE[3:0] table below)
43	CLK125_EN	I/O	CLK125_EN is latched at power-up / reset and is defined as follows: Pull-up = Enable 125MHz Clock Output Pull-down = Disable 125MHz Clock Output Pin 55 (CLK125_NDO) provides the 125MHz reference clock output option for use by the MAC.
55	LED_MODE	I/O	LED_MODE is latched at power-up / reset and is defined as follows: Pull-up = Single LED Mode Pull-down = Tri-color Dual LED Mode

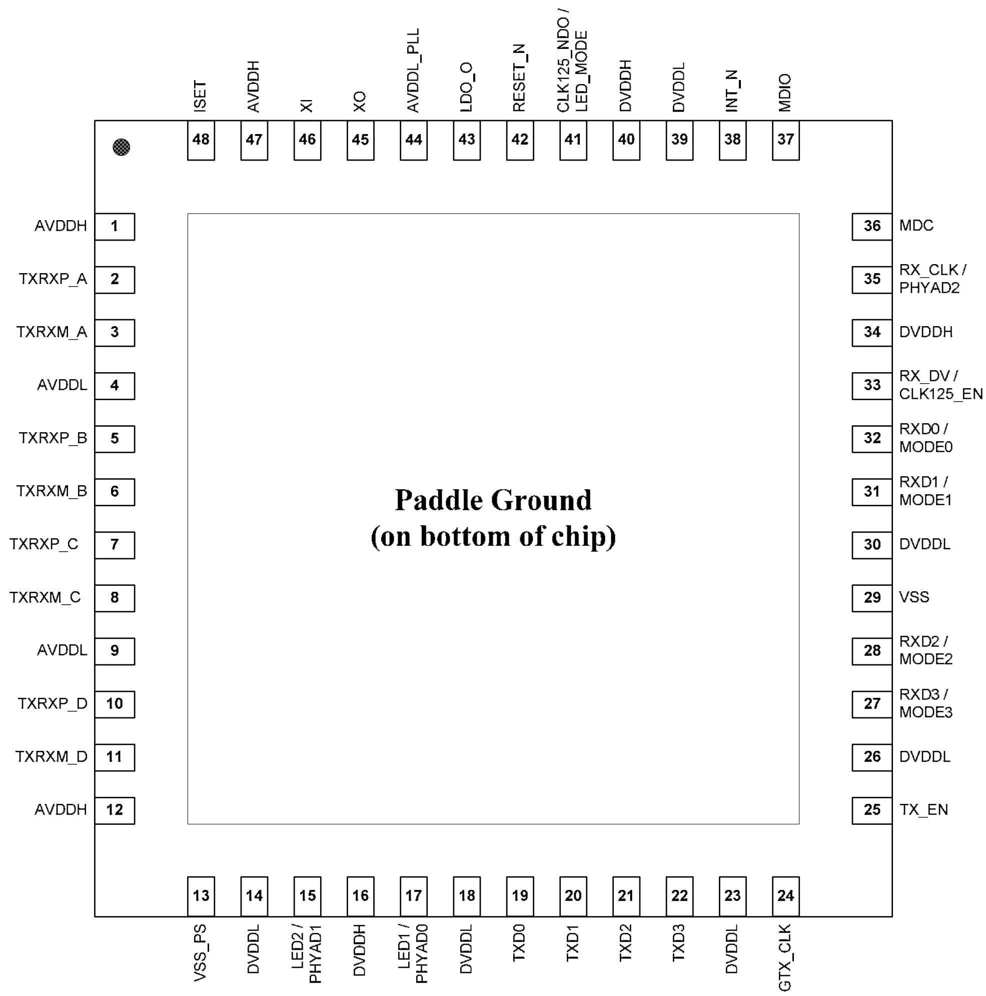
MODE[3:0]	Mode
0000	Reserved – not used
0001	Reserved – not used
0010	Reserved – not used
0011	Reserved – not used
0100	NAND Tree Mode
0101	Reserved – not used
0110	Reserved – not used
0111	Chip Power Down Mode
1000	Reserved – not used
1001	Reserved – not used
1010	Reserved – not used
1011	Reserved – not used
1100	RGMII Mode – advertise 1000Base-T full-duplex only
1101	RGMII Mode – advertise 1000Base-T full and half-duplex only
1110	RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex),except 1000Base-T half-duplex
1111	RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex)

Note:

1. I/O = Bi-directional.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during power-up or reset, and consequently cause the PHY strap-in pins on the RGMII signals to be latched to the incorrect configuration. In this case, it is recommended to add external pull-ups/pull-downs on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

Pin Configuration – KSZ9021RN



48-Pin QFN
(Top View)

Pin Description – KSZ9021RN

Pin Number	Pin Name	Type(1)	Pin Function
1	AVDDH	P	3.3V analog V_{DD}
2	TXRXP_A	I/O	Media Dependent Interface[0], positive signal of differential pair 1000Base-T Mode: TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively.
3	TXRXM_A	I/O	Media Dependent Interface[0], negative signal of differential pair 1000Base-T Mode: TXRXM_A corresponds to BI_DA- for MDI configuration and BI_DB- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_A is the negative transmit signal (TX-) for MDI configuration and the negative receive signal (RX-) for MDI-X configuration, respectively.
4	AVDDL	P	1.2V analog V_{DD}
5	TXRXP_B	I/O	Media Dependent Interface[1], positive signal of differential pair 1000Base-T Mode: TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively.
6	TXRXM_B	I/O	Media Dependent Interface[1], negative signal of differential pair 1000Base-T Mode: TXRXM_B corresponds to BI_DB- for MDI configuration and BI_DA- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_B is the negative receive signal (RX-) for MDI configuration and the negative transmit signal (TX-) for MDI-X configuration, respectively.
7	TXRXP_C	I/O	Media Dependent Interface[2], positive signal of differential pair 1000Base-T Mode: TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_C is not used.
8	TXRXM_C	I/O	Media Dependent Interface[2], negative signal of differential pair 1000Base-T Mode: TXRXM_C corresponds to BI_DC- for MDI configuration and BI_DD- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_C is not used.
9	AVDDL	P	1.2V analog V_{DD}

Pin Number	Pin Name	Type[(1)]	Pin Function
10	TXRXP_D	I/O	Media Dependent Interface[3], positive signal of differential pair 1000Base-T Mode: TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_D is not used.
11	TXRXM_D	I/O	Media Dependent Interface[3], negative signal of differential pair 1000Base-T Mode: TXRXM_D corresponds to BI_DD- for MDI configuration and BI_DC- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_D is not used.
12	AVDDH	P	3.3V analog V_{DD}
13	VSS_PS	Gnd	Digital ground
14	DVDDL	P	1.2V digital V_{DD}
15	LED2 / PHYAD1	I/O	LED Output: Programmable LED2 Output / Config Mode: The pull-up/pull-down value is latched as PHYAD[1] during power-up / reset. See “Strapping Options” section for details. The LED2 pin is programmed by the LED_MODE strapping option (pin 41), and is defined as follows.

Single LED Mode

Link	Pin State	LED Definition
Link off	H	OFF
Link on (any speed)	L	ON

Tri-color Dual LED Mode

Link / Activity	Pin State		LED Definition	
	LED2	LED1	LED2	LED1
Link off	H	H	OFF	OFF
1000 Link / No Activity	L	H	ON	OFF
1000 Link / Activity (RX, TX)	Toggle	H	Blinking	OFF
100 Link / No Activity	H	L	OFF	ON
100 Link / Activity (RX, TX)	H	Toggle	OFF	Blinking
10 Link / No Activity	L	L	ON	ON
10 Link / Activity (RX, TX)	Toggle	Toggle	Blinking	Blinking

For Tri-color Dual LED Mode, LED2 works in conjunction with LED1 (pin 17) to indicate 10 Mbps Link and Activity.

Pin Number	Pin Name	Type[(1)]	Pin Function
16	DVDDH	P	3.3V / 2.5V digital V_{DD}

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[1]</th><th>Pin Function</th></tr>
<tr><td>17</td><td>LED1 /
PHYAD0</td><td>I/O</td><td>LED Output: Programmable LED1 Output /
Config Mode: The pull-up/pull-down value is latched as PHYAD[0] during power-up / reset. See “Strapping Options” section for details.
The LED1 pin is programmed by the LED_MODE strapping option (pin 41), and is defined as follows.

Single LED Mode
<table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity (RX, TX)</td><td>Toggle</td><td>Blinking</td></tr>
</table>

Tri-color Dual LED Mode
<table>
<tr><th rowspan="2">Link / Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>

For Tri-color Dual LED Mode, LED1 works in conjunction with LED2 (pin 15) to indicate 10 Mbps Link and Activity.</td></tr>
<tr><td>18</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>19</td><td>TXD0</td><td>I</td><td>RGMII Mode: RGMII TD0 (Transmit Data 0) Input</td></tr>
<tr><td>20</td><td>TXD1</td><td>I</td><td>RGMII Mode: RGMII TD1 (Transmit Data 1) Input</td></tr>
<tr><td>21</td><td>TXD2</td><td>I</td><td>RGMII Mode: RGMII TD2 (Transmit Data 2) Input</td></tr>
<tr><td>22</td><td>TXD3</td><td>I</td><td>RGMII Mode: RGMII TD3 (Transmit Data 3) Input</td></tr>
<tr><td>23</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>24</td><td>GTX_CLK</td><td>I</td><td>RGMII Mode: RGMII TXC (Transmit Reference Clock) Input</td></tr>
<tr><td>25</td><td>TX_EN</td><td>I</td><td>RGMII Mode: RGMII TX_CTL (Transmit Control) Input</td></tr>
<tr><td>26</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>27</td><td>RXD3 /
MODE3</td><td>I/O</td><td>RGMII Mode: RGMII RD3 (Receive Data 3) Output /
Config Mode: The pull-up/pull-down value is latched as MODE3 during power-up / reset. See “Strapping Options” section for details.</td></tr>
<tr><td>28</td><td>RXD2 /
MODE2</td><td>I/O</td><td>RGMII Mode: RGMII RD2 (Receive Data 2) Output /
Config Mode: The pull-up/pull-down value is latched as MODE2 during power-up / reset. See “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>30</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>31</td><td>RXD1 /
MODE1</td><td>I/O</td><td>RGMII Mode: RGMII RD1 (Receive Data 1) Output /
Config Mode: The pull-up/pull-down value is latched as MODE1 during power-up / reset. See “Strapping Options” section for details.</td></tr>
</table>

Pin Number	Pin Name	Type[(1)]	Pin Function
32	RXD0 / MODE0	I/O	RGMII Mode: RGMII RD0 (Receive Data 0) Output / Config Mode: The pull-up/pull-down value is latched as MODE0 during power-up / reset. See "Strapping Options" section for details.
33	RX_DV / CLK125_EN	I/O	RGMII Mode: RGMII RX_CTL (Receive Control) Output / Config Mode: Latched as CLK125_NDO Output Enable during power-up / reset. See "Strapping Options" section for details.
34	DVDDH	P	3.3V / 2.5V digital V_{DD}
35	RX_CLK / PHYAD2	I/O	RGMII Mode: RGMII RXC (Receive Reference Clock) Output / Config Mode: The pull-up/pull-down value is latched as PHYAD[2] during power-up / reset. See "Strapping Options" section for details.
36	MDC	Ipu	Management Data Clock Input This pin is the input reference clock for MDIO (pin 37).
37	MDIO	Ipu/O	Management Data Input / Output This pin is synchronous to MDC (pin 36) and requires an external pull-up resistor to 3.3V digital V_{DD} in a range from 1.0KΩ to 4.7KΩ.
38	INT_N	O	Interrupt Output This pin provides a programmable interrupt output and requires an external pull-up resistor to 3.3V digital V_{DD} in a range from 1.0KΩ to 4.7KΩ when active low. Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 14 sets the interrupt output to active low (default) or active high.
39	DVDDL	P	1.2V digital V_{DD}
40	DVDDH	P	3.3V / 2.5V digital V_{DD}
41	CLK125_NDO / LED_MODE	I/O	125MHz Clock Output This pin provides a 125MHz reference clock output option for use by the MAC. / Config Mode: The pull-up/pull-down value is latched as LED_MODE during power-up / reset. See "Strapping Options" section for details.
42	RESET_N	Ipu	Chip Reset (active low) Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See "Strapping Options" section for more details.
43	LDO_O	O	On-chip 1.2V LDO Controller Output This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip's core voltages. If 1.2V is provided by the system and this pin is not used, it can be left floating.
44	AVDDL_PLL	P	1.2V analog V_{DD} for PLL
45	XO	O	25MHz Crystal feedback This pin is a no connect if oscillator or external clock source is used.
46	XI	I	Crystal / Oscillator / External Clock Input 25MHz +/-50ppm tolerance
47	AVDDH	P	3.3V analog V_{DD}
48	ISET	I/O	Set transmit output level Connect a 4.99KΩ 1% resistor to ground on this pin.
PADDLE	P_GND	Gnd	Exposed Paddle on bottom of chip Connect P_GND to ground.

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up.
   Ipu/O = Input with internal pull-up / Output.

Strapping Options – KSZ9021RN

Pin Number	Pin Name	Type[(1)]	Pin Function
35 15 17	PHYAD2 PHYAD1 PHYAD0	I/O I/O I/O	The PHY Address, PHYAD[2:0], is latched at power-up / reset and is configurable to any value from 1 to 7. Each PHY address bit is configured as follows: Pull-up = 1 Pull-down = 0 PHY Address bits [4:3] are always set to '00'.
27 28 31 32	MODE3 MODE2 MODE1 MODE0	I/O I/O I/O I/O	The MODE[3:0] strap-in pins are latched at power-up / reset and are defined as follows: (see MODE table below)
33	CLK125_EN	I/O	CLK125_EN is latched at power-up / reset and is defined as follows: Pull-up = Enable 125MHz Clock Output Pull-down = Disable 125MHz Clock Output Pin 41 (CLK125_NDO) provides the 125MHz reference clock output option for use by the MAC.
41	LED_MODE	I/O	LED_MODE is latched at power-up / reset and is defined as follows: Pull-up = Single LED Mode Pull-down = Tri-color Dual LED Mode

MODE[3:0]	Mode
0000	Reserved – not used
0001	Reserved – not used
0010	Reserved – not used
0011	Reserved – not used
0100	NAND Tree Mode
0101	Reserved – not used
0110	Reserved – not used
0111	Chip Power Down Mode
1000	Reserved – not used
1001	Reserved – not used
1010	Reserved – not used
1011	Reserved – not used
1100	RGMII Mode – advertise 1000Base-T full-duplex only
1101	RGMII Mode – advertise 1000Base-T full and half-duplex only
1110	RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex),except 1000Base-T half-duplex
1111	RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex)

Note:

1. I/O = Bi-directional.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during power-up or reset, and consequently cause the PHY strap-in pins on the RGMII signals to be latched to the incorrect configuration. In this case, it is recommended to add external pull-ups/pull-downs on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

Functional Overview

The KSZ9021RL/RN is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver solution for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable. Its on-chip proprietary 1000Base-T transceiver and Manchester/MLT-3 signaling-based 10Base-T/100Base-TX transceivers are all IEEE 802.3 compliant.

The KSZ9021RL/RN reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9021RL/RN can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

The KSZ9021RL/RN provides the RGMII interface for a direct and seamless connection to RGMII MACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000Mbps speed.

The following figure shows a high-level block diagram of the KSZ9021RL/RN.

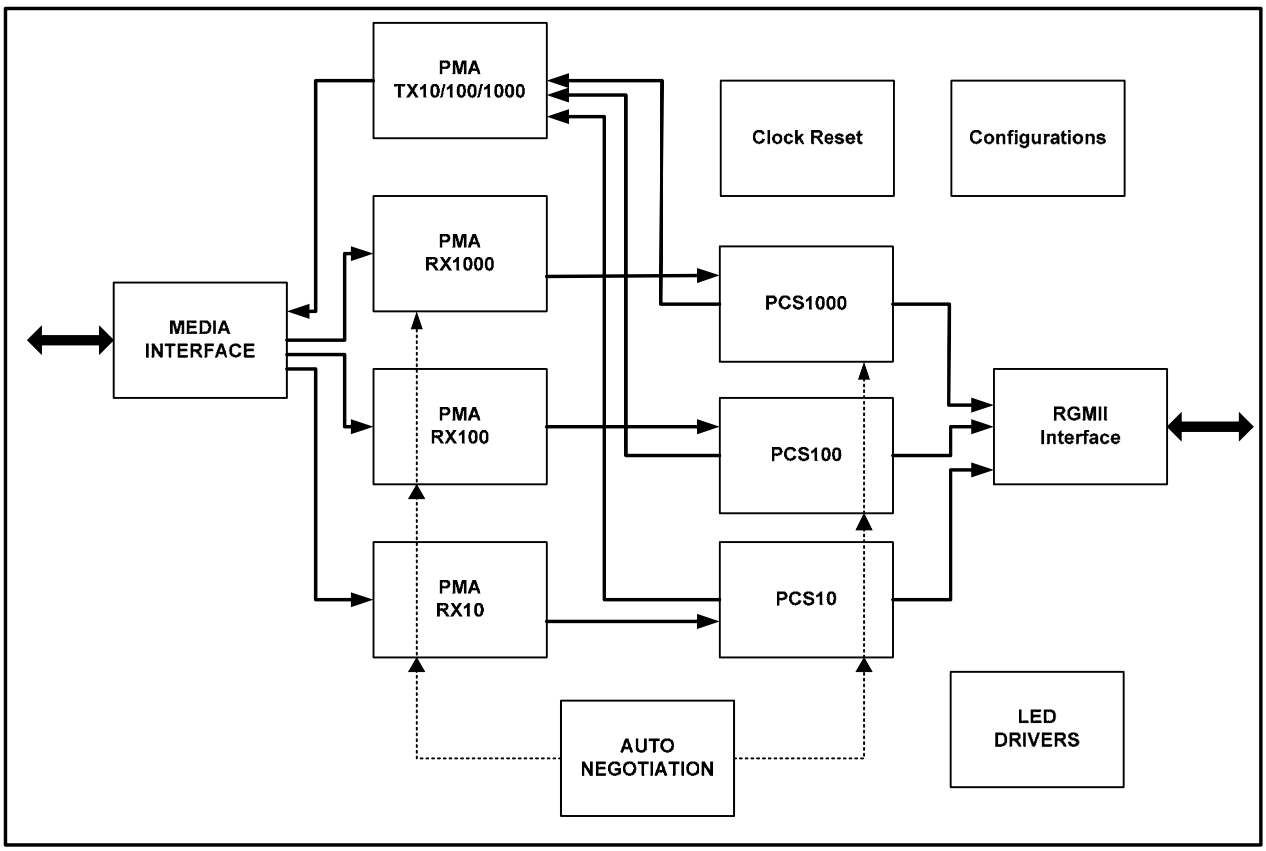


Figure 1. KSZ9021RL/RN Block Diagram

Functional Description: 10Base-T/100Base-TX Transceiver

100Base-TX Transmit

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the RGMII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 4.99KΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

100Base-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the RGMII format and provided as the input data to the MAC.

Scrambler/De-scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

10Base-T Transmit

The output 10Base-T driver is incorporated into the 100Base-TX driver to allow transmission with the same magnetic. They are internally wave-shaped and pre-emphasized into typical outputs of 2.5V amplitude. The harmonic contents are at least 31 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths in order to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9021RL/RN decodes a data frame. The receiver clock is maintained active during idle periods in between receiving data frames.

Functional Description: 1000Base-T Transceiver

The 1000Base-T transceiver is based on a mixed-signal/digital signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancellers, cross-talk cancellers, precision clock recovery scheme, and power efficient line drivers.

The following figure shows a high-level block diagram of a single channel of the 1000Base-T transceiver for one of the four differential pairs.

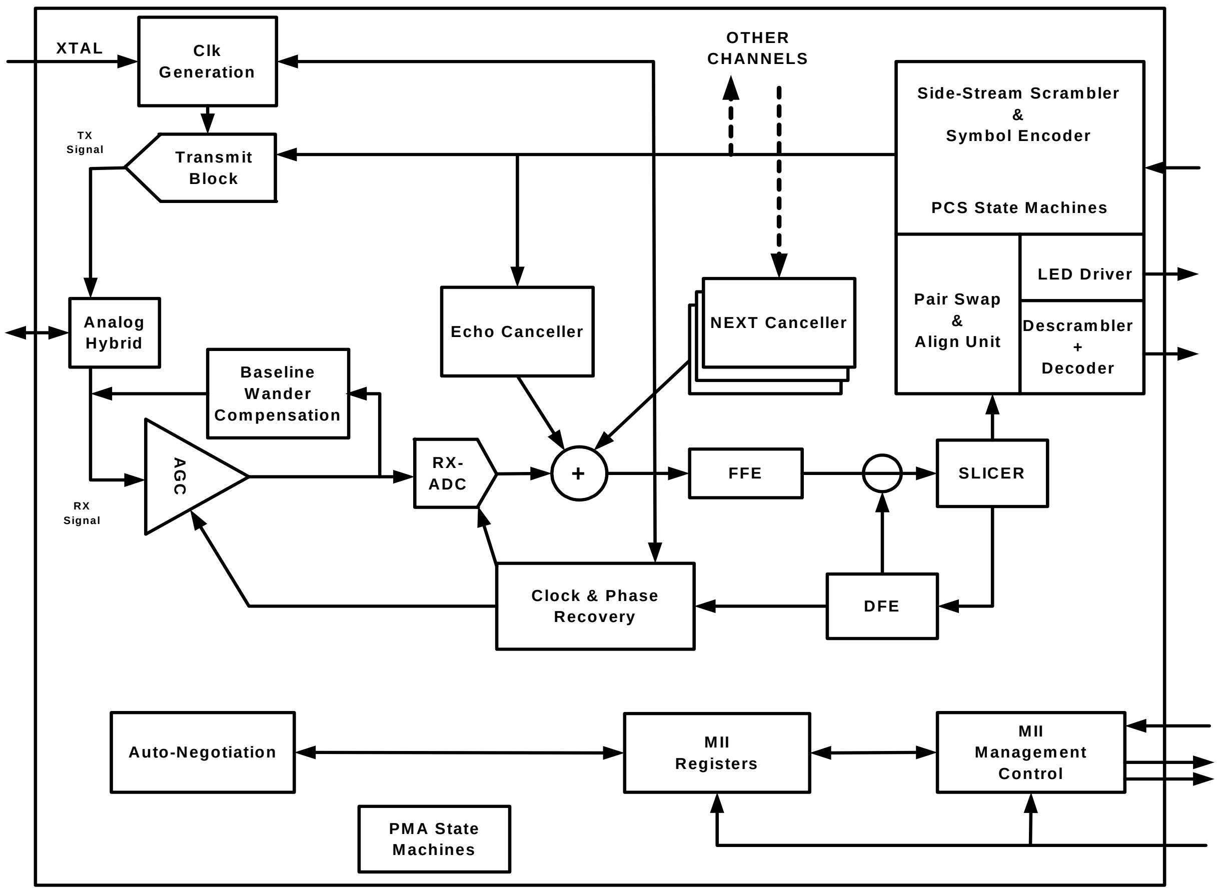


Figure 2. KSZ9021RL/RN 1000Base-T Block Diagram – Single Channel

Analog Echo Cancellation Circuit

In 1000Base-T mode, the analog echo cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10Base-T/100Base-TX mode.

Automatic Gain Control (AGC)

In 1000Base-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

Analog-to-Digital Converter (ADC)

In 1000Base-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10Base-T/100Base-TX mode.

Timing Recovery Circuit

In 1000Base-T mode, the mixed-signal clock recovery circuit, together with the digital phase locked loop, is used to recover and track the incoming timing information from the received data. The digital phase locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000Base-T slave PHY is required to transmit the exact receive clock frequency recovered from the received data back to the 1000Base-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. Additionally, this helps to facilitate echo cancellation and NEXT removal.

Adaptive Equalizer

In 1000Base-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid and echo due to impedance mismatch. The KSZ9021RL/RN employs a digital echo canceller to further reduce echo components on the receive signal.

In 1000Base-T mode, the data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high frequency cross-talk coming from adjacent wires. The KSZ9021RL/RN employs three NEXT cancellers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10Base-T/100Base-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

Trellis Encoder and Decoder

In 1000Base-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9021RL/RN is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order and polarity have to be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and then de-scrambled into 8-bit data.

Functional Description: 10/100/1000 Transceiver Features

Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9021RL/RN and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and then assigns the MDI/MDI-X pair mapping of the KSZ9021RL/RN accordingly.

The following table shows the KSZ9021RL/RN 10/100/1000 pin-out assignments for MDI/MDI-X pin mapping.

Pin (RJ-45 pair)	MDI			MDI-X		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
TXRXP/M_A (1,2)	A+/-	TX+/-	TX+/-	B+/-	RX+/-	RX+/-
TXRXP/M_B (3,6)	B+/-	RX+/-	RX+/-	A+/-	TX+/-	TX+/-
TXRXP/M_C (4,5)	C+/-	Not used	Not used	D+/-	Not used	Not used
TXRXP/M_D (7,8)	D+/-	Not used	Not used	C+/-	Not used	Not used

Table 1. MDI / MDI-X Pin Mapping

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to register 28 (1Ch) bit 6. MDI and MDI-X mode is set by register 28 (1Ch) bit 7 if auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X.

Pair- Swap, Alignment, and Polarity Check

In 1000Base-T mode, the KSZ9021RL/RN

- Detects incorrect channel order and automatically restore the pair order for the A, B, C, D pairs (four channels)
- Supports 50±10ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected 4-pairs of data symbols are synchronized

Incorrect pair polarities of the differential signals are automatically corrected for all speeds.

Wave Shaping, Slew Rate Control and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000Base-T, a special partial response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100Base-TX, a simple slew rate control method is used to minimize EMI.
- For 10Base-T, pre-emphasis is used to extend the signal quality through the cable.

PLL Clock Synthesizer

The KSZ9021RL/RN generates 125MHz, 25MHz and 10MHz clocks for system timing. Internal clocks are generated from the external 25MHz crystal or reference clock.

Auto-Negotiation

The KSZ9021RL/RN conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (Unshielded Twisted Pair) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 1000Base-T, full-duplex
- Priority 2: 1000Base-T, half-duplex
- Priority 3: 100Base-TX, full-duplex
- Priority 4: 100Base-TX, half-duplex
- Priority 5: 10Base-T, full-duplex
- Priority 6: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ9021RL/RN link partner is forced to bypass auto-negotiation for 10Base-T and 100Base-TX modes, then the KSZ9021RL/RN sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the KSZ9021RL/RN to establish a link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The auto-negotiation link up process is shown in the following flow chart.

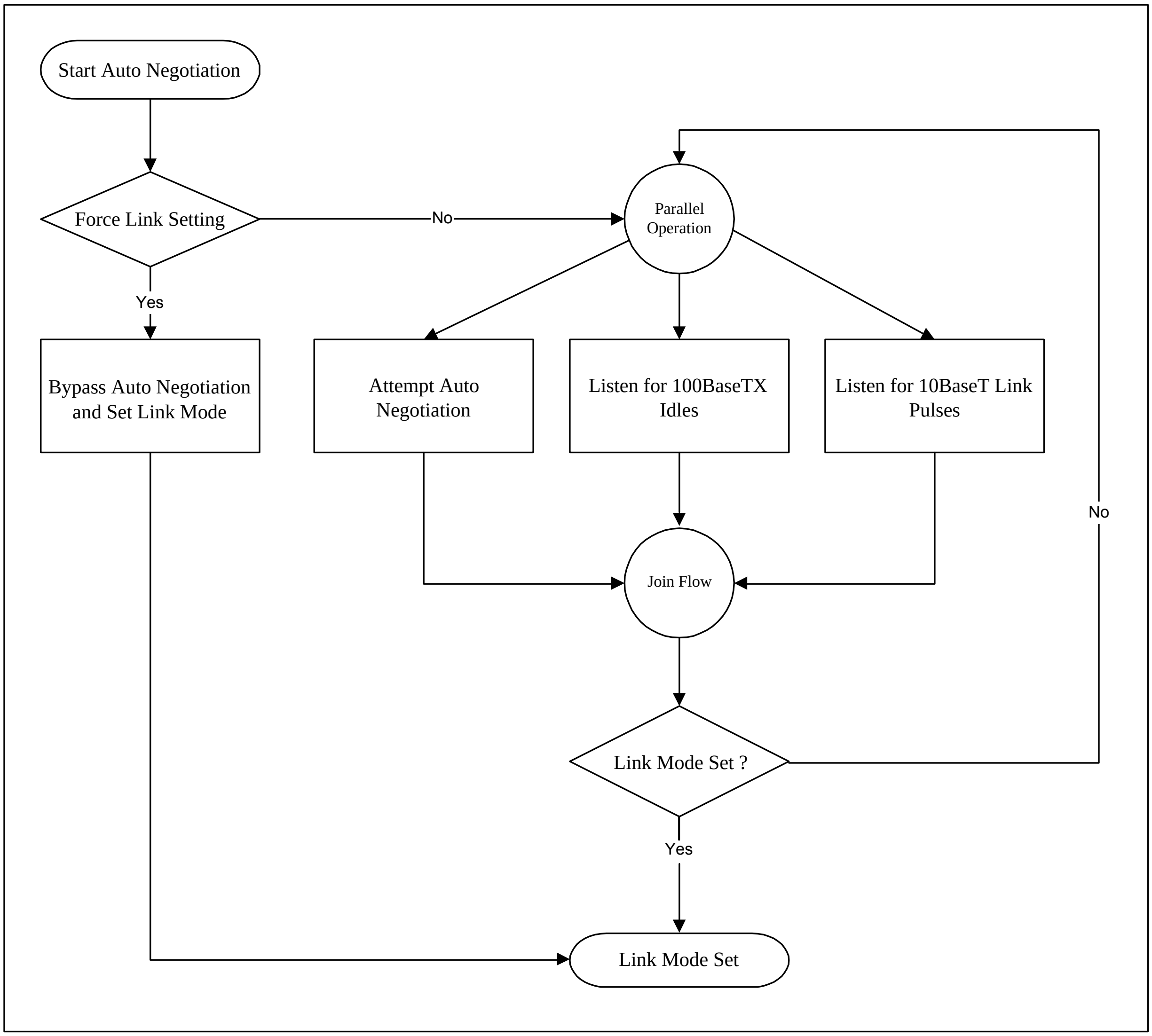


Figure 3. Auto-Negotiation Flow Chart

For 1000Base-T mode, auto-negotiation is required and always used to establish link. During 1000Base-T auto-negotiation, Master and Slave configuration is first resolved between link partners, and then link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default at power-up or after hardware reset. Afterwards, auto-negotiation can be enabled or disabled through register 0 bit 12. If auto-negotiation is disabled, then the speed is set by register 0 bits 6 and 13, and the duplex is set by register 0 bit 8.

If the speed is changed on the fly, then the link goes down and either auto-negotiation or parallel detection will initiate until a common speed between KSZ9021RL/RN and its link partner is re-established for link.

If link is already established, and there is no change of speed on the fly, then the changes will not take effect unless either auto-negotiation is restarted through register 0 bit 9, or a link down to link up transition occurs (i.e., disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in register 1 and the link partner capabilities are updated in registers 5, 6, and 10.

The auto-negotiation finite state machines employ interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions are summarized in the following table.

Auto-Negotiation Interval Timers	Time Duration
Transmit Burst interval	16 ms
Transmit Pulse interval	68 us
FLP detect minimum time	17.2 us
FLP detect maximum time	185 us
Receive minimum Burst interval	6.8 ms
Receive maximum Burst interval	112 ms
Data detect minimum interval	35.4 us
Data detect maximum interval	95 us
NLP test minimum interval	4.5 ms
NLP test maximum interval	30 ms
Link Loss time	52 ms
Break Link time	1480 ms
Parallel Detection wait time	830 ms
Link Enable wait time	1000 ms

Table 2. Auto-Negotiation Timers

RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) is compliant with the RGMII Version 1.3 Specification. It provides a common interface between RGMII PHYs and MACs, and has the following key characteristics:

- Pin count is reduced from 24 pins for the IEEE Gigabit Media Independent Interface (GMII) to 12 pins for RGMII.
- All speeds (10Mbps, 100Mbps, and 1000Mbps) are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4-bit wide, a nibble.

In RGMII operation, the RGMII pins function as follow:

- The MAC sources the transmit reference clock, TXC, at 125MHz for 1000Mbps, 25MHz for 100Mbps and 2.5MHz for 10Mbps.
- The PHY recovers and sources the receive reference clock, RXC, at 125MHz for 1000Mbps, 25MHz for 100Mbps and 2.5MHz for 10Mbps.
- For 1000Base-T, the transmit data, TXD[3:0], is presented on both edges of TXC, and the received data, RXD[3:0], is clocked out on both edges of the recovered 125 MHz clock, RXC.
- For 10Base-T/100Base-TX, the MAC will hold TX_CTL low until both PHY and MAC operate at the same speed. During the speed transition, the receive clock will be stretched on either positive or negative pulse to ensure that no clock glitch is presented to the MAC at any time.
- TX_ER and RX_ER are combined with TX_EN and RX_DV, respectively, to form TX_CTL and RX_CTL. These two RGMII control signals are valid at the falling clock edge.

After power-up or reset, the KSZ9021RL/RN is configured to RGMII mode if the MODE[3:0] strap-in pins are set to one of the RGMII mode capability options. See Strapping Options section for available options.

The KSZ9021RL/RN has the option to output a low jitter 125MHz reference clock on the CLK125_NDO pin. This clock provides a lower cost reference clock alternative for RGMII MACs that require a 125MHz crystal or oscillator. The 125MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

RGMII Signal Definition

The following table describes the RGMII signals. Refer to the RGMII Version 1.3 Specification for more detailed information.

RGMII Signal Name (per spec)	RGMII Signal Name (per KSZ9021RL/RN)	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
TXC	GTX_CLK	Input	Output	Transmit Reference Clock (125MHz for 1000Mbps, 25MHz for 100Mbps, 2.5MHz for 10Mbps)
TX_CTL	TX_EN	Input	Output	Transmit Control
TXD[3:0]	TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	RX_CLK	Output	Input	Receive Reference Clock (125MHz for 1000Mbps, 25MHz for 100Mbps, 2.5MHz for 10Mbps)
RX_CTL	RX_DV	Output	Input	Receive Control
RXD[3:0]	RXD[3:0]	Output	Input	Receive Data [3:0]

Table 3. RGMII Signal Definition

RGMII Signal Diagram

The KSZ9021RL/RN RGMII pin connections to the MAC are shown in the following figure.

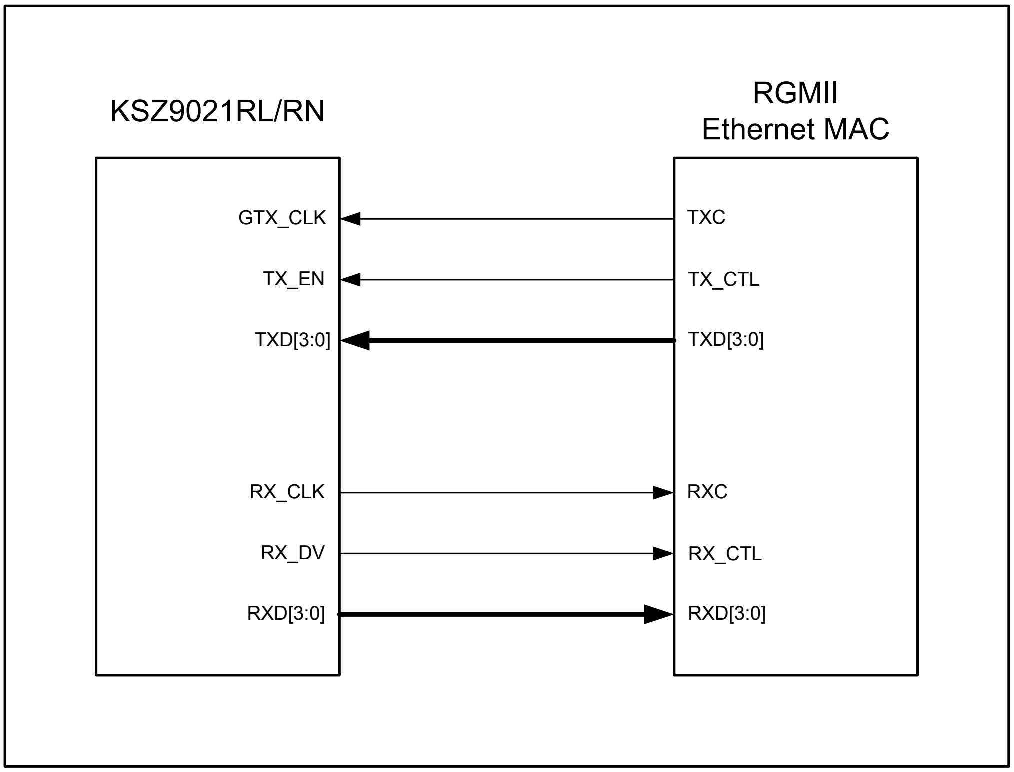


Figure 4. KSZ9021RL/RN RGMII Interface

RGMII In-band Status

The KSZ9021RL/RN can provide in-band status to the MAC during the inter-frame gap when RX_DV is de-asserted. RGMII in-band status is disabled by default. It is enabled by writing a one to extended register 256 (100h) bit 8.

The in-band status is sent to the MAC using the RXD[3:0] data pins, and is described in the following table.

RX_DV	RXD3	RXD[2:1]	RXD0
0 (valid only when RX_DV is low and register 256 bit 8 is set to 1)	Duplex Status 0 = half-duplex 1 = full-duplex	RX_CLK clock speed 00 =2.5MHz 01 =25MHz 10 =125MHz 11 = reserved	Link Status 0 = Link down 1 = Link up

Table 4. RGMII In-Band Status

MII Management (MIIM) Interface

The KSZ9021RL/RN supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ9021RL/RN. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further detail on the MIIM interface can be found in Clause 22.2.4.5 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with one or more KSZ9021RL/RN device. Each KSZ9021RL/RN device is assigned a PHY address between 1 and 7 by the PHYAD[2:0] strapping pins.
- A 32 register address space to access the KSZ9021RL/RN IEEE Defined Registers, Vendor Specific Registers and Extended Registers. See Register Map section.

The following table shows the MII Management frame format for the KSZ9021RL/RN.

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1’s	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1’s	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Table 5. MII Management Frame Format – for KSZ9021RL/RN

Interrupt (INT_N)

The INT_N pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the KSZ9021RL/RN PHY register. Bits [15:8] of register 27 (1Bh) are the interrupt control bits to enable and disable the conditions for asserting the INT_N signal. Bits [7:0] of register 27 (1Bh) are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 27 (1Bh).

Bit 14 of register 31 (1Fh) sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ9021RL/RN control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

LED Mode

The KSZ9021RL/RN provides two programmable LED output pins, LED2 and LED1, which are configurable to support two LED modes. The LED mode is configured by the LED_MODE strap-in pin. It is latched at power-up/reset and is defined as follows:

- Pull-up: Single LED Mode
- Pull-down: Tri-color Dual LED Mode

Single LED Mode

In Single LED Mode, the LED2 pin indicates the link status while the LED1 pin indicates the activity status, as shown in the following table.

LED pin	Pin State	LED Definition	Link / Activity
LED2	H	OFF	Link off
	L	ON	Link on (any speed)
LED1	H	OFF	No Activity
	Toggle	Blinking	Activity (RX, TX)

Table 6. Single LED Mode – Pin Definition

Tri-color Dual LED Mode

In Tri-color Dual LED Mode, the Link and Activity status are indicated by the LED2 pin for 1000Base-T, by the LED1 pin for 100Base-TX, and by both LED2 and LED1 pin, working in conjunction, for 10Base-T. This is summarized in the following table.

LED Pin (State)		LED Pin (Definition)		Link / Activity
LED2	**LED1**	**LED2**	**LED1**	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link / No Activity
Toggle	Toggle	Blinking	Blinking	10 Link / Activity (RX, TX)

Table 7. Tri-color Dual LED Mode – Pin Definition

Each LED output pin can directly drive a LED with a series resistor (typically 220Ω to 470Ω).

For activity indication, the LED output toggles at approximately 12.5Hz (80ms) to ensure visibility to the human eye.

NAND Tree Support

The KSZ9021RL/RN provides parametric NAND tree support for fault detection between chip I/Os and board. NAND tree mode is enabled at power-up / reset with the MODE[3:0] strap-in pins set to 0100.

The following tables list the NAND tree pin order for KSZ9021RL and KSZ9021RN.

Pin	Description
LED2	Input
LED1	Input
TXD0	Input
TXD1	Input
TXD2	Input
TXD3	Input
TX_ER	Input
GTX_CLK	Input
TX_EN	Input
RX_DV	Input
RX_ER	Input
RX_CLK	Input
CRS	Input
COL	Input
INT_N	Input
MDC	Input
MDIO	Input
CLK125_NDO	Output

Table 8. NAND Tree Test Pin Order – for KSZ9021RL

Pin	Description
LED2	Input
LED1	Input
TXD0	Input
TXD1	Input
TXD2	Input
TXD3	Input
GTX_CLK	Input
TX_EN	Input
RX_DV	Input
RX_CLK	Input
INT_N	Input
MDC	Input
MDIO	Input
CLK125_NDO	Output

Table 9. NAND Tree Test Pin Order – for KSZ9021RN

Power Management

The KSZ9021RL/RN offers the following power management modes:

Power Saving Mode

This mode is a KSZ9021RL/RN green feature to reduce power consumption when the cable is unplugged. It is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

Software Power Down Mode

This mode is used to power down the KSZ9021RL/RN device when it is not in use after power-up. Power down mode is enabled by writing a one to register 0h bit 11. In the power down state, the KSZ9021RL/RN disables all internal functions, except for the MII management interface. The KSZ9021RL/RN exits power down mode after writing a zero to register 0h bit 11.

Chip Power Down Mode

This mode provides the lowest power state for the KSZ9021RL/RN when it is not in use and is mounted on the board. Chip power down mode is enabled at power-up / reset with the MODE[3:0] strap-in pins set to 0111. The KSZ9021RL/RN exits chip power down mode when a hardware reset is applied to the RESET_N pin with the MODE[3:0] strap-in pins set to an operating mode other than chip power down mode.

Register Map

The IEEE 802.3 Specification provides a 32 register address space for the PHY. Registers 0 thru 15 are standard PHY registers, defined per the specification. Registers 16 thru 31 are vendor specific registers.

The KSZ9021RL/RN uses the IEEE provided register space for IEEE Defined Registers and Vendor Specific Registers, and uses the following registers to access Extended Registers:

- Register 11 (Bh) for Extended Register – Control
- Register 12 (Ch) for Extended Register – Data Write
- Register 13 (Dh) for Extended Register – Data Read

Examples:

- Extended Register Read // Read from Operation Mode Strap Status Register
  1. Write register 11 (Bh) with 0103h // Set register 259 (103h) for read
  2. Read register 13 (Dh) // Read register value

- Extended Register Write // Write to Operation Mode Strap Override Register
  1. Write register 11 (Bh) with 8102h // Set register 258 (102h) for write
  2. Write register 12 (Ch) with 0010h // Write 0010h value to register to set NAND Tree mode

Register Number (Hex)	Description
IEEE Defined Registers	
0 (0h)	Basic Control
1 (1h)	Basic Status
2 (2h)	PHY Identifier 1
3 (3h)	PHY Identifier 2
4 (4h)	Auto-Negotiation Advertisement
5 (5h)	Auto-Negotiation Link Partner Ability
6 (6h)	Auto-Negotiation Expansion
7 (7h)	Auto-Negotiation Next Page

Register Number (Hex)	Description
8 (8h)	Auto-Negotiation Link Partner Next Page Ability
9 (9h)	1000Base-T Control
10 (Ah)	1000Base-T Status
11 (Bh)	Extended Register – Control
12 (Ch)	Extended Register – Data Write
13 (Dh)	Extended Register – Data Read
14 (Eh)	Reserved
15 (Fh)	Extended – MII Status
Vendor Specific Registers	
16 (10h)	Reserved
17 (11h)	Remote Loopback, LED Mode
18 (12h)	LinkMD® – Cable Diagnostic
19 (13h)	Digital PMA/PCS Status
20 (14h)	Reserved
21 (15h)	RXER Counter
22 (16h) – 26 (1Ah)	Reserved
27 (1Bh)	Interrupt Control/Status
28 (1Ch)	Digital Debug Control 1
29 (1Dh) – 30 (1Eh)	Reserved
31 (1Fh)	PHY Control
Extended Registers	
256 (100h)	Common Control
257 (101h)	Strap Status
258 (102h)	Operation Mode Strap Override
259 (103h)	Operation Mode Strap Status
260 (104h)	RGMII Clock and Control Pad Skew
261 (105h)	RGMII RX Data Pad Skew
263 (107h)	Analog Test Register

Register Description

IEEE Defined Registers

Address	Name	Description	Mode[(1)]	Default
Register 0 (0h) – Basic Control				
0.15	Reset	1 = Software PHY reset 0 = Normal operation This bit is self-cleared after a ‘1’ is written to it.	RW/SC	0
0.14	Loop-back	1 = Loop-back mode 0 = Normal operation	RW	0

Address	Name	Description	Mode(1)	Default
0.13	Speed Select (LSB)	[0.6, 0.13] [1,1] = Reserved [1,0] = 1000Mbps [0,1] = 100Mbps [0,0] = 10Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1).	RW	Hardware Setting
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, auto-negotiation result overrides settings in register 0.13, 0.8 and 0.6.	RW	1
0.11	Power Down	1 = Power down mode 0 = Normal operation	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from RGMII 0 = Normal operation	RW	0
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a ‘1’ is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	Hardware Setting
0.7	Reserved		RW	0
0.6	Speed Select (MSB)	[0.6, 0.13] [1,1] = Reserved [1,0] = 1000Mbps [0,1] = 100Mbps [0,0] = 10Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1).	RW	0
0.5:0	Reserved		RO	00_0000
Register 1 (1h) – Basic Status				
1.15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100Base-TX Full Duplex	1 = Capable of 100Mbps full-duplex 0 = Not capable of 100Mbps full-duplex	RO	1
1.13	100Base-TX Half Duplex	1 = Capable of 100Mbps half-duplex 0 = Not capable of 100Mbps half-duplex	RO	1
1.12	10Base-T Full Duplex	1 = Capable of 10Mbps full-duplex 0 = Not capable of 10Mbps full-duplex	RO	1
1.11	10Base-T Half Duplex	1 = Capable of 10Mbps half-duplex 0 = Not capable of 10Mbps half-duplex	RO	1
1.10:9	Reserved		RO	00
1.8	Extended Status	1 = Extended Status Information in Reg. 15. 0 = No Extended Status Information in Reg. 15.	RO	1

Address	Name	Description	Mode(1)	Default
1.7	Reserved		RO	0
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Capable to perform auto-negotiation 0 = Not capable to perform auto-negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capabilities registers	RO	1
Register 2 (2h) – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0022h
Register 3 (3h) – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0001_01
3.9:4	Model Number	Six bit manufacturer's model number	RO	10_0001
3.3:0	Revision Number	Four bit manufacturer's revision number	RO	Indicates silicon revision
Register 4 (4h) – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability.	RW	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved		RO	0
4.11:10	Pause	[4.11, 4.10] [0,0] = No PAUSE [1,0] = Asymmetric PAUSE (link partner) [0,1] = Symmetric PAUSE [1,1] = Symmetric & Asymmetric PAUSE (local device)	RW	00
4.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	1

Address	Name	Description	Mode[1]	Default
4.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RW	1
4.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RW	1
4.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001
Register 5 (5h) – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved		RO	0
5.11:10	Pause	[5.11, 5.10] [0,0] = No PAUSE [1,0] = Asymmetric PAUSE (link partner) [0,1] = Symmetric PAUSE [1,1] = Symmetric & Asymmetric PAUSE (local device)	RW	00
5.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RO	0
5.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RO	0
5.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RO	0
5.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0000
Register 6 (6h) – Auto-Negotiation Expansion				
6.15:5	Reserved		RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection.	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0

Address	Name	Description	Mode(1)	Default
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0
Register 7 (7h) – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next page(s) will follow 0 = Last page	RW	0
7.14	Reserved		RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001
Register 8 (8h) – Auto-Negotiation Link Partner Next Page Ability				
8.15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0
8.12	Acknowledge2	1 = Able to act on the information 0 = Not able to act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one	RO	0
8.10:0	Message Field		RO	000_0000_0000
Register 9 (9h) – 1000Base-T Control				

Address	Name	Description	Mode(1)	Default
9:15:13	Test Mode Bits	Transmitter test mode operations [9.15:13] Mode [000] Normal Operation [001] Test mode 1 –Transmit waveform test [010] Test mode 2 –Transmit jitter test in Master mode [011] Test mode 3 –Transmit jitter test in Slave mode [100] Test mode 4 –Transmitter distortion test [101] Reserved, operations not identified [110] Reserved, operations not identified [111] Reserved, operations not identified	RW	000
9.12	MASTER-SLAVE Manual Config Enable	1 = Enable MASTER-SLAVE Manual configuration value 0 = Disable MASTER-SLAVE Manual configuration value	RW	0
9.11	MASTER-SLAVE Manual Config Value	1 = Configure PHY as MASTER during MASTER-SLAVE negotiation 0 = Configure PHY as SLAVE during MASTER-SLAVE negotiation This bit is ignored if MASTER-SLAVE Manual Config is disabled (register 9.12 = 0).	RW	0
9.10	Port Type	1 = Indicate the preference to operate as multiport device **(MASTER)** 0 = Indicate the preference to operate as single-port device (**SLAVE**) This bit is valid only if the MASTER-SLAVE Manual Config Enable bit is disabled (register 9.12 = 0).	RW	0
9.9	1000Base-T Full-Duplex	1 = Advertise PHY is 1000Base-T full-duplex capable 0 = Advertise PHY is not 1000Base-T full-duplex capable	RW	1
9.8	1000Base-T Half-Duplex	1 = Advertise PHY is 1000Base-T half-duplex capable 0 = Advertise PHY is not 1000Base-T half-duplex capable	RW	Hardware Setting
9.7:0	Reserved	Write as 0, ignore on read	RO	
Register 10 (Ah) – 1000Base-T Status				
10.15	MASTER-SLAVE configuration fault	1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected	RO/LH/SC	0

Address	Name	Description	Mode(1)	Default
10.14	MASTER-SLAVE configuration resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	RO	0
10.13	Local Receiver Status	1 = Local Receiver OK (loc_rcvr_status = 1) 0 = Local Receiver not OK (loc_rcvr_status = 0)	RO	0
10.12	Remote Receiver Status	1 = Remote Receiver OK (rem_rcvr_status = 1) 0 = Remote Receiver not OK (rem_rcvr_status = 0)	RO	0
10.11	LP 1000T FD	1 = Link Partner is capable of 1000Base-T full-duplex 0 = Link Partner is not capable of 1000Base-T full-duplex	RO	0
A.10	LP 1000T HD	1 = Link Partner is capable of 1000Base-T half-duplex 0 = Link Partner is not capable of 1000Base-T half-duplex	RO	0
10.9:8	Reserved		RO	00
10.7:0	Idle Error Count	Cumulative count of errors detected when receiver is receiving idles and PMA_TXMODE.indicate = SEND_N. The counter is incremented every symbol period that rxerror_status = ERROR.	RO/SC	0000_0000
Register 11 (Bh) – Extended Register – Control				
11.15	Extended Register – read/write select	1 = Write Extended Register 0 = Read Extended Register	RW	0
11.14:9	Reserved		RW	000_000
11.8	Extended Register – page	Select page for Extended Register	RW	0
11.7:0	Extended Register – address	Select Extended Register Address	RW	0000_0000
Register 12 (Ch) – Extended Register – Data Write				
12.15:0	Extended Register – write	16-bit value to write to Extend Register Address in register 11 (Bh) bits [7:0]	RW	0000_0000_0000_0000
Register 13 (Dh) – Extended Register – Data Read				
13.15:0	Extended Register – read	16-bit value read from Extend Register Address in register 11 (Bh) bits [7:0]	RO	0000_0000_0000_0000
Register 15 (Fh) – Extended – MII Status				
15.15	1000Base-X Full-duplex	1 = PHY able to perform 1000Base-X full-duplex 0 = PHY not able to perform 1000Base-X full-duplex	RO	0

Address	Name	Description	Mode(1)	Default
15.14	1000Base-X Half-duplex	1 = PHY able to perform 1000Base-X half-duplex 0 = PHY not able to perform 1000Base-X half-duplex	RO	0
15.13	1000Base-T Full-duplex	1 = PHY able to perform 1000Base-T full-duplex 1000BASE-X 0 = PHY not able to perform 1000Base-T full-duplex	RO	1
15.12	1000Base-T Half-duplex	1 = PHY able to perform 1000Base-T half-duplex 0 = PHY not able to perform 1000Base-T half-duplex	RO	1
15.11:0	Reserved	Ignore when read	RO	-

Note:

1. RW = Read/Write.
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.
   LL = Latch low.

Vendor Specific Registers

Address	Name	Description	Mode(1)	Default
Register 17 (11h) – Remote Loopback, LED Mode				
17.15:9	Reserved		RW	0000_001
17.8	Remote Loopback	1 = Enable Remote Loopback 0 = Disable Remote Loopback	RW	0
17.7:6	Reserved		RW	11
17.5:4	Reserved		RW	11
17.3	LED Test Enable	1 = Enable LED test mode 0 = Disable LED test mode	RW	0
17.2:1	Reserved		RW	00
17.0	Reserved		RO	0
Register 18 (12h) – LinkMD® – Cable Diagnostic				
18.15	Reserved		RW/SC	0
18.14:8	Reserved		RW	000_0000
18.7:0	Reserved		RO	0000_0000
Register 19 (13h) – Digital PMA/PCS Status				
19.15:3	Reserved		RO/LH	0000_0000_0000_0
19.2	1000Base-T Link Status	1000 Base-T Link Status 1 = Link status is OK 0 = Link status is not OK	RO	0

Address	Name	Description	Mode(1)	Default
19.1	100Base-TX Link Status	100 Base-TX Link Status 1 = Link status is OK 0 = Link status is not OK	RO	0
19.0	Reserved		RO	0
Register 21 (15h) – RXER Counter				
21.15:0	RXER Counter	Receive error counter for Symbol Error frames	RO/RC	0000_0000_0000_0000
Register 27 (1Bh) – Interrupt Control/Status				
27.15	Jabber Interrupt Enable	1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt	RW	0
27.14	Receive Error Interrupt Enable	1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt	RW	0
27.13	Page Received Interrupt Enable	1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt	RW	0
27.12	Parallel Detect Fault Interrupt Enable	1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt	RW	0
27.11	Link Partner Acknowledge Interrupt Enable	1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt	RW	0
27.10	Link Down Interrupt Enable	1 = Enable Link Down Interrupt 0 = Disable Link Down Interrupt	RW	0
27.9	Remote Fault Interrupt Enable	1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt	RW	0
27.8	Link Up Interrupt Enable	1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt	RW	0
27.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occurred	RO/RC	0
27.6	Receive Error Interrupt	1 = Receive Error occurred 0 = Receive Error did not occurred	RO/RC	0
27.5	Page Receive Interrupt	1 = Page Receive occurred 0 = Page Receive did not occurred	RO/RC	0
27.4	Parallel Detect Fault Interrupt	1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occurred	RO/RC	0
27.3	Link Partner Acknowledge Interrupt	1 = Link Partner Acknowledge occurred 0 = Link Partner Acknowledge did not occurred	RO/RC	0
27.2	Link Down Interrupt	1 = Link Down occurred 0 = Link Down did not occurred	RO/RC	0
27.1	Remote Fault Interrupt	1 = Remote Fault occurred 0 = Remote Fault did not occurred	RO/RC	0

Address	Name	Description	Mode(1)	Default
27.0	Link Up Interrupt	1 = Link Up occurred 0 = Link Up did not occurred	RO/RC	0
Register 28 (1Ch) – Digital Debug Control 1				
28.15:8	Reserved		RW	0000_0000
28.7	mdi_set	mdi_set has no function when swapoff (reg28.6) is de-asserted. 1 = When swapoff is asserted, if mdi_set is asserted, chip will operate at MDI mode. 0 = When swapoff is asserted, if mdi_set is de-asserted, chip will operate at MDI-X mode.	RW	0
28.6	swapoff	1 = Disable auto crossover function 0 = Enable auto crossover function	RW	0
28.5:1	Reserved		RW	00_000
28.0	PCS Loopback	1 = Enable 10Base-T and 100Base-TX Loopback for register 0h bit 14. 0 = normal function	RW	0
Register 31 (1Fh) – PHY Control				
31.15	Reserved		RW	0
31.14	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
31.13:12	Reserved		RW	00
31.11:10	Reserved		RO/LH/RC	00
31.9	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
31.8:7	Reserved		RW	00
31.6	Speed status 1000Base-T	1 = Indicate chip final speed status at 1000Base-T	RO	0
31.5	Speed status 100Base-TX	1 = Indicate chip final speed status at 100Base-TX	RO	0
31.4	Speed status 10Base-T	1 = Indicate chip final speed status at 10Base-T	RO	0
31.3	Duplex status	Indicate chip duplex status 1 = Full-duplex 0 = Half-duplex	RO	0
31.2	1000Base-T Mater/Slave status	1 = Indicate 1000Base-T Master mode 0 = Indicate 1000Base-T Slave mode	RO	0
31.1	Software Reset	1 = Reset chip, except all registers 0 = Disable reset	RW	0
31.0	Link Status Check Fail	1 = Fail 0 = Not Failing	RO	0

Note:

1. RW = Read/Write.
   RC = Read-cleared
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.

Extended Registers

Address	Name	Description	Mode(1)	Default
Register 256 (100h) – Common Control				
256.15:9	Reserved		RW	0000_000
256.8	RGMII In-band PHY Status	1 = Enable 0 = Disable	RW	0
256.7:0	Reserved		RW	
Register 257 (101h) – Strap Status				
257.15:6	Reserved		RO	
257.5	CLK125_EN status	1 = CLK125_EN strap-in is enabled 0 = CLK125_EN strap-in is disabled	RO	
257.4:0	PHYAD[4:0] status	Strapped-in value for PHY Address	RO	
Register 258 (102h) – Operation Mode Strap Override				
258.15	RGMII all capabilities override	1 = Override strap-in for RGMII advertise all capabilities	RW	
258.14	RGMII no 1000BT_HD override	1 = Override strap-in for RGMII advertise all capabilities except 1000Base-T half-duplex	RW	
258.13	RGMII 1000BT_H/FD only override	1 = Override strap-in for RGMII advertise 1000Base-T full and half-duplex only	RW	
258.12	RGMII 1000BT_FD only override	1 = Override strap-in for RGMII advertise 1000Base-T full-duplex only	RW	
258.11:8	Reserved		RW	
258.7	Tri-state all digital I/Os	1 = Tri-state all digital I/Os for further power saving during software power down	RW	0
258.6:5	Reserved		RW	
258.4	NAND Tree override	1 = Override strap-in for NAND Tree mode	RW	
258.3:0	Reserved		RW	
Register 259 (103h) – Operation Mode Strap Status				
259.15	RGMII all capabilities strap-in status	1 = Strap to RGMII advertise all capabilities	RO	
259.14	RGMII no 1000BT_HD strap-in status	1 = Strap to RGMII advertise all capabilities except 1000Base-T half-duplex	RO	
259.13	RGMII only 1000BT_H/FD strap-in status	1 = Strap to RGMII advertise 1000Base-T full and half-duplex only	RO	
259.12	RGMII only 1000BT_FD strap-in status	1 = Strap to RGMII advertise 1000Base-T full-duplex only	RO	
259.11:5	Reserved		RO	

Address	Name	Description	Mode(1)	Default
259.4	NAND Tree strap-in status	1 = Strap to NAND Tree mode	RO	
259.3:0	Reserved		RO	
Register 260 (104h) – RGMII Clock and Control Pad Skew				
260.15:12	rxc_pad_skew	RGMII RXC PAD Skew Control (0.2ns/step)	RW	0111
260.11:8	rxdv_pad_skew	RGMII RX_CTL PAD Skew Control (0.2ns/step)	RW	0111
260.7:4	txc_pad_skew	RGMII TXC PAD Skew Control (0.2ns/step)	RW	0111
260.3:0	txen_pad_skew	RGMII TX_CTL PAD Skew Control (0.2ns/step)	RW	0111
Register 261 (105h) – RGMII RX Data Pad Skew				
261.15:12	rxd3_pad_skew	RGMII RXD3 PAD Skew Control (0.2ns/step)	RW	0111
261.11:8	rxd2_pad_skew	RGMII RXD2 PAD Skew Control (0.2ns/step)	RW	0111
261.7:4	rxd1_pad_skew	RGMII RXD1 PAD Skew Control (0.2ns/step)	RW	0111
261.3:0	rxd0_pad_skew	RGMII RXD0 PAD Skew Control (0.2ns/step)	RW	0111
Register 263 (107h) – Analog Test Register				
263.15	LDO disable	1 = LDO controller disable 0 = LDO controller enable	RW	0
263.14:9	Reserved		RW	000_000
263.8	Low frequency oscillator mode	1 = Low frequency oscillator mode enable 0 = Low frequency oscillator mode disable Use for further power saving during software power down.	RW	0
263.7:0	Reserved		RW	0000_0000

Note:

1. RW = Read/Write.
   RO = Read only.

Absolute Maximum Ratings[1]

Supply Voltage
- (DVDDL, AVDDL, AVDDL_PLL)....... -0.5V to V_{DD}+10%
- (AVDDH).. -0.5V to V_{DD} +10%
- (DVDDH)............................... -0.5V to V_{DD} (3.3V)+10%

Input Voltage (all inputs) .... -0.5V to V_{DD} +10%
Output Voltage (all outputs) .... -0.5V to V_{DD} +10%
Lead Temperature (soldering, 10sec.)...................... 260°C
Storage Temperature (T_s) ....-55°C to +150°C

Operating Ratings[2]

Supply Voltage
- (DVDDL, AVDDL, AVDDL_PLL).... +1.140V to +1.260V
- (AVDDH)....................................... +3.135V to +3.465V
- (DVDDH @ 3.3V) .... +3.135V to +3.465V
- (DVDDH @ 2.5V) .... +2.375V to +2.625V

Ambient Temperature
- (T_A Commercial: KSZ9021RL/RN) .... 0°C to +70°C
- (T_A Industrial: KSZ9021RLI/RNI)..........-40°C to +85°C

Maximum Junction Temperature (T_J Max) .... 125°C
Thermal Resistance (θ_{JA})...................................31.85°C/W
Thermal Resistance (θ_{JC}).....................................8.07°C/W

Electrical Characteristics[3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Supply Current – Core / Digital I/Os						
I_{CORE}	1.2V total of:	1000Base-T Link-up (no traffic)		528		mA
	DVDDL (1.2V digital core) +	1000Base-T Full-duplex @ 100% utilization		563		mA
	AVDDL (1.2V analog core) +	100Base-TX Link-up (no traffic)		158		mA
	AVDDL_PLL (1.2V for PLL)	100Base-TX Full-duplex @ 100% utilization		158		mA
		10Base-T Link-up (no traffic)		7		mA
		10Base-T Full-duplex @ 100% utilization		7		mA
		Power Saving Mode (cable unplugged)		15		mA
		Software Power Down Mode (register 0.11 =1)		1.3		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = 0111)		1.3		mA
$I_{DVDDH\_2.5}$	2.5V for digital I/Os	1000Base-T Link-up (no traffic)		13		mA
		1000Base-T Full-duplex @ 100% utilization		37		mA
	(RGMII operating @ 2.5V)	100Base-TX Link-up (no traffic)		4		mA
		100Base-TX Full-duplex @ 100% utilization		9		mA
		10Base-T Link-up (no traffic)		2		mA
		10Base-T Full-duplex @ 100% utilization		5		mA
		Power Saving Mode (cable unplugged)		7		mA
		Software Power Down Mode (register 0.11 =1)		3		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = 0111)		1		mA
$I_{DVDDH\_3.3}$	3.3V for digital I/Os	1000Base-T Link-up (no traffic)		20		mA
		1000Base-T Full-duplex @ 100% utilization		58		mA
	(RGMII operating @ 3.3V)	100Base-TX Link-up (no traffic)		11		mA
		100Base-TX Full-duplex @ 100% utilization		15		mA
		10Base-T Link-up (no traffic)		5		mA
		10Base-T Full-duplex @ 100% utilization		11		mA
		Power Saving Mode (cable unplugged)		9		mA
		Software Power Down Mode (register 0.11 =1)		7		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = 0111)		1		mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
Supply Current – Transceiver (equivalent to current draw through external transformer center taps for PHY transceivers with current-mode transmit drivers)						
I_{AVDDH}	3.3V for transceiver	1000Base-T Link-up (no traffic)		75		mA
		1000Base-T Full-duplex @ 100% utilization		75		mA
		100Base-TX Link-up (no traffic)		29		mA
		100Base-TX Full-duplex @ 100% utilization		29		mA
		10Base-T Link-up (no traffic)		35		mA
		10Base-T Full-duplex @ 100% utilization		43		mA
		Power Saving Mode (cable unplugged)		36		mA
		Software Power Down Mode (register 0.11 =1)		2		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = 0111)		1		mA
TTL Inputs						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current	V_{IN} = GND ~ V_{DDIO}		-10	10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
$\|I_{oz}\|$	Output Tri-State Leakage				10	µA
100Base-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination across differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination across differential output			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				± 0.25	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of I_{SET}	$R(I_{SET})$ = 4.99K		0.535		V
	Output Jitter	Peak-to-peak		0.7	1.4	ns
10Base-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	100Ω termination across differential output	2.2		2.8	V
	Jitter Added	Peak-to-peak			3.5	ns
	Harmonic Rejection	Transmit all-one signal sequence		-31		dB
10Base-T Receive						
V_{SQ}	Squelch Threshold	5MHz square wave	300	400		mV

Notes:

1. Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
2. The device is not guaranteed to function outside its operating rating.
3. T_A = 25°C. Specification is for packaged product only.

Timing Diagrams

RGMII Timing

The KSZ9021RL/RN RGMII timing conforms to the timing requirements per the RGMII Version 1.3 Specification.

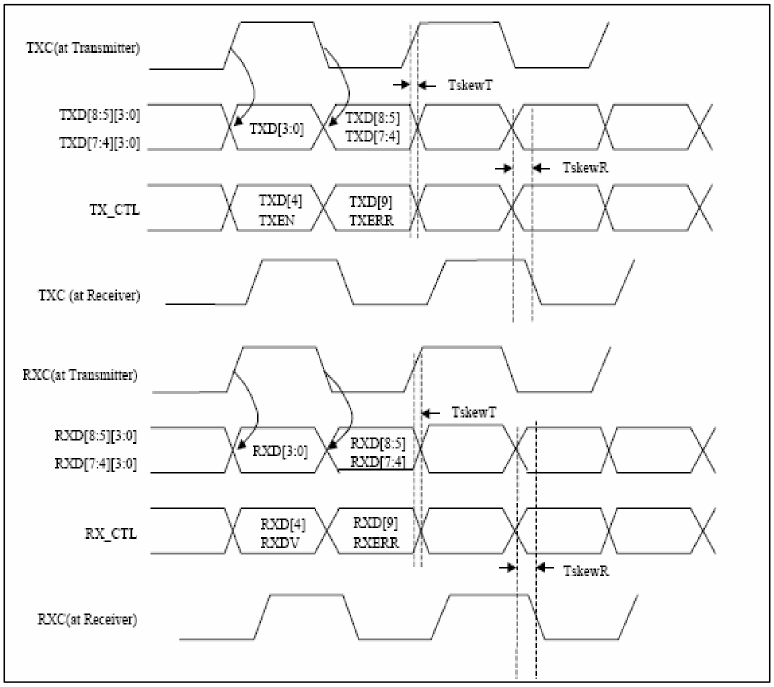


Figure 5. RGMII v1.3 Specification (Figure 2 – Multiplexing and Timing Diagram)

Timing Parameter	Description	Min	Typ	Max	Unit
TskewT	Data to Clock output Skew (at Transmitter)	-500		500	ps
TskewR	Data to Clock input Skew (at Receiver)	1		2.6	ns
Tcyc (1000Base-T)	Clock Cycle Duration for 1000Base-T	7.2	8	8.8	ns
Tcyc (100Base-TX)	Clock Cycle Duration for 100Base-TX	36	40	44	ns
Tcyc (10Base-T)	Clock Cycle Duration for 10Base-T	360	400	440	ns

Table 10. RGMII v1.3 Specification (Timing Specifics from Table 2)

Accounting for TskewT, the TskewR specification in the above table requires the PCB board design to incorporate clock routing for TXC and RXC with an additional trace delay of greater than 1.5ns and less than 2.1ns for 1000Base-T. For 10Base-T/100Base-TX, the maximum delay is much greater than the 2.1ns for 1000Base-T, and thus is not specified.

Auto-Negotiation Timing

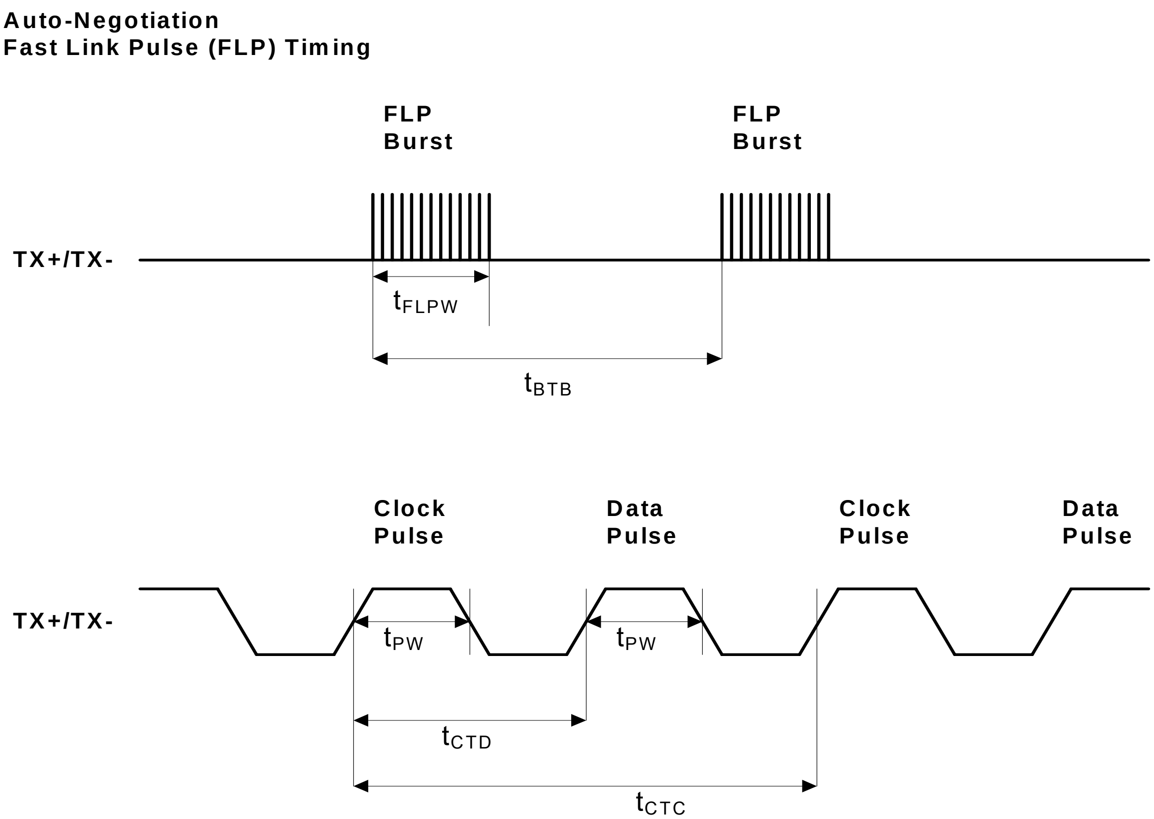


Figure 6. Auto-Negotiation Fast Link Pulse (FLP) Timing

Timing Parameter	Description	Min	Typ	Max	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst width		2		ms
t_{PW}	Clock/Data Pulse width		100		ns
t_{CTD}	Clock Pulse to Data Pulse	55.5	64	69.5	µs
t_{CTC}	Clock Pulse to Clock Pulse	111	128	139	µs
	Number of Clock/Data Pulse per FLP Burst	17		33	

Table 11. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

MDC/MDIO Timing

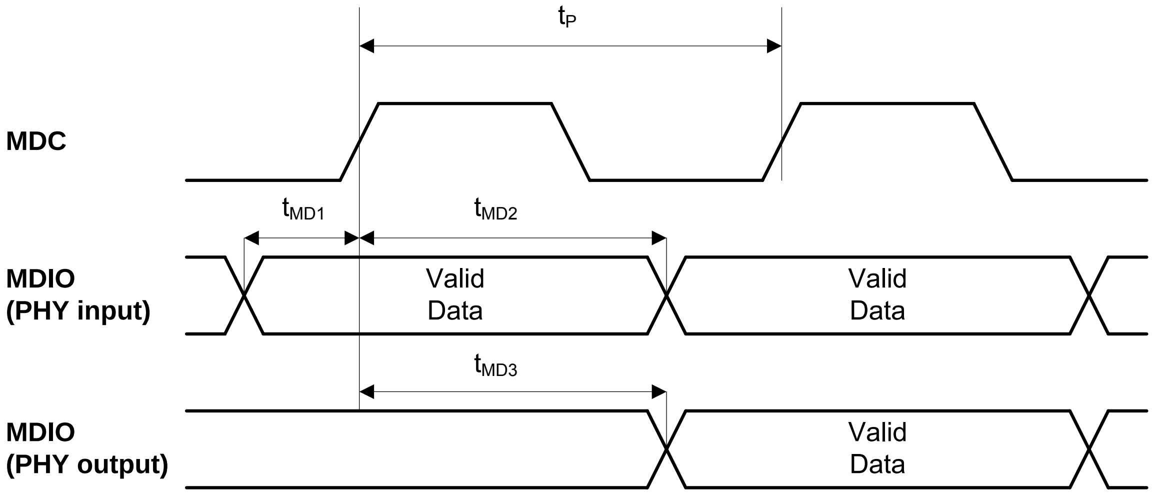


Figure 7. MDC/MDIO Timing

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	MDC period		400		ns
t_{1MD1}	MDIO (PHY input) setup to rising edge of MDC	10			ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	10			ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC	0			ns

Table 12. MDC/MDIO Timing Parameters

Reset Timing

The recommended KSZ9021RL/RN power-up reset timing is summarized in the following figure and table.

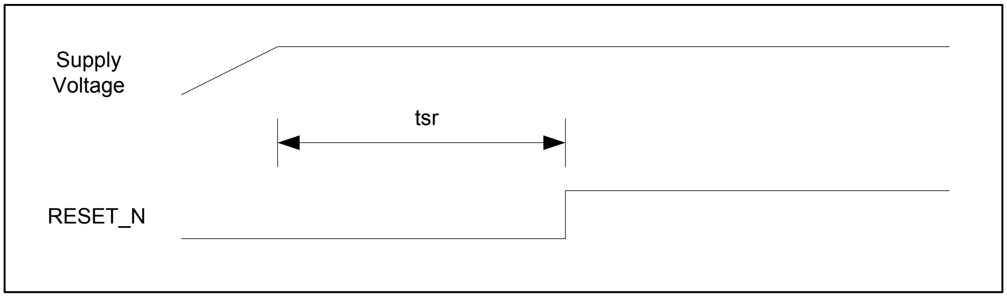


Figure 8. Reset Timing

Parameter	Description	Min	Max	Units
t_{sr}	Stable supply voltage to reset high	10		ms

Table 13. Reset Timing Parameters

After the de-assertion of reset, it is recommended to wait a minimum of 100µs before starting programming on the MIIM (MDC/MDIO) Interface.

Reset Circuit

The following reset circuit is recommended for powering up the KSZ9021RL/RN if reset is triggered by the power supply.

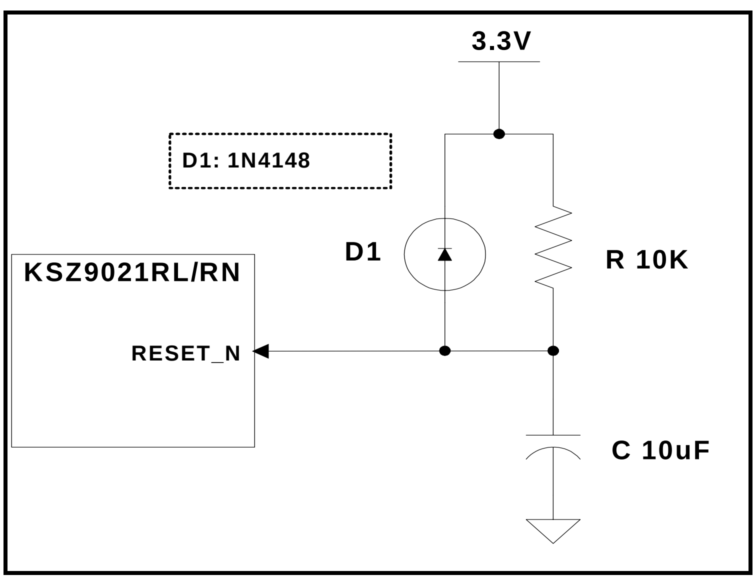


Figure 9. Recommended Reset Circuit

The following reset circuit is recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ9021RL/RN device. The RST_OUT_n from CPU/FPGA provides the warm reset after power up.

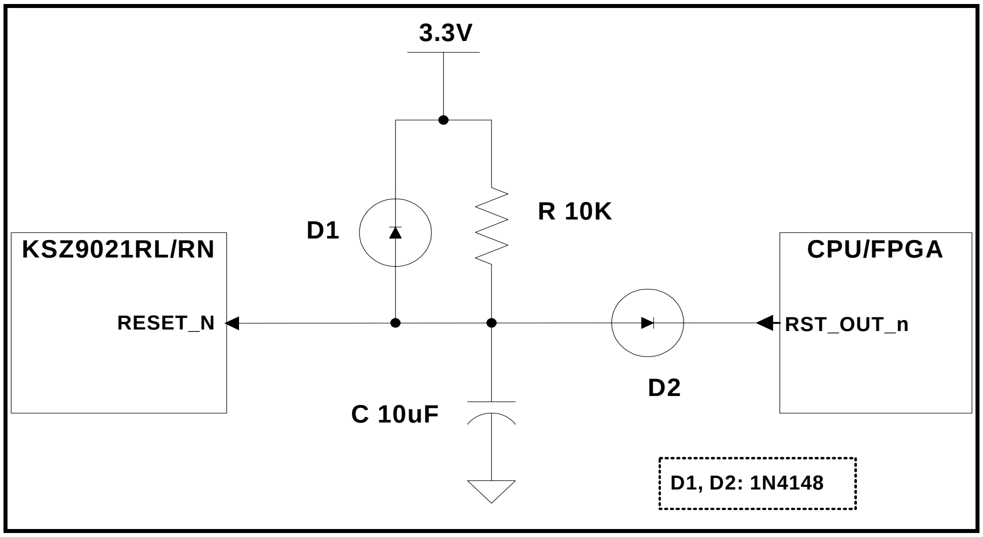


Figure 10. Recommended Reset Circuit for Interfacing with CPU/FPGA Reset Output

Reference Circuits – LED Strap-in Pins

The pull-up and pull-down reference circuits for the LED2/PHYAD1 and LED1/PHYAD0 strapping pins are shown in the following figure.

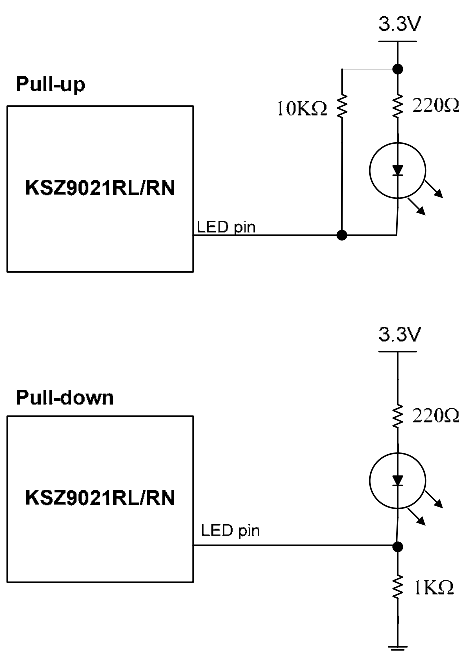


Figure 11. Reference Circuits for LED Strapping Pins

Reference Clock – Connection and Selection

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ9021RL/RN. The reference clock is 25 MHz for all operating modes of the KSZ9021RL/RN.

The following figure and table shows the reference clock connection to pins XI and XO of the KSZ9021RL/RN, and the reference clock selection criteria.

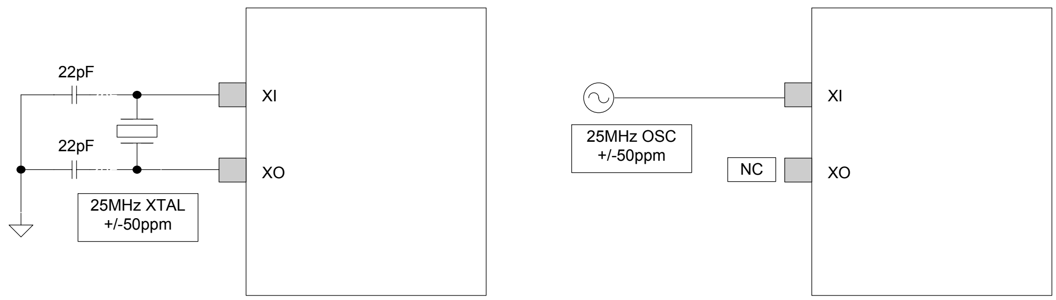


Figure 12. 25MHz Crystal / Oscillator Reference Clock Connection

Characteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max)	±50	ppm

Table 14. Reference Crystal/Clock Selection Criteria

Magnetics Specification

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode chokes is recommended for exceeding FCC requirements.

The following tables provide recommended magnetic characteristics and a list of qualified magnetics for the KSZ9021RL/RN.

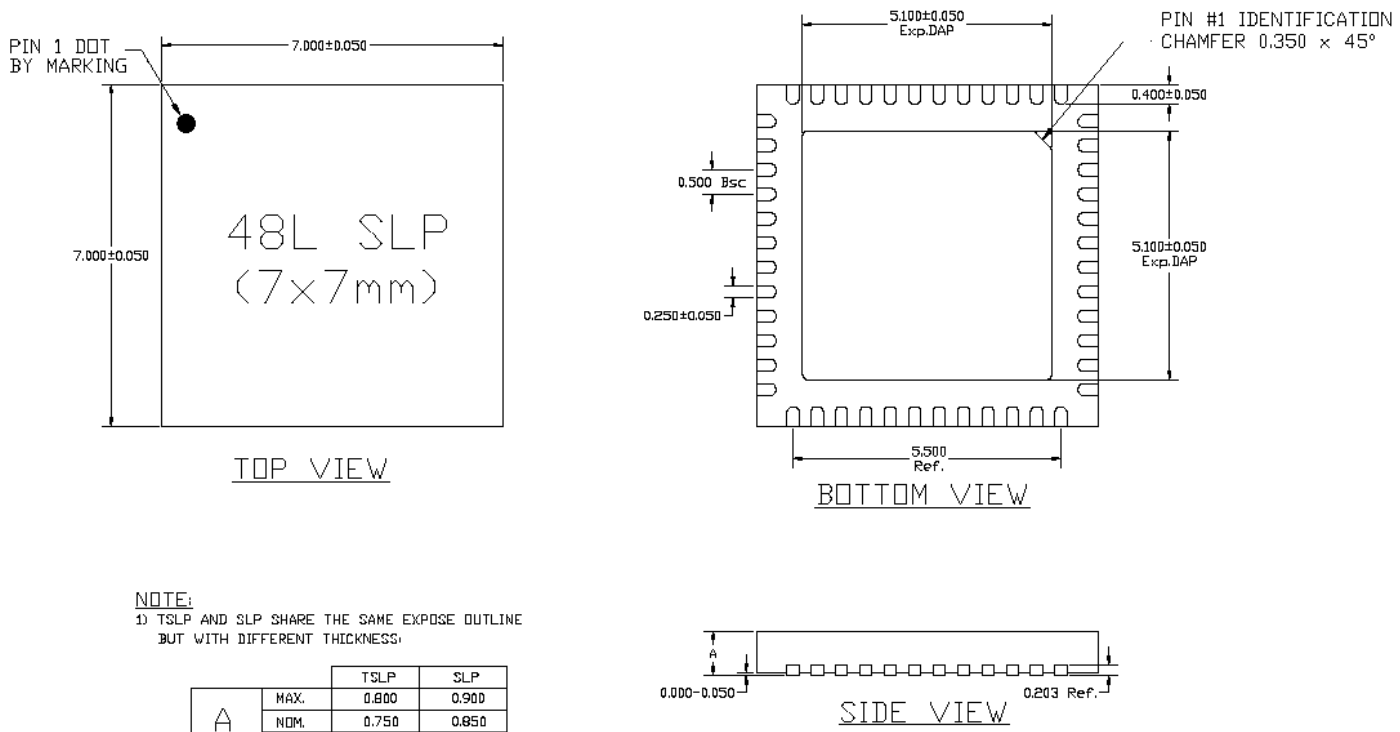
Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min.)	350μH	100mV, 100kHz, 8mA
Insertion loss (max.)	1.0dB	0MHz – 100MHz
HIPOT (min.)	1500Vrms	

Table 15. Magnetics Selection Criteria

Magnetic Manufacturer	Part Number	Auto MDI-X	Number of Port
Pulse	H5007NL	Yes	1
TDK	TLA-7T101LF	Yes	1

Table 16. Qualified Single Port 10/100/1000 Magnetics

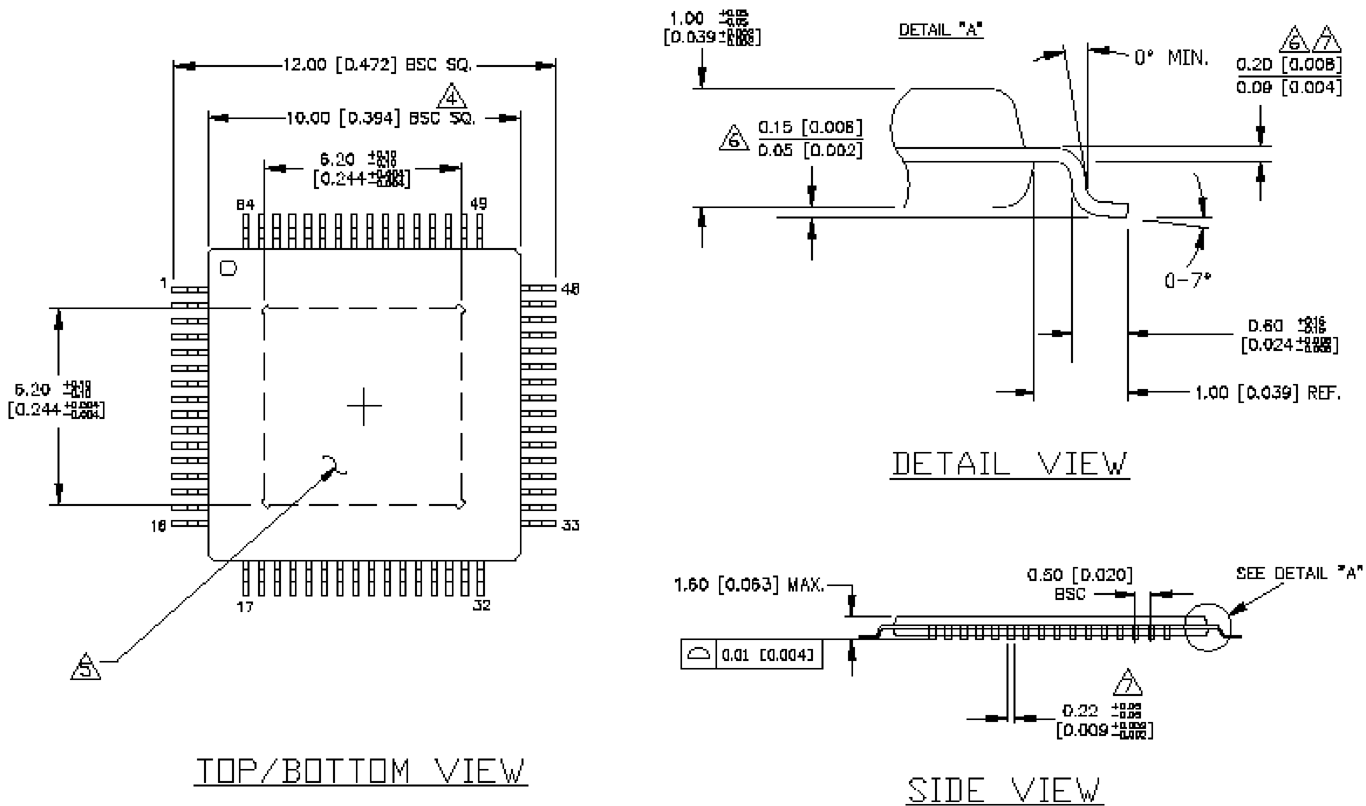
Package Information



NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE
BUT WITH DIFFERENT THICKNESS.

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

48-Pin (7mm x 7mm) QFN



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.25[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

64-Pin (10mm x 10mm) E-LQFP (V)

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