Application Note 157

Optimized Power Scheme for High Efficiency, Low-Power Consumption and Dissipation

KSZ9021 Gigabit Ethernet PHY

General Description

Gigabit Ethernet brings a big power consumption penalty vs. 10/100Mbps Ethernet. This increased power consumption vs. fast Ethernet must be addressed for severe environment applications, i.e., applications that can reach more than 70°C ambient temperature around the PHY. On the other hand, some applications are not heavily constrained by ambient temperature, but rather by current/power consumption. This application note describes options available for such applications, specifically the need to either optimize or reduce the following:

- Power dissipation
- Power consumption
- Size

Depending on KSZ9021 version used (G or R), Interface connecting the CPU MAC engine to the PHY is either GMII (Gigabit Media Independent Interface) or RGMII (Reduced Gigabit Media Independent Interface). This interface can be powered at 3.3V or 2.5V depending on CPU I/O constraints. The PHY itself needs two power rails. The transmit physical interface to the transformer/RJ45 is powered by analog 3.3V rail that comes from the system (AVDDH). This 3.3V is also used to power the internal high voltage digital engine (DVDDH). The other power rail needed is 1.2V and can be built from integrated LDO controller (using external FET to split power dissipation) or by an external source. 1.2V analog powers the receiving engine (AVDDL) and the internal PLL (AVDD_PLL). The 1.2V digital (DVDDL) powers the digital core. Figure 1 describes typical system implementation of Gigabit PHY but we will see in this application note that changing from typical power supply scheme can improve/optimize the system performances to comply with tough environment requirements that can be experienced in some applications. Typical implementation is primarily focusing on cost optimized solution, not lowest power consumption or lowest power dissipation.

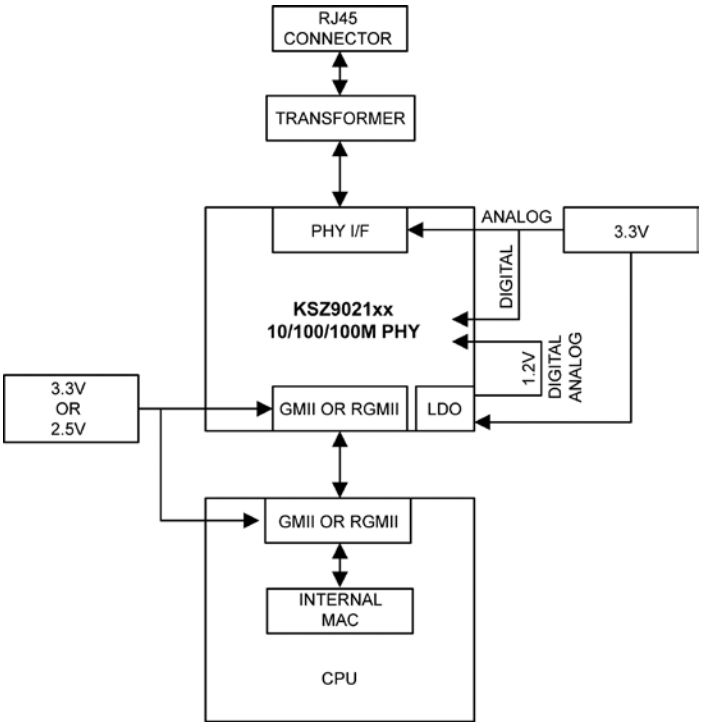

Figure 1. KSZ9021 Typical System Block Diagram

It is important to note that for application utilizing a higher than 70°C ambient temperature around the PHY, an industrial grade part must be selected. Industrial grade parts are denoted with an "I" at the end of the part name. For example: KSZ9021GNI, KSZ9021GQI, KSZ9021RLI, and KSZ9021RNI.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

PHY Power Highlights

Table 1 illustrates the required power rails and tolerances necessary to effectively utilize the KSZ9021:

Rail	Minimum (V)	Typical (V)	Maximum (V)
Analog TX/RX Interface (AVDDH)	3.135	3.3	3.465
Digital Interface and IOs (DVDDH)	3.135	3.3	3.465
	2.375	2.5	2.625
Analog and Digital Core (DVDDL, AVDDL)	1.14	1.2	1.26

Table 1. KSZ9021 Required Power Rails

A safe design rule is to size the power to sustain the worst possible case. An example of a worst case scenario is when the PHY is in 1000Base-T mode in full duplex with 100% traffic load. Table 2 offers power consumptions on each rail in this scenario. When PHY is not loaded with 100% traffic, idle frame is anyway always sent to keep the link up. In this case, analog PHY is running normally, only digital machine inside PHY is not exercised. Looking at power consumption in datasheet shows that there is not big difference between no traffic and 100% traffic use cases. As soon as traffic load cannot be controlled, taking 100% traffic load power consumption is normal way of designing power around the PHY.

Rail	Typical Consumption (mA)	Typical +20% (Process Variation) (mA)
Analog TX/RX Interface (AVDDH)	74	89
Digital Interface and IOs (DVDDH)	57	69
Analog and Digital Core (DVDDL, AVDDL)	555	666

Table 2. KSZ9021 Worst-Case Power Consumptions in 1000BT Mode

The default power supply scheme for the KSZ9021 uses an external MOSFET to generate the 1.2V core voltage. This MOSFET is driven internally by the KSZ9021 LDO controller, as illustrated in Figure 2.

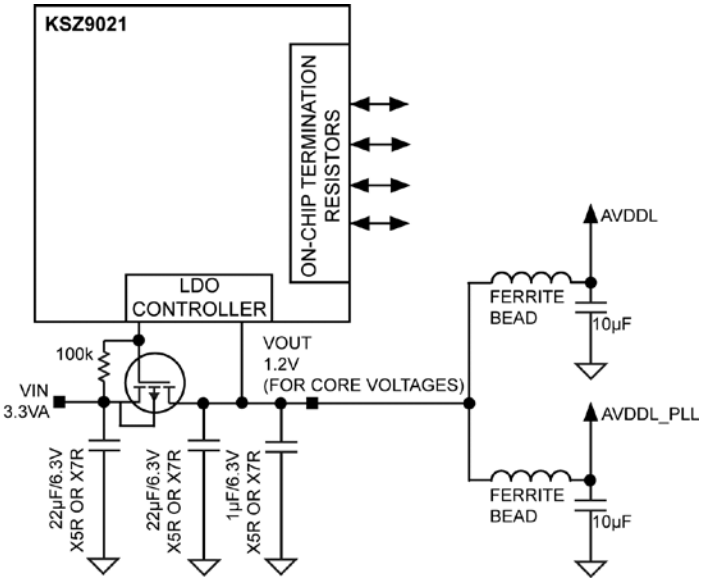

Figure 2. KSZ9021 Internal LDO Controller Driving External MOSEFT

Power Architecture Performances

Solutions Overview

Figure 3 and Table 3 illustrate the distribution solutions proposed depending on cost, size, EMI, and efficiency/power dissipation application constraints.

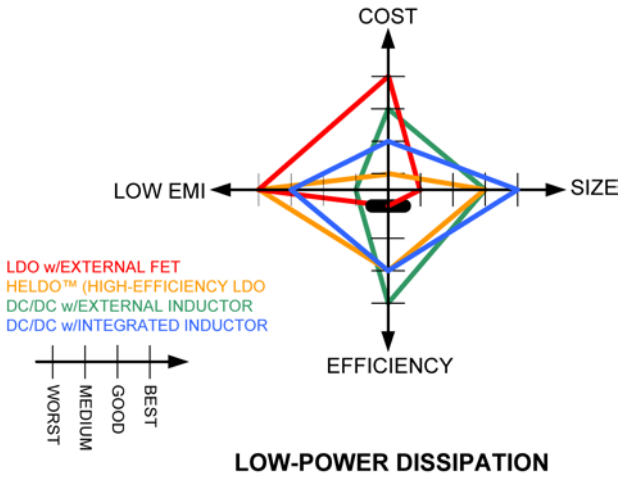

Figure 3. KSZ9021 Distribution Solutions

See Figure 4 for step-by-step, design constraint-dependent solution selection.

Application Constraint	LDO w/External FET	HELDO™	DC/DC External Inductor	DC/DC Internal Inductor
Efficiency	36%	~80%	>90%	~80%
Size	~650mm^2	~100mm^2	~100mm^2	<50mm^2
EMI	Very Low	Very Low	Caution	Low
Cost	Very Low	High	Low	Medium

Table 3. KSZ9021 Distribution Solutions

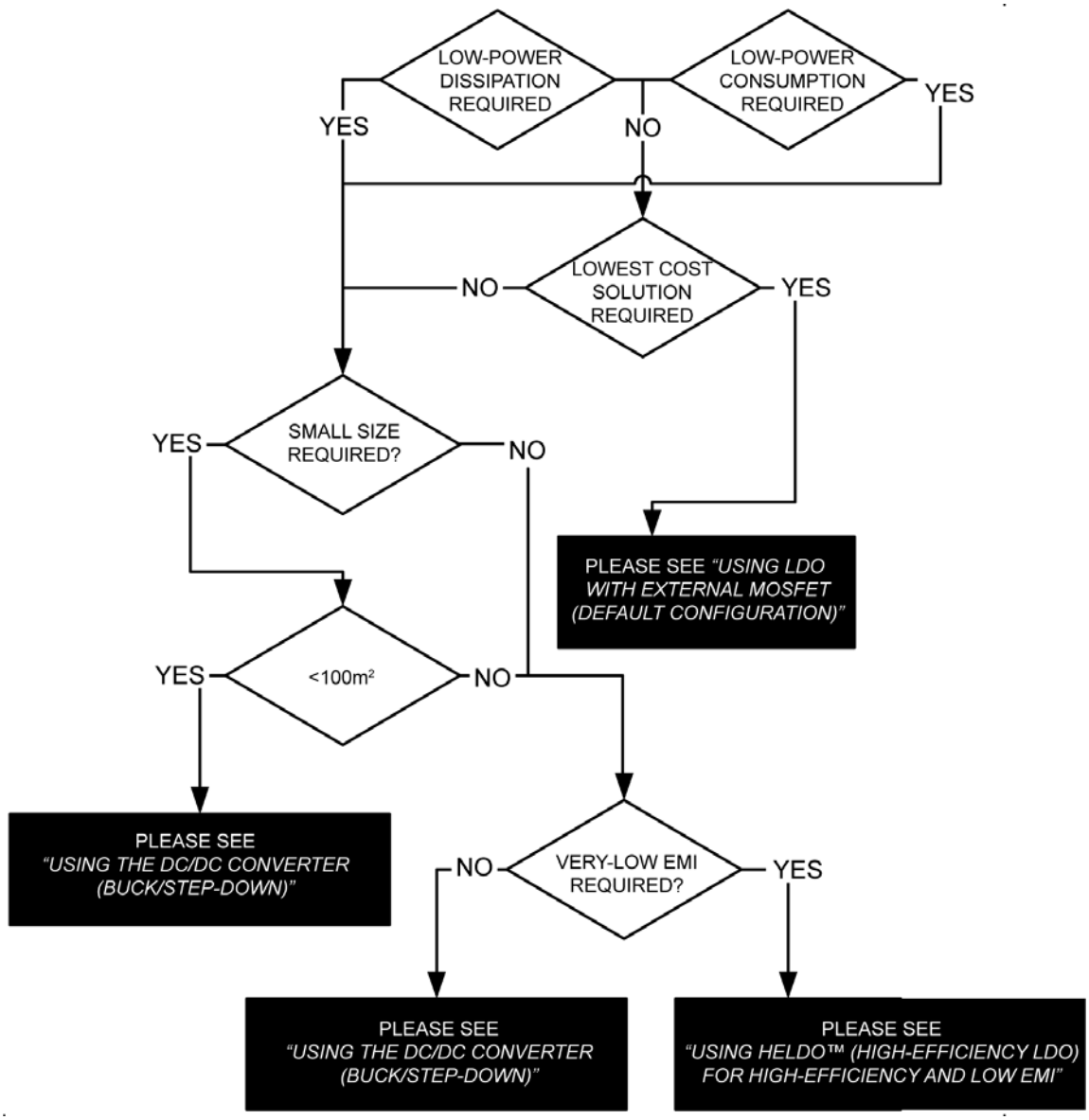

Figure 4. Design Constraint-Dependent Solution Selection

Using Internal LDO with External MOSFET (Default Configuration)

Using an LDO or external MOSFET does imply a low efficiency and then high power dissipation. Equation 1 illustrates power dissipation for an LDO:

$$P_{LOSSES(MAX)} = (V_{AVDDH(MAX)} - V_{DVDDL(MAX)}) \times I_{DVDDL+AVDDL(MAX)}$$

$$P_{LOSSES(MAX)} = 1.55W \quad \text{Eq. 1}$$

100% of this power must be dissipated by the MOSFET. The maximum ambient temperature achievable assuming the worst case scenario is as noted in Equation 2:

$$T_{AMBIENT(MAX)} = T_{JUNCTION(MAX)} - (R\theta_{JA} \times P_{LOSSES(MAX)}) \quad \text{Eq. 2}$$

With $T_{JUNCTION(MAX)}$ being the maximum junction temperature of the MOSFET and RθJA the junction to ambient thermal resistance of the MOSFET.

The MOSFET recommended in the KS9021 evaluation board design is Fairchild FDT434P with 1inch^2 PCB heatsink. The thermal resistance is 42°C/W. In this case, the design is safe for 85°C ambient temperature around the PHY. As shown in Figure 5, the commercial temperature range (up to 70°C) allows a maximum thermal resistance θ_{JA} of 52°C/W.

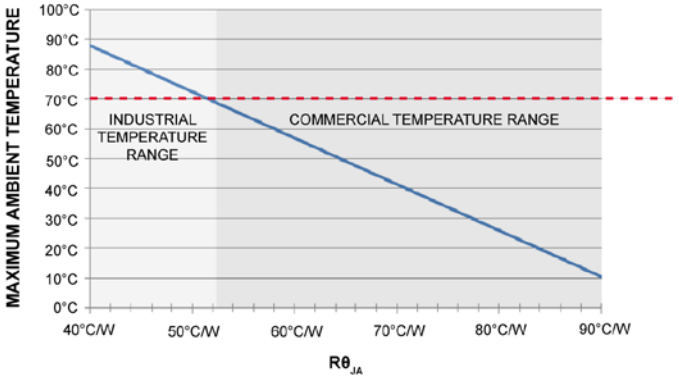

Figure 5. Maximum Ambient Temperature (°C) vs. FET Thermal Resistance (°C/W)

From a system efficiency standpoint, the performances are not optimized. PHY sub-system efficiency is driven by 1.2V rail performances.

Power rail efficiency is given in Equation 3:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{VI_N \times I_{IN}} \quad \text{Eq. 3}$$

For an LDO, output current is equal to input current, as shown in Equation 4:

$$\eta = \frac{V_{OUT}}{V_{IN}} = \frac{1.2V}{3.3V} \cong 36\% \quad \text{Eq. 4}$$

In default configuration, 1.2V rail efficiency is 36%, driving the need of the MOSFET with big package (SOT223) and big heatsink (1inch^2).

Important parameters to consider when choosing the MOSFET include:

- MOSFET package thermal resistance must comply with Figure 4, depending on maximum ambient temperature of the application (53°C/W for commercial temperature range and 42°C/W for industrial temperature range.
- The MOSFET must allow driving the current (i.e. ≈700mA) at 1.9V VDS (LDO minimum drop-out) with a –VGS below 2.5V. Figure 6 illustrates the FDT434P example that is used in the KSZ9021 evaluation board. This parameter is particularly important to note as the MOSFET must be allowed to drive the current required with the swing available on the gate drive at the minimum LDO voltage drop. Additionally, VDSMIN is (3.3V – 5%) – 1.26V ≈ 1.9V and the MOSEFT must be able to sustain approximately 700mA at 1.9V VDS.

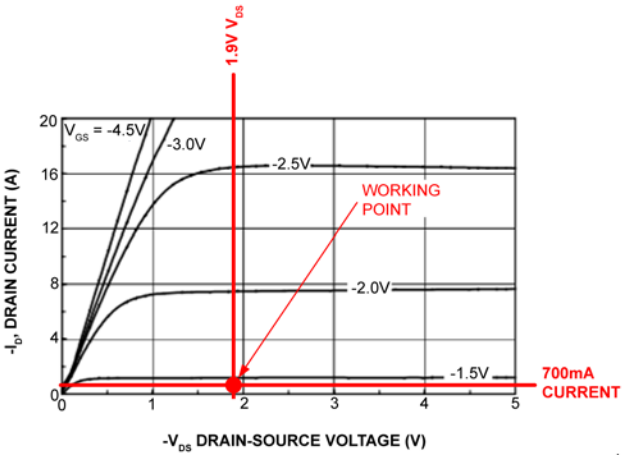

Figure 6. FDT434P Example Used In KSZ9021 Evaluation Board

Per Figure 6, working point shows the MOSFET allows to drive the current at 1.9V voltage drop with a –VGS below 1.5V. The input capacitance (CISS) must be below 2nF and the maximum RDSON at 125°C of junction temperature must not exceed 1Ω.

It is recommended to add a 100kΩ resistor between the MOSFET gate and source in order to avoid any large inrush current from 3.3V when the LDO powers up.

Figure 7 (KSZ9021GN), Figure 8 (KSZ9021GQ), Figure 9 (KSZ9021RN), and Figure 10 (KSZ9021RL) show the recommended power supply design for each rail. This design can be used as a baseline for decoupling capacitors. However, it is important to note that AVDDL rail does not feature any ferrite bead when using LDO controller with external MOSFET because it is used internally as the LDO controller feedback input. Ferrite bead might degrade LDO load regulation in this case.

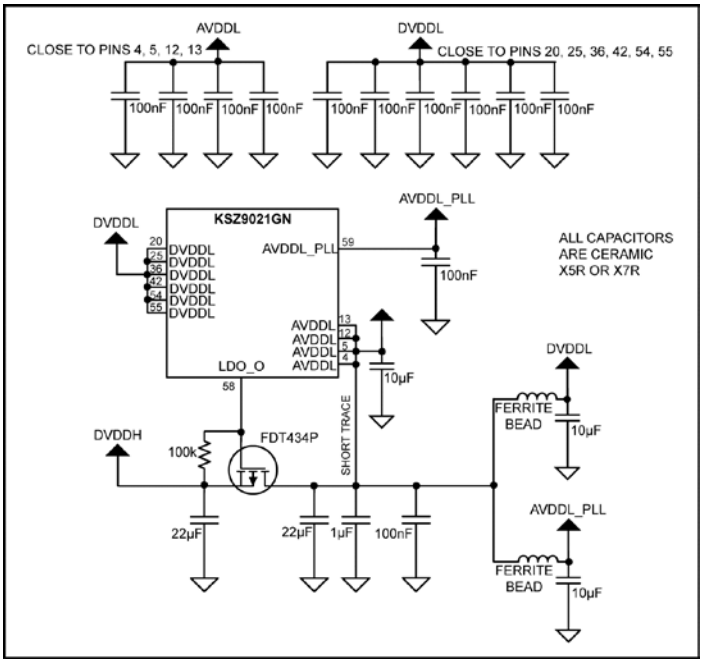

Figure 7. KSZ9021GN Internal LDO Controller Driving External MOSFET

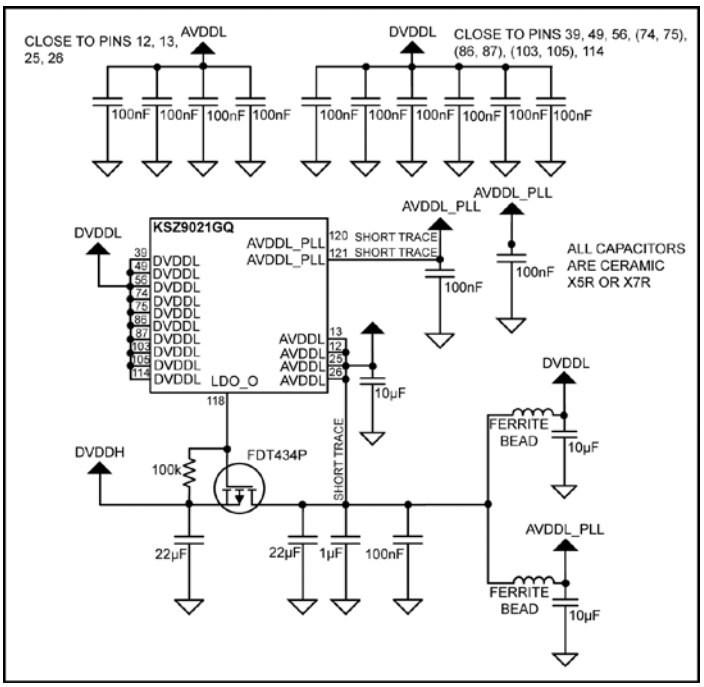

Figure 8. KSZ9021GQ Internal LDO Controller Driving External MOSFET

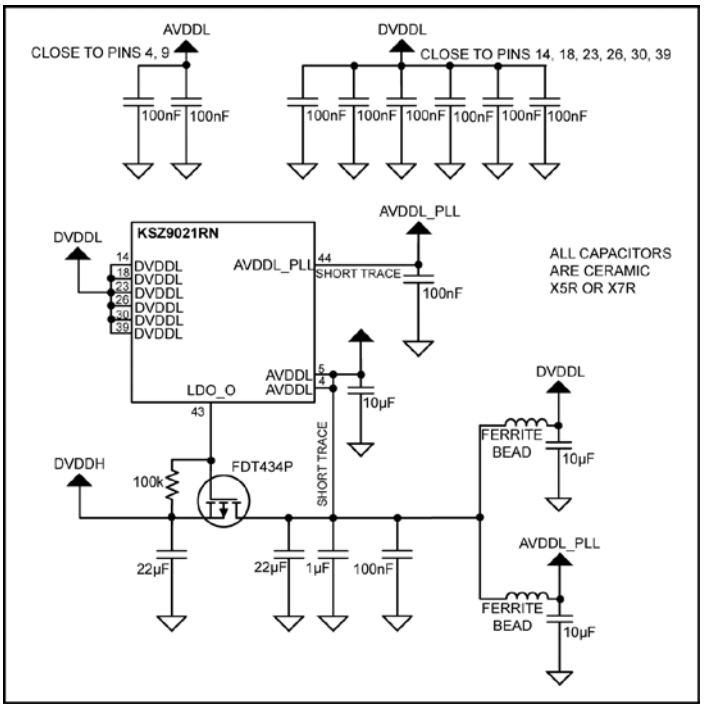

Figure 9. KSZ9021RN Internal LDO Controller Driving External MOSFET

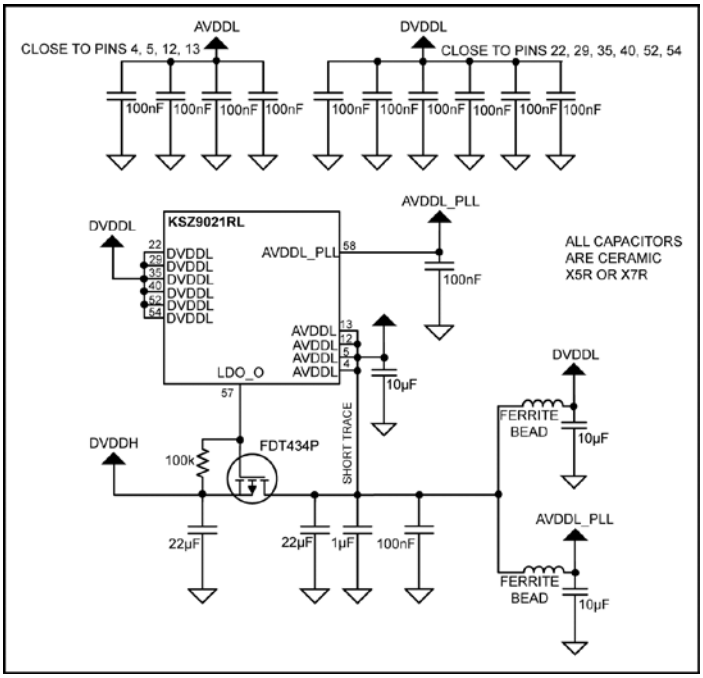

Figure 10. KSZ9021RL Internal LDO Controller Driving External MOSFET

Using the DC/DC Converter (Buck/Step-Down)

Using a DC/DC converter instead of LDO (with external MOSFET) for 1.2V rail will enhance significantly efficiency. This will lower current consumption from 3.3V and power dissipation as well. In Industrial types of application, ambient temperature becomes an issue. That is why it can be very important to lower as much as possible all sources of heat around critical components (CPU, Memories, Connectivity etc…). Figure 3 summarizes advantages and disadvantages of such solution.

Two options are offered depending on cost and size. Those options provide much better efficiency and smaller size compared to LDO with external FET.

Figure 11 shows the lowest cost solution that provides highest efficiency (>90%) with a small size (around 100mm^2). In order to limit emissions, special care must be taken for layout and a shielded inductor has to be chosen.

Design guidelines, reference layout and full bill of material can be found at the end of MIC23150 datasheet: http://www.micrel.com/_PDF/mic23150.pdf.

Evaluation board document is available here:

http://www.micrel.com/_PDF/Eval-Board/mic23150_eb.pdf.

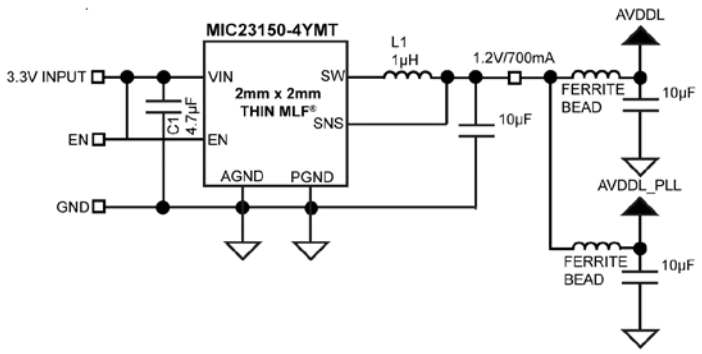

Figure 11. DC/DC Buck Converter with External Inductor

The MIC23150 runs at 4MHz switching frequency which provides best optimized solution in terms of size and cost without compromising on performance. 4MHz switching frequency ensures low peak current into the inductor with a low inductance value. The issue of inductor saturation is that effective inductance value drops very quickly when the magnetic circuit starts to saturate. The main consequence of this is that it leads to high temperature rise in the inductor and overall bad performance. On one hand, a shielded inductor is usually required to reduce DCDC converter emissions and to avoid any magnetic coupling between the inductor and components/traces around it. On the other hand, shielded inductors exhibit lower saturation current compared to non-shielded ones. One way to overcome the issue of low saturation current with shielded inductors is to raise switching frequency to lower the peak current.

As a conclusion, high frequency such as 4MHz, for relatively low currents (<2A), provide best balanced solution to find small and low cost shielded inductors without significantly impacting efficiency performance.

Another good point for high switching frequency is that it allows using smaller input and output capacitors while also keeping very good load regulation and output ripple. The main issue with high speed digital ICs, is that they require very good load regulation during large and fast current transients. 4MHz switching frequency and constant on-time (COT) architecture in the MIC23150 allows handling load transient in less than a switching cycle; that is, in less than 250ns.

Assuming the following parameters:

- 4MHz switching frequency (250ns switching period)
- 1µH +/-20% inductor
- 3.3V +/-5% input voltage
- 1.2V +/-5% output voltage

We obtain, as given by following equation, the maximum on time (maximum duty cycle):

$$T_{ON_{MAX}} = \frac{V_{OUT_{MAX}}}{V_{IN_{MIN}}} = \frac{1.26V}{3.3V + 5\%}.250ns$$

$$T_{ON_{MAX}} = 37\%.250ns = 91ns \quad \text{Eq.5}$$

The maximum ripple current in inductor (AC domain) is then given by Equation 6:

$$\Delta I_{L_{MAX}} = \frac{V_{IN} - V_{OUT}}{L_{MIN}} \times T_{ON_{MAX}} = \frac{3.3V - 1.2V}{1.10\text{^}-6 - 20\%}.91ns$$

$$\Delta I_{L_{MAX}} = 238mA \quad \text{Eq. 6}$$

The inductor minimum saturation current is:

$$I_{SAT_{MIN}} = (I_{LOAD_{MAX}} + \frac{\Delta IL_{MAX}}{2}) + 20\%$$

$$I_{SAT_{MIN}} = (700mA + 119mA) \cdot 1.20 \approx 1A \quad \text{Eq. 7}$$

Table 4 gives some proposal regarding inductors that can be used:

Manufacturer	Part Number	Description
TDK	MLP2016S1R0MT VLS201610ET-1R0N	2x1.6x1mm 2x1.6x1mm
Coilcraft	EPL2010-102ML	2.2x2.2x1.05mm
Vishay	IFSC0806AZER1R0M01	2x1.6x1mm Not Shielded
Bourns	CC453232-1R0KL SRU2009-1R0Y	4.2x3.2x3.2mm 2.8x2.8x0.9mm

Table 4. MIC23150 Proposed Inductors

Figure 12 shows same implementation with a DCDC Buck converter that does integrate the inductor. As a consequence, the package acts as a shield and switching power paths are isolated from the outside world. The performance compared to a DCDC converter with external inductor is:

- Slightly lower efficiency: 80%
- Lower EMI (emissions are contained within the package)
- Smaller size (<50mm^2)

Design guidelines, reference layout and full bill of material can be found at the end of MIC33153 datasheet: http://www.micrel.com/_PDF/mic33153.pdf.

Evaluation board document is available here:

http://www.micrel.com/_PDF/Eval-Board/mic33153_eb.pdf.

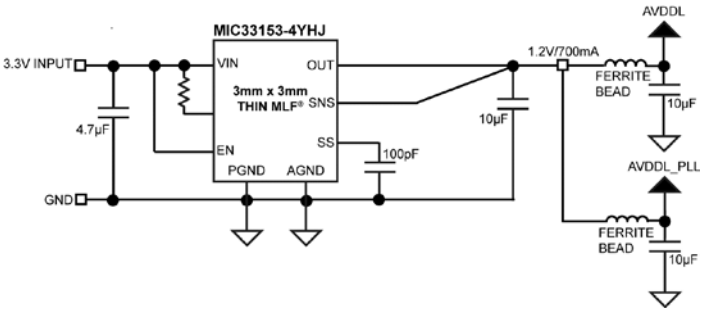

Figure 12. MIC33153 DC/DC Buck Converter with Integrated Inductor

Using HELDO™ (High-Efficiency LDO) for High-Efficiency and Low EMI

HELDO™ (High-Efficiency LDO) is a unique solution that allows getting DC/DC converter efficiency merged with LDO advantages (fast load/line regulation, ultra-low noise, and low EMI).

Figure 13 shows how this can be achieved. The HELDO™ integrates a DC/DC buck converter and its inductor into a single package. The buck converter feeds the input of an ultra-fast/ultra-low-noise LDO that filters out most noise from the buck converter. As a consequence, the device operates like an LDO, but features the efficiency of a DC/DC buck converter.

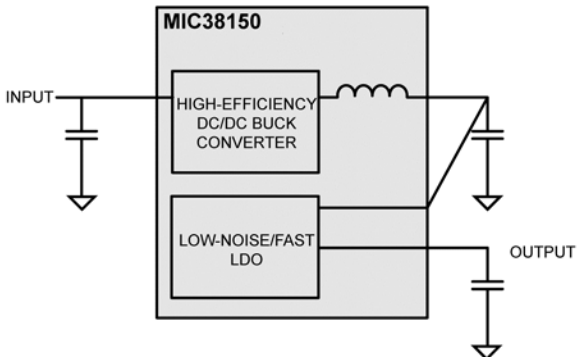

Figure 13. HELDO™ Integration into Single Package

Figure 15 illustrates the implementation. The performance compared to the DC/DC buck converter with external inductor is:

- Slightly lower efficiency: 80%
- Ultra-low EMI (emissions are contained within the package and filtered by integrated LDO). See Figure 14:

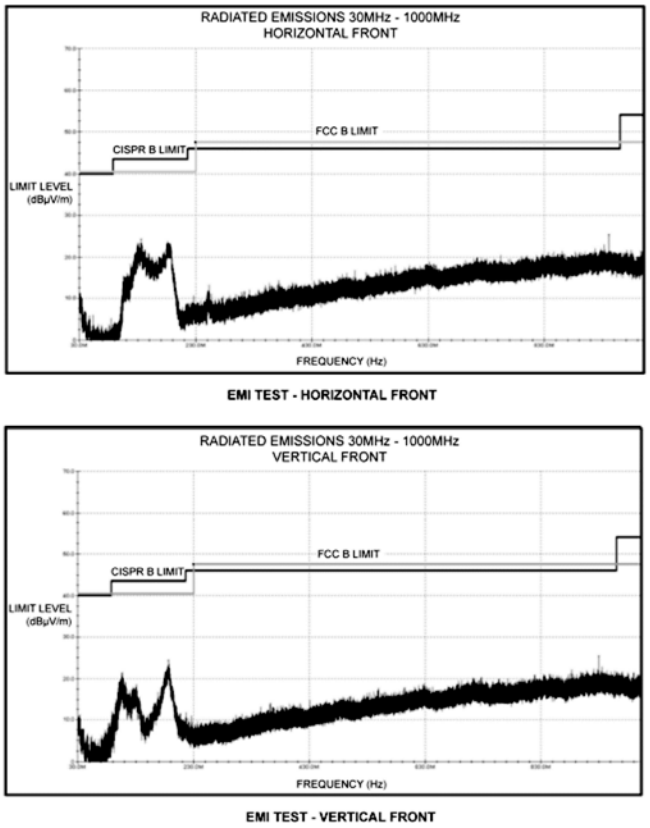

Figure 14. MIC38150 EMI Profiles

Design guidelines, reference layout, full bill of material and performance can be found at the end of MIC38150 datasheet: http://www.micrel.com/_PDF/mic38150.pdf.

Evaluation board document is available here:

http://www.micrel.com/_PDF/Eval-Board/mic38150_eb.pdf.

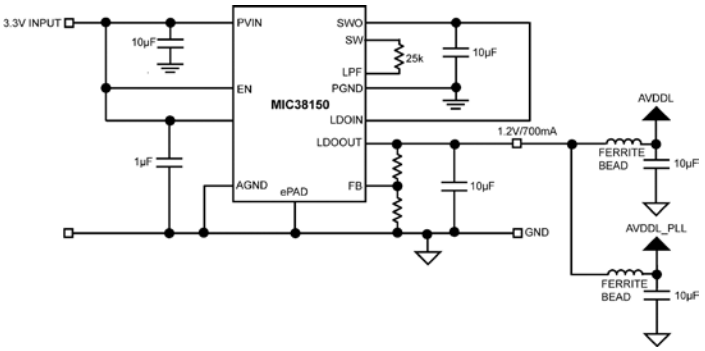

Figure 15. MIC38150 Implementation Schematic

Revision History

Revision	Date	Changes
1.0	October 2012	First Release

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