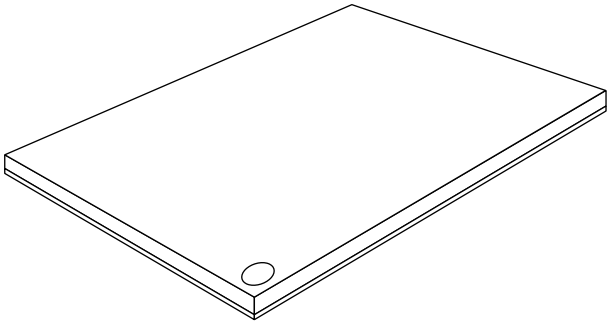
NAND Flash Memory

MT29F2G08AAD, MT29F2G16AAD, MT29F2G08ABD, MT29F2G16ABD

Features

- Open NAND Flash Interface (ONFI) 1.0-compliant
- Single-level cell (SLC) technology
- Organization
  - Page size:
    - x8: 2,112 bytes (2,048 + 64 bytes)
    - x16: 1,056 words (1,024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Device size: 2Gb: 2,048 blocks
- READ performance
  - Random READ: 25µs
  - Sequential READ: 25ns (3.3V)
  - Sequential READ: 35ns (1.8V)
- WRITE performance
  - PROGRAM PAGE: 220µs (TYP, 3.3V)
  - PROGRAM PAGE: 300µs (TYP, 1.8V)
  - BLOCK ERASE: 500µs (TYP)
- Data retention: 10 years
- Endurance: 100,000 PROGRAM/ERASE cycles
- First block (block address 00h) guaranteed to be valid with ECC when shipped from factory[1]
- Industry-standard basic NAND Flash command set
- Advanced command set:
  - PROGRAM PAGE CACHE MODE
  - PAGE READ CACHE MODE
  - One-time programmable (OTP) commands
  - BLOCK LOCK (1.8V only)
  - PROGRAMMABLE DRIVE STRENGTH
  - READ UNIQUE ID
- Operation status byte provides a software method of detecting:
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: write protect entire device
- RESET required as first command after power-up
- INTERNAL DATA MOVE operations supported
- Alternate method of device initialization (Nand_Init) after power up[4] (Contact Factory)

Figure 1: 63-Ball VFBGA



Options

- Density[2]: 2Gb (single die)
- Device width: x8, x16
- Configuration:

# of die	# of CE#	# of R/B#	I/O
1	1	1	Common

- VCC: 2.7–3.6V
- VCC: 1.65–1.95V
- Package
  - 48-pin TSOP type I CPL[3] (lead-free plating, 3.3V only)
  - 63-ball VFBGA (lead-free, 1.8V only)
- Operating temperature:
  - Commercial (0°C to +70°C)
  - Extended (–40°C to +85°C)

1. See “Error Management” on page 61.
2. For part numbering and markings, see Figure 2 on page 2 and Figure 3 on page 3.
3. CPL = center parting line
4. Available only in 1.8V VFBGA package.

Part Numbering Information

Micron® NAND Flash devices are available in several different configurations and densities (see Figure 2).

Figure 2: Part Number Chart (3.3V)

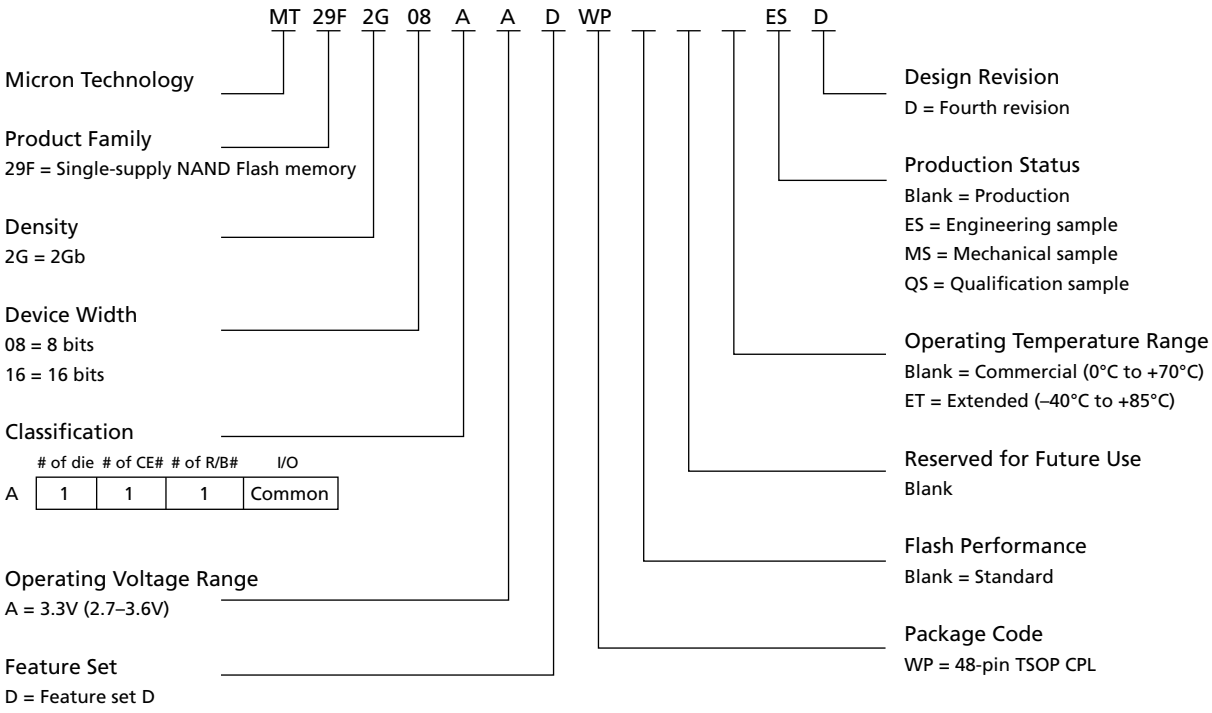
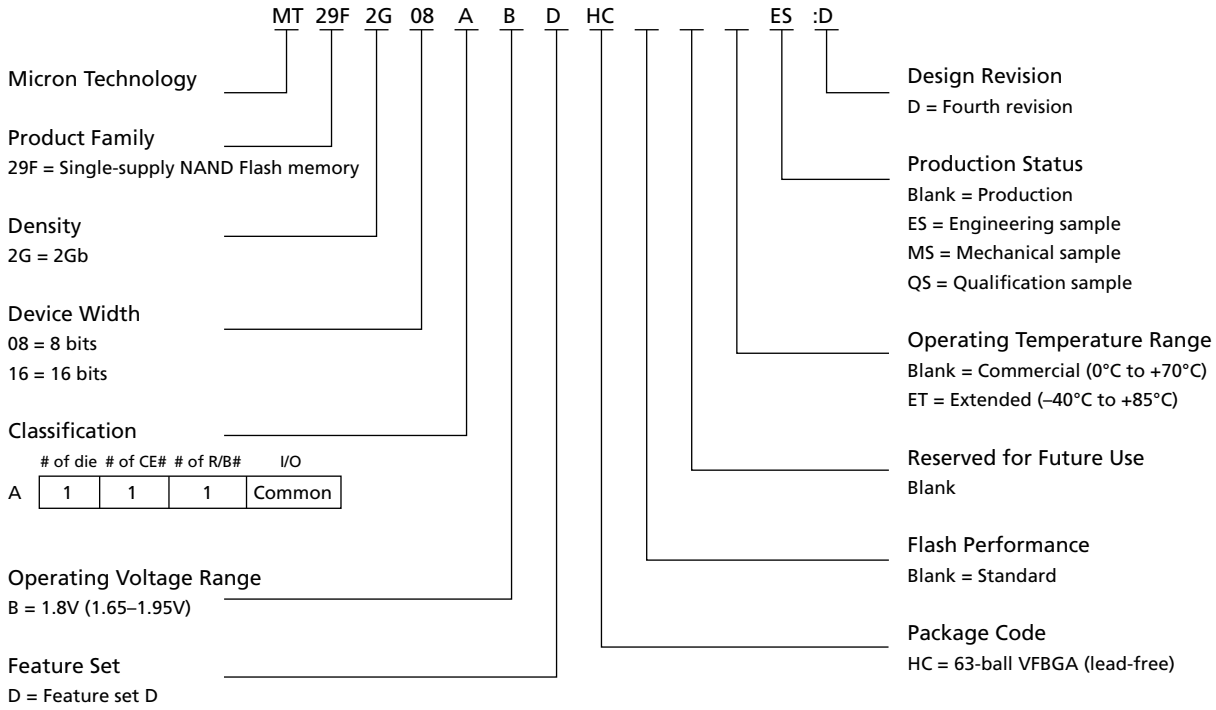


Figure 3: Part Number Chart (1.8V)



Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part number is offered and valid by using the Micron Parametric Part Search Web site at www.micron.com/products/parametric. If the device required is not on this list, contact the factory.

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General Description

NAND Flash technology provides a cost-effective solution for applications requiring high-density, solid-state storage. The MT29F2GxxAxD is a 2Gb NAND Flash memory device. Micron NAND Flash devices include standard NAND Flash features as well as new features designed to enhance system-level performance.

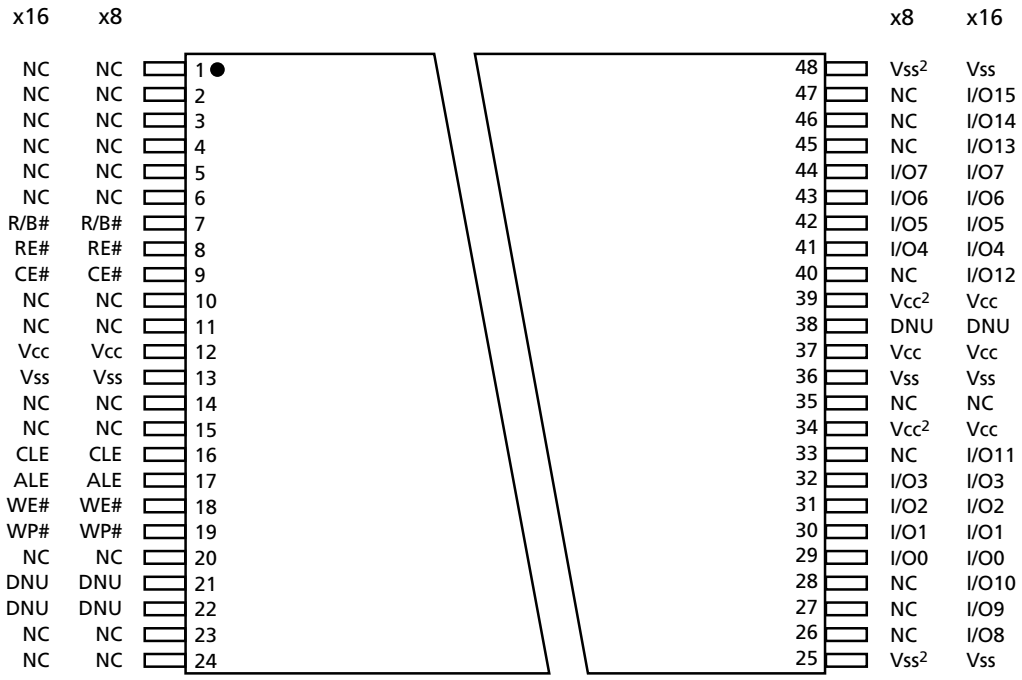
Micron NAND Flash devices use a highly multiplexed 8-bit bus (I/O[7:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND Flash command bus interface protocol. Additional pins control hardware write protection (WP#), monitor the device ready/busy (R/B#) state, and enable block lock functionality (LOCK).

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

The MT29F2G device contains 2,048 blocks. Each block is subdivided into 64 programmable pages. Each page consists of 2,112 bytes. The pages are further divided into a 2,048-byte data storage region with a separate 64-byte area. The 64-byte area is typically used for error management functions.

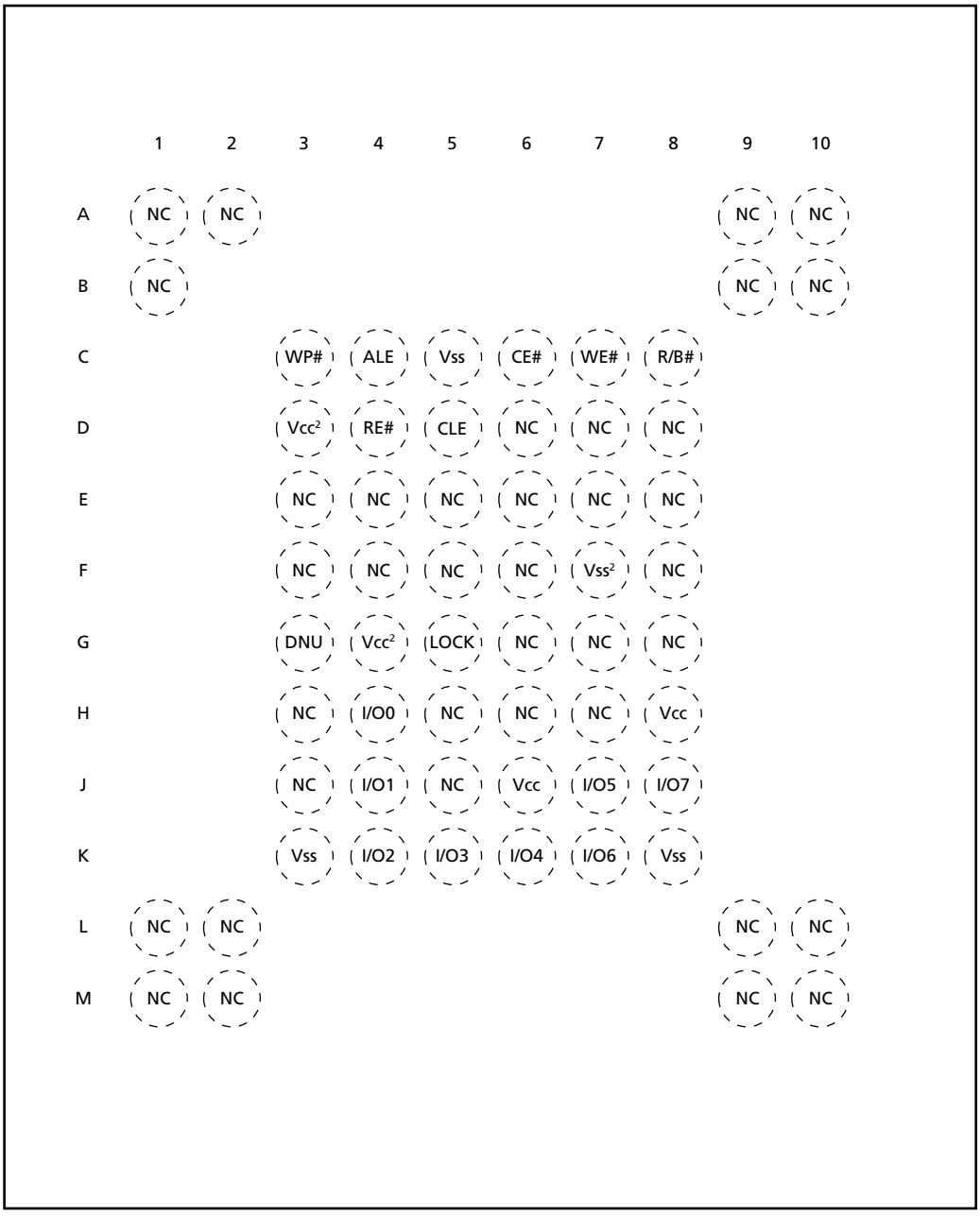
The contents of each page can be programmed in tPROG (TYP), and an entire block can be erased in tBERS (TYP). On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. PROGRAM/ERASE endurance is specified at 100,000 cycles using appropriate error correction code (ECC) and error management.

Figure 4: Pin Assignment 48-Pin TSOP Type 1 CPL (Top View)



Notes: 1. For package dimensions, see Figure 91 on page 99.
2. These pins might not be bonded in the package. However, Micron recommends that the customer connect these pins to the designated external sources for ONFI compatibility.

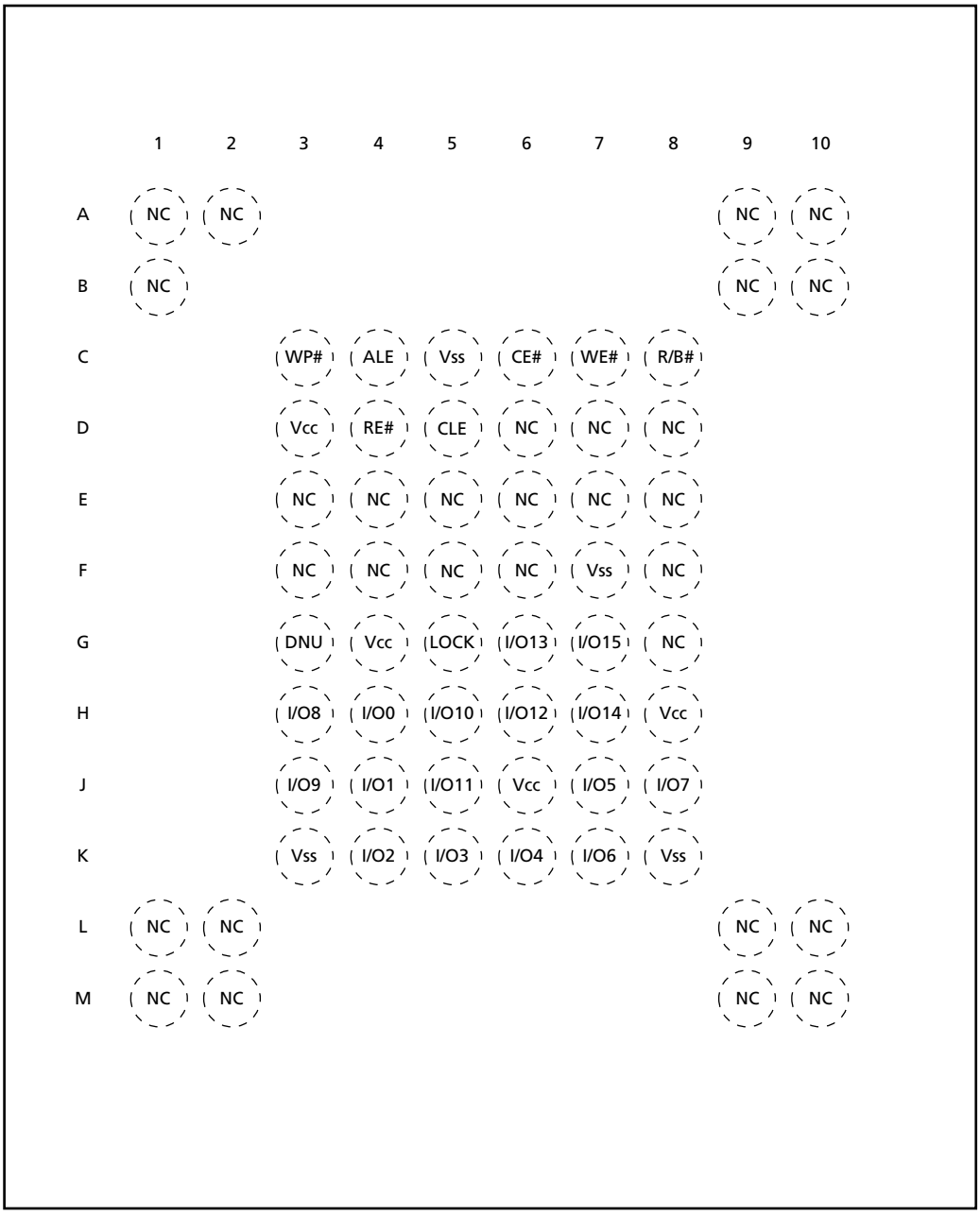
Figure 5: Ball Assignment: 63-Ball VFBGA (x8)



Top View, Ball Down

Notes: 1. For package dimensions, see Figure 77 on page 87
2. These pins might not be bonded in the package. However, Micron recommends that the customer connect these pins to the designated external sources for ONFI compatibility.

Figure 6: Ball Assignment: 63-Ball VFBGA (x16)



Top View, Ball Down

Notes: 1. For package dimensions, see Figure 77 on page 87.

Table 1: Signal Descriptions

Symbol	Type	Description
ALE	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE#	Input	Chip enable: This gates transfers between the host system and the NAND Flash device. After the device starts a PROGRAM or ERASE operation, CE# can be de-asserted. See "Bus Operation" on page 18 for additional operational details.
CLE	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
LOCK	Input	When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable the BLOCK LOCK, connect LOCK to V_{SS} during power-up, or leave it disconnected (internal pull-down).
RE#	Input	Read enable: This gates transfers from the NAND Flash device to the host system.
WE#	Input	Write enable: This gates transfers from the host system to the NAND Flash device.
WP#	Input	Write protect: This protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW.
I/O[7:0] (x8) I/O[15:0] (x16)	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.
R/B#	Output	Ready/busy: This is an open-drain, active-LOW output that uses an external pull-up resistor. R/B# is used to indicate when the chip is processing a PROGRAM or ERASE operation. It is also used during READ operations to indicate when data is being transferred from the array into the serial data register. When these operations have completed, R/B# returns to the high-impedance state.
V_{CC}	Supply	V_{CC}: This is the power supply.
V_{SS}	Supply	V_{SS}: This is the ground connection.
NC	–	No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	–	Do not use: DNUs must be left unconnected.

Architecture

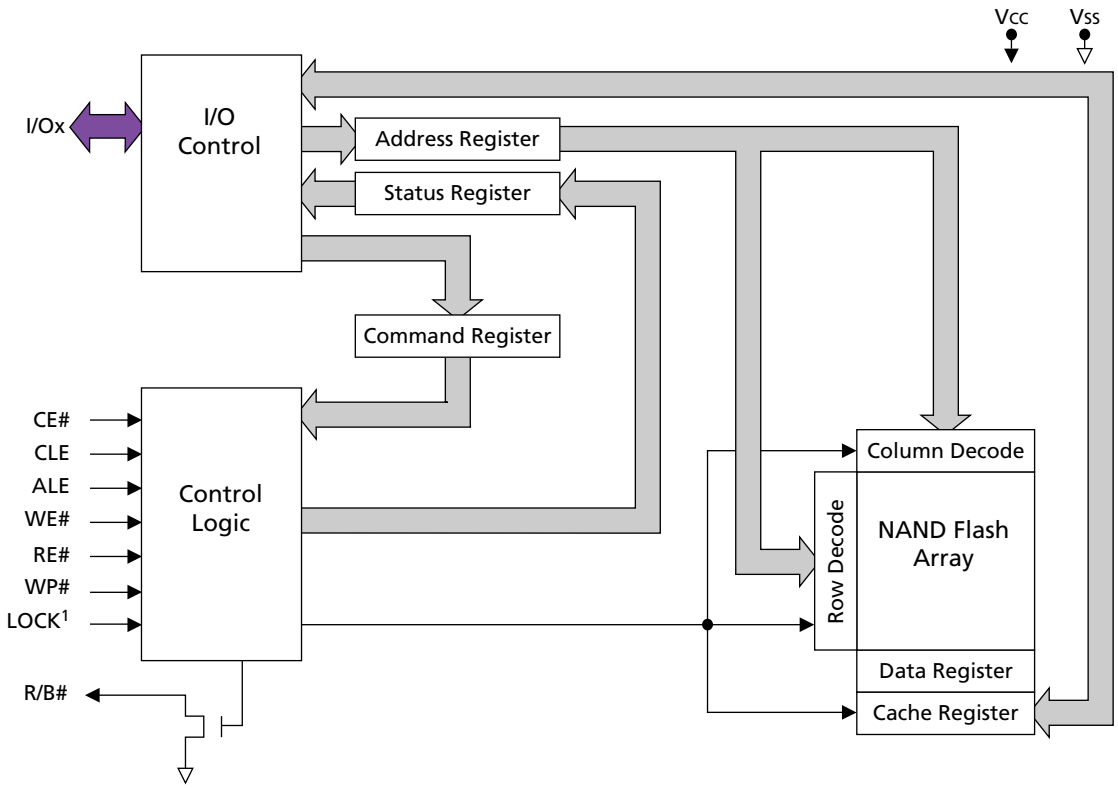
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. This provides a memory device with a low pin count. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder or a column decoder to select a row address or a column address, respectively.

The data are transferred to or from the NAND Flash memory array, byte by byte (x8) or word by word (x16), through a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data, whereas the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations and is erased in block-based operations. During normal page operations, the data and cache registers are tied together and act as a single register. During cache operations the data and cache registers operate independently to increase data throughput.

These devices also have a status register that reports the status of device operation.

Figure 7: NAND Flash Functional Block Diagram



Notes: 1. LOCK pin is used for 1.8V device.

Addressing

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a 5-cycle sequence as shown in Tables 4 and 5, on pages 16 and 17. See Figure 8 for additional memory mapping and addressing details.

Memory Mapping

Figure 8: Memory Map (x8)

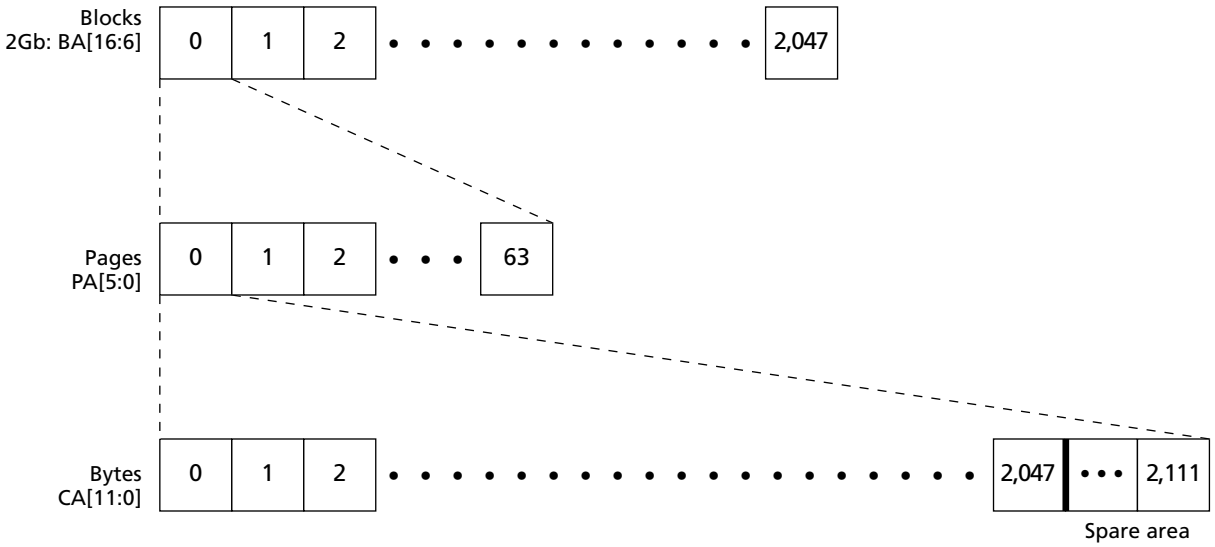


Table 2: Operational Example (x8)

Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x000000083F	0x0000000840–0x0000000FFF
0	1	0x0000010000	0x000001083F	0x0000010840–0x0000010FFF
0	2	0x0000020000	0x000002083F	0x0000020840–0x0000020FFF
…	…	…	…	
2,046	62	0x01FFFE0000	0x01FFFE083F	0x01FFFE0840–0x01FFFE0FFF
2,047	63	0x01FFFF0000	0x01FFFF083F	0x01FFFF0840–0x01FFFF0FFF

Notes: 1. As shown in Table 4 on page 16, the high nibble of ADDRESS cycle 2 has no assigned address bits; however, these 4 bits must be held LOW during the ADDRESS cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in ADDRESS cycle 2 even though they do not have address bits assigned to them.

2. The 12-bit column address is capable of addressing from 0 to 2,047 bytes on a x8 device; however, only bytes 0 through 2,111 are valid. Bytes 2,112 through 4,095 of each page are "out of bounds," do not exist in the device, and cannot be addressed.

Figure 9: Memory Map x16

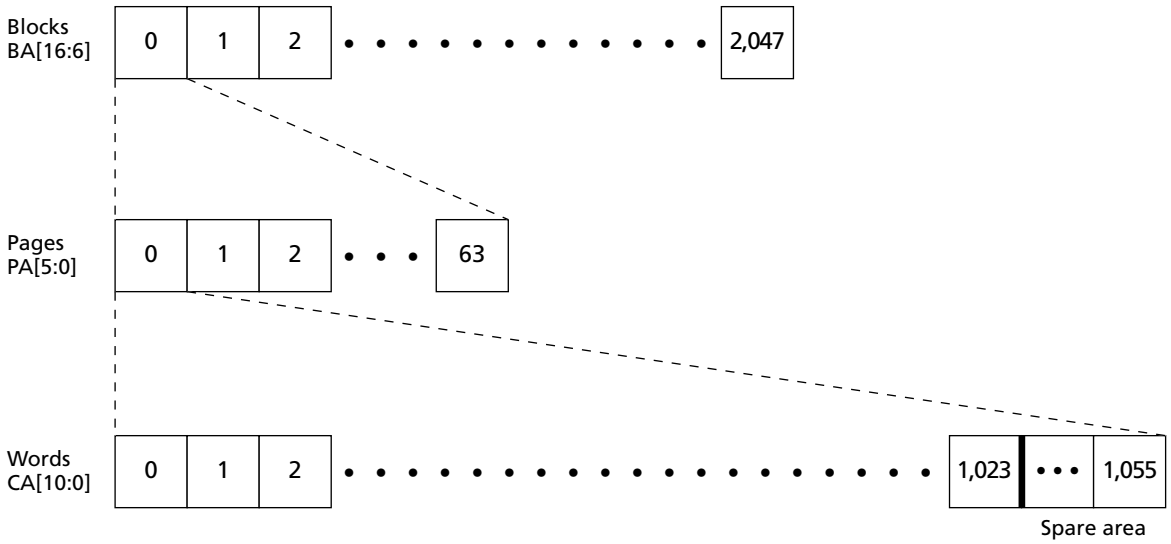


Table 3: Operational Example (x16)

Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x000000041F	0x0000000420–0x0000000FFF
0	1	0x0000010000	0x000001041F	0x0000010420–0x0000010FFF
0	2	0x0000020000	0x000002041F	0x0000020420–0x0000020FFF
…	…	…	…	
2,046	62	0x01FFFE0000	0x01FFFE041F	0x01FFFE0420–0x01FFFE0FFF
2,047	63	0x01FFFF0000	0x01FFFF041F	0x01FFFF0420–0x01FFFF0FFF

Notes: 1. As shown in Table 5 on page 17, the upper 5 bits of ADDRESS cycle 2 have no assigned address bits; however, these 5 bits must be held LOW during the ADDRESS cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in ADDRESS cycle 2 even though they do not have address bits assigned to them.

2. The 11-bit column address is capable of addressing from 0 to 2,047 words on x16 devices; however, only words 0 through 1,055 are valid. Words 1,056 through 2,048 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

Array Organization

Figure 10: Array Organization for MT29F2G08AxD (x8)

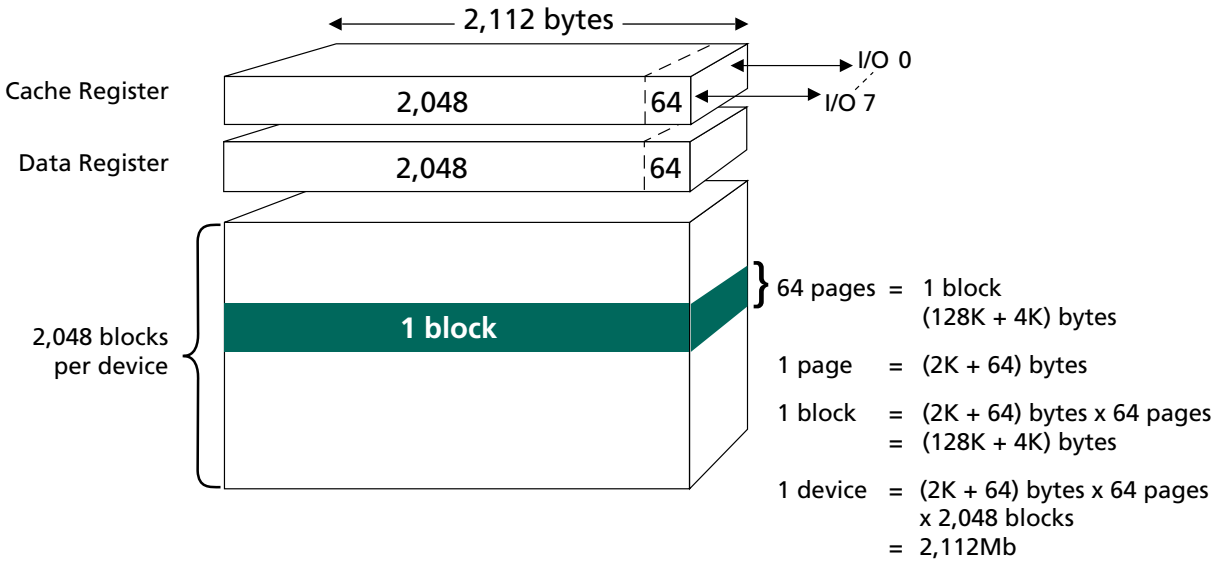


Table 4: Array Addressing: MT29F2G08AxD

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11[1]	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

Notes: 1. If CA11 is "1," then CA[10:6] must be "0."
2. Block address concatenated with page address = actual page address; CAx = column address; PAx = page address; BAx = block address.

Figure 11: Array Organization for MT29F2G16AxD (x16)

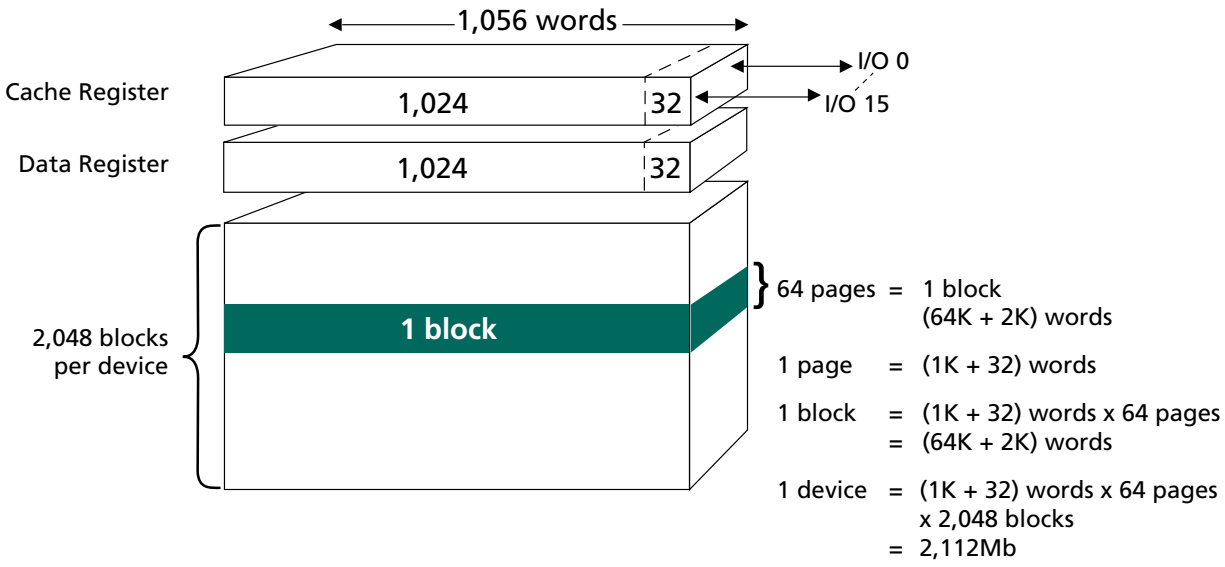


Table 5: Array Addressing: MT29F2G16AxD

Cycle	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	LOW	CA10[1]	CA9	CA8
Third	LOW	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

Notes: 1. If CA10 is "1," then CA[9:5] must be "0."
2. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
3. I/O[15:8] are not used during the addressing sequence and should be driven LOW.

Bus Operation

The bus on the MT29Fxxx devices is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O[15:8] are used only for data in the x16 configuration. Addresses and commands are always supplied on I/O[7:0].

The command sequence normally consists of a COMMAND LATCH cycle, ADDRESS INPUT cycles, and one or more DATA cycles—either READ or WRITE.

Control Signals

CE#, WE#, RE#, CLE, ALE and WP# control NAND Flash device READ and WRITE operations.

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the NAND Flash memory will accept command, address, and data information.

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption. See Figure 61 on page 75 and Figure 69 on page 81 for examples of CE# "Don't Care" operations.

The CE# "Don't Care" operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- The device is not busy

As exceptions, the device accepts the READ STATUS and RESET commands when busy. Commands are transferred to the command register on the rising edge of WE# (see Figure 54 on page 71).

Commands are input on I/O[7:0] only. For devices with a x16 interface, I/O[15:8] must be written with zeros when a command is issued.

Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are LOW, and
- ALE is HIGH

Addresses are input on I/O[7:0]. Bits not part of the address space must be LOW.

For devices with a x16 interface, I/O[15:8] must be written with zeros when an address is issued (see Figure 55 on page 71).

The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Table 7 on page 24).

Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- the device is not busy

Data is input on I/O[7:0] on x8 devices and on I/O[15:0] on x16 devices. See Figure 56 on page 72 for additional data input details.

READs

After a READ command is issued, data is transferred from the memory array to the data register on the rising edge of WE#. R/B# goes LOW for ^{t}R and transitions HIGH after the transfer is complete. When data is available in the data register, it is clocked out of the part by RE# going LOW. See Figure 60 on page 74 for detailed timing information.

The READ STATUS (70h) command or the R/B# signal can be used to determine when the device is ready.

If a controller is using a timing of 30ns or longer for ^{t}RC, use Figure 57 on page 72 for proper timing.

Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of PROGRAM, ERASE, and READ operations. The signal requires a pull-up resistor for proper operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin's open-drain driver enables multiple R/B# outputs to be OR-tied. The READ STATUS command can be used in place of R/B#. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 12 on page 20**).**

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# pin. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10- to 90-percent points on the R/B# waveform, rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance and may be changed if R/B pull-down strength is not set to "full."

Figure 15 on page 21 and Figures 16 and 17 on page 22 depict approximate Rp values using a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

$$Rp\,(\text{MIN, 1.8V part}) = \frac{V_{CC}\,(MAX) - V_{OL}\,(MAX)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

Where ΣI_L is the sum of the input currents of all devices tied to the R/B# pin.

Figure 12: READY/BUSY# Open Drain

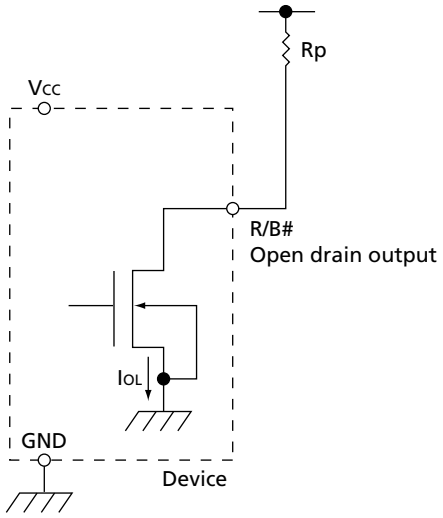
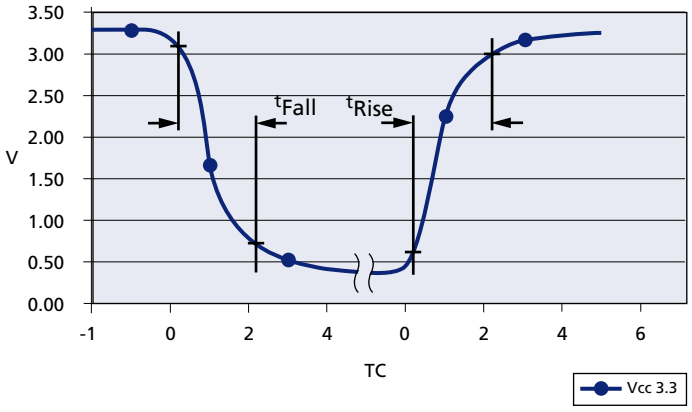
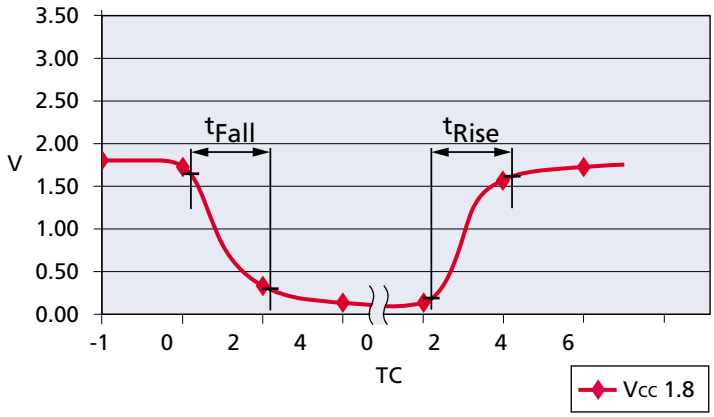


Figure 13: ^{t}Fall and ^{t}Rise (3.3V)



Notes:
1. ^{t}Fall and ^{t}Rise calculated at 10 percent and 90 percent points.
2. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 7ns at 1.8V.
4. See TC values in Figure 17 on page 22 for approximate Rp value and TC.

Figure 14: ^{t}Fall and ^{t}Rise (1.8V)



Notes: 1. ^{t}Fall and ^{t}Rise calculated at 10 percent and 90 percent points.
2. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 7ns at 1.8V.
4. See TC values in Figure 17 on page 22 for approximate Rp value and TC.

Figure 15: I_{OL} vs. Rp (3.3V)

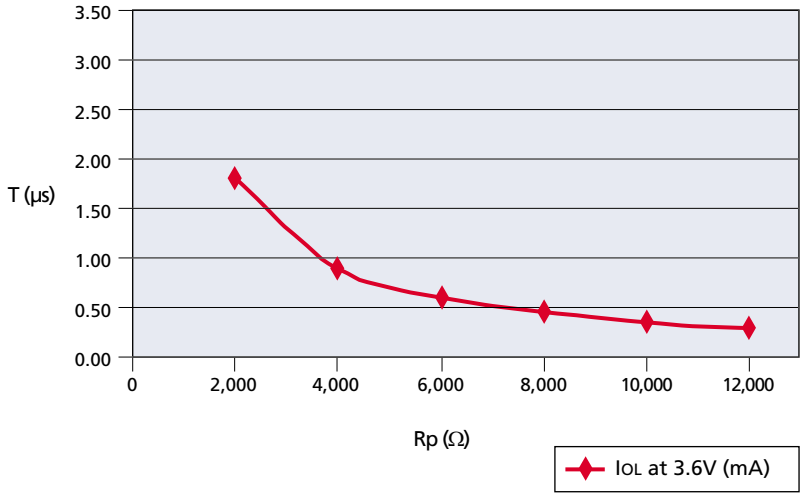


Figure 16: IOL vs. Rp (1.8V)

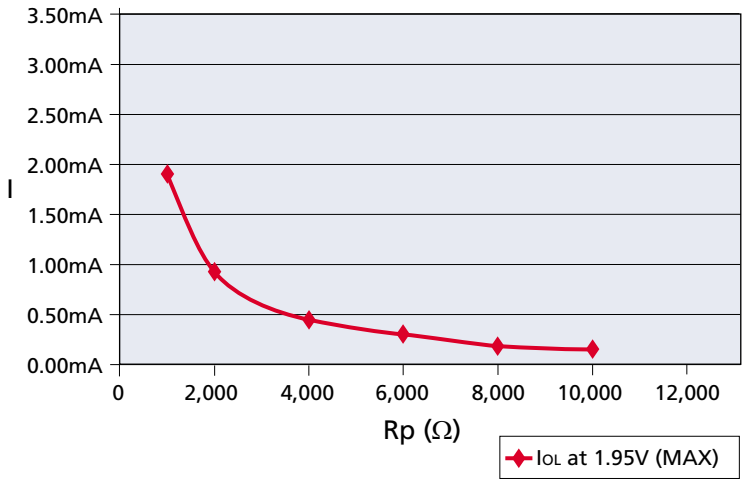


Figure 17: TC vs. Rp

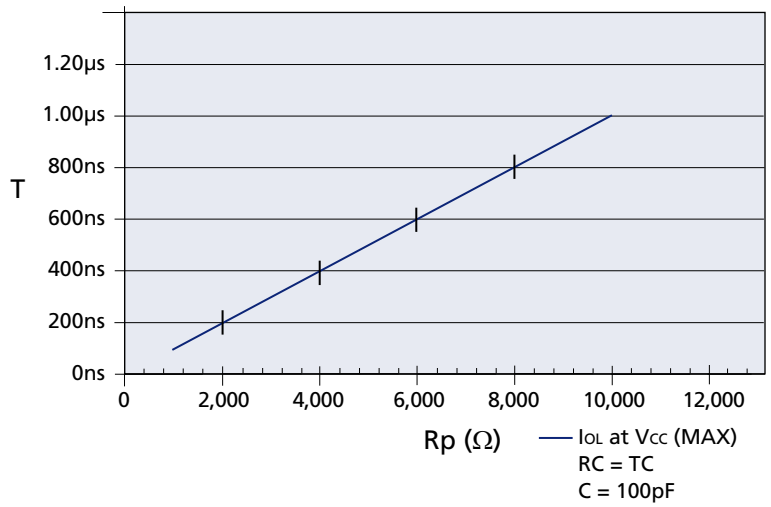


Table 6: Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	LOCK[3]	Mode	
H	L	L	↑	H	X	X	Read mode	Command input
L	H	L	↑	H	X	X		Address input
H	L	L	↑	H	H	X	Write mode	Command input
L	H	L	↑	H	H	X		Address input
L	L	L	↑	H	H	X	Data input	
L	L	L	H	↓	X	X	Sequential read and data output	
X	X	X	H	H	X	X	During read (busy)	
X	X	X	X	X	H	X	During program (busy)	
X	X	X	X	X	H	X	During erase (busy)	
X	X	X	X	X	L	X	Write protect	
X	X	H	X	X	0V/V_{CC}[1]	X	Standby	

Notes: 1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Command Definitions

Table 7: Command Set

Command	Command Cycle 1	Number of Address Cycles	Data Cycles Required[1]	Command Cycle 2	Valid During Busy	Notes
PAGE READ	00h	5	No	30h	No	
PAGE READ CACHE MODE RANDOM	00h	5	No	31h	No	
PAGE READ CACHE MODE SEQUENTIAL	31h	–	No	–	No	
PAGE READ CACHE MODE LAST	3Fh	–	No	–	No	
READ for INTERNAL DATA MOVE	00h	5	No	35h	No	
RANDOM DATA READ	05h	2	No	E0h	No	2
READ ID	90h	1	No	–	No	
READ UNIQUE ID	EDh	1	No	–	No	
READ PARAMETER PAGE	ECh	1	No	–	No	
READ STATUS	70h	–	No	–	Yes	
PROGRAM PAGE	80h	5	Yes	10h	No	
PROGRAM PAGE CACHE MODE	80h	5	Yes	15h	No	
PROGRAM for INTERNAL DATA MOVE	85h	5	Optional	10h	No	
RANDOM DATA INPUT	85h	2	Yes	–	No	3
BLOCK ERASE	60h	3	No	D0h	No	
RESET	FFh	–	No	–	Yes	
OTP DATA PROGRAM	A0h	5	Yes	10h	No	
OTP DATA PROTECT	A5h	5	No	10h	No	
OTP DATA READ	AFh	5	No	30h	No	
GET FEATURES	EEh	1	No	–	No	
SET FEATURES	EFh	1	4	–	No	

Notes: 1. Indicates required data cycles between command cycle 1 and command cycle 2.
2. RANDOM DATA READ command limited to use within a single page.
3. RANDOM DATA INPUT command limited to use within a single page.

Table 8: Block-Lock Command Set

Command	Command Cycle 1	Number of Address Cycles	Command Cycle 2	Number of Address Cycles	Valid During Busy
UNLOCK	23h	3	24h	3	No
BLOCK LOCK	2Ah	–	–	–	No
BLOCK LOCK-TIGHT	2Ch	–	–	–	No
BLOCK LOCK READ STATUS	7Ah	3	–	–	No

READ Operations

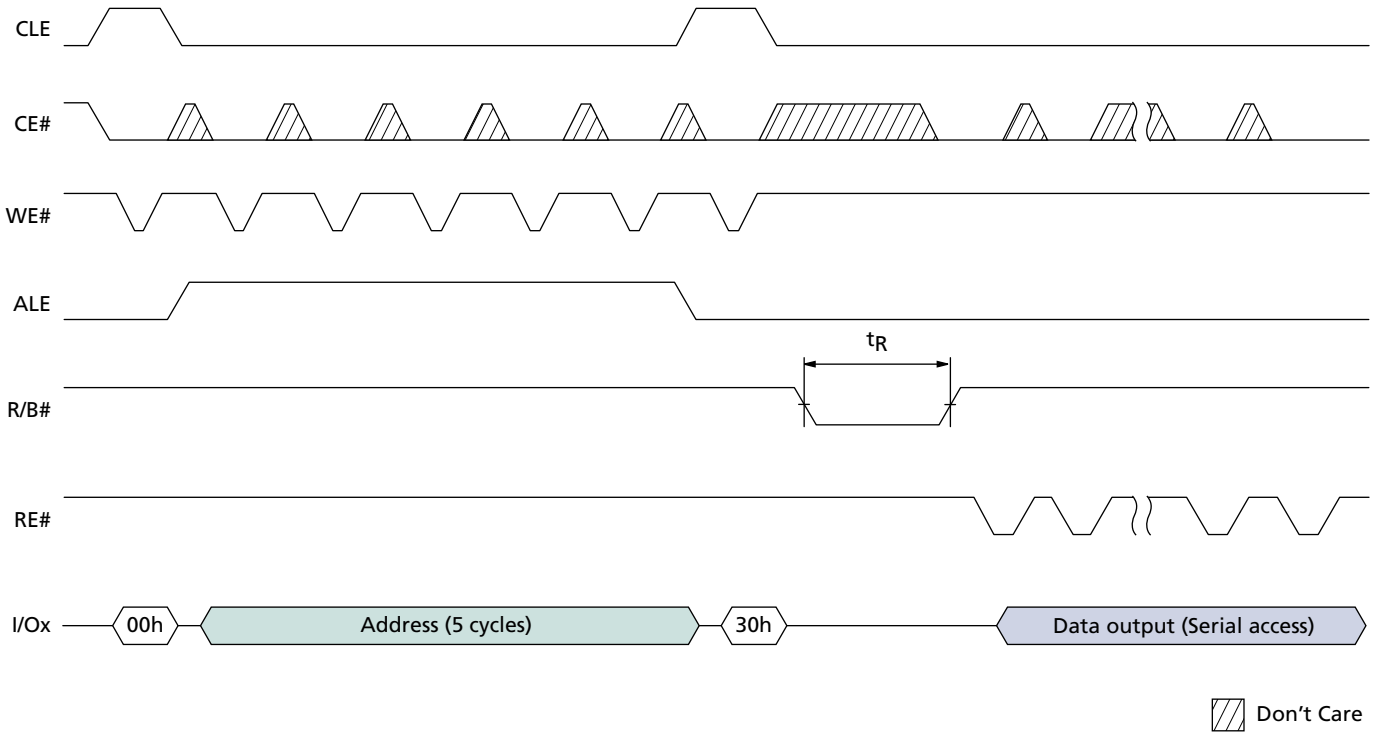
PAGE READ 00h-30h

At power-on, the device defaults to READ mode. To enter READ mode while in operation, write the 00h command to the command register, then write 5 ADDRESS cycles, and conclude with the 30h command.

To determine the progress of the data transfer from the NAND Flash array to the data register (^{t}R), monitor the R/B# signal; or alternatively, issue a READ STATUS (70h) command. If the READ STATUS command is used to monitor the data transfer, the user must reissue the READ (00h) command to receive data output from the data register. See Figure 65 on page 79 and Figure 66 on page 80 for examples. After the READ command has been reissued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate (see Figure 18).

Figure 18: PAGE READ Operation



RANDOM DATA READ 05h-E0h

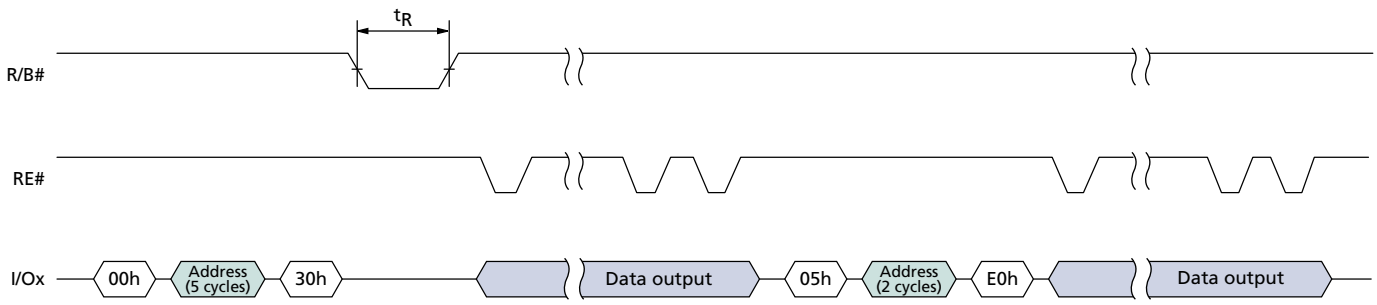
The RANDOM DATA READ command enables the user to specify a new column address so the data at single or multiple addresses can be read. The random read mode is enabled after a normal PAGE READ (00h-30h) sequence.

Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (2 cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially (see Figure 19).

Figure 19: RANDOM DATA READ Operation



PAGE READ CACHE MODE Operations

Micron NAND Flash devices have a cache register that can be used to increase the READ operation speed. Data can be output from the device's cache register while a page is concurrently moved from the NAND Flash array to the data register.

To begin a PAGE READ CACHE MODE command sequence, issue the PAGE READ (00h-30h) command to read a page from the NAND Flash array to the cache register. R/B# goes LOW during ^{t}R (status register bits 6 and 5 = 00). After ^{t}R (R/B# is HIGH and status register bits 6 and 5 = 11), issue either:

- the PAGE READ CACHE MODE SEQUENTIAL (31h) command to begin copying the next sequential page from the NAND Flash array to the data register, or
- the PAGE READ CACHE MODE RANDOM (00h-31h) command to begin copying the page specified in this command from the NAND Flash array to the data register.

After the PAGE READ CACHE MODE SEQUENTIAL or PAGE READ CACHE MODE RANDOM command has been issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}DCBSYR1 while the device begins to copy the next page into the data register. After ^{t}DCBSYR1, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available. At this point, data can be output from the cache register by toggling RE# beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

After the desired number of bytes are output from the cache register, it is possible to either begin an additional PAGE READ CACHE MODE (31h or 00h-31h) operation or issue the PAGE READ CACHE MODE LAST (3Fh) command.

If an additional PAGE READ CACHE MODE (31h or 00h-31h) operation is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}DCBSYR2 while the data register is copied to the cache register and the device begins to copy the next page into the data register. After ^{t}DCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that

the cache register is available. At this point, data can be output from the cache register by toggling RE# beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

If the PAGE READ CACHE MODE LAST (3Fh) command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}DCBSYR2 while the data register is copied into the cache register. After ^{t}DCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 11, indicating that the cache register is available and that the NAND Flash array is ready for another command. At this point, data can be output from the cache register by toggling RE# beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

During busy times (^{t}DCBSYR1 and ^{t}DCBSYR2), the only valid commands are READ STATUS (70h) and RESET (FFh). Until status register bit 5 = 1, the only valid commands during PAGE READ CACHE MODE operations are READ STATUS (70h), PAGE READ CACHE MODE (31h and 00h-31h), RANDOM DATA READ (05h-E0h), and RESET (FFh).

PAGE READ CACHE MODE SEQUENTIAL 31h

The PAGE READ CACHE MODE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register.

To issue this command, write 31h to the command register.

When this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}DCBSYR1 or ^{t}DCBSYR2. After ^{t}DCBSYR1 or ^{t}DCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available. At this point, data can be output from the cache register by toggling RE# beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

PAGE READ CACHE MODE RANDOM 00h-31h

The PAGE READ CACHE MODE RANDOM (00h-31h) command reads the specified page into the data register while the previous page is output from the cache register.

To issue this command, write 00h to the command register. Then write 5 address cycles to the address register. Conclude the sequence by writing 31h to the command register. The column address in the address specified is ignored.

When this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}DCBSYR1 or ^{t}DCBSYR2. After ^{t}DCBSYR1 or ^{t}DCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available. At this point, data can be output from the cache register by toggling RE# beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

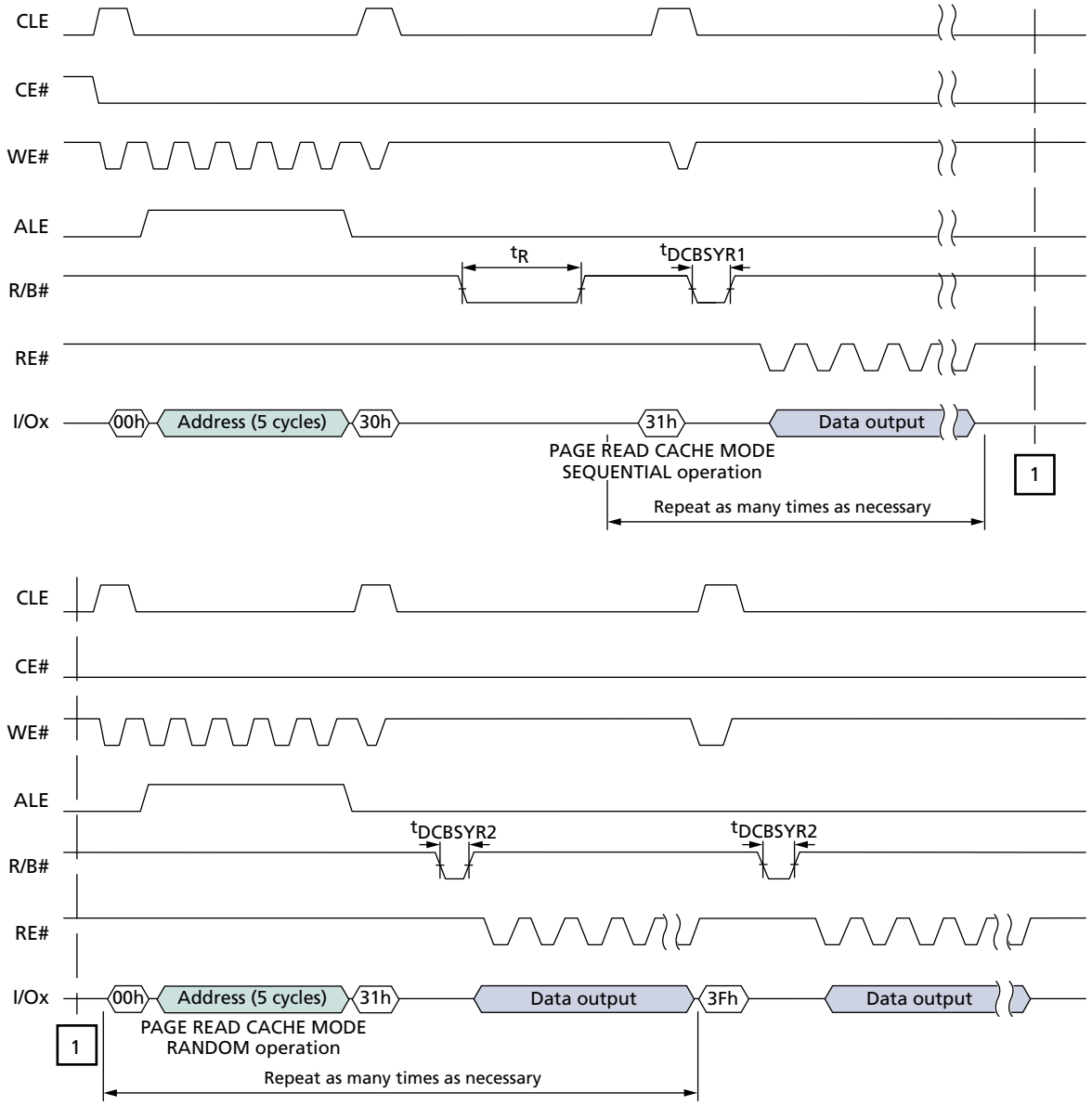
PAGE READ CACHE MODE LAST 3Fh

The PAGE READ CACHE MODE LAST (3Fh) command copies a page from the data register to the cache register without beginning a new cache read.

To issue this command, write 3Fh to the command register.

When this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}DCBSYR2. After ^{t}DCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 11, indicating that the cache register is available and that the NAND Flash array is ready for another command. At this point, data can be output from the cache register by toggling RE# beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

Figure 20: PAGE READ CACHE MODE Operations

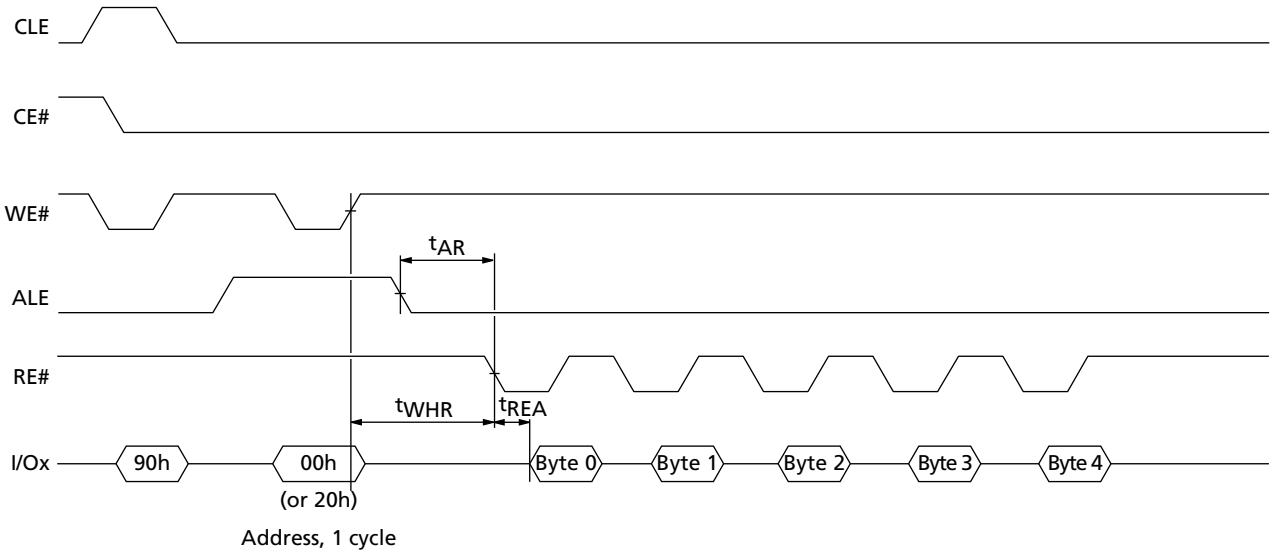


READ ID 90h

The READ ID command is used to read the 5 bytes of identifier code programmed into the NAND Flash devices. The READ ID command reads a 5-byte table that includes manufacturer ID, device configuration, and part-specific information (see Table 9 on page 30).

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until the next command cycle is issued (see Figure 21**).**

Figure 21: READ ID Operation



Note: See Table 9 on page 30 for byte definitions.

Table 9: Device ID and Configuration Codes for Address 00h

Address = 00h	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]
Byte 0	Manufacturer ID									
	Micron	0	0	1	0	1	1	0	0	2Ch
Byte 1	Device ID									
MT29FG08AAD	2Gb, x8, 3V	1	1	0	1	1	0	1	0	DAh
MT29F2G16AAD	2Gb, x16, 3V	1	1	0	0	1	0	1	0	CAh
MT29F2G08ABD	2Gb, x8, 1.8V	1	0	1	0	1	0	1	0	AAh
MT29F2G16ABD	2Gb, x16, 1.8V	1	0	1	1	1	0	1	0	BAh
Byte 2										
Number of die per CE	1							0	0	00b
Cell type	SLC					0	0			00b
Number of simultaneously programmed pages	1			0	0					01b
Interleaved operations between multiple die	Not supported		0							0b
Cache programming	Supported	1								1b
Byte value	MT29F2Gxxxxx	1	0	0	0	0	0	0	0	80h
Byte 3										
Page size	2KB							0	1	01b
Spare area size (bytes)	64B						1			1b
Block size (w/o spare)	128KB			0	1					01b
Organization	x8		0							0b
	x16		1							1b
Serial access (MIN)	25ns	1				0				1xxxb
Serial access (MIN)	35ns	0				0				0xxx0b
Byte value	MT29F2G08AAD	1	0	0	1	0	1	0	1	95h
	MT29F2G16AAD	1	1	0	1	0	1	0	1	D5h
Byte value	MT29F2G08ABD	0	0	0	1	0	1	0	1	15h
	MT29F2G16ABD	0	1	0	1	0	1	0	1	55h
Byte 4										
Reserved								0	0	00b
Planes per CE#	1					0	0			00b
Plane size	2Gb		1	0	1					101b
Reserved		0								0b
Byte value	MT29F2Gxx	0	1	0	1	0	0	0	0	50h

Notes: 1. b = binary; h = hex.

Table 10: Device ID and Configuration Codes for Address 20h

Address = 20h	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
Byte 0	“O”	0	1	0	0	1	1	1	1	4Fh	
Byte 1	“N”	0	1	0	0	1	1	1	0	4Eh	
Byte 2	“F”	0	1	0	0	0	1	1	0	46h	
Byte 3	“I”	0	1	0	0	1	0	0	1	49h	
Byte 4	Undefined	X	X	X	X	X	X	X	X	XXh	

READ UNIQUE ID EDh

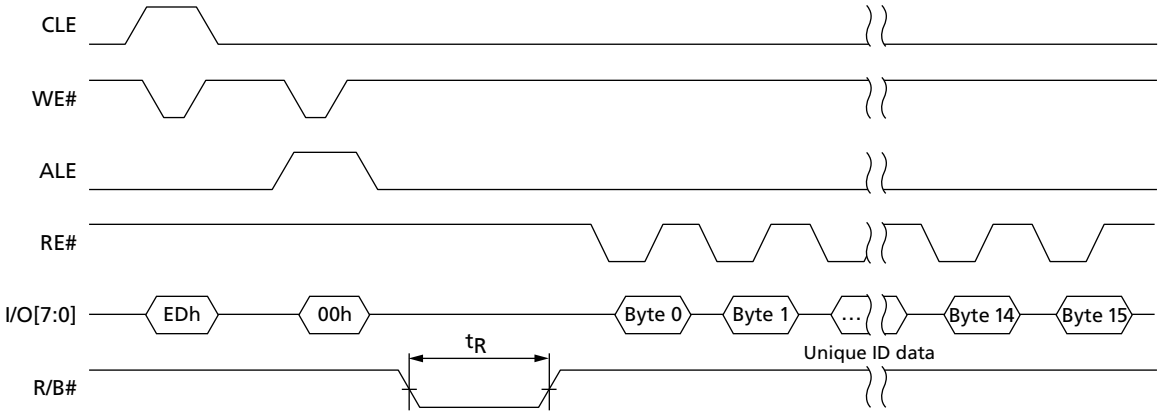
Micron offers the READ UNIQUE ID command to provide a method for uniquely identifying a NAND Flash device.

The READ UNIQUE ID operation uses standard command and address timing. The format of the ID is arbitrary; however, this ID is guaranteed to be unique for every NAND Flash device manufactured.

Many controllers use proprietary error correction code (ECC) schemes; thus, it is not possible for Micron to protect unique ID data with factory-programmed ECC. However, to ensure data integrity, Micron programs the noted NAND Flash devices with a 16-byte unique ID, beginning at byte 0 of the page, then follows with 16 bytes of complement ID. These 32 bytes of data are then repeated a total of 16 times, such that the last byte of the last copy of complement unique ID resides at byte 511 in the page. The user can simply XOR the first copy of the unique ID and its complement. If the result is "1," the unique ID is good. In the unlikely event that the result is non-zero, the user can repeat the XOR operation on a subsequent copy of the unique ID data. Figure 22 shows timing for the device.

The upper eight I/Os on an x16 device are not used and are a "Don't Care" for x16 devices.

Figure 22: READ UNIQUE ID Operation



READ PARAMETER PAGE ECh

The READ PARAMETER PAGE function retrieves the data structure that describes the device's organization, features, timings, and other behavioral parameters. The data structure is repeated at least three times. Figure 23 defines the READ PARAMETER PAGE behavior.

The RANDOM DATA READ (05h-E0h) command is permitted during data output.

The upper eight I/Os on an x16 device are not used and are a "Don't Care" for x16 devices.

Figure 23: READ PARAMETER PAGE ECh

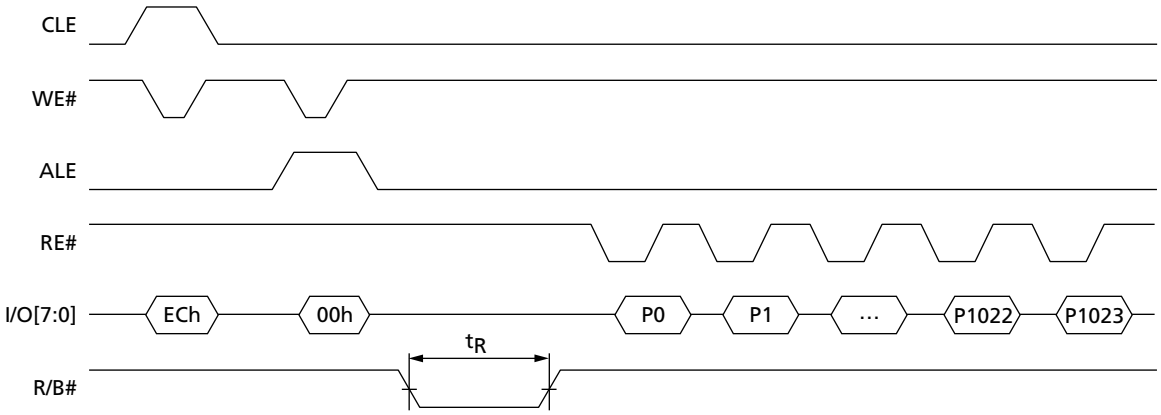


Table 11: ONFI Parameters

Byte	Description		Value
0–3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4–5	Revision number		02h, 00h
6-7	Features supported	MT29F2G08AAD	10h, 00h
		MT29F2G16AAD	11h, 00h
		MT29F2G08ABD	10h, 00h
		MT29F2G16ABD	11h, 00h
8-9	Optional commands supported		3Fh, 00h
10–31	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32–43	Device manufacturer		4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model	MT29F2G08AAD	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 30h, 38h, 41h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F2G16AAD	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 31h, 36h, 41h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F2G08ABD	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 30h, 38h, 41h, 42h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F2G16ABD	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 31h, 36h, 41h, 42h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		2Ch
65–66	Date code		00h,00h
67–79	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80–83	Number of data bytes per page		00h, 08h, 00h, 00h

Table 11: ONFI Parameters (Continued)

Byte	Description		Value
84–85	Number of spare bytes per page		40h, 00h
86–89	Number of data bytes per partial page		00h, 02h, 00h, 00h
90–91	Number of spare bytes per partial page		10h, 00h
92–95	Number of pages per block		40h, 00h, 00h, 00h
96-99	Number of blocks per unit		00h, 08h, 00h, 00h
100	Number of logical units		01h
101	Number of address cycles		23h
102	Number of bits per cell		01h
103–104	Bad blocks maximum per unit		28h, 00h
105–106	Block endurance		01h, 05h
107	Guaranteed valid blocks at beginning of target		01h
108–109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of programs per page		04h
111	Partial programming attributes		00h
112	Number of ECC bits		01h
113	Number of interleaved address bits		00h
114	Interleaved operation attributes		00h
115–127	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O pin capacitance		0Ah
129–130	Timing mode support	MT29F2G08AAD	1Fh, 00h
		MT29F2G16AAD	1Fh, 00h
		MT29F2G08ABD	07h, 00h
		MT29F2G16ABD	07h, 00h
131–132	Program cache timing	MT29F2G08AAD	1Fh, 00h
		MT29F2G16AAD	1Fh, 00h
		MT29F2G08ABD	07h, 00h
		MT29F2G16ABD	07h, 00h
133–134	^{t}PROG maximum page program time	MT29F2G08AAD	F4h, 01h
		MT29F2G16AAD	F4h, 01h
		MT29F2G08ABD	BCh, 02h
		MT29F2G16ABD	BCh, 02h
135–136	^{t}BERS maximum block erase time		B8h, 0Bh
137–138	^{t}R maximum page read time		19h, 00h
139–140	^{t}CCS minimum	MT29F2G08AAD	46h, 00h
		MT29F2G16AAD	46h, 00h
		MT29F2G08ABD	64h, 00h
		MT29F2G16ABD	64h, 00h
141–163	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164–165	Vendor-specific revision number		01h, 00h

Table 11: ONFI Parameters (Continued)

Byte	Description	Value
166–253	Vendor specific	00h, 00h, 00h, 02h, 04h, 80h, 01h, 81h, 04h, 01h, 02h, 01h, 0Ah, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
254–255	Integrity CRC	Set at TEST.
256–511	Value of bytes 0–255	
512–767	Value of bytes 0–255	
768+	Additional redundant parameter pages	

READ STATUS 70h

These NAND Flash devices have an 8-bit status register the software can read during device operation. On the x16 device, I/O[15:8] are "0" when the status register is being read. Table 12 describes the status register.

After a READ STATUS command, all READ cycles will be from the status register until a new command is issued. Changes in the status register will be seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to start a new READ STATUS cycle to see these changes.

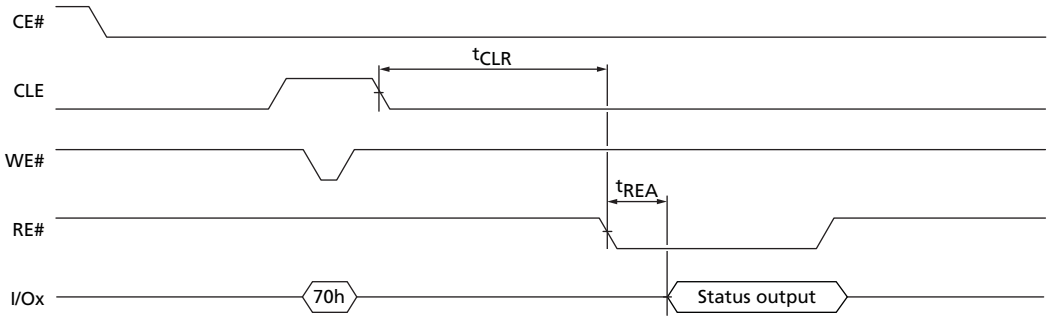
While monitoring the status register to determine when the ^{t}R (transfer from NAND Flash array to data register) is complete, the user must reissue the READ (00h) command to make the change from status to read mode. After the READ command has been reissued, pulsing the RE# line will result in outputting data, starting from the initial column address.

Table 12: Status Register Bit Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Definition
0	Pass/fail	Pass/fail (N)	–	–	Pass/fail	0 = Successful PROGRAM/ERASE 1 = Error in PROGRAM/ERASE
1	–	Pass/fail (N-1)	–	–	–	0 = Successful PROGRAM 1 = Error in PROGRAM
2	–	–	–	–	–	0
3	–	–	–	–	–	0
4	–	–	–	–	–	0
5	Ready/busy	Ready/busy[1]	Ready/busy	Ready/busy[1]	Ready/busy	0 = Busy 1 = Ready
6	Ready/busy	Ready/busy cache[2]	Ready/busy	Ready/busy cache[2]	Ready/busy	0 = Busy 1 = Ready
7	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected

Notes: 1. Status register bit 5 is "0" during the actual programming operation. If cache mode is used, this bit will be "1" when all internal operations are complete.
2. Status register bit 6 is "1" when the cache is ready to accept new data. R/B# follows bit 6. See Figure 27 on page 37 and Figure 73 on page 84.

Figure 24: Status Register Operation



PROGRAM Operations

PROGRAM PAGE 80h-10h

Micron NAND Flash devices are inherently page-programmed devices. Pages must be programmed consecutively within a block, from the least significant page address to most significant page address (i.e., 0, 1, 2, …, 63). Random page address programming is prohibited.

Micron NAND Flash devices also support partial-page programming operations. This means that any single bit can only be programmed one time before an erase is required; however, the page can be partitioned such that a maximum of four programming operations are supported before an erase is required.

SERIAL DATA INPUT 80h

PROGRAM PAGE operations require loading the SERIAL DATA INPUT (80h) command into the command register, followed by 5 ADDRESS cycles, then the data. Serial data is loaded on consecutive WE# cycles starting at the given address. The PROGRAM (10h) command is written after the data input is complete. The control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operation. Write verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW for the duration of array programming time, ^{t}PROG. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the programming operation. Bit 6 of the status register will reflect the state of R/B#. When the device reaches ready, read bit 0 of the status register to determine if the program operation passed or failed (see Figure 25). The command register stays in read status register mode until another valid command is written to it.

RANDOM DATA INPUT 85h

After the initial data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to issuing the PAGE WRITE (10h) command. See Figures 25 for the proper command sequence.

Figure 25: PROGRAM and READ STATUS Operation

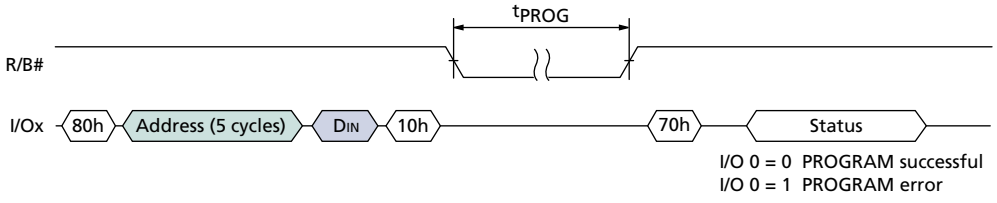
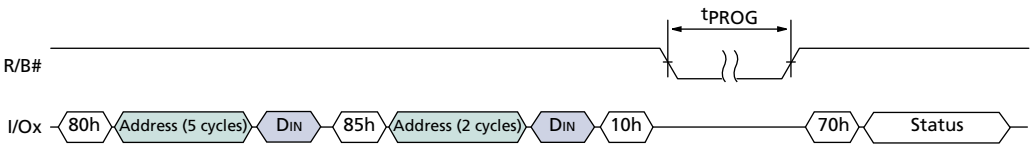


Figure 26: RANDOM DATA INPUT



PROGRAM PAGE CACHE MODE 80h-15h

Cache programming is actually a buffered programming mode of the standard PROGRAM PAGE command. Programming is started by loading the SERIAL DATA INPUT (80h) command to the command register, followed by 5 cycles of address, and a full or partial page of data. The data is initially copied into the cache register, and the CACHE PROGRAM (15h) command is then latched to the command register. Data is transferred from the cache register to the data register on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data register and R/B# returns to HIGH, memory array programming begins.

When R/B# returns to HIGH, new data can be written to the cache register by issuing another CACHE PROGRAM command sequence. The time that R/B# stays LOW will be controlled by the actual programming time. The first time through equals the time it takes to transfer the cache register contents to the data register. On the second and subsequent programming passes, transfer from the cache register to the data register is held off until current data register content has been programmed into the array.

The PROGRAM PAGE CACHE MODE command can cross block address boundaries. RANDOM DATA INPUT (85h) commands are permitted with PROGRAM PAGE CACHE MODE operations.

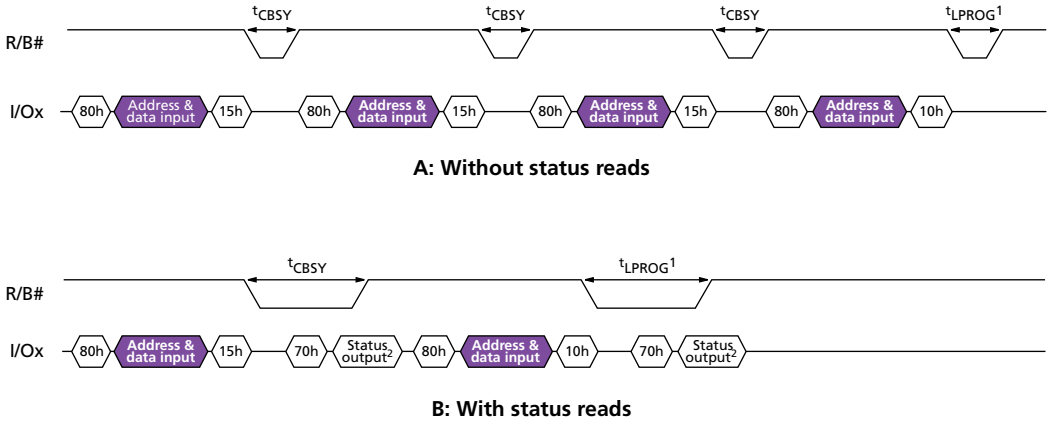
Bit 6 (Cache R/B#) of the status register can be read by issuing the READ STATUS (70h) command to determine when the cache register is ready to accept new data. The R/B# pin always follows bit 6.

Bit 5 (R/B#) of the status register can be polled to determine when the actual programming of the array is complete for the current programming cycle.

If just the R/B# pin is used to determine programming completion, the last page of the program sequence must use the PROGRAM PAGE (10h) command instead of the CACHE PROGRAM (15h) command. If the CACHE PROGRAM (15h) command is used every time, including the last page of the programming sequence, status register bit 5 must be used to determine when programming is complete (see Figure 27 on page 37).

Bit 1 of the status register returns the pass/fail for the previous page when bit 6 of the status register is a “1” (ready state). The pass/fail status of the current PROGRAM operation is returned with bit 0 of the status register when bit 5 of the status register is a “1” (ready state) as shown in Figure 27 on page 37.

Figure 27: PROGRAM PAGE CACHE MODE Example



Notes: 1. See Note 3, Table 32 on page 70.
2. Check I/O[6:5] for internal ready/busy. Check I/O[1:0] for pass/fail status. RE# can stay LOW or pulse multiple times after a 70h command.

Internal Data Move

An internal data move requires two command sequences. Issue a READ for INTERNAL DATA MOVE (00h-35h) command first, then the PROGRAM for INTERNAL DATA MOVE (85h-10h) command.

READ FOR INTERNAL DATA MOVE 00h-35h

The READ for INTERNAL DATA MOVE (00h-35h) command is used in conjunction with the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. First, 00h is written to the command register, then the internal source address is written (5 cycles). After the address is input, the READ for INTERNAL DATA MOVE (35h) command writes to the command register. This transfers a page from memory into the cache register.

All 5 ADDRESS cycles are required when a READ for INTERNAL DATA MOVE command is issued.

After a READ for INTERNAL DATA MOVE (00h-35h) command is issued and R/B# returns HIGH, signifying operation completion, the data transferred from the source page into the cache register may be read out by toggling RE#. Data is output sequentially from the column address originally specified with the READ FOR INTERNAL DATA MOVE (00h-35h) command. RANDOM DATA READ (05h-E0h) commands can be issued without limit after the READ FOR INTERNAL DATA MOVE command.

The memory device is now ready to accept the PROGRAM for INTERNAL DATA MOVE command. Please refer to the description of this command in the following section.

PROGRAM for INTERNAL DATA MOVE 85h-10h

After the READ for INTERNAL DATA MOVE (00h-35h) command has been issued and R/B# goes HIGH, the PROGRAM for INTERNAL DATA MOVE (85h-10h) command can be written to the command register. This command transfers the data from the cache register to the data register and programming of the new destination page begins. The sequence: 85h, destination address (5 cycles), then 10h, is written to the device. After 10h is written, R/B# goes LOW while the control logic automatically programs the new page. The READ STATUS command can be used instead of the R/B# line to determine when the write is complete. When status register bit 6 = 1, bit 0 of the status register indicates if the operation was successful.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for INTERNAL DATA MOVE command sequence to modify one or more bytes of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

When 10h is written to the command register, the original data plus the modified data are transferred to the data register, and programming of the new page is started. The RANDOM DATA INPUT command can be issued as many times as necessary before starting the programming sequence with 10h (see Figures 28 and 29 on page 39).

Because INTERNAL DATA MOVE operations do not use external memory, ECC cannot be used to check for errors before programming the data to a new page. This can lead to a data error if the source page contains a bit error due to charge loss or charge gain. In the case that multiple INTERNAL DATA MOVE operations are performed, these bit errors may accumulate without correction. For this reason, it is highly recommended that systems using INTERNAL DATA MOVE operations also use a robust ECC scheme that can correct 2 or more bits per sector.

Figure 28: INTERNAL DATA MOVE

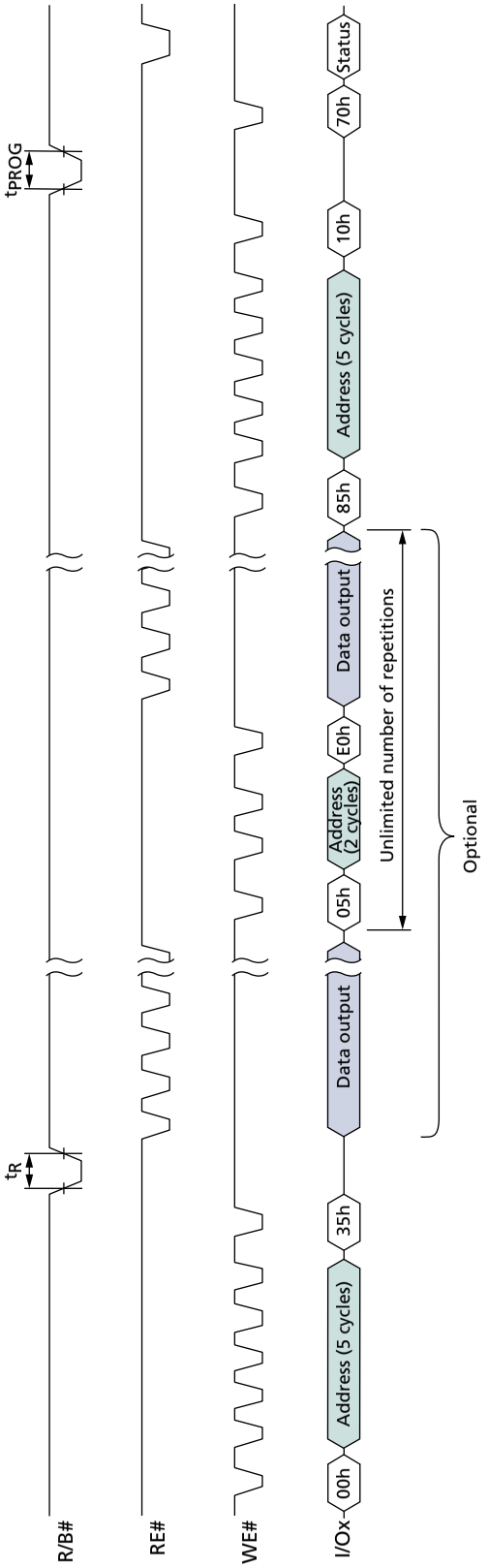
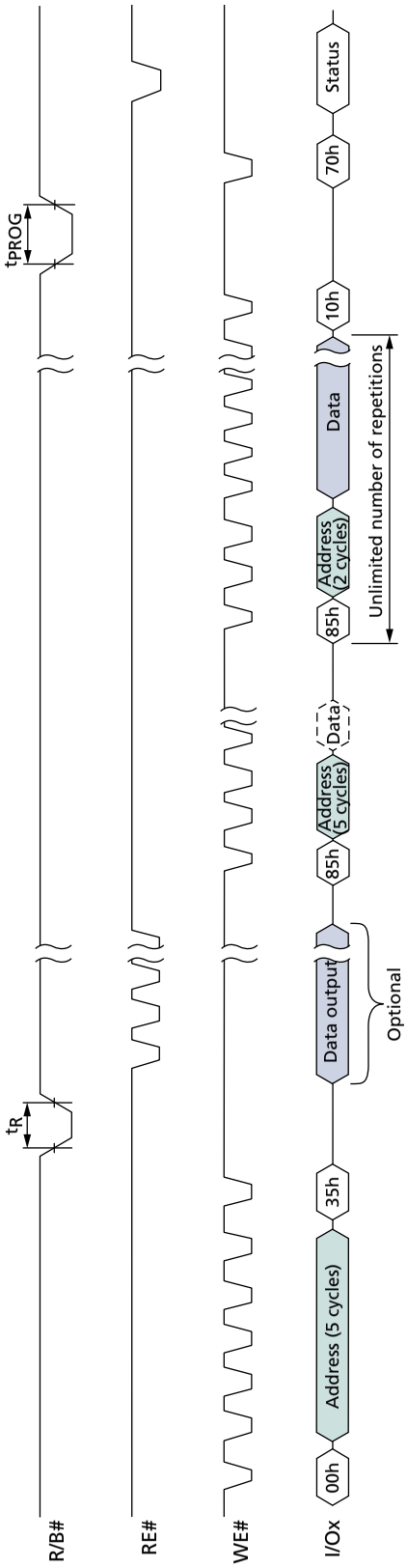


Figure 29: INTERNAL DATA MOVE with Optional RANDOM DATA Output and RANDOM DATA Input



BLOCK ERASE Operation

BLOCK ERASE 60h-D0h

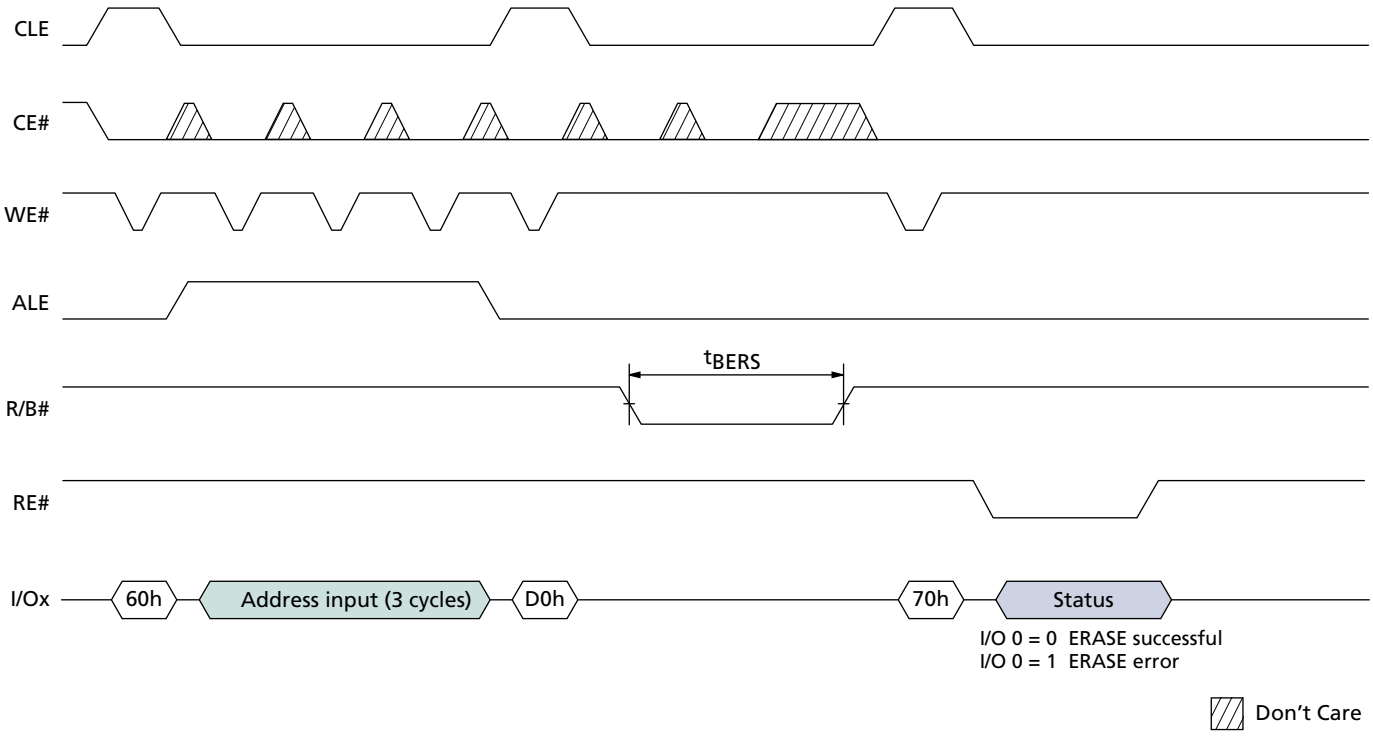
Erasing occurs at the block level. For example, the MT29F2G08ABD device has 2,048 erase blocks, organized into 64 pages per block, 2,112 bytes per page (2,048 + 64 bytes). Each block is 132K bytes (128K + 4K bytes). The BLOCK ERASE command operates on one block at a time (see Figure 30).

Three cycles of addresses BA[18:6] and PA[5:0] are required. Although page addresses PA[5:0] are loaded, they are a "Don't Care" and are ignored for BLOCK ERASE operations. See Table 4 on page 16 for addressing details.

The actual command sequence is a two-step process. The ERASE SETUP (60h) command is first written to the command register. Then 3 cycles of addresses are written to the device. Next, the ERASE CONFIRM (D0h) command is written to the command register. At the rising edge of WE#, R/B# goes LOW and the control logic automatically controls the timing and erase-verify operations. R/B# stays LOW for the entire ^{t}BERS erase time.

The READ STATUS (70h) command can be used to check the status of the BLOCK ERASE operation. When bit 6 = 1, the ERASE operation is complete. Bit 0 indicates a pass/fail condition where 0 = pass (see Figure 30, and Table 12 on page 34).

Figure 30: BLOCK ERASE Operation



Notes: 1. I/O[15:8] is applicable only for x16 devices.
2. Invert area bit is applicable for 24h command; it may be LOW or HIGH for 23h command.

Block Lock Feature

The block lock feature of this NAND Flash device provides the ability to protect the entire device or ranges of blocks from PROGRAM and ERASE operations. Using this block lock feature offers increased functionality and flexibility over using just the WP# pin to prevent PROGRAM and ERASE operations.

Block lock features are enabled and disabled at power-on through the use of the LOCK pin. At power-on, if LOCK is LOW, all block lock commands are disabled. However, at power-on, if LOCK is HIGH, the block lock commands are enabled and, by default, all of the blocks on the device are protected, or locked, from PROGRAM and ERASE operations, even if WP# is HIGH.

Before the contents of the device can be modified, the device must first be unlocked. Either a range of blocks or the entire device may be unlocked. PROGRAM and ERASE operations complete successfully only in the block ranges that have been unlocked. Blocks, once unlocked, can be locked again to protect them from further PROGRAM and ERASE operations.

Blocks that are locked can be protected further, or locked tight. When locked tight, the device's blocks can no longer be locked or unlocked until the device is power cycled.

WP# and Block Lock

- Holding WP# LOW locks all blocks provided the blocks are not locked tight.
- If WP# is held LOW to lock blocks, then returned to HIGH, a new UNLOCK command must be issued to unlock blocks.

UNLOCK 23h-24h

By default at power-on if LOCK is HIGH, all of the blocks in the NAND Flash device are locked, meaning that they are protected from PROGRAM and ERASE operations. The UNLOCK (23h) command is used to unlock a range of blocks. Unlocked blocks have no protection and can be programmed or erased.

The UNLOCK command uses two registers, a lower boundary block address register and an upper boundary block address register, and the invert area bit to determine what range of blocks are unlocked. When the invert area bit = 0, the range of blocks within the lower and upper boundary address registers are unlocked. When the invert area bit = 1, the range of blocks outside the boundaries of the lower and upper boundary address registers are unlocked. The lower boundary block address must be less than the upper boundary block address. Figures 31 and 32 on page 42 show examples of how the lower and upper boundary address registers work with the invert area bit.

To unlock a range of blocks, issue the UNLOCK (23h) command followed by the appropriate ADDRESS cycles that indicate the lower boundary block address. Then issue the 24h command followed by the appropriate ADDRESS cycles that indicate the upper boundary block address. The least significant page address bit, PA0, should be set to "1" if setting the invert area bit; otherwise, it should be "0." The other page address bits should be "0" (see Figure 33 on page 43).

Only one range of blocks can be specified in the lower and upper boundary block address registers. If after unlocking a range of blocks the UNLOCK command is again issued, the new block address range determines which blocks are unlocked. The previous unlocked block address range is not retained.

Figure 31: Flash Array Protected: Inverted Area Bit = 0

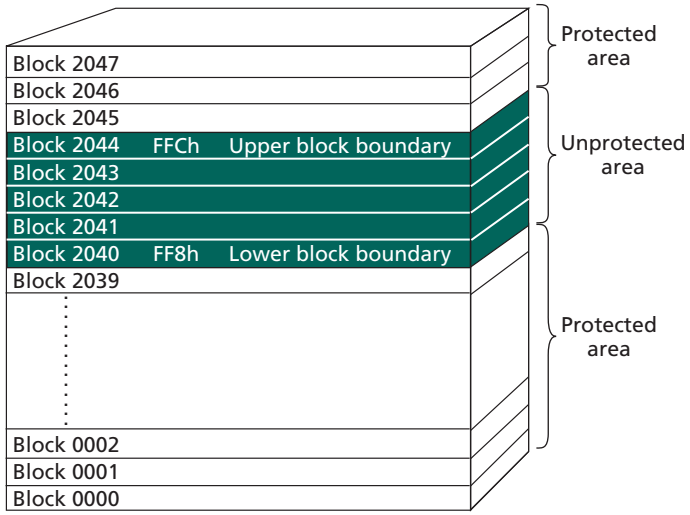


Figure 32: Flash Array Protected: Invert Area Bit = 1

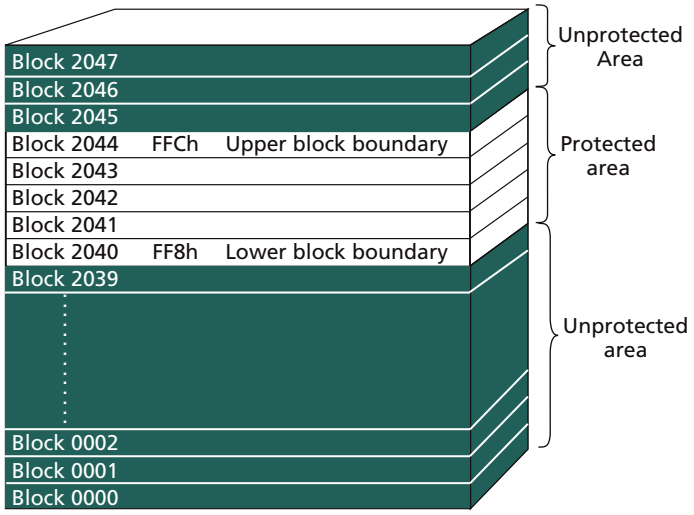
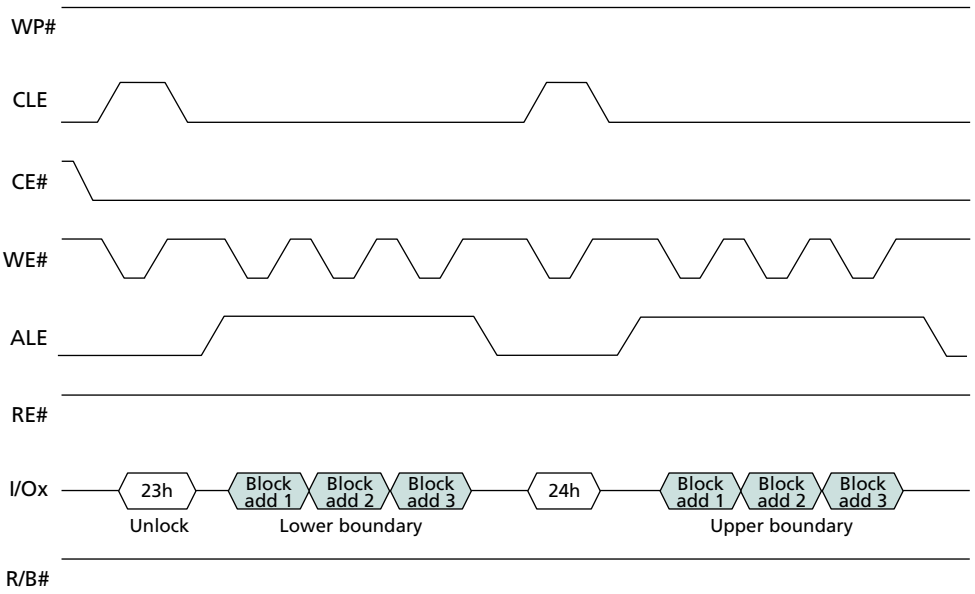


Table 13: Block Lock Address Cycle Assignments

ALE Cycle	I/O[15:8][1]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	BA7	BA6	LOW	LOW	LOW	LOW	LOW	Invert area bit[2]
Second	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Third	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes: 1. I/O[15:8] is applicable only for x16 devices.
2. Invert area bit is applicable for 24h command; it may be LOW or HIGH for 23h command.

Figure 33: UNLOCK Operation



LOCK 2Ah

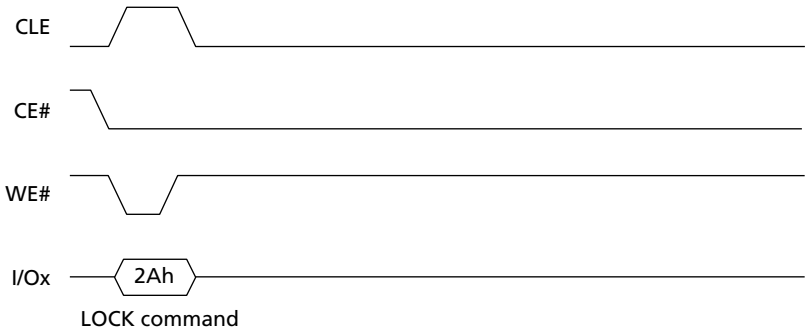
By default at power-on, if LOCK is HIGH, all of the blocks in the NAND Flash device are locked, meaning that they are protected from PROGRAM and ERASE operations. If portions of the device are unlocked using the UNLOCK (23h) command, they can be locked again using the LOCK (2Ah) command. The LOCK command locks all of the blocks in the device. Locked blocks are write-protected from PROGRAM and ERASE operations.

To lock all of the blocks in the device, issue the LOCK (2Ah) command.

When a PROGRAM or ERASE operation is issued to a locked block, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. Any READ STATUS command reports bit 7 as "0," indicating that the block is protected.

The LOCK (2Ah) command is disabled if LOCK is LOW at power-on or if the device is locked tight (see "LOCK-TIGHT 2Ch" on page 44).

Figure 34: LOCK Operation



LOCK-TIGHT 2Ch

The LOCK-TIGHT (2Ch) command prevents locked blocks from being unlocked and also prevents unlocked blocks from being locked. When this command is issued, the UNLOCK (23h) and LOCK (2Ah) commands are disabled. This provides an additional level of protection against inadvertent PROGRAM and ERASE operations to locked blocks.

To implement lock-tight in all of the locked blocks in the device, verify that WP# is HIGH and then issue the LOCK-TIGHT (2Ch) command.

When a PROGRAM or ERASE operation is issued to a locked block that has also been locked tight, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. The READ STATUS (70h) command reports bit 7 as "0," indicating that the block is protected. PROGRAM and ERASE operations complete successfully to blocks that were not locked at the time the LOCK-TIGHT command was issued.

After the LOCK-TIGHT command is issued, the command cannot be disabled via a software command. The only ways to disable the lock-tight status is to power cycle the device. When the lock-tight status is disabled, all of the blocks become locked, the same as if the LOCK (2Ah) command had been issued.

The LOCK-TIGHT (2Ch) command is disabled if LOCK is LOW at power-on.

Figure 35: LOCK-TIGHT Operation

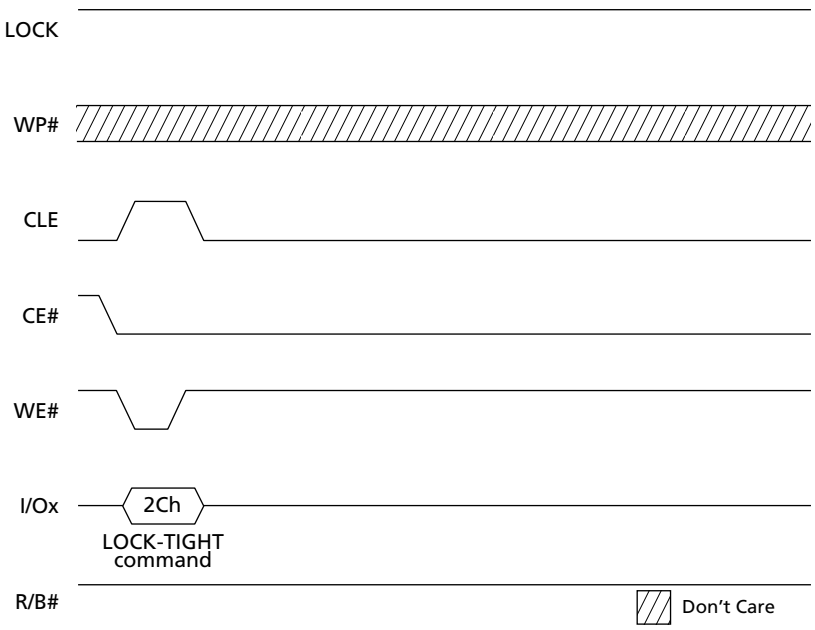
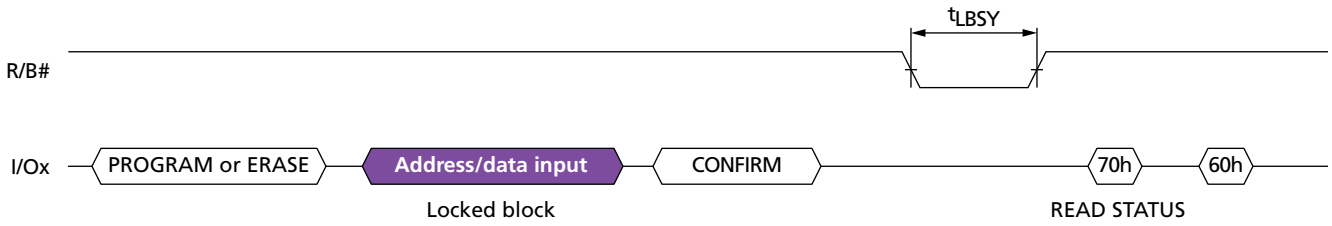


Figure 36: PROGRAM/ERASE Issued to Locked Block



BLOCK LOCK READ STATUS 7Ah

The BLOCK LOCK READ STATUS (7Ah) command is used to determine the protection status of individual blocks. The ADDRESS cycles have the same format as shown in Table 14; the invert area bit should be set LOW. On the falling edge of RE# the I/O pins output the block lock status register which contains the information on the protection status of the block. Table 14 shows how to interpret the block lock status register bits.

Table 14: Block Lock Status Register Bit Definitions

Block Lock Status Register Definitions	I/O[7:3]	I/O2 (Lock#)	I/O1 (LT#)	I/O0 (LT)
Block is locked-tight	X	0	0	1
Block is locked	X	0	1	0
Block is unlocked, and device is locked-tight	X	1	0	1
Block is unlocked, and device is not locked-tight	X	1	1	0

Figure 37: BLOCK LOCK READ STATUS

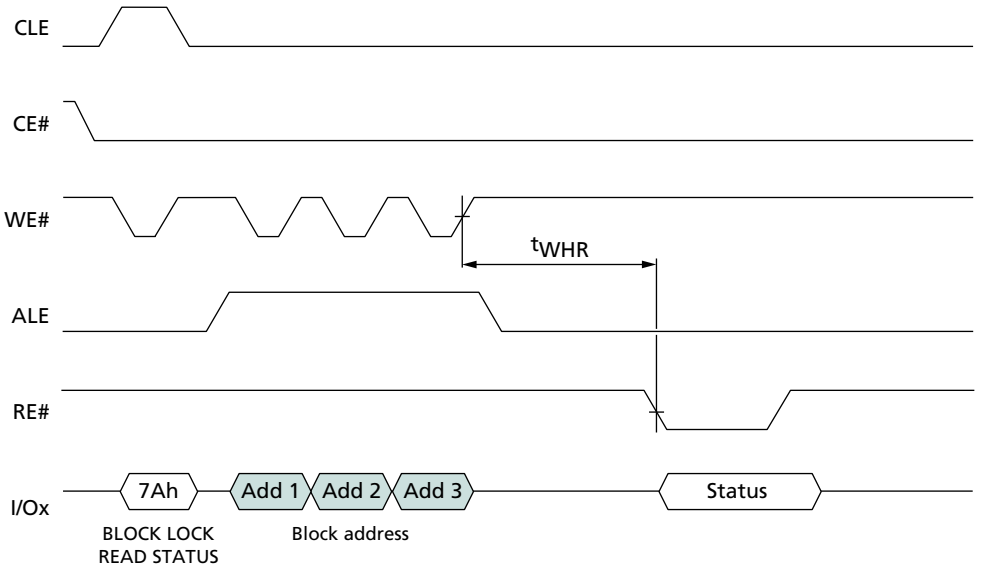
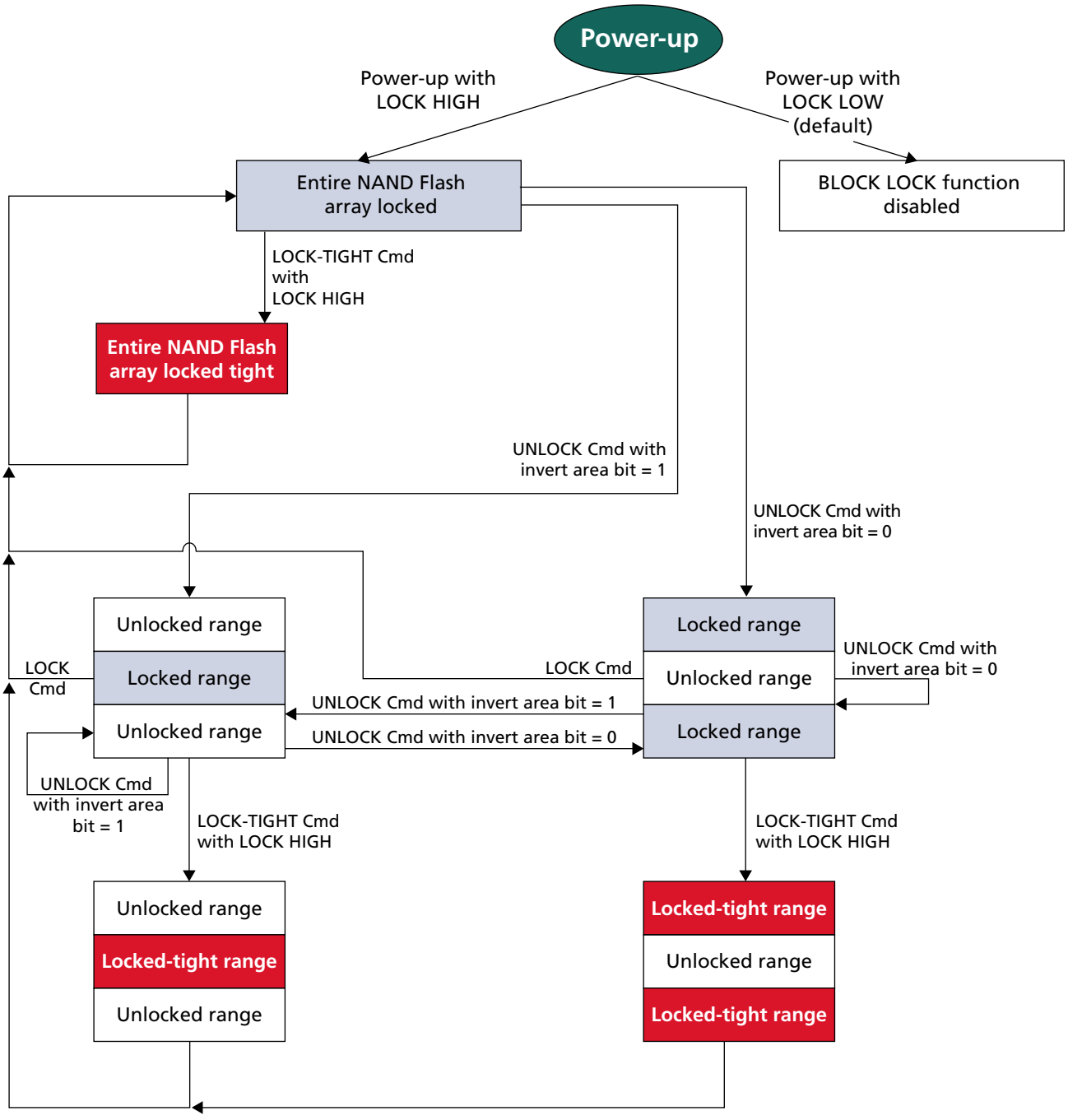


Figure 38: BLOCK LOCK Flow Chart



One-Time Programmable (OTP) Area

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (2,112 bytes per page) of OTP data is available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

In Micron NAND Flash devices, the OTP area leaves the factory in a non-written state (all bits are "1s"). Programming or partial-page programming enables the user to program only "0" bits in the OTP area. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area simply prevents further programming of the OTP area.

While the OTP area is referred to as "one-time programmable," Micron provides a unique way to program and verify data—before permanently protecting it and preventing future changes.

OTP programming and protection are accomplished in two discrete operations. First, using the OTP DATA PROGRAM (A0h-10h) command, an OTP page is programmed entirely in one operation, or in up to four partial-page programming sequences. Programming can occur on other pages within the OTP area in a similar manner. Second, the OTP area is permanently protected from further programming using the OTP DATA PROTECT (A5h-10h) command. The pages within the OTP area can always be read using the OTP DATA READ (AFh-30h) command, whether or not it is protected.

To determine whether or not the device is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command.

OTP DATA PROGRAM A0h-10h

The OTP DATA PROGRAM (A0h-10h) command is used to write data to the pages within the OTP area. An entire page can be programmed at one time, or a page can be partially programmed up to four times. There is no ERASE operation for the OTP pages.

The OTP DATA PROGRAM command allows programming into an offset of an OTP page, using the 2 bytes of column address (CA[11:0] for x8 devices or CA[10:0] for x16 devices). The OTP DATA PROGRAM command will not execute if the OTP area has been protected.

To use the OTP DATA PROGRAM command, issue the A0h command. Issue 5 ADDRESS cycles: the first 2 ADDRESS cycles are the column address, and for the remaining 3 cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Next, write from 1 to 2,112 bytes of data. After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification. Program verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW during the duration of the array programming time (^{t}PROG). The READ STATUS (70h) command is the only command valid during the OTP DATA PROGRAM operation. Bit 5 of the status register will reflect the state of R/B#. If bit 7 is "0," then the OTP area has been protected; otherwise, it will be a "1."

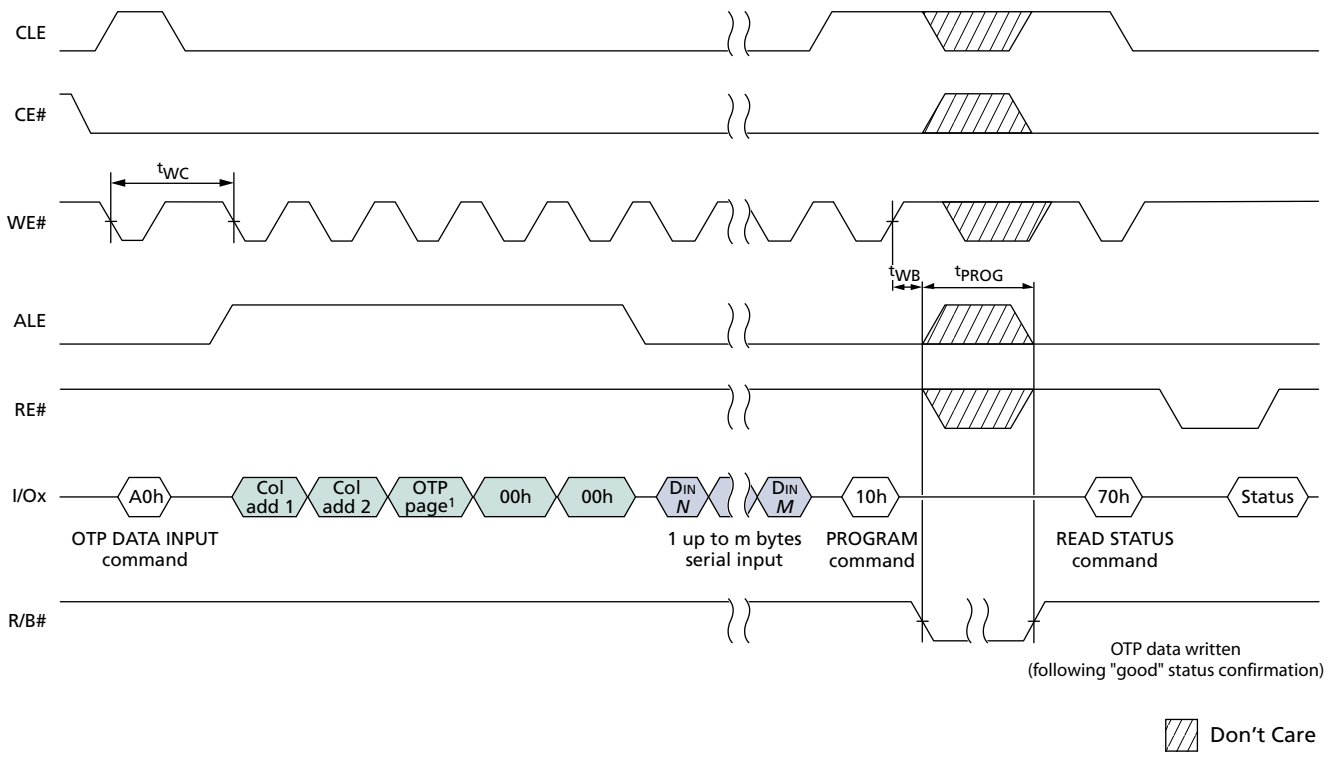
When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 12 on page 34).

It is possible to program each OTP page a maximum of four times.

RANDOM DATA INPUT 85h

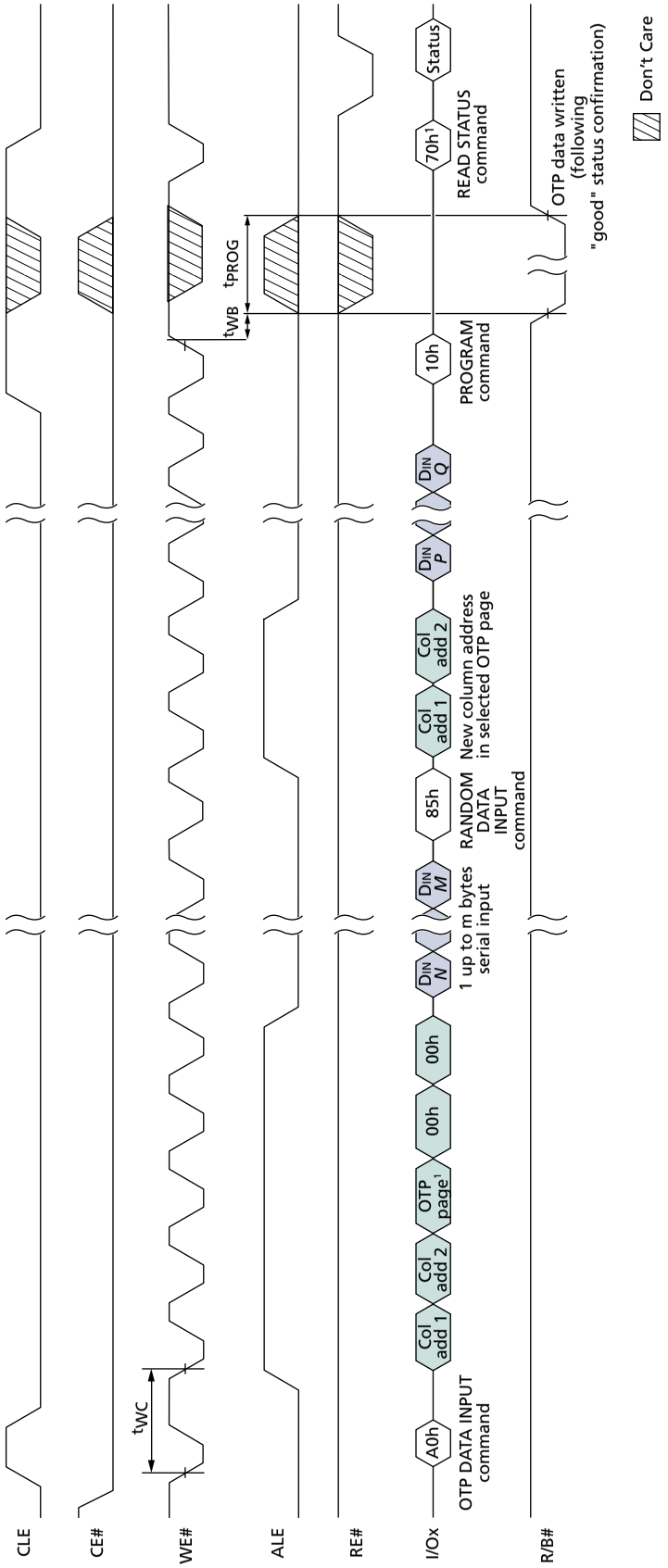
After the initial OTP data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to issuance of the OTP PAGE WRITE (10h) command. See Figure 40 for the proper command sequence.

Figure 39: OTP DATA PROGRAM



Notes: 1. The OTP page must be within the 02h–0Bh range.

Figure 40: OTP PROGRAM with RANDOM DATA INPUT



OTP DATA PROTECT A5h-10h

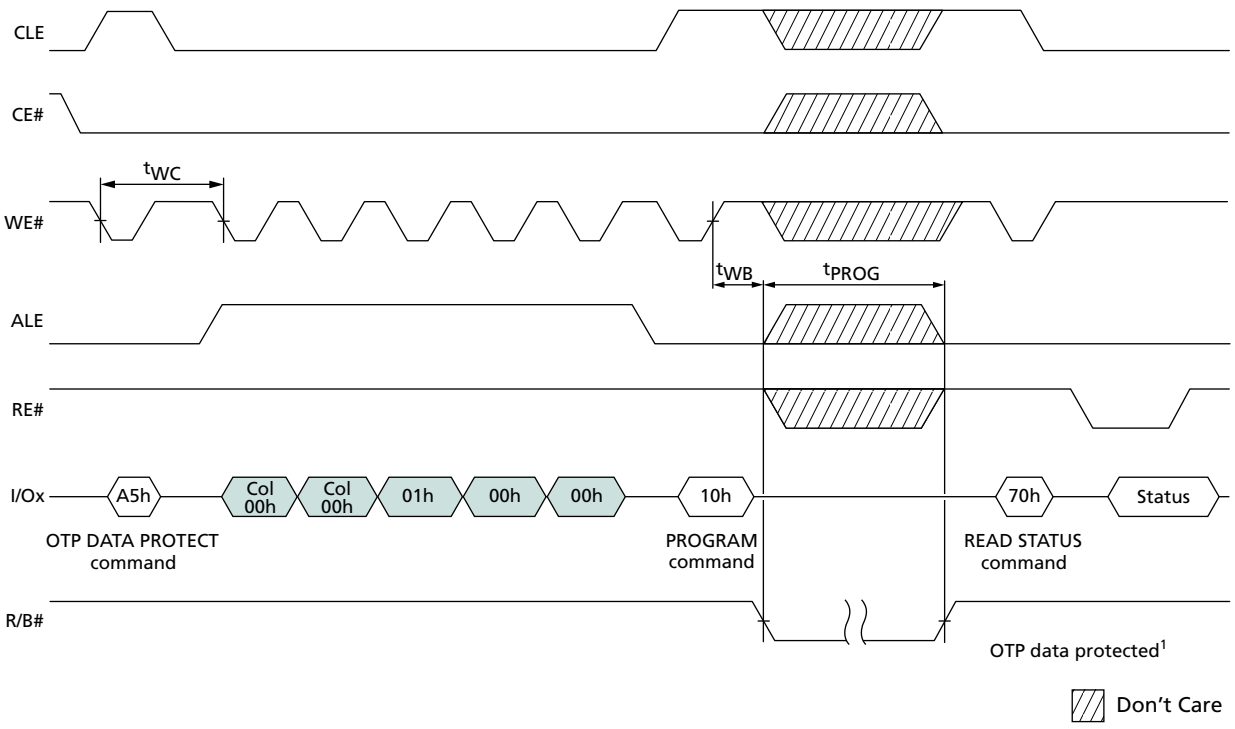
The OTP DATA PROTECT (A5h-10h) command is used to protect all the data in the OTP area. After the data is protected it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

To use the OTP DATA PROTECT command, issue the A5h command. Next, issue the following 5 ADDRESS cycles: 00h-00h-01h-00h-00h. Finally, issue the 10h command.

R/B# goes LOW while the OTP area is being protected. The protect command duration is similar to a normal page programming operation, ^{t}PROG. The READ STATUS (70h) command is the only command valid during the OTP DATA PROTECT operation. Bit 5 of the status register will reflect the state of R/B#.

When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 12 on page 34).

Figure 41: OTP DATA PROTECT



Notes: 1. OTP data is protected following "good" status confirmation.

OTP DATA READ AFh-30h

The OTP DATA READ (AFh-30h) command is used to read data from a page within the OTP area. An OTP page within the OTP area is available for reading data whether or not the area is protected.

To use the OTP DATA READ command, issue the AFh command. Next, issue 5 ADDRESS cycles: the first 2 ADDRESS cycles are the column address, and for the remaining 3 cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Finally, issue the 30h command.

R/B# goes LOW (^{t}R) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the OTP DATA READ operation. Bit 5 of the status register will reflect the state of R/B#. For details, refer to Table 12 on page 34.

Normal READ operation timings apply to OTP read accesses (see Figure 42). Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

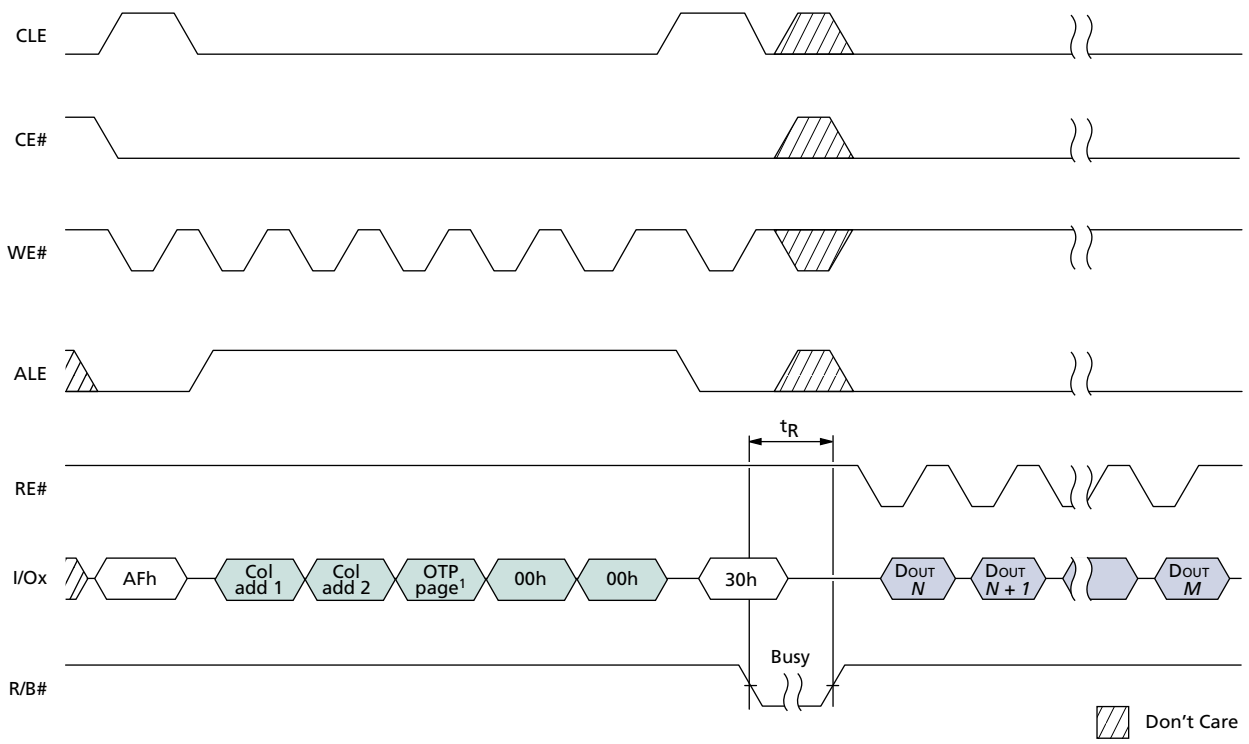
The RANDOM DATA READ command enables the user to specify a new column address within the OTP page so the data at single or multiple column addresses can be read. The random read mode is enabled after a normal OTP DATA READ (AFh-30h) sequence.

Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (2 cycles).

The RANDOM DATA READ command can be issued without limit within the OTP page.

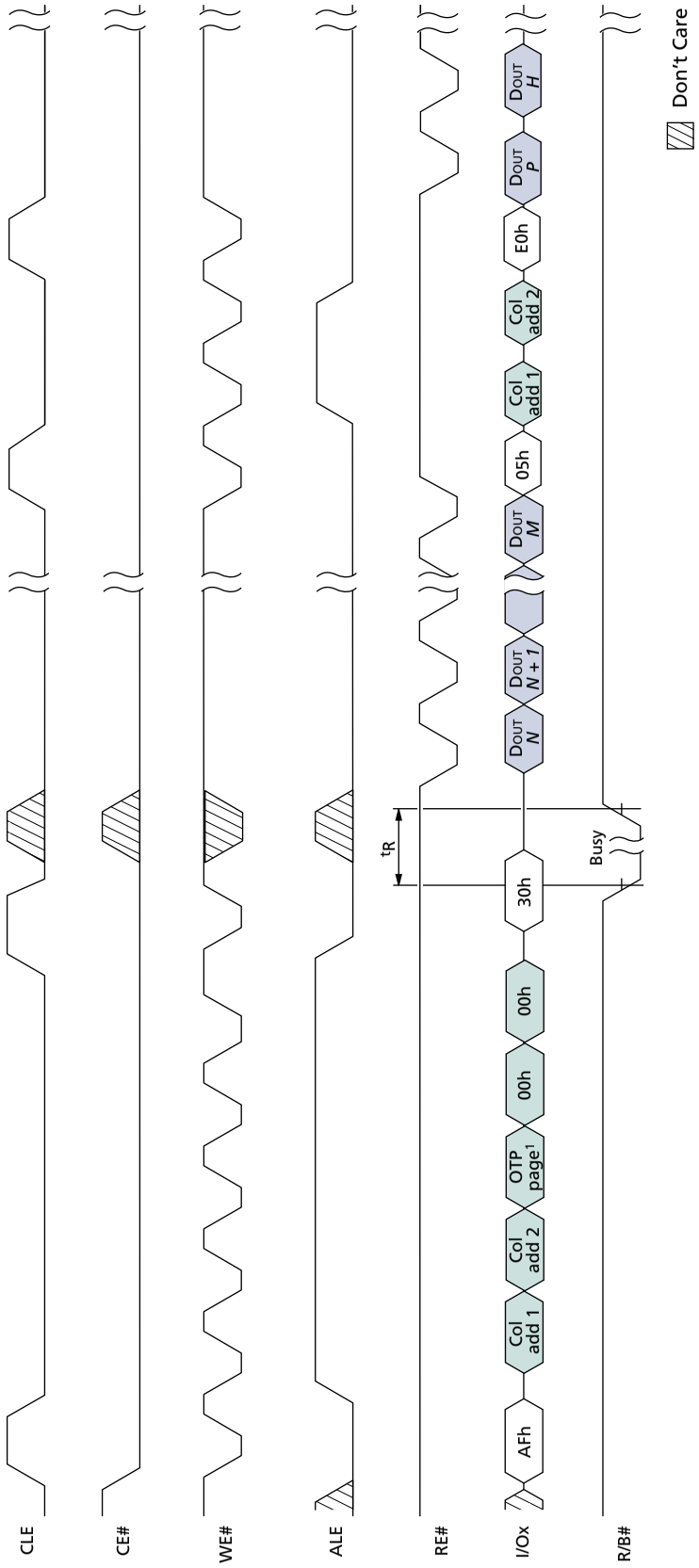
Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially (see Figure 43 on page 53).

Figure 42: OTP DATA READ Operation



Notes: 1. The OTP page must be within the 02h–0Bh range.

Figure 43: OTP DATA READ with RANDOM DATA READ



Notes: 1. The OTP page must be within the range 02h–0Bh.

Features Operations

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to alter the NAND Flash device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Each feature (in the range of 0 to 255) is defined in the features table (Table 15). The GET FEATURES (EEh) command (see "GET FEATURES EEh" on page 56) simply reads the parameter in the features table (4 bytes). The SET FEATURES (EFh) command (see "SET FEATURES EFh" on page 57) places parameters in the features table (4 bytes).

When a feature is set, by default it remains active until the device is power-cycled. It is volatile. Unless otherwise specified in the features table, once a device is set it remains set, even if a RESET (FFh) command is issued.

Table 15: Features

Feature Address	Description
00h	N/A
01h	Timing mode
02h–7Fh	Reserved
80h	Vendor-specific parameter: Programmable I/O drive strength
81h	Vendor-specific parameter: Programmable R/B# pull-down strength
82h-FFh	Reserved

Table 16: Feature Address 01h: Timing Mode

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing mode	Mode 0 (default)	Reserved (0)					0	0	0	00h	1,2
	Mode 1	Reserved (0)					0	0	1	01h	2
	Mode 2	Reserved (0)					0	1	0	01h	3
	Mode 3	Reserved (0)					0	1	1	01h	3
	Mode 4	Reserved (0)					1	0	0	01h	3
	Mode 5	Reserved (0)					1	0	1	01h	4
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Notes:
1. The timing-mode feature address is used to change the default timing mode. The timing mode should be selected to indicate the maximum speed at which the device will receive commands, addresses, and data cycles. The five supported settings for the timing mode are shown. The default timing mode is mode 0. The device returns to mode 0 when the device is power cycled. Supported timing modes are reported in the parameter page.
2. Supported for both 1.8V and 3.3V.
3. Supported for 3.3V only.
4. Not supported.

Table 17: Feature Address 80h: Programmable I/O Drive Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Notes: 1. The PROGRAMMABLE DRIVE STRENGTH feature address is used to change the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive-strength settings. The default drive strength is full strength. The device returns to the default drive strength mode when the device is power cycled. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.

Table 18: Feature Address 81h: Programmable R/B# Pull-down Strength

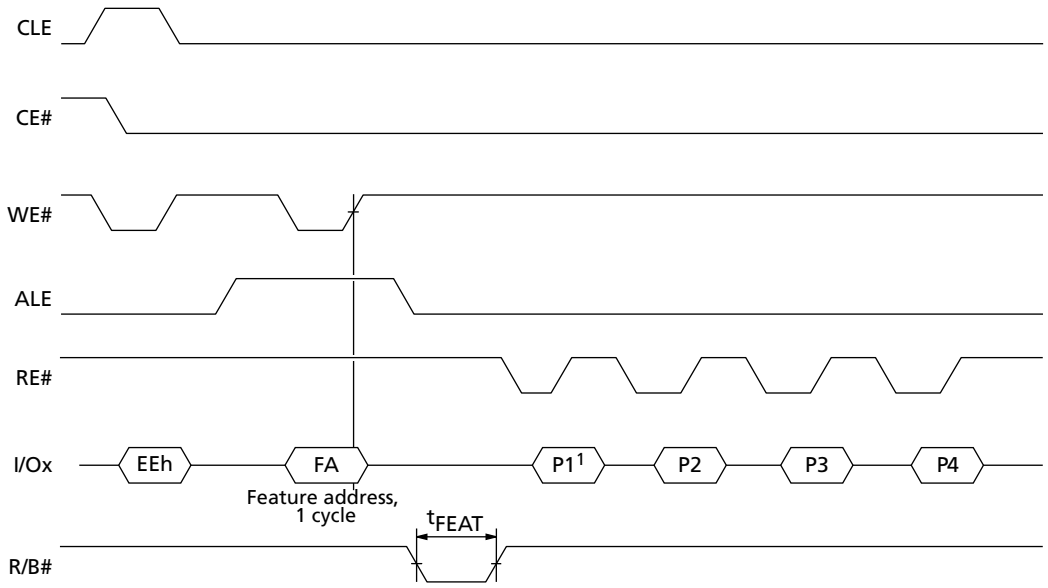
Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
R/B# pull-down strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Notes: 1. The programmable R/B# pull-down strength feature address is used to change the default R/B# pull-down strength. R/B# pull-down strength should be selected based on expected loading of R/B#. The four supported pull-down strength settings are shown. The default pull-down strength is full strength. The device returns to the default pull-down strength when the device is power cycled.

GET FEATURES EEh

The GET FEATURES command is used to determine the current settings for the specified feature address. This command returns the parameter settings, including modifications made previously with the SET FEATURES function. Figure 44 defines GET FEATURES behavior and timing.

Figure 44: GET FEATURES (EEh)

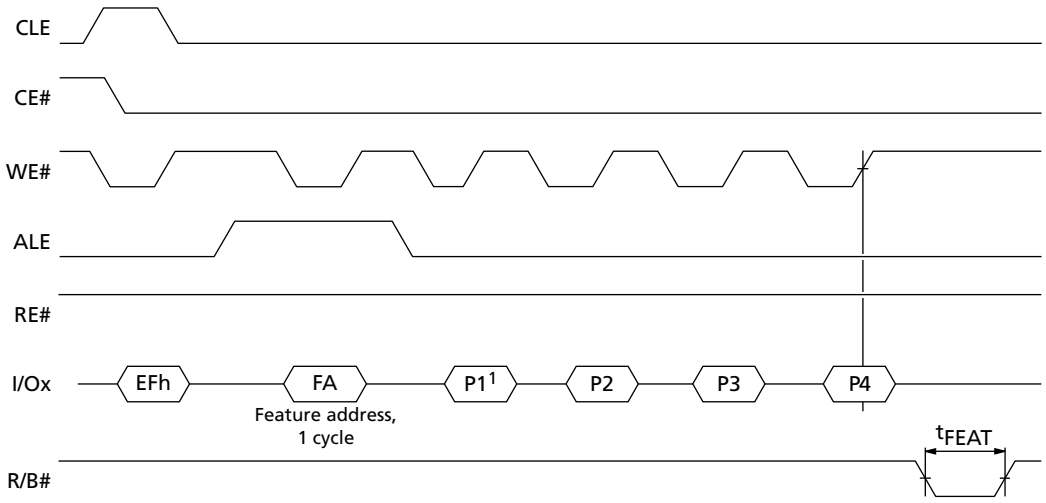


Notes: 1. P1–P4 are the parameters for the specified feature address (FA).

SET FEATURES EFh

The SET FEATURES command is used to set the parameters at a specified feature address. These parameters are stored in the device until power is cycled. They are applied to all die on the CE# to which this command is issued.

Figure 45: SET FEATURES (EFh)



Notes: 1. P1–P4 are the parameters for the specified feature address (FA).

RESET Operation

RESET FFh

The RESET command is used to put the memory device into a known condition and to abort the command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are marked invalid.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes LOW for ^{t}RST after the RESET command is written to the command register (see Figure 46 and Table 19).

The RESET command must be issued to all CE#s as the first command after power-on. The device will be busy for a maximum of 1ms.

Figure 46: RESET Operation

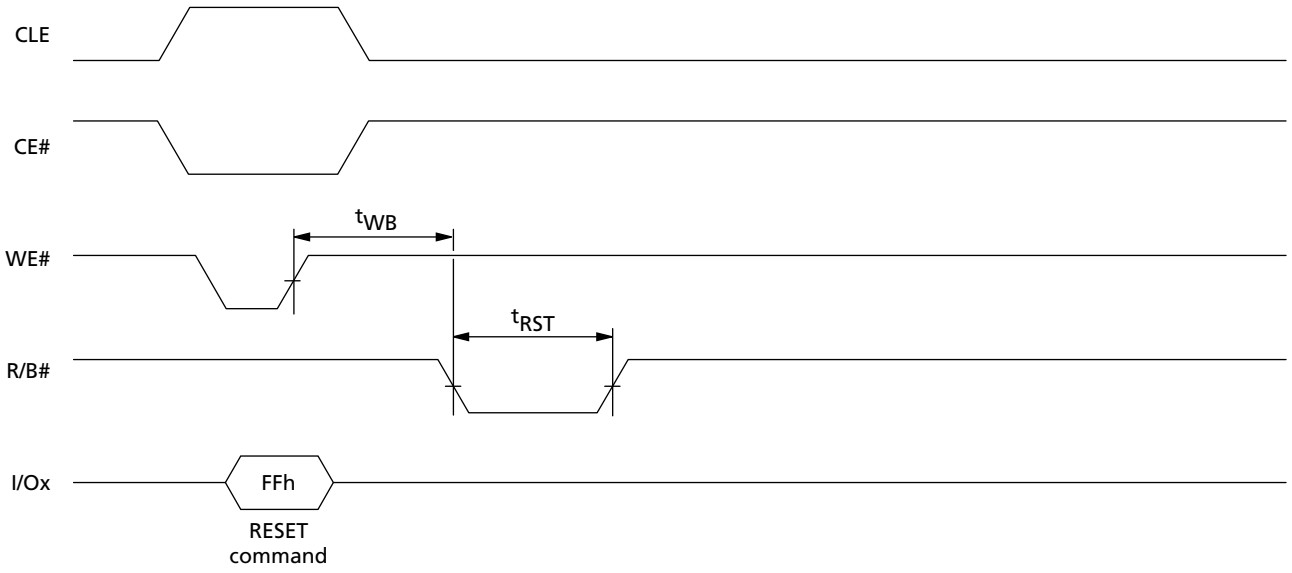


Table 19: Status Register Contents After RESET Operation

Condition	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
WP# HIGH	Ready	1	1	1	0	0	0	0	0	E0h
WP# LOW	Ready and write protected	0	1	1	0	0	0	0	0	60h

WRITE PROTECT Operation

It is possible to enable and disable PROGRAM and ERASE commands using the WP# pin. Figures 47 through 50 illustrate the setup time (^{t}WW) required from WP# toggling until a PROGRAM or ERASE command is latched into the command register. After command cycle 1 is latched, the WP# pin must not be toggled until the command is complete and the device is ready (status register bit 5 is "1").

Figure 47: ERASE Enable

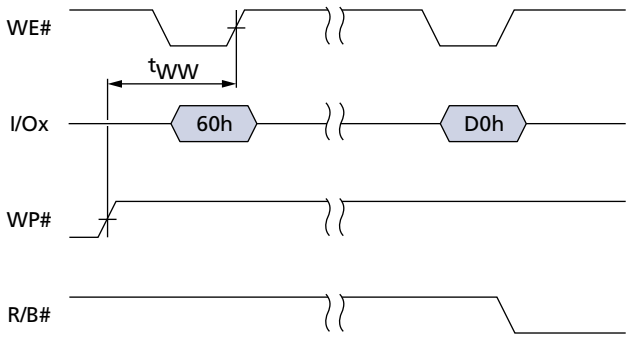


Figure 48: ERASE Disable

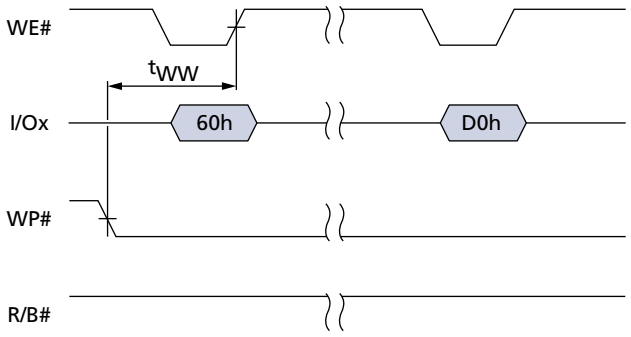


Figure 49: PROGRAM Enable

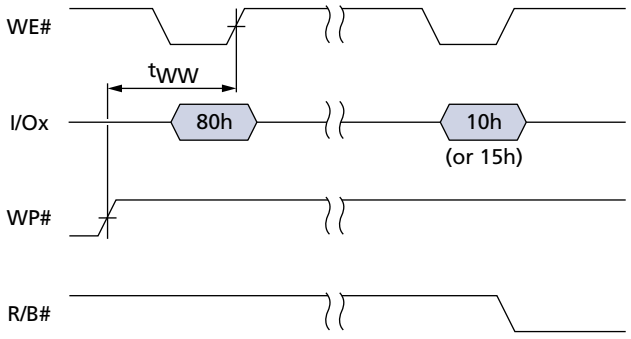


Figure 50: PROGRAM Disable

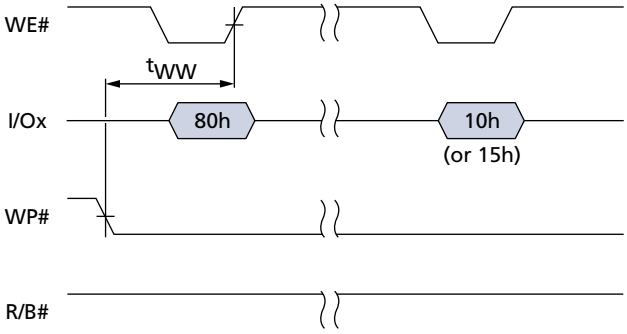


Figure 51: PROGRAM for INTERNAL DATA MOVE Enable

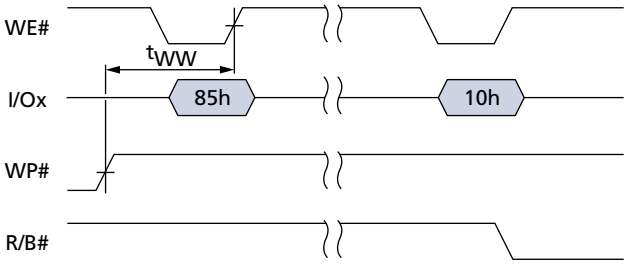
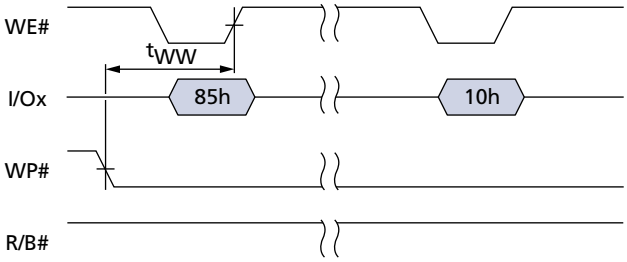


Figure 52: PROGRAM for INTERNAL DATA MOVE Disable



Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in Table 20. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.
Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.
Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.
NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See Table 20 for the bad-block mark.
System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.
Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Check status after each PROGRAM and ERASE operation.
- Under typical conditions, use the minimum required ECC shown in Table 20.
- Use bad-block management and wear-leveling algorithms.

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 20: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB)	2,008
Total available blocks per die	2,048
Minimum required ECC	1-bit ECC per 528 bytes of data
First spare area location	x8: byte 2,048 x16: word 1,024
Bad-block mark	x8: 00h x16: 0000h

Electrical Characteristics

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating ***only***, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 21: Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}

Parameter/Condition		Symbol	Min	Max	Unit
Voltage Input	3.3V	V_{IN}	–0.6	+4.6	V
Voltage input	1.8V	V_{IN}	–0.6	+2.4	V
V_{CC} supply voltage	3.3V	V_{CC}	–0.6	+4.6	V
V_{CC} supply voltage	1.8V	V_{CC}	–0.6	+2.4	V
Storage temperature		T_{STG}	–65	+150	°C
Short circuit output current, I/Os			–	5	mA

Table 22: Recommended Operating Conditions

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Operating temperature	T_A	0	–	+70	°C
Extended temperature		–40	–	+85	°C
V_{CC} supply voltage	V_{CC}	2.7	3.3	3.6	V
V_{CC} supply voltage	V_{CC}	1.65	1.8	1.95	V
Ground supply voltage	V_{SS}	0	0	0	V

VCC Power Cycling

Micron NAND Flash devices are designed to prevent data corruption during power transitions. VCC is internally monitored. (The WP# signal permits additional hardware protection during power transitions.) When VCC reaches 2.5V for a 3.3V device or 1.5V for a 1.8V device, a minimum of 100µs should be allowed for the Flash device to initialize before any commands are executed (see Figures 53 for the states of signals during VCC power cycling).

Both of the following conditions must be satisfied before R/B# will be valid:

- 50µs have elapsed since Vcc started its ramp.
- 10µs have elapsed since Vcc reached ≈ 2.5V for 3.3V or ≈ 1.5V for 1.8V

The RESET command must be issued to all CE#s as the first command after the NAND Flash device is powered on. Each CE# will be busy for a maximum of 1ms after a RESET command is issued.

Each NAND die will draw no more than IST prior to execution of the first RESET command after the device is powered on.

Figure 53: AC Waveforms During Power Transitions

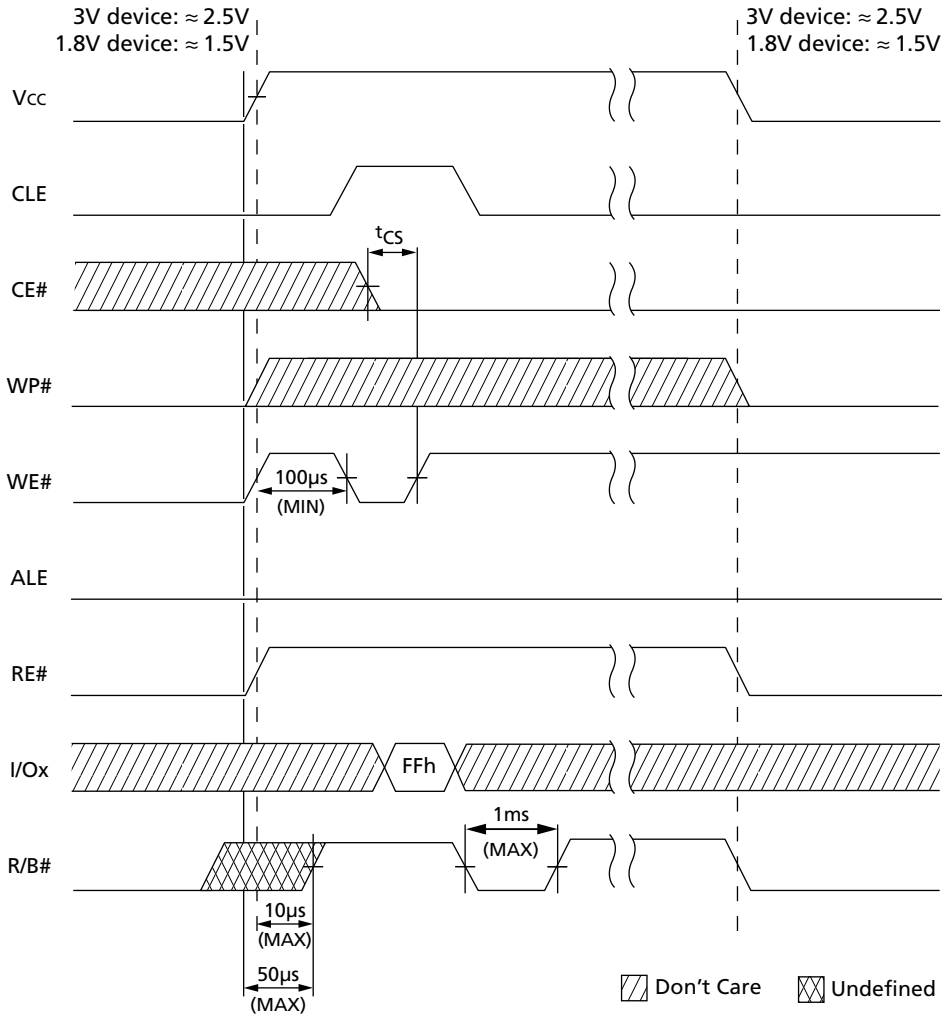


Table 23: DC and Operating Characteristics (3.3V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	$^{t}RC = {}^{t}RC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	$I_{CC}1$	–	25	35	mA	
PROGRAM current	–	$I_{CC}2$	–	25	35	mA	
ERASE current	–	$I_{CC}3$	–	25	35	mA	
Standby current (TTL)	CE# = V_{IH}; WP# = 0V/V_{CC}	$I_{SB}1$	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; WP# = 0V/V_{CC}	$I_{SB}2$	–	10	50	µA	
Staggered power-up current[3]	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10 per die	mA	3
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	
Input high voltage	I/O[7:0], I/O[15:0], CE#, CLE, ALE, WE#, RE#, WP#, R/B#	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –400µA	V_{OH}	2.4	–	–	V	1
Output low voltage	I_{OL} = 2.1mA	V_{OL}	–	–	0.4	V	1
Output low current	V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA	2

Notes:
1. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to "full."
2. I_{OL} (RB#) may need to be relaxed if R/B pull-down strength is not set to "full."
3. Measurement is taken with 1ms averaging intervals and begins after Vcc reaches Vcc (MIN).

Table 24: DC and Operating Characteristics (1.8V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	$^{t}RC = {}^{t}RC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	$I_{CC}1$	–	10	20	mA	
PROGRAM current	–	$I_{CC}2$	–	10	20	mA	
ERASE current	–	$I_{CC}3$	–	10	20	mA	
Standby current (TTL)	CE# = V_{IH}; LOCK = WP# = 0V/V_{CC}	$I_{SB}1$	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; LOCK = WP# = 0V/V_{CC}	$I_{SB}2$	–	10	50	µA	
Staggered power-up current[3]	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10 per die	mA	3
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	
Input high voltage	I/O[7:0], I/O[15:0], CE#, CLE, ALE, WE#, RE#, WP#, R/B#, LOCK	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –100µA	V_{OH}	V_{CC} - 0.1	–	–	V	1
Output low voltage	I_{OL} = 100µA	V_{OL}	–	–	0.1	V	1
Output low current	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	2

Notes: 1. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to "full."
2. I_{OL} (RB#) may need to be relaxed if R/B pull-down strength is not set to "full."
3. Measurement is taken with 1ms averaging intervals and begins after Vcc reaches Vcc (MIN).

Table 25: Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	N_{VB}	MT29F2GxxAxD	2,008	2,048	blocks	1, 2

Notes: 1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below N_{VB} during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block) is guaranteed to be valid with ECC when shipped from the factory.

Table 26: Capacitance

Description	Symbol	Max	Unit	Notes
Input capacitance	C_{IN}	10	pF	1,2
Input/output capacitance (I/O)	C_{IO}	10	pF	1.2

Notes: 1. These parameters are verified in device characterization and are not 100 percent tested.
2. Test conditions: T_c = 25°C; f = 1 MHz; V_{IN} = 0V.

Table 27: Test Conditions

Parameter		Device	Value	Notes
Input pulse levels		MT29F2GxxAxD	0.0V to V_{CC}	
Input rise and fall times			5ns	
Input and output timing levels			$V_{CC}/2$	
Output load	3.3V		1 TTL GATE and CL = 50pF	1
	1.8V		1 TTL GATE and CL = 30pF	1

Notes: 1. Verified in device characterization, not 100 percent tested.

Table 28: AC Characteristics: Command, Data, and Address Input (3.3V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	70	–	ns	1
ALE hold time	^{t}ALH	5	–	ns	
ALE to setup time	^{t}ALS	10	–	ns	
CE# hold time	^{t}CH	5	–	ns	
CLE hold time	^{t}CLH	5	–	ns	
CLE setup time	^{t}CLS	10	–	ns	
CE# setup time	^{t}CS	15	–	ns	
DATA hold time	^{t}DH	5	–	ns	
DATA setup time	^{t}DS	10	–	ns	
WRITE cycle time	^{t}WC	25	–	ns	
WE# pulse width HIGH	^{t}WH	10	–	ns	
WE# pulse width	^{t}WP	12	–	ns	
WP# setup time	^{t}WW	100	–	ns	

Notes: 1. Timing for begins ^{t}ADL begins in the ADDRESS cycle on the final rising edge of WE# and ends with the first rising edge of WE# for data input.

Table 29: AC Characteristics: Command, Data, and Address Input (1.8 V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	100	–	ns	1
ALE hold time	^{t}ALH	4	–	ns	
ALE setup time	^{t}ALS	15	–	ns	
CE# hold time	^{t}CH	4	–	ns	
CLE hold time	^{t}CLH	5	–	ns	
CLE setup time	^{t}CLS	15	–	ns	
CE# setup time	^{t}CS	24	–	ns	
Data hold time	^{t}DH	4	–	ns	
Data setup time	^{t}DS	15	–	ns	
WRITE cycle time	^{t}WC	35	–	ns	
WE# pulse width HIGH	^{t}WH	15	–	ns	
WE# pulse width	^{t}WP	17	–	ns	
WP# setup time	^{t}WW	100	–	ns	

Notes: 1. Timing for begins ^{t}ADL begins in the ADDRESS cycle on the final rising edge of WE# and ends with the first rising edge of WE# for data input.

Table 30: AC Characteristics: Normal Operation (3.3V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	^{t}AR	10	–	ns	1
CE# access time	^{t}CEA	–	25	ns	1
CE# HIGH to output High-Z	^{t}CHZ	–	30	ns	1, 2
CLE to RE# delay	^{t}CLR	10	–	ns	1
CE# HIGH to output hold	^{t}COH	15	–	ns	1
Cache busy in page read cache mode (first 31h)	^{t}DCBSYR1	–	3	µs	1
Cache busy in page read cache mode (next 31h and 3Fh)	^{t}DCBSYR2	^{t}DCBSYR1	25	µs	1
Output High-Z to RE# LOW	^{t}IR	0	–	ns	1
Data transfer from Flash array to data register	^{t}R	–	25	µs	1
READ cycle time	^{t}RC	25	–	ns	1
RE# access time	^{t}REA	–	20	ns	1
RE# HIGH hold time	^{t}REH	10	–	ns	1
RE# HIGH to output hold	^{t}RHOH	15	–	ns	1
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	1
RE# HIGH to output High-Z	^{t}RHZ	–	100	ns	1, 2
RE# LOW to output hold	^{t}RLOH	5	–	ns	1
RE# pulse width	^{t}RP	12	–	ns	1
Ready to RE# LOW	^{t}RR	20	–	ns	1
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	1, 3
WE# HIGH to busy	^{t}WB	–	100	ns	1, 4
WE# HIGH to RE# LOW	^{t}WHR	60	–	ns	1

Notes:
1. AC characteristics may need to be relaxed if I/O drive strength is not set to "full."
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will go busy for a maximum of 1ms. Thereafter, the device goes busy for maximum 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

Table 31: AC Characteristics: Normal Operation (1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	^{t}AR	10	–	ns	1
CE# access time	^{t}CEA	–	30	ns	1
CE# HIGH to output High-Z	^{t}CHZ	–	45	ns	1, 2
CLE to RE# delay	^{t}CLR	10	–	ns	1
CE# HIGH to output hold	^{t}COH	15	–	ns	1
Cache busy in page read cache mode (first 31h)	^{t}DCBSYR1	–	3	µs	1
Cache busy in page read cache mode (next 31h and 3Fh)	^{t}DCBSYR2	^{t}DCBSYR1	25	µs	1
Output High-Z to RE# LOW	^{t}IR	0	–	ns	1
Data transfer from Flash array to data register	^{t}R	–	25	µs	1
READ cycle time	^{t}RC	35	–	ns	1
RE# access time	^{t}REA	–	24	ns	1
RE# HIGH hold time	^{t}REH	15	–	ns	1
RE# HIGH to output hold	^{t}RHOH	15	–	ns	1
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	1
RE# HIGH to output High-Z	^{t}RHZ	–	100	ns	1, 2
RE# LOW to output hold	^{t}RLOH	0	–	ns	1
RE# pulse width	^{t}RP	17	–	ns	1
Ready to RE# LOW	^{t}RR	20	–	ns	1
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	1, 3
WE# HIGH to busy	^{t}WB	–	100	ns	1, 4
WE# HIGH to RE# LOW	^{t}WHR	80	–	ns	1

Notes:
1. AC characteristics may need to be relaxed if I/O drive strength is not set to "full."
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will go busy for a maximum of 1ms. Thereafter, the device goes busy for maximum 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

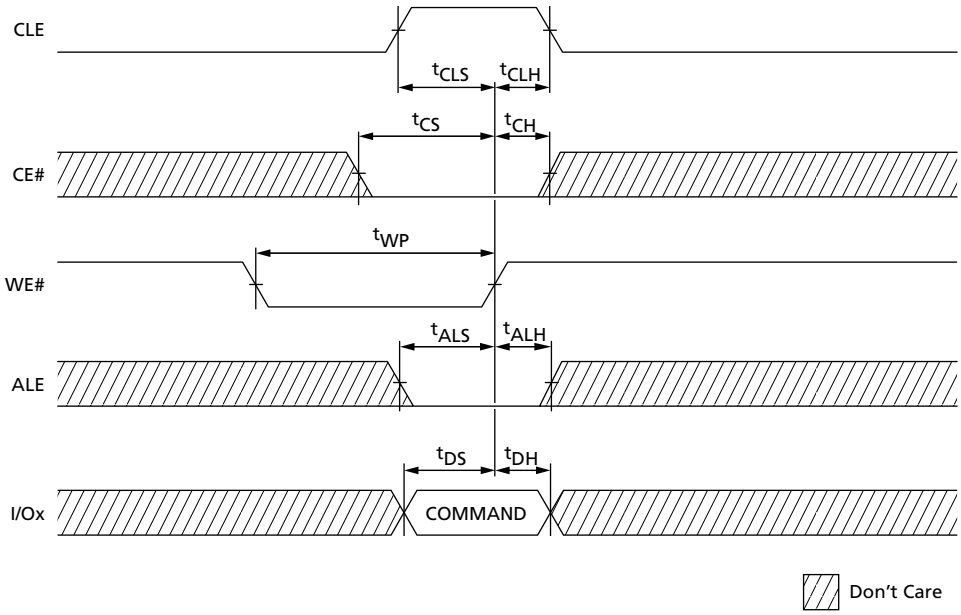
Table 32: PROGRAM/ERASE Characteristics

Symbol	Parameter	Typ	Max	Unit	Notes
NOP	Number of partial page programs	–	4	cycles	1
^{t}BERS	BLOCK ERASE operation time	0.5	3	ms	
^{t}CBSY	Busy time for PROGRAM CACHE operation (3.3V)	3	500	µs	2
^{t}CBSY	Busy time for PROGRAM CACHE operation (1.8V)	3	600	µs	2
^{t}FEAT	Busy time for SET FEATURES and GET FEATURES operations (3.3V)	–	1	µs	
^{t}FEAT	Busy time for SET FEATURES and GET FEATURES operations (1.8V)	–	3	µs	
^{t}LBSY	Busy time for PROGRAM/ERASE on locked block	–	3	µs	
^{t}LPROG	LAST PAGE PROGRAM operation time	–	–	–	3
^{t}OBSY	Busy time for OTP DATA PROGRAM operation if OTP is protected	–	30	µs	
^{t}PROG	PAGE PROGRAM operation time (1.8V)	300	600	µs	
^{t}PROG	PAGE PROGRAM operation time (3.3V)	220	500	µs	

Notes: 1. Four total partial-page programs to the same page.
2. ^{t}CBSY MAX time depends on timing between internal program completion and data-in.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).

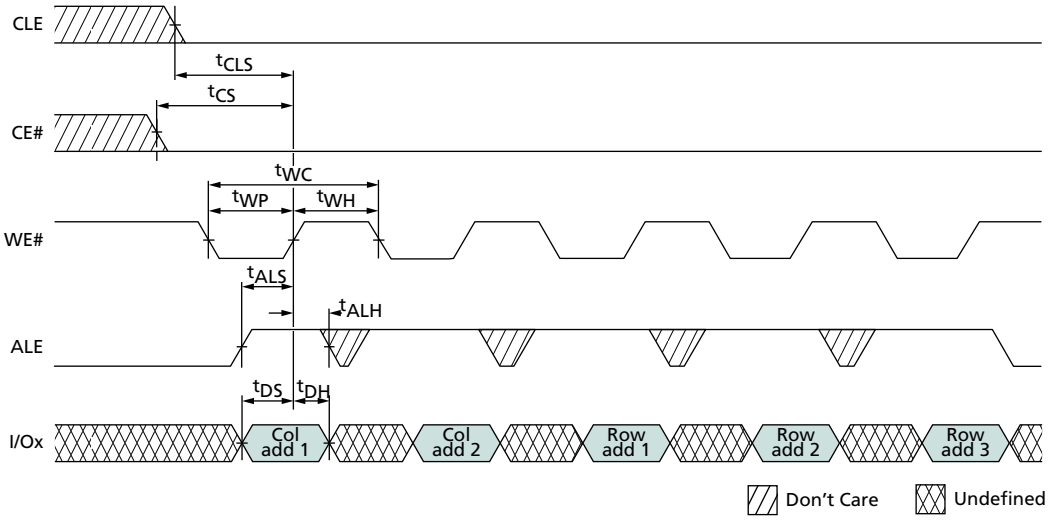
Timing Diagrams

Figure 54: COMMAND LATCH Cycle



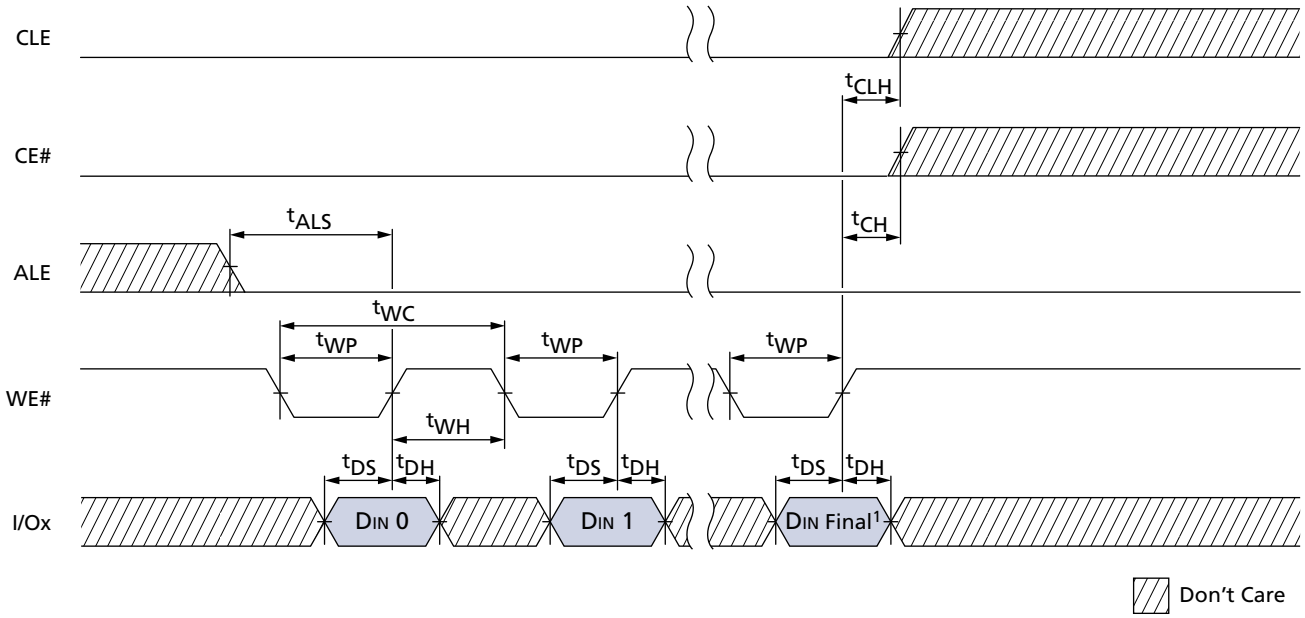
Note: x16: I/O[15:8] must be set to "0."

Figure 55: ADDRESS LATCH Cycle



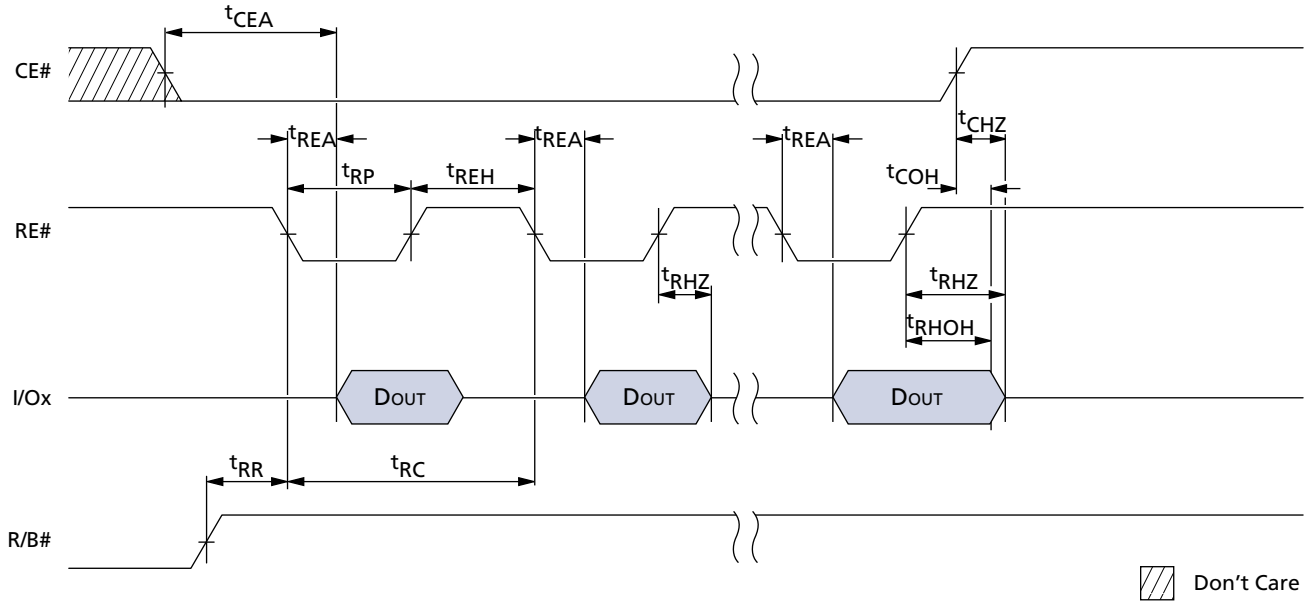
Note: x16: I/O[15:8] must be set to "0."

Figure 56: INPUT DATA LATCH Cycle



Notes: 1. DIN Final = 2,111 (x8).

Figure 57: SERIAL ACCESS Cycle After READ



Note: Use this timing diagram for $^{t}RC \geq 30ns$.

Figure 58: Serial Access Cycle After READ (EDO Mode)

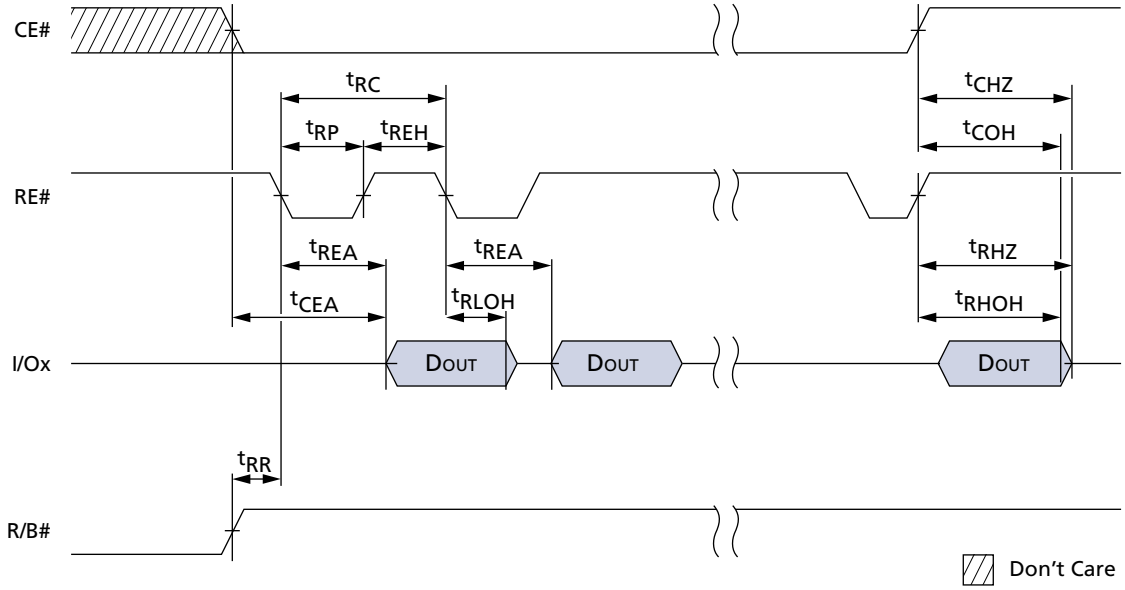


Figure 59: READ STATUS Operation

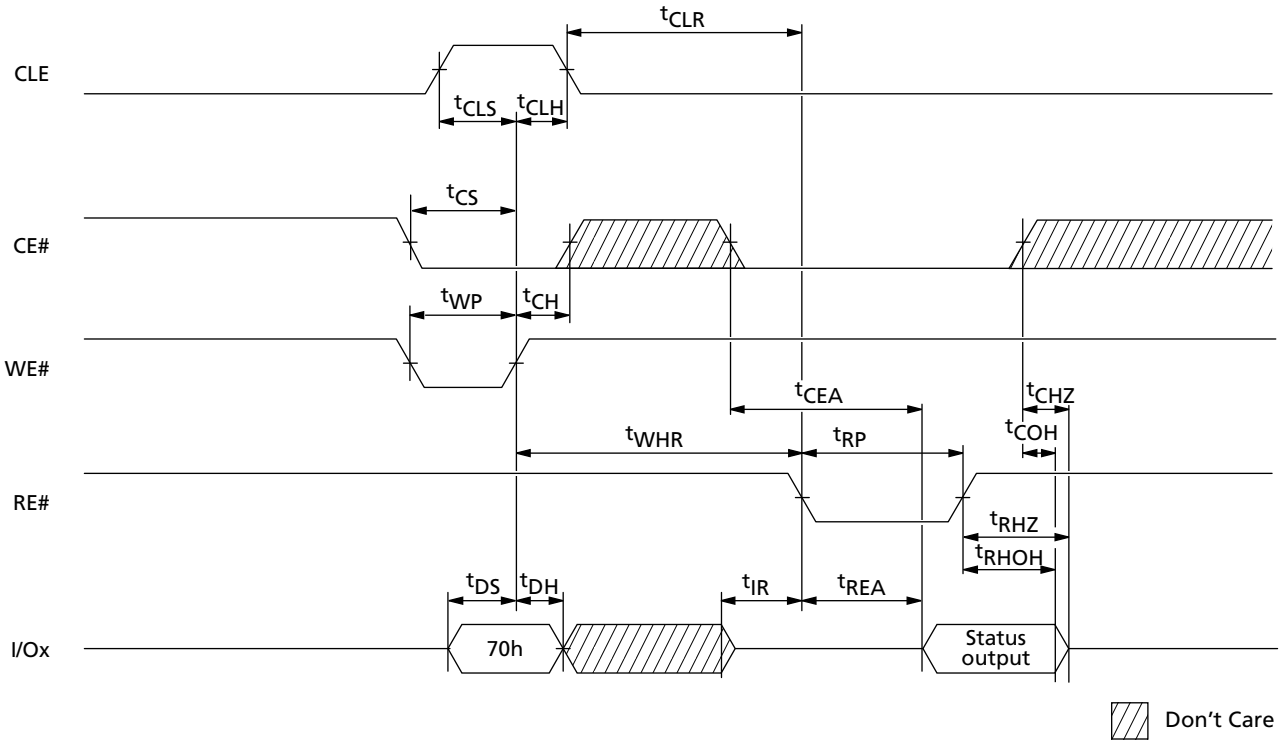
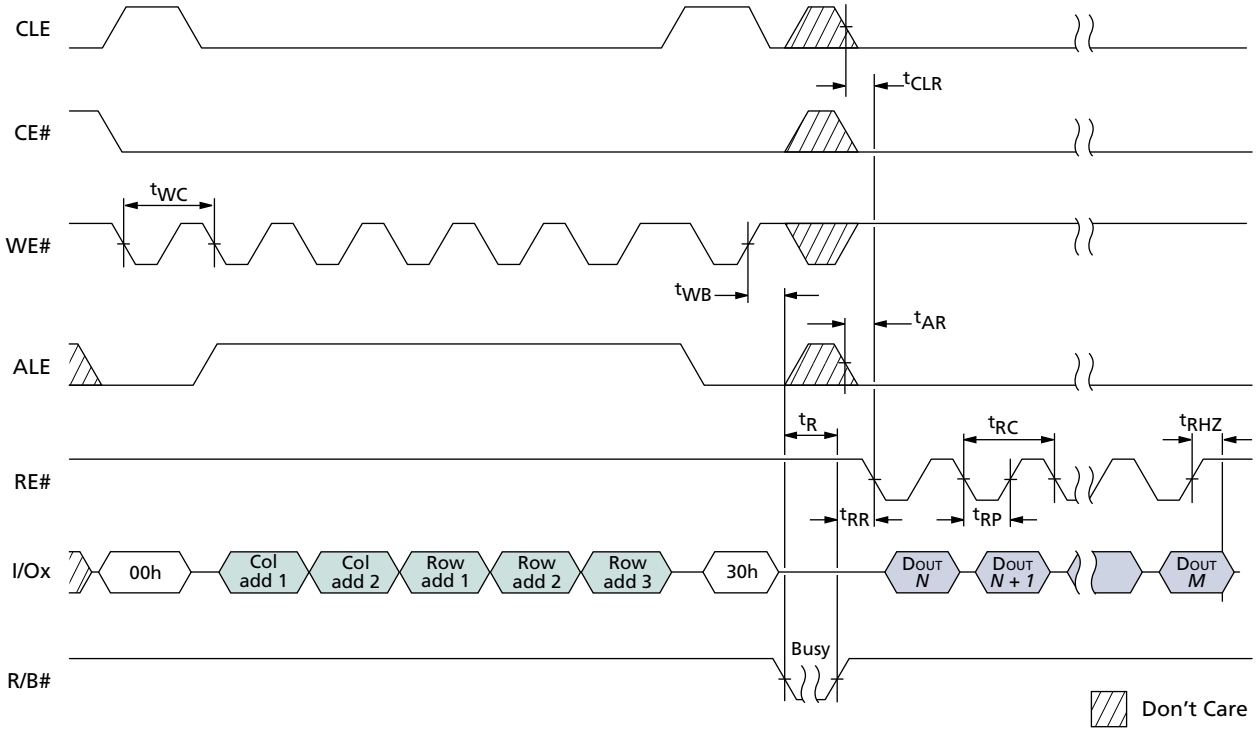


Figure 60: PAGE READ Operation



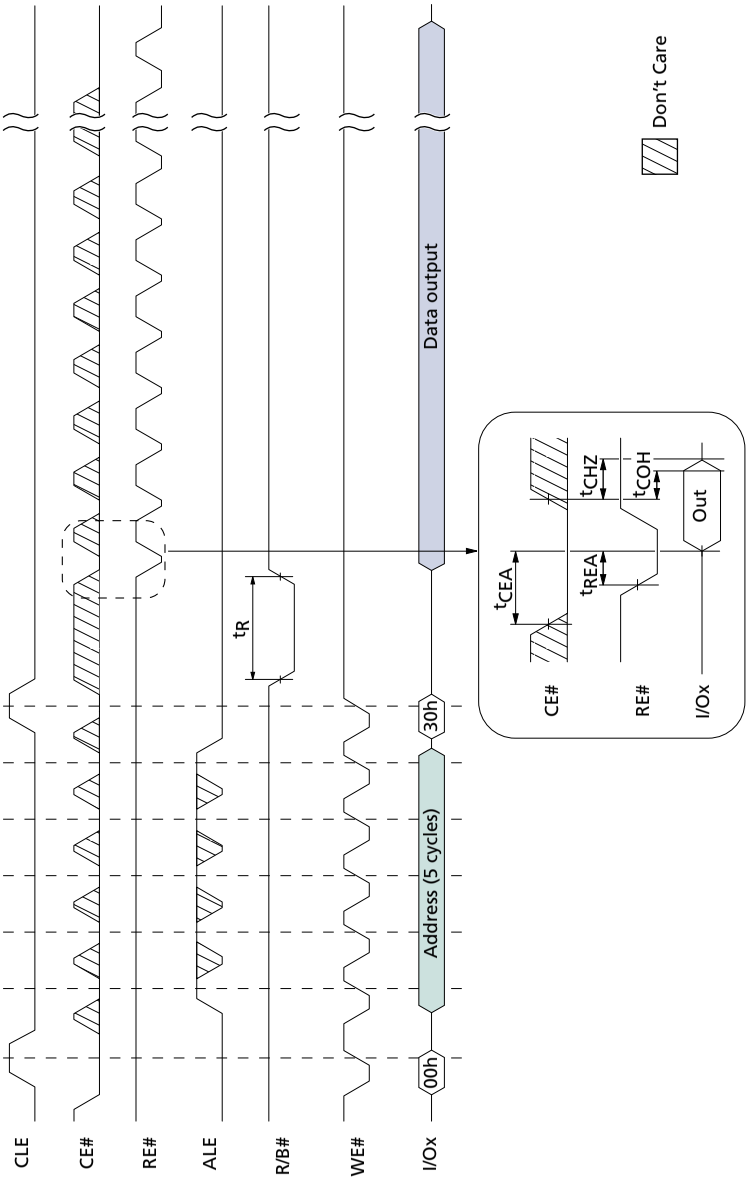


Figure 61: READ Operation with CE# "Don't Care"

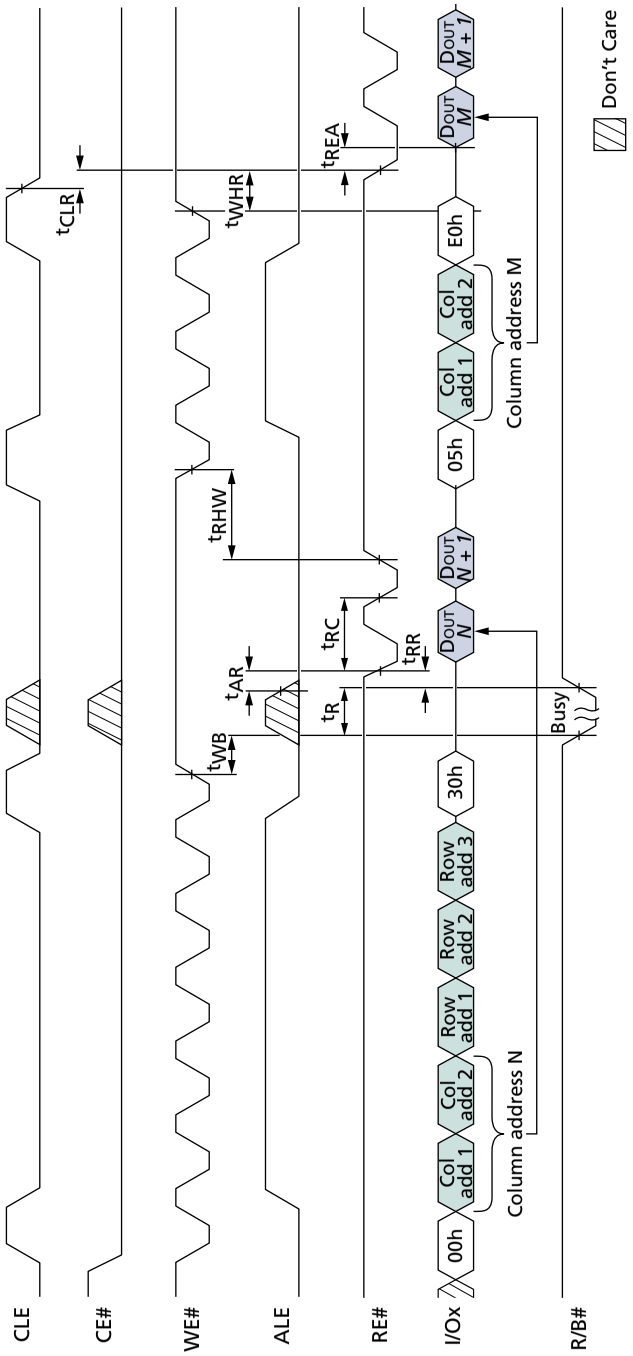


Figure 62: RANDOM DATA READ Operation

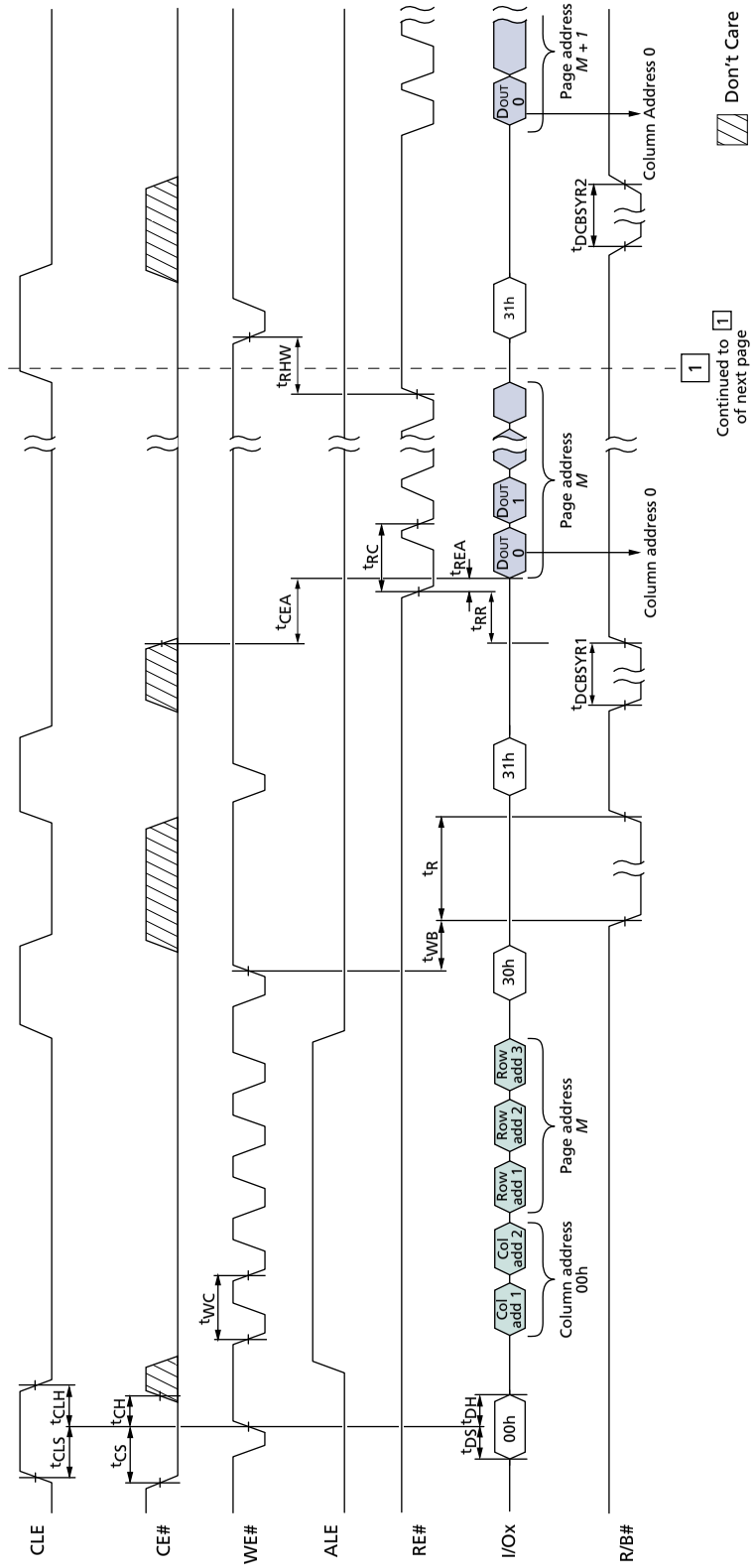


Figure 63: PAGE READ CACHE MODE Operation, Part 1 of 2

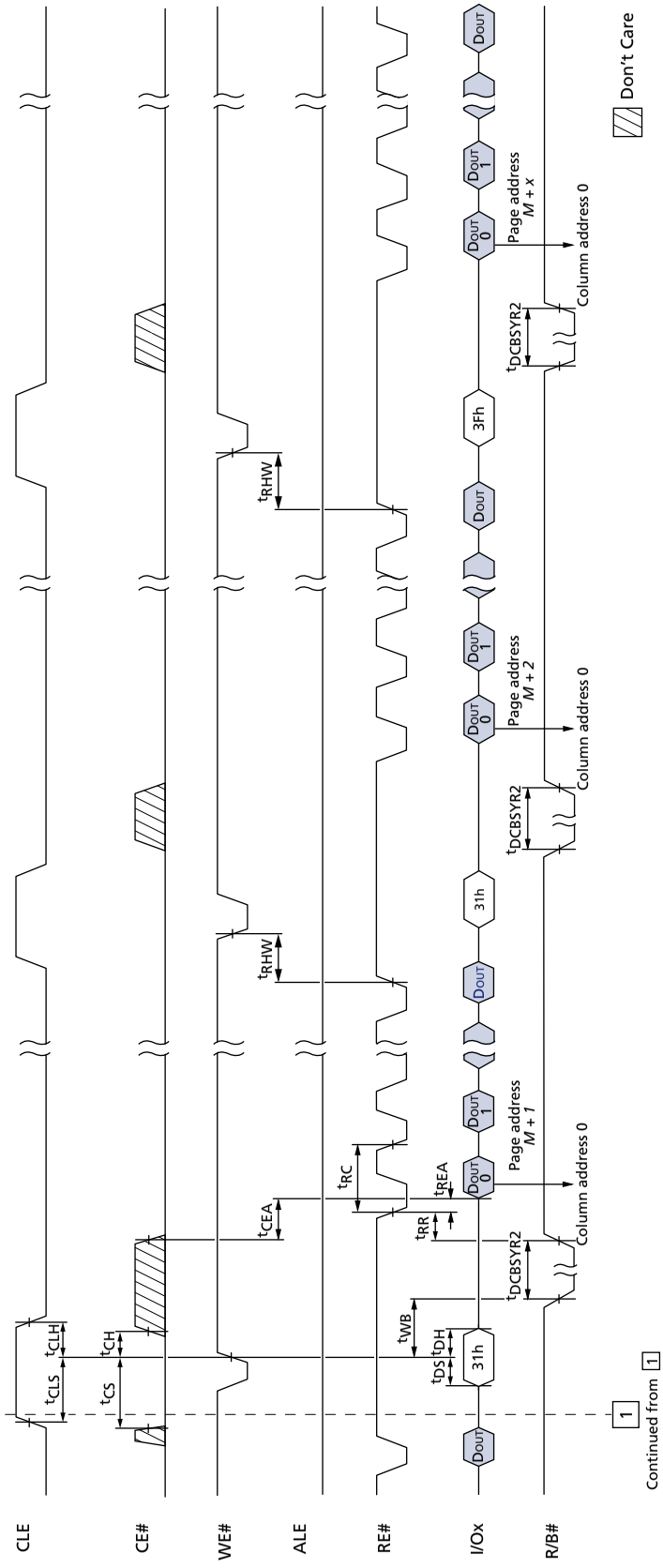


Figure 64: PAGE READ CACHE MODE Operation, Part 2 of 2

Figure 65: PAGE READ CACHE MODE Operation Without R/B#, Part 1 of 2

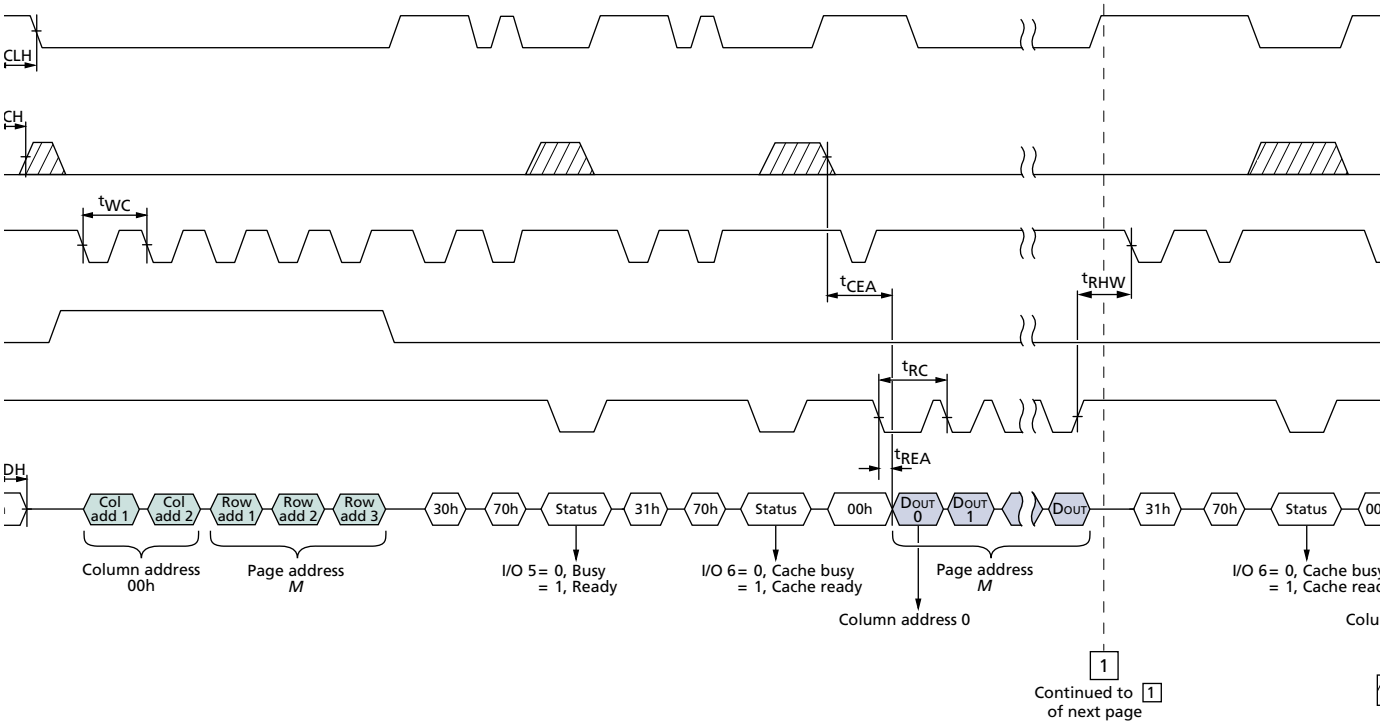


Figure 66: PAGE READ CACHE MODE Operation Without R/B#, Part 2 of 2

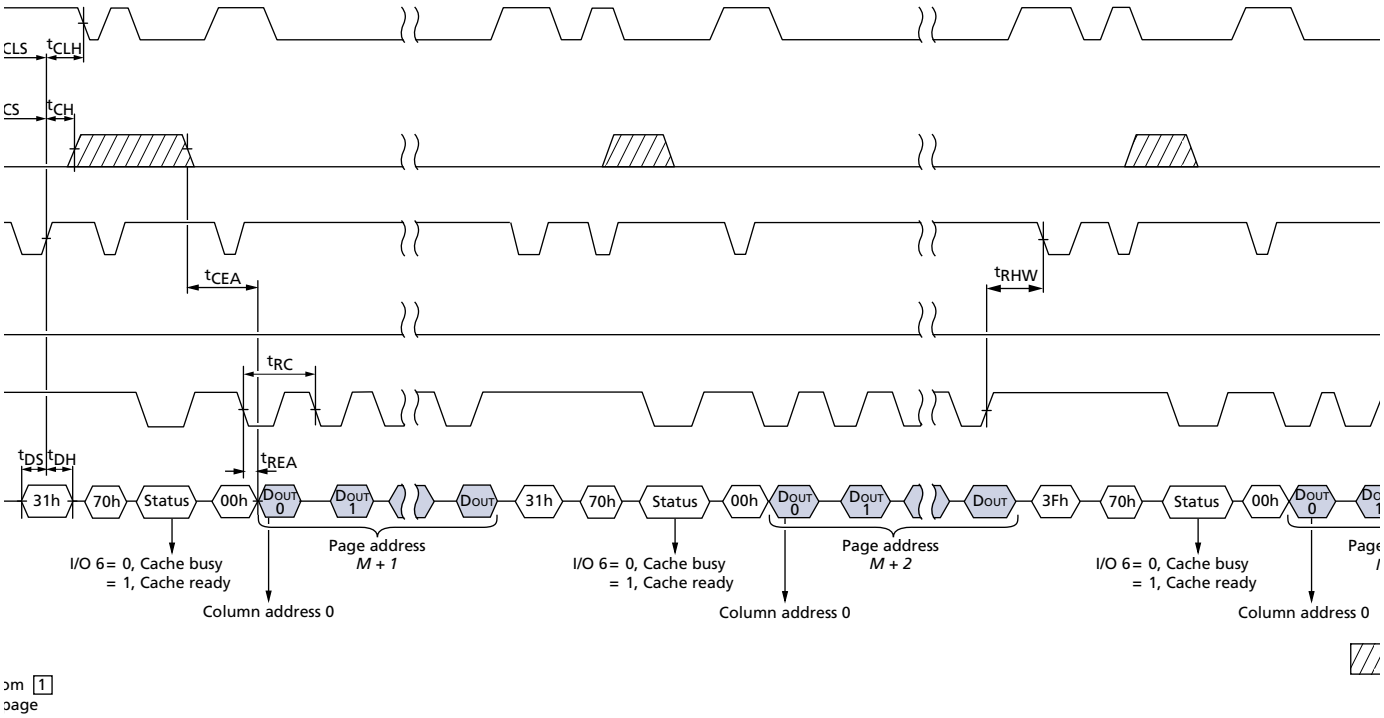
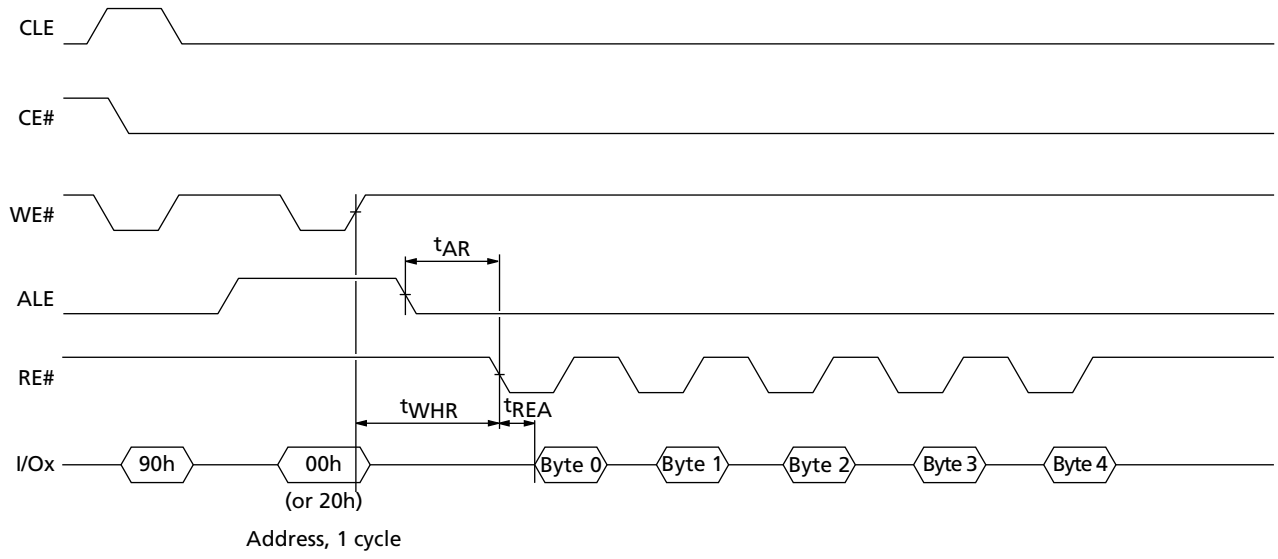


Figure 67: READ ID Operation



Note: See Table 9 on page 30 for actual values.

Figure 68: PROGRAM PAGE Operation

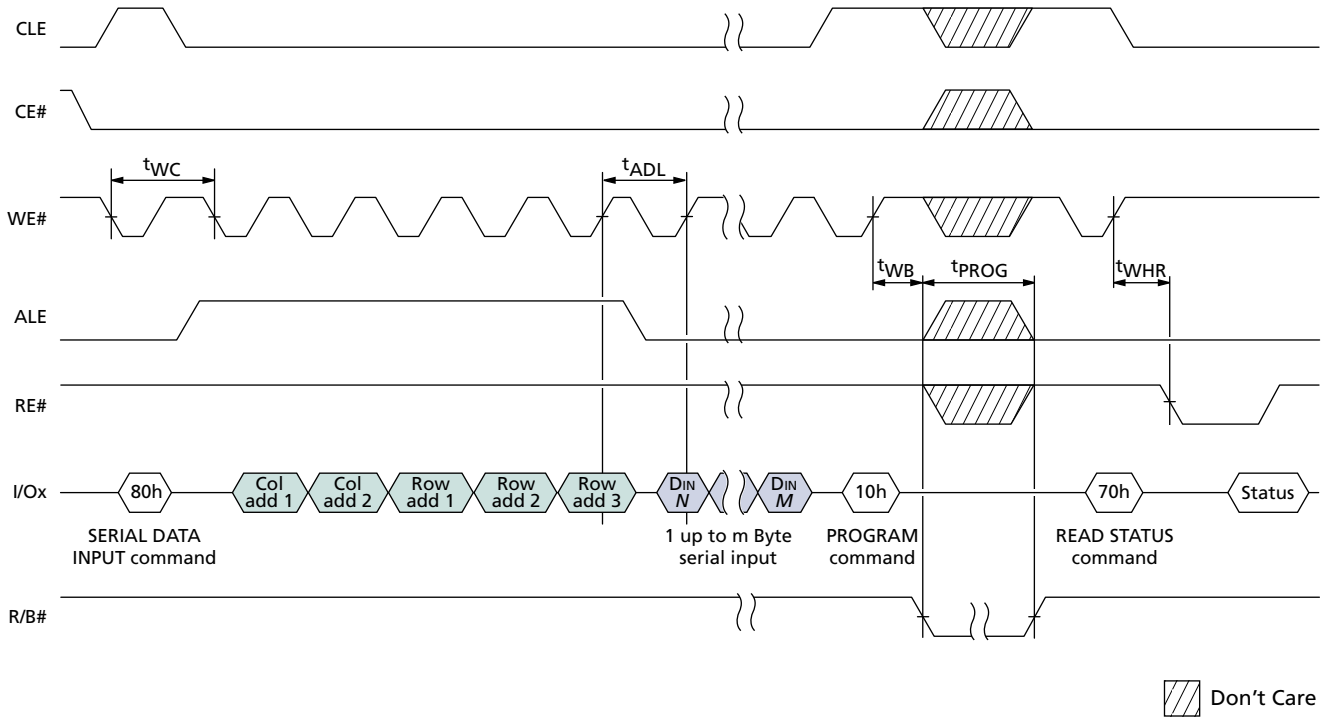
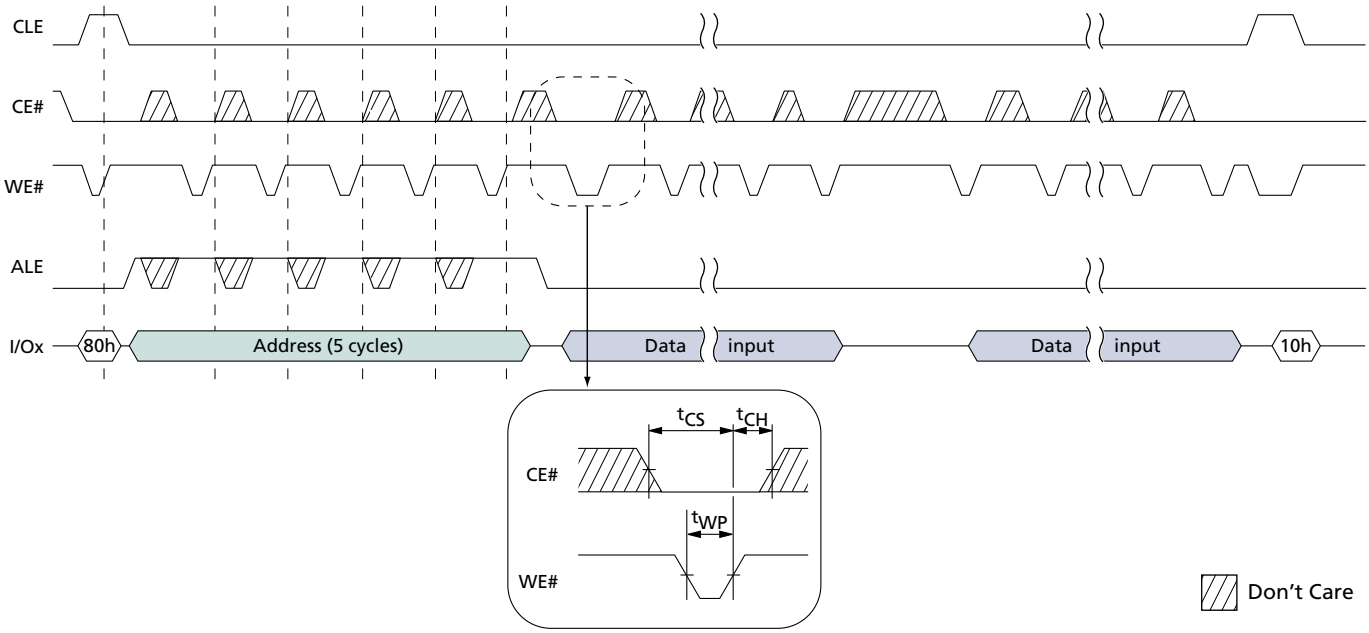


Figure 69: Program Operation with CE# "Don't Care"



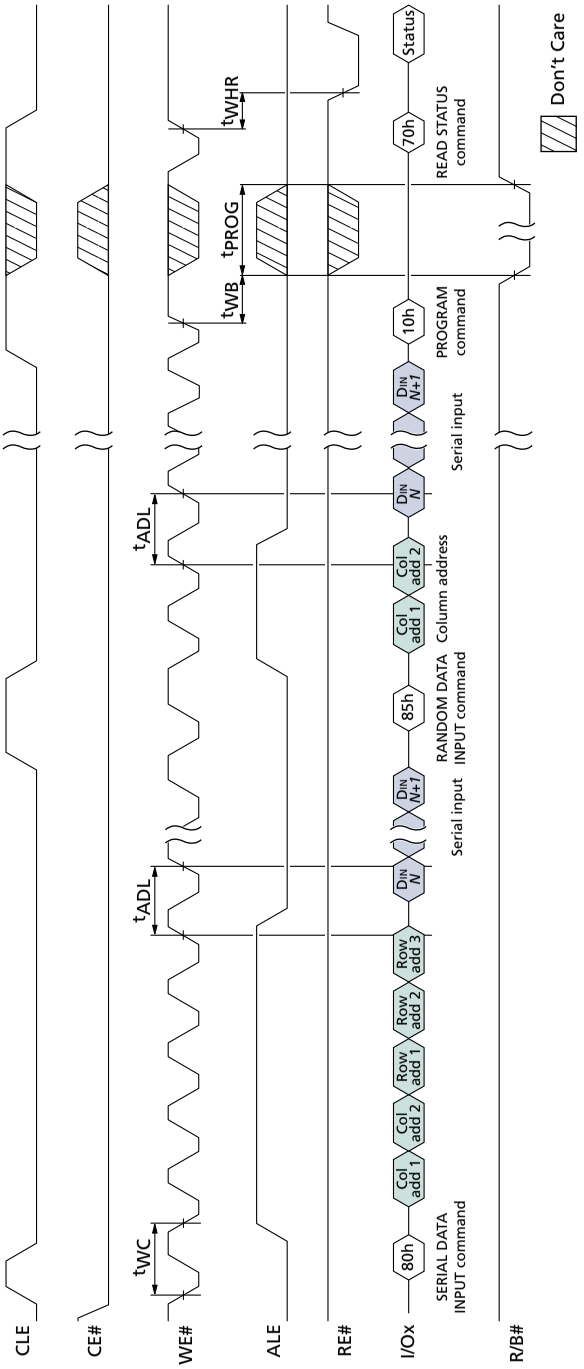


Figure 70: PROGRAM PAGE Operation with RANDOM DATA INPUT

Figure 71: INTERNAL DATA MOVE Operation

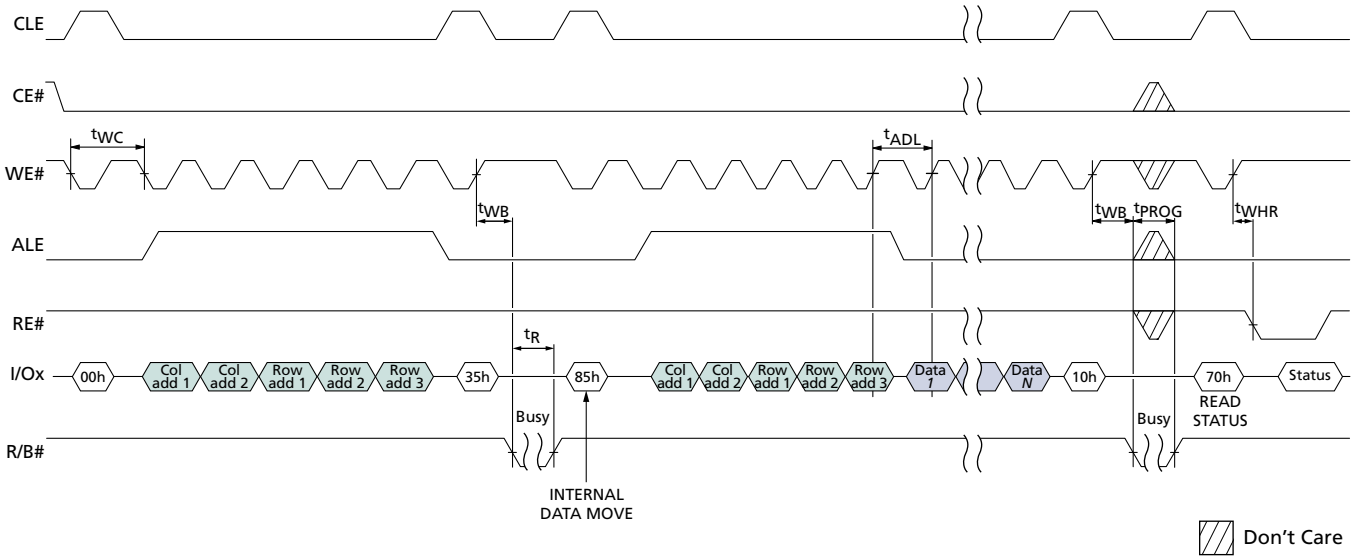


Figure 72: PROGRAM PAGE CACHE MODE Operation

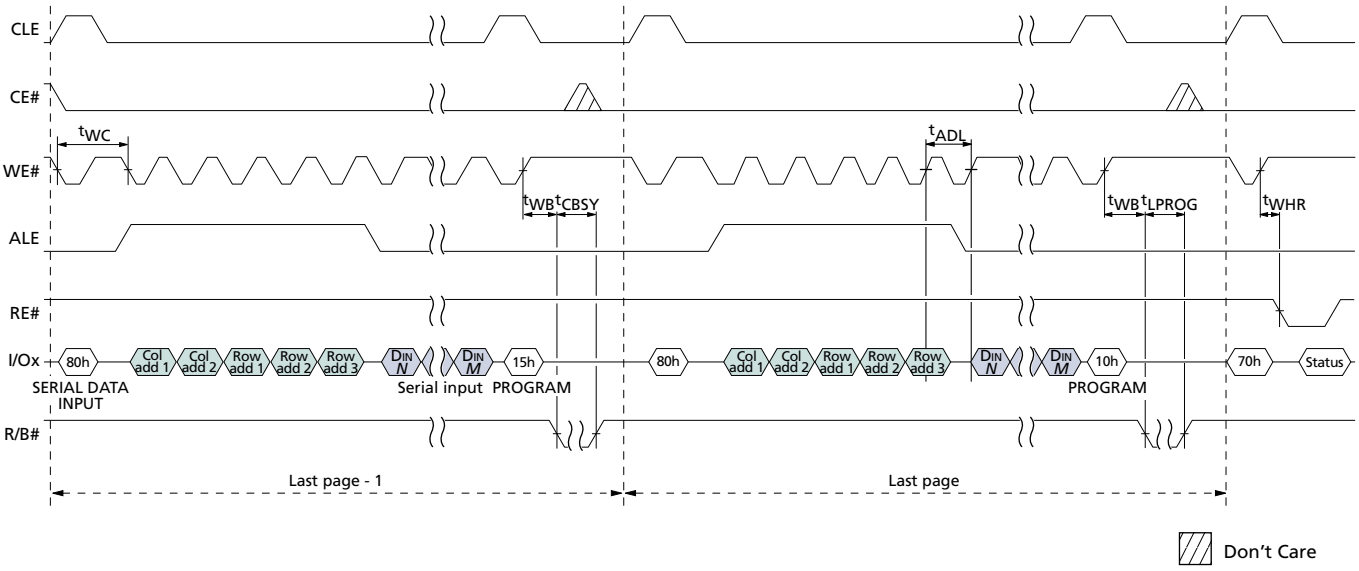


Figure 73: PROGRAM PAGE CACHE MODE Operation Ending on 15h

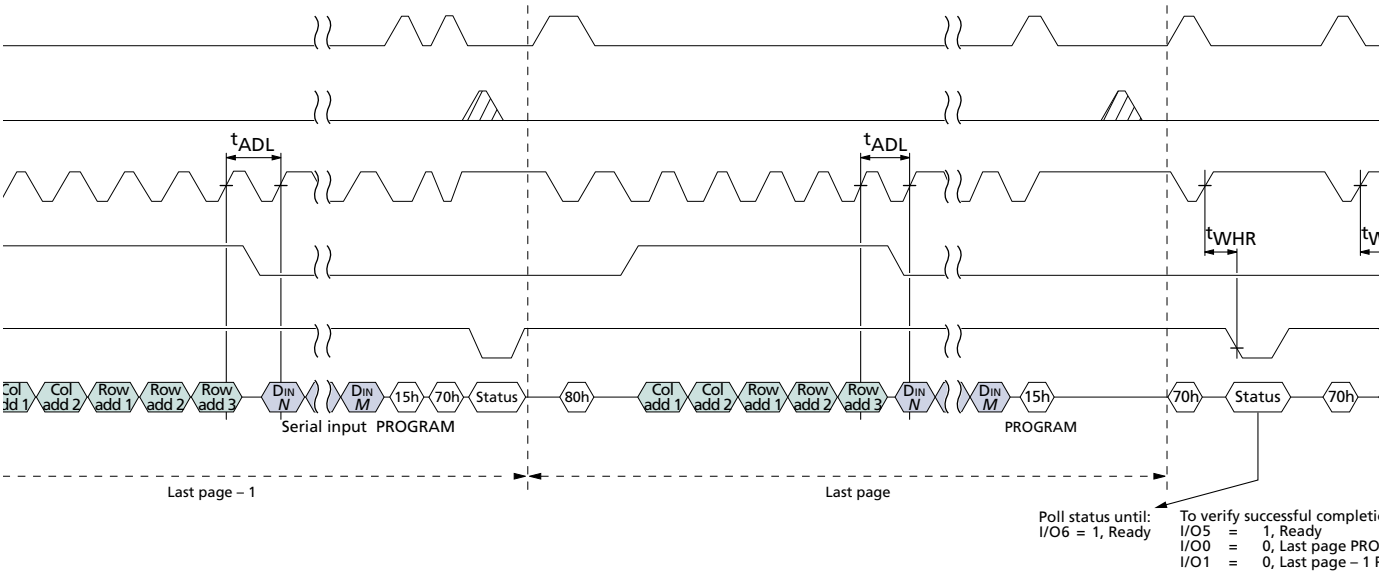


Figure 74: BLOCK ERASE Operation

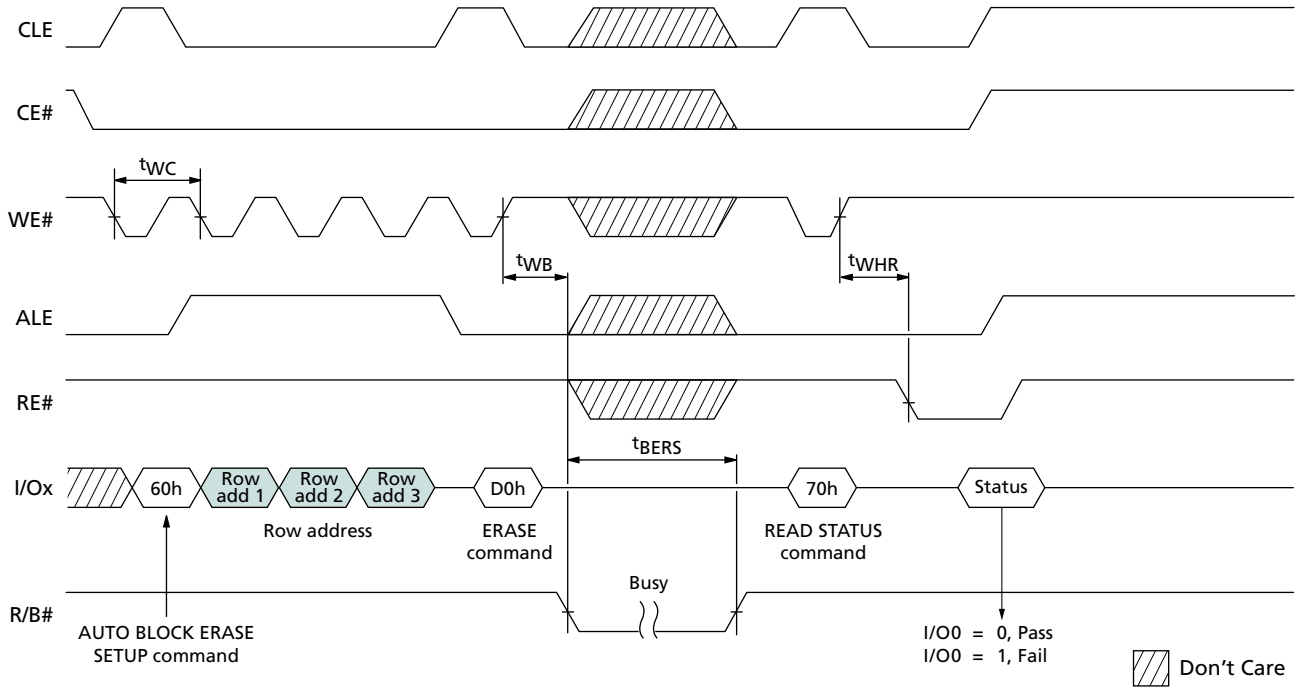
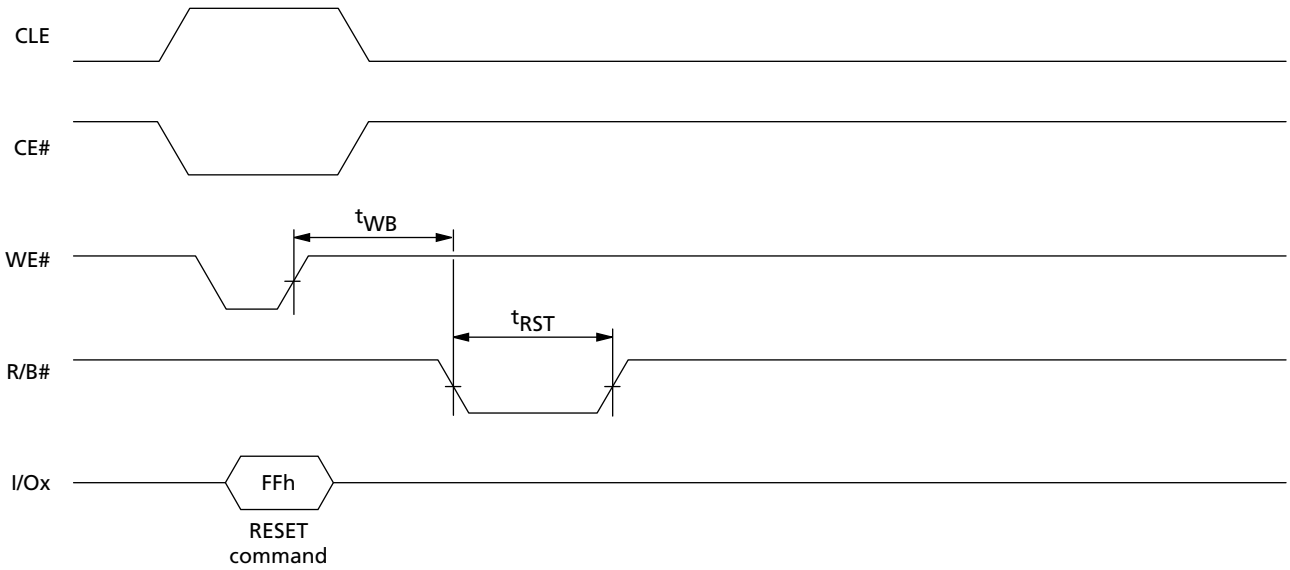


Figure 75: RESET Operation



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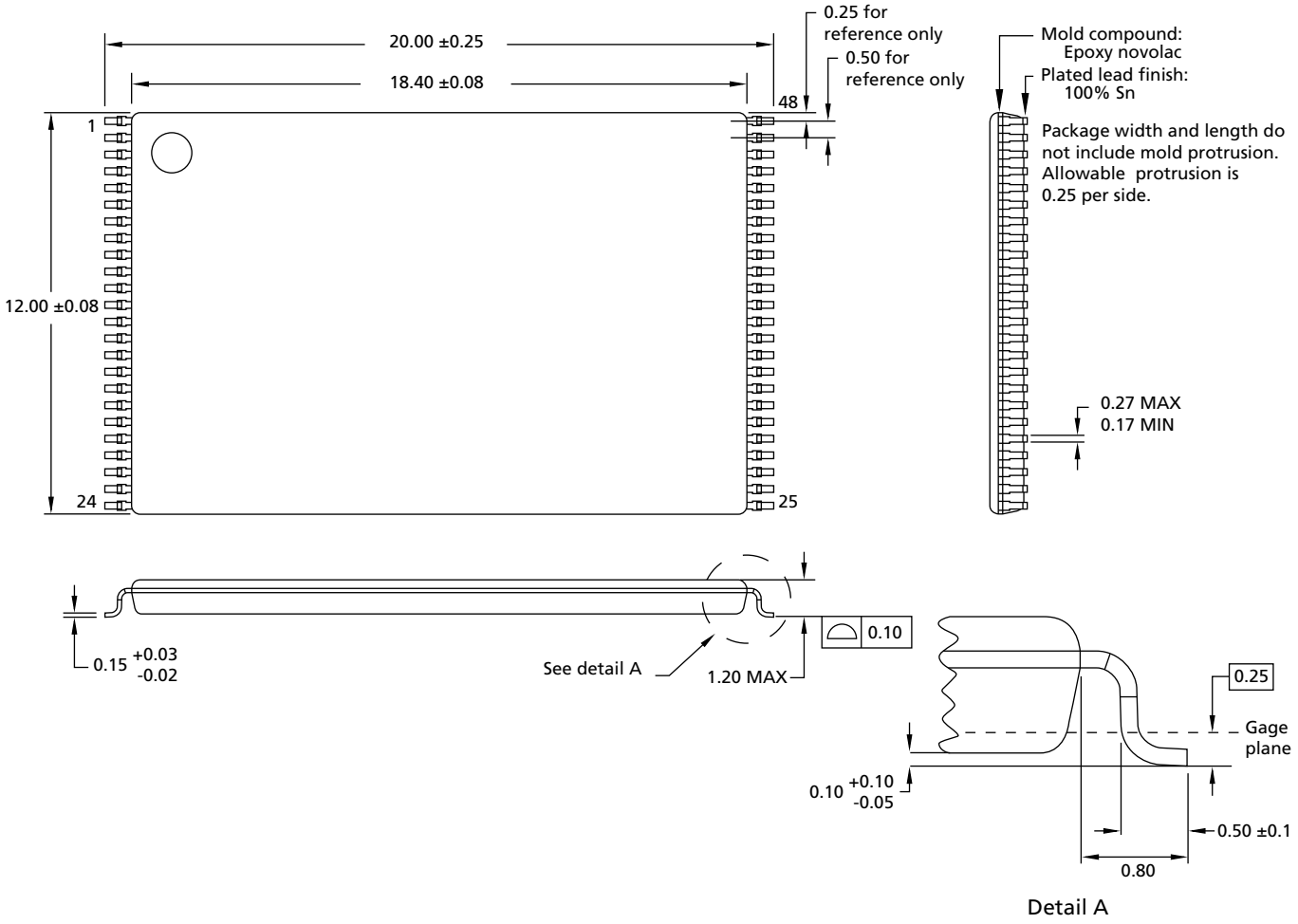
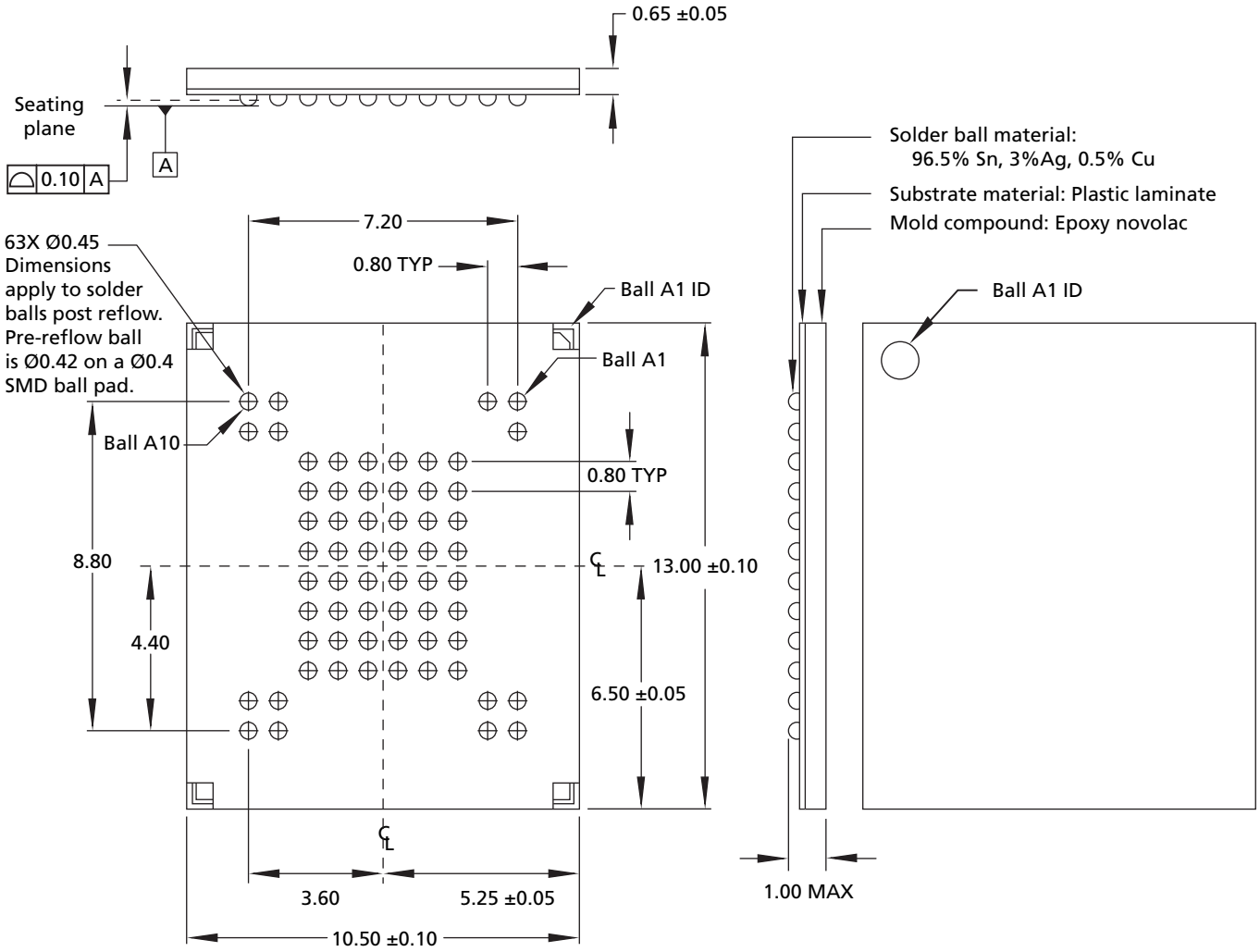
Package Dimensions

Figure 76: 48-Pin TSOP Package



Note: All dimensions are in millimeters.

Figure 77: 63-Ball VFBGA Package



Note: All dimensions are in millimeters.

Revision History

Rev. A, Production 8/08

- Initial release.