AN 15.17

PCB Layout Guide for USB Hubs

Introduction

This application note provides information on designing a printed circuit board (PCB) for the SMSC USB251x/xB Family of USB 2.0 Hub Controllers including industrial grade products in the family. The PCB only requires two layers of copper.

Two Layer PCB

A successful PCB with only two copper layers for the USB 2.0 hub designs decreases the total cost of a finished USB Hub compared to a four-layer design. However, the design of the PCB will require more care to maintain controlled USB impedance and to provide good supply and ground paths. This application note addresses several of these issues. The self-powered hub evaluation board EVB-USB2514QFN36 is used as an example for this application note. **The schematic for this board is shown on the SMSC website at http://www.smsc.com/EVB-USB2513Q36-BAS**

PCB Constraints

- Material: FR-4
- Copper thickness: 1.0 to 2.0 ounces
- Dielectric thickness: 37 mils (1 mm finished board thickness)

PCB Considerations

- Control differential impedance on USB traces (90 Ω).
- Isolate USB traces from other circuitry and signals.
- Tie the shield on upstream connector to the shield on downstream connector with a low impedance, wide and isolated trace, preferably along the periphery of the design.
- Provide adequate low impedance supply connection to VBUS of downstream ports.
- Keep bulk capacitors for downstream port's VBUS power close to connectors.
- Isolate the crystal and the oscillator.
- Isolate the RBIAS resistor and keep traces short.
- Bypass capacitors should be placed on the top side; no components should be placed on the bottom side for reduced assembly cost.

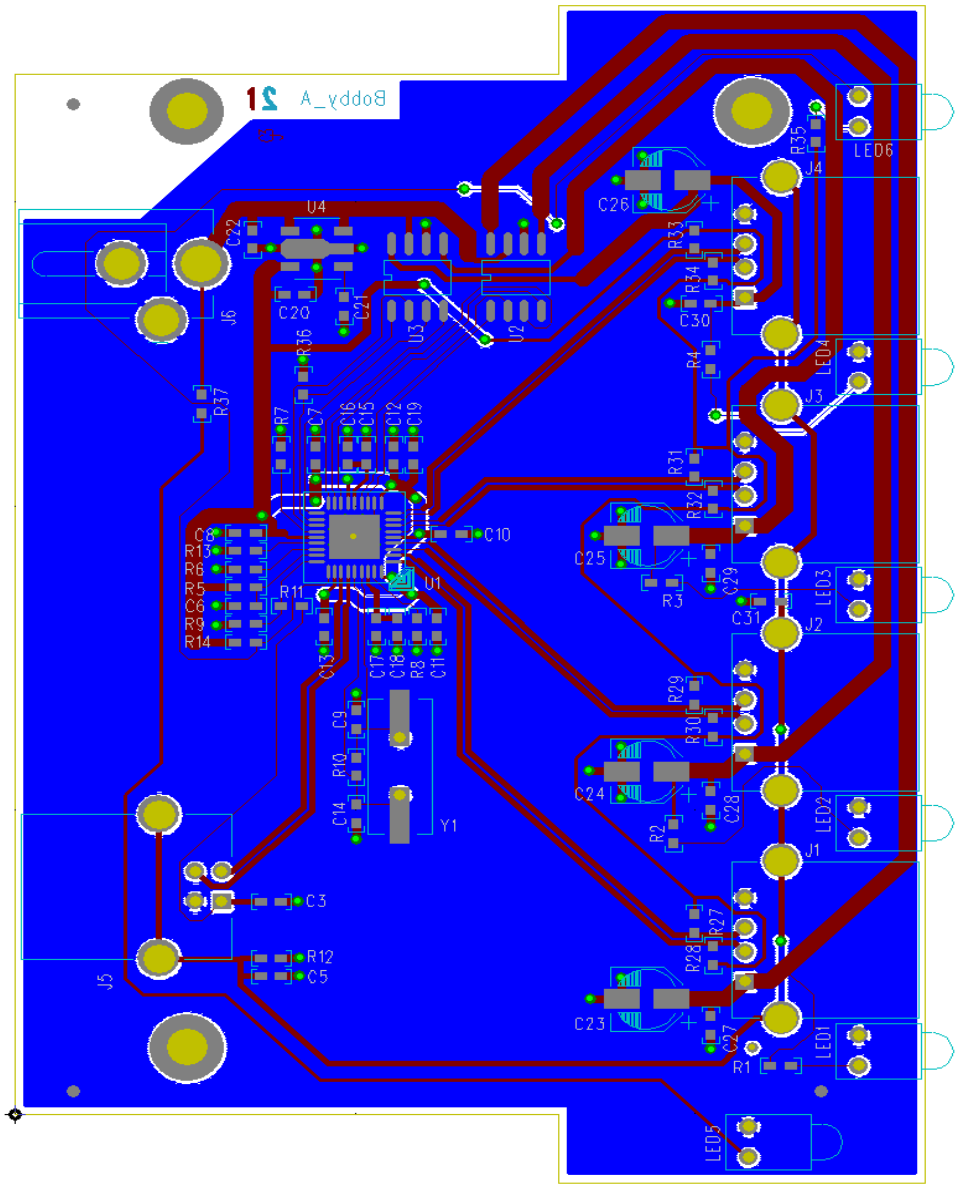

Figure 1 Overall View Showing Three Layers:
Top Silk-Screen (white), Top Copper Layer (red) and Bottom Copper Layer (blue)

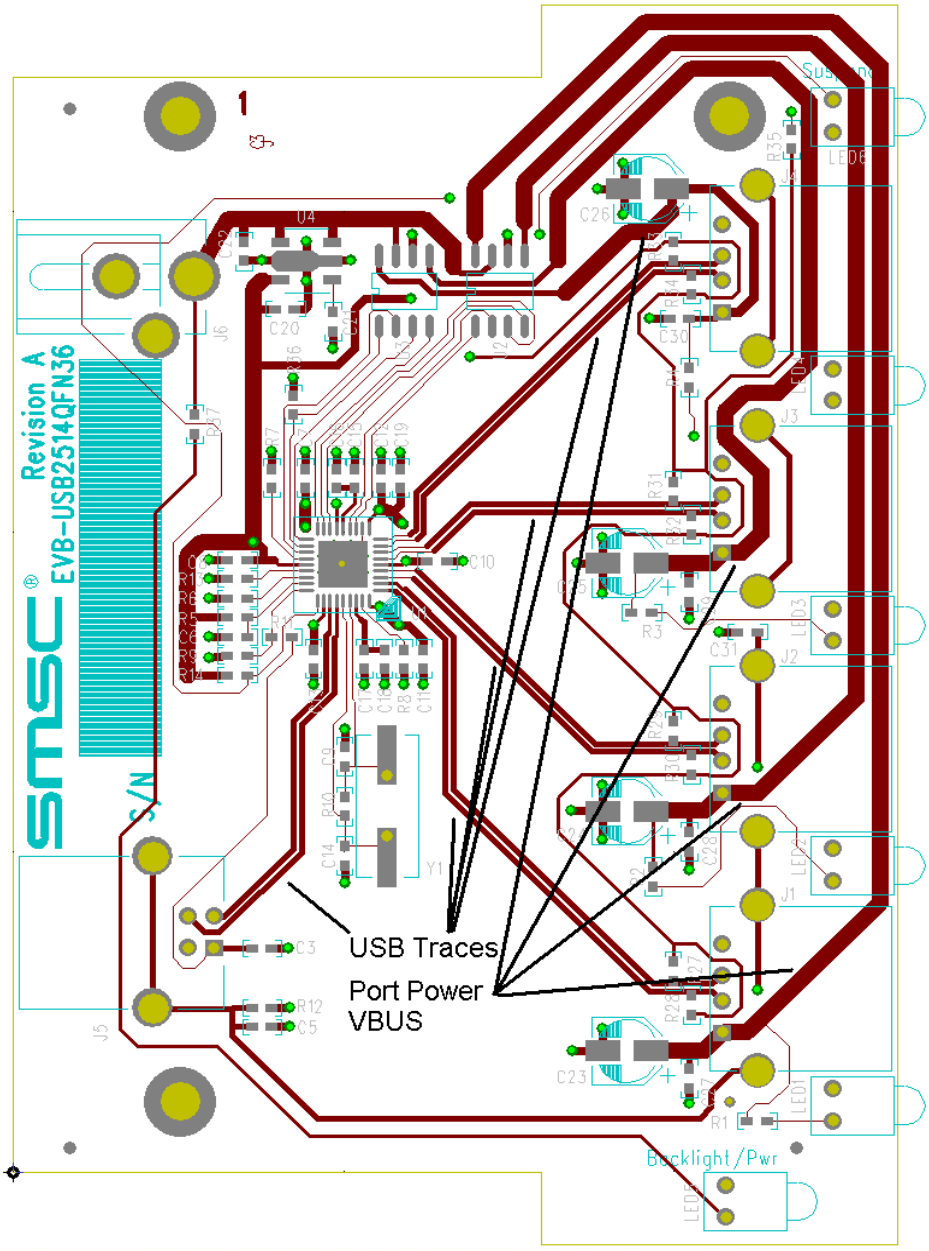

Figure 2 Top Layer Copper: USB Traces and Port Power

Controlled Impedance for USB Traces

The USB 2.0 specification requires that USB DP/DM traces maintain nominally 90 Ω differential impedance. In this design, the USB DP/DM traces are 27 mils wide with 5 mils spacing. A continuous ground plane is required directly beneath the DP/DM traces and extending at least five times the spacing width (5 x 5 mils = 25 mils) to either side of DP and DM.

- Maintain close to 90 Ω differential impedance. For different dielectric thickness, copper thickness or board stack-up, trace width and spacing needs to be recalculated.
- Maintain symmetry between DP and DM in regards to shape. Trace lengths should be matched.
- Keep unrelated signal traces, supplies and components away from DP/DM traces. A good rule of thumb to apply is using five times the trace width (ex., 25 mils in this design). This minimizes coupling effects and impedance mismatch along the trace.

- Single ended impedance is not as critical as the differential impedance. A range from 45 to 80 Ω is acceptable.

In Figure 3 the USB traces are 27 x 5 mils, but close to the pads of the USB2514 they are tapered down to 7 mils wide to access the pads of the USB2514. The discontinuity in the trace width causes an impedance mismatch. It is important to keep the length of the discontinuity as short as possible to reduce its impact to the USB signal quality.

Another example of a compromise is that the ideal clearance distance of five times the width, 25 mils in this case, is not met near the chip as shown in Figure 3 on page 4. Decoupling capacitors are placed as close to the chip as possible to keep series inductance low. Since the capacitors are mounted on the top side only one via in series with the capacitor is needed to connect the ground plane on the bottom layer. Note that in this case the clearance is minimal space between the pads for the capacitor and DP/DM traces. The pad size is small relative to the overall trace length. Keeping this spacing as large as possible, and keeping the length of the violation as short as possible makes the negative effect on the impedance mismatch smaller. In this case it is desirable to keep the power trace from the USB2514 to the decoupling capacitor as short as possible.

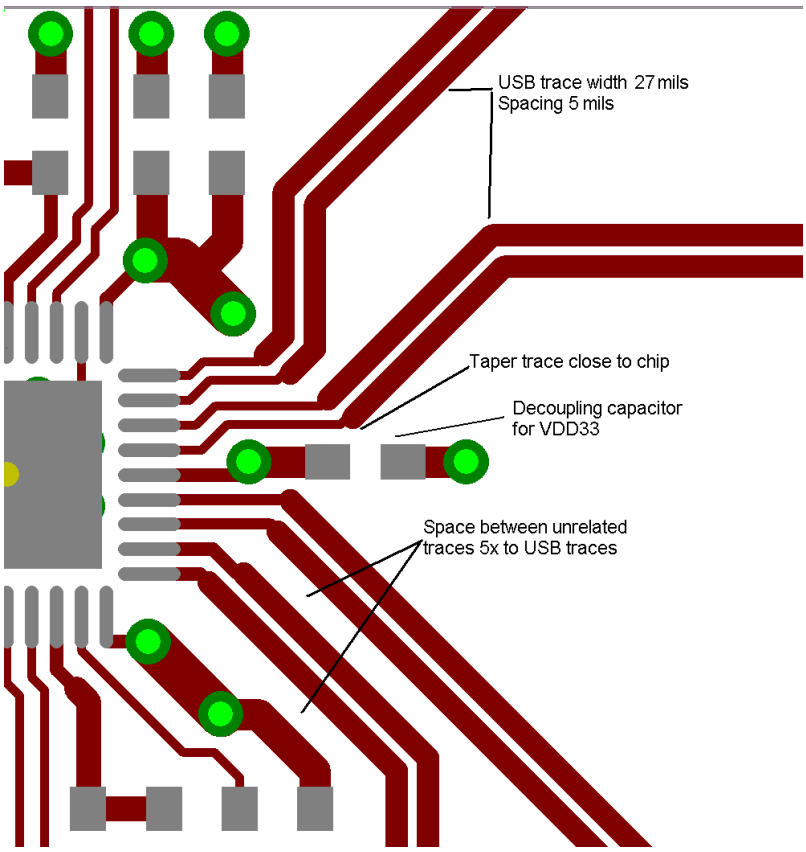

Figure 3 USB DP/DM Traces to Upstream and Downstream Ports (top copper layer)

Shield

For self-powered hubs with isolated main power supplies the shield on downstream USB connectors is tied to the upstream USB port shield. The shield is isolated from the signal ground. A wide trace on the periphery away from other signals should connect the down stream port's shield with the upstream port's shield. This is important to minimize effects from ESD immunity events. If the main power supply is earth grounded for a self-powered hub, connect the shield as a separate trace to a single earth ground point near the entry point for the power supply on the board.

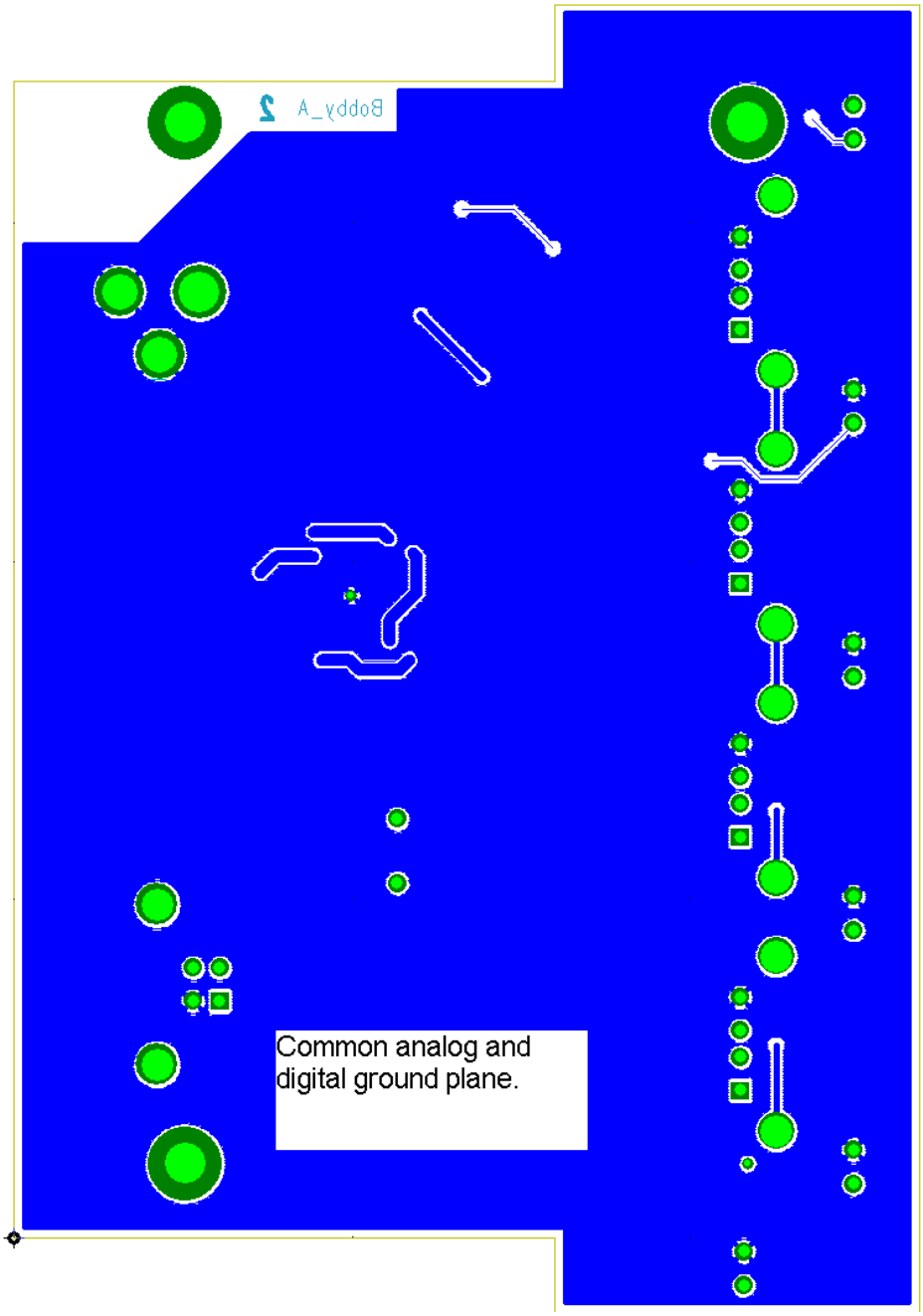

Figure 4 Bottom Layer Copper: Common Analog and Digital Ground

VBUS Supply

Downstream ports supply power to plugged-in devices. For self-powered hubs the maximum current per port is limited to 500 mA. This design is self-powered with four downstream ports that have individual over current protection port power switches. The maximum current from the supply to the downstream ports is 2A. The power supply connects on J6 in the upper left hand corner in Figure 2 on page 3. The two port power controller devices are adjacent to the 3.3 V regulator and power connector J6. Each +5 V VBUS trace is distributed along the periphery to the down stream ports.

There are two USB-IF tests directly targeting board layout and circuit design that should be considered. The first test is the drop test, which measures the VBUS voltage under full load on all downstream ports. This test requires that the voltage drop from the main supply is limited. Therefore traces carrying

VBUS power must be wide and short to minimize the IR drop under full load. The second test is the droop test, which measures the effect when a device is first plugged in while all other ports are fully loaded. A 10 µF capacitive load in parallel with a 50 Ω resistive load emulates the device in this test. The momentary droop in voltage on the loaded ports has to be minimized by minimizing charge sharing from one port to the other. Make supply and return paths wide and short, and consider using thicker copper on the PCB (>= 1.5 oz.), to lower instantaneous voltage drops. Fan out the supply traces from on board bulk capacitors to each downstream port in such a way to minimize the impact of each port's effect on the other.

Crystal Oscillator

The crystal oscillator is sensitive to stray capacitances and noise from other signals. It can also disturb other signals and cause EMI noise. The load capacitors, crystal and parallel resistors should be placed close to each other. The ground connection for the load capacitors should be short and out of the way from return currents from USB, VBUS and digital logic power supply.

Figure 5 on page 6 shows the crystal circuit consisting of the crystal Y1, load capacitors C9 and C14 and parallel resistor R10. All four components are moved away from USB traces. The bottom side is solid ground under this circuit and no other traces are adjacent to the main X1 and X2 signals.

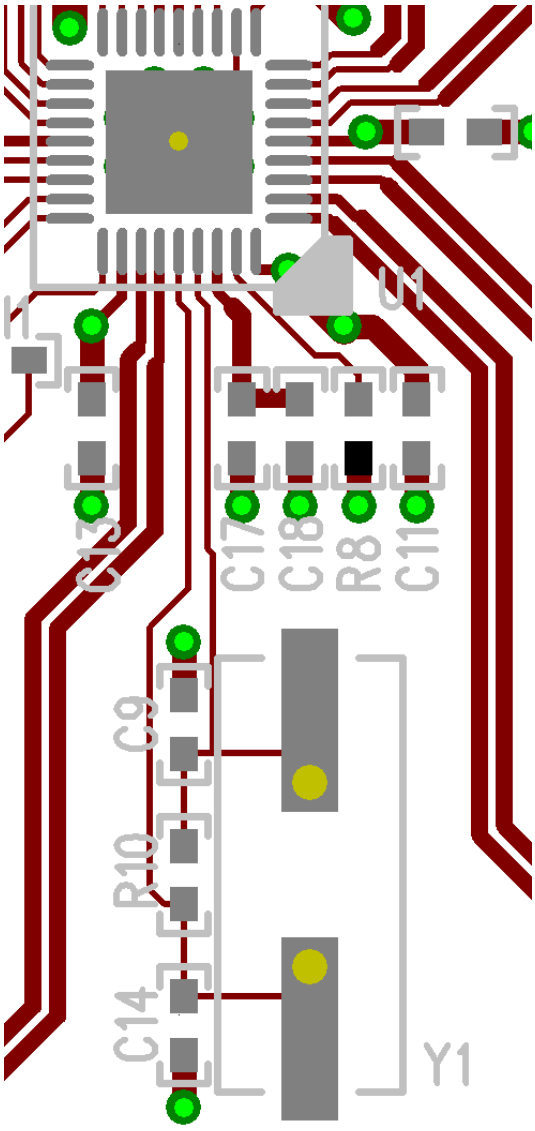

Figure 5 Detail of Crystal, Load Capacitors C9, C14, Parallel Resistor R10, and RBIAS R8

RBIAS

The RBIAS resistor provides the external reference for DC levels internal to the device. Any noise induced on the RBIAS traces directly impacts internal references and eye-diagram quality. The RBIAS resistor should be placed very close to RBIAS (pin 35) and the ground return should be short and close to the USB2514. Traces for RBIAS should be very short, direct, and five times the trace width away from any other traces if possible, especially the XTALIN and XTALOUT crystal circuit traces. Figure 5 shows the RBIAS connection with the ground connection near the USB2514.

Bypass Capacitors

This example has bypass capacitors for the HUB placed on the top side of the board as shown in Figure 6, "Detail of Top Side Decoupling Capacitors". There is a tradeoff in cost by requiring two-pass assembly versus board space. In this example board space is dictated by the space required for USB connectors so there is space to put all components on one side allowing for single pass assembly. Bypass capacitors should be placed close to the supply pins of the USB2514 with short and wide traces. Critical capacitors in the sample design are C17/C18 for PLLFILT, C15/C16 for CRFILT, and C10/C11/C12/C13 for VDD33.

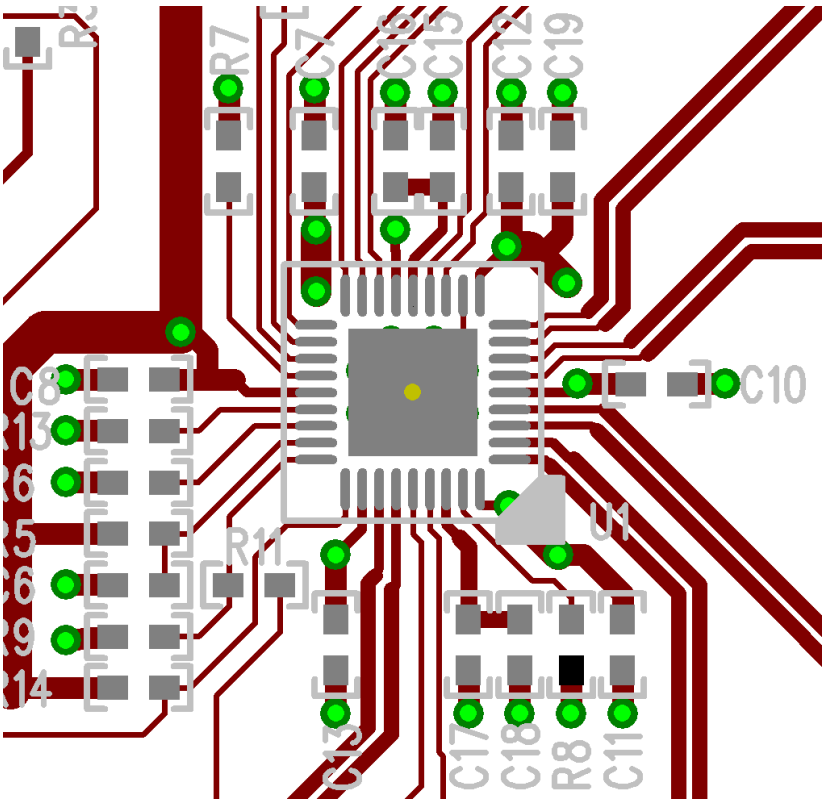

Figure 6 Detail of Top Side Decoupling Capacitors

Application Note Revision History

Table 1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Revision 1.0 (10-13-11)	"Two Layer PCB"	Replaced EVB-USB2514QFN 36 schematic in document with link to schematic on SMSC website.

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI