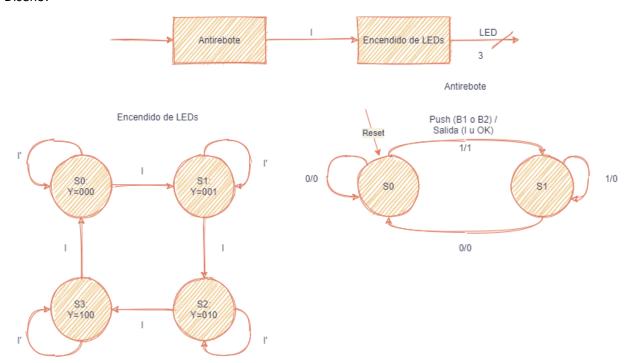
# Laboratorio 7

Electrónica Digital

Carné: 19072

Ejercicio 1:

Diseño:



## Transición de Estados:

S1	SO	I	SN2	SN2
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

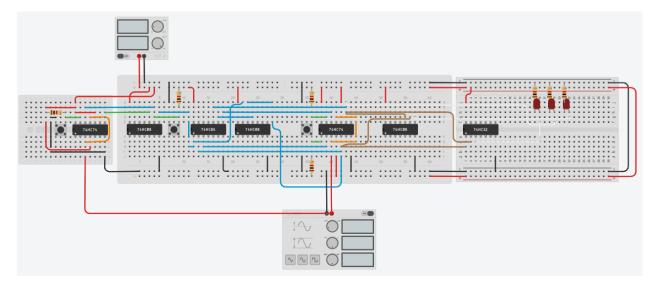
S1	S0	1	=>	SN1	SN2	Imported from file:
1	0	Χ		1		SN1 = S1' S0 I + S1 S0' I' + S1 S0' I + S1 S0 I';
1	X	0		1		SN2 = S1' S0' I + S1' S0 I' + S1 S0' I + S1 S0 I';
0	1	1		1		
X	0	1			1	Minimized:
X	1	0			1	SN1 = S1 S0' + S1 I' + S1' S0 I;
						SN2 = S0' I + S0 I';

#### Salidas:

S1	SO	L2	L1	L0
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

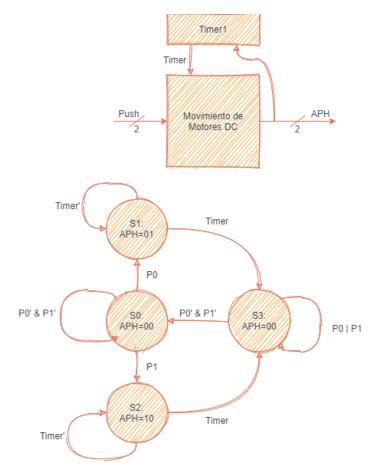
```
Imported from file:
SN1 = S1' S0 I + S1 S0' I' + S1 S0' I + S1 S0 I';
SN2 = S1' S0' I + S1' S0 I' + S1 S0' I + S1 S0 I';
Minimized:
SN1 = S1 S0' + S1 I' + S1' S0 I;
SN2 = S0' I + S0 I';
```

## Implementación:



# Ejercicio 2:

# Diseño:



## Transición de Estados:

<b>S1</b>	S0	P1	P0	TIMER	SN1	SN0
0	0	0	0	Χ	0	0
0	0	0	1	Χ	0	1
0	0	1	0	Χ	1	0
0	0	1	1	Χ	0	0
0	1	Χ	Χ	0	0	1
0	1	Χ	Χ	1	1	1
1	0	Χ	Χ	0	1	0
1	0	Χ	Χ	1	1	1
1	1	0	0	Χ	0	0
1	1	1	0	Χ	1	1
1	1	0	1	Χ	1	1
1	1	1	1	Χ	1	1

SO P1 P0' TIMER + S1' S0 P1 P0 TIMER + S1 S0' P1' P0' TIMER' + S1 S0' P1' P0' TIMER + S1 S0' P1' P0

TIMER' + S1 S0' P1' P0 TIMER + S1 S0' P1 P0' TIMER' + S1 S0' P1 P0' TIMER + S1 S0' P1 P0 TIMER' + S1

S0' P1 P0 TIMER + S1 S0 P1' P0 TIMER' + S1 S0 P1' P0 TIMER + S1 S0 P1 P0' TIMER' + S1 S0 P1 P0' TIMER

+ S1 S0 P1 P0 TIMER' + S1 S0 P1 P0 TIMER;

SNO = S1' S0' P1' P0 TIMER' + S1' S0' P1' P0 TIMER + S1' S0 P1' P0' TIMER' + S1' S0 P1' P0' TIMER +

SNO = S1' S0' P1' P0 TIMER' + S1' S0' P1' P0 TIMER + S1' S0 P1' P0' TIMER' + S1' S0 P1' P0' TIMER + S1' S0 P1' P0 TIMER' + S1' S0 P1' P0 TIMER + S1' S0 P1 P0' TIMER' + S1' S0 P1 P0' TIMER + S1' S0 P1 P0' TIMER + S1' S0 P1 P0' TIMER + S1 S0' P1' P0 TIMER + S1 S0' P1 P0' TIMER + S1 S0 P1 P0' TIMER + S1 S0 P1 P0' TIMER + S1 S0 P1 P0' TIMER' + S1 S0 P1 P

```
Minimized:

SN1 = S1 S0' + S1 P1 + S1 P0 + S0' P1 P0' + S1' S0 TIMER;

SN0 = S1' S0 + S0 P1 + S0 P0 + S1' P1' P0 + S1 S0' TIMER;
```

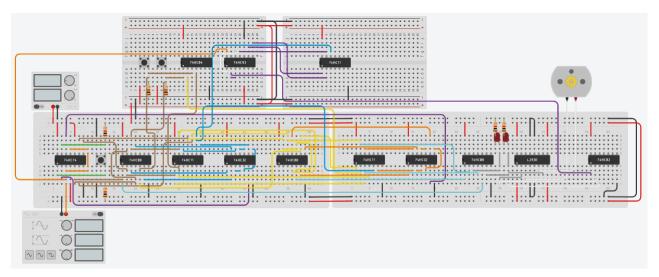
#### Salidas:

S1	S0	APH1	APH0
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

```
Imported from file:
APH1 = S1 S0';
APH0 = S1' S0;

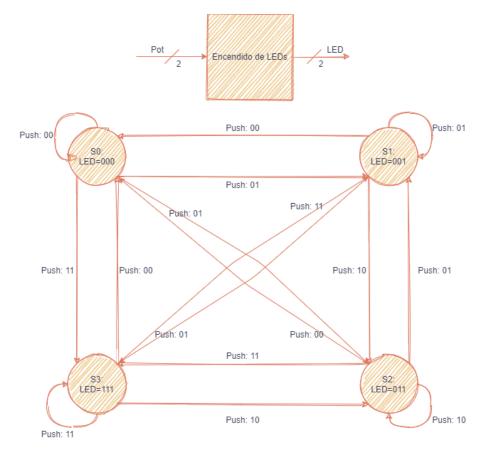
Minimized:
APH1 = S1 S0';
APH0 = S1' S0;
```

## Implementación:



# Ejercicio 3:

# Diseño:



# Transición de Estados:

S1	S0	P1	P0	SN1	SN0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	1	1

### Salidas:

S1	SO SO	L2	L1	LO
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

S1	S0	=>	L2	L1	L0	Imp	or	tec	l fr	om	fi	le:			
1	1		1			L2	=	Sl	S0;						
1	X			1		Ll	=	Sl	S0'	+	Sl	S0;			
1	Χ				1	LO	=	S1'	S	+	Sl	S0'	+	Sl	S0;
X	1				1										
						Mir	nin	nize	ed:						
						L2	=	Sl	S0;						
						Ll	=	Sl	;						
						LO	=	Sl	+	S0;	;				

## Implementación:

