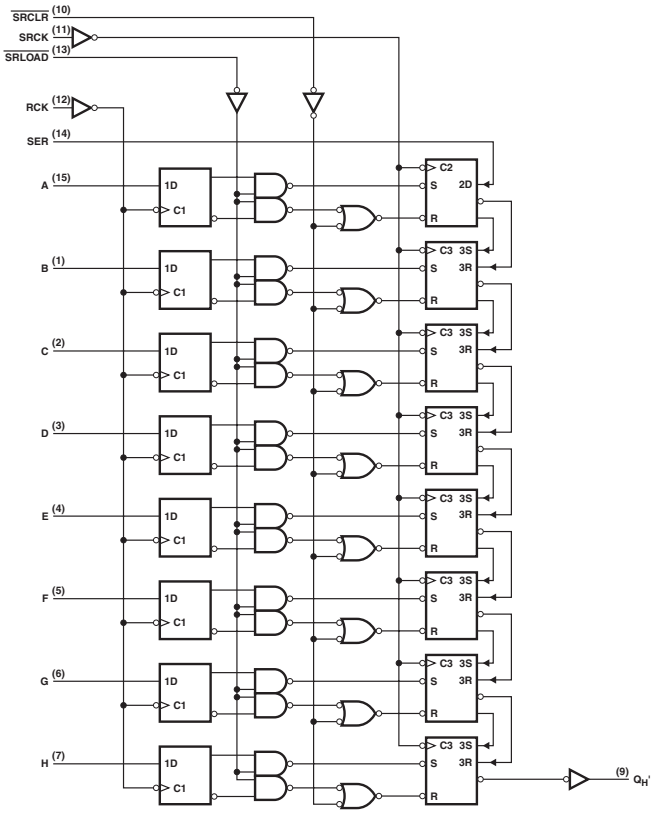
597

SERIAL-OUT SHIFT REGISTERS WITH INPUT LATCHES

- 8-Bit Parallel Storage Registers Inputs
- Shift Register Has Direct Overriding Load and Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram (SN74LS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	53	0.16	0.16	mA
I_{OH}	MAX	-1	-4	-4	mA
I_{OL}	MAX	16	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
f_{max}	SRCK	Q	MIN	20	-	-
	SRCK	QH'	MIN	20	-	-
	SH_{CP}		MIN	-	20	16
t_w	SRCK high		MIN	15	-	-
	SRCK low		MIN	35	-	-
	RCK		MIN	20	-	-
	$\overline{SRCLR}$		MIN	20	-	-
	$\overline{SRLOAD}$		MIN	40	-	-
	SH_{CP}		MIN	-	20	30
	ST_{CP}		MIN	-	15	20
	$\overline{MR}$		MIN	-	20	27
	$\overline{PL}$		MIN	-	18	24
t_{su}	Data before RCK ↑		MIN	20	-	-
	$\overline{SRCLR}$ inactive beforeSRCK ↑		MIN	25	-	-
	$\overline{SRLOAD}$ inactive before SRCK ↑		MIN	30	-	-
	RCK ↑ brfore SRLOAD ↑		MIN	40	-	-
	SER before SRCK ↑		MIN	20	-	-
	ST_{CP} to SH_{CP}		MIN	-	30	36
	D_s to SH_{CP}		MIN	-	15	15
	D_n to ST_{CP}		MIN	-	15	15
t_h	LS597 only		MIN	0	-	-
	ST_{CP} to SH_{CP}			-	0	0
	D_s to SH_{CP}			-	3	3
	D_n to ST_{CP}			-	3	3
t_{PLH}	SRCK ↑	QH'	MAX	23	-	-
t_{PHL}				23	-	-
t_{PLH}	$\overline{SRLOAD}$ ↓	QH'	MAX	57	-	-
t_{PHL}				44	-	-
t_{PHL}	$\overline{SRCLR}$ ↓	QH'	MAX	36	-	-
t_{PLH}	RCK ↑	QH'	MAX	60	-	-
t_{PHL}				48	-	-
t_{PLH}	SH_{CP}	Q7	MAX	-	53	57
t_{PHL}				-	53	57
t_{PLH}	$\overline{PL}$	Q7	MAX	-	60	72
t_{PHL}				-	60	72
t_{PLH}	ST_{CP}	Q7	MAX	-	72	84
t_{PHL}				-	72	84
t_{PLH}	$\overline{MR}$	Q7	MAX	-	53	66
t_{PHL}				-	53	66

UNIT f_{max} : MHz, other : ns