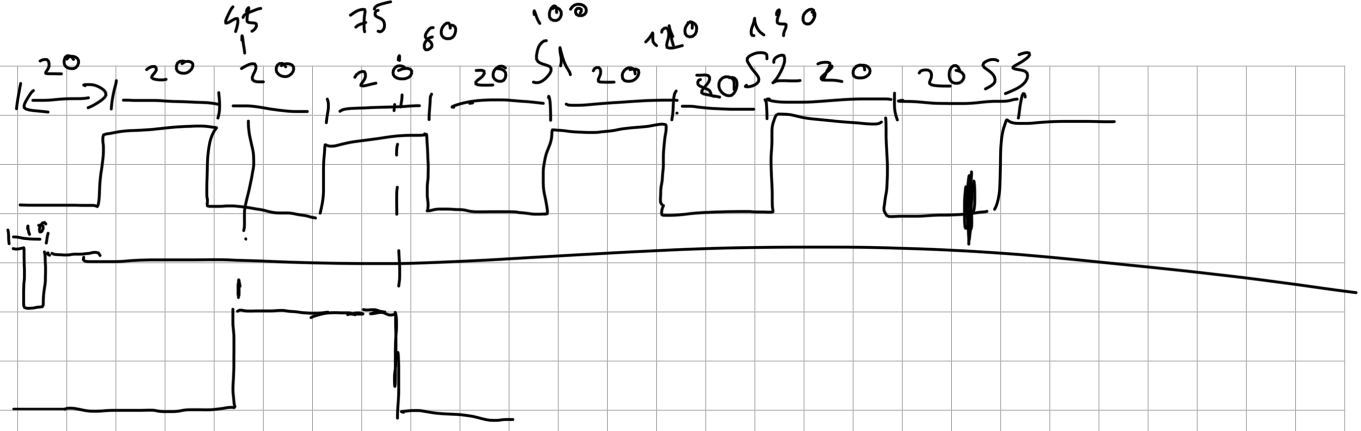


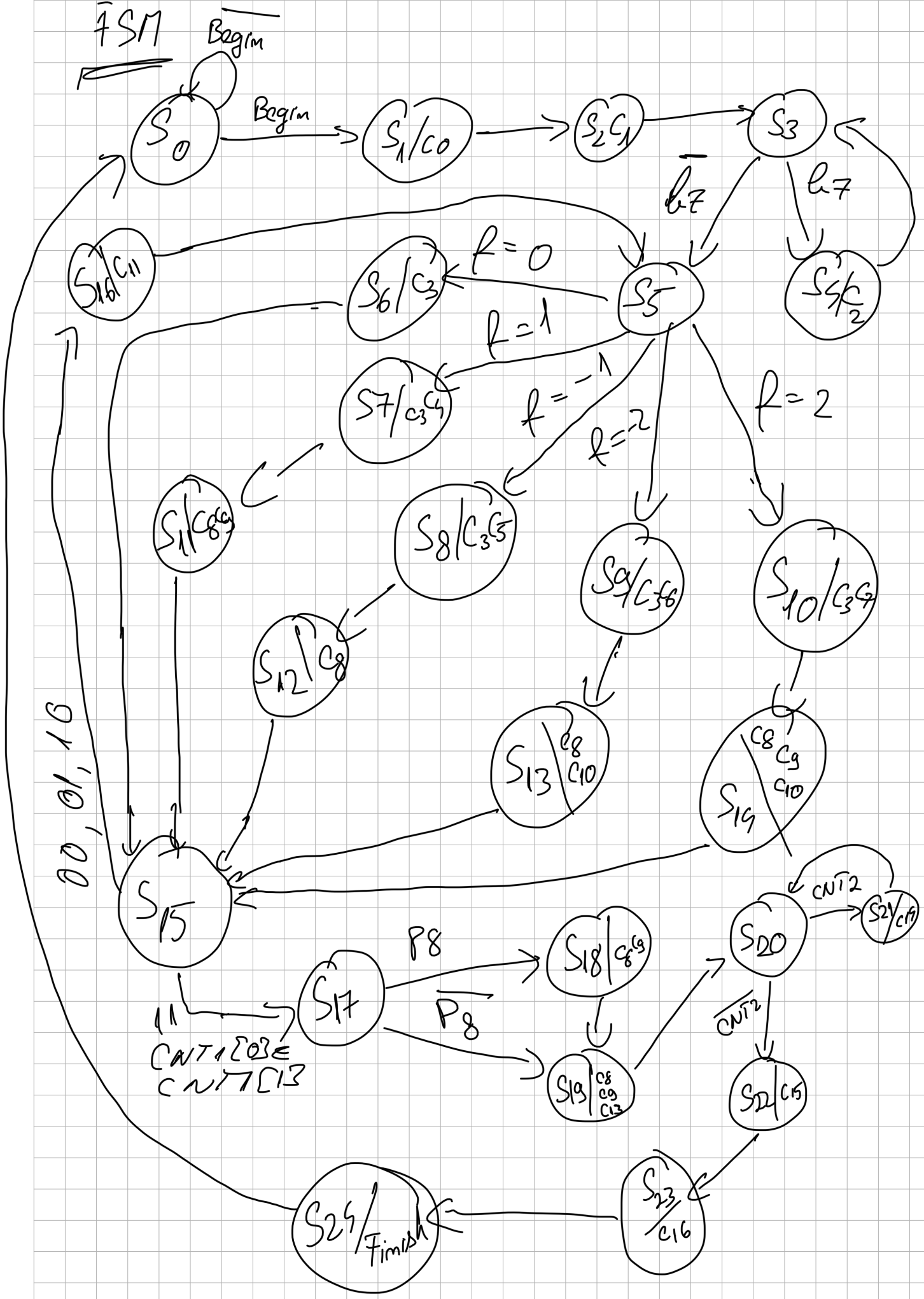
−12

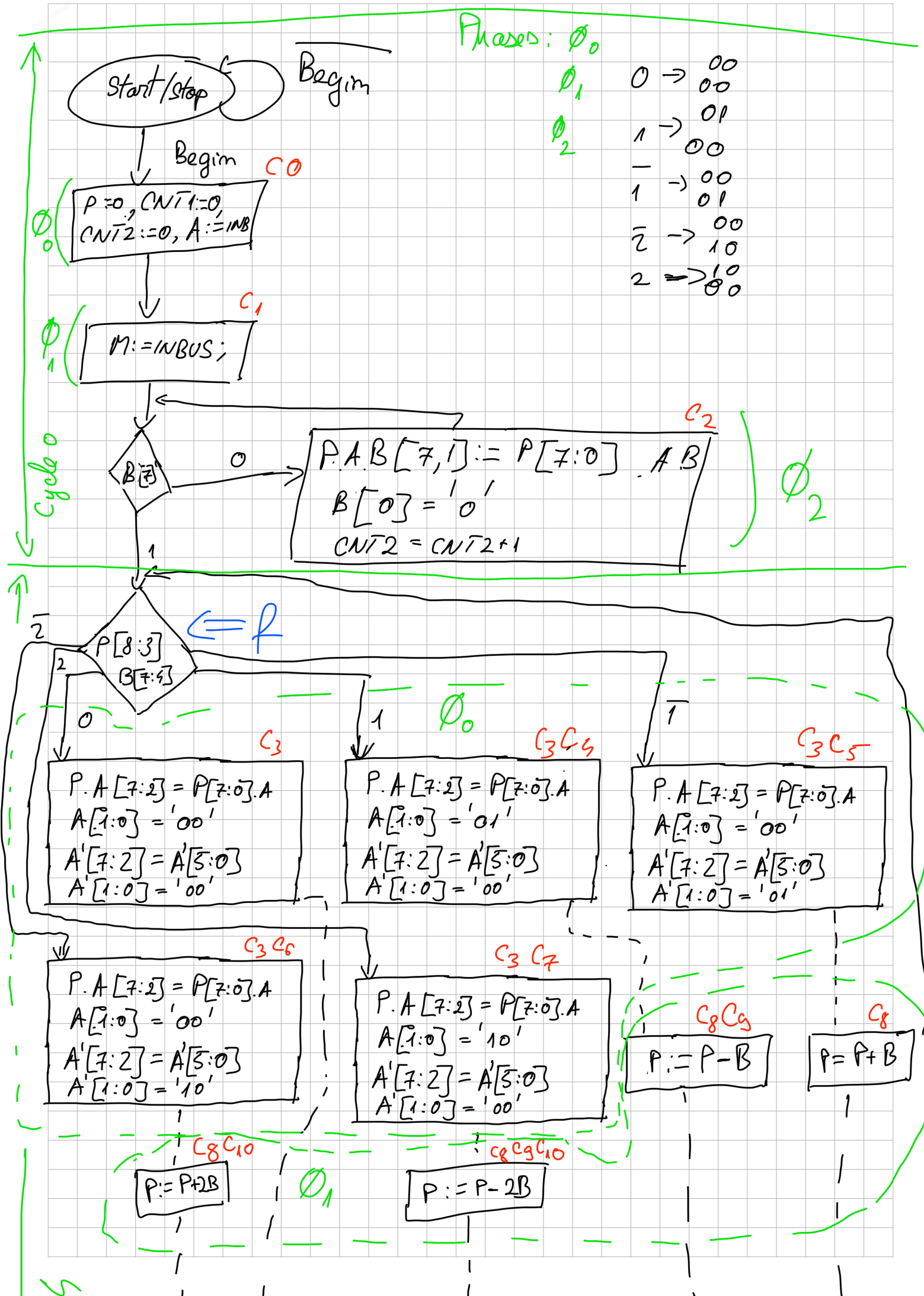
1

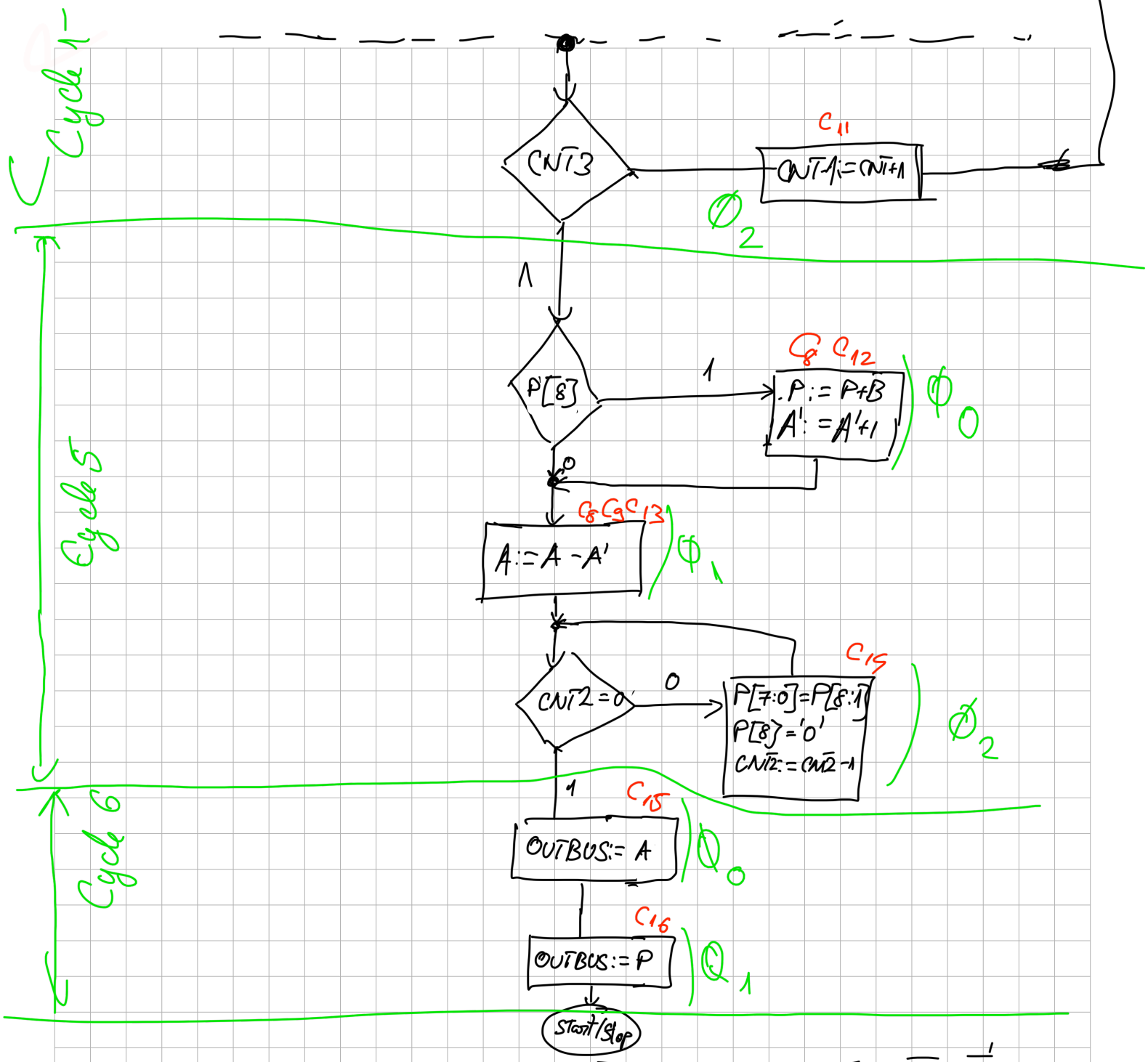
01100

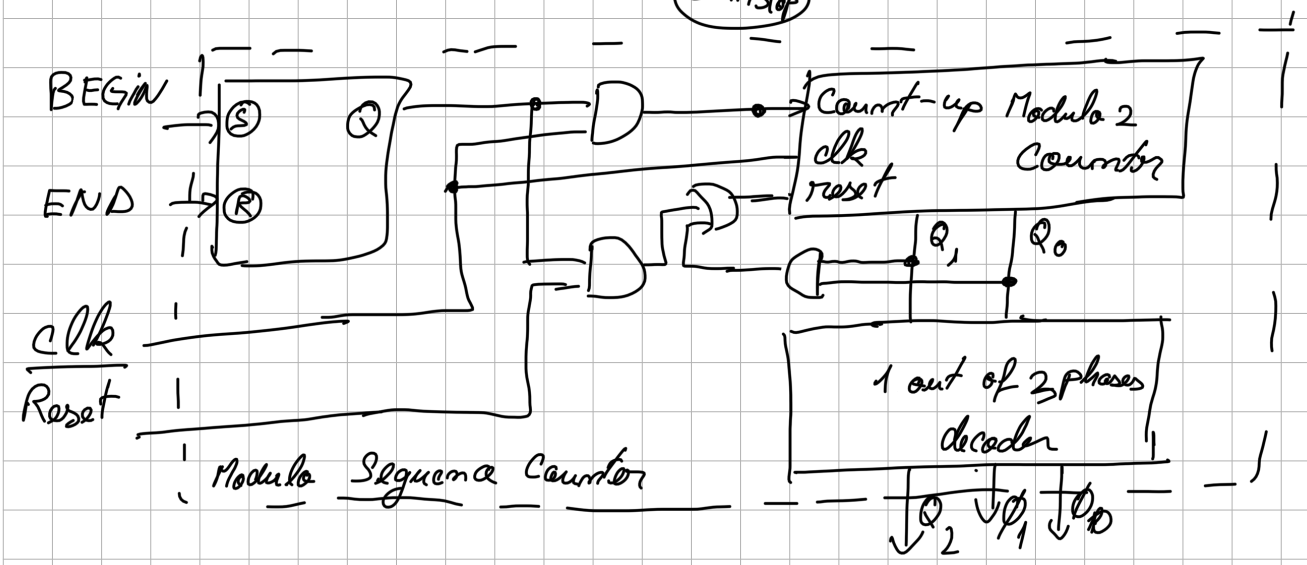
10100

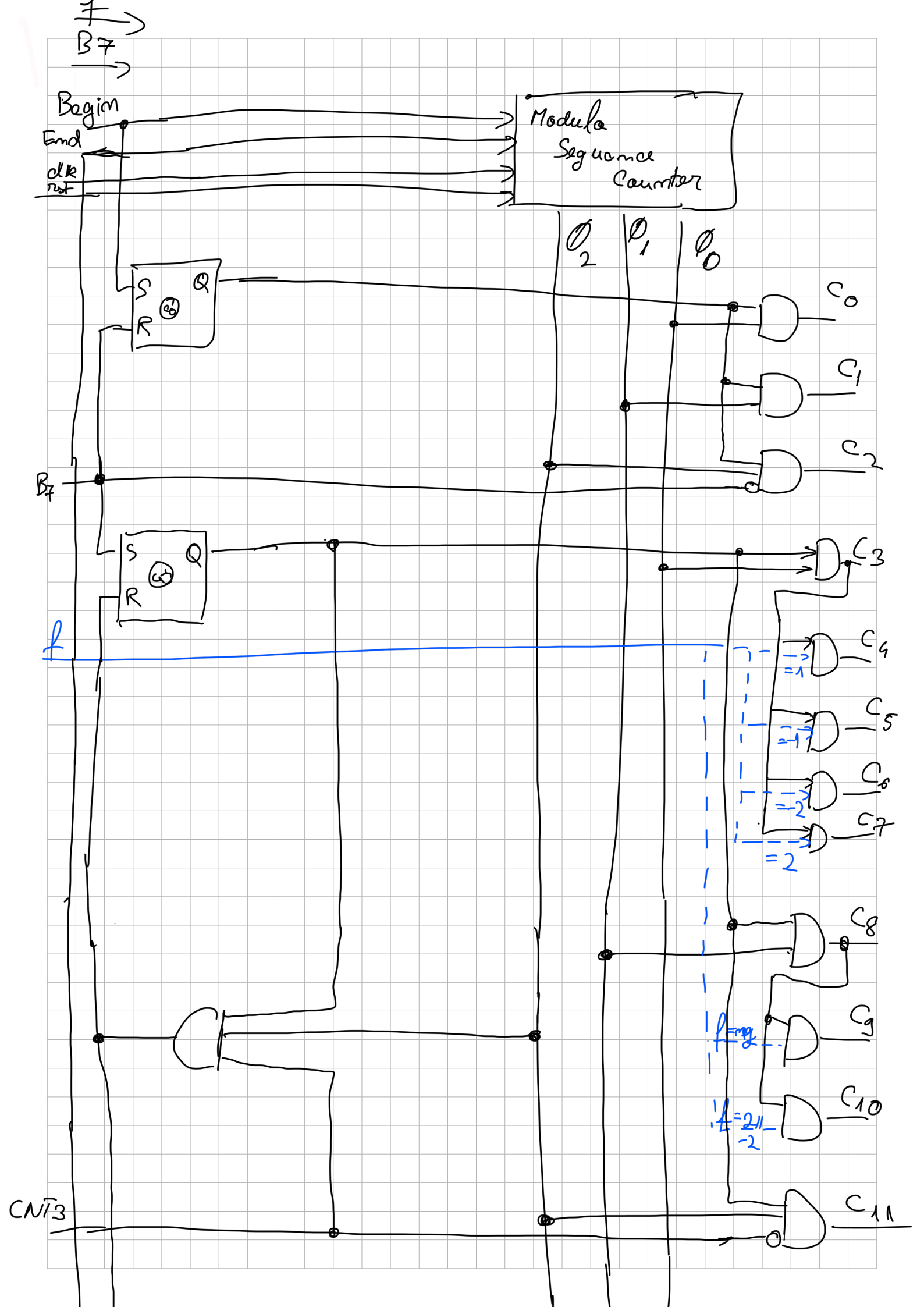
FSM

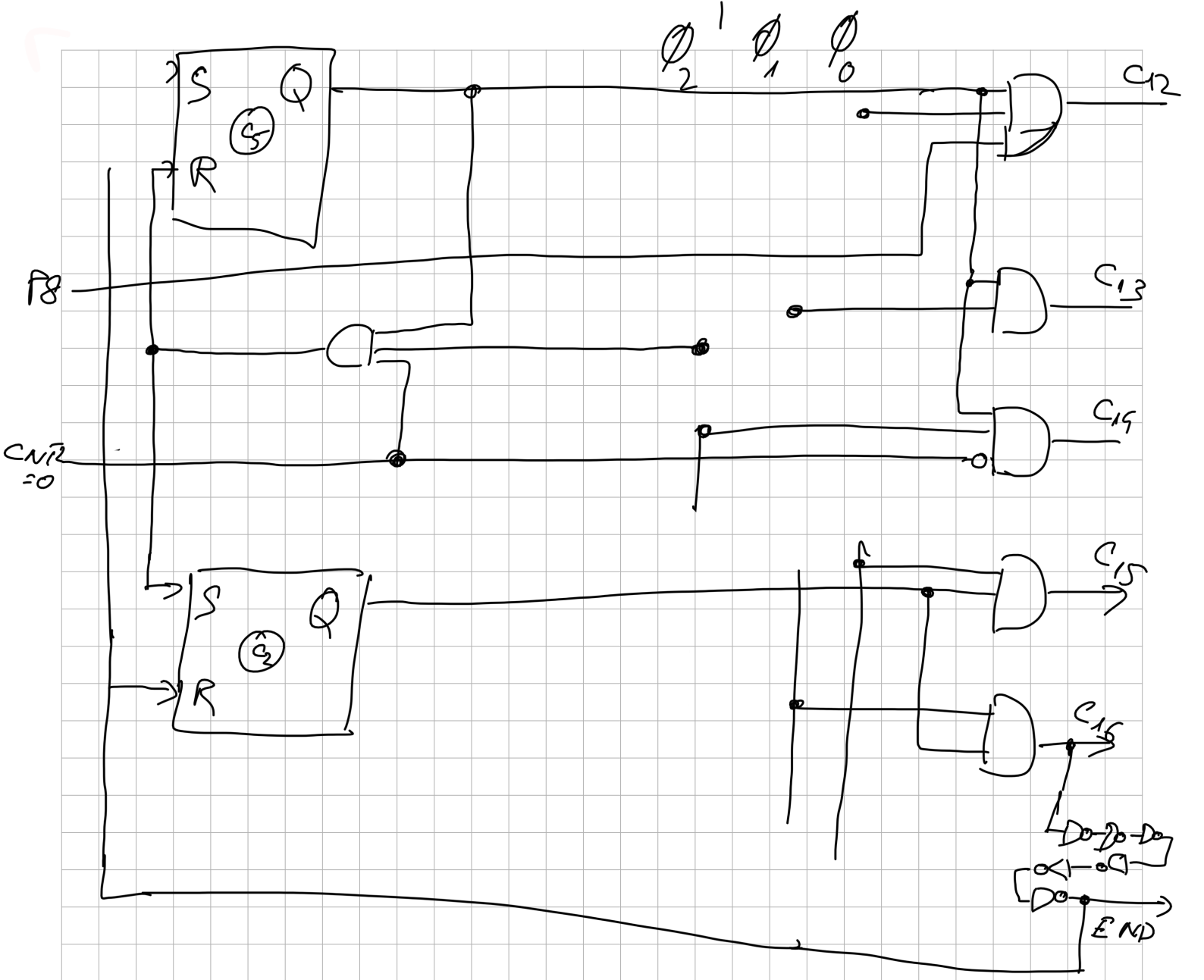

Begin
Begin
S0
S1/C0
S2 C1
S3
b7
b7
S4/C2
S5
S6/C3
f=0
f=1
f=-1
f=-2
f=2
S7/C3C4
S8/C3C5
S9/C3C6
S10/C3C7
S11/C8C9
S12/C8
S13/C8 C10
S14/C8 C9 C10
S15
00, 01, 10
11
CNT1[03]=
CNT1[13]
S16/C11
S17
P8
P8
S18/C8C9
S19/C8 C9 C13
S20
CNT2
S21/C15
CNT2
S22/C15
S23/C16
S24/Finish


Phases: $\emptyset_0$
$\emptyset_1$
$\emptyset_2$
0 → 00 00
1 → 01 00
$\bar{1}$ → 00 01
$\bar{2}$ → 00 10
2 → 10 00
Start/Stop
Begin
Begin
C0
P:=0, CNT1:=0, CNT2:=0, A:=INB
$\emptyset_0$
C1
M:=INBUS;
$\emptyset_1$
B[7]
0
1
C2
P.A.B[7,1]:= P[7:0] . A B
B[0] = '0'
CNT2 = CNT2+1
$\emptyset_2$
Cycle 0
P[8:3]
B[7:5]
$\bar{2}$
2
0
1
$\bar{1}$
$\emptyset_0$
C3
P.A[7:2] = P[7:0].A
A[1:0] = '00'
A'[7:2] = A'[5:0]
A'[1:0] = '00'
C3C4
P.A[7:2] = P[7:0].A
A[1:0] = '01'
A'[7:2] = A'[5:0]
A'[1:0] = '00'
C3C5
P.A[7:2] = P[7:0].A
A[1:0] = '00'
A'[7:2] = A'[5:0]
A'[1:0] = '01'
C3C6
P.A[7:2] = P[7:0].A
A[1:0] = '00'
A'[7:2] = A'[5:0]
A'[1:0] = '10'
C3C7
P.A[7:2] = P[7:0].A
A[1:0] = '10'
A'[7:2] = A'[5:0]
A'[1:0] = '00'
C8C9
P:= P-B
C8
P= P+B
C8C10
P:= P+2B
$\emptyset_1$
C8C9C10
P:= P-2B


Cycle 1
CNT3
C11
CNT1:=CNT1+1
Φ2
1
P[8]
1
C8 C12
P:=P+B
A':=A'+1
Φ0
0
Cycle 5
C8 C9 C13
A:=A-A'
Φ1
CNT2=0
0
C15
P[7:0]=P[8:1]
P[8]='0'
CNT2:=CNT2-1
Φ2
1
Cycle 6
C15
OUTBUS:=A
Φ0
C16
OUTBUS:=P
Φ1
Start/Stop


BEGIN
END
S
R
Q
clk
Reset
Count-up Modulo 2 Counter
clk
reset
Q1
Q0
1 out of 3 phases decoder
Φ2
Φ1
Φ0
Modulo Sequence Counter


f
B7
Begin
End
clk
rst
Modulo Sequence Counter
$\emptyset_2$
$\emptyset_1$
$\emptyset_0$
S
Q
R
C_0
C_1
C_2
B_7
C_3
C_4
C_5
C_6
C_7
=1
=1
=2
=2
C_8
C_9
C_{10}
C_{11}
CNT3


S
Q
R
S
R
Q
ϕ_2
ϕ_1
ϕ_0
C12
C13
C14
C15
C16
P8
CNT2
=0
END