

# Sexto Pré-Relatório

Pedro Henrique Luz de Araujo, 170043452, 5 de outubro de 2018

## Visto 1

### VHDL

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity jklatch is
    Port ( PR : in  STD_LOGIC;
          CLR : in  STD_LOGIC;
          CLK : in  STD_LOGIC;
          J   : in  STD_LOGIC;
          K   : in  STD_LOGIC;
          Q   : out STD_LOGIC);
end jklatch;

architecture Behavioral of jklatch is
    signal JK : STD_LOGIC_VECTOR(1 downto 0);
    signal Qbuf : STD_LOGIC;
begin
    JK <= J & K;

    process(PR, CLR, CLK)
    begin
```

```

    if PR = '1' then Qbuf <= '1';
    elsif CLR = '1' then Qbuf <= '0';
    elsif rising_edge(CLK) then
        case JK is
            WHEN "00" => Qbuf <= Qbuf;
            WHEN "01" => Qbuf <= '0';
            WHEN "10" => Qbuf <= '1';
            WHEN "11" => Qbuf <= not(Qbuf);
            WHEN others => Qbuf <= Qbuf;
        end case;
    end if;
end process;
Q <= Qbuf;
end Behavioral;

```

## UCF

```

NET CLK CLOCK_DEDICATED_ROUTE = FALSE;
NET "PR" LOC = "G3";
NET "CLR" LOC = "B4";
NET "CLK" LOC = "K3";
NET "J" LOC = "L3";
NET "K" LOC = "P11";

NET "Q" LOC = "M5";

```

# Visto 2

## VHDL

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity shifter is
    Port ( CLK : in  STD_LOGIC;
          RST : in  STD_LOGIC;
          LOAD : in  STD_LOGIC;
          D : in  STD_LOGIC_VECTOR (3 downto 0);
          DIR : in  STD_LOGIC;
          L : in  STD_LOGIC;
          R : in  STD_LOGIC;
          Q : out STD_LOGIC_VECTOR (3 downto 0));
end shifter;

architecture Behavioral of shifter is
    signal Qbuf : STD_LOGIC_VECTOR(3 downto 0);
begin
    process(CLK)
    begin
        if RST = '1' then Qbuf <= "0000";
        elsif LOAD = '1' then Qbuf <= D;
        elsif rising_edge(CLK) then
            case DIR is
```

```

        WHEN '0' => Qbuf <= Qbuf(2 downto 0) & L;
        WHEN '1' => Qbuf <= R & Qbuf(3 downto 1);
        WHEN others => Qbuf <= Qbuf;

    end case;

end if;

end process;

Q <= Qbuf;

end Behavioral;

```

## UCF 1

```

NET CLK CLOCK_DEDICATED_ROUTE = FALSE;

NET "RST" LOC = "C11";
NET "LOAD" LOC = "G12";

NET "CLK" LOC = "N3";
NET "DIR" LOC = "E2";
NET "L" LOC = "F3";
NET "R" LOC = "G3";
NET "D<3>" LOC = "B4";
NET "D<2>" LOC = "K3";
NET "D<1>" LOC = "L3";
NET "D<0>" LOC = "P11";

```

```
NET "Q<3>" LOC = "P6";  
NET "Q<2>" LOC = "P7";  
NET "Q<1>" LOC = "M11";  
NET "Q<0>" LOC = "M5";
```