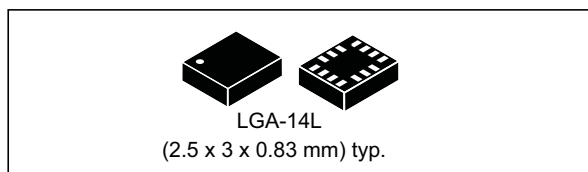


iNEMO inertial module: always-on 3D accelerometer and 3D gyroscope

Datasheet - production data



Features

- “Always-on” experience with low power consumption for both accelerometer and gyroscope
- Power consumption: 0.4 mA in combo normal mode and 0.65 mA in combo high-performance mode
- Smart FIFO up to 4 kbyte based on features set
- Android M compliant
- Auxiliary SPI for OIS data output for gyroscope and accelerometer
- Hard, soft ironing for external magnetic sensor corrections
- $\pm 2/\pm 4/\pm 8/\pm 16$ g full scale
- $\pm 125/\pm 250/\pm 500/\pm 1000/\pm 2000$ dps full scale
- Analog supply voltage: 1.71 V to 3.6 V
- SPI & I²C serial interface with main processor data synchronization
- Dedicated gyroscope low-pass filters for UI and OIS applications
- Smart embedded functions: pedometer, step detector and step counter, significant motion and tilt
- Standard interrupts: free-fall, wakeup, 6D/4D orientation, click and double-click
- Embedded temperature sensor
- ECOPACK[®], RoHS and “Green” compliant

Applications

- Motion tracking and gesture detection
- Sensor hub
- Indoor navigation
- IoT and connected devices
- Smart power saving for handheld devices
- EIS and OIS for camera applications
- Vibration monitoring and compensation

Description

The LSM6DSM is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope performing at 0.65 mA in high-performance mode and enabling always-on low-power features for an optimal motion experience for the consumer.

The LSM6DSM supports main OS requirements, offering real, virtual and batch sensors with 4 kbyte for dynamic data batching.

ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DSM has a full-scale acceleration range of $\pm 2/\pm 4/\pm 8/\pm 16$ g and an angular rate range of $\pm 125/\pm 250/\pm 500/\pm 1000/\pm 2000$ dps.

The LSM6DSM fully supports EIS and OIS applications as the module includes a dedicated configurable signal processing path for OIS and auxiliary SPI configurable for both the gyroscope and accelerometer.

High robustness to mechanical shock makes the LSM6DSM the preferred choice of system designers for the creation and manufacturing of reliable products.

The LSM6DSM is available in a plastic land grid array (LGA) package.

Table 1. Device summary

| Part number | Temp. range [°C] | Package | Packing |
|-------------|------------------|---------------------------|-------------|
| LSM6DSM | -40 to +85 | LGA-14L (2.5x3x0.83mm) | Tray |
| LSM6DSMTR | -40 to +85 | | Tape & Reel |

Contents

| | | |
|----------|---|-----------|
| 1 | Overview | 17 |
| 2 | Embedded low-power features | 18 |
| 2.1 | Tilt detection | 18 |
| 2.2 | Absolute wrist tilt | 19 |
| 3 | Pin description | 20 |
| 3.1 | Pin connections | 21 |
| 4 | Module specifications | 23 |
| 4.1 | Mechanical characteristics | 23 |
| 4.2 | Electrical characteristics | 26 |
| 4.3 | Temperature sensor characteristics | 27 |
| 4.4 | Communication interface characteristics | 28 |
| 4.4.1 | SPI - serial peripheral interface | 28 |
| 4.4.2 | I ² C - inter-IC control interface | 29 |
| 4.5 | Absolute maximum ratings | 31 |
| 4.6 | Terminology | 32 |
| 4.6.1 | Sensitivity | 32 |
| 4.6.2 | Zero-g and zero-rate level | 32 |
| 5 | Functionality | 33 |
| 5.1 | Operating modes | 33 |
| 5.2 | Gyroscope power modes | 33 |
| 5.3 | Accelerometer power modes | 33 |
| 5.4 | Block diagram of filters | 34 |
| 5.4.1 | Block diagrams of the gyroscope filters | 34 |
| 5.4.2 | Block diagrams of the accelerometer filters | 36 |
| 5.5 | FIFO | 38 |
| 5.5.1 | Bypass mode | 38 |
| 5.5.2 | FIFO mode | 39 |
| 5.5.3 | Continuous mode | 39 |
| 5.5.4 | Continuous-to-FIFO mode | 39 |

| | | | |
|-----------|-------|---|-----------|
| | 5.5.5 | Bypass-to-Continuous mode | 39 |
| | 5.5.6 | FIFO reading procedure | 40 |
| 6 | | Digital interfaces | 41 |
| | 6.1 | I ² C/SPI interface | 41 |
| | 6.2 | Master I ² C | 41 |
| | 6.3 | Auxiliary SPI | 42 |
| | 6.4 | I ² C serial interface | 42 |
| | 6.4.1 | I ² C operation | 42 |
| | 6.5 | SPI bus interface | 45 |
| | 6.5.1 | SPI read | 46 |
| | 6.5.2 | SPI write | 47 |
| | 6.5.3 | SPI read in 3-wire mode | 48 |
| 7 | | Application hints | 49 |
| | 7.1 | LSM6DSM electrical connections in Mode 1 | 49 |
| | 7.2 | LSM6DSM electrical connections in Mode 2 | 50 |
| | 7.3 | LSM6DSM electrical connections in Mode 3 and Mode 4 | 51 |
| 8 | | Auxiliary SPI configurations | 55 |
| | 8.1 | Gyroscope filtering | 55 |
| | 8.2 | Accelerometer filtering | 56 |
| | 8.2.1 | Accelerometer full scale set from primary interface | 56 |
| | 8.2.2 | Accelerometer full scale set from auxiliary SPI | 56 |
| 9 | | Register mapping | 57 |
| 10 | | Register description | 61 |
| | 10.1 | FUNC_CFG_ACCESS (01h) | 61 |
| | 10.2 | SENSOR_SYNC_TIME_FRAME (04h) | 61 |
| | 10.3 | SENSOR_SYNC_RES_RATIO (05h) | 62 |
| | 10.4 | FIFO_CTRL1 (06h) | 62 |
| | 10.5 | FIFO_CTRL2 (07h) | 63 |
| | 10.6 | FIFO_CTRL3 (08h) | 64 |
| | 10.7 | FIFO_CTRL4 (09h) | 65 |

| | | |
|-------|------------------------------------|----|
| 10.8 | FIFO_CTRL5 (0Ah) | 66 |
| 10.9 | DRDY_PULSE_CFG (0Bh) | 67 |
| 10.10 | INT1_CTRL (0Dh) | 67 |
| 10.11 | INT2_CTRL (0Eh) | 68 |
| 10.12 | WHO_AM_I (0Fh) | 68 |
| 10.13 | CTRL1_XL (10h) | 69 |
| 10.14 | CTRL2_G (11h) | 70 |
| 10.15 | CTRL3_C (12h) | 71 |
| 10.16 | CTRL4_C (13h) | 72 |
| 10.17 | CTRL5_C (14h) | 72 |
| 10.18 | CTRL6_C (15h) | 74 |
| 10.19 | CTRL7_G (16h) | 75 |
| 10.20 | CTRL8_XL (17h) | 75 |
| 10.21 | CTRL9_XL (18h) | 76 |
| 10.22 | CTRL10_C (19h) | 77 |
| 10.23 | MASTER_CONFIG (1Ah) | 77 |
| 10.24 | WAKE_UP_SRC (1Bh) | 78 |
| 10.25 | TAP_SRC (1Ch) | 79 |
| 10.26 | D6D_SRC (1Dh) | 79 |
| 10.27 | STATUS_REG/STATUS_SPIAux (1Eh) | 80 |
| 10.28 | OUT_TEMP_L (20h), OUT_TEMP_H (21h) | 80 |
| 10.29 | OUTX_L_G (22h) | 81 |
| 10.30 | OUTX_H_G (23h) | 81 |
| 10.31 | OUTY_L_G (24h) | 82 |
| 10.32 | OUTY_H_G (25h) | 82 |
| 10.33 | OUTZ_L_G (26h) | 83 |
| 10.34 | OUTZ_H_G (27h) | 83 |
| 10.35 | OUTX_L_XL (28h) | 84 |
| 10.36 | OUTX_H_XL (29h) | 84 |
| 10.37 | OUTY_L_XL (2Ah) | 84 |
| 10.38 | OUTY_H_XL (2Bh) | 85 |
| 10.39 | OUTZ_L_XL (2Ch) | 85 |
| 10.40 | OUTZ_H_XL (2Dh) | 85 |

| | | |
|-------|------------------------|----|
| 10.41 | SENSORHUB1_REG (2Eh) | 85 |
| 10.42 | SENSORHUB2_REG (2Fh) | 86 |
| 10.43 | SENSORHUB3_REG (30h) | 86 |
| 10.44 | SENSORHUB4_REG (31h) | 86 |
| 10.45 | SENSORHUB5_REG (32h) | 86 |
| 10.46 | SENSORHUB6_REG (33h) | 87 |
| 10.47 | SENSORHUB7_REG (34h) | 87 |
| 10.48 | SENSORHUB8_REG (35h) | 87 |
| 10.49 | SENSORHUB9_REG (36h) | 87 |
| 10.50 | SENSORHUB10_REG (37h) | 88 |
| 10.51 | SENSORHUB11_REG (38h) | 88 |
| 10.52 | SENSORHUB12_REG (39h) | 88 |
| 10.53 | FIFO_STATUS1 (3Ah) | 88 |
| 10.54 | FIFO_STATUS2 (3Bh) | 89 |
| 10.55 | FIFO_STATUS3 (3Ch) | 89 |
| 10.56 | FIFO_STATUS4 (3Dh) | 90 |
| 10.57 | FIFO_DATA_OUT_L (3Eh) | 90 |
| 10.58 | FIFO_DATA_OUT_H (3Fh) | 90 |
| 10.59 | TIMESTAMP0_REG (40h) | 91 |
| 10.60 | TIMESTAMP1_REG (41h) | 91 |
| 10.61 | TIMESTAMP2_REG (42h) | 91 |
| 10.62 | STEP_TIMESTAMP_L (49h) | 91 |
| 10.63 | STEP_TIMESTAMP_H (4Ah) | 92 |
| 10.64 | STEP_COUNTER_L (4Bh) | 92 |
| 10.65 | STEP_COUNTER_H (4Ch) | 92 |
| 10.66 | SENSORHUB13_REG (4Dh) | 92 |
| 10.67 | SENSORHUB14_REG (4Eh) | 93 |
| 10.68 | SENSORHUB15_REG (4Fh) | 93 |
| 10.69 | SENSORHUB16_REG (50h) | 93 |
| 10.70 | SENSORHUB17_REG (51h) | 93 |
| 10.71 | SENSORHUB18_REG (52h) | 94 |
| 10.72 | FUNC_SRC1 (53h) | 94 |
| 10.73 | FUNC_SRC2 (54h) | 95 |

| | | |
|-----------|--|------------|
| 10.74 | WRIST_TILT_IA (55h) | 95 |
| 10.75 | TAP_CFG (58h) | 96 |
| 10.76 | TAP_THS_6D (59h) | 97 |
| 10.77 | INT_DUR2 (5Ah) | 97 |
| 10.78 | WAKE_UP_THS (5Bh) | 98 |
| 10.79 | WAKE_UP_DUR (5Ch) | 98 |
| 10.80 | FREE_FALL (5Dh) | 99 |
| 10.81 | MD1_CFG (5Eh) | 100 |
| 10.82 | MD2_CFG (5Fh) | 101 |
| 10.83 | MASTER_CMD_CODE (60h) | 102 |
| 10.84 | SENS_SYNC_SPI_ERROR_CODE (61h) | 102 |
| 10.85 | OUT_MAG_RAW_X_L (66h) | 102 |
| 10.86 | OUT_MAG_RAW_X_H (67h) | 102 |
| 10.87 | OUT_MAG_RAW_Y_L (68h) | 103 |
| 10.88 | OUT_MAG_RAW_Y_H (69h) | 103 |
| 10.89 | OUT_MAG_RAW_Z_L (6Ah) | 103 |
| 10.90 | OUT_MAG_RAW_Z_H (6Bh) | 103 |
| 10.91 | INT_OIS (6Fh) | 104 |
| 10.92 | CTRL1_OIS (70h) | 104 |
| 10.93 | CTRL2_OIS (71h) | 105 |
| 10.94 | CTRL3_OIS (72h) | 106 |
| 10.95 | X_OFS_USR (73h) | 107 |
| 10.96 | Y_OFS_USR (74h) | 107 |
| 10.97 | Z_OFS_USR (75h) | 107 |
| 11 | Embedded functions register mapping | 108 |
| 12 | Embedded functions registers description - Bank A | 110 |
| 12.1 | SLV0_ADD (02h) | 110 |
| 12.2 | SLV0_SUBADD (03h) | 110 |
| 12.3 | SLAVE0_CONFIG (04h) | 110 |
| 12.4 | SLV1_ADD (05h) | 111 |
| 12.5 | SLV1_SUBADD (06h) | 111 |
| 12.6 | SLAVE1_CONFIG (07h) | 112 |

| | | |
|-----------|--|------------|
| 12.7 | SLV2_ADD (08h) | 112 |
| 12.8 | SLV2_SUBADD (09h) | 112 |
| 12.9 | SLAVE2_CONFIG (0Ah) | 113 |
| 12.10 | SLV3_ADD (0Bh) | 113 |
| 12.11 | SLV3_SUBADD (0Ch) | 113 |
| 12.12 | SLAVE3_CONFIG (0Dh) | 114 |
| 12.13 | DATAWRITE_SRC_MODE_SUB_SLV0 (0Eh) | 114 |
| 12.14 | CONFIG_PEDO_THS_MIN (0Fh) | 114 |
| 12.15 | SM_THS (13h) | 115 |
| 12.16 | PEDO_DEB_REG (14h) | 115 |
| 12.17 | STEP_COUNT_DELTA (15h) | 115 |
| 12.18 | MAG_SI_XX (24h) | 116 |
| 12.19 | MAG_SI_XY (25h) | 116 |
| 12.20 | MAG_SI_XZ (26h) | 116 |
| 12.21 | MAG_SI_YX (27h) | 116 |
| 12.22 | MAG_SI_YY (28h) | 117 |
| 12.23 | MAG_SI_YZ (29h) | 117 |
| 12.24 | MAG_SI_ZX (2Ah) | 117 |
| 12.25 | MAG_SI_ZY (2Bh) | 117 |
| 12.26 | MAG_SI_ZZ (2Ch) | 118 |
| 12.27 | MAG_OFFX_L (2Dh) | 118 |
| 12.28 | MAG_OFFX_H (2Eh) | 118 |
| 12.29 | MAG_OFFY_L (2Fh) | 118 |
| 12.30 | MAG_OFFY_H (30h) | 119 |
| 12.31 | MAG_OFFZ_L (31h) | 119 |
| 12.32 | MAG_OFFZ_H (32h) | 119 |
| 13 | Embedded functions registers description - Bank B | 120 |
| 13.1 | A_WRIST_TILT_LAT (50h) | 120 |
| 13.2 | A_WRIST_TILT_THS (54h) | 120 |
| 13.3 | A_WRIST_TILT_Mask (59h) | 120 |
| 14 | Soldering information | 121 |

| | | |
|-----------|--|------------|
| 15 | Package information | 122 |
| | 15.1 LGA-14L package information | 122 |
| | 15.2 LGA-14 packing information | 123 |
| 16 | Revision history | 125 |



List of tables

| | | |
|-----------|---|----|
| Table 1. | Device summary | 1 |
| Table 2. | Pin description | 22 |
| Table 3. | Mechanical characteristics | 23 |
| Table 4. | Electrical characteristics | 26 |
| Table 5. | Temperature sensor characteristics | 27 |
| Table 6. | SPI slave timing values (in mode 3) | 28 |
| Table 7. | I ² C slave timing values | 29 |
| Table 8. | I ² C master timing values | 30 |
| Table 9. | Absolute maximum ratings | 31 |
| Table 10. | Serial interface pin description | 41 |
| Table 11. | Master I ² C pin details | 41 |
| Table 12. | Auxiliary SPI pin details | 42 |
| Table 13. | I ² C terminology | 42 |
| Table 14. | SAD+Read/Write patterns | 43 |
| Table 15. | Transfer when master is writing one byte to slave | 43 |
| Table 16. | Transfer when master is writing multiple bytes to slave | 43 |
| Table 17. | Transfer when master is receiving (reading) one byte of data from slave | 43 |
| Table 18. | Transfer when master is receiving (reading) multiple bytes of data from slave | 43 |
| Table 19. | Internal pin status | 53 |
| Table 20. | Registers address map | 57 |
| Table 21. | FUNC_CFG_ACCESS register | 61 |
| Table 22. | FUNC_CFG_ACCESS register description | 61 |
| Table 23. | Configuration of embedded functions register banks | 61 |
| Table 24. | SENSOR_SYNC_TIME_FRAME register | 61 |
| Table 25. | SENSOR_SYNC_TIME_FRAME register description | 61 |
| Table 26. | SENSOR_SYNC_RES_RATIO register | 62 |
| Table 27. | SENSOR_SYNC_RES_RATIO register description | 62 |
| Table 28. | FIFO_CTRL1 register | 62 |
| Table 29. | FIFO_CTRL1 register description | 62 |
| Table 30. | FIFO_CTRL2 register | 63 |
| Table 31. | FIFO_CTRL2 register description | 63 |
| Table 32. | FIFO_CTRL3 register | 64 |
| Table 33. | FIFO_CTRL3 register description | 64 |
| Table 34. | Gyro FIFO decimation setting | 64 |
| Table 35. | Accelerometer FIFO decimation setting | 64 |
| Table 36. | FIFO_CTRL4 register | 65 |
| Table 37. | FIFO_CTRL4 register description | 65 |
| Table 38. | Fourth FIFO data set decimation setting | 65 |
| Table 39. | Third FIFO data set decimation setting | 65 |
| Table 40. | FIFO_CTRL5 register | 66 |
| Table 41. | FIFO_CTRL5 register description | 66 |
| Table 42. | FIFO ODR selection | 66 |
| Table 43. | FIFO mode selection | 66 |
| Table 44. | DRDY_PULSE_CFG register | 67 |
| Table 45. | DRDY_PULSE_CFG register description | 67 |
| Table 46. | INT1_CTRL register | 67 |
| Table 47. | INT1_CTRL register description | 67 |
| Table 48. | INT2_CTRL register | 68 |

| | | |
|------------|---|----|
| Table 49. | INT2_CTRL register description | 68 |
| Table 50. | WHO_AM_I register | 68 |
| Table 51. | CTRL1_XL register | 69 |
| Table 52. | CTRL1_XL register description | 69 |
| Table 53. | Accelerometer ODR register setting | 69 |
| Table 54. | CTRL2_G register | 70 |
| Table 55. | CTRL2_G register description | 70 |
| Table 56. | Gyroscope ODR configuration setting | 70 |
| Table 57. | CTRL3_C register | 71 |
| Table 58. | CTRL3_C register description | 71 |
| Table 59. | CTRL4_C register | 72 |
| Table 60. | CTRL4_C register description | 72 |
| Table 61. | CTRL5_C register | 72 |
| Table 62. | CTRL5_C register description | 72 |
| Table 63. | Output registers rounding pattern | 73 |
| Table 64. | Angular rate sensor self-test mode selection | 73 |
| Table 65. | Linear acceleration sensor self-test mode selection | 73 |
| Table 66. | CTRL6_C register | 74 |
| Table 67. | CTRL6_C register description | 74 |
| Table 68. | Trigger mode selection | 74 |
| Table 69. | Gyroscope LPF1 bandwidth selection | 74 |
| Table 70. | CTRL7_G register | 75 |
| Table 71. | CTRL7_G register description | 75 |
| Table 72. | CTRL8_XL register | 75 |
| Table 73. | CTRL8_XL register description | 75 |
| Table 74. | Accelerometer bandwidth selection | 76 |
| Table 75. | CTRL9_XL register | 76 |
| Table 76. | CTRL9_XL register description | 76 |
| Table 77. | CTRL10_C register | 77 |
| Table 78. | CTRL10_C register description | 77 |
| Table 79. | MASTER_CONFIG register | 77 |
| Table 80. | MASTER_CONFIG register description | 78 |
| Table 81. | WAKE_UP_SRC register | 78 |
| Table 82. | WAKE_UP_SRC register description | 78 |
| Table 83. | TAP_SRC register | 79 |
| Table 84. | TAP_SRC register description | 79 |
| Table 85. | D6D_SRC register | 79 |
| Table 86. | D6D_SRC register description | 79 |
| Table 87. | STATUS_REG register | 80 |
| Table 88. | STATUS_REG register description | 80 |
| Table 89. | STATUS_SPIAux register | 80 |
| Table 90. | STATUS_SPIAux description | 80 |
| Table 91. | OUT_TEMP_L register | 80 |
| Table 92. | OUT_TEMP_H register | 80 |
| Table 93. | OUT_TEMP register description | 80 |
| Table 94. | OUTX_L_G register | 81 |
| Table 95. | OUTX_L_G register description | 81 |
| Table 96. | OUTX_H_G register | 81 |
| Table 97. | OUTX_H_G register description | 81 |
| Table 98. | OUTY_L_G register | 82 |
| Table 99. | OUTY_L_G register description | 82 |
| Table 100. | OUTY_H_G register | 82 |

| | | |
|------------|--|----|
| Table 101. | OUTY_H_G register description | 82 |
| Table 102. | OUTZ_L_G register | 83 |
| Table 103. | OUTZ_L_G register description | 83 |
| Table 104. | OUTZ_H_G register | 83 |
| Table 105. | OUTZ_H_G register description | 83 |
| Table 106. | OUTX_L_XL register. | 84 |
| Table 107. | OUTX_L_XL register description | 84 |
| Table 108. | OUTX_H_XL register | 84 |
| Table 109. | OUTX_H_XL register description | 84 |
| Table 110. | OUTY_L_XL register. | 84 |
| Table 111. | OUTY_L_XL register description | 84 |
| Table 112. | OUTY_H_XL register | 85 |
| Table 113. | OUTY_H_XL register description | 85 |
| Table 114. | OUTZ_L_XL register. | 85 |
| Table 115. | OUTZ_L_XL register description | 85 |
| Table 116. | OUTZ_H_XL register | 85 |
| Table 117. | OUTZ_H_XL register description | 85 |
| Table 118. | SENSORHUB1_REG register | 85 |
| Table 119. | SENSORHUB1_REG register description | 85 |
| Table 120. | SENSORHUB2_REG register | 86 |
| Table 121. | SENSORHUB2_REG register description | 86 |
| Table 122. | SENSORHUB3_REG register | 86 |
| Table 123. | SENSORHUB3_REG register description | 86 |
| Table 124. | SENSORHUB4_REG register | 86 |
| Table 125. | SENSORHUB4_REG register description | 86 |
| Table 126. | SENSORHUB5_REG register | 86 |
| Table 127. | SENSORHUB5_REG register description | 86 |
| Table 128. | SENSORHUB6_REG register | 87 |
| Table 129. | SENSORHUB6_REG register description | 87 |
| Table 130. | SENSORHUB7_REG register | 87 |
| Table 131. | SENSORHUB7_REG register description | 87 |
| Table 132. | SENSORHUB8_REG register | 87 |
| Table 133. | SENSORHUB8_REG register description | 87 |
| Table 134. | SENSORHUB9_REG register | 87 |
| Table 135. | SENSORHUB9_REG register description | 87 |
| Table 136. | SENSORHUB10_REG register | 88 |
| Table 137. | SENSORHUB10_REG register description | 88 |
| Table 138. | SENSORHUB11_REG register | 88 |
| Table 139. | SENSORHUB11_REG register description | 88 |
| Table 140. | SENSORHUB12_REG register | 88 |
| Table 141. | SENSORHUB12_REG register description | 88 |
| Table 142. | FIFO_STATUS1 register | 88 |
| Table 143. | FIFO_STATUS1 register description | 88 |
| Table 144. | FIFO_STATUS2 register | 89 |
| Table 145. | FIFO_STATUS2 register description | 89 |
| Table 146. | FIFO_STATUS3 register | 89 |
| Table 147. | FIFO_STATUS3 register description | 89 |
| Table 148. | FIFO_STATUS4 register | 90 |
| Table 149. | FIFO_STATUS4 register description | 90 |
| Table 150. | FIFO_DATA_OUT_L register | 90 |
| Table 151. | FIFO_DATA_OUT_L register description | 90 |
| Table 152. | FIFO_DATA_OUT_H register. | 90 |

| | | |
|------------|---|-----|
| Table 153. | FIFO_DATA_OUT_H register description | 90 |
| Table 154. | TIMESTAMP0_REG register | 91 |
| Table 155. | TIMESTAMP0_REG register description | 91 |
| Table 156. | TIMESTAMP1_REG register | 91 |
| Table 157. | TIMESTAMP1_REG register description | 91 |
| Table 158. | TIMESTAMP2_REG register | 91 |
| Table 159. | TIMESTAMP2_REG register description | 91 |
| Table 160. | STEP_TIMESTAMP_L register | 91 |
| Table 161. | STEP_TIMESTAMP_L register description | 91 |
| Table 162. | STEP_TIMESTAMP_H register | 92 |
| Table 163. | STEP_TIMESTAMP_H register description | 92 |
| Table 164. | STEP_COUNTER_L register | 92 |
| Table 165. | STEP_COUNTER_L register description | 92 |
| Table 166. | STEP_COUNTER_H register | 92 |
| Table 167. | STEP_COUNTER_H register description | 92 |
| Table 168. | SENSORHUB13_REG register | 92 |
| Table 169. | SENSORHUB13_REG register description | 92 |
| Table 170. | SENSORHUB14_REG register | 93 |
| Table 171. | SENSORHUB14_REG register description | 93 |
| Table 172. | SENSORHUB15_REG register | 93 |
| Table 173. | SENSORHUB15_REG register description | 93 |
| Table 174. | SENSORHUB16_REG register | 93 |
| Table 175. | SENSORHUB16_REG register description | 93 |
| Table 176. | SENSORHUB17_REG register | 93 |
| Table 177. | SENSORHUB17_REG register description | 93 |
| Table 178. | SENSORHUB18_REG register | 94 |
| Table 179. | SENSORHUB18_REG register description | 94 |
| Table 180. | FUNC_SRC1 register | 94 |
| Table 181. | FUNC_SRC1 register description | 94 |
| Table 182. | FUNC_SRC2 register | 95 |
| Table 183. | FUNC_SRC2 register description | 95 |
| Table 184. | WRIST_TILT_IA register | 95 |
| Table 185. | WRIST_TILT_IA register description | 95 |
| Table 186. | TAP_CFG register | 96 |
| Table 187. | TAP_CFG register description | 96 |
| Table 188. | TAP_THS_6D register | 97 |
| Table 189. | TAP_THS_6D register description | 97 |
| Table 190. | Threshold for D4D/D6D function | 97 |
| Table 191. | INT_DUR2 register | 97 |
| Table 192. | INT_DUR2 register description | 97 |
| Table 193. | WAKE_UP_THS register | 98 |
| Table 194. | WAKE_UP_THS register description | 98 |
| Table 195. | WAKE_UP_DUR register | 98 |
| Table 196. | WAKE_UP_DUR register description | 98 |
| Table 197. | FREE_FALL register | 99 |
| Table 198. | FREE_FALL register description | 99 |
| Table 199. | Threshold for free-fall function | 99 |
| Table 200. | MD1_CFG register | 100 |
| Table 201. | MD1_CFG register description | 100 |
| Table 202. | MD2_CFG register | 101 |
| Table 203. | MD2_CFG register description | 101 |
| Table 204. | MASTER_CMD_CODE register | 102 |

| | | |
|------------|--|-----|
| Table 205. | MASTER_CMD_CODE register description | 102 |
| Table 206. | SENS_SYNC_SPI_ERROR_CODE register | 102 |
| Table 207. | SENS_SYNC_SPI_ERROR_CODE register description | 102 |
| Table 208. | OUT_MAG_RAW_X_L register | 102 |
| Table 209. | OUT_MAG_RAW_X_L register description | 102 |
| Table 210. | OUT_MAG_RAW_X_H register | 102 |
| Table 211. | OUT_MAG_RAW_X_H register description | 102 |
| Table 212. | OUT_MAG_RAW_Y_L register | 103 |
| Table 213. | OUT_MAG_RAW_Y_L register description | 103 |
| Table 214. | OUT_MAG_RAW_Y_H register | 103 |
| Table 215. | OUT_MAG_RAW_Y_H register description | 103 |
| Table 216. | OUT_MAG_RAW_Z_L register | 103 |
| Table 217. | OUT_MAG_RAW_Z_L register description | 103 |
| Table 218. | OUT_MAG_RAW_Z_H register | 103 |
| Table 219. | OUT_MAG_RAW_Z_H register description | 103 |
| Table 220. | INT_OIS register | 104 |
| Table 221. | INT_OIS register description | 104 |
| Table 222. | CTRL1_OIS register | 104 |
| Table 223. | CTRL1_OIS register description | 104 |
| Table 224. | DEN mode selection | 105 |
| Table 225. | CTRL2_OIS register | 105 |
| Table 226. | CTRL2_OIS register description | 105 |
| Table 227. | Gyroscope OIS chain LPF1 bandwidth selection | 105 |
| Table 228. | CTRL3_OIS register | 106 |
| Table 229. | CTRL3_OIS register description | 106 |
| Table 230. | Accelerometer OIS channel bandwidth selection | 106 |
| Table 231. | Self-test nominal output variation | 107 |
| Table 232. | X_OFS_USR register | 107 |
| Table 233. | X_OFS_USR register description | 107 |
| Table 234. | Y_OFS_USR register | 107 |
| Table 235. | Y_OFS_USR register description | 107 |
| Table 236. | Z_OFS_USR register | 107 |
| Table 237. | Z_OFS_USR register description | 107 |
| Table 238. | Register address map - Bank A - embedded functions | 108 |
| Table 239. | Register address map - Bank B - embedded functions | 109 |
| Table 240. | SLV0_ADD register | 110 |
| Table 241. | SLV0_ADD register description | 110 |
| Table 242. | SLV0_SUBADD register | 110 |
| Table 243. | SLV0_SUBADD register description | 110 |
| Table 244. | SLAVE0_CONFIG register | 110 |
| Table 245. | SLAVE0_CONFIG register description | 111 |
| Table 246. | SLV1_ADD register | 111 |
| Table 247. | SLV1_ADD register description | 111 |
| Table 248. | SLV1_SUBADD register | 111 |
| Table 249. | SLV1_SUBADD register description | 111 |
| Table 250. | SLAVE1_CONFIG register | 112 |
| Table 251. | SLAVE1_CONFIG register description | 112 |
| Table 252. | SLV2_ADD register | 112 |
| Table 253. | SLV2_ADD register description | 112 |
| Table 254. | SLV2_SUBADD register | 112 |
| Table 255. | SLV2_SUBADD register description | 112 |
| Table 256. | SLAVE2_CONFIG register | 113 |

| | | |
|------------|--|-----|
| Table 257. | SLAVE2_CONFIG register description | 113 |
| Table 258. | SLV3_ADD register | 113 |
| Table 259. | SLV3_ADD register description | 113 |
| Table 260. | SLV3_SUBADD register | 113 |
| Table 261. | SLV3_SUBADD register description | 113 |
| Table 262. | SLAVE3_CONFIG register | 114 |
| Table 263. | SLAVE3_CONFIG register description | 114 |
| Table 264. | DATAWRITE_SRC_MODE_SUB_SLV0 register | 114 |
| Table 265. | DATAWRITE_SRC_MODE_SUB_SLV0 register description | 114 |
| Table 266. | CONFIG_PEDO_THS_MIN register | 114 |
| Table 267. | CONFIG_PEDO_THS_MIN register description | 114 |
| Table 268. | SM_THS register | 115 |
| Table 269. | SM_THS register description | 115 |
| Table 270. | PEDO_DEB_REG register | 115 |
| Table 271. | PEDO_DEB_REG register description | 115 |
| Table 272. | STEP_COUNT_DELTA register | 115 |
| Table 273. | STEP_COUNT_DELTA register description | 115 |
| Table 274. | MAG_SI_XX register | 116 |
| Table 275. | MAG_SI_XX register description | 116 |
| Table 276. | MAG_SI_XY register | 116 |
| Table 277. | MAG_SI_XY register description | 116 |
| Table 278. | MAG_SI_XZ register | 116 |
| Table 279. | MAG_SI_XZ register description | 116 |
| Table 280. | MAG_SI_YX register | 116 |
| Table 281. | MAG_SI_YX register description | 116 |
| Table 282. | MAG_SI_YY register | 117 |
| Table 283. | MAG_SI_YY register description | 117 |
| Table 284. | MAG_SI_YZ register | 117 |
| Table 285. | MAG_SI_YZ register description | 117 |
| Table 286. | MAG_SI_ZX register | 117 |
| Table 287. | MAG_SI_ZX register description | 117 |
| Table 288. | MAG_SI_ZY register | 117 |
| Table 289. | MAG_SI_ZY register description | 117 |
| Table 290. | MAG_SI_ZZ register | 118 |
| Table 291. | MAG_SI_ZZ register description | 118 |
| Table 292. | MAG_OFFX_L register | 118 |
| Table 293. | MAG_OFFX_L register description | 118 |
| Table 294. | MAG_OFFX_H register | 118 |
| Table 295. | MAG_OFFX_H register description | 118 |
| Table 296. | MAG_OFFY_L register | 118 |
| Table 297. | MAG_OFFY_L register description | 118 |
| Table 298. | MAG_OFFY_H register | 119 |
| Table 299. | MAG_OFFY_H register description | 119 |
| Table 300. | MAG_OFFZ_L register | 119 |
| Table 301. | MAG_OFFZ_L register description | 119 |
| Table 302. | MAG_OFFZ_H register | 119 |
| Table 303. | MAG_OFFZ_H register description | 119 |
| Table 304. | A_WRIST_TILT_LAT register | 120 |
| Table 305. | A_WRIST_TILT_LAT register description | 120 |
| Table 306. | A_WRIST_TILT_THS register | 120 |
| Table 307. | A_WRIST_TILT_THS register description | 120 |
| Table 308. | A_WRIST_TILT_Mask register | 120 |

| | | |
|------------|---|-----|
| Table 309. | A_WRIST_TILT_Mask register description. | 120 |
| Table 310. | Reel dimensions for carrier tape of LGA-14 package. | 124 |
| Table 311. | Document revision history. | 125 |

List of figures

| | | |
|------------|--|-----|
| Figure 1. | Pin connections | 20 |
| Figure 2. | LSM6DSM connection modes | 21 |
| Figure 3. | SPI slave timing diagram (in mode 3) | 28 |
| Figure 4. | I ² C timing diagram | 29 |
| Figure 5. | Block diagram of filters | 34 |
| Figure 6. | Gyroscope digital chain - Mode 1 (UI/EIS) and Mode 2 | 34 |
| Figure 7. | Gyroscope digital chain - Mode 3 / Mode 4 (OIS/EIS) | 35 |
| Figure 8. | Accelerometer chain | 36 |
| Figure 9. | Accelerometer composite filter (for Modes 1/2 and Mode 3*) | 36 |
| Figure 10. | Accelerometer composite filter (Mode 4 only*) | 37 |
| Figure 11. | Read and write protocol (in mode 3) | 45 |
| Figure 12. | SPI read protocol (in mode 3) | 46 |
| Figure 13. | Multiple byte SPI read protocol (2-byte example) (in mode 3) | 46 |
| Figure 14. | SPI write protocol (in mode 3) | 47 |
| Figure 15. | Multiple byte SPI write protocol (2-byte example) (in mode 3) | 47 |
| Figure 16. | SPI read protocol in 3-wire mode (in mode 3) | 48 |
| Figure 17. | LSM6DSM electrical connections in Mode 1 | 49 |
| Figure 18. | LSM6DSM electrical connections in Mode 2 | 50 |
| Figure 19. | LSM6DSM electrical connections in Mode 3 and Mode 4 (auxiliary 3-wire SPI) | 51 |
| Figure 20. | LSM6DSM electrical connections in Mode 3 and Mode 4 (auxiliary 4-wire SPI) | 52 |
| Figure 21. | Gyroscope chain | 55 |
| Figure 22. | Accelerometer chain (available only in Mode 4) | 56 |
| Figure 23. | LGA-14L 2.5x3x0.86 mm package outline and mechanical data | 122 |
| Figure 24. | Carrier tape information for LGA-14 package | 123 |
| Figure 25. | LGA-14 package orientation in carrier tape | 123 |
| Figure 26. | Reel information for carrier tape of LGA-14 package | 124 |

1 Overview

The LSM6DSM is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

The integrated power-efficient modes are able to reduce the power consumption down to 0.65 mA in high-performance mode, combining always-on low-power features with superior sensing precision for an optimal motion experience for the consumer thanks to ultra-low noise performance for both the gyroscope and accelerometer.

The LSM6DSM delivers best-in-class motion sensing that can detect orientation and gestures in order to empower application developers and consumers with features and capabilities that are more sophisticated than simply orienting their devices to portrait and landscape mode.

The event-detection interrupts enable efficient and reliable motion tracking and contextual awareness, implementing hardware recognition of free-fall events, 6D orientation, click and double-click sensing, activity or inactivity, and wakeup events.

The LSM6DSM supports main OS requirements, offering real, virtual and batch mode sensors. In addition, the LSM6DSM can efficiently run the sensor-related features specified in Android, saving power and enabling faster reaction time. In particular, the LSM6DSM has been designed to implement hardware features such as significant motion, tilt, pedometer functions, timestamping and to support the data acquisition of an external magnetometer with ironing correction (hard, soft).

The LSM6DSM offers hardware flexibility to connect the pins with different mode connections to external sensors to expand functionalities such as adding a sensor hub, auxiliary SPI, etc.

Up to 4 kbyte of FIFO with dynamic allocation of significant data (i.e. external sensors, timestamp, etc.) allows overall power saving of the system.

The LSM6DSM fully supports OIS/EIS applications using both the gyroscope and accelerometer sensor. The device can output OIS data through a dedicated auxiliary SPI and includes a dedicated configurable signal processing path for OIS. OIS data can be sent directly to the application processor for data processing. The gyroscope UI signal processing path is completely independent from that of the OIS and is readable through FIFO.

Like the entire portfolio of MEMS sensor modules, the LSM6DSM leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DSM is available in a small plastic land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultra-compact solutions.

2 Embedded low-power features

The LSM6DSM has been designed to be fully compliant with Android, featuring the following on-chip functions:

- 4 kbyte data buffering
 - 100% efficiency with flexible configurations and partitioning
 - Possibility to store timestamp
- Event-detection interrupts (fully configurable):
 - Free-fall
 - Wakeup
 - 6D orientation
 - Click And double-click sensing
 - Activity / inactivity recognition
- Specific IP blocks with negligible power consumption and high-performance:
 - Pedometer functions: step detector and step counters
 - Tilt (refer to [Section 2.1: Tilt detection](#) for additional information)
 - Absolute Wrist Tilt (refer to [Section 2.2: Absolute wrist tilt](#) for additional information)
 - Significant Motion Detection
- Sensor hub
 - Up to 6 total sensors: 2 internal (accelerometer and gyroscope) and 4 external sensors
- Data rate synchronization with external trigger for reduced sensor access and enhanced fusion

2.1 Tilt detection

The tilt function helps to detect activity change and has been implemented in hardware using only the accelerometer to achieve both the targets of ultra-low power consumption and robustness during the short duration of dynamic accelerations.

It is based on a trigger of an event each time the device's tilt changes. For a more customized user experience, in the LSM6DSM the tilt function is configurable through:

- a programmable average window
- a programmable average threshold

The tilt function can be used with different scenarios, for example:

- a) Triggers when phone is in a front pants pocket and the user goes from sitting to standing or standing to sitting;
- b) Doesn't trigger when phone is in a front pants pocket and the user is walking, running or going upstairs.

2.2 Absolute wrist tilt

The LSM6DSM implements in hardware the Absolute Wrist Tilt (AWT) function which allows detecting when the angle between a selectable accelerometer semi-axis and the horizontal plane becomes higher than a specific user-selectable value.

Configurable threshold and latency parameters are associated with the AWT function: the threshold parameter defines the amplitude of the tilt angle; the latency parameter defines the minimum duration of the AWT event to be recognized. The AWT interrupt signal is generated if the tilt angle is higher than the threshold angle for a period of time equal to or greater than the latency period.

The AWT function is based on the accelerometer sensor only and works at 26 Hz, so the accelerometer ODR must be set at a value of 26 Hz or higher.

By default, the AWT algorithm is applied to the positive X-axis.

In order to enable the AWT function it is necessary to set to 1 both the FUNC_EN bit and the WRIST_TILT_EN bit of [CTRL10_C \(19h\)](#).

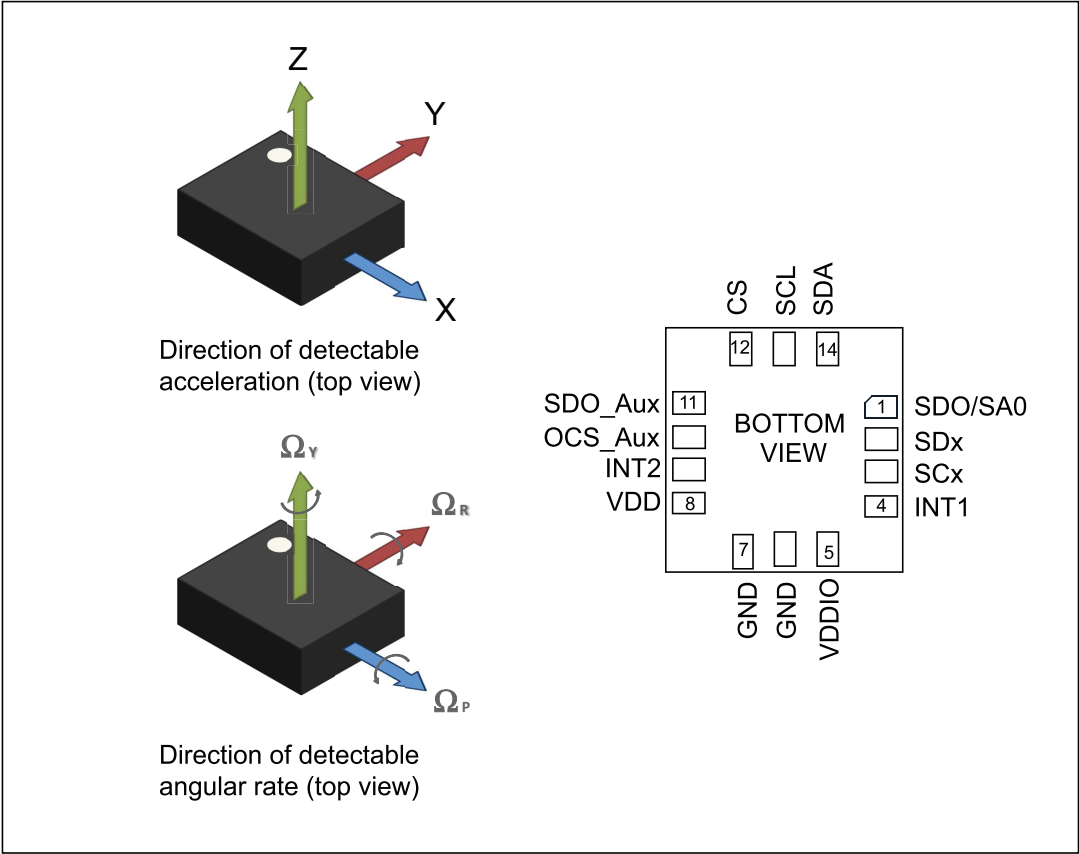
The AWT interrupt signal can be driven to the INT2 interrupt pin by setting to 1 the INT2_WRIST_TILT bit of the [DRDY_PULSE_CFG \(0Bh\)](#) register; it can also be checked by reading the WRIST_TILT_IA bit of the [FUNC_SRC2 \(54h\)](#) register (it will also clear the interrupt signal if latched).

[WRIST_TILT_IA \(55h\)](#) is the status register to be used to detect which axis has triggered the AWT event (not applicable when using one axis side only).

The full description and an example is given in the dedicated application note.

3 Pin description

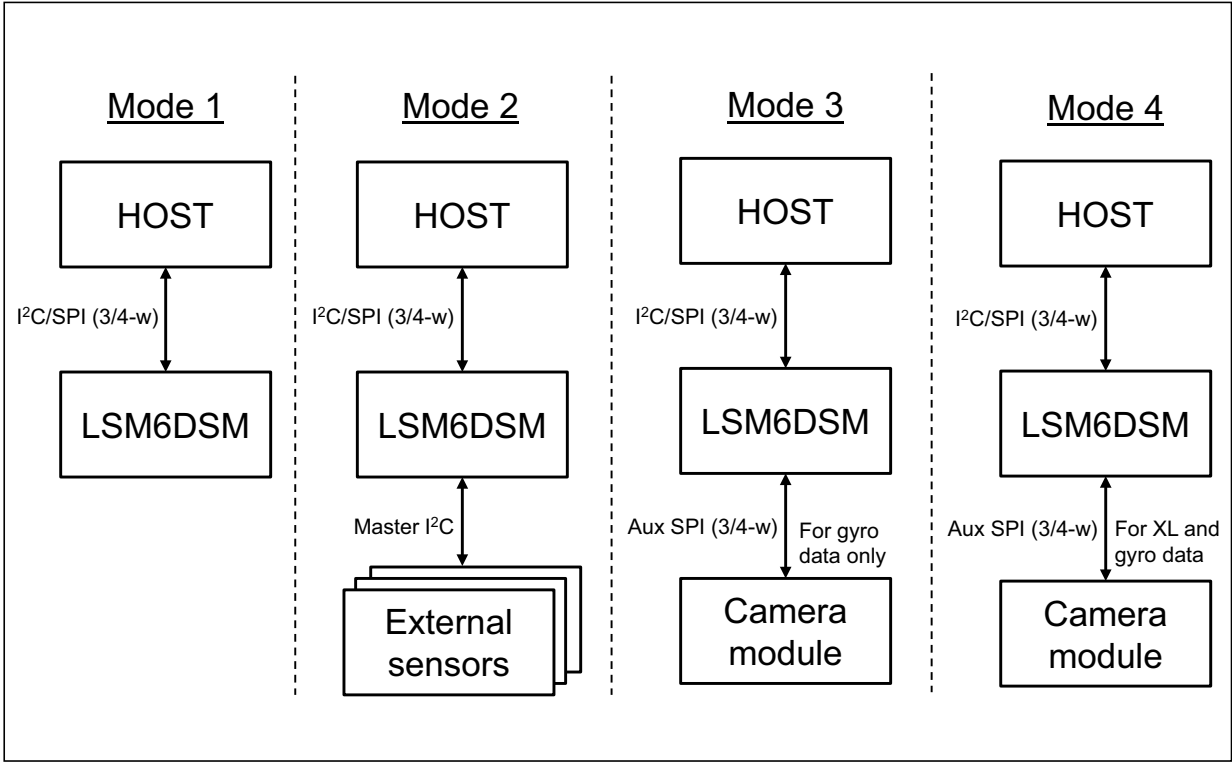
Figure 1. Pin connections



3.1 Pin connections

- The LSM6DSM offers flexibility to connect the pins in order to have four different mode connections and functionalities. In detail:
- **Mode 1:** I²C slave interface or SPI (3- and 4-wire) serial interface is available;
 - **Mode 2:** I²C slave interface or SPI (3- and 4-wire) serial interface and I²C interface master for external sensor connections are available;
 - **Mode 3:** I²C slave interface or SPI (3- and 4-wire) serial interface is available for the application processor interface while an auxiliary SPI (3- and 4-wire) serial interface for external sensor connections (i.e. camera module) is available for the gyroscope ONLY;
 - **Mode 4:** I²C slave interface or SPI (3- and 4-wire) serial interface is available for the application processor interface while an auxiliary SPI (3- and 4-wire) serial interface for external sensor connections (i.e. camera module with hybrid OIS) is available for the accelerometer and gyroscope.

Figure 2. LSM6DSM connection modes



In the following table each mode is described for the pin connections and function.

Table 2. Pin description

| Pin# | Name | Mode 1 function | Mode 2 function | Mode 3 / Mode 4 function |
|------|----------------------|--|--|--|
| 1 | SDO/SA0 | SPI 4-wire interface serial data output (SDO) I ² C least significant bit of the device address (SA0) | SPI 4-wire interface serial data output (SDO) I ² C least significant bit of the device address (SA0) | SPI 4-wire interface serial data output (SDO) I ² C least significant bit of the device address (SA0) |
| 2 | SDx | Connect to VDDIO or GND | I ² C serial data master (MSDA) | Auxiliary SPI 3/4-wire interface serial data input (SDI) and SPI 3-wire serial data output (SDO) |
| 3 | SCx | Connect to VDDIO or GND | I ² C serial clock master (MSCL) | Auxiliary SPI 3-wire interface serial port clock (SPC_Aux) |
| 4 | INT1 | Programmable interrupt 1 | | |
| 5 | VDDIO ⁽¹⁾ | Power supply for I/O pins | | |
| 6 | GND | 0 V supply | | |
| 7 | GND | 0 V supply | | |
| 8 | VDD ⁽¹⁾ | Power supply | | |
| 9 | INT2 | Programmable interrupt 2 (INT2) / Data enable (DEN) | Programmable interrupt 2 (INT2)/ Data enable (DEN)/ I ² C master external synchronization signal (MDRDY) | Programmable interrupt 2 (INT2)/ Data enable (DEN) |
| 10 | OCS_Aux | Leave unconnected ⁽²⁾ | Leave unconnected ⁽²⁾ | Auxiliary SPI 3/4-wire interface enable |
| 11 | SDO_Aux | Connect to VDDIO or leave unconnected ⁽²⁾ | Connect to VDDIO or leave unconnected ⁽²⁾ | Auxiliary SPI 3-wire interface: leave unconnected ⁽²⁾ Auxiliary SPI 4-wire interface: serial data output (SDO_Aux) |
| 12 | CS | I ² C/SPI mode selection (1: SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled) | I ² C/SPI mode selection (1: SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled) | I ² C/SPI mode selection (1: SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled) |
| 13 | SCL | I ² C serial clock (SCL) SPI serial port clock (SPC) | I ² C serial clock (SCL) SPI serial port clock (SPC) | I ² C serial clock (SCL) SPI serial port clock (SPC) |
| 14 | SDA | I ² C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO) | I ² C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO) | I ² C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO) |

1. Recommended 100 nF filter capacitor.

2. Leave pin electrically unconnected and soldered to PCB.

4 Module specifications

4.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

Table 3. Mechanical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|----------|--|--------------------|------|---------------------|------|----------|
| LA_FS | Linear acceleration measurement range | | | ±2 | | g |
| | | | | ±4 | | |
| | | | | ±8 | | |
| | | | | ±16 | | |
| G_FS | Angular rate measurement range | | | ±125 | | dps |
| | | | | ±250 | | |
| | | | | ±500 | | |
| | | | | ±1000 | | |
| | | | | ±2000 | | |
| LA_So | Linear acceleration sensitivity ⁽²⁾ | FS = ±2 | | 0.061 | | mg/LSB |
| | | FS = ±4 | | 0.122 | | |
| | | FS = ±8 | | 0.244 | | |
| | | FS = ±16 | | 0.488 | | |
| G_So | Angular rate sensitivity ⁽²⁾ | FS = ±125 | | 4.375 | | mdps/LSB |
| | | FS = ±250 | | 8.75 | | |
| | | FS = ±500 | | 17.50 | | |
| | | FS = ±1000 | | 35 | | |
| | | FS = ±2000 | | 70 | | |
| G_So% | Sensitivity tolerance ⁽³⁾ | at component level | | ±1 | | % |
| LA_SoDr | Linear acceleration sensitivity change vs. temperature ⁽⁴⁾ | from -40° to +85° | | ±0.01 | | %/°C |
| G_SoDr | Angular rate sensitivity change vs. temperature ⁽⁴⁾ | from -40° to +85° | | ±0.007 | | %/°C |
| LA_TyOff | Linear acceleration zero-g level offset accuracy ⁽⁵⁾ | | | ±40 | | mg |
| G_TyOff | Angular rate zero-rate level ⁽⁵⁾ | | | ±2 | | dps |
| LA_OffDr | Linear acceleration zero-g level change vs. temperature ⁽⁴⁾ | | | ±0.1 | | mg/°C |
| G_OffDr | Angular rate typical zero-rate level change vs. temperature ⁽⁴⁾ | | | ±0.015 | | dps/°C |

Table 3. Mechanical characteristics (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--------|---|------------------------|------|---|------|--------------------------------|
| Rn | Rate noise density in high-performance mode ⁽⁶⁾ | | | 3.8 | | mdps/ $\sqrt{\text{Hz}}$ |
| RnRMS | Gyroscope RMS noise in normal/low-power mode ⁽⁷⁾ | | | 75 | | mdps |
| An | Acceleration noise density in high-performance mode ⁽⁸⁾ | FS = $\pm 2\text{ g}$ | | 75 | | $\mu\text{g}/\sqrt{\text{Hz}}$ |
| | | FS = $\pm 4\text{ g}$ | | 80 | | |
| | | FS = $\pm 8\text{ g}$ | | 90 | | |
| | | FS = $\pm 16\text{ g}$ | | 130 | | |
| RMS | Acceleration RMS noise in normal/low-power mode ⁽⁹⁾⁽¹⁰⁾ | FS = $\pm 2\text{ g}$ | | 1.8 | | mg(RMS) |
| | | FS = $\pm 4\text{ g}$ | | 2.0 | | |
| | | FS = $\pm 8\text{ g}$ | | 2.4 | | |
| | | FS = $\pm 16\text{ g}$ | | 3.0 | | |
| LA_ODR | Linear acceleration output data rate | | | 1.6 ⁽¹¹⁾ 12.5 26 52 104 208 416 833 1666 3332 6664 | | Hz |
| G_ODR | Angular rate output data rate | | | 12.5 26 52 104 208 416 833 1666 3332 6664 | | |
| Vst | Linear acceleration self-test output change ⁽¹²⁾⁽¹³⁾⁽¹⁴⁾ | | 90 | | 1700 | mg |
| | Angular rate self-test output change ⁽¹⁵⁾⁽¹⁶⁾ | FS = 250 dps | 20 | | 80 | dps |
| | | FS = 2000 dps | 150 | | 700 | dps |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.

2. Sensitivity values after factory calibration test and trimming.

3. Subject to change.

4. Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples. Not measured during final test for production.
5. Values after factory calibration test and trimming.
6. Gyroscope rate noise density in high-performance mode is independent of the ODR and FS setting.
7. Gyroscope RMS noise in normal/low-power mode is independent of the ODR and FS setting.
8. Accelerometer noise density in high-performance mode is independent of the ODR.
9. Accelerometer RMS noise in normal/low-power mode is independent of the ODR.
10. Noise RMS related to $BW = ODR / 2$ (for $ODR / 9$, typ value can be calculated by $Typ * 0.6$).
11. This ODR is available when accelerometer is in low-power mode.
12. The sign of the linear acceleration self-test output change is defined by the STx_XL bits in [CTRL5_C \(14h\)](#), [Table 65](#) for all axes.
13. The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of: $OUTPUT[LSb] \text{ (self-test enabled)} - OUTPUT[LSb] \text{ (self-test disabled)}$. $1LSb = 0.061 \text{ mg}$ at $\pm 2 \text{ g}$ full scale.
14. Accelerometer self-test limits are full-scale independent.
15. The sign of the angular rate self-test output change is defined by the STx_G bits in [CTRL5_C \(14h\)](#), [Table 64](#) for all axes.
16. The angular rate self-test output change is defined with the device in stationary condition as the absolute value of: $OUTPUT[LSb] \text{ (self-test enabled)} - OUTPUT[LSb] \text{ (self-test disabled)}$. $1LSb = 70 \text{ mdps}$ at $\pm 2000 \text{ dps}$ full scale.

4.2 Electrical characteristics

@ V_{dd} = 1.8 V, T = 25 °C unless otherwise noted.

Table 4. Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|----------------------|--|--|--------------------------|---------------------|-------------------------|------|
| V _{dd} | Supply voltage | | 1.71 | 1.8 | 3.6 | V |
| V _{dd_IO} | Power supply for I/O | | 1.62 | | 3.6 | V |
| I _{ddHP} | Gyroscope and accelerometer current consumption in high-performance mode | ODR = 1.6 kHz | | 0.65 | | mA |
| I _{ddNM} | Gyroscope and accelerometer current consumption in normal mode | ODR = 208 Hz | | 0.45 | | mA |
| I _{ddLP} | Gyroscope and accelerometer current consumption in low-power mode | ODR = 52 Hz | | 0.29 | | mA |
| LA_I _{ddHP} | Accelerometer current consumption in high-performance mode | ODR < 1.6 kHz ODR ≥ 1.6 kHz | | 150 160 | | μA |
| LA_I _{ddNM} | Accelerometer current consumption in normal mode | ODR = 208 Hz | | 85 | | μA |
| LA_I _{ddLM} | Accelerometer current consumption in low-power mode | ODR = 52 Hz ODR = 12.5 Hz ODR = 1.6 Hz | | 25 9 4.5 | | μA |
| I _{ddPD} | Gyroscope and accelerometer current consumption during power-down | | | 3 | | μA |
| T _{on} | Turn-on time | | | 35 | | ms |
| V _{IH} | Digital high-level input voltage | | 0.7 *V _{DD_IO} | | | V |
| V _{IL} | Digital low-level input voltage | | | | 0.3 *V _{DD_IO} | V |
| V _{OH} | High-level output voltage | I _{OH} = 4 mA ⁽²⁾ | V _{DD_IO} - 0.2 | | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 4 mA ⁽²⁾ | | | 0.2 | V |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.

2. 4 mA is the maximum driving capability, i.e. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.

4.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

Table 5. Temperature sensor characteristics

| Symbol | Parameter | Test condition | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|---------------------|---|----------------|------|---------------------|------|--------|
| TODR ⁽²⁾ | Temperature refresh rate | | | 52 | | Hz |
| Toff | Temperature offset ⁽³⁾ | | -15 | | +15 | °C |
| TSen | Temperature sensitivity | | | 256 | | LSB/°C |
| TST | Temperature stabilization time ⁽⁴⁾ | | | | 500 | µs |
| T_ADC_res | Temperature ADC resolution | | | 16 | | bit |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.
2. When the accelerometer is in Low-Power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.
3. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
4. Time from power ON bit to valid data based on characterization data.

4.4 Communication interface characteristics

4.4.1 SPI - serial peripheral interface

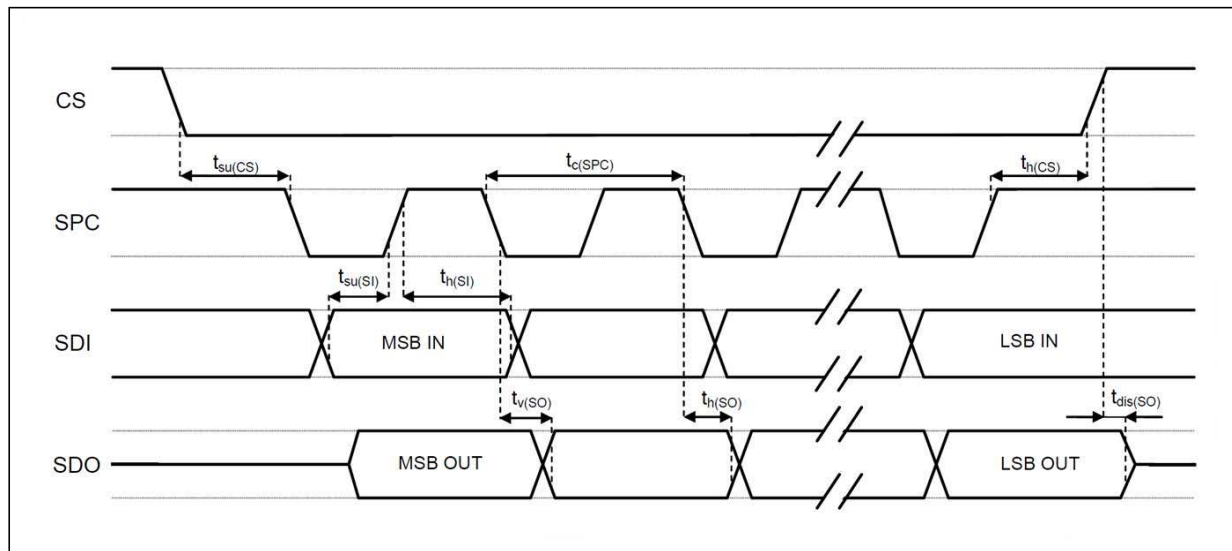
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values (in mode 3)

| Symbol | Parameter | Value ⁽¹⁾ | | Unit |
|---------------|-------------------------|----------------------|-----|------|
| | | Min | Max | |
| $t_{c(SPC)}$ | SPI clock cycle | 100 | | ns |
| $f_{c(SPC)}$ | SPI clock frequency | | 10 | MHz |
| $t_{su(CS)}$ | CS setup time | 5 | | ns |
| $t_{h(CS)}$ | CS hold time | 20 | | |
| $t_{su(SI)}$ | SDI input setup time | 5 | | |
| $t_{h(SI)}$ | SDI input hold time | 15 | | |
| $t_{v(SO)}$ | SDO valid output time | | 50 | |
| $t_{h(SO)}$ | SDO output hold time | 5 | | |
| $t_{dis(SO)}$ | SDO output disable time | | 50 | |

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram (in mode 3)

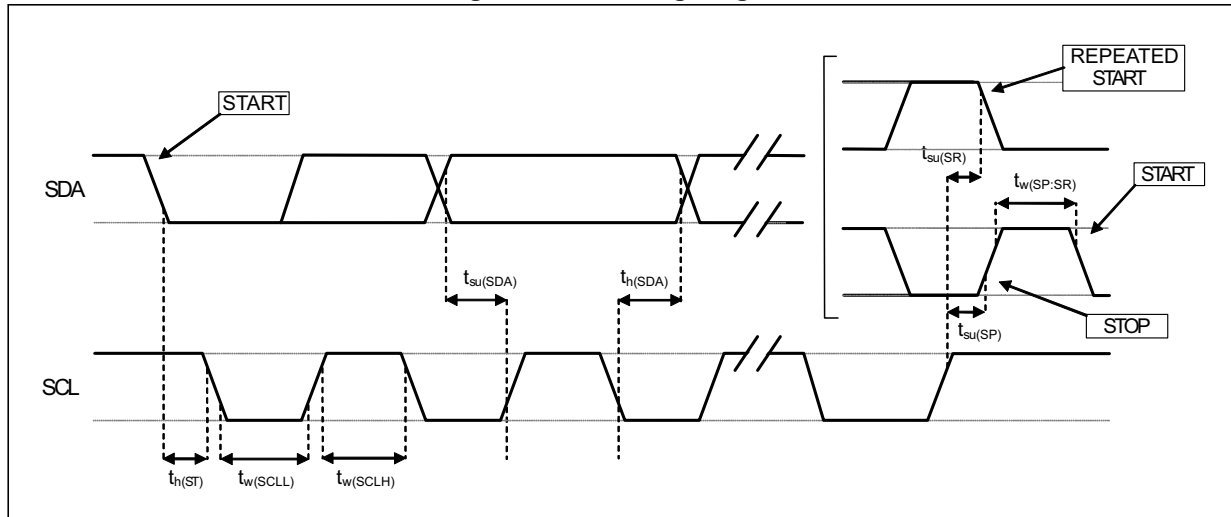


Note: Measurement points are done at $0.2 \cdot V_{dd_IO}$ and $0.8 \cdot V_{dd_IO}$, for both input and output ports.

4.4.2 I²C - inter-IC control interface

Subject to general operating conditions for Vdd and Top.

Figure 4. I²C timing diagram



4.4.2.1 I²C slave

Table 7. I²C slave timing values

| Symbol | Parameter | I ² C standard mode ⁽¹⁾ | | I ² C fast mode ⁽¹⁾ | | Unit |
|-----------------------|--|---|------|---|-----|------|
| | | Min | Max | Min | Max | |
| f _(SCL) | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| t _{w(SCLL)} | SCL clock low time | 4.7 | | 1.3 | | μs |
| t _{w(SCLH)} | SCL clock high time | 4.0 | | 0.6 | | |
| t _{su(SDA)} | SDA setup time | 250 | | 100 | | ns |
| t _{h(SDA)} | SDA data hold time | 0 | 3.45 | 0 | 0.9 | μs |
| t _{h(ST)} | START condition hold time | 4 | | 0.6 | | μs |
| t _{su(SR)} | Repeated START condition setup time | 4.7 | | 0.6 | | |
| t _{su(SP)} | STOP condition setup time | 4 | | 0.6 | | |
| t _{w(SP:SR)} | Bus free time between STOP and START condition | 4.7 | | 1.3 | | |

1. Data based on standard I²C protocol requirement, not tested in production.

Note: Measurement points are done at 0.2·Vdd_{IO} and 0.8·Vdd_{IO}, for both ports.

4.4.2.2 I²C master

When in I²C Master Mode, an external sensor can be connected to LSM6DSM. LSM6DSM supports I²C Master - Fast Mode only.

Table 8. I²C master timing values

| Symbol | Parameter | I ² C Master | I ² C Fast Mode (min) | Unit |
|-----------------------|--|-------------------------|----------------------------------|------|
| f _(SCL) | SCL clock frequency | 116.3 | 0 (400 kHz max) | kHz |
| t _{w(SCLL)} | SCL clock low time | 5.86 | 1.3 | μs |
| t _{w(SCLH)} | SCL clock high time | 2.74 | 0.6 | ns |
| | Data valid time | 3.9 | - | μs |
| | SDA hold time | ≥0 | 0 | ns |
| | SDA setup time | ≥100 | 100 | ns |
| t _{su(SR)} | Repeated START condition setup time | 1.56 | 0.6 | μs |
| t _{su(HD)} | Repeated START condition hold time | 1.56 | 0.6 | μs |
| t _{su(SP)} | STOP condition setup time | 2.73 | 0.6 | μs |
| t _{w(SP:SR)} | Bus free time between STOP and START condition | 21 | 1.3 | μs |

4.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

| Symbol | Ratings | Maximum value | Unit |
|------------------|---|---------------------|----------|
| Vdd | Supply voltage | -0.3 to 4.8 | V |
| T _{STG} | Storage temperature range | -40 to +125 | °C |
| Sg | Acceleration <i>g</i> for 0.2 ms | 10,000 | <i>g</i> |
| ESD | Electrostatic discharge protection (HBM) | 2 | kV |
| Vin | Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0) | -0.3 to Vdd_IO +0.3 | V |

Note: *Supply voltage on any pin should never exceed 4.8 V.*



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4.6 Terminology

4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ± 1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see [Table 3](#)).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see [Table 3](#)).

4.6.2 Zero-g and zero-rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in [Table 3](#). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see [Table 3](#)).

5 Functionality

5.1 Operating modes

In the LSM6DSM, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The LSM6DSM has three operating modes available:

- only accelerometer active and gyroscope in power-down
- only gyroscope active and accelerometer in power-down
- both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power-down by writing ODR_XL[3:0] in [CTRL1_XL \(10h\)](#) while the gyroscope is activated from power-down by writing ODR_G[3:0] in [CTRL2_G \(11h\)](#). For combo-mode the ODRs are totally independent.

5.2 Gyroscope power modes

In the LSM6DSM, the gyroscope can be configured in four different operating modes: power-down, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the G_HM_MODE bit in [CTRL7_G \(16h\)](#). If G_HM_MODE is set to '0', high-performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).

To enable the low-power and normal mode, the G_HM_MODE bit has to be set to '1'. Low-power mode is available for lower ODRs (12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

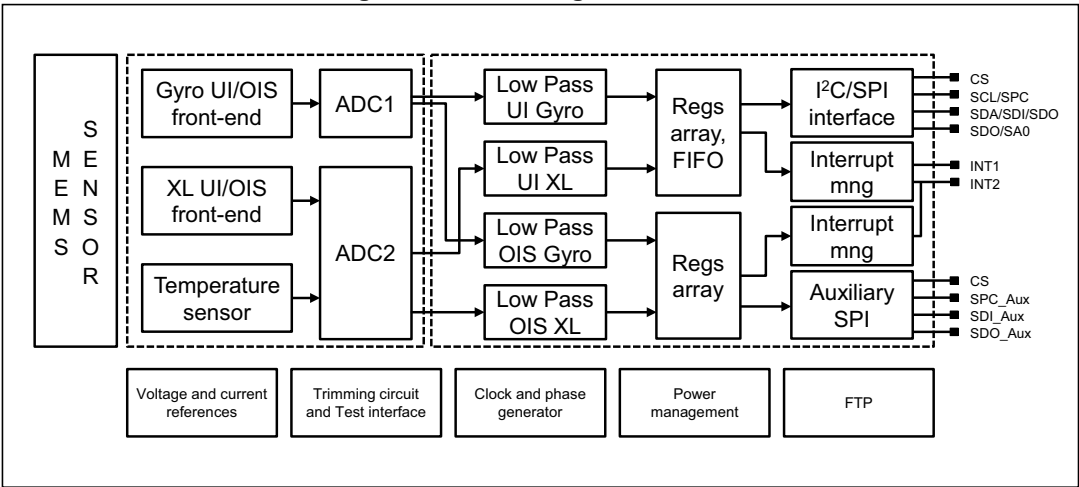
5.3 Accelerometer power modes

In the LSM6DSM, the accelerometer can be configured in four different operating modes: power-down, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the XL_HM_MODE bit in [CTRL6_C \(15h\)](#). If XL_HM_MODE is set to '0', high-performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).

To enable the low-power and normal mode, the XL_HM_MODE bit has to be set to '1'. Low-power mode is available for lower ODRs (1.6, 12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

5.4 Block diagram of filters

Figure 5. Block diagram of filters

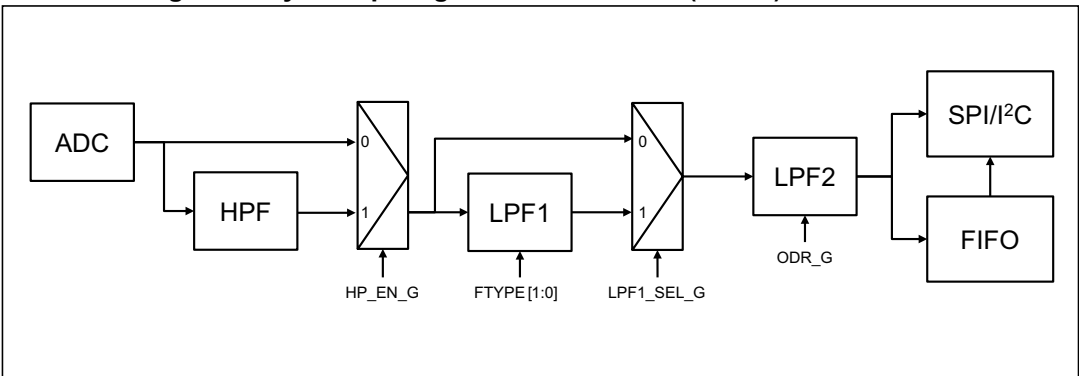


5.4.1 Block diagrams of the gyroscope filters

In the LSM6DSM, the gyroscope filtering chain depends on the mode configuration:

1. Mode 1 (for User Interface (UI) and Electronic Image Stabilization (EIS) functionality through primary interface) and Mode 2

Figure 6. Gyroscope digital chain - Mode 1 (UI/EIS) and Mode 2

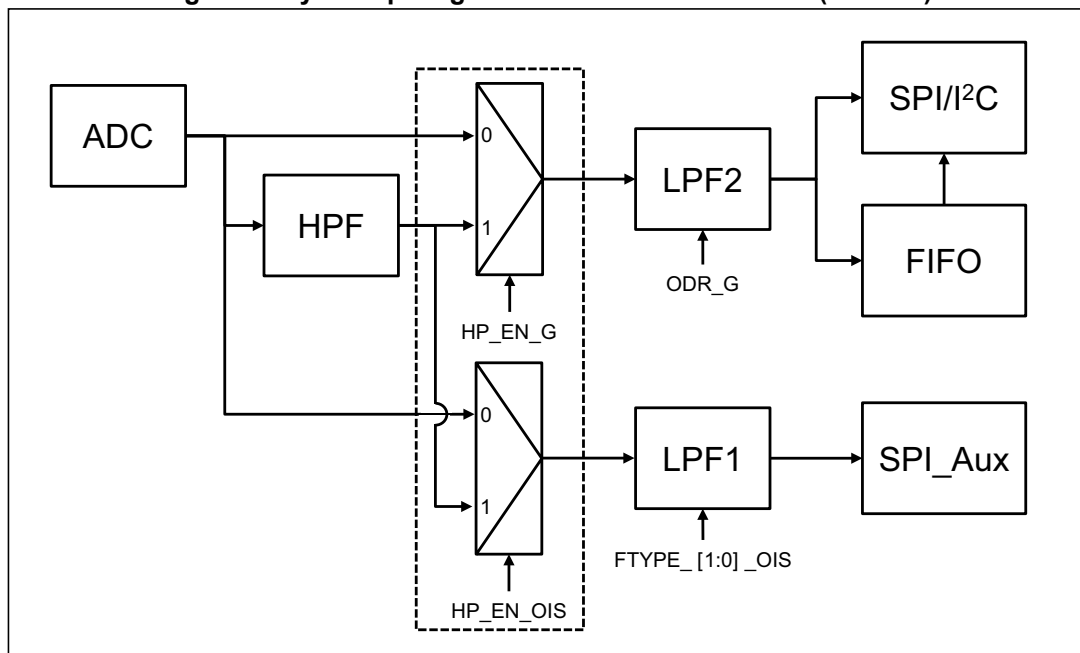


In this configuration, the gyroscope ODR is selectable from 12.5 Hz up to 6.66 kHz. A low-pass filter (LPF1) is available if the auxiliary SPI is disabled, for more details about the filter characteristics see [Table 69: Gyroscope LPF1 bandwidth selection](#).

Data can be acquired from the output registers and FIFO over the primary I²C/SPI interface.

2. Mode 3 / Mode 4 (for OIS and EIS functionality)

Figure 7. Gyroscope digital chain - Mode 3 / Mode 4 (OIS/EIS)



Note: *HP_EN_OIS is active to select HPF on the auxiliary SPI chain only if HPF is not already used in the primary interface.*

In this configuration, there are two paths:

- the chain for User Interface (UI) where the ODR is selectable from 12.5 Hz up to 6.66 kHz
- the chain for OIS/EIS where the ODR is at 6.66 kHz and the LPF1 is available. For more details about the filter characteristics see [Table 227: Gyroscope OIS chain LPF1 bandwidth selection](#).

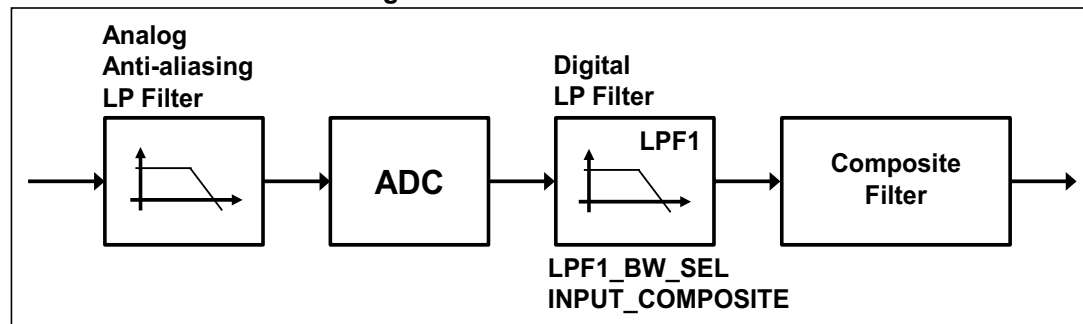
5.4.2 Block diagrams of the accelerometer filters

In the LSM6DSM, the filtering chain for the accelerometer part is composed of the following:

- Analog filter (anti-aliasing)
- Digital filter (LPF1)
- Composite filter

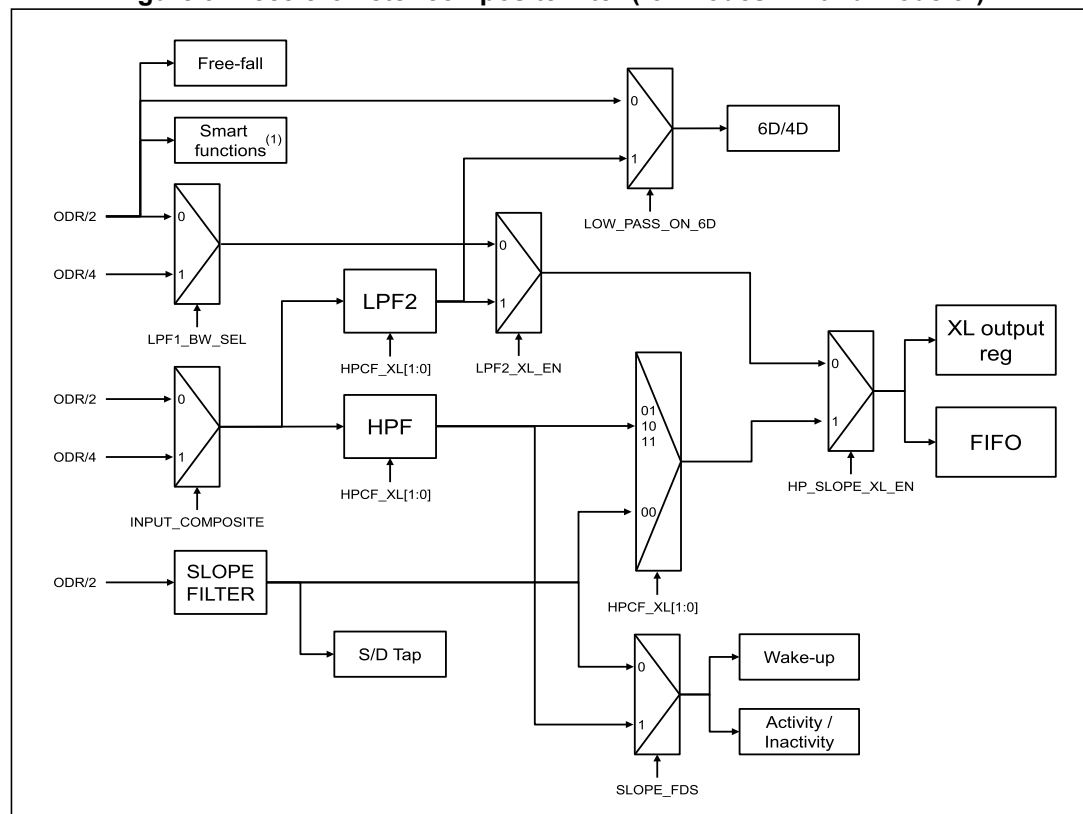
Details of the block diagram appear in the following figure.

Figure 8. Accelerometer chain



The configuration of the digital filter can be set using the LPF1_BW_SEL bit in [CTRL1_XL \(10h\)](#) and the INPUT_COMPOSITE bit in [CTRL8_XL \(17h\)](#).

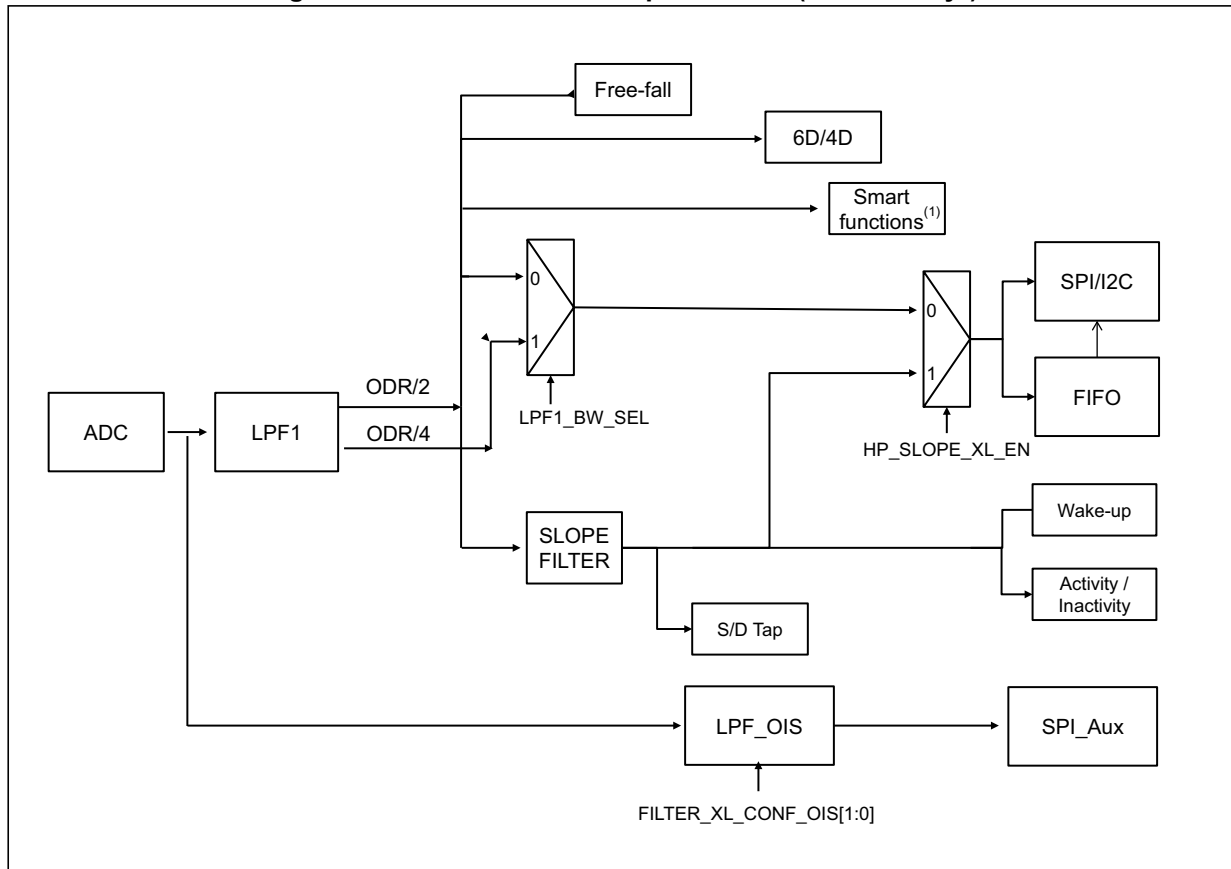
Figure 9. Accelerometer composite filter (for Modes 1/2 and Mode 3*)



1. Pedometer, step detector and step counter, significant motion and tilt functions.

Note: * Mode 3 is available only if Mode4_EN = 0 and OIS_EN_SPI2 = 1 in [CTRL1_OIS \(70h\)](#).

Figure 10. Accelerometer composite filter (Mode 4 only*)



1. Pedometer, step detector and step counter, significant motion and tilt functions.

Note: *Mode 4 is enabled when `Mode4_EN = 1` and `OIS_EN_SPI2 = 1` in `CTRL1_OIS (70h)`.

5.5 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The LSM6DSM embeds 4 kbytes data FIFO to store the following data:

- gyroscope
- accelerometer
- external sensors
- step counter and timestamp
- temperature

Writing data in the FIFO can be configured to be triggered by the:

- accelerometer/gyroscope data-ready signal; in which case the ODR must be lower than or equal to both the accelerometer and gyroscope ODRs;
- sensor hub data-ready signal;
- step detection signal.

In addition, each data can be stored at a decimated data rate compared to FIFO ODR and it is configurable by the user, setting the [FIFO_CTRL3 \(08h\)](#) and [FIFO_CTRL4 \(09h\)](#) registers. The available decimation factors are 2, 3, 4, 8, 16, 32.

The programmable FIFO threshold can be set in [FIFO_CTRL1 \(06h\)](#) and [FIFO_CTRL2 \(07h\)](#) using the FTH [10:0] bits.

To monitor the FIFO status, dedicated registers ([FIFO_STATUS1 \(3Ah\)](#), [FIFO_STATUS2 \(3Bh\)](#), [FIFO_STATUS3 \(3Ch\)](#), [FIFO_STATUS4 \(3Dh\)](#)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO threshold status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pads of these status events, the configuration can be set in [INT1_CTRL \(0Dh\)](#) and [INT2_CTRL \(0Eh\)](#).

The FIFO buffer can be configured according to five different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode

Each mode is selected by the FIFO_MODE_[2:0] bits in the [FIFO_CTRL5 \(0Ah\)](#) register. To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

5.5.1 Bypass mode

In Bypass mode ([FIFO_CTRL5 \(0Ah\)](#) (FIFO_MODE_[2:0] = 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

5.5.2 FIFO mode

In FIFO mode (*FIFO_CTRL5 (0Ah)* (FIFO_MODE_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, Bypass mode should be selected by writing *FIFO_CTRL5 (0Ah)* (FIFO_MODE_[2:0]) to '000'. After this reset command, it is possible to restart FIFO mode by writing *FIFO_CTRL5 (0Ah)* (FIFO_MODE_[2:0]) to '001'.

FIFO buffer memorizes up to 4096 samples of 16 bits each but the depth of the FIFO can be resized by setting the FTH [10:0] bits in *FIFO_CTRL1 (06h)* and *FIFO_CTRL2 (07h)*. If the STOP_ON_FTH bit in *FIFO_CTRL4 (09h)* is set to '1', FIFO depth is limited up to FTH [10:0] bits in *FIFO_CTRL1 (06h)* and *FIFO_CTRL2 (07h)*.

5.5.3 Continuous mode

Continuous mode (*FIFO_CTRL5 (0Ah)* (FIFO_MODE_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag *FIFO_STATUS2 (3Bh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_CTRL1 (06h)* and *FIFO_CTRL2 (07h)*(FTH [10:0]).

It is possible to route *FIFO_STATUS2 (3Bh)* (FTH) to the INT1 pin by writing in register *INT1_CTRL (0Dh)* (INT1_FTH) = '1' or to the INT2 pin by writing in register *INT2_CTRL (0Eh)* (INT2_FTH) = '1'.

A full-flag interrupt can be enabled, *INT1_CTRL (0Dh)* (INT_FULL_FLAG) = '1', in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the OVER_RUN flag in *FIFO_STATUS2 (3Bh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO_STATUS1 (3Ah)* and *FIFO_STATUS2 (3Bh)* (DIFF_FIFO [10:0]).

5.5.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO_CTRL5 (0Ah)* (FIFO_MODE_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt registers *FUNC_SRC1 (53h)*, *TAP_SRC (1Ch)*, *WAKE_UP_SRC (1Bh)* and *D6D_SRC (1Dh)*.

When the selected trigger bit is equal to '1', FIFO operates in FIFO mode.

When the selected trigger bit is equal to '0', FIFO operates in Continuous mode.

5.5.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL5 (0Ah)* (FIFO_MODE_[2:0] = '100'), data measurement storage inside FIFO operates in Continuous mode when selected triggers in one of the following interrupt registers *FUNC_SRC1 (53h)*, *TAP_SRC (1Ch)*, *WAKE_UP_SRC (1Bh)* and *D6D_SRC (1Dh)* are equal to '1', otherwise FIFO content is reset (Bypass mode).

5.5.6 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers (*FIFO_DATA_OUT_L (3Eh)* and *FIFO_DATA_OUT_H (3Fh)*) and each FIFO sample is composed of 16 bits.

All FIFO status registers (*FIFO_STATUS1 (3Ah)*, *FIFO_STATUS2 (3Bh)*, *FIFO_STATUS3 (3Ch)*, *FIFO_STATUS4 (3Dh)*) can be read at the start of a reading operation, minimizing the intervention of the application processor.

Saving data in the FIFO buffer is organized in four FIFO data sets consisting of 6 bytes each:

The 1st FIFO data set is reserved for gyroscope data;

The 2nd FIFO data set is reserved for accelerometer data;

The 3rd FIFO data set is reserved for the external sensor data stored in the registers from *SENSORHUB1_REG (2Eh)* to *SENSORHUB6_REG (33h)*;

The 4th FIFO data set can be alternately associated to the external sensor data stored in the registers from *SENSORHUB7_REG (34h)* to *SENSORHUB12_REG (39h)*, to the step counter and timestamp info, or to the temperature sensor data.

6 Digital interfaces

6.1 I²C/SPI interface

The registers embedded inside the LSM6DSM may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped onto the same pins. To select/exploit the I²C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 10. Serial interface pin description

| Pin name | Pin description |
|-------------|---|
| CS | SPI enable I ² C/SPI mode selection (1: SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled) |
| SCL/SPC | I ² C Serial Clock (SCL) SPI Serial Port Clock (SPC) |
| SDA/SDI/SDO | I ² C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO) |
| SDO/SA0 | SPI Serial Data Output (SDO) I ² C less significant bit of the device address |

6.2 Master I²C

If the LSM6DSM is configured in Mode 2, a master I²C line is available. The master serial interface is mapped in the following dedicated pins.

Table 11. Master I²C pin details

| Pin name | Pin description |
|----------|---|
| MSCL | I ² C serial clock master |
| MSDA | I ² C serial data master |
| MDRDY | I ² C master external synchronization signal |

6.3 Auxiliary SPI

If LSM6DSM is configured in Mode 3, the auxiliary SPI is available. The auxiliary SPI interface is mapped in the following dedicated pins.

Table 12. Auxiliary SPI pin details

| Pin name | Pin description |
|----------|--|
| OCS_Aux | Auxiliary SPI 3/4-wire enable |
| SDx | Auxiliary SPI 3/4-wire data input (SDI_Aux) and SPI 3-wire data output (SDO_Aux) |
| SCx | Auxiliary SPI 3/4-wire interface serial port clock |
| SDO_Aux | SPI serial data |

6.4 I²C serial interface

The LSM6DSM I²C is a bus slave. The I²C is employed to write the data to the registers, whose content can also be read back.

The relevant I²C terminology is provided in the table below.

Table 13. I²C terminology

| Term | Description |
|-------------|--|
| Transmitter | The device which sends data to the bus |
| Receiver | The device which receives data from the bus |
| Master | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave | The device addressed by the master |

There are two signals associated with the I²C bus: the serial clock line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I²C interface is implemented with fast mode (400 kHz) I²C standards as well as with the standard mode.

In order to disable the I²C block, (I2C_disable) = 1 must be written in [CTRL4_C \(13h\)](#).

6.4.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave Address (SAD) associated to the LSM6DSM is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is '1' (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is '0' (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM6DSM behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The increment of the address is configured by the [CTRL3_C \(12h\)](#) (IF_INC).

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. [Table 14](#) explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 14. SAD+Read/Write patterns

| Command | SAD[6:1] | SAD[0] = SA0 | R/W | SAD+R/W |
|---------|----------|--------------|-----|----------------|
| Read | 110101 | 0 | 1 | 11010101 (D5h) |
| Write | 110101 | 0 | 0 | 11010100 (D4h) |
| Read | 110101 | 1 | 1 | 11010111 (D7h) |
| Write | 110101 | 1 | 0 | 11010110 (D6h) |

Table 15. Transfer when master is writing one byte to slave

| | | | | | | | | |
|--------|----|---------|-----|-----|-----|------|-----|----|
| Master | ST | SAD + W | | SUB | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | |

Table 16. Transfer when master is writing multiple bytes to slave

| | | | | | | | | | | |
|--------|----|---------|-----|-----|-----|------|-----|------|-----|----|
| Master | ST | SAD + W | | SUB | | DATA | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | | SAK | |

Table 17. Transfer when master is receiving (reading) one byte of data from slave

| | | | | | | | | | | | |
|--------|----|---------|-----|-----|-----|----|---------|-----|------|------|----|
| Master | ST | SAD + W | | SUB | | SR | SAD + R | | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | |

Table 18. Transfer when master is receiving (reading) multiple bytes of data from slave

| | | | | | | | | | | | | | | | |
|--------|----|-------|-----|-----|-----|----|-------|-----|------|-----|------|-----|------|------|----|
| Master | ST | SAD+W | | SUB | | SR | SAD+R | | | MAK | | MAK | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | DATA | | DATA | | |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

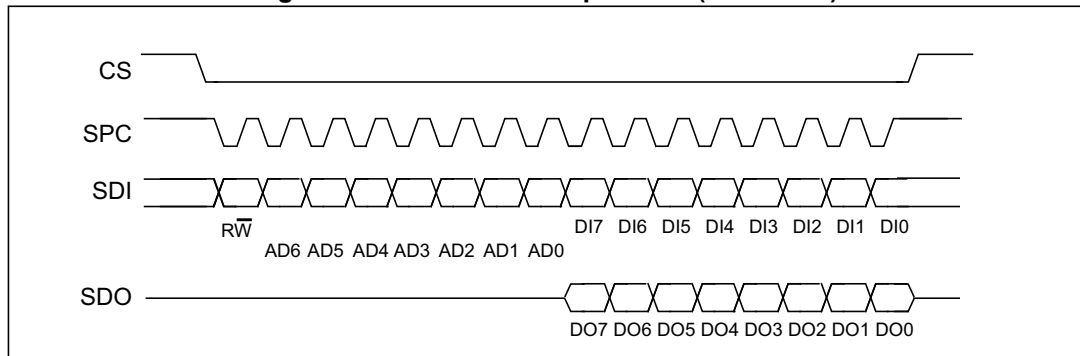
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

6.5 SPI bus interface

The LSM6DSM SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface communicates to the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 11. Read and write protocol (in mode 3)



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: \overline{RW} bit. When 0, the data $DI(7:0)$ is written into the device. When 1, the data $DO(7:0)$ from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address $AD(6:0)$. This is the address field of the indexed register.

bit 8-15: data $DI(7:0)$ (write mode). This is the data that is written into the device (MSb first).

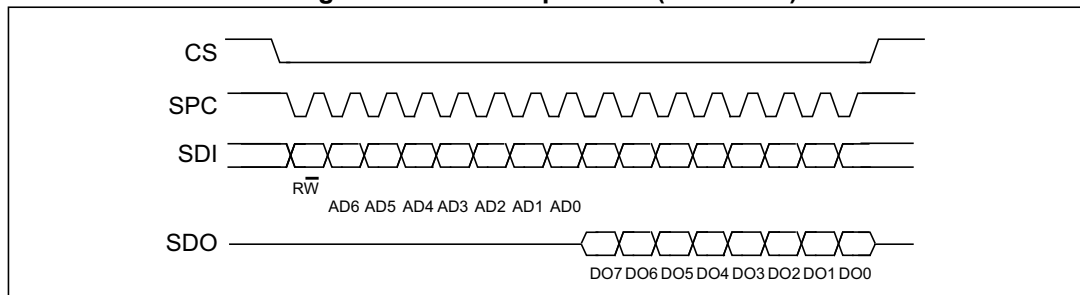
bit 8-15: data $DO(7:0)$ (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the [CTRL3_C \(12h\)](#) (IF_INC) bit is '0', the address used to read/write data remains the same for every block. When the [CTRL3_C \(12h\)](#) (IF_INC) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.5.1 SPI read

Figure 12. SPI read protocol (in mode 3)



The SPI Read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

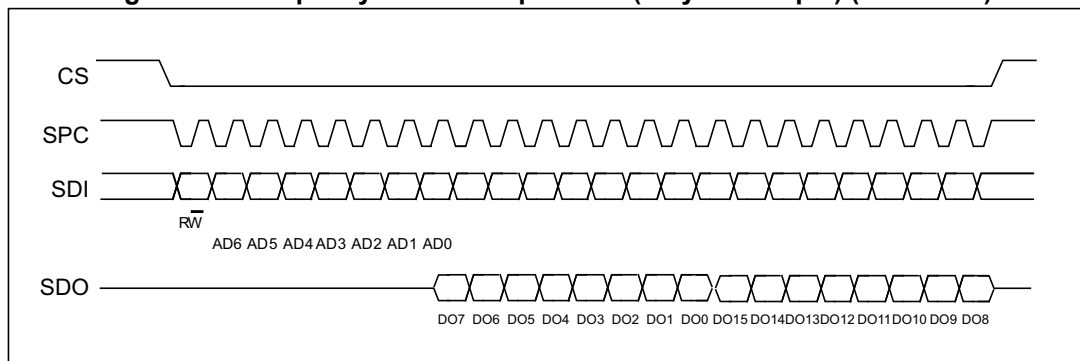
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

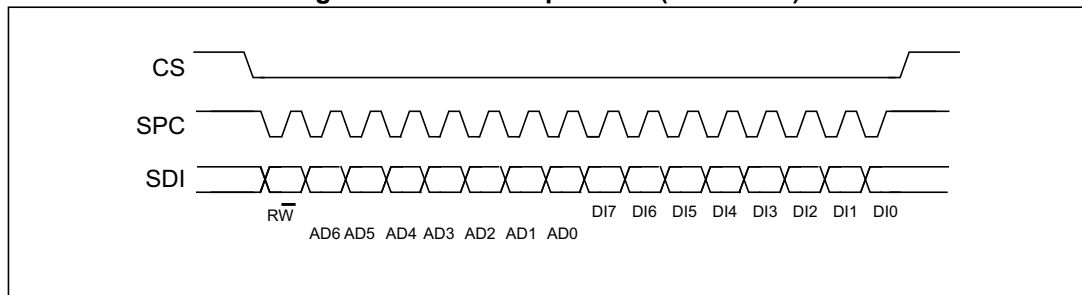
bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 13. Multiple byte SPI read protocol (2-byte example) (in mode 3)



6.5.2 SPI write

Figure 14. SPI write protocol (in mode 3)



The SPI Write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

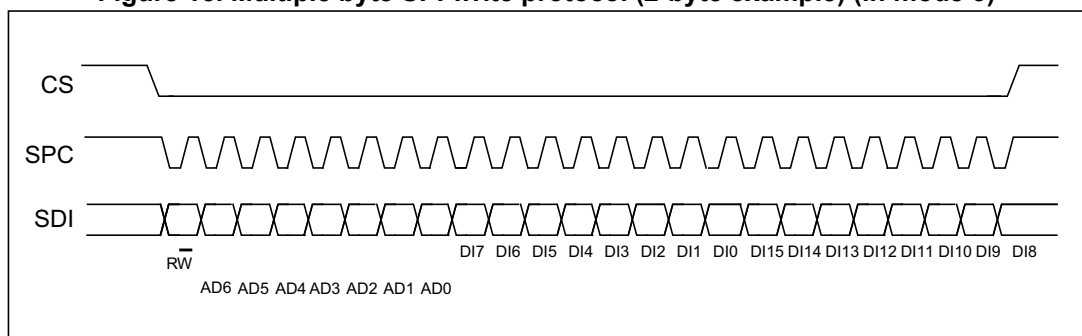
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

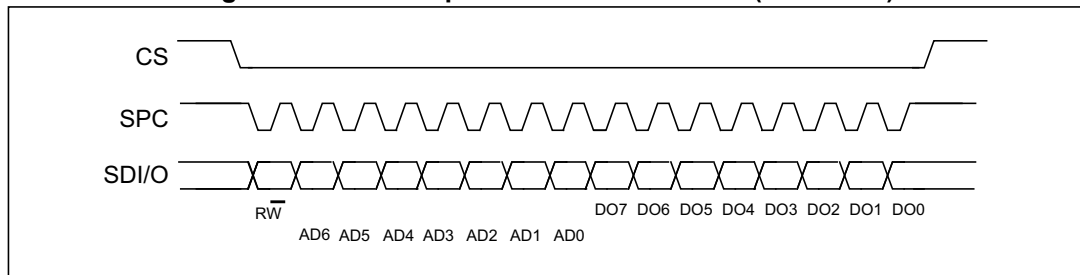
Figure 15. Multiple byte SPI write protocol (2-byte example) (in mode 3)



6.5.3 SPI read in 3-wire mode

A 3-wire mode is entered by setting the *CTRL3_C (12h)* (SIM) bit equal to '1' (SPI serial interface mode selection).

Figure 16. SPI read protocol in 3-wire mode (in mode 3)



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

7.1 LSM6DSM electrical connections in Mode 1

Pin Configuration:

- SDA:** Serial Data Out/In (I2C)
- SCL:** Serial Clock (I2C)
- CS:** Chip Select (SPI)
- SDO/SA0:** Serial Data Out/Slave Address (SPI)
- SDx:** Serial Data In/Out (SPI)
- SCx:** Serial Clock (SPI)
- INT1:** Interrupt 1
- NC⁽¹⁾:** No Connection
- INT2:** Interrupt 2
- VDD:** Digital Supply Voltage
- VDDIO:** I/O Supply Voltage
- GND:** Ground

I2C Configuration:

The I2C configuration shows the SDA and SCL lines connected to the HOST. The SDA line is bidirectional, and the SCL line is unidirectional. The pull-up resistors R_{pu} are connected to the VDD_IO supply voltage.

Mode 1:

The diagram shows the HOST connected to the LSM6DSM via I2C/SPI (3/4-wire) interface. The LSM6DSM is configured in Mode 1.

Capacitors:

- C1:** 100 nF capacitor connected to VDD and GND.
- C2:** 100 nF capacitor connected to VDDIO and GND.

Notes:

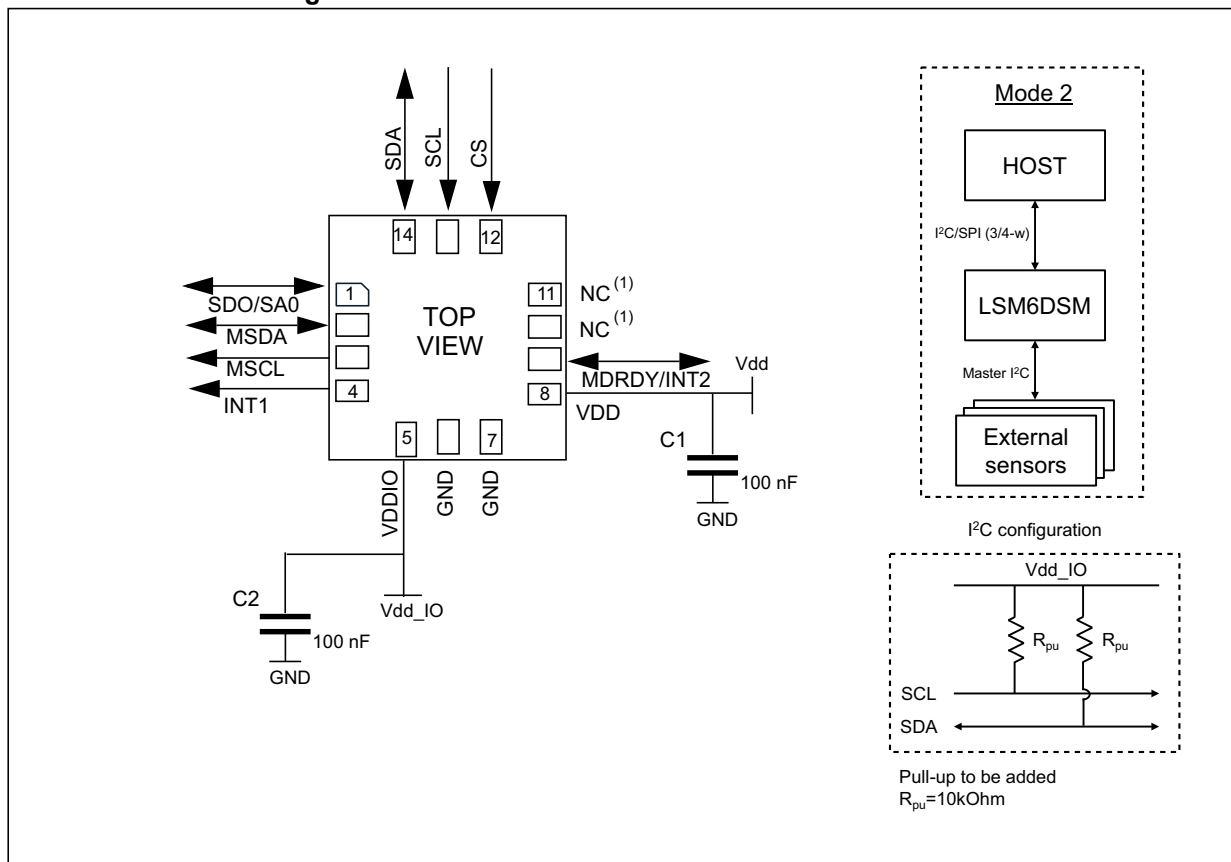
- ⁽¹⁾ NC: No Connection

- The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C interface.

7.2 LSM6DSM electrical connections in Mode 2

Figure 18. LSM6DSM electrical connections in Mode 2



1. Leave pin electrically unconnected and soldered to PCB.

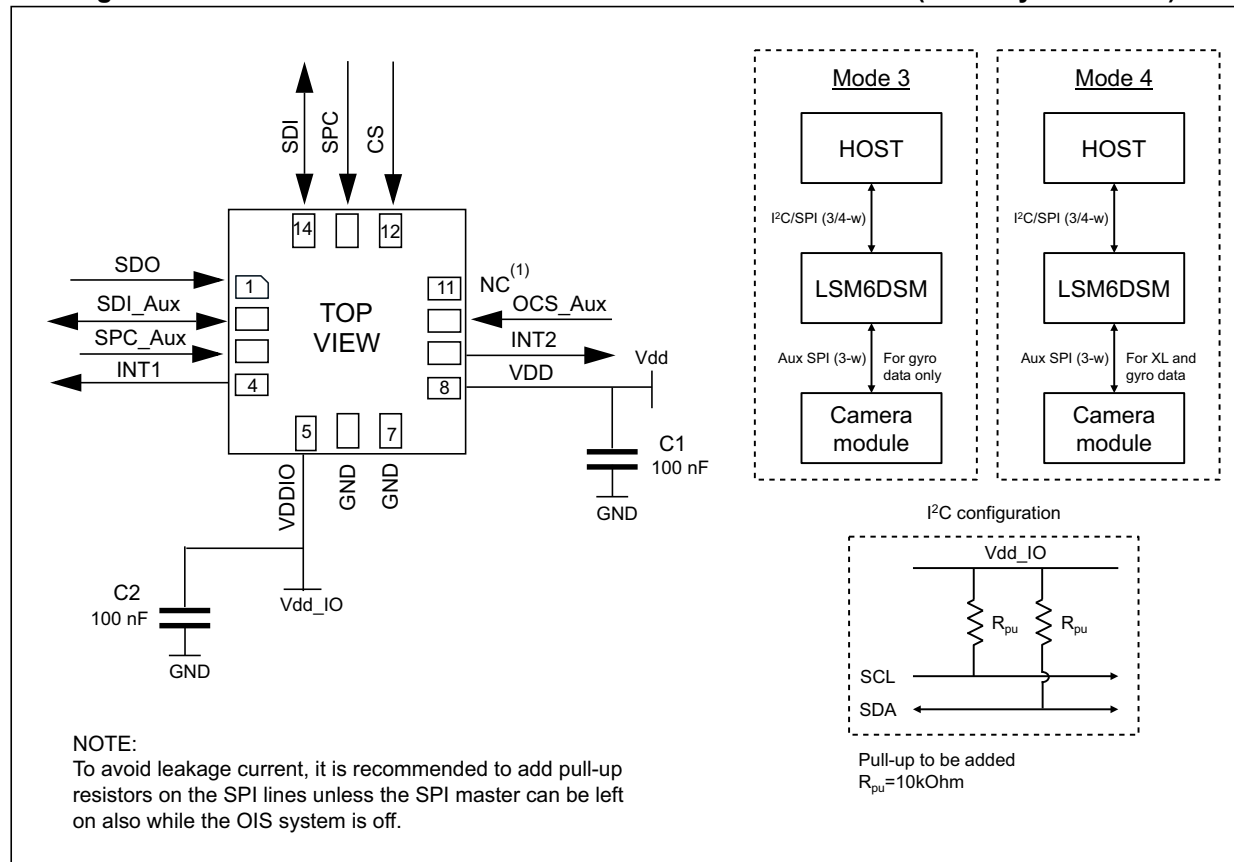
The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C interface.

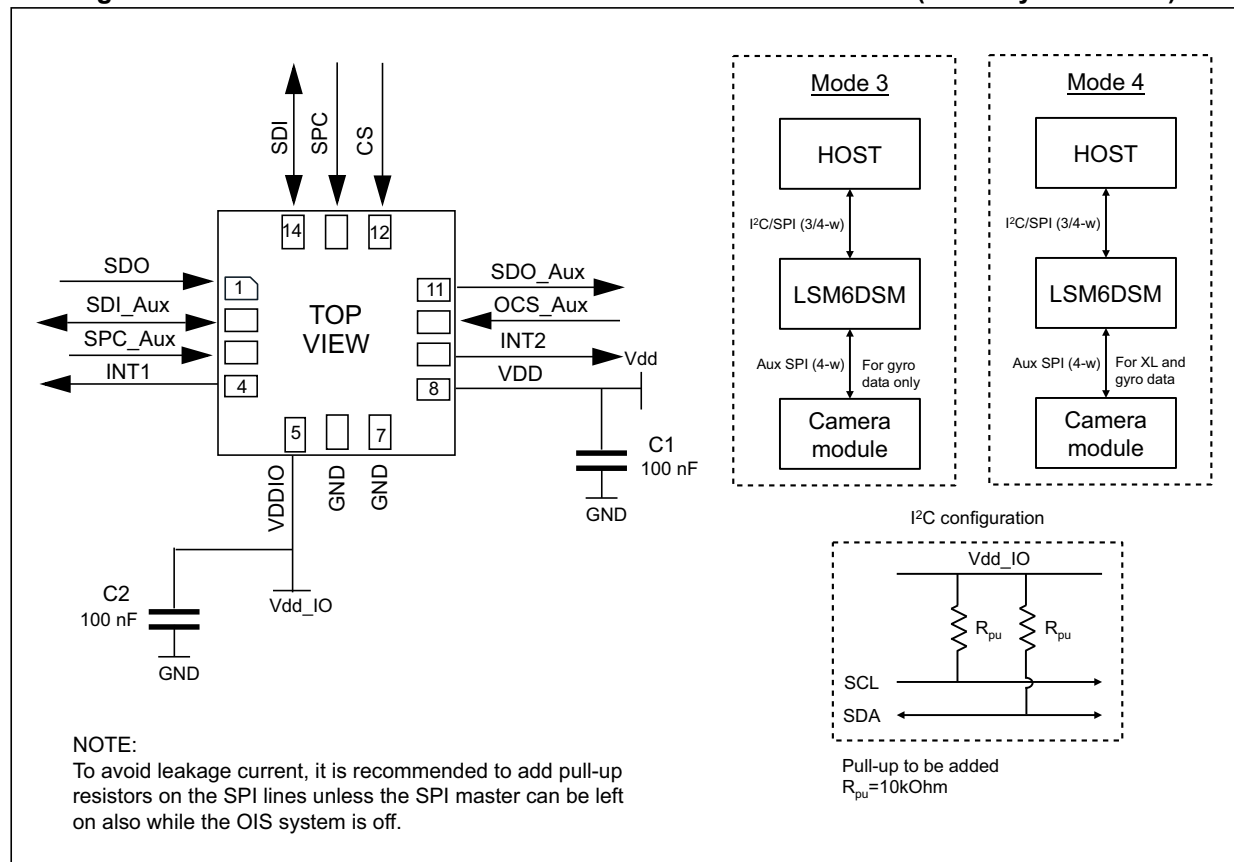
7.3 LSM6DSM electrical connections in Mode 3 and Mode 4

Figure 19. LSM6DSM electrical connections in Mode 3 and Mode 4 (auxiliary 3-wire SPI)



1. Leave pin electrically unconnected and soldered to PCB.

Figure 20. LSM6DSM electrical connections in Mode 3 and Mode 4 (auxiliary 4-wire SPI)



The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C interface.

Table 19. Internal pin status

| pin# | Name | Mode 1 function | Mode 2 function | Mode 3 / Mode 4 function | Pin status Mode 1 | Pin status Mode 2 | Pin status Mode 3/4 |
|------|--------|--|--|--|---|---|---|
| 1 | SDO | SPI 4-wire interface serial data output (SDO) | SPI 4-wire interface serial data output (SDO) | SPI 4-wire interface serial data output (SDO) | Default: Input without pull-up. Pull-up is enabled if bit SIM = 1 (SPI 3-wire) in reg 12h. | Default: Input without pull-up. Pull-up is enabled if bit SIM = 1 (SPI 3-wire) in reg 12h. | Default: Input without pull-up. Pull-up is enabled if bit SIM = 1 (SPI 3-wire) in reg 12h. |
| | SA0 | I ² C least significant bit of the device address (SA0) | I ² C least significant bit of the device address (SA0) | I ² C least significant bit of the device address (SA0) | | | |
| 2 | SDx | Connect to VDDIO or GND | I ² C serial data master (MSDA) | Auxiliary SPI 3/4-wire interface serial data input (SDI) and SPI 3-wire serial data output (SDO) | Default: input without pull-up. Pull-up is enabled if bit PULL_UP_EN = 1 in reg 1Ah. | Default: input without pull-up. Pull-up is enabled if bit PULL_UP_EN = 1 in reg 1Ah. | Default: input without pull-up. Pull-up is enabled if bit PULL_UP_EN = 1 in reg 1Ah. |
| 3 | SCx | Connect to VDDIO or GND | I ² C serial clock master (MSCL) | Auxiliary SPI 3/4-wire interface serial port clock (SPC_Aux) | Default: input without pull-up. Pull-up is enabled if bit PULL_UP_EN = 1 in reg 1Ah. | Default: input without pull-up. Pull-up is enabled if bit PULL_UP_EN = 1 in reg 1Ah. | Default: input without pull-up. Pull-up is enabled if bit PULL_UP_EN = 1 in reg 1Ah. |
| 4 | INT1 | Programmable interrupt 1 | Programmable interrupt 1 | Programmable interrupt 1 | Default: Output forced to ground | Default: Output forced to ground | Default: Output forced to ground |
| 5 | Vdd_IO | Power supply for I/O pins | Power supply for I/O pins | Power supply for I/O pins | | | |
| 6 | GND | 0 V supply | 0 V supply | 0 V supply | | | |
| 7 | GND | 0 V supply | 0 V supply | 0 V supply | | | |
| 8 | Vdd | Power supply | Power supply | Power supply | | | |
| 9 | INT2 | Programmable interrupt 2 (INT2) / Data enabled (DEN) | Programmable interrupt 2 (INT2) / Data enabled (DEN) / I ² C master external synchronization signal (MDRDY) | Programmable interrupt 2 (INT2) / Data enabled (DEN) | Default: Output forced to ground | Default: Output forced to ground | Default: Output forced to ground |

Table 19. Internal pin status (continued)

| pin# | Name | Mode 1 function | Mode 2 function | Mode 3 / Mode 4 function | Pin status Mode 1 | Pin status Mode 2 | Pin status Mode 3/4 |
|------|---------|---|---|---|--|--|--|
| 10 | OCS_Aux | Leave unconnected | Leave unconnected | Auxiliary SPI 3/4-wire interface enabled | Default: Input with pull-up. (See note below to disable pull-up) | Default: Input with pull-up. (See note below to disable pull-up) | Input without pull-up |
| 11 | SDO_Aux | Connect to VDDIO or leave unconnected | Connect to VDDIO or leave unconnected | Auxiliary SPI 3-wire interface: leave unconnected / Auxiliary SPI 4-wire interface: serial data output (SDO_Aux) | Default: Input with pull-up. (See note below to disable pull-up) | Default: Input with pull-up. (See note below to disable pull-up) | Default: Input without pull-up. Pull-up is enabled if bit SIM_OIS =1 (Aux_SPI 3-wire) in reg 70h. |
| 12 | CS | I ² C/SPI mode selection (1:SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled) | I ² C/SPI mode selection (1:SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled) | I ² C/SPI mode selection (1:SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled) | Default: Input with pull-up. Pull-up is disabled if bit I2C_disable = 1 in reg 13h. | Default: Input with pull-up. Pull-up is disabled if bit I2C_disable = 1 in reg 13h. | Default: Input with pull-up. Pull-up is disabled if bit I2C_disable = 1 in reg 13h. |
| 13 | SCL | I ² C serial clock (SCL) / SPI serial port clock (SPC) | I ² C serial clock (SCL) / SPI serial port clock (SPC) | I ² C serial clock (SCL) / SPI serial port clock (SPC) | Input without pull-up | Input without pull-up | Input without pull-up |
| 14 | SDA | I ² C serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO) | I ² C serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO) | I ² C serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO) | Input without pull-up | Input without pull-up | Input without pull-up |

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on VDDIO.

Note: *The procedure to disable the pull-up on pins 10-11 is as follows:*

1. *AP side: write 80h in register at address 00h*
2. *AP side: write 01h in register at address 05h (disable the pull-up on pins 10 and 11 of LSM6DSM)*
3. *AP side: write 00h in register at address 00h*

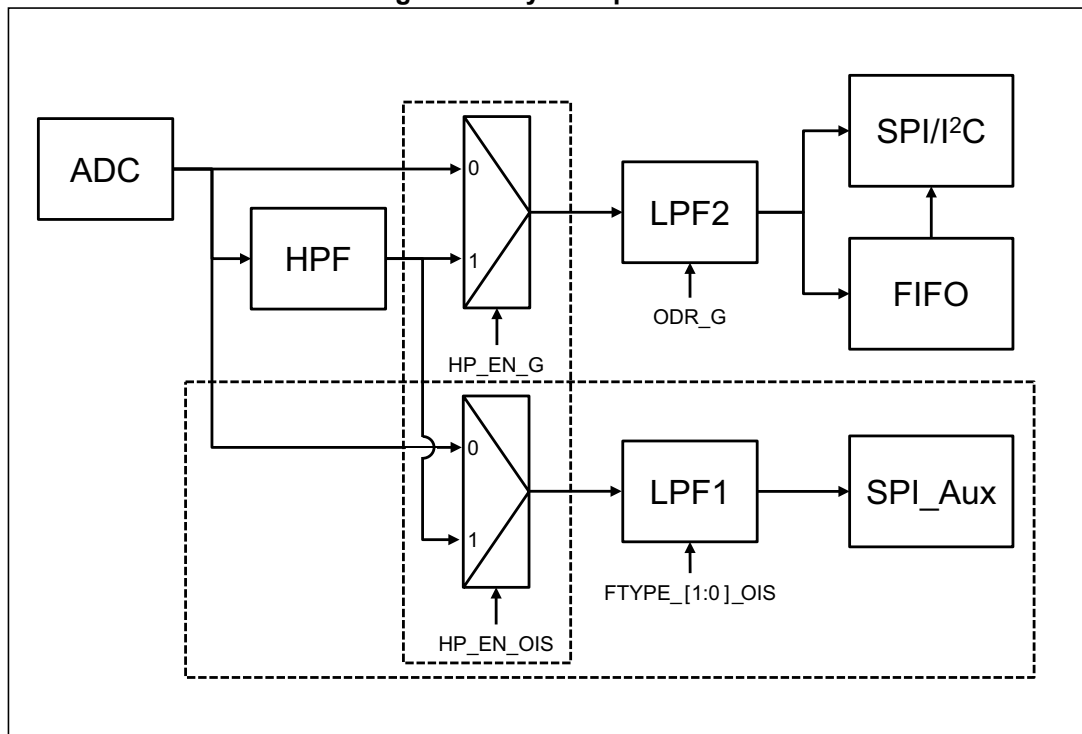
8 Auxiliary SPI configurations

When the LSM6DSM is configured in Mode 3 and Mode 4, the auxiliary SPI can be connected to a camera module for OIS/EIS support. In this interface, the SPI can write only to the dedicated registers *INT_OIS (6Fh)*, *CTRL1_OIS (70h)*, *CTRL2_OIS (71h)*, *CTRL3_OIS (72h)*.

8.1 Gyroscope filtering

The gyroscope filtering chain is illustrated in the following figure.

Figure 21. Gyroscope chain



Note: *HP_EN_OIS* is active to select HPF on the auxiliary SPI chain only if HPF is not already used in the primary interface.

The auxiliary interface needs to be enabled in *CTRL1_OIS (70h)*.

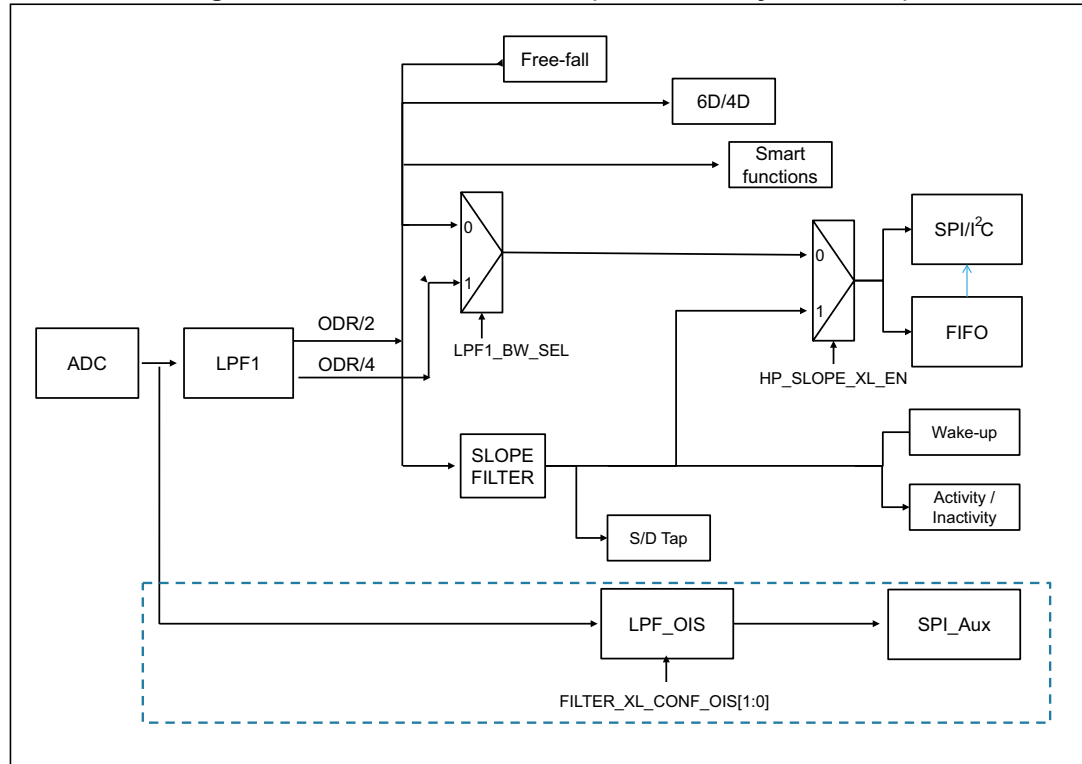
Gyroscope output values are in registers 22h to 27h with selected full scale (FS[1:0]_G_OIS bit in *CTRL1_OIS (70h)*) and ODR at 6.66 kHz.

LPF1 configuration depends on the setting of the FTYPE_[1:0]_OIS bit in register *CTRL2_OIS (71h)*.

8.2 Accelerometer filtering

Accelerometer filtering is available only when Mode 4 is enabled.

Figure 22. Accelerometer chain (available only in Mode 4)



Accelerometer output values are in registers *OUTX_L_XL* (28h) through *OUTZ_H_XL* (2Dh) and ODR at 6.66 kHz.

8.2.1 Accelerometer full scale set from primary interface

If the SPI/I²C primary interface is used, the full-scale setting has been configured by the primary interface and *CTRL3_OIS* (72h) must be set to the same full-scale setting of the primary interface.

8.2.2 Accelerometer full scale set from auxiliary SPI

If the configuration uses only the auxiliary SPI, the full scale can be set using the FS[1:0]_XL_OIS bits in *CTRL3_OIS* (72h). The configuration of the low-pass filter depends on the setting of the FILTER_XL_CONF_OIS[1:0] bits in register *CTRL3_OIS* (72h).

9 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

Table 20. Registers address map

| Name | Type | Register address | | Default | Comment |
|------------------------|------|------------------|-----------|----------|---|
| | | Hex | Binary | | |
| RESERVED | - | 00 | 00000000 | - | Reserved |
| FUNC_CFG_ACCESS | r/w | 01 | 00000001 | 00000000 | Embedded functions configuration register |
| RESERVED | - | 02 | 00000010 | - | Reserved |
| RESERVED | - | 03 | 00000011 | - | Reserved |
| SENSOR_SYNC_TIME_FRAME | r/w | 04 | 00000100 | 00000000 | Sensor sync configuration register |
| SENSOR_SYNC_RES_RATIO | r/w | 05 | 00000101 | 00000000 | |
| FIFO_CTRL1 | r/w | 06 | 00000110 | 00000000 | FIFO configuration registers |
| FIFO_CTRL2 | r/w | 07 | 00000111 | 00000000 | |
| FIFO_CTRL3 | r/w | 08 | 00001000 | 00000000 | |
| FIFO_CTRL4 | r/w | 09 | 00001001 | 00000000 | |
| FIFO_CTRL5 | r/w | 0A | 00001010 | 00000000 | |
| DRDY_PULSE_CFG | r/w | 0B | 00001011 | 00000000 | |
| RESERVED | - | 0C | 00001100 | - | Reserved |
| INT1_CTRL | r/w | 0D | 00001101 | 00000000 | INT1 pin control |
| INT2_CTRL | r/w | 0E | 00001110 | 00000000 | INT2 pin control |
| WHO_AM_I | r | 0F | 00001111 | 01101010 | Who I am ID |
| CTRL1_XL | r/w | 10 | 00010000 | 00000000 | Accelerometer and gyroscope control registers |
| CTRL2_G | r/w | 11 | 00010001 | 00000000 | |
| CTRL3_C | r/w | 12 | 00010010 | 00000100 | |
| CTRL4_C | r/w | 13 | 00010011 | 00000000 | |
| CTRL5_C | r/w | 14 | 00010100 | 00000000 | |
| CTRL6_C | r/w | 15 | 00010101 | 00000000 | |
| CTRL7_G | r/w | 16 | 00010110 | 00000000 | |
| CTRL8_XL | r/w | 17 | 0001 0111 | 00000000 | |
| CTRL9_XL | r/w | 18 | 00011000 | 11100000 | |
| CTRL10_C | r/w | 19 | 00011001 | 00000000 | |

Table 20. Registers address map (continued)

| Name | Type | Register address | | Default | Comment |
|---|------|------------------|----------|----------|--|
| | | Hex | Binary | | |
| MASTER_CONFIG | r/w | 1A | 00011010 | 00000000 | I ² C master configuration register |
| WAKE_UP_SRC | r | 1B | 00011011 | output | Interrupt registers |
| TAP_SRC | r | 1C | 00011100 | output | |
| D6D_SRC | r | 1D | 00011101 | output | |
| STATUS_REG ⁽¹⁾ / STATUS_SPIAux ⁽²⁾ | r | 1E | 00011110 | output | Status data register for user interface and OIS data |
| RESERVED | - | 1F | 00011111 | - | Reserved |
| OUT_TEMP_L | r | 20 | 00100000 | output | Temperature output data registers |
| OUT_TEMP_H | r | 21 | 00100001 | output | |
| OUTX_L_G | r | 22 | 00100010 | output | Gyroscope output registers for user interface and OIS data |
| OUTX_H_G | r | 23 | 00100011 | output | |
| OUTY_L_G | r | 24 | 00100100 | output | |
| OUTY_H_G | r | 25 | 00100101 | output | |
| OUTZ_L_G | r | 26 | 00100110 | output | |
| OUTZ_H_G | r | 27 | 00100111 | output | |
| OUTX_L_XL | r | 28 | 00101000 | output | Accelerometer output registers |
| OUTX_H_XL | r | 29 | 00101001 | output | |
| OUTY_L_XL | r | 2A | 00101010 | output | |
| OUTY_H_XL | r | 2B | 00101011 | output | |
| OUTZ_L_XL | r | 2C | 00101100 | output | |
| OUTZ_H_XL | r | 2D | 00101101 | output | |
| SENSORHUB1_REG | r | 2E | 00101110 | output | Sensor hub output registers |
| SENSORHUB2_REG | r | 2F | 00101111 | output | |
| SENSORHUB3_REG | r | 30 | 00110000 | output | |
| SENSORHUB4_REG | r | 31 | 00110001 | output | |
| SENSORHUB5_REG | r | 32 | 00110010 | output | |
| SENSORHUB6_REG | r | 33 | 00110011 | output | |
| SENSORHUB7_REG | r | 34 | 00110100 | output | |
| SENSORHUB8_REG | r | 35 | 00110101 | output | |
| SENSORHUB9_REG | r | 36 | 00110110 | output | |
| SENSORHUB10_REG | r | 37 | 00110111 | output | |
| SENSORHUB11_REG | r | 38 | 00111000 | output | |
| SENSORHUB12_REG | r | 39 | 00111001 | output | |

Table 20. Registers address map (continued)

| Name | Type | Register address | | Default | Comment |
|------------------|------|------------------|-----------|----------|----------------------------------|
| | | Hex | Binary | | |
| FIFO_STATUS1 | r | 3A | 00111010 | output | FIFO status registers |
| FIFO_STATUS2 | r | 3B | 00111011 | output | |
| FIFO_STATUS3 | r | 3C | 00111100 | output | |
| FIFO_STATUS4 | r | 3D | 00111101 | output | |
| FIFO_DATA_OUT_L | r | 3E | 00111110 | output | FIFO data output registers |
| FIFO_DATA_OUT_H | r | 3F | 00111111 | output | |
| TIMESTAMP0_REG | r | 40 | 01000000 | output | Timestamp output registers |
| TIMESTAMP1_REG | r | 41 | 01000001 | output | |
| TIMESTAMP2_REG | r/w | 42 | 01000010 | output | |
| RESERVED | - | 43-48 | | - | Reserved |
| STEP_TIMESTAMP_L | r | 49 | 0100 1001 | output | Step counter timestamp registers |
| STEP_TIMESTAMP_H | r | 4A | 0100 1010 | output | |
| STEP_COUNTER_L | r | 4B | 01001011 | output | Step counter output registers |
| STEP_COUNTER_H | r | 4C | 01001100 | output | |
| SENSORHUB13_REG | r | 4D | 01001101 | output | Sensor hub output registers |
| SENSORHUB14_REG | r | 4E | 01001110 | output | |
| SENSORHUB15_REG | r | 4F | 01001111 | output | |
| SENSORHUB16_REG | r | 50 | 01010000 | output | |
| SENSORHUB17_REG | r | 51 | 01010001 | output | |
| SENSORHUB18_REG | r | 52 | 01010010 | output | |
| FUNC_SRC1 | r | 53 | 01010011 | output | Interrupt registers |
| FUNC_SRC2 | r | 54 | 01010100 | output | |
| WRIST_TILT_IA | r | 55 | 01010101 | output | Interrupt register |
| RESERVED | - | 56-57 | | - | Reserved |
| TAP_CFG | r/w | 58 | 01011000 | 00000000 | Interrupt registers |
| TAP_THS_6D | r/w | 59 | 01011001 | 00000000 | |
| INT_DUR2 | r/w | 5A | 01011010 | 00000000 | |
| WAKE_UP_THS | r/w | 5B | 01011011 | 00000000 | |
| WAKE_UP_DUR | r/w | 5C | 01011100 | 00000000 | |
| FREE_FALL | r/w | 5D | 01011101 | 00000000 | |
| MD1_CFG | r/w | 5E | 01011110 | 00000000 | |
| MD2_CFG | r/w | 5F | 01011111 | 00000000 | |
| MASTER_CMD_CODE | r/w | 60 | 01100000 | 00000000 | |

Table 20. Registers address map (continued)

| Name | Type | Register address | | Default | Comment |
|--------------------------|------|------------------|-----------|----------|---|
| | | Hex | Binary | | |
| SENS_SYNC_SPI_ERROR_CODE | r/w | 61 | 0110 0001 | 00000000 | |
| RESERVED | - | 62-65 | | - | Reserved |
| OUT_MAG_RAW_X_L | r | 66 | 01100110 | output | External magnetometer raw data output registers |
| OUT_MAG_RAW_X_H | r | 67 | 01100111 | output | |
| OUT_MAG_RAW_Y_L | r | 68 | 01101000 | output | |
| OUT_MAG_RAW_Y_H | r | 69 | 01101001 | output | |
| OUT_MAG_RAW_Z_L | r | 6A | 01101010 | output | |
| OUT_MAG_RAW_Z_H | r | 6B | 01101011 | output | |
| RESERVED | - | 6C-6E | | - | Reserved |
| INT_OIS | r/w | 6F | 01101111 | 00000000 | |
| CTRL1_OIS | r/w | 70 | 01110000 | 00000000 | Control registers for OIS connection |
| CTRL2_OIS | r/w | 71 | 01110001 | 00000000 | |
| CTRL3_OIS | r/w | 72 | 01110010 | 00000000 | |
| X_OFS_USR | r/w | 73 | 01110011 | 00000000 | Accelerometer user offset correction |
| Y_OFS_USR | r/w | 74 | 01110100 | 00000000 | |
| Z_OFS_USR | r/w | 75 | 01110101 | 00000000 | |
| RESERVED | - | 76-7F | | - | Reserved |

1. This register status is read using the primary interface for user interface data.
2. This register status is read using the auxiliary SPI for OIS data.

10 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

10.1 FUNC_CFG_ACCESS (01h)

Enable embedded functions register (r/w).

Table 21. FUNC_CFG_ACCESS register

| | | | | | | | |
|-------------|------------------|---------------|------------------|------------------|------------------|------------------|------------------|
| FUNC_CFG_EN | 0 ⁽¹⁾ | FUNC_CFG_EN_B | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ |
|-------------|------------------|---------------|------------------|------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 22. FUNC_CFG_ACCESS register description

| | |
|---------------|--|
| FUNC_CFG_EN | Enable access to the embedded functions configuration registers bank A and B ⁽¹⁾ . Default value: 0. Refer to Table 23 . |
| FUNC_CFG_EN_B | Enable access to the embedded functions configuration register bank B ⁽¹⁾ . Default value: 0. Refer to Table 23 . |

1. The embedded functions configuration registers details are available in [Section 11: Embedded functions register mapping](#), [Section 12: Embedded functions registers description - Bank A](#), and [Section 13: Embedded functions registers description - Bank B](#).

Table 23. Configuration of embedded functions register banks

| FUNC_CFG_EN | FUNC_CFG_EN_B | Status of embedded register banks |
|-------------|---------------|-----------------------------------|
| 0 | 0 | Bank A and B disabled (default) |
| 0 | 1 | Forbidden |
| 1 | 0 | Bank A enabled |
| 1 | 1 | Bank B enabled |

10.2 SENSOR_SYNC_TIME_FRAME (04h)

Sensor synchronization time frame register (r/w).

Table 24. SENSOR_SYNC_TIME_FRAME register

| | | | | | | | |
|------------------|------------------|------------------|------------------|-------|-------|-------|-------|
| 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | TPH_3 | TPH_2 | TPH_1 | TPH_0 |
|------------------|------------------|------------------|------------------|-------|-------|-------|-------|

1. This bit must be set to '0' for the correct operation of the device.

Table 25. SENSOR_SYNC_TIME_FRAME register description

| | |
|------------|--|
| TPH_ [3:0] | Sensor synchronization time frame with the step of 500 ms and full range of 5 s. Unsigned 8-bit. Default value: 0000 0000 (sensor sync disabled) |
|------------|--|

10.3 SENSOR_SYNC_RES_RATIO (05h)

Sensor synchronization resolution ratio (r/w)

Table 26. SENSOR_SYNC_RES_RATIO register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------|------|
| 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | RR_1 | RR_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------|------|

1. This bit must be set to '0' for the correct operation of the device.

Table 27. SENSOR_SYNC_RES_RATIO register description

| | |
|----------|--|
| RR_[1:0] | Resolution ratio of error code for sensor synchronization: |
| | 00: SensorSync, Res_Ratio = 2-11 |
| | 01: SensorSync, Res_Ratio = 2-12 |
| | 10: SensorSync, Res_Ratio = 2-13 |
| | 11: SensorSync, Res_Ratio = 2-14 |

10.4 FIFO_CTRL1 (06h)

FIFO control register (r/w).

Table 28. FIFO_CTRL1 register

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| FTH_7 | FTH_6 | FTH_5 | FTH_4 | FTH_3 | FTH_2 | FTH_1 | FTH_0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

Table 29. FIFO_CTRL1 register description

| | |
|-----------|---|
| FTH_[7:0] | FIFO threshold level setting ⁽¹⁾ . Default value: 0000 0000. |
| | Watermark flag rises when the number of bytes written to FIFO after the next write is greater than or equal to the threshold level. |
| | Minimum resolution for the FIFO is 1 LSB = 2 bytes (1 word) in FIFO |

1. For a complete watermark threshold configuration, consider FTH_[10:8] in [FIFO_CTRL2 \(07h\)](#).

10.5 FIFO_CTRL2 (07h)

FIFO control register (r/w).

Table 30. FIFO_CTRL2 register

| | | | | | | | |
|--------------------|----------------------|------------------|------------------|--------------|-------|-------|-------|
| TIMER_PEDO_FIF0_EN | TIMER_PEDO_FIF0_DRDY | 0 ⁽¹⁾ | 0 ⁽¹⁾ | FIFO_TEMP_EN | FTH10 | FTH_9 | FTH_8 |
|--------------------|----------------------|------------------|------------------|--------------|-------|-------|-------|

1. This bit must be set to '0' for the correct operation of the device.

Table 31. FIFO_CTRL2 register description

| | |
|----------------------|--|
| TIMER_PEDO_FIF0_EN | Enable pedometer step counter and timestamp as 4 th FIFO data set. Default: 0 (0: disable step counter and timestamp data as 4 th FIFO data set; 1: enable step counter and timestamp data as 4 th FIFO data set) |
| TIMER_PEDO_FIF0_DRDY | FIFO write mode ⁽¹⁾ . Default: 0 (0: enable write in FIFO based on XL/Gyro data-ready; 1: enable write in FIFO at every step detected by step counter.) |
| FIFO_TEMP_EN | Enable the temperature data storage in FIFO. Default: 0. (0: temperature not included in FIFO; 1: temperature included in FIFO) |
| FTH_[10:8] | FIFO threshold level setting ⁽²⁾ . Default value: 0000 Watermark flag rises when the number of bytes written to FIFO after the next write is greater than or equal to the threshold level. Minimum resolution for the FIFO is 1LSB = 2 bytes (1 word) in FIFO |

1. This bit is effective if the DATA_VALID_SEL_FIF0 bit of the [MASTER_CONFIG \(1Ah\)](#) register is set to 0.
2. For a complete watermark threshold configuration, consider FTH_[7:0] in [FIFO_CTRL1 \(06h\)](#)

10.6 FIFO_CTRL3 (08h)

FIFO control register (r/w).

Table 32. FIFO_CTRL3 register

| | | | | | | | |
|------------------|------------------|----------------|----------------|----------------|--------------|--------------|--------------|
| 0 ⁽¹⁾ | 0 ⁽¹⁾ | DEC_FIFO_GYRO2 | DEC_FIFO_GYRO1 | DEC_FIFO_GYRO0 | DEC_FIFO_XL2 | DEC_FIFO_XL1 | DEC_FIFO_XL0 |
|------------------|------------------|----------------|----------------|----------------|--------------|--------------|--------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 33. FIFO_CTRL3 register description

| | |
|---------------------|---|
| DEC_FIFO_GYRO [2:0] | Gyro FIFO (first data set) decimation setting. Default: 000 For the configuration setting, refer to Table 34 . |
| DEC_FIFO_XL [2:0] | Accelerometer FIFO (second data set) decimation setting. Default: 000 For the configuration setting, refer to Table 35 . |

Table 34. Gyro FIFO decimation setting

| DEC_FIFO_GYRO [2:0] | Configuration |
|---------------------|---------------------------|
| 000 | Gyro sensor not in FIFO |
| 001 | No decimation |
| 010 | Decimation with factor 2 |
| 011 | Decimation with factor 3 |
| 100 | Decimation with factor 4 |
| 101 | Decimation with factor 8 |
| 110 | Decimation with factor 16 |
| 111 | Decimation with factor 32 |

Table 35. Accelerometer FIFO decimation setting

| DEC_FIFO_XL [2:0] | Configuration |
|-------------------|----------------------------------|
| 000 | Accelerometer sensor not in FIFO |
| 001 | No decimation |
| 010 | Decimation with factor 2 |
| 011 | Decimation with factor 3 |
| 100 | Decimation with factor 4 |
| 101 | Decimation with factor 8 |
| 110 | Decimation with factor 16 |
| 111 | Decimation with factor 32 |

10.7 FIFO_CTRL4 (09h)

FIFO control register (r/w).

Table 36. FIFO_CTRL4 register

| | | | | | | | |
|-------------|----------------|---------------|---------------|---------------|---------------|---------------|---------------|
| STOP_ON_FTH | ONLY_HIGH_DATA | DEC_DS4_FIFO2 | DEC_DS4_FIFO1 | DEC_DS4_FIFO0 | DEC_DS3_FIFO2 | DEC_DS3_FIFO1 | DEC_DS3_FIFO0 |
|-------------|----------------|---------------|---------------|---------------|---------------|---------------|---------------|

Table 37. FIFO_CTRL4 register description

| | |
|-------------------|--|
| STOP_ON_FTH | Enable FIFO threshold level use. Default value: 0. (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level) |
| ONLY_HIGH_DATA | 8-bit data storage in FIFO. Default: 0 (0: disable MSByte only memorization in FIFO for XL and Gyro; 1: enable MSByte only memorization in FIFO for XL and Gyro in FIFO) |
| DEC_DS4_FIFO[2:0] | Fourth FIFO data set decimation setting. Default: 000 For the configuration setting, refer to Table 38 . |
| DEC_DS3_FIFO[2:0] | Third FIFO data set decimation setting. Default: 000 For the configuration setting, refer to Table 39 . |

Table 38. Fourth FIFO data set decimation setting

| DEC_DS4_FIFO[2:0] | Configuration |
|-------------------|----------------------------------|
| 000 | Fourth FIFO data set not in FIFO |
| 001 | No decimation |
| 010 | Decimation with factor 2 |
| 011 | Decimation with factor 3 |
| 100 | Decimation with factor 4 |
| 101 | Decimation with factor 8 |
| 110 | Decimation with factor 16 |
| 111 | Decimation with factor 32 |

Table 39. Third FIFO data set decimation setting

| DEC_DS3_FIFO[2:0] | Configuration |
|-------------------|---------------------------------|
| 000 | Third FIFO data set not in FIFO |
| 001 | No decimation |
| 010 | Decimation with factor 2 |
| 011 | Decimation with factor 3 |
| 100 | Decimation with factor 4 |
| 101 | Decimation with factor 8 |
| 110 | Decimation with factor 16 |
| 111 | Decimation with factor 32 |

10.8 FIFO_CTRL5 (0Ah)

FIFO control register (r/w).

Table 40. FIFO_CTRL5 register

| | | | | | | | |
|------------------|------------|------------|------------|------------|-------------|-------------|-------------|
| 0 ⁽¹⁾ | ODR_FIFO_3 | ODR_FIFO_2 | ODR_FIFO_1 | ODR_FIFO_0 | FIFO_MODE_2 | FIFO_MODE_1 | FIFO_MODE_0 |
|------------------|------------|------------|------------|------------|-------------|-------------|-------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 41. FIFO_CTRL5 register description

| | |
|-----------------|---|
| ODR_FIFO_[3:0] | FIFO ODR selection, setting FIFO_MODE also. Default: 0000 For the configuration setting, refer to Table 42 . |
| FIFO_MODE_[2:0] | FIFO mode selection bits, setting ODR_FIFO also. Default value: 000 For the configuration setting, refer to Table 43 . |

Table 42. FIFO ODR selection

| ODR_FIFO_[3:0] | Configuration ⁽¹⁾ |
|----------------|------------------------------|
| 0000 | FIFO disabled |
| 0001 | FIFO ODR is set to 12.5 Hz |
| 0010 | FIFO ODR is set to 26 Hz |
| 0011 | FIFO ODR is set to 52 Hz |
| 0100 | FIFO ODR is set to 104 Hz |
| 0101 | FIFO ODR is set to 208 Hz |
| 0110 | FIFO ODR is set to 416 Hz |
| 0111 | FIFO ODR is set to 833 Hz |
| 1000 | FIFO ODR is set to 1.66 kHz |
| 1001 | FIFO ODR is set to 3.33 kHz |
| 1010 | FIFO ODR is set to 6.66 kHz |

1. If the device is working at an ODR slower than the one selected, FIFO ODR is limited to that ODR value. Moreover, these bits are effective if both the DATA_VALID_SEL FIFO bit of [MASTER_CONFIG \(1Ah\)](#) and the TIMER_PEDO_FIFO_DRDY bit of [FIFO_CTRL2 \(07h\)](#) are set to 0.

Table 43. FIFO mode selection

| FIFO_MODE_[2:0] | Configuration mode |
|-----------------|--|
| 000 | Bypass mode. FIFO disabled. |
| 001 | FIFO mode. Stops collecting data when FIFO is full. |
| 010 | Reserved |
| 011 | Continuous mode until trigger is deasserted, then FIFO mode. |
| 100 | Bypass mode until trigger is deasserted, then Continuous mode. |
| 101 | Reserved |
| 110 | Continuous mode. If the FIFO is full, the new sample overwrites the older one. |
| 111 | Reserved |

10.9 DRDY_PULSE_CFG (0Bh)

DataReady configuration register (r/w).

Table 44. DRDY_PULSE_CFG register

| | | | | | | | |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|
| DRDY_PULSED | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | INT2_WRIST_TILT |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 45. DRDY_PULSE_CFG register description

| | |
|-----------------|---|
| DRDY_PULSED | Enable pulsed DataReady mode. Default value: 0 (0: DataReady latched mode. Returns to 0 only after output data has been read; 1: DataReady pulsed mode. The DataReady pulses are 75 µs long.) |
| INT2_WRIST_TILT | Wrist tilt interrupt on INT2 pad. Default value: 0 (0: disabled; 1: enabled) |

10.10 INT1_CTRL (0Dh)

INT1 pad control register (r/w).

Each bit in this register enables a signal to be carried through INT1. The pad's output will supply the OR combination of the selected signals.

Table 46. INT1_CTRL register

| | | | | | | | |
|--------------------|---------------|----------------|---------------|----------|-----------|-------------|--------------|
| INT1_STEP_DETECTOR | INT1_SIGN_MOT | INT1_FULL_FLAG | INT1_FIFO_OVR | INT1_FTH | INT1_BOOT | INT1_DRDY_G | INT1_DRDY_XL |
|--------------------|---------------|----------------|---------------|----------|-----------|-------------|--------------|

Table 47. INT1_CTRL register description

| | |
|--------------------|--|
| INT1_STEP_DETECTOR | Pedometer step recognition interrupt enable on INT1 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT1_SIGN_MOT | Significant motion interrupt enable on INT1 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT1_FULL_FLAG | FIFO full flag interrupt enable on INT1 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT1_FIFO_OVR | FIFO overrun interrupt on INT1 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT1_FTH | FIFO threshold interrupt on INT1 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT1_BOOT | Boot status available on INT1 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT1_DRDY_G | Gyroscope Data Ready on INT1 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT1_DRDY_XL | Accelerometer Data Ready on INT1 pad. Default value: 0 (0: disabled; 1: enabled) |

10.11 INT2_CTRL (0Eh)

INT2 pad control register (r/w).

Each bit in this register enables a signal to be carried through INT2. The pad's output will supply the OR combination of the selected signals.

Table 48. INT2_CTRL register

| | | | | | | | |
|-----------------|--------------------|----------------|---------------|----------|----------------|-------------|--------------|
| INT2_STEP_DELTA | INT2_STEP_COUNT_OV | INT2_FULL_FLAG | INT2_FIFO_OVR | INT2_FTH | INT2_DRDY_TEMP | INT2_DRDY_G | INT2_DRDY_XL |
|-----------------|--------------------|----------------|---------------|----------|----------------|-------------|--------------|

Table 49. INT2_CTRL register description

| | |
|--------------------|---|
| INT2_STEP_DELTA | Pedometer step recognition interrupt on delta time ⁽¹⁾ enable on INT2 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT2_STEP_COUNT_OV | Step counter overflow interrupt enable on INT2 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT2_FULL_FLAG | FIFO full flag interrupt enable on INT2 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT2_FIFO_OVR | FIFO overrun interrupt on INT2 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT2_FTH | FIFO threshold interrupt on INT2 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT2_DRDY_TEMP | Temperature Data Ready on INT2 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT2_DRDY_G | Gyroscope Data Ready on INT2 pad. Default value: 0 (0: disabled; 1: enabled) |
| INT2_DRDY_XL | Accelerometer Data Ready on INT2 pad. Default value: 0 (0: disabled; 1: enabled) |

1. Delta time value is defined in register [STEP_COUNT_DELTA \(15h\)](#).

10.12 WHO_AM_I (0Fh)

Who_AM_I register (r). This register is a read-only register. Its value is fixed at 6Ah.

Table 50. WHO_AM_I register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
|---|---|---|---|---|---|---|---|

10.13 CTRL1_XL (10h)

Linear acceleration sensor control register 1 (r/w).

Table 51. CTRL1_XL register

| | | | | | | | |
|---------|---------|---------|---------|--------|--------|-------------|--------|
| ODR_XL3 | ODR_XL2 | ODR_XL1 | ODR_XL0 | FS_XL1 | FS_XL0 | LPF1_BW_SEL | BW0_XL |
|---------|---------|---------|---------|--------|--------|-------------|--------|

Table 52. CTRL1_XL register description

| | |
|--------------|--|
| ODR_XL [3:0] | Output data rate and power mode selection. Default value: 0000 (see Table 53). |
| FS_XL [1:0] | Accelerometer full-scale selection. Default value: 00. (00: ± 2 g; 01: ± 16 g; 10: ± 4 g; 11: ± 8 g) |
| LPF1_BW_SEL | Accelerometer digital LPF (LPF1) bandwidth selection. For bandwidth selection refer to CTRL8_XL (17h) . |
| BW0_XL | Accelerometer analog chain bandwidth selection (only for accelerometer ODR ≥ 1.67 kHz). (0: BW @ 1.5 kHz; 1: BW @ 400 Hz) |

Table 53. Accelerometer ODR register setting

| ODR_XL3 | ODR_XL2 | ODR_XL1 | ODR_XL0 | ODR selection [Hz] when XL_HM_MODE = 1 | ODR selection [Hz] when XL_HM_MODE = 0 |
|---------|---------|---------|---------|--|--|
| 0 | 0 | 0 | 0 | Power-down | Power-down |
| 1 | 0 | 1 | 1 | 1.6 Hz (low power only) | 12.5 Hz (high performance) |
| 0 | 0 | 0 | 1 | 12.5 Hz (low power) | 12.5 Hz (high performance) |
| 0 | 0 | 1 | 0 | 26 Hz (low power) | 26 Hz (high performance) |
| 0 | 0 | 1 | 1 | 52 Hz (low power) | 52 Hz (high performance) |
| 0 | 1 | 0 | 0 | 104 Hz (normal mode) | 104 Hz (high performance) |
| 0 | 1 | 0 | 1 | 208 Hz (normal mode) | 208 Hz (high performance) |
| 0 | 1 | 1 | 0 | 416 Hz (high performance) | 416 Hz (high performance) |
| 0 | 1 | 1 | 1 | 833 Hz (high performance) | 833 Hz (high performance) |
| 1 | 0 | 0 | 0 | 1.66 kHz (high performance) | 1.66 kHz (high performance) |
| 1 | 0 | 0 | 1 | 3.33 kHz (high performance) | 3.33 kHz (high performance) |
| 1 | 0 | 1 | 0 | 6.66 kHz (high performance) | 6.66 kHz (high performance) |
| 1 | 1 | x | x | Not allowed | Not allowed |

10.14 CTRL2_G (11h)

Angular rate sensor control register 2 (r/w).

Table 54. CTRL2_G register

| | | | | | | | |
|--------|--------|--------|--------|-------|-------|--------|------------------|
| ODR_G3 | ODR_G2 | ODR_G1 | ODR_G0 | FS_G1 | FS_G0 | FS_125 | 0 ⁽¹⁾ |
|--------|--------|--------|--------|-------|-------|--------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 55. CTRL2_G register description

| | |
|-------------|---|
| ODR_G [3:0] | Gyroscope output data rate selection. Default value: 0000 (Refer to Table 56) |
| FS_G [1:0] | Gyroscope full-scale selection. Default value: 00 (00: 250 dps; 01: 500 dps; 10: 1000 dps; 11: 2000 dps) |
| FS_125 | Gyroscope full-scale at 125 dps. Default value: 0 (0: disabled; 1: enabled) |

Table 56. Gyroscope ODR configuration setting

| ODR_G3 | ODR_G2 | ODR_G1 | ODR_G0 | ODR [Hz] when G_HM_MODE = 1 | ODR [Hz] when G_HM_MODE = 0 |
|--------|--------|--------|--------|--------------------------------|--------------------------------|
| 0 | 0 | 0 | 0 | Power down | Power down |
| 0 | 0 | 0 | 1 | 12.5 Hz (low power) | 12.5 Hz (high performance) |
| 0 | 0 | 1 | 0 | 26 Hz (low power) | 26 Hz (high performance) |
| 0 | 0 | 1 | 1 | 52 Hz (low power) | 52 Hz (high performance) |
| 0 | 1 | 0 | 0 | 104 Hz (normal mode) | 104 Hz (high performance) |
| 0 | 1 | 0 | 1 | 208 Hz (normal mode) | 208 Hz (high performance) |
| 0 | 1 | 1 | 0 | 416 Hz (high performance) | 416 Hz (high performance) |
| 0 | 1 | 1 | 1 | 833 Hz (high performance) | 833 Hz (high performance) |
| 1 | 0 | 0 | 0 | 1.66 kHz (high performance) | 1.66 kHz (high performance) |
| 1 | 0 | 0 | 1 | 3.33 kHz (high performance) | 3.33 kHz (high performance) |
| 1 | 0 | 1 | 0 | 6.66 kHz (high performance) | 6.66 kHz (high performance) |
| 1 | 0 | 1 | 1 | Not available | Not available |

10.15 CTRL3_C (12h)

Control register 3 (r/w).

Table 57. CTRL3_C register

| | | | | | | | |
|------|-----|-----------|-------|-----|--------|-----|----------|
| BOOT | BDU | H_LACTIVE | PP_OD | SIM | IF_INC | BLE | SW_RESET |
|------|-----|-----------|-------|-----|--------|-----|----------|

Table 58. CTRL3_C register description

| | |
|-----------|---|
| BOOT | Reboots memory content. Default value: 0 (0: normal mode; 1: reboot memory content) |
| BDU | Block Data Update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read) |
| H_LACTIVE | Interrupt activation level. Default value: 0 (0: interrupt output pads active high; 1: interrupt output pads active low) |
| PP_OD | Push-pull/open-drain selection on INT1 and INT2 pads. Default value: 0 (0: push-pull mode; 1: open-drain mode) |
| SIM | SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface) |
| IF_INC | Register address automatically incremented during a multiple byte access with a serial interface (I ² C or SPI). Default value: 1 (0: disabled; 1: enabled) |
| BLE | Big/Little Endian Data selection. Default value 0 (0: data LSB @ lower address; 1: data MSB @ lower address) |
| SW_RESET | Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is automatically cleared. |

10.16 CTRL4_C (13h)

Control register 4 (r/w).

Table 59. CTRL4_C register

| | | | | | | | |
|-----------|-------|--------------|---------------|-----------|-------------|------------|------------------|
| DEN_XL_EN | SLEEP | INT2_on_INT1 | DEN_DRDY_INT1 | DRDY_MASK | I2C_disable | LPF1_SEL_G | 0 ⁽¹⁾ |
|-----------|-------|--------------|---------------|-----------|-------------|------------|------------------|

Table 60. CTRL4_C register description

| | |
|---------------|--|
| DEN_XL_EN | Extend DEN functionality to accelerometer sensor. Default value: 0 (0: disabled; 1: enabled) |
| SLEEP | Gyroscope sleep mode enable. Default value: 0 (0: disabled; 1: enabled) |
| INT2_on_INT1 | All interrupt signals available on INT1 pad enable. Default value: 0 (0: interrupt signals divided between INT1 and INT2 pads; 1: all interrupt signals in logic or on INT1 pad) |
| DEN_DRDY_INT1 | DEN DRDY signal on INT1 pad. Default value: 0 (0: disabled; 1: enabled) |
| DRDY_MASK | Configuration 1 data available enable bit. Default value: 0 (0: DA timer disabled; 1: DA timer enabled) |
| I2C_disable | Disable I ² C interface. Default value: 0 (0: both I ² C and SPI enabled; 1: I ² C disabled, SPI only) |
| LPF1_SEL_G | Enable gyroscope digital LPF1 if auxiliary SPI is disabled; the bandwidth can be selected through FTYPE [1:0] in CTRL6_C (15h) (0: disabled; 1: enabled) |

10.17 CTRL5_C (14h)

Control register 5 (r/w).

Table 61. CTRL5_C register

| | | | | | | | |
|-----------|-----------|-----------|--------|-------|-------|--------|--------|
| ROUNDING2 | ROUNDING1 | ROUNDING0 | DEN_LH | ST1_G | ST0_G | ST1_XL | ST0_XL |
|-----------|-----------|-----------|--------|-------|-------|--------|--------|

Table 62. CTRL5_C register description

| | |
|---------------|--|
| ROUNDING[2:0] | Circular burst-mode (rounding) read from output registers through the primary interface. Default value: 000 (000: no rounding; Others: refer to Table 63) |
| DEN_LH | DEN active level configuration. Default value: 0 (0: active low; 1: active high) |
| ST_G [1:0] | Angular rate sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to Table 64) |
| ST_XL [1:0] | Linear acceleration sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to Table 65) |

Table 63. Output registers rounding pattern

| ROUNDING[2:0] | Rounding pattern |
|---------------|--|
| 000 | No rounding |
| 001 | Accelerometer only |
| 010 | Gyroscope only |
| 011 | Gyroscope + accelerometer |
| 100 | Registers from SENSORHUB1_REG (2Eh) to SENSORHUB6_REG (33h) only |
| 101 | Accelerometer + registers from SENSORHUB1_REG (2Eh) to SENSORHUB6_REG (33h) |
| 110 | Gyroscope + accelerometer + registers from SENSORHUB1_REG (2Eh) to SENSORHUB6_REG (33h) and registers from SENSORHUB7_REG (34h) to SENSORHUB12_REG (39h) |
| 111 | Gyroscope + accelerometer + registers from SENSORHUB1_REG (2Eh) to SENSORHUB6_REG (33h) |

Table 64. Angular rate sensor self-test mode selection

| ST1_G | ST0_G | Self-test mode |
|-------|-------|-------------------------|
| 0 | 0 | Normal mode |
| 0 | 1 | Positive sign self-test |
| 1 | 0 | Not allowed |
| 1 | 1 | Negative sign self-test |

Table 65. Linear acceleration sensor self-test mode selection

| ST1_XL | ST0_XL | Self-test mode |
|--------|--------|-------------------------|
| 0 | 0 | Normal mode |
| 0 | 1 | Positive sign self-test |
| 1 | 0 | Negative sign self-test |
| 1 | 1 | Not allowed |

10.18 CTRL6_C (15h)

Angular rate sensor control register 6 (r/w).

Table 66. CTRL6_C register

| | | | | | | | |
|---------|---------|---------|------------|-----------|------------------|---------|---------|
| TRIG_EN | LVL1_EN | LVL2_EN | XL_HM_MODE | USR_OFF_W | 0 ⁽¹⁾ | FTYPE_1 | FTYPE_0 |
|---------|---------|---------|------------|-----------|------------------|---------|---------|

1. This bit must be set to '0' for the correct operation of the device.

Table 67. CTRL6_C register description

| | |
|------------|--|
| TRIG_EN | DEN data edge-sensitive trigger enable. Refer to Table 68 . |
| LVL1_EN | DEN data level-sensitive trigger enable. Refer to Table 68 . |
| LVL2_EN | DEN level-sensitive latched enable. Refer to Table 68 . |
| XL_HM_MODE | High-performance operating mode disable for accelerometer. Default value: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled) |
| USR_OFF_W | Weight of XL user offset bits of registers X_OFS_USR (73h) , Y_OFS_USR (74h) , Z_OFS_USR (75h) 0 = 2 ⁻¹⁰ g/LSB 1 = 2 ⁻⁶ g/LSB |
| FTYPE[1:0] | Gyroscope's low-pass filter (LPF1) bandwidth selection Table 69 shows the selectable bandwidth values (available if auxiliary SPI is disabled). |

Table 68. Trigger mode selection

| TRIG_EN, LVL1_EN, LVL2_EN | Trigger mode |
|---------------------------|--|
| 100 | Edge-sensitive trigger mode is selected |
| 010 | Level-sensitive trigger mode is selected |
| 011 | Level-sensitive latched mode is selected |
| 110 | Level-sensitive FIFO enable mode is selected |

Table 69. Gyroscope LPF1 bandwidth selection

| FTYPE[1:0] | ODR = 800 Hz | | ODR = 1.6 kHz | | ODR = 3.3 kHz | | ODR = 6.6 kHz | |
|------------|--------------|----------------------------|---------------|----------------------------|---------------|----------------------------|---------------|----------------------------|
| | BW | Phase delay ⁽¹⁾ | BW | Phase delay ⁽¹⁾ | BW | Phase delay ⁽¹⁾ | BW | Phase delay ⁽¹⁾ |
| 00 | 245 Hz | 14° | 315 Hz | 10° | 343 Hz | 8° | 351 Hz | 7° |
| 01 | 195 Hz | 17° | 224 Hz | 12° | 234 Hz | 10° | 237 Hz | 9° |
| 10 | 155 Hz | 19° | 168 Hz | 15° | 172 Hz | 12° | 173 Hz | 11° |
| 11 | 293 Hz | 13° | 505 Hz | 8° | 925 Hz | 6° | 937 Hz | 5° |

1. Phase delay @ 20 Hz

10.19 CTRL7_G (16h)

Angular rate sensor control register 7 (r/w).

Table 70. CTRL7_G register

| | | | | | | | |
|-----------|---------|--------|--------|------------------|-----------------|------------------|------------------|
| G_HM_MODE | HP_EN_G | HPM1_G | HPM0_G | 0 ⁽¹⁾ | ROUNDING_STATUS | 0 ⁽¹⁾ | 0 ⁽¹⁾ |
|-----------|---------|--------|--------|------------------|-----------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 71. CTRL7_G register description

| | |
|-----------------|--|
| G_HM_MODE | High-performance operating mode disable for gyroscope(1). Default: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled) |
| HP_EN_G | Gyroscope digital high-pass filter enable. The filter is enabled only if the gyro is in HP mode. Default value: 0 (0: HPF disabled; 1: HPF enabled) |
| HPM_G[1:0] | Gyroscope digital HP filter cutoff selection. Default: 00 (00 = 16 mHz 01 = 65 mHz 10 = 260 mHz 11 = 1.04 Hz) |
| ROUNDING_STATUS | Source register rounding function on WAKE_UP_SRC (1Bh) , TAP_SRC (1Ch) , D6D_SRC (1Dh) , STATUS_REG (1Eh) , and FUNC_SRC1 (53h) registers in the primary interface. Default value: 0 (0: Rounding disabled; 1: Rounding enabled) |

10.20 CTRL8_XL (17h)

Linear acceleration sensor control register 8 (r/w).

Table 72. CTRL8_XL register

| | | | | | | | |
|------------|----------|----------|-------------|-----------------|----------------|------------------|----------------|
| LPF2_XL_EN | HPCF_XL1 | HPCF_XL0 | HP_REF_MODE | INPUT_COMPOSITE | HP_SLOPE_XL_EN | 0 ⁽¹⁾ | LOW_PASS_ON_6D |
|------------|----------|----------|-------------|-----------------|----------------|------------------|----------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 73. CTRL8_XL register description

| | |
|-----------------|--|
| LPF2_XL_EN | Accelerometer low-pass filter LPF2 selection. Refer to Figure 9 . |
| HPCF_XL[1:0] | Accelerometer LPF2 and high-pass filter configuration and cutoff setting. Refer to Table 74 . |
| HP_REF_MODE | Enable HP filter reference mode. Default value: 0 (0: disabled; 1: enabled ⁽¹⁾) |
| INPUT_COMPOSITE | Composite filter input selection. Default: 0 (0: ODR/2 low pass filtered sent to composite filter (default) 1: ODR/4 low pass filtered sent to composite filter) |
| HP_SLOPE_XL_EN | Accelerometer slope filter / high-pass filter selection. Refer to Figure 9 . |
| LOW_PASS_ON_6D | LPF2 on 6D function selection. Refer to Figure 9 . |

1. When enabled, the first output data has to be discarded.

Table 74. Accelerometer bandwidth selection

| HP_SLOPE_XL_EN | LPF2_XL_EN | LPF1_BW_SEL | HPCF_XL[1:0] | INPUT_COMPOSITE | Bandwidth |
|--------------------------------------|------------|-------------|--------------|----------------------------------|-----------|
| 0 (low-pass path) ⁽¹⁾ | 0 | 0 | - | - | ODR/2 |
| | | 1 | - | - | ODR/4 |
| | 1 | - | 00 | 1 (low noise) 0 (low latency) | ODR/50 |
| | | | 01 | | ODR/100 |
| | | | 10 | | ODR/9 |
| | | | 11 | | ODR/400 |
| 1 (high-pass path) ⁽²⁾ | - | - | 00 | 0 | ODR/4 |
| | | | 01 | | ODR/100 |
| | | | 10 | | ODR/9 |
| | | | 11 | | ODR/400 |

1. The bandwidth column is related to LPF1 if LPF2_XL_EN = 0 or to LPF2 if LPF2_XL_EN = 1.

2. The bandwidth column is related to the slope filter if HPCF_XL[1:0] = 00 or to the HP filter if HPCF_XL[1:0] = 01/10/11.

10.21 CTRL9_XL (18h)

Linear acceleration sensor control register 9 (r/w).

Table 75. CTRL9_XL register

| | | | | | | | |
|-------|-------|-------|----------|------------------|---------|------------------|------------------|
| DEN_X | DEN_Y | DEN_Z | DEN_XL_G | 0 ⁽¹⁾ | SOFT_EN | 0 ⁽¹⁾ | 0 ⁽¹⁾ |
|-------|-------|-------|----------|------------------|---------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 76. CTRL9_XL register description

| | |
|----------|--|
| DEN_X | DEN value stored in LSB of X-axis. Default value: 1 (0: DEN not stored in X-axis LSB; 1: DEN stored in X-axis LSB) |
| DEN_Y | DEN value stored in LSB of Y-axis. Default value: 1 (0: DEN not stored in Y-axis LSB; 1: DEN stored in Y-axis LSB) |
| DEN_Z | DEN value stored in LSB of Z-axis. Default value: 1 (0: DEN not stored in Z-axis LSB; 1: DEN stored in Z-axis LSB) |
| DEN_XL_G | DEN stamping sensor selection. Default value: 0 (0: DEN pin info stamped in the gyroscope axis selected by bits [7:5]; 1: DEN pin info stamped in the accelerometer axis selected by bits [7:5]) |
| SOFT_EN | Enable soft-iron correction algorithm for magnetometer ⁽¹⁾ . Default value: 0 (0: soft-iron correction algorithm disabled; 1: soft-iron correction algorithm enabled) |

1. This bit is effective if the IRON_EN bit of [MASTER_CONFIG \(1Ah\)](#) and FUNC_EN bit of [CTRL10_C \(19h\)](#) are set to 1.

10.22 CTRL10_C (19h)

Control register 10 (r/w).

Table 77. CTRL10_C register

| | | | | | | | |
|---------------|------------------|----------|---------|---------|---------|---------------|----------------|
| WRIST_TILT_EN | 0 ⁽¹⁾ | TIMER_EN | PEDO_EN | TILT_EN | FUNC_EN | PEDO_RST_STEP | SIGN_MOTION_EN |
|---------------|------------------|----------|---------|---------|---------|---------------|----------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 78. CTRL10_C register description

| | |
|----------------|---|
| WRIST_TILT_EN | Enable wrist tilt algorithm. ⁽¹⁾⁽²⁾ Default value: 0 (0: wrist tilt algorithm disabled; 1: wrist tilt algorithm enabled) |
| TIMER_EN | Enable timestamp count. The count is saved in TIMESTAMP0_REG (40h) , TIMESTAMP1_REG (41h) and TIMESTAMP2_REG (42h) . Default: 0 (0: timestamp count disabled; 1: timestamp count enabled) |
| PEDO_EN | Enable pedometer algorithm. ⁽²⁾ Default value: 0 (0: pedometer algorithm disabled; 1: pedometer algorithm enabled) |
| TILT_EN | Enable tilt calculation. ⁽²⁾ |
| FUNC_EN | Enable embedded functionalities (pedometer, tilt, wrist tilt, significant motion detection, sensor hub and ironing). Default value: 0 (0: disable functionalities of embedded functions and accelerometer filters; 1: enable functionalities of embedded functions and accelerometer filters) |
| PEDO_RST_STEP | Reset pedometer step counter. Default value: 0 (0: disabled; 1: enabled) |
| SIGN_MOTION_EN | Enable significant motion detection function. ⁽²⁾ Default value: 0 (0: disabled; 1: enabled) |

1. By default, the wrist tilt algorithm is applied to the positive X-axis.
2. This is effective if the FUNC_EN bit is set to '1'.

10.23 MASTER_CONFIG (1Ah)

Master configuration register (r/w).

Table 79. MASTER_CONFIG register

| | | | | | | | |
|--------------|---------------------|------------------|--------------|------------|-------------------|---------|-----------|
| DRDY_ON_INT1 | DATA_VALID_SEL_FIFO | 0 ⁽¹⁾ | START_CONFIG | PULL_UP_EN | PASS_THROUGH_MODE | IRON_EN | MASTER_ON |
|--------------|---------------------|------------------|--------------|------------|-------------------|---------|-----------|

1. This bit must be set to '0' for the correct operation of the device.

Table 80. MASTER_CONFIG register description

| | |
|---------------------|---|
| DRDY_ON_INT1 | Manage the Master DRDY signal on INT1 pad. Default: 0 (0: disable Master DRDY on INT1; 1: enable Master DRDY on INT1) |
| DATA_VALID_SEL_FIFO | Selection of FIFO data-valid signal. Default value: 0 (0: data-valid signal used to write data in FIFO is the XL/Gyro data-ready or step detection ⁽¹⁾ ; 1: data-valid signal used to write data in FIFO is the sensor hub data-ready) |
| START_CONFIG | Sensor Hub trigger signal selection. Default value: 0 (0: Sensor hub signal is the XL/Gyro data-ready; 1: Sensor hub signal external from INT2 pad.) |
| PULL_UP_EN | Auxiliary I ² C pull-up. Default value: 0 (0: internal pull-up on auxiliary I ² C line disabled; 1: internal pull-up on auxiliary I ² C line enabled) |
| PASS_THROUGH_MODE | I ² C interface pass-through. Default value: 0 (0: pass-through disabled; 1: pass-through enabled) |
| IRON_EN | Enable hard-iron correction algorithm for magnetometer ⁽²⁾ . Default value: 0 (0: hard-iron correction algorithm disabled; 1: hard-iron correction algorithm enabled) |
| MASTER_ON | Sensor hub I ² C master enable ⁽²⁾ . Default: 0 (0: master I ² C of sensor hub disabled; 1: master I ² C of sensor hub enabled) |

1. If the TIMER_PEDO_FIFO_DRDY bit in [FIFO_CTRL2 \(07h\)](#) is set to 0, the trigger for writing data in FIFO is XL/Gyro data-ready, otherwise it's the step detection.

2. This is effective if the FUNC_EN bit is set to '1'.

10.24 WAKE_UP_SRC (1Bh)

Wake-up interrupt source register (r).

Table 81. WAKE_UP_SRC register

| | | | | | | | |
|---|---|-------|----------------|-------|------|------|------|
| 0 | 0 | FF_IA | SLEEP_STATE_IA | WU_IA | X_WU | Y_WU | Z_WU |
|---|---|-------|----------------|-------|------|------|------|

Table 82. WAKE_UP_SRC register description

| | |
|----------------|---|
| FF_IA | Free-fall event detection status. Default: 0 (0: free-fall event not detected; 1: free-fall event detected) |
| SLEEP_STATE_IA | Sleep event status. Default value: 0 (0: sleep event not detected; 1: sleep event detected) |
| WU_IA | Wakeup event detection status. Default value: 0 (0: wakeup event not detected; 1: wakeup event detected.) |
| X_WU | Wakeup event detection status on X-axis. Default value: 0 (0: wakeup event on X-axis not detected; 1: wakeup event on X-axis detected) |
| Y_WU | Wakeup event detection status on Y-axis. Default value: 0 (0: wakeup event on Y-axis not detected; 1: wakeup event on Y-axis detected) |
| Z_WU | Wakeup event detection status on Z-axis. Default value: 0 (0: wakeup event on Z-axis not detected; 1: wakeup event on Z-axis detected) |

10.25 TAP_SRC (1Ch)

Tap source register (r).

Table 83. TAP_SRC register

| | | | | | | | |
|---|--------|------------|------------|----------|-------|-------|-------|
| 0 | TAP_IA | SINGLE_TAP | DOUBLE_TAP | TAP_SIGN | X_TAP | Y_TAP | Z_TAP |
|---|--------|------------|------------|----------|-------|-------|-------|

Table 84. TAP_SRC register description

| | |
|------------|---|
| TAP_IA | Tap event detection status. Default: 0 (0: tap event not detected; 1: tap event detected) |
| SINGLE_TAP | Single-tap event status. Default value: 0 (0: single tap event not detected; 1: single tap event detected) |
| DOUBLE_TAP | Double-tap event detection status. Default value: 0 (0: double-tap event not detected; 1: double-tap event detected.) |
| TAP_SIGN | Sign of acceleration detected by tap event. Default: 0 (0: positive sign of acceleration detected by tap event; 1: negative sign of acceleration detected by tap event) |
| X_TAP | Tap event detection status on X-axis. Default value: 0 (0: tap event on X-axis not detected; 1: tap event on X-axis detected) |
| Y_TAP | Tap event detection status on Y-axis. Default value: 0 (0: tap event on Y-axis not detected; 1: tap event on Y-axis detected) |
| Z_TAP | Tap event detection status on Z-axis. Default value: 0 (0: tap event on Z-axis not detected; 1: tap event on Z-axis detected) |

10.26 D6D_SRC (1Dh)

Portrait, landscape, face-up and face-down source register (r)

Table 85. D6D_SRC register

| | | | | | | | |
|----------|--------|----|----|----|----|----|----|
| DEN_DRDY | D6D_IA | ZH | ZL | YH | YL | XH | XL |
|----------|--------|----|----|----|----|----|----|

Table 86. D6D_SRC register description

| | |
|----------|--|
| DEN_DRDY | DEN data-ready signal. It is set high when data output is related to the data coming from a DEN active condition. ⁽¹⁾ |
| D6D_IA | Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0 (0: change position not detected; 1: change position detected) |
| ZH | Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected) |
| ZL | Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected) |
| YH | Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over-threshold) detected) |
| YL | Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected) |
| XH | X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected) |
| XL | X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected) |

1. The DEN data-ready signal can be latched or pulsed depending on the value of the dataready_pulsed bit of the *DRDY_PULSE_CFG (0Bh)* register.

10.27 STATUS_REG/STATUS_SPIAux (1Eh)

The STATUS_REG register is read by the primary interface SPI/I²C (r).

Table 87. STATUS_REG register

| | | | | | | | |
|---|---|---|---|---|-----|-----|------|
| 0 | 0 | 0 | 0 | 0 | TDA | GDA | XLDA |
|---|---|---|---|---|-----|-----|------|

Table 88. STATUS_REG register description

| | |
|------|--|
| TDA | Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output) |
| GDA | Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output) |
| XLDA | Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output) |

The STATUS_SPIAux register is read by the auxiliary SPI.

Table 89. STATUS_SPIAux register

| | | | | | | | |
|---|---|---|---|---|---------------|-----|------|
| 0 | 0 | 0 | 0 | 0 | GYRO_SETTLING | GDA | XLDA |
|---|---|---|---|---|---------------|-----|------|

Table 90. STATUS_SPIAux description

| | |
|---------------|--|
| GYRO_SETTLING | High when the gyroscope output is in the settling phase |
| GDA | Gyroscope data available (reset when one of the high parts of the output data is read) |
| XLDA | Accelerometer data available (reset when one of the high parts of the output data is read) |

10.28 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (r). L and H registers together express a 16-bit word in two's complement.

Table 91. OUT_TEMP_L register

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

Table 92. OUT_TEMP_H register

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|-------|-------|
| Temp15 | Temp14 | Temp13 | Temp12 | Temp11 | Temp10 | Temp9 | Temp8 |
|--------|--------|--------|--------|--------|--------|-------|-------|

Table 93. OUT_TEMP register description

| | |
|------------|--|
| Temp[15:0] | Temperature sensor output data The value is expressed as two's complement sign extended on the MSB. |
|------------|--|

10.29 OUTX_L_G (22h)

Angular rate sensor pitch axis (X) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full scale and ODR settings ([CTRL2_G \(11h\)](#)) of gyro user interface.

If this register is read by the auxiliary interface, data are according to the full scale and ODR (6.66 kHz) settings of the OIS gyro.

Table 94. OUTX_L_G register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

Table 95. OUTX_L_G register description

| | |
|--------|--|
| D[7:0] | Pitch axis (X) angular rate value (LSbyte) D[15:0] expressed in two's complement and its value depends on the interface used: SPI1/I ² C: Gyro UI chain pitch axis output SPI2: Gyro OIS chain pitch axis output |
|--------|--|

10.30 OUTX_H_G (23h)

Angular rate sensor pitch axis (X) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full scale and ODR settings ([CTRL2_G \(11h\)](#)) of the gyro user interface.

If this register is read by the auxiliary interface, data are according to the full scale and ODR (6.66 kHz) settings of the OIS gyro.

Table 96. OUTX_H_G register

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|
|-----|-----|-----|-----|-----|-----|----|----|

Table 97. OUTX_H_G register description

| | |
|---------|--|
| D[15:8] | Pitch axis (X) angular rate value (MSbyte) D[15:0] expressed in two's complement and its value depends on the interface used: SPI1/I ² C: Gyro UI chain pitch axis output SPI2: Gyro OIS chain pitch axis output |
|---------|--|

10.31 OUTY_L_G (24h)

Angular rate sensor roll axis (Y) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full scale and ODR settings ([CTRL2_G \(11h\)](#)) of the gyro user interface.

If this register is read by the auxiliary interface, data are according to the full scale and ODR (6.66 kHz) settings of the OIS gyro.

Table 98. OUTY_L_G register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

Table 99. OUTY_L_G register description

| | |
|--------|---|
| D[7:0] | Roll axis (Y) angular rate value (LSbyte) D[15:0] expressed in two's complement and its value depends on the interface used: SPI1/I ² C: Gyro UI chain roll axis output SPI2: Gyro OIS chain roll axis output |
|--------|---|

10.32 OUTY_H_G (25h)

Angular rate sensor roll axis (Y) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full scale and ODR settings ([CTRL2_G \(11h\)](#)) of the gyro user interface.

If this register is read by the auxiliary interface, data are according to the full scale and ODR (6.66 kHz) settings of the OIS gyro.

Table 100. OUTY_H_G register

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|
|-----|-----|-----|-----|-----|-----|----|----|

Table 101. OUTY_H_G register description

| | |
|---------|---|
| D[15:8] | Roll axis (Y) angular rate value (MSbyte) D[15:0] expressed in two's complement and its value depends on the interface used: SPI1/I ² C: Gyro UI chain roll axis output SPI2: Gyro OIS chain roll axis output |
|---------|---|

10.33 OUTZ_L_G (26h)

Angular rate sensor yaw axis (Z) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full scale and ODR settings ([CTRL2_G \(11h\)](#)) of the gyro user interface.

If this register is read by the auxiliary interface, data are according to the full scale and ODR (6.66 kHz) settings of the OIS gyro.

Table 102. OUTZ_L_G register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

Table 103. OUTZ_L_G register description

| | |
|--------|--|
| D[7:0] | Yaw axis (Z) angular rate value (LSbyte) D[15:0] expressed in two's complement and its value depends on the interface used: SPI1/I ² C: Gyro UI chain yaw axis output SPI2: Gyro OIS chain yaw axis output |
|--------|--|

10.34 OUTZ_H_G (27h)

Angular rate sensor Yaw axis (Z) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full scale and ODR settings ([CTRL2_G \(11h\)](#)) of the gyro user interface.

If this register is read by the auxiliary interface, data are according to the full scale and ODR (6.66 kHz) settings of the OIS gyro.

Table 104. OUTZ_H_G register

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|
|-----|-----|-----|-----|-----|-----|----|----|

Table 105. OUTZ_H_G register description

| | |
|---------|--|
| D[15:8] | Yaw axis (Z) angular rate value (MSbyte) D[15:0] expressed in two's complement and its value depends on the interface used: SPI1/I ² C: Gyro UI chain yaw axis output SPI2: Gyro OIS chain yaw axis output |
|---------|--|

10.35 OUTX_L_XL (28h)

Linear acceleration sensor X-axis output register (r). The value is expressed as a 16-bit word in two's complement.

Accelerometer data can be read also from AUX SPI @6.6 kHz.

Table 106. OUTX_L_XL register

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Table 107. OUTX_L_XL register description

| | |
|--------|---|
| D[7:0] | X-axis linear acceleration value (LSbyte) |
|--------|---|

10.36 OUTX_H_XL (29h)

Linear acceleration sensor X-axis output register (r). The value is expressed as a 16-bit word in two's complement.

Accelerometer data can be read also from AUX SPI @6.6 kHz.

Table 108. OUTX_H_XL register

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

Table 109. OUTX_H_XL register description

| | |
|---------|---|
| D[15:8] | X-axis linear acceleration value (MSbyte) |
|---------|---|

10.37 OUTY_L_XL (2Ah)

Linear acceleration sensor Y-axis output register (r). The value is expressed as a 16-bit word in two's complement.

Accelerometer data can be read also from AUX SPI @6.6 kHz.

Table 110. OUTY_L_XL register

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Table 111. OUTY_L_XL register description

| | |
|--------|---|
| D[7:0] | Y-axis linear acceleration value (LSbyte) |
|--------|---|

10.38 OUTY_H_XL (2Bh)

Linear acceleration sensor Y-axis output register (r). The value is expressed as a 16-bit word in two's complement.

Accelerometer data can be read also from AUX SPI @6.6 kHz.

Table 112. OUTY_H_XL register

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

Table 113. OUTY_H_XL register description

| | |
|---------|---|
| D[15:8] | Y-axis linear acceleration value (MSbyte) |
|---------|---|

10.39 OUTZ_L_XL (2Ch)

Linear acceleration sensor Z-axis output register (r). The value is expressed as a 16-bit word in two's complement.

Accelerometer data can be read also from AUX SPI @6.6 kHz.

Table 114. OUTZ_L_XL register

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Table 115. OUTZ_L_XL register description

| | |
|--------|---|
| D[7:0] | Z-axis linear acceleration value (LSbyte) |
|--------|---|

10.40 OUTZ_H_XL (2Dh)

Linear acceleration sensor Z-axis output register (r). The value is expressed as a 16-bit word in two's complement.

Accelerometer data can be read also from AUX SPI @6.6 kHz.

Table 116. OUTZ_H_XL register

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

Table 117. OUTZ_H_XL register description

| | |
|---------|---|
| D[15:8] | Z-axis linear acceleration value (MSbyte) |
|---------|---|

10.41 SENSORHUB1_REG (2Eh)

First byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 118. SENSORHUB1_REG register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub1_7 | SHub1_6 | SHub1_5 | SHub1_4 | SHub1_3 | SHub1_2 | SHub1_1 | SHub1_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 119. SENSORHUB1_REG register description

| | |
|-------------|---|
| SHub1_[7:0] | First byte associated to external sensors |
|-------------|---|

10.42 SENSORHUB2_REG (2Fh)

Second byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operations configurations (for external sensors from x = 0 to x = 3).

Table 120. SENSORHUB2_REG register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub2_7 | SHub2_6 | SHub2_5 | SHub2_4 | SHub2_3 | SHub2_2 | SHub2_1 | SHub2_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 121. SENSORHUB2_REG register description

| | |
|-------------|--|
| SHub2_[7:0] | Second byte associated to external sensors |
|-------------|--|

10.43 SENSORHUB3_REG (30h)

Third byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operations configurations (for external sensors from x = 0 to x = 3).

Table 122. SENSORHUB3_REG register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub3_7 | SHub3_6 | SHub3_5 | SHub3_4 | SHub3_3 | SHub3_2 | SHub3_1 | SHub3_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 123. SENSORHUB3_REG register description

| | |
|-------------|---|
| SHub3_[7:0] | Third byte associated to external sensors |
|-------------|---|

10.44 SENSORHUB4_REG (31h)

Fourth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 124. SENSORHUB4_REG register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub4_7 | SHub4_6 | SHub4_5 | SHub4_4 | SHub4_3 | SHub4_2 | SHub4_1 | SHub4_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 125. SENSORHUB4_REG register description

| | |
|-------------|--|
| SHub4_[7:0] | Fourth byte associated to external sensors |
|-------------|--|

10.45 SENSORHUB5_REG (32h)

Fifth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 126. SENSORHUB5_REG register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub5_7 | SHub5_6 | SHub5_5 | SHub5_4 | SHub5_3 | SHub5_2 | SHub5_1 | SHub5_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 127. SENSORHUB5_REG register description

| | |
|-------------|---|
| SHub5_[7:0] | Fifth byte associated to external sensors |
|-------------|---|

10.46 SENSORHUB6_REG (33h)

Sixth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 128. SENSORHUB6_REG register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub6_7 | SHub6_6 | SHub6_5 | SHub6_4 | SHub6_3 | SHub6_2 | SHub6_1 | SHub6_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 129. SENSORHUB6_REG register description

| | |
|-------------|---|
| SHub6_[7:0] | Sixth byte associated to external sensors |
|-------------|---|

10.47 SENSORHUB7_REG (34h)

Seventh byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 130. SENSORHUB7_REG register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub7_7 | SHub7_6 | SHub7_5 | SHub7_4 | SHub7_3 | SHub7_2 | SHub7_1 | SHub7_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 131. SENSORHUB7_REG register description

| | |
|-------------|---|
| SHub7_[7:0] | Seventh byte associated to external sensors |
|-------------|---|

10.48 SENSORHUB8_REG (35h)

Eighth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 132. SENSORHUB8_REG register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub8_7 | SHub8_6 | SHub8_5 | SHub8_4 | SHub8_3 | SHub8_2 | SHub8_1 | SHub8_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 133. SENSORHUB8_REG register description

| | |
|-------------|--|
| SHub8_[7:0] | Eighth byte associated to external sensors |
|-------------|--|

10.49 SENSORHUB9_REG (36h)

Ninth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 134. SENSORHUB9_REG register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub9_7 | SHub9_6 | SHub9_5 | SHub9_4 | SHub9_3 | SHub9_2 | SHub9_1 | SHub9_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 135. SENSORHUB9_REG register description

| | |
|-------------|---|
| SHub9_[7:0] | Ninth byte associated to external sensors |
|-------------|---|

10.50 SENSORHUB10_REG (37h)

Tenth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 136. SENSORHUB10_REG register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub10_7 | SHub10_6 | SHub10_5 | SHub10_4 | SHub10_3 | SHub10_2 | SHub10_1 | SHub10_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 137. SENSORHUB10_REG register description

| | |
|--------------|---|
| SHub10_[7:0] | Tenth byte associated to external sensors |
|--------------|---|

10.51 SENSORHUB11_REG (38h)

Eleventh byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 138. SENSORHUB11_REG register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub11_7 | SHub11_6 | SHub11_5 | SHub11_4 | SHub11_3 | SHub11_2 | SHub11_1 | SHub11_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 139. SENSORHUB11_REG register description

| | |
|--------------|--|
| SHub11_[7:0] | Eleventh byte associated to external sensors |
|--------------|--|

10.52 SENSORHUB12_REG (39h)

Twelfth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 140. SENSORHUB12_REG register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub12_7 | SHub12_6 | SHub12_5 | SHub12_4 | SHub12_3 | SHub12_2 | SHub12_1 | SHub12_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 141. SENSORHUB12_REG register description

| | |
|-------------|---|
| SHub12[7:0] | Twelfth byte associated to external sensors |
|-------------|---|

10.53 FIFO_STATUS1 (3Ah)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3_C \(12h\)](#) to 1.

Table 142. FIFO_STATUS1 register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| DIFF_FIFO_7 | DIFF_FIFO_6 | DIFF_FIFO_5 | DIFF_FIFO_4 | DIFF_FIFO_3 | DIFF_FIFO_2 | DIFF_FIFO_1 | DIFF_FIFO_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 143. FIFO_STATUS1 register description

| | |
|-----------------|--|
| DIFF_FIFO_[7:0] | Number of unread words (16-bit axes) stored in FIFO ⁽¹⁾ . |
|-----------------|--|

1. For a complete number of unread samples, consider DIFF_FIFO [10:8] in [FIFO_STATUS2 \(3Bh\)](#)

10.54 FIFO_STATUS2 (3Bh)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3_C \(12h\)](#) to 1.

Table 144. FIFO_STATUS2 register

| | | | | | | | |
|--------|----------|-----------------|------------|---|--------------|-------------|-------------|
| WaterM | OVER_RUN | FIFO_FULL_SMART | FIFO_EMPTY | 0 | DIFF_FIFO_10 | DIFF_FIFO_9 | DIFF_FIFO_8 |
|--------|----------|-----------------|------------|---|--------------|-------------|-------------|

Table 145. FIFO_STATUS2 register description

| | |
|------------------|---|
| WaterM | FIFO watermark status. The watermark is set through bits FTH_[7:0] in FIFO_CTRL1 (06h) . Default value: 0 (0: FIFO filling is lower than watermark level ⁽¹⁾ ; 1: FIFO filling is equal to or higher than the watermark level) |
| OVER_RUN | FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled) |
| FIFO_FULL_SMART | Smart FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO will be full at the next ODR) |
| FIFO_EMPTY | FIFO empty bit. Default value: 0 (0: FIFO contains data; 1: FIFO is empty) |
| DIFF_FIFO_[10:8] | Number of unread words (16-bit axes) stored in FIFO ⁽²⁾ . |

1. FIFO watermark level is set in FTH_[10:0] in [FIFO_CTRL1 \(06h\)](#) and [FIFO_CTRL2 \(07h\)](#)

2. For a complete number of unread samples, consider DIFF_FIFO [7:0] in [FIFO_STATUS1 \(3Ah\)](#)

10.55 FIFO_STATUS3 (3Ch)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3_C \(12h\)](#) to 1.

Table 146. FIFO_STATUS3 register

| | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| FIFO_PATTERN_7 | FIFO_PATTERN_6 | FIFO_PATTERN_5 | FIFO_PATTERN_4 | FIFO_PATTERN_3 | FIFO_PATTERN_2 | FIFO_PATTERN_1 | FIFO_PATTERN_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

Table 147. FIFO_STATUS3 register description

| | |
|--------------------|---|
| FIFO_PATTERN_[7:0] | Word of recursive pattern read at the next reading. |
|--------------------|---|

10.56 FIFO_STATUS4 (3Dh)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3_C \(12h\)](#) to 1.

Table 148. FIFO_STATUS4 register

| | | | | | | | |
|---|---|---|---|---|---|----------------|----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | FIFO_PATTERN_9 | FIFO_PATTERN_8 |
|---|---|---|---|---|---|----------------|----------------|

Table 149. FIFO_STATUS4 register description

| | |
|--------------------|---|
| FIFO_PATTERN_[9:8] | Word of recursive pattern read at the next reading. |
|--------------------|---|

10.57 FIFO_DATA_OUT_L (3Eh)

FIFO data output register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3_C \(12h\)](#) to 1.

Table 150. FIFO_DATA_OUT_L register

| | | | | | | | |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| DATA_OUT_FIFO_L_7 | DATA_OUT_FIFO_L_6 | DATA_OUT_FIFO_L_5 | DATA_OUT_FIFO_L_4 | DATA_OUT_FIFO_L_3 | DATA_OUT_FIFO_L_2 | DATA_OUT_FIFO_L_1 | DATA_OUT_FIFO_L_0 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|

Table 151. FIFO_DATA_OUT_L register description

| | |
|-----------------------|-------------------------------|
| DATA_OUT_FIFO_L_[7:0] | FIFO data output (first byte) |
|-----------------------|-------------------------------|

10.58 FIFO_DATA_OUT_H (3Fh)

FIFO data output register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3_C \(12h\)](#) to 1.

Table 152. FIFO_DATA_OUT_H register

| | | | | | | | |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| DATA_OUT_FIFO_H_7 | DATA_OUT_FIFO_H_6 | DATA_OUT_FIFO_H_5 | DATA_OUT_FIFO_H_4 | DATA_OUT_FIFO_H_3 | DATA_OUT_FIFO_H_2 | DATA_OUT_FIFO_H_1 | DATA_OUT_FIFO_H_0 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|

Table 153. FIFO_DATA_OUT_H register description

| | |
|-----------------------|--------------------------------|
| DATA_OUT_FIFO_H_[7:0] | FIFO data output (second byte) |
|-----------------------|--------------------------------|

10.59 TIMESTAMP0_REG (40h)

Timestamp first (least significant) byte data output register (r). The value is expressed as a 24-bit word and the bit resolution is defined by setting the value in [WAKE_UP_DUR \(5Ch\)](#).

Table 154. TIMESTAMP0_REG register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| TIMESTA MP0_7 | TIMESTA MP0_6 | TIMESTA MP0_5 | TIMESTA MP0_4 | TIMESTA MP0_3 | TIMESTA MP0_2 | TIMESTA MP0_1 | TIMESTA MP0_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Table 155. TIMESTAMP0_REG register description

| | |
|------------------|----------------------------------|
| TIMESTAMP0_[7:0] | TIMESTAMP first byte data output |
|------------------|----------------------------------|

10.60 TIMESTAMP1_REG (41h)

Timestamp second byte data output register (r). The value is expressed as a 24-bit word and the bit resolution is defined by setting value in [WAKE_UP_DUR \(5Ch\)](#).

Table 156. TIMESTAMP1_REG register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| TIMESTA MP1_7 | TIMESTA MP1_6 | TIMESTA MP1_5 | TIMESTA MP1_4 | TIMESTA MP1_3 | TIMESTA MP1_2 | TIMESTA MP1_1 | TIMESTA MP1_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Table 157. TIMESTAMP1_REG register description

| | |
|------------------|-----------------------------------|
| TIMESTAMP1_[7:0] | TIMESTAMP second byte data output |
|------------------|-----------------------------------|

10.61 TIMESTAMP2_REG (42h)

Timestamp third (most significant) byte data output register (r/w). The value is expressed as a 24-bit word and the bit resolution is defined by setting the value in [WAKE_UP_DUR \(5Ch\)](#). To reset the timer, the AAh value has to be stored in this register.

Table 158. TIMESTAMP2_REG register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| TIMESTA MP2_7 | TIMESTA MP2_6 | TIMESTA MP2_5 | TIMESTA MP2_4 | TIMESTA MP2_3 | TIMESTA MP2_2 | TIMESTA MP2_1 | TIMESTA MP2_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Table 159. TIMESTAMP2_REG register description

| | |
|------------------|----------------------------------|
| TIMESTAMP2_[7:0] | TIMESTAMP third byte data output |
|------------------|----------------------------------|

10.62 STEP_TIMESTAMP_L (49h)

Step counter timestamp information register (r). When a step is detected, the value of TIMESTAMP_REG1 register is copied in STEP_TIMESTAMP_L.

Table 160. STEP_TIMESTAMP_L register

| | | | | | | | |
|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| STEP_ TIMESTA MP_L_7 | STEP_ TIMESTA MP_L_6 | STEP_ TIMESTA MP_L_5 | STEP_ TIMESTA MP_L_4 | STEP_ TIMESTA MP_L_3 | STEP_ TIMESTA MP_L_2 | STEP_ TIMESTA MP_L_1 | STEP_ TIMESTA MP_L_0 |
|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|

Table 161. STEP_TIMESTAMP_L register description

| | |
|-----------------------|----------------------------------|
| STEP_TIMESTAMP_L[7:0] | Timestamp of last step detected. |
|-----------------------|----------------------------------|

10.63 STEP_TIMESTAMP_H (4Ah)

Step counter timestamp information register (r). When a step is detected, the value of TIMESTAMP_REG2 register is copied in STEP_TIMESTAMP_H.

Table 162. STEP_TIMESTAMP_H register

| | | | | | | | |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| STEP_TIMESTAMP_H_7 | STEP_TIMESTAMP_H_6 | STEP_TIMESTAMP_H_5 | STEP_TIMESTAMP_H_4 | STEP_TIMESTAMP_H_3 | STEP_TIMESTAMP_H_2 | STEP_TIMESTAMP_H_1 | STEP_TIMESTAMP_H_0 |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|

Table 163. STEP_TIMESTAMP_H register description

| | |
|-----------------------|----------------------------------|
| STEP_TIMESTAMP_H[7:0] | Timestamp of last step detected. |
|-----------------------|----------------------------------|

10.64 STEP_COUNTER_L (4Bh)

Step counter output register (r).

Table 164. STEP_COUNTER_L register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| STEP_COUNTER_L_7 | STEP_COUNTER_L_6 | STEP_COUNTER_L_5 | STEP_COUNTER_L_4 | STEP_COUNTER_L_3 | STEP_COUNTER_L_2 | STEP_COUNTER_L_1 | STEP_COUNTER_L_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Table 165. STEP_COUNTER_L register description

| | |
|---------------------|------------------------------|
| STEP_COUNTER_L[7:0] | Step counter output (LSbyte) |
|---------------------|------------------------------|

10.65 STEP_COUNTER_H (4Ch)

Step counter output register (r).

Table 166. STEP_COUNTER_H register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| STEP_COUNTER_H_7 | STEP_COUNTER_H_6 | STEP_COUNTER_H_5 | STEP_COUNTER_H_4 | STEP_COUNTER_H_3 | STEP_COUNTER_H_2 | STEP_COUNTER_H_1 | STEP_COUNTER_H_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Table 167. STEP_COUNTER_H register description

| | |
|---------------------|------------------------------|
| STEP_COUNTER_H[7:0] | Step counter output (MSbyte) |
|---------------------|------------------------------|

10.66 SENSORHUB13_REG (4Dh)

Thirteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 168. SENSORHUB13_REG register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub13_7 | SHub13_6 | SHub13_5 | SHub13_4 | SHub13_3 | SHub13_2 | SHub13_1 | SHub13_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 169. SENSORHUB13_REG register description

| | |
|-------------|--|
| SHub13[7:0] | Thirteenth byte associated to external sensors |
|-------------|--|

10.67 SENSORHUB14_REG (4Eh)

Fourteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 170. SENSORHUB14_REG register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub14_7 | SHub14_6 | SHub14_5 | SHub14_4 | SHub14_3 | SHub14_2 | SHub14_1 | SHub14_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 171. SENSORHUB14_REG register description

| | |
|--------------|--|
| SHub14_[7:0] | Fourteenth byte associated to external sensors |
|--------------|--|

10.68 SENSORHUB15_REG (4Fh)

Fifteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 172. SENSORHUB15_REG register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub15_7 | SHub15_6 | SHub15_5 | SHub15_4 | SHub15_3 | SHub15_2 | SHub15_1 | SHub15_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 173. SENSORHUB15_REG register description

| | |
|--------------|---|
| SHub15_[7:0] | Fifteenth byte associated to external sensors |
|--------------|---|

10.69 SENSORHUB16_REG (50h)

Sixteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 174. SENSORHUB16_REG register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub16_7 | SHub16_6 | SHub16_5 | SHub16_4 | SHub16_3 | SHub16_2 | SHub16_1 | SHub16_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 175. SENSORHUB16_REG register description

| | |
|--------------|---|
| SHub16_[7:0] | Sixteenth byte associated to external sensors |
|--------------|---|

10.70 SENSORHUB17_REG (51h)

Seventeenth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 176. SENSORHUB17_REG register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub17_7 | SHub17_6 | SHub17_5 | SHub17_4 | SHub17_3 | SHub17_2 | SHub17_1 | SHub17_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 177. SENSORHUB17_REG register description

| | |
|--------------|---|
| SHub17_[7:0] | Seventeenth byte associated to external sensors |
|--------------|---|

10.71 SENSORHUB18_REG (52h)

Eighteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx_CONFIG number of read operation configurations (for external sensors from $x = 0$ to $x = 3$).

Table 178. SENSORHUB18_REG register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub18_7 | SHub18_6 | SHub18_5 | SHub18_4 | SHub18_3 | SHub18_2 | SHub18_1 | SHub18_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 179. SENSORHUB18_REG register description

| | |
|--------------|--|
| SHub18_[7:0] | Eighteenth byte associated to external sensors |
|--------------|--|

10.72 FUNC_SRC1 (53h)

Significant motion, tilt, step detector, hard/soft-iron and sensor hub interrupt source register (r).

Table 180. FUNC_SRC1 register

| | | | | | | | |
|---------------------|----------------|---------|---------------|---------------|---------|-----------|-------------------|
| STEP_COUNT_DELTA_IA | SIGN_MOTION_IA | TILT_IA | STEP_DETECTED | STEP_OVERFLOW | HI_FAIL | SI_END_OP | SENSOR_HUB_END_OP |
|---------------------|----------------|---------|---------------|---------------|---------|-----------|-------------------|

Table 181. FUNC_SRC1 register description

| | |
|---------------------|---|
| STEP_COUNT_DELTA_IA | Pedometer step recognition on delta time status. Default value: 0 (0: no step recognized during delta time; 1: at least one step recognized during delta time) |
| SIGN_MOTION_IA | Significant motion event detection status. Default value: 0 (0: significant motion event not detected; 1: significant motion event detected) |
| TILT_IA | Tilt event detection status. Default value: 0 (0: tilt event not detected; 1: tilt event detected) |
| STEP_DETECTED | Step detector event detection status. Default value: 0 (0: step detector event not detected; 1: step detector event detected) |
| STEP_OVERFLOW | Step counter overflow status. Default value: 0 (0: step counter value $< 2^{16}$; 1: step counter value reached 2^{16}) |
| HI_FAIL | Fail in hard/soft-ironing algorithm. |
| SI_END_OP | Hard/soft-iron calculation status. Default value: 0 (0: Hard/soft-iron calculation not concluded; 1: Hard/soft-iron calculation concluded) |
| SENSORHUB_END_OP | Sensor hub communication status. Default value: 0 (0: sensor hub communication not concluded; 1: sensor hub communication concluded) |

10.73 FUNC_SRC2 (54h)

Wrist tilt interrupt source register (r).

Table 182. FUNC_SRC2 register

| | | | | | | | |
|---|-------------|-------------|-------------|-------------|---|---|---------------|
| 0 | SLAVE3_NACK | SLAVE2_NACK | SLAVE1_NACK | SLAVE0_NACK | 0 | 0 | WRIST_TILT_IA |
|---|-------------|-------------|-------------|-------------|---|---|---------------|

Table 183. FUNC_SRC2 register description

| | |
|---------------|---|
| SLAVE3_NACK | This bit is set to 1 if Not acknowledge occurs on slave 3 communication. Default value: 0 |
| SLAVE2_NACK | This bit is set to 1 if Not acknowledge occurs on slave 2 communication. Default value: 0 |
| SLAVE1_NACK | This bit is set to 1 if Not acknowledge occurs on slave 1 communication. Default value: 0 |
| SLAVE0_NACK | This bit is set to 1 if Not acknowledge occurs on slave 0 communication. Default value: 0 |
| WRIST_TILT_IA | Wrist tilt event detection status. Default value: 0 (0: Wrist tilt event not detected; 1: Wrist tilt event detected) |

10.74 WRIST_TILT_IA (55h)

Wrist tilt interrupt source register (r).

Table 184. WRIST_TILT_IA register

| | | | | | | | |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|---|---|
| WRIST_TILT_IA_Xpos | WRIST_TILT_IA_Xneg | WRIST_TILT_IA_Ypos | WRIST_TILT_IA_Yneg | WRIST_TILT_IA_Zpos | WRIST_TILT_IA_Zneg | 0 | 0 |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|---|---|

Table 185. WRIST_TILT_IA register description

| | |
|--------------------|--|
| WRIST_TILT_IA_Xpos | Absolute Wrist Tilt event detection status on X-positive axis. Default value: 0 (0: Absolute Wrist Tilt event on X-positive axis not detected; 1: Absolute Wrist Tilt event on X-positive axis detected) |
| WRIST_TILT_IA_Xneg | Absolute Wrist Tilt event detection status on X-negative axis. Default value: 0 (0: Absolute Wrist Tilt event on X-negative axis not detected; 1: Absolute Wrist Tilt event on X-negative axis detected) |
| WRIST_TILT_IA_Ypos | Absolute Wrist Tilt event detection status on Y-positive axis. Default value: 0 (0: Absolute Wrist Tilt event on Y-positive axis not detected; 1: Absolute Wrist Tilt event on Y-positive axis detected) |
| WRIST_TILT_IA_Yneg | Absolute Wrist Tilt event detection status on Y-negative axis. Default value: 0 (0: Absolute Wrist Tilt event on Y-negative axis not detected; 1: Absolute Wrist Tilt event on Y-negative axis detected) |
| WRIST_TILT_IA_Zpos | Absolute Wrist Tilt event detection status on Z-positive axis. Default value: 0 (0: Absolute Wrist Tilt event on Z-positive axis not detected; 1: Absolute Wrist Tilt event on Z-positive axis detected) |
| WRIST_TILT_IA_Zneg | Absolute Wrist Tilt event detection status on Z-negative axis. Default value: 0 (0: Absolute Wrist Tilt event on Z-negative axis not detected; 1: Absolute Wrist Tilt event on Z-negative axis detected) |

10.75 TAP_CFG (58h)

Enables interrupt and inactivity functions, configuration of filtering, and tap recognition functions (r/w).

Table 186. TAP_CFG register

| INTERRUPTS_ENABLE | INACT_EN1 | INACT_EN0 | SLOPE_FDS | TAP_X_EN | TAP_Y_EN | TAP_Z_EN | LIR |
|-------------------|-----------|-----------|-----------|----------|----------|----------|-----|
|-------------------|-----------|-----------|-----------|----------|----------|----------|-----|

Table 187. TAP_CFG register description

| | |
|-------------------|---|
| INTERRUPTS_ENABLE | Enable basic interrupts (6D/4D, free-fall, wake-up, tap, inactivity). Default value: 0 (0: interrupt disabled; 1: interrupt enabled) |
| INACT_EN[1:0] | Enable inactivity function. Default value: 00 (00: disabled 01: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro does not change; 10: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to sleep mode; 11: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to power-down mode) |
| SLOPE_FDS | HPF or SLOPE filter selection on wake-up and Activity/Inactivity functions. Refer to Figure 9 . Default value: 0 (0: SLOPE filter applied; 1: HPF applied) |
| TAP_X_EN | Enable X direction in tap recognition. Default value: 0 (0: X direction disabled; 1: X direction enabled) |
| TAP_Y_EN | Enable Y direction in tap recognition. Default value: 0 (0: Y direction disabled; 1: Y direction enabled) |
| TAP_Z_EN | Enable Z direction in tap recognition. Default value: 0 (0: Z direction disabled; 1: Z direction enabled) |
| LIR | Latched Interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) |

10.76 TAP_THS_6D (59h)

Portrait/landscape position and tap function threshold register (r/w).

Table 188. TAP_THS_6D register

| | | | | | | | |
|--------|-----------|-----------|----------|----------|----------|----------|----------|
| D4D_EN | SIXD_THS1 | SIXD_THS0 | TAP_THS4 | TAP_THS3 | TAP_THS2 | TAP_THS1 | TAP_THS0 |
|--------|-----------|-----------|----------|----------|----------|----------|----------|

Table 189. TAP_THS_6D register description

| | |
|---------------|--|
| D4D_EN | 4D orientation detection enable. Z-axis position detection is disabled. Default value: 0 (0: enabled; 1: disabled) |
| SIXD_THS[1:0] | Threshold for 4D/6D function. Default value: 00 For details, refer to Table 190 . |
| TAP_THS[4:0] | Threshold for tap recognition. Default value: 00000 1 LSB corresponds to $FS_{XL}/2^5$ |

Table 190. Threshold for D4D/D6D function

| SIXD_THS[1:0] | Threshold value |
|---------------|-----------------|
| 00 | 80 degrees |
| 01 | 70 degrees |
| 10 | 60 degrees |
| 11 | 50 degrees |

10.77 INT_DUR2 (5Ah)

Tap recognition function setting register (r/w).

Table 191. INT_DUR2 register

| | | | | | | | |
|------|------|------|------|--------|--------|--------|--------|
| DUR3 | DUR2 | DUR1 | DUR0 | QUIET1 | QUIET0 | SHOCK1 | SHOCK0 |
|------|------|------|------|--------|--------|--------|--------|

Table 192. INT_DUR2 register description

| | |
|------------|--|
| DUR[3:0] | Duration of maximum time gap for double tap recognition. Default: 0000 When double tap recognition is enabled, this register expresses the maximum time between two consecutive detected taps to determine a double tap event. The default value of these bits is 0000b which corresponds to $16 \cdot ODR_{XL}$ time. If the DUR[3:0] bits are set to a different value, 1LSB corresponds to $32 \cdot ODR_{XL}$ time. |
| QUIET[1:0] | Expected quiet time after a tap detection. Default value: 00 Quiet time is the time after the first detected tap in which there must not be any overthreshold event. The default value of these bits is 00b which corresponds to $2 \cdot ODR_{XL}$ time. If the QUIET[1:0] bits are set to a different value, 1LSB corresponds to $4 \cdot ODR_{XL}$ time. |
| SHOCK[1:0] | Maximum duration of overthreshold event. Default value: 00 Maximum duration is the maximum time of an overthreshold signal detection to be recognized as a tap event. The default value of these bits is 00b which corresponds to $4 \cdot ODR_{XL}$ time. If the SHOCK[1:0] bits are set to a different value, 1LSB corresponds to $8 \cdot ODR_{XL}$ time. |

10.78 WAKE_UP_THS (5Bh)

Single and double-tap function threshold register (r/w).

Table 193. WAKE_UP_THS register

| | | | | | | | |
|-------------------|---|---------|---------|---------|---------|---------|---------|
| SINGLE_DOUBLE_TAP | 0 | WK_THS5 | WK_THS4 | WK_THS3 | WK_THS2 | WK_THS1 | WK_THS0 |
|-------------------|---|---------|---------|---------|---------|---------|---------|

Table 194. WAKE_UP_THS register description

| | |
|-------------------|---|
| SINGLE_DOUBLE_TAP | Single/double-tap event enable. Default: 0 (0: only single-tap event enabled; 1: both single and double-tap events enabled) |
| WK_THS[5:0] | Threshold for wakeup. Default value: 000000 1 LSb corresponds to $FS_{XL}/2^6$ |

10.79 WAKE_UP_DUR (5Ch)

Free-fall, wakeup, timestamp and sleep mode functions duration setting register (r/w).

Table 195. WAKE_UP_DUR register

| | | | | | | | |
|---------|-----------|-----------|----------|------------|------------|------------|------------|
| FF_DUR5 | WAKE_DUR1 | WAKE_DUR0 | TIMER_HR | SLEEP_DUR3 | SLEEP_DUR2 | SLEEP_DUR1 | SLEEP_DUR0 |
|---------|-----------|-----------|----------|------------|------------|------------|------------|

Table 196. WAKE_UP_DUR register description

| | |
|----------------|--|
| FF_DUR5 | Free fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR[4:0] in FREE_FALL (5Dh) configuration. 1 LSB = 1 ODR_time |
| WAKE_DUR[1:0] | Wake up duration event. Default: 00 1LSB = 1 ODR_time |
| TIMER_HR | Timestamp register resolution setting ⁽¹⁾ . Default value: 0 (0: 1LSB = 6.4 ms; 1: 1LSB = 25 μ s) |
| SLEEP_DUR[3:0] | Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR) 1 LSB = 512 ODR |

1. Configuration of this bit affects [TIMESTAMP0_REG \(40h\)](#), [TIMESTAMP1_REG \(41h\)](#), [TIMESTAMP2_REG \(42h\)](#), [STEP_TIMESTAMP_L \(49h\)](#), [STEP_TIMESTAMP_H \(4Ah\)](#), and [STEP_COUNT_DELTA \(15h\)](#) registers.

10.80 FREE_FALL (5Dh)

Free-fall function duration setting register (r/w).

Table 197. FREE_FALL register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| FF_DUR4 | FF_DUR3 | FF_DUR2 | FF_DUR1 | FF_DUR0 | FF_THS2 | FF_THS1 | FF_THS0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

Table 198. FREE_FALL register description

| | |
|-------------|---|
| FF_DUR[4:0] | Free-fall duration event. Default: 0 For the complete configuration of the free fall duration, refer to FF_DUR5 in WAKE_UP_DUR (5Ch) configuration |
| FF_THS[2:0] | Free fall threshold setting. Default: 000 For details refer to Table 199 . |

Table 199. Threshold for free-fall function

| FF_THS[2:0] | Threshold value |
|-------------|-----------------|
| 000 | 156 mg |
| 001 | 219 mg |
| 010 | 250 mg |
| 011 | 312 mg |
| 100 | 344 mg |
| 101 | 406 mg |
| 110 | 469 mg |
| 111 | 500 mg |

10.81 MD1_CFG (5Eh)

Functions routing on INT1 register (r/w).

Table 200. MD1_CFG register

| | | | | | | | |
|------------------|-----------------|---------|---------|-----------------|---------|-----------|------------|
| INT1_INACT_STATE | INT1_SINGLE_TAP | INT1_WU | INT1_FF | INT1_DOUBLE_TAP | INT1_6D | INT1_TILT | INT1_TIMER |
|------------------|-----------------|---------|---------|-----------------|---------|-----------|------------|

Table 201. MD1_CFG register description

| | |
|------------------|---|
| INT1_INACT_STATE | Routing on INT1 of inactivity mode. Default: 0 (0: routing on INT1 of inactivity disabled; 1: routing on INT1 of inactivity enabled) |
| INT1_SINGLE_TAP | Single-tap recognition routing on INT1. Default: 0 (0: routing of single-tap event on INT1 disabled; 1: routing of single-tap event on INT1 enabled) |
| INT1_WU | Routing of wakeup event on INT1. Default value: 0 (0: routing of wakeup event on INT1 disabled; 1: routing of wakeup event on INT1 enabled) |
| INT1_FF | Routing of free-fall event on INT1. Default value: 0 (0: routing of free-fall event on INT1 disabled; 1: routing of free-fall event on INT1 enabled) |
| INT1_DOUBLE_TAP | Routing of tap event on INT1. Default value: 0 (0: routing of double-tap event on INT1 disabled; 1: routing of double-tap event on INT1 enabled) |
| INT1_6D | Routing of 6D event on INT1. Default value: 0 (0: routing of 6D event on INT1 disabled; 1: routing of 6D event on INT1 enabled) |
| INT1_TILT | Routing of tilt event on INT1. Default value: 0 (0: routing of tilt event on INT1 disabled; 1: routing of tilt event on INT1 enabled) |
| INT1_TIMER | Routing of end counter event of timer on INT1. Default value: 0 (0: routing of end counter event of timer on INT1 disabled; 1: routing of end counter event of timer event on INT1 enabled) |

10.82 MD2_CFG (5Fh)

Functions routing on INT2 register (r/w).

Table 202. MD2_CFG register

| | | | | | | | |
|------------------|-----------------|---------|---------|-----------------|---------|-----------|-----------|
| INT2_INACT_STATE | INT2_SINGLE_TAP | INT2_WU | INT2_FF | INT2_DOUBLE_TAP | INT2_6D | INT2_TILT | INT2_IRON |
|------------------|-----------------|---------|---------|-----------------|---------|-----------|-----------|

Table 203. MD2_CFG register description

| | |
|------------------|--|
| INT2_INACT_STATE | Routing on INT2 of inactivity mode. Default: 0 (0: routing on INT2 of inactivity disabled; 1: routing on INT2 of inactivity enabled) |
| INT2_SINGLE_TAP | Single-tap recognition routing on INT2. Default: 0 (0: routing of single-tap event on INT2 disabled; 1: routing of single-tap event on INT2 enabled) |
| INT2_WU | Routing of wakeup event on INT2. Default value: 0 (0: routing of wakeup event on INT2 disabled; 1: routing of wake-up event on INT2 enabled) |
| INT2_FF | Routing of free-fall event on INT2. Default value: 0 (0: routing of free-fall event on INT2 disabled; 1: routing of free-fall event on INT2 enabled) |
| INT2_DOUBLE_TAP | Routing of tap event on INT2. Default value: 0 (0: routing of double-tap event on INT2 disabled; 1: routing of double-tap event on INT2 enabled) |
| INT2_6D | Routing of 6D event on INT2. Default value: 0 (0: routing of 6D event on INT2 disabled; 1: routing of 6D event on INT2 enabled) |
| INT2_TILT | Routing of tilt event on INT2. Default value: 0 (0: routing of tilt event on INT2 disabled; 1: routing of tilt event on INT2 enabled) |
| INT2_IRON | Routing of soft-iron/hard-iron algorithm end event on INT2. Default value: 0 (0: routing of soft-iron/hard-iron algorithm end event on INT2 disabled; 1: routing of soft-iron/hard-iron algorithm end event on INT2 enabled) |

10.83 MASTER_CMD_CODE (60h)

Table 204. MASTER_CMD_CODE register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MASTER_CMD_CODE7 | MASTER_CMD_CODE6 | MASTER_CMD_CODE5 | MASTER_CMD_CODE4 | MASTER_CMD_CODE3 | MASTER_CMD_CODE2 | MASTER_CMD_CODE1 | MASTER_CMD_CODE0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Table 205. MASTER_CMD_CODE register description

| | |
|----------------------|---|
| MASTER_CMD_CODE[7:0] | Master command code used for stamping for sensor sync. Default value: 0 |
|----------------------|---|

10.84 SENS_SYNC_SPI_ERROR_CODE (61h)

Table 206. SENS_SYNC_SPI_ERROR_CODE register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| ERROR_CODE7 | ERROR_CODE6 | ERROR_CODE5 | ERROR_CODE4 | ERROR_CODE3 | ERROR_CODE2 | ERROR_CODE1 | ERROR_CODE0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 207. SENS_SYNC_SPI_ERROR_CODE register description

| | |
|-----------------|--|
| ERROR_CODE[7:0] | Error code used for sensor synchronization. Default value: 0 |
|-----------------|--|

10.85 OUT_MAG_RAW_X_L (66h)

External magnetometer raw data (r).

Table 208. OUT_MAG_RAW_X_L register

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Table 209. OUT_MAG_RAW_X_L register description

| | |
|--------|---|
| D[7:0] | X-axis external magnetometer value (LSbyte) |
|--------|---|

10.86 OUT_MAG_RAW_X_H (67h)

External magnetometer raw data (r).

Table 210. OUT_MAG_RAW_X_H register

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

Table 211. OUT_MAG_RAW_X_H register description

| | |
|---------|---|
| D[15:8] | X-axis external magnetometer value (MSbyte) |
|---------|---|

10.87 OUT_MAG_RAW_Y_L (68h)

External magnetometer raw data (r).

Table 212. OUT_MAG_RAW_Y_L register

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Table 213. OUT_MAG_RAW_Y_L register description

| | |
|--------|---|
| D[7:0] | Y-axis external magnetometer value (LSbyte) |
|--------|---|

10.88 OUT_MAG_RAW_Y_H (69h)

External magnetometer raw data (r).

Table 214. OUT_MAG_RAW_Y_H register

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

Table 215. OUT_MAG_RAW_Y_H register description

| | |
|---------|---|
| D[15:8] | Y-axis external magnetometer value (MSbyte) |
|---------|---|

10.89 OUT_MAG_RAW_Z_L (6Ah)

External magnetometer raw data (r).

Table 216. OUT_MAG_RAW_Z_L register

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Table 217. OUT_MAG_RAW_Z_L register description

| | |
|--------|---|
| D[7:0] | Z-axis external magnetometer value (LSbyte) |
|--------|---|

10.90 OUT_MAG_RAW_Z_H (6Bh)

External magnetometer raw data (r).

Table 218. OUT_MAG_RAW_Z_H register

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

Table 219. OUT_MAG_RAW_Z_H register description

| | |
|---------|---|
| D[15:8] | Z-axis external magnetometer value (MSbyte) |
|---------|---|

10.91 INT_OIS (6Fh)

OIS interrupt configuration register. Primary interface for read-only (r); only Aux SPI can write to this register (r/w).

Table 220. INT_OIS register

| | | | | | | | |
|---------------|----------|---|---|---|---|---|---|
| INT2_DRDY_OIS | LVL2_OIS | - | - | - | - | - | - |
|---------------|----------|---|---|---|---|---|---|

Table 221. INT_OIS register description

| | |
|---------------|---|
| INT2_DRDY_OIS | Enables the OIS chain DRDY on the INT2 pad. This setting has priority over all other INT2 settings. |
| LVL2_OIS | Enables level-sensitive latched mode on the OIS chain. Default value: 0 |

10.92 CTRL1_OIS (70h)

OIS configuration register. Primary interface for read-only (r); only Aux SPI can write to this register (r/w).

Table 222. CTRL1_OIS register

| | | | | | | | |
|---------|----------|---------|----------|-----------|-----------|------------|-------------|
| BLE_OIS | LVL1_OIS | SIM_OIS | MODE4_EN | FS1_G_OIS | FS0_G_OIS | FS_125_OIS | OIS_EN_SPI2 |
|---------|----------|---------|----------|-----------|-----------|------------|-------------|

Table 223. CTRL1_OIS register description

| | |
|---------------|--|
| BLE_OIS | Big/Little Endian data selection. Default value: 0 (0: output LSbyte at lower register address; 1: output LSbyte at higher register address) |
| LVL1_OIS | Enables level-sensitive trigger mode on OIS chain. Default value: 0 |
| SIM_OIS | SPI2 3- or 4-wire mode. Default value: 0 (0: 4-wire SPI2; 1: 3-wire SPI2) |
| MODE4_EN | Enables accelerometer OIS chain if OIS_EN_SPI2 = 1. Default value: 0 (0: disable; 1: enable) |
| FS[1:0]_G_OIS | Gyroscope OIS chain full-scale selection. (00: 250 dps; 01: 500 dps; 10: 1000 dps; 11: 2000 dps) |
| FS_125_OIS | Selects gyroscope's OIS chain full scale 125 dps (0: FS selected through bits FS[1:0]_G_OIS; 1 = 125 dps) |
| OIS_EN_SPI2 | Enables OIS chain data processing for gyro in Mode 3 and Mode 4 (mode4_en = 1) and accelerometer data in and Mode 4 (mode4_en = 1). When the OIS chain is enabled, the OIS outputs are available through the SPI2 in registers <i>OUTX_L_G (22h)</i> through <i>OUTZ_H_G (27h)</i> and <i>STATUS_REG/STATUS_SPIAux (1Eh)</i> , and LPF1 is dedicated to this chain. |

DEN mode selection can be done using the LVL1_OIS bit of register [CTRL1_OIS \(70h\)](#) and the LVL2_OIS bit of register [INT_OIS \(6Fh\)](#).

DEN mode on the OIS path is active in the gyroscope only.

Table 224. DEN mode selection

| LVL1_OIS, LVL2_OIS | DEN mode |
|--------------------|--|
| 10 | Level-sensitive trigger mode is selected |
| 11 | Level-sensitive latched mode is selected |

10.93 CTRL2_OIS (71h)

OIS configuration register. Primary interface for read-only (r); only Aux SPI can write to this register (r/w).

Table 225. CTRL2_OIS register

| | | | | | | | |
|------------------|------------------|----------|----------|------------------|-------------|-------------|-----------|
| 0 ⁽¹⁾ | 0 ⁽¹⁾ | HPM1_OIS | HPM0_OIS | 0 ⁽¹⁾ | FTYPE_1_OIS | FTYPE_0_OIS | HP_EN_OIS |
|------------------|------------------|----------|----------|------------------|-------------|-------------|-----------|

1. This bit must be set to '0' for the correct operation of the device.

Table 226. CTRL2_OIS register description

| | |
|-----------------|--|
| HPM[1:0]_OIS | Gyroscope's OIS chain digital high-pass filter cutoff selection. Default value: 00 (00: 16 mHz; 01: 65 mHz; 10: 260 mHz; 11: 1.04 Hz) |
| FTYPE_[1:0]_OIS | Gyroscope's digital LPF1 filter bandwidth selection Table 227 shows cutoff and phase values obtained with all configurations |
| HP_EN_OIS | Enables gyroscope's OIS chain HPF. This filter is available on the OIS chain only if HP_EN_G in CTRL7_G (16h) is set to '0' ⁽¹⁾ . |

1. HP_EN_OIS is active to select HPF on the auxiliary SPI chain only if HPF is not already used in the primary interface.

Table 227. Gyroscope OIS chain LPF1 bandwidth selection

| FTYPE_[1:0]_OIS | ODR = 6.6 kHz | |
|-----------------|---------------|---------------------|
| | BW | Phase delay @ 20 Hz |
| 00 | 351 Hz | 7° |
| 01 | 237 Hz | 9° |
| 10 | 173 Hz | 11° |
| 11 | 937 Hz | 5° |

Sampling data with frequency equal or higher to 3.3 kHz is recommended.

If data is down-sampled @ 1 kHz, it is recommended to use a cutoff @ 173 Hz.

If data is down-sampled @ 2 kHz, it is recommended to use a cutoff @ 237 Hz.

10.94 CTRL3_OIS (72h)

OIS configuration register. Primary interface for read-only (r); only Aux SPI can write to this register (r/w).

Table 228. CTRL3_OIS register

| | | | | | | | |
|------------|------------|------------|----------------------|----------------------|---------|---------|-----------------|
| DEN_LH_OIS | FS1_XL_OIS | FS0_XL_OIS | FILTER_XL_CONF_OIS_1 | FILTER_XL_CONF_OIS_0 | ST1_OIS | ST0_OIS | ST_OIS_CLAMPDIS |
|------------|------------|------------|----------------------|----------------------|---------|---------|-----------------|

Table 229. CTRL3_OIS register description

| | |
|--------------------------|--|
| DEN_LH_OIS | Polarity of DEN signal on OIS chain (0: DEN pin is active-low; 1: DEN pin is active-high) |
| FS[1:0]_XL_OIS | Accelerometer OIS channel full-scale selection. Default value: 00 (00: 2 g; 01: 16 g; 10: 4 g; 11: 8 g) These two bits act only when the accelerometer UI chain is in power-down, otherwise the accelerometer FS value is selected only from the UI side (but it is readable also from the OIS side). |
| FILTER_XL_CONF_OIS [1:0] | Accelerometer OIS channel bandwidth selection (see Table 230) |
| ST[1:0]_OIS | Gyroscope OIS chain self-test selection Table 231 lists the output variation when the self-test is enabled and ST_OIS_CLAMPDIS = '1'. Default value: 00 (00: Normal mode; 01: Positive sign self-test; 10: Normal mode; 11: Negative sign self-test) |
| ST_OIS_CLAMPDIS | Gyro OIS chain clamp disable (0: All gyro OIS chain outputs = 8000h during self-test applied from primary interface; 1: OIS chain self-test outputs as shown in Table 231 if self-test applied from primary or auxiliary interfaces) |

Table 230. Accelerometer OIS channel bandwidth selection

| FILTER_XL_CONF_OIS [1:0] | ODR_UI = 0 ODR UI ≥ 1600 Hz | | ODR UI ≤ 800 Hz | |
|--------------------------|--------------------------------|----------------------------|-----------------|----------------------------|
| | BW | Phase delay ⁽¹⁾ | BW | Phase delay ⁽¹⁾ |
| 00 | 140 Hz | 9.39° | 128 Hz | 11.5° |
| 01 | 68.2 Hz | 17.6° | 66.5 Hz | 19.7° |
| 10 | 636 Hz | 2.96° | 329 Hz | 5.08° |
| 11 | 295 Hz | 5.12° | 222 Hz | 7.23° |

1. Phase delay @ 20 Hz

Table 231. Self-test nominal output variation

| Full scale | Output variation [dps] |
|------------|------------------------|
| 2000 | 400 |
| 1000 | 200 |
| 500 | 100 |
| 250 | 50 |
| 125 | 25 |

10.95 X_OFS_USR (73h)

Accelerometer X-axis user offset correction (r/w). The offset value set in the X_OFS_USR offset register is internally added to the acceleration value measured on the X-axis.

Table 232. X_OFS_USR register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| X_OFS_USR_7 | X_OFS_USR_6 | X_OFS_USR_5 | X_OFS_USR_4 | X_OFS_USR_3 | X_OFS_USR_2 | X_OFS_USR_1 | X_OFS_USR_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 233. X_OFS_USR register description

| | |
|---------------|---|
| X_OFS_USR_7:0 | Accelerometer X-axis user offset correction expressed in two's complement, weight depends on the CTRL6_C(4) bit. The value must be in the range [-127 127]. |
|---------------|---|

10.96 Y_OFS_USR (74h)

Accelerometer Y-axis user offset correction (r/w). The offset value set in the Y_OFS_USR offset register is internally added to the acceleration value measured on the Y-axis.

Table 234. Y_OFS_USR register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Y_OFS_USR_7 | Y_OFS_USR_6 | Y_OFS_USR_5 | Y_OFS_USR_4 | Y_OFS_USR_3 | Y_OFS_USR_2 | Y_OFS_USR_1 | Y_OFS_USR_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 235. Y_OFS_USR register description

| | |
|---------------|---|
| Y_OFS_USR_7:0 | Accelerometer Y-axis user offset correction expressed in two's complement, weight depends on the CTRL6_C(4) bit. The value must be in the range [-127 127]. |
|---------------|---|

10.97 Z_OFS_USR (75h)

Accelerometer Z-axis user offset correction (r/w). The offset value set in the Z_OFS_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

Table 236. Z_OFS_USR register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Z_OFS_USR_7 | Z_OFS_USR_6 | Z_OFS_USR_5 | Z_OFS_USR_4 | Z_OFS_USR_3 | Z_OFS_USR_2 | Z_OFS_USR_1 | Z_OFS_USR_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 237. Z_OFS_USR register description

| | |
|---------------|---|
| Z_OFS_USR_7:0 | Accelerometer Z-axis user offset correction expressed in two's complement, weight depends on the CTRL6_C(4) bit. The value must be in the range [-127 127]. |
|---------------|---|

11 Embedded functions register mapping

The tables given below provide a list of the first (A) and second (B) bank registers related to the embedded functions available in the device and the corresponding addresses.

The embedded functions registers of bank A are accessible when FUNC_CFG_EN is set to '1' in [FUNC_CFG_ACCESS \(01h\)](#).

The embedded functions registers of bank B are accessible when both FUNC_CFG_EN and FUNC_CFG_EN_B set to '1' in [FUNC_CFG_ACCESS \(01h\)](#).

Note: All modifications of the content of the embedded functions registers have to be performed with the device in power-down mode.

Table 238. Register address map - Bank A - embedded functions

| Name | Type | Register address | | Default | Comment |
|-----------------------------|------|------------------|-----------|----------|----------|
| | | Hex | Binary | | |
| SLV0_ADD | r/w | 02 | 00000010 | 00000000 | |
| SLV0_SUBADD | r/w | 03 | 00000011 | 00000000 | |
| SLAVE0_CONFIG | r/w | 04 | 00000100 | 00000000 | |
| SLV1_ADD | r/w | 05 | 00000101 | 00000000 | |
| SLV1_SUBADD | r/w | 06 | 00000110 | 00000000 | |
| SLAVE1_CONFIG | r/w | 07 | 00000111 | 00000000 | |
| SLV2_ADD | r/w | 08 | 00001000 | 00000000 | |
| SLV2_SUBADD | r/w | 09 | 00001001 | 00000000 | |
| SLAVE2_CONFIG | r/w | 0A | 00001010 | 00000000 | |
| SLV3_ADD | r/w | 0B | 00001011 | 00000000 | |
| SLV3_SUBADD | r/w | 0C | 00001100 | 00000000 | |
| SLAVE3_CONFIG | r/w | 0D | 00001101 | 00000000 | |
| DATAWRITE_SRC_MODE_SUB_SLV0 | r/w | 0E | 00001110 | 00000000 | |
| CONFIG_PEDO_THS_MIN | r/w | 0F | 00001111 | 00010000 | |
| RESERVED | - | 10-12 | | - | Reserved |
| SM_THS | r/w | 13 | 00010011 | 00000110 | |
| PEDO_DEB_REG | r/w | 14 | 00010100 | 01101110 | |
| STEP_COUNT_DELTA | r/w | 15 | 0001 0101 | 00000000 | |
| MAG_SI_XX | r/w | 24 | 00100100 | 00001000 | |
| MAG_SI_XY | r/w | 25 | 00100101 | 00000000 | |
| MAG_SI_XZ | r/w | 26 | 00100110 | 00000000 | |
| MAG_SI_YX | r/w | 27 | 00100111 | 00000000 | |
| MAG_SI_YY | r/w | 28 | 00101000 | 00001000 | |

Table 238. Register address map - Bank A - embedded functions (continued)

| Name | Type | Register address | | Default | Comment |
|------------|------|------------------|----------|----------|---------|
| | | Hex | Binary | | |
| MAG_SI_YZ | r/w | 29 | 00101001 | 00000000 | |
| MAG_SI_ZX | r/w | 2A | 00101010 | 00000000 | |
| MAG_SI_ZY | r/w | 2B | 00101011 | 00000000 | |
| MAG_SI_ZZ | r/w | 2C | 00101100 | 00001000 | |
| MAG_OFFX_L | r/w | 2D | 00101101 | 00000000 | |
| MAG_OFFX_H | r/w | 2E | 00101110 | 00000000 | |
| MAG_OFFY_L | r/w | 2F | 00101111 | 00000000 | |
| MAG_OFFY_H | r/w | 30 | 00110000 | 00000000 | |
| MAG_OFFZ_L | r/w | 31 | 00110001 | 00000000 | |
| MAG_OFFZ_H | r/w | 32 | 00110010 | 00000000 | |

Table 239. Register address map - Bank B - embedded functions

| Name | Type | Register address | | Default | Comment |
|-------------------|------|------------------|----------|----------|----------|
| | | Hex | Binary | | |
| A_WRIST_TILT_LAT | r/w | 50 | 01010000 | 00001111 | |
| RESERVED | - | 51-53 | | | Reserved |
| A_WRIST_TILT_THS | r/w | 54 | 01010100 | 00100000 | |
| RESERVED | - | 55-58 | | | Reserved |
| A_WRIST_TILT_Mask | r/w | 59 | 01011001 | 11000000 | |

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

12 Embedded functions registers description - Bank A

Note: All modifications of the content of the embedded functions registers have to be performed with the device in power-down mode.

12.1 SLV0_ADD (02h)

I²C slave address of the first external sensor (Sensor1) register (r/w).

Table 240. SLV0_ADD register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|
| Slave0_add6 | Slave0_add5 | Slave0_add4 | Slave0_add3 | Slave0_add2 | Slave0_add1 | Slave0_add0 | rw_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|

Table 241. SLV0_ADD register description

| | |
|-----------------|---|
| Slave0_add[6:0] | I ² C slave address of Sensor1 that can be read by sensor hub. Default value: 0000000 |
| rw_0 | Read/write operation on Sensor1. Default value: 0 (0: write operation; 1: read operation) |

12.2 SLV0_SUBADD (03h)

Address of register on the first external sensor (Sensor1) register (r/w).

Table 242. SLV0_SUBADD register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave0_reg7 | Slave0_reg6 | Slave0_reg5 | Slave0_reg4 | Slave0_reg3 | Slave0_reg2 | Slave0_reg1 | Slave0_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 243. SLV0_SUBADD register description

| | |
|-----------------|--|
| Slave0_reg[7:0] | Address of register on Sensor1 that has to be read/write according to the rw_0 bit value in SLV0_ADD (02h) . Default value: 00000000 |
|-----------------|--|

12.3 SLAVE0_CONFIG (04h)

First external sensor (Sensor1) configuration and sensor hub settings register (r/w).

Table 244. SLAVE0_CONFIG register

| | | | | | | | |
|--------------|--------------|--------------|--------------|----------|---------------|---------------|---------------|
| Slave0_rate1 | Slave0_rate0 | Aux_sens_on1 | Aux_sens_on0 | Src_mode | Slave0_numop2 | Slave0_numop1 | Slave0_numop0 |
|--------------|--------------|--------------|--------------|----------|---------------|---------------|---------------|

Table 245. SLAVE0_CONFIG register description

| | |
|-------------------|---|
| Slave0_rate[1:0] | Decimation of read operation on Sensor1 starting from the sensor hub trigger. Default value: 00 (00: no decimation 01: update every 2 samples 10: update every 4 samples 11: update every 8 samples) |
| Aux_sens_on[1:0] | Number of external sensors to be read by sensor hub. Default value: 00 (00: one sensor 01: two sensors 10: three sensors 11: four sensors) |
| Src_mode | Source mode conditioned read ⁽¹⁾ . Default value: 0 (0: source mode read disabled; 1: source mode read enabled) |
| Slave0_numop[2:0] | Number of read operations on Sensor1. |

1. Read conditioned by the content of the register at address specified in the [DATAWRITE_SRC_MODE_SUB_SLV0 \(0Eh\)](#) register. If the content is non-zero, the operation continues with the reading of the address specified in the [SLV0_SUBADD \(03h\)](#) register, else the operation is interrupted.

12.4 SLV1_ADD (05h)

I²C slave address of the second external sensor (Sensor2) register (r/w).

Table 246. SLV1_ADD register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| Slave1_add6 | Slave1_add5 | Slave1_add4 | Slave1_add3 | Slave1_add2 | Slave1_add1 | Slave1_add0 | r_1 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|

Table 247. SLV1_ADD register description

| | |
|-----------------|---|
| Slave1_add[6:0] | I ² C slave address of Sensor2 that can be read by sensor hub. Default value: 0000000 |
| r_1 | Read operation on Sensor2 enable. Default value: 0 (0: read operation disabled; 1: read operation enabled) |

12.5 SLV1_SUBADD (06h)

Address of register on the second external sensor (Sensor2) register (r/w).

Table 248. SLV1_SUBADD register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave1_reg7 | Slave1_reg6 | Slave1_reg5 | Slave1_reg4 | Slave1_reg3 | Slave1_reg2 | Slave1_reg1 | Slave1_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 249. SLV1_SUBADD register description

| | |
|-----------------|---|
| Slave1_reg[7:0] | Address of register on Sensor2 that has to be read according to the r_1 bit value in SLV1_ADD (05h) . Default value: 00000000 |
|-----------------|---|

12.6 SLAVE1_CONFIG (07h)

Second external sensor (Sensor2) configuration register (r/w).

Table 250. SLAVE1_CONFIG register

| | | | | | | | |
|--------------|--------------|------------|------------------|------------------|---------------|---------------|---------------|
| Slave1_rate1 | Slave1_rate0 | write_once | 0 ⁽¹⁾ | 0 ⁽¹⁾ | Slave1_numop2 | Slave1_numop1 | Slave1_numop0 |
|--------------|--------------|------------|------------------|------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 251. SLAVE1_CONFIG register description

| | |
|-------------------|---|
| Slave1_rate[1:0] | Decimation of read operation on Sensor2 starting from the sensor hub trigger. Default value: 00 (00: no decimation 01: update every 2 samples 10: update every 4 samples 11: update every 8 samples) |
| write_once | Slave 0 write operation is performed only at the first sensor hub cycle. ⁽¹⁾ Default value: 0 0: write operation for each sensor hub cycle 1: write operation only for the first sensor hub cycle |
| Slave1_numop[2:0] | Number of read operations on Sensor2. |

1. This is effective if the Aux_sens_on[1:0] field in [SLAVE0_CONFIG \(04h\)](#) is set to a value other than 00.

12.7 SLV2_ADD (08h)

I²C slave address of the third external sensor (Sensor3) register (r/w).

Table 252. SLV2_ADD register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| Slave2_add6 | Slave2_add5 | Slave2_add4 | Slave2_add3 | Slave2_add2 | Slave2_add1 | Slave2_add0 | r_2 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|

Table 253. SLV2_ADD register description

| | |
|-----------------|---|
| Slave2_add[6:0] | I ² C slave address of Sensor3 that can be read by sensor hub. Default value: 0000000 |
| r_2 | Read operation on Sensor3 enable. Default value: 0 (0: read operation disabled; 1: read operation enabled) |

12.8 SLV2_SUBADD (09h)

Address of register on the third external sensor (Sensor3) register (r/w).

Table 254. SLV2_SUBADD register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave2_reg7 | Slave2_reg6 | Slave2_reg5 | Slave2_reg4 | Slave2_reg3 | Slave2_reg2 | Slave2_reg1 | Slave2_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 255. SLV2_SUBADD register description

| | |
|-----------------|---|
| Slave2_reg[7:0] | Address of register on Sensor3 that has to be read according to the r_2 bit value in SLV2_ADD (08h) . Default value: 00000000 |
|-----------------|---|

12.9 SLAVE2_CONFIG (0Ah)

Third external sensor (Sensor3) configuration register (r/w).

Table 256. SLAVE2_CONFIG register

| | | | | | | | |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|
| Slave2_rate1 | Slave2_rate0 | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | Slave2_numop2 | Slave2_numop1 | Slave2_numop0 |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 257. SLAVE2_CONFIG register description

| | |
|-------------------|---|
| Slave2_rate[1:0] | Decimation of read operation on Sensor3 starting from the sensor hub trigger. Default value: 00 (00: no decimation 01: update every 2 samples 10: update every 4 samples 11: update every 8 samples) |
| Slave2_numop[2:0] | Number of read operations on Sensor3. |

12.10 SLV3_ADD (0Bh)

I²C slave address of the fourth external sensor (Sensor4) register (r/w).

Table 258. SLV3_ADD register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| Slave3_add6 | Slave3_add5 | Slave3_add4 | Slave3_add3 | Slave3_add2 | Slave3_add1 | Slave3_add0 | r_3 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|

Table 259. SLV3_ADD register description

| | |
|-----------------|---|
| Slave3_add[6:0] | I ² C slave address of Sensor4 that can be read by the sensor hub. Default value: 0000000 |
| r_3 | Read operation on Sensor4 enable. Default value: 0 (0: read operation disabled; 1: read operation enabled) |

12.11 SLV3_SUBADD (0Ch)

Address of register on the fourth external sensor (Sensor4) register (r/w).

Table 260. SLV3_SUBADD register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave3_reg7 | Slave3_reg6 | Slave3_reg5 | Slave3_reg4 | Slave3_reg3 | Slave3_reg2 | Slave3_reg1 | Slave3_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 261. SLV3_SUBADD register description

| | |
|-----------------|---|
| Slave3_reg[7:0] | Address of register on Sensor4 that has to be read according to the r_3 bit value in SLV3_ADD (0Bh) . Default value: 00000000 |
|-----------------|---|

12.12 SLAVE3_CONFIG (0Dh)

Fourth external sensor (Sensor4) configuration register (r/w).

Table 262. SLAVE3_CONFIG register

| | | | | | | | |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|
| Slave3_rate1 | Slave3_rate0 | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | Slave3_numop2 | Slave3_numop1 | Slave3_numop0 |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

Table 263. SLAVE3_CONFIG register description

| | |
|-------------------|---|
| Slave3_rate[1:0] | Decimation of read operation on Sensor4 starting from the sensor hub trigger. Default value: 00 (00: no decimation 01: update every 2 samples 10: update every 4 samples 11: update every 8 samples) |
| Slave3_numop[2:0] | Number of read operations on Sensor4. |

12.13 DATAWRITE_SRC_MODE_SUB_SLV0 (0Eh)

Data to be written into the slave device register (r/w).

Table 264. DATAWRITE_SRC_MODE_SUB_SLV0 register

| | | | | | | | |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Slave_dataw7 | Slave_dataw6 | Slave_dataw5 | Slave_dataw4 | Slave_dataw3 | Slave_dataw2 | Slave_dataw1 | Slave_dataw0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

Table 265. DATAWRITE_SRC_MODE_SUB_SLV0 register description

| | |
|------------------|--|
| Slave_dataw[7:0] | Data to be written into the slave device according to the rw_0 bit in SLV0_ADD (02h) register or address to be read in source mode. Default value: 00000000 |
|------------------|--|

12.14 CONFIG_PEDO_THS_MIN (0Fh)

Table 266. CONFIG_PEDO_THS_MIN register

| | | | | | | | |
|---------|---|---|-----------|-----------|-----------|-----------|-----------|
| PEDO_FS | 0 | 0 | ths_min_4 | ths_min_3 | ths_min_2 | ths_min_1 | ths_min_0 |
|---------|---|---|-----------|-----------|-----------|-----------|-----------|

Table 267. CONFIG_PEDO_THS_MIN register description

| | |
|---------------|---|
| PEDO_FS | Pedometer data elaboration at 4 g. (0: elaboration of 2 g data; 1: elaboration of 4 g data) |
| ths_min_[4:0] | Minimum threshold to detect a peak. Default is 10h. |

12.15 SM_THS (13h)

Significant motion configuration register (r/w).

Table 268. SM_THS register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SM_THS_7 | SM_THS_6 | SM_THS_5 | SM_THS_4 | SM_THS_3 | SM_THS_2 | SM_THS_1 | SM_THS_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

Table 269. SM_THS register description

| | |
|-------------|---|
| SM_THS[7:0] | Significant motion threshold. Default value: 00000110 |
|-------------|---|

12.16 PEDO_DEB_REG (14h)

Table 270. PEDO_DEB_REG register

| | | | | | | | |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| DEB_TIME4 | DEB_TIME3 | DEB_TIME2 | DEB_TIME1 | DEB_TIME0 | DEB_STEP2 | DEB_STEP1 | DEB_STEP0 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

Table 271. PEDO_DEB_REG register description

| | |
|---------------|--|
| DEB_TIME[4:0] | Debounce time. If the time between two consecutive steps is greater than DEB_TIME*80ms, the debouncer is reactivated. Default value: 01101 |
| DEB_STEP[2:0] | Debounce threshold. Minimum number of steps to increment step counter (debounce). Default value: 110 |

12.17 STEP_COUNT_DELTA (15h)

Time period register for step detection on delta time (r/w).

Table 272. STEP_COUNT_DELTA register

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| SC_DELTA_7 | SC_DELTA_6 | SC_DELTA_5 | SC_DELTA_4 | SC_DELTA_3 | SC_DELTA_2 | SC_DELTA_1 | SC_DELTA_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

Table 273. STEP_COUNT_DELTA register description

| | |
|---------------|--|
| SC_DELTA[7:0] | Time period value ⁽¹⁾ (1LSB = 1.6384 s) |
|---------------|--|

1. This value is effective if the TIMER_EN bit of [CTRL10_C \(19h\)](#) is set to 1 and the TIMER_HR bit of [WAKE_UP_DUR \(5Ch\)](#) is set to 0.

12.18 MAG_SI_XX (24h)

Soft-iron matrix correction register (r/w).

Table 274. MAG_SI_XX register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_XX_7 | MAG_SI_XX_6 | MAG_SI_XX_5 | MAG_SI_XX_4 | MAG_SI_XX_3 | MAG_SI_XX_2 | MAG_SI_XX_1 | MAG_SI_XX_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 275. MAG_SI_XX register description

| | |
|----------------|---|
| MAG_SI_XX[7:0] | Soft-iron correction row1 col1 coefficient ⁽¹⁾ . Default value: 00001000 |
|----------------|---|

1. Value is expressed in sign-module format.

12.19 MAG_SI_XY (25h)

Soft-iron matrix correction register (r/w).

Table 276. MAG_SI_XY register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_XY_7 | MAG_SI_XY_6 | MAG_SI_XY_5 | MAG_SI_XY_4 | MAG_SI_XY_3 | MAG_SI_XY_2 | MAG_SI_XY_1 | MAG_SI_XY_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 277. MAG_SI_XY register description

| | |
|----------------|---|
| MAG_SI_XY[7:0] | Soft-iron correction row1 col2 coefficient ⁽¹⁾ . Default value: 00000000 |
|----------------|---|

1. Value is expressed in sign-module format.

12.20 MAG_SI_XZ (26h)

Soft-iron matrix correction register (r/w).

Table 278. MAG_SI_XZ register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_XZ_7 | MAG_SI_XZ_6 | MAG_SI_XZ_5 | MAG_SI_XZ_4 | MAG_SI_XZ_3 | MAG_SI_XZ_2 | MAG_SI_XZ_1 | MAG_SI_XZ_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 279. MAG_SI_XZ register description

| | |
|----------------|---|
| MAG_SI_XZ[7:0] | Soft-iron correction row1 col3 coefficient ⁽¹⁾ . Default value: 00000000 |
|----------------|---|

1. Value is expressed in sign-module format.

12.21 MAG_SI_YX (27h)

Soft-iron matrix correction register (r/w).

Table 280. MAG_SI_YX register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_YX_7 | MAG_SI_YX_6 | MAG_SI_YX_5 | MAG_SI_YX_4 | MAG_SI_YX_3 | MAG_SI_YX_2 | MAG_SI_YX_1 | MAG_SI_YX_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 281. MAG_SI_YX register description

| | |
|----------------|---|
| MAG_SI_YX[7:0] | Soft-iron correction row2 col1 coefficient ⁽¹⁾ . Default value: 00000000 |
|----------------|---|

1. Value is expressed in sign-module format.

12.22 MAG_SI_YY (28h)

Soft-iron matrix correction register (r/w).

Table 282. MAG_SI_YY register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_YY_7 | MAG_SI_YY_6 | MAG_SI_YY_5 | MAG_SI_YY_4 | MAG_SI_YY_3 | MAG_SI_YY_2 | MAG_SI_YY_1 | MAG_SI_YY_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 283. MAG_SI_YY register description

| | |
|----------------|---|
| MAG_SI_YY[7:0] | Soft-iron correction row2 col2 coefficient ⁽¹⁾ . Default value: 00001000 |
|----------------|---|

1. Value is expressed in sign-module format.

12.23 MAG_SI_YZ (29h)

Soft-iron matrix correction register (r/w).

Table 284. MAG_SI_YZ register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_YZ_7 | MAG_SI_YZ_6 | MAG_SI_YZ_5 | MAG_SI_YZ_4 | MAG_SI_YZ_3 | MAG_SI_YZ_2 | MAG_SI_YZ_1 | MAG_SI_YZ_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 285. MAG_SI_YZ register description

| | |
|----------------|---|
| MAG_SI_YZ[7:0] | Soft-iron correction row2 col3 coefficient ⁽¹⁾ . Default value: 00000000 |
|----------------|---|

1. Value is expressed in sign-module format.

12.24 MAG_SI_ZX (2Ah)

Soft-iron matrix correction register (r/w).

Table 286. MAG_SI_ZX register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_ZX_7 | MAG_SI_ZX_6 | MAG_SI_ZX_5 | MAG_SI_ZX_4 | MAG_SI_ZX_3 | MAG_SI_ZX_2 | MAG_SI_ZX_1 | MAG_SI_ZX_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 287. MAG_SI_ZX register description

| | |
|----------------|---|
| MAG_SI_ZX[7:0] | Soft-iron correction row3 col1 coefficient ⁽¹⁾ . Default value: 00000000 |
|----------------|---|

1. Value is expressed in sign-module format.

12.25 MAG_SI_ZY (2Bh)

Soft-iron matrix correction register (r/w).

Table 288. MAG_SI_ZY register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_ZY_7 | MAG_SI_ZY_6 | MAG_SI_ZY_5 | MAG_SI_ZY_4 | MAG_SI_ZY_3 | MAG_SI_ZY_2 | MAG_SI_ZY_1 | MAG_SI_ZY_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 289. MAG_SI_ZY register description

| | |
|----------------|---|
| MAG_SI_ZY[7:0] | Soft-iron correction row3 col2 coefficient ⁽¹⁾ . Default value: 00000000 |
|----------------|---|

1. Value is expressed in sign-module format.

12.26 MAG_SI_ZZ (2Ch)

Soft-iron matrix correction register (r/w).

Table 290. MAG_SI_ZZ register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_ZZ_7 | MAG_SI_ZZ_6 | MAG_SI_ZZ_5 | MAG_SI_ZZ_4 | MAG_SI_ZZ_3 | MAG_SI_ZZ_2 | MAG_SI_ZZ_1 | MAG_SI_ZZ_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

Table 291. MAG_SI_ZZ register description

| | |
|----------------|---|
| MAG_SI_ZZ[7:0] | Soft-iron correction row3 col3 coefficient ⁽¹⁾ . Default value: 00001000 |
|----------------|---|

1. Value is expressed in sign-module format.

12.27 MAG_OFFX_L (2Dh)

Offset for X-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

Table 292. MAG_OFFX_L register

| | | | | | | | |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| MAG_OFF_X_L_7 | MAG_OFF_X_L_6 | MAG_OFF_X_L_5 | MAG_OFF_X_L_4 | MAG_OFF_X_L_3 | MAG_OFF_X_L_2 | MAG_OFF_X_L_1 | MAG_OFF_X_L_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

Table 293. MAG_OFFX_L register description

| | |
|-----------------|---|
| MAG_OFFX_L[7:0] | Offset for X-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

12.28 MAG_OFFX_H (2Eh)

Offset for X-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

Table 294. MAG_OFFX_H register

| | | | | | | | |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| MAG_OFF_X_H_7 | MAG_OFF_X_H_6 | MAG_OFF_X_H_5 | MAG_OFF_X_H_4 | MAG_OFF_X_H_3 | MAG_OFF_X_H_2 | MAG_OFF_X_H_1 | MAG_OFF_X_H_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

Table 295. MAG_OFFX_H register description

| | |
|-----------------|---|
| MAG_OFFX_H[7:0] | Offset for X-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

12.29 MAG_OFFY_L (2Fh)

Offset for Y-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

Table 296. MAG_OFFY_L register

| | | | | | | | |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| MAG_OFF_Y_L_7 | MAG_OFF_Y_L_6 | MAG_OFF_Y_L_5 | MAG_OFF_Y_L_4 | MAG_OFF_Y_L_3 | MAG_OFF_Y_L_2 | MAG_OFF_Y_L_1 | MAG_OFF_Y_L_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

Table 297. MAG_OFFY_L register description

| | |
|-----------------|---|
| MAG_OFFY_L[7:0] | Offset for Y-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

12.30 MAG_OFFY_H (30h)

Offset for Y-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

Table 298. MAG_OFFY_H register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MAG_OFF Y_H_7 | MAG_OFF Y_H_6 | MAG_OFF Y_H_5 | MAG_OFF Y_H_4 | MAG_OFF Y_H_3 | MAG_OFF Y_H_2 | MAG_OFF Y_H_1 | MAG_OFF Y_H_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Table 299. MAG_OFFY_H register description

| | |
|-----------------|---|
| MAG_OFFY_H[7:0] | Offset for Y-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

12.31 MAG_OFFZ_L (31h)

Offset for Z-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

Table 300. MAG_OFFZ_L register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MAG_OFF Z_L_7 | MAG_OFF Z_L_6 | MAG_OFF Z_L_5 | MAG_OFF Z_L_4 | MAG_OFF Z_L_3 | MAG_OFF Z_L_2 | MAG_OFF Z_L_1 | MAG_OFF Z_L_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Table 301. MAG_OFFZ_L register description

| | |
|-----------------|---|
| MAG_OFFZ_L[7:0] | Offset for Z-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

12.32 MAG_OFFZ_H (32h)

Offset for Z-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

Table 302. MAG_OFFZ_H register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MAG_OFF Z_H_7 | MAG_OFF Z_H_6 | MAG_OFF Z_H_5 | MAG_OFF Z_H_4 | MAG_OFF Z_H_3 | MAG_OFF Z_H_2 | MAG_OFF Z_H_1 | MAG_OFF Z_H_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Table 303. MAG_OFFZ_H register description

| | |
|-----------------|---|
| MAG_OFFZ_H[7:0] | Offset for Z-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

13 Embedded functions registers description - Bank B

13.1 A_WRIST_TILT_LAT (50h)

Absolute Wrist Tilt latency register (r/w).

Table 304. A_WRIST_TILT_LAT register

| | | | | | | | |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| WRIST_TILT_TIMER7 | WRIST_TILT_TIMER6 | WRIST_TILT_TIMER5 | WRIST_TILT_TIMER4 | WRIST_TILT_TIMER3 | WRIST_TILT_TIMER2 | WRIST_TILT_TIMER1 | WRIST_TILT_TIMER0 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|

Table 305. A_WRIST_TILT_LAT register description

| | |
|-----------------------|---|
| WRIST_TILT_TIMER[7:0] | Absolute wrist tilt latency parameters. 1 LSB = 40 ms. Default value: 0Fh (600 ms) |
|-----------------------|---|

13.2 A_WRIST_TILT_THS (54h)

Absolute Wrist Tilt threshold register (r/w).

Table 306. A_WRIST_TILT_THS register

| | | | | | | | |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| WRIST_TILT_THS7 | WRIST_TILT_THS6 | WRIST_TILT_THS5 | WRIST_TILT_THS4 | WRIST_TILT_THS3 | WRIST_TILT_THS2 | WRIST_TILT_THS1 | WRIST_TILT_THS0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

Table 307. A_WRIST_TILT_THS register description

| | |
|---------------------|---|
| WRIST_TILT_THS[7:0] | Absolute wrist tilt threshold parameters. 1 LSB = 15.625 mg. Default value: 20h (500 mg) |
|---------------------|---|

13.3 A_WRIST_TILT_Mask (59h)

Absolute Wrist Tilt mask register (r/w).

Table 308. A_WRIST_TILT_Mask register

| | | | | | | | |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|---|---|
| WRIST_TILT_MASK_Xpos | WRIST_TILT_MASK_Xneg | WRIST_TILT_MASK_Ypos | WRIST_TILT_MASK_Yneg | WRIST_TILT_MASK_Zpos | WRIST_TILT_MASK_Zneg | 0 | 0 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|---|---|

Table 309. A_WRIST_TILT_Mask register description

| | |
|----------------------|---|
| WRIST_TILT_MASK_Xpos | Absolute wrist tilt positive X-axis enable. Default value: 1 (0: disable; 1: enable) |
| WRIST_TILT_MASK_Xneg | Absolute wrist tilt negative X-axis enable. Default value: 1 (0: disable; 1: enable) |
| WRIST_TILT_MASK_Ypos | Absolute wrist tilt positive Y-axis enable. Default value: 0 (0: disable; 1: enable) |
| WRIST_TILT_MASK_Yneg | Absolute wrist tilt negative Y-axis enable. Default value: 0 (0: disable; 1: enable) |
| WRIST_TILT_MASK_Zpos | Absolute wrist tilt positive Z-axis enable. Default value: 0 (0: disable; 1: enable) |
| WRIST_TILT_MASK_Zneg | Absolute wrist tilt negative Z-axis enable. Default value: 0 (0: disable; 1: enable) |

14 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and "Green" standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

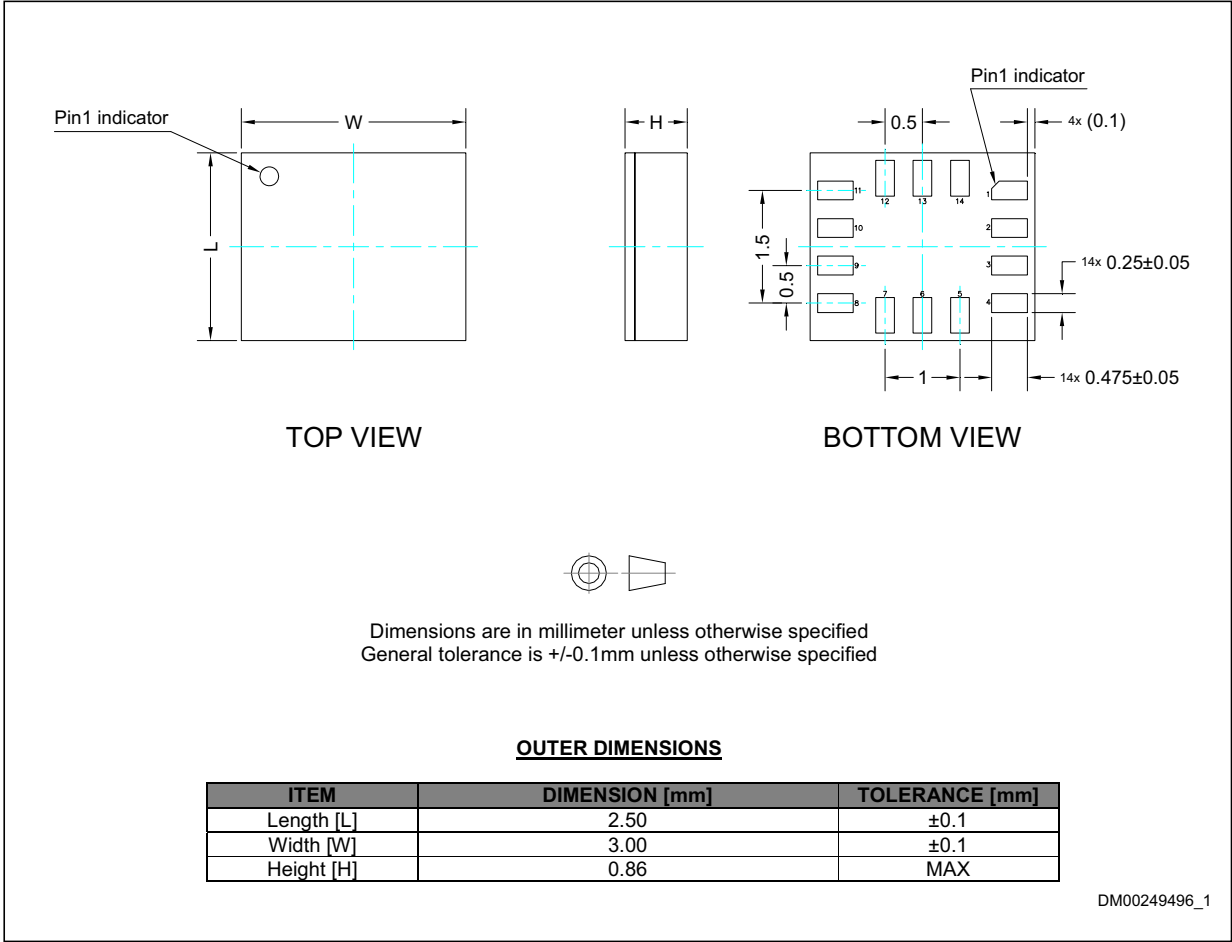
Land pattern and soldering recommendations are available at www.st.com/mems.

15 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

15.1 LGA-14L package information

Figure 23. LGA-14L 2.5x3x0.86 mm package outline and mechanical data



15.2 LGA-14 packing information

Figure 24. Carrier tape information for LGA-14 package

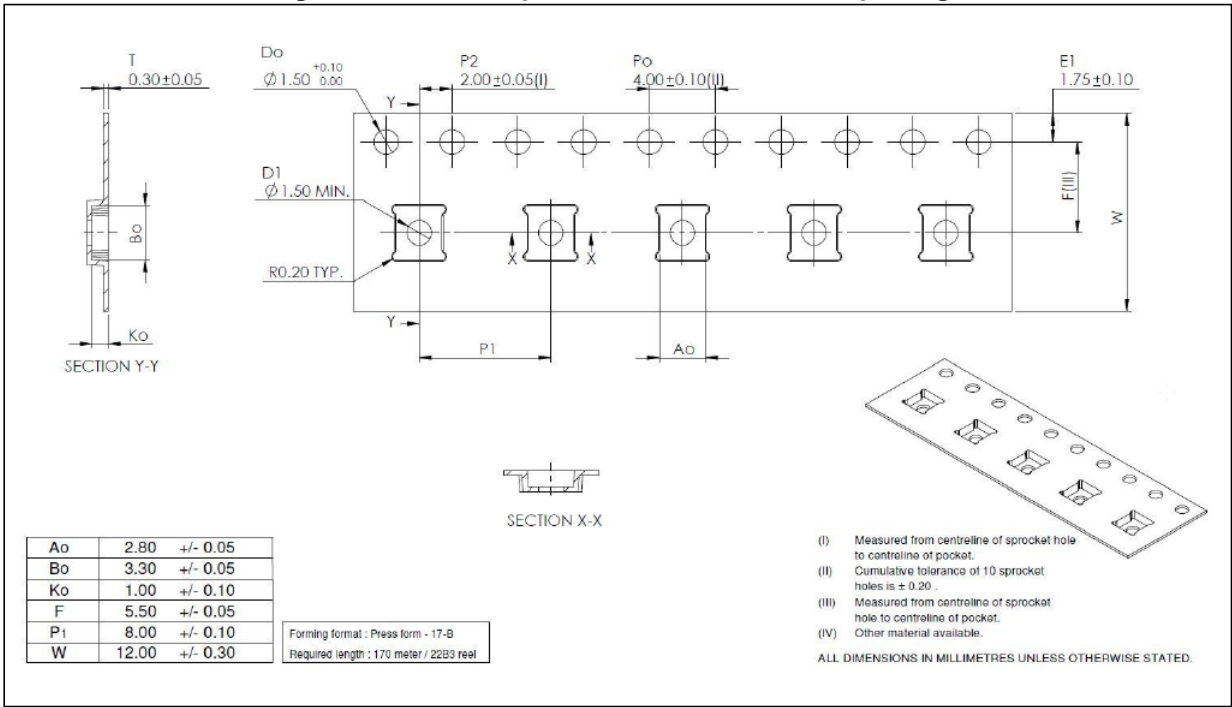


Figure 25. LGA-14 package orientation in carrier tape

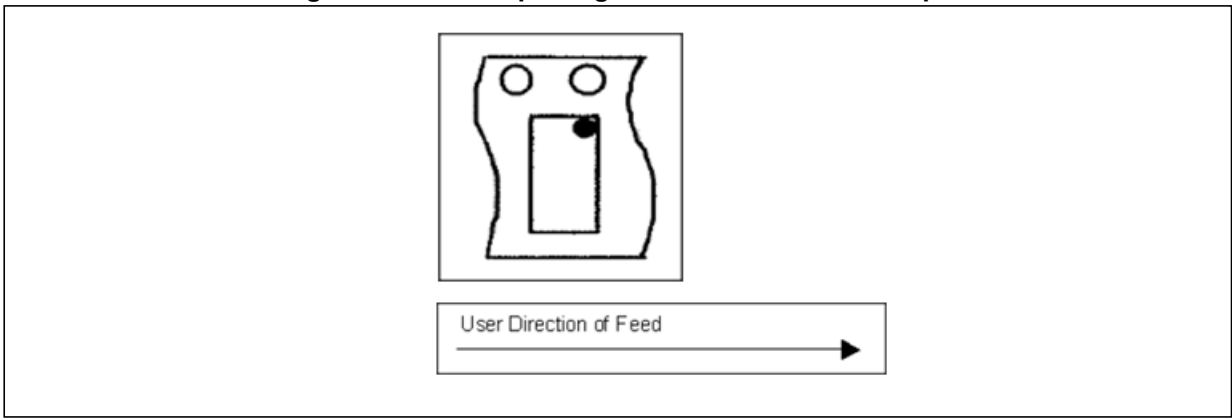


Figure 26. Reel information for carrier tape of LGA-14 package

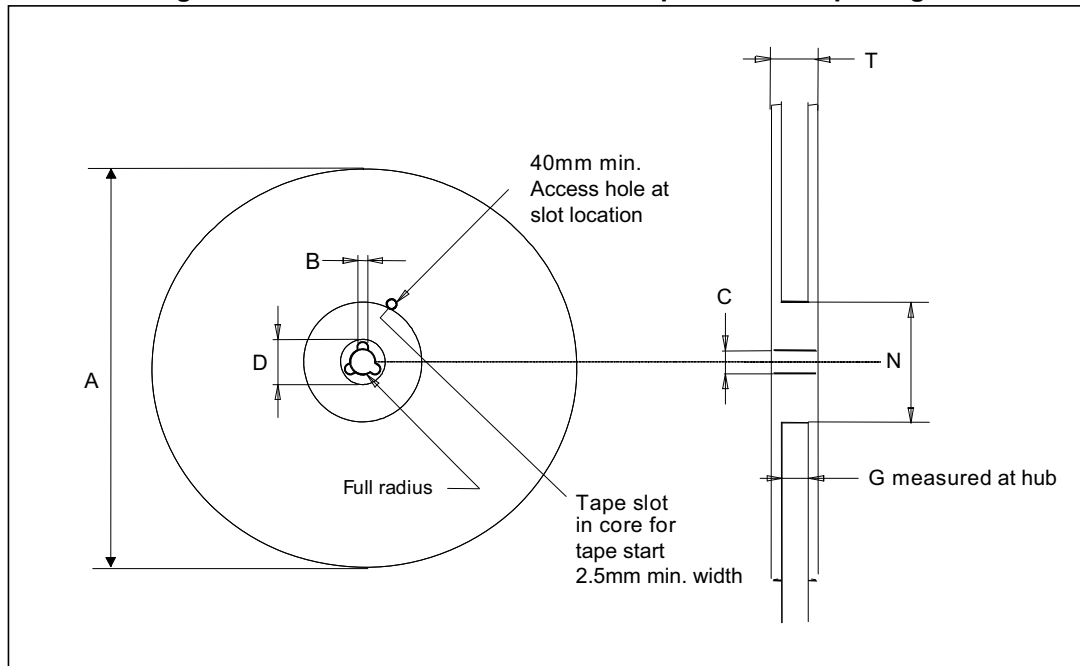


Table 310. Reel dimensions for carrier tape of LGA-14 package

| Reel dimensions (mm) | |
|----------------------|------------|
| A (max) | 330 |
| B (min) | 1.5 |
| C | 13 ±0.25 |
| D (min) | 20.2 |
| N (min) | 60 |
| G | 12.4 +2/-0 |
| T (max) | 18.4 |

16 Revision history

Table 311. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 03-May-2017 | 6 | <p>Updated Section 4.4.2: I²C - inter-IC control interface (added Table 8: I²C master timing values)</p> <p>Updated Figure 13 and Figure 15</p> <p>Updated footnotes 1 and 2 of Table 20: Registers address map</p> <p>Updated description of SW_RESET bit in Table 58: CTRL3_C register description</p> <p>Updated bit 0 in CTRL1_XL (10h)</p> <p>Updated description of INT_OIS (6Fh), CTRL1_OIS (70h), CTRL2_OIS (71h) and CTRL3_OIS (72h)</p> <p>Updated description of X_OFS_USR (73h), Y_OFS_USR (74h), Z_OFS_USR (75h)</p> <p>Minor textual updates</p> |
| 29-Sep-2017 | 7 | <p>Updated Table 3: Mechanical characteristics</p> <p>Specified SPI mode 3 in Section 4.4.1: SPI - serial peripheral interface and throughout Section 6: Digital interfaces</p> |

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved