LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT6911UXC

HDMI2.0 to Dual-Port MIPI DSI/CSI with Audio

Datasheet

1. Features

- **HDMI2.0 Receiver**
  - Compliant with HDMI2.0b, HDMI1.4 and DVI1.0
  - Compliant with HDCP2.2 and HDCP1.4
  - Data rate up to 6Gbps
  - Adaptive receiver equalization
  - AC-couple capable
  - Support channel swap(arbitrarily) and polarity inversion(independent)
  - Support 4k@60Hz
  - Supported 3D formats: frame packing(progressive), side-by-side(half/full), top-and-bottom, line alternative
  - Supported video formats:
    CSC/DSC disabled: 24/30/36-bit RGB, 16/20/24-bit YCbCr4:2:2, 8-bit YCbCr4:2:0
    CSC disabled, DSC enabled: 24-bit RGB, 16/20/24-bit YCbCr4:2:2, 8-bit YCbCr4:2:0
    CSC enabled, DSC disabled: 24-bit RGB/YCbCr4:4:4, 16/20/24-bit YCbCr4:2:2
    CSC/DSC enabled: 24-bit RGB/YCbCr4:4:4, 16/20/24-bit YCbCr4:2:2
  - HDR support
  - Support TMDS descrambling for EMI/RFI reduction
  - Support SCDC
  - 5V tolerance DDC/HPD I/Os
  - Integrated EDID shadow
- **Single/Dual-Port MIPI DSI/CSI Transmitter**
  - Compliant with DCS1.1, D-PHY1.2 & DSI1.3 & CSI-2 1.3
  - Integrated DSC1.2 encoder
  - 1/2 configurable ports
  - 1 clock lane and 1/2/3/4 configurable data lanes per port
  - 80Mbps~2Gbps per data lane
  - Programmable transmitter swing and pre-emphasis
  - Support lane swap(arbitrarily) and polarity inversion(independent)
  - 3D support: two ports simultaneously transmitting L and R frames or odd-L/even-R alternative pixels
  - DSI support both burst mode and non-burst mode
  - DSI support video formats:
    CSC/DSC disabled: Packed 16/18/24/30/36-bit RGB, Loosely Packed 18-bit RGB, Packed 16/24-bit YCbCr4:2:2, Loosely Packed 20-bit YCbCr4:2:2, Packed 12-bit YCbCr4:2:0
    CSC disabled, DSC enabled: Packed 24-bit RGB, Packed 16-bit YCbCr4:2:2, Packed 12-bit YCbCr4:2:0
    CSC enabled, DSC disabled: Packed 16/18/24-bit RGB, Loosely Packed 18-bit RGB, Packed 16-bit YCbCr4:2:2
    CSC/DSC enabled: Packed 24-bit RGB, Packed 16-bit YCbCr4:2:2
  - CSI support video formats:
    CSC/DSC disabled: RGB565/666/888, YUV422 8/10-bit, Legacy YUV420 8-bit
    CSC disabled, DSC enabled: RGB888, YUV422 8-bit, Legacy YUV420 8-bit
    CSC enabled, DSC disabled: RGB565/666/888, YUV422 8-bit
    CSC/DSC enabled: RGB888, YUV422 8-bit
  - CSI support interlaced mode
  - Maximum 64 pixels overlap for each half
  - Video stream copy mode for each port
- **Digital Audio Output**
  - I2S interface supporting 2-channel audio, with sample rates of 32~192 kHz and sample sizes of 16~24 bits
  - SPDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
  - IEC60958 or IEC61937 compatible
- **Miscellaneous**
  - CSC: RGB <-> YUV444 <-> YUV422
  - External oscillator
  - Integrated microprocessor
  - Embedded SPI flash for firmware and HDCP keys
  - GPIOs for system controls
  - Integrated 100/400kHz I2C slave
  - Firmware update through I2C interface
  - Power supply: 3.3V for I/O and 1.2V for core
  - ESD 4kV HBM
  - Temperature Range: -40℃ ~ +85℃
  - Package: QFN64(7.5mm*7.5mm)
  - Pin compatible with LT6911C

2. General Description

The LT6911UXC is a high performance HDMI2.0 to MIPI DSI/CSI converter for VR, Smart phone, Display applications.

The HDMI2.0 input supports data rate up to 6Gbps which provides sufficient bandwidth for 4k@60Hz video. Also HDCP2.2 is supported for data decryption.

For MIPI DSI/CSI output, LT6911UXC features configurable single-port or dual-port MIPI DSI/CSI with 1 high-speed clock lane, and 1~4 high-speed data lanes operating at maximum 2Gbps/lane, which can support a total bandwidth of up to 16Gbps. LT6911UXC supports burst mode DSI video data transferring, also supports flexible video data mapping path. Integrated DSC encoder implements up to 3:1 visually lossless compression which reduces bandwidth requirement for UHD video transport, also power consumption and EMI.

Two digital audio output interfaces are available, I2S and SPDIF. The I2S interface supports 2-ch LPCM and the SPDIF interface supports 2-ch LPCM or compressed audio, both at maximum 192kHz sample rate.

The device is capable of automatic operation which is enabled by an integrated microprocessor that uses an embedded SPI flash for firmware storage. System control is also available through the configuration I2C slave interface.

3. Applications

- Mobile system
- Display
- VR

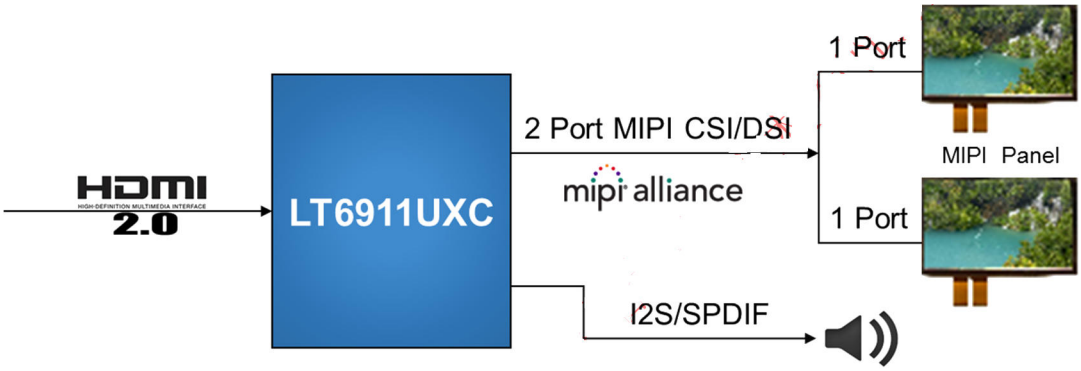


Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT6911UXC	-40℃ to +85℃	QFN64 (7.5*7.5)	Tray

Table of Contents

5. Revision History

Version	Owner	Content	Date
R0.5	HF X	Initial datasheet creation	03/05/2018
R0.6	HF X	Updated pin description	04/03/2018
R0.7	HF X	Updated SPDIF channel number(8->2)	07/18/2018
R0.8	HF X	Added pin description about UART	07/24/2018
	N Wang	Update package information	11/15/2018
R0.9	HF X	Removed MIPI TX feature: skew calibration	11/20/2018

6. Pinning Information

6.1 Pin Configuration

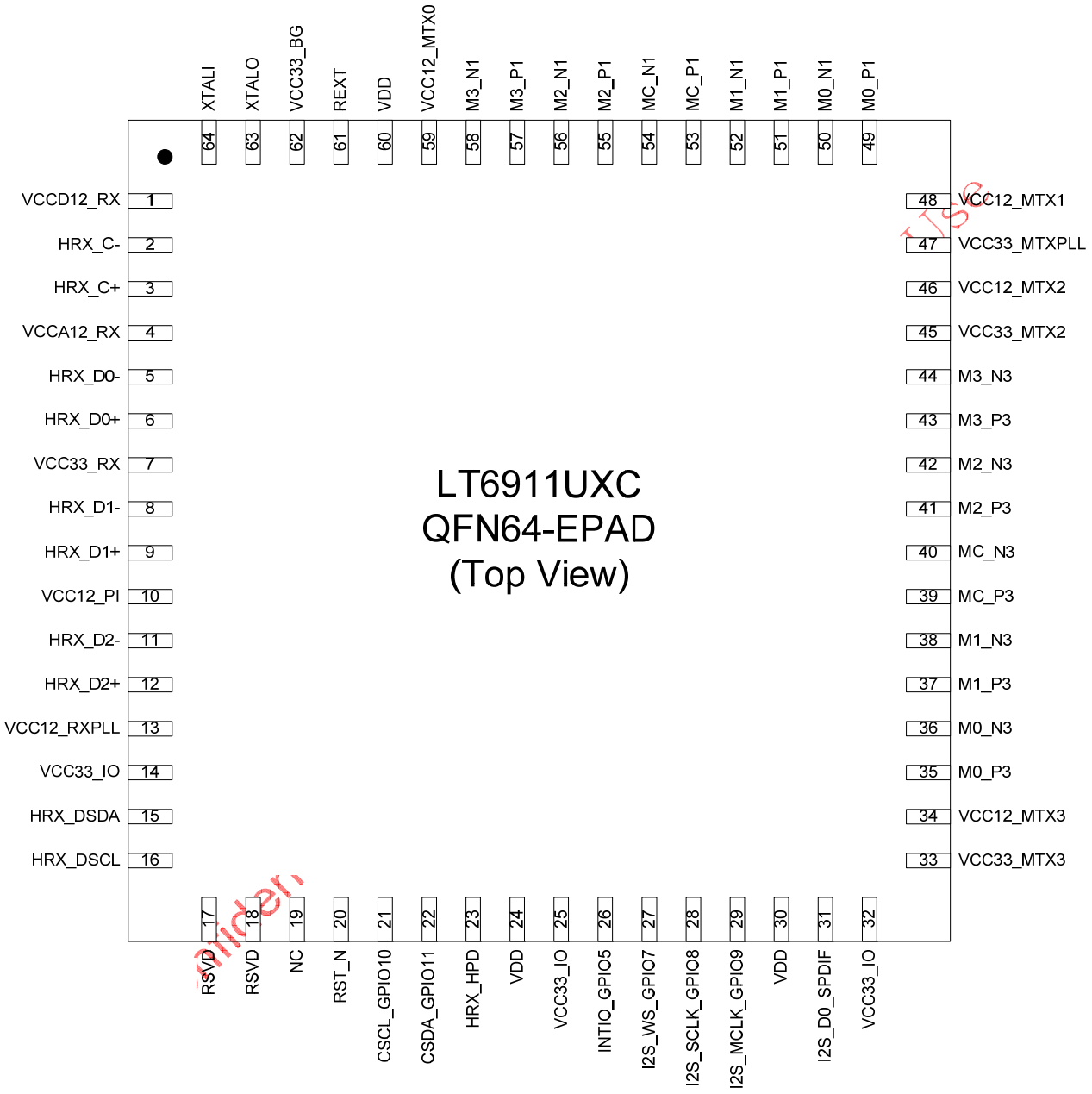


Figure 6.1.1 Pin Configuration

6.2 Pin Description

Table 6.2.1 Pin Description

Pin#	Pin Name	I/O Type	I/O Dir	Description
1	VCCD12_RX	PG	I	Power rail of 1.2V digital power for HDMI RX
4	VCCA12_RX	PG	I	Power rail of 1.2V analog power for HDMI RX
7	VCC33_RX	PG	I	Power rail of 3.3V HDMI RX power
10	VCC12_PI	PG	I	Power rail of 1.2V HDMI RX PI power
13	VCC12_RXPLL	PG	I	Power rail of 1.2V HDMI RX PLL power
14,25,32	VCC33_IO	PG	I	Power rail of 3.3V I/O power
24,30,60	VDD	PG	I	Power rail of 1.2V digital core power
33	VCC33_MTX3	PG	I	Power rail of 3.3V MIPI TX port 3 power
34	VCC12_MTX3	PG	I	Power rail of 1.2V MIPI TX port 3 power
45	VCC33_MTX2	PG	I	Power rail of 3.3V MIPI TX port 2 power
46	VCC12_MTX2	PG	I	Power rail of 1.2V MIPI TX port 2 power
47	VCC33_MTXPLL	PG	I	Power rail of 3.3V MIPI TX PLL power
48	VCC12_MTX1	PG	I	Power rail of 1.2V MIPI TX port 1 power
59	VCC12_MTX0	PG	I	Power rail of 1.2V MIPI TX port 0 power
62	VCC33_BG	PG	I	Power rail of 3.3V BG power
2	HRX_C-	Analog	I	HDMI RX clock channel negative input
3	HRX_C+	Analog	I	HDMI RX clock channel positive input
5	HRX_D0-	Analog	I	HDMI RX data channel 0 negative input
6	HRX_D0+	Analog	I	HDMI RX data channel 0 positive input
8	HRX_D1-	Analog	I	HDMI RX data channel 1 negative input
9	HRX_D1+	Analog	I	HDMI RX data channel 1 positive input
11	HRX_D2-	Analog	I	HDMI RX data channel 2 negative input
12	HRX_D2+	Analog	I	HDMI RX data channel 2 positive input
35	M0_P3	Analog	O	MIPI TX port 3 data lane 0 positive output
36	M0_N3	Analog	O	MIPI TX port 3 data lane 0 negative output
37	M1_P3	Analog	O	MIPI TX port 3 data lane 1 positive output
38	M1_N3	Analog	O	MIPI TX port 3 data lane 1 negative output
39	MC_P3	Analog	O	MIPI TX port 3 clock lane positive output
40	MC_N3	Analog	O	MIPI TX port 3 clock lane negative output
41	M2_P3	Analog	O	MIPI TX port 3 data lane 2 positive output
42	M2_N3	Analog	O	MIPI TX port 3 data lane 2 negative output
43	M3_P3	Analog	O	MIPI TX port 3 data lane 3 positive output
44	M3_N3	Analog	O	MIPI TX port 3 data lane 3 negative output
49	M0_P1	Analog	O	MIPI TX port 1 data lane 0 positive output
50	M0_N1	Analog	O	MIPI TX port 1 data lane 0 negative output
51	M1_P1	Analog	O	MIPI TX port 1 data lane 1 positive output
52	M1_N1	Analog	O	MIPI TX port 1 data lane 1 negative output
53	MC_P1	Analog	O	MIPI TX port 1 clock lane positive output
54	MC_N1	Analog	O	MIPI TX port 1 clock lane negative output
55	M2_P1	Analog	O	MIPI TX port 1 data lane 2 positive output
56	M2_N1	Analog	O	MIPI TX port 1 data lane 2 negative output

Pin#	Pin Name	I/O Type	I/O Dir	Description
57	M3_P1	Analog	O	MIPI TX port 1 data lane 3 positive output
58	M3_N1	Analog	O	MIPI TX port 1 data lane 3 negative output
15	HRX_DSDA	Schmitt, OD	I/O	HDMI RX DDC/SCDC channel SDA signal
16	HRX_DSCL	Schmitt	I	HDMI RX DDC/SCDC channel SCL signal
20	RST_N	Schmitt	I	Active low reset input
21	CSCL_GPIO10	LVTTL	I/O	Configuration I2C SCL signal, also shared as general purpose I/O 10. It can be used as UART RX for debug.
22	CSDA_GPIO11	LVTTL	I/O	Configuration I2C SDA signal, also shared as general purpose I/O 11
23	HRX_HPD	OD	O	HDMI RX HPD signal
26	INTIO_GPIO5	LVTTL	I/O	Interrupt I/O, also shared as general purpose I/O 5. It can be used as UART TX or RX for debug.
27	I2S_WS_GPIO7	LVTTL	I/O	Audio I2S word selection output, also shared as general purpose I/O 7. It can be used as UART TX for debug.
28	I2S_SCLK_GPIO8	LVTTL	I/O	Audio I2S serial clock output, also shared as general purpose I/O 8. It can be used as UART TX for debug.
29	I2S_MCLK_GPIO9	LVTTL	I/O	Audio I2S master clock output, also shared as general purpose I/O 9. It can be used as UART TX for debug.
31	I2S_D0_SPDIF	LVTTL	O	Audio I2S serial data 0 output, also shared as audio SPDIF output
63	XTALO	LVTTL	O	24MHz crystal oscillator output
64	XTALI	LVTTL	I	24MHz crystal oscillator input
61	REXT	Analog	O	Analog current reference. A resistor of 7.68kΩ (1%) should tie this pin to ground.
17,18	RSVD	LVTTL	O	Reserved pin
19	NC	N/A	N/A	No connection
65	EPAD	N/A	O	Exposed pad which should be connected to ground

7. Function Description

7.1 Function Block Diagram

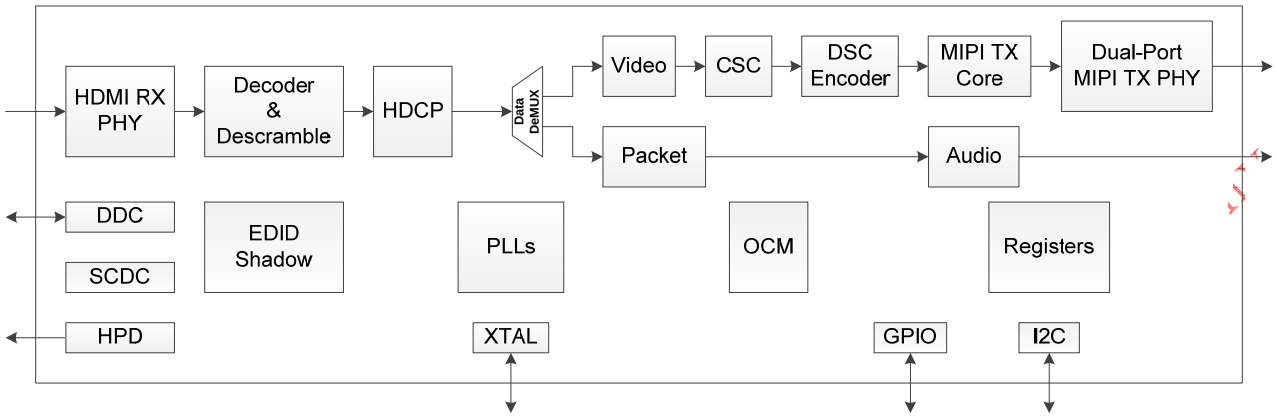


Figure 7.1.1 Function Block Diagram

8. Specification

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_RX, VCC33_IO, VCC33_MTX3, VCC33_MTX2, VCC33_MTXPLL, VCC33_BG	3.3V Power Supply Voltage	-0.3		3.9	V
VCCD12_RX, VCCA12_RX, VCC12_PI, VCC12_RXPLL, VDD, VCC12_MTX3, VCC12_MTX2, VCC12_MTX1, VCC12_MTX0	1.2V Power Supply Voltage	-0.3		1.5	V
V_I	CMOS Terminal Input Voltage Range	-0.3		3.9	V
V_O	CMOS Terminal Output Voltage Range	-0.3		3.9	V
T_S	Storage Temperature	-60		140	℃
ESD	HBM Electrostatic Discharge Level		4000		V

Notes:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_RX, VCC33_IO, VCC33_MTX3, VCC33_MTX2, VCC33_MTXPLL, VCC33_BG	3.3V Power Supply Voltage	2.97	3.3	3.63	V
VCCD12_RX, VCCA12_RX, VCC12_PI, VCC12_RXPLL, VDD, VCC12_MTX3, VCC12_MTX2, VCC12_MTX1, VCC12_MTX0	1.2V Power Supply Voltage	1.08	1.2	1.32	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

TMDS RX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{IDIFF}	Differential input voltage level	150		1200	mV
V_{ICM}	Input common mode voltage	VCC33_RX-700		VCC33_RX-37.5	mV
R_{TERM}	Single-ended termination resistance	45	50	55	Ω
MIPI HS Line TX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{CM}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS transmit output high voltage			360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
MIPI LP Line TX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{OL}	Output low-level SE voltage	-50	0	50	mV
V_{OH}	Output high-level SE voltage	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance	110			Ω

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

TMDS RX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_S	Minimum differential sensitivity(peak to peak) after the reference cable equalizer	150			mV
T_{INTRA_SKEW}	Intra-pair skew at sink connector			$0.15T_{bit}+112$	ps
T_{INTER_SKEW}	Inter-pair skew at sink connector			$0.2T_{character}+1.78$	ns
T_{JITTER}	TMDS clock jitter			$0.3T_{bit}$	ps
MIPI HS Line TX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
$\Delta V_{CMTX(HF)}$	Common mode Voltage variation above 450MHz			15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common mode Voltage variation between 50-450MHz			25	mV_{PEAK}
t_R and t_F (rise/fall time, 20%-80%)	Data rate <1Gbps	150		0.3UI	ps
	Data rate 1Gbps~1.5Gbps	100		0.35UI	ps
	Data rate >1.5Gbps	50		0.4UI	ps
MIPI LP Line TX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**

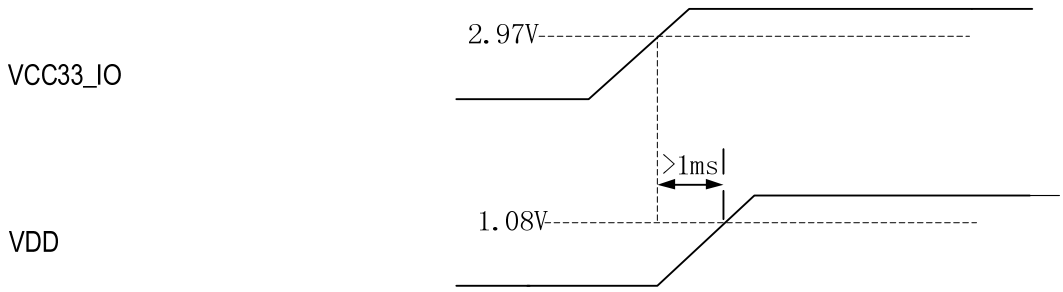
T_{RLP}/T_{FLP}	Single ended output rise/fall time,15% to 85%, C_L< 70pF			25	ns
T_{REOT}	Single ended output rise/fall time,30% to 85%, C_L< 70pF			35	ns
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	20			ns
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90			ns
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0			500	mV/ns
	Slew rate @ C_{LOAD} = 5pF			350	mV/ns
	Slew rate @ C_{LOAD} = 20pF			250	mV/ns
	Slew rate @ C_{LOAD} = 70pF			150	mV/ns
	Slew rate @ C_{LOAD} = 0 to 70pF(falling edge only)	30			mV/ns
	Slew rate @ C_{LOAD} = 0 to 70pF(rising edge only)	30			mV/ns
	Slew rate @ C_{LOAD} = 0 to 70pF(rising edge only)	30–0.075*($V_{O,INST}$-700)			mV/ns

8.5 Power Consumption

Table 8.5.1 Power Consumption

Condition	Supply Current(3.3V)	Supply Current(1.2V)	Unit
4k60Hz, 2-port TX, DSC enabled	TBD	TBD	mA
4k30Hz, 2-port TX, DSC disabled	TBD	TBD	mA
1080p, 1-port TX, DSC disabled	TBD	TBD	mA

8.6 Power-up and Reset Sequence



Note: 1.2V power should be set up at least 1ms later than 3.3V power, the reset signal should be released after 1.2V power is ready.

Figure 8.6.1 Power-up and Reset Sequence

9. Package Information

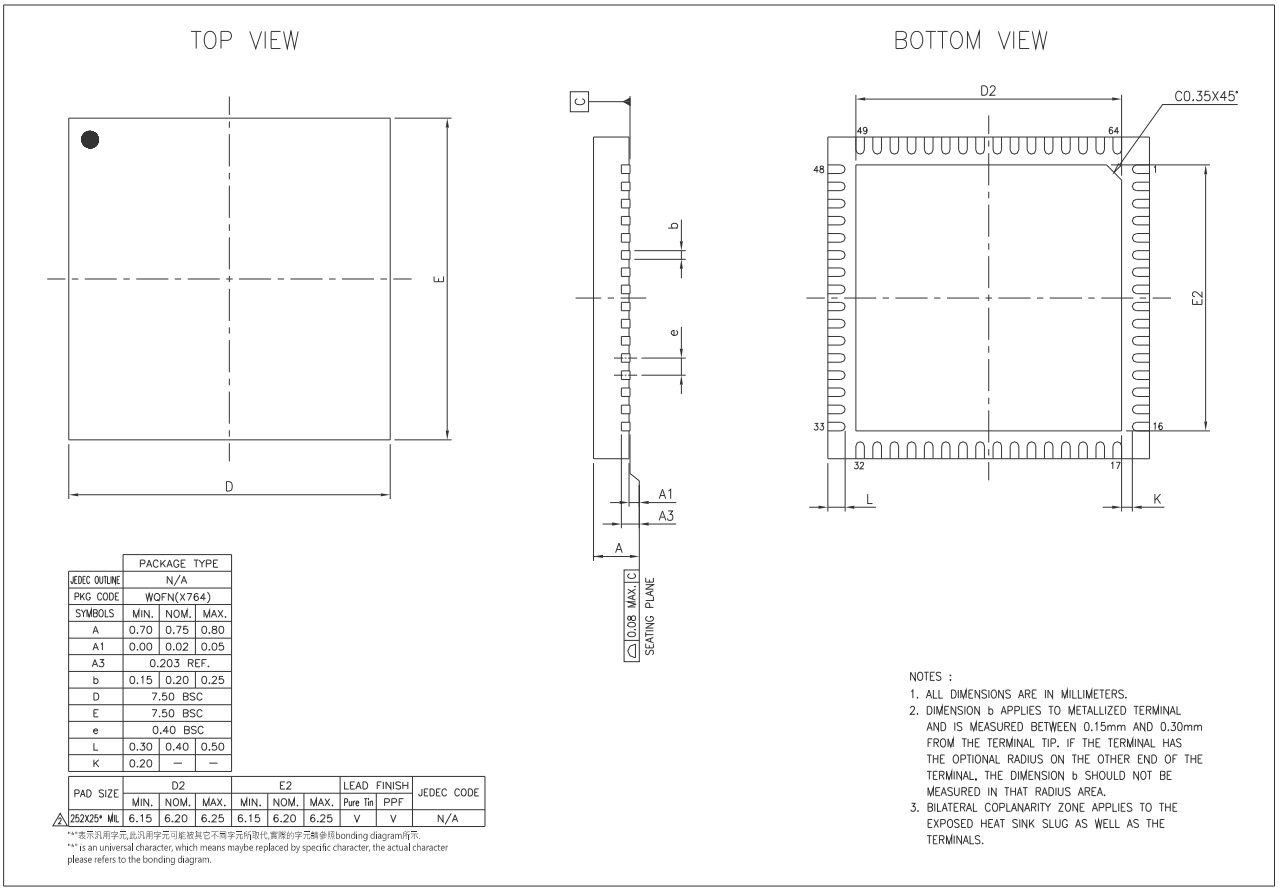
9.1 ePad Enhancement

The LT6911UXC is packaged in a 64-lead QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground. A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

9.2 Package Dimensions



	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	–	–

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
⚠252X25* MIL	6.15	6.20	6.25	6.15	6.20	6.25	V	V	N/A

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 9.2.1 Package Dimensions

Visit our corporate web page at: www.lontiumsemi.com
Technical support: support@lontium.com
Sales: sales@lontium.com