

# EE 599 Spring 2020 Homework 2

Name: Pengmiao Zhang

ID: 7865959675

Github Repo: [https://github.com/pengmiao-usc/EE-599\\_PengmiaoZhang\\_7865959675](https://github.com/pengmiao-usc/EE-599_PengmiaoZhang_7865959675)

## 1. Barrel Shifter

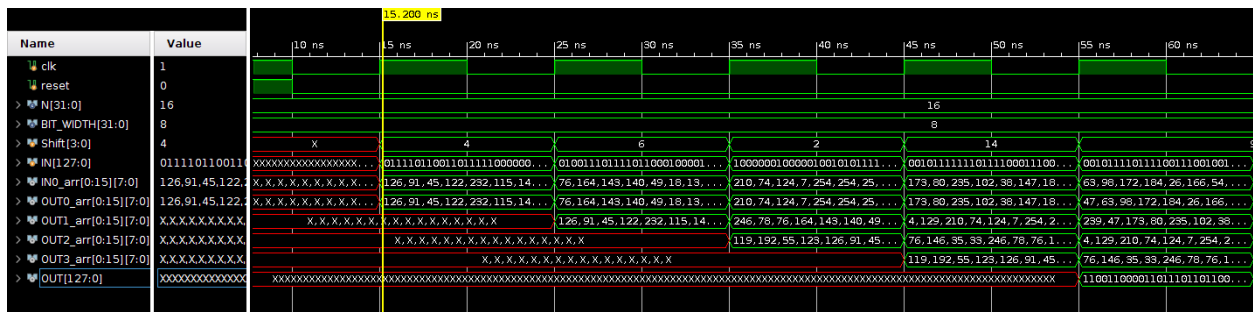
### 1.1. 16 elements

#### 1.1.1. Waveforms

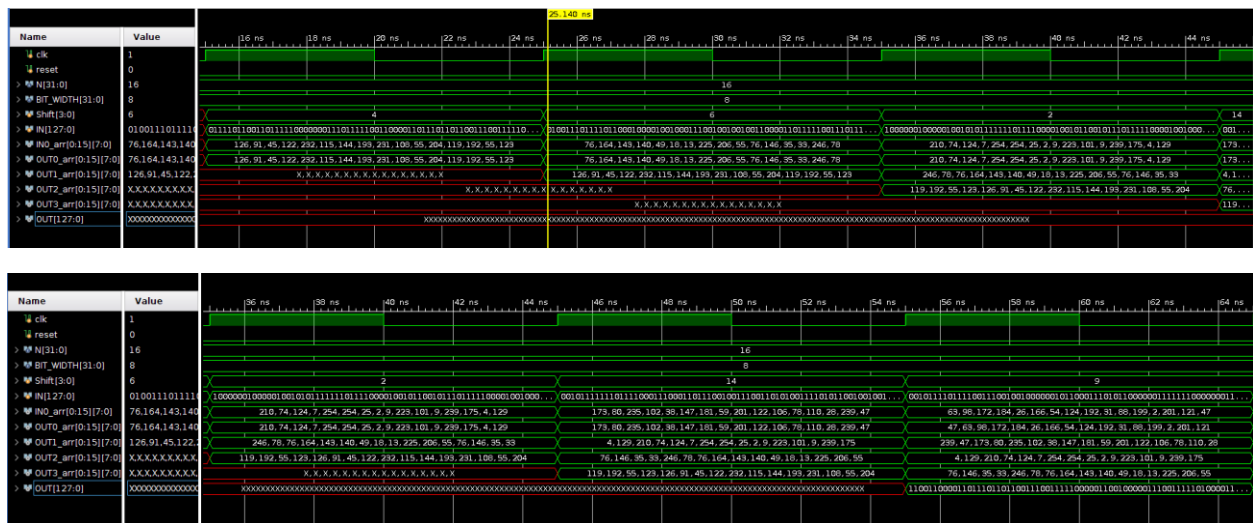
The array value and shift value are given randomly.

IN is the input bus, IN0\_arr is an array decoded from the bus. OUTn\_arr is the shift output of every layer, also the input of the register at the end of this layer. The final output is the output of the final register, which is a bus with 127 bits instead of an array.

#### (1) pipeline

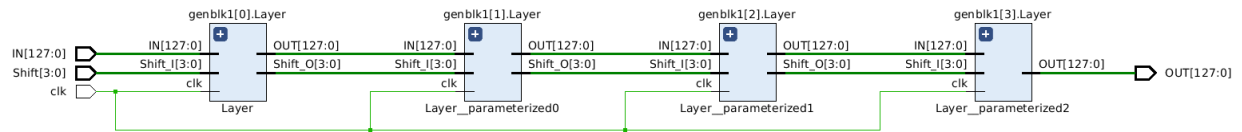


#### (2) detail values

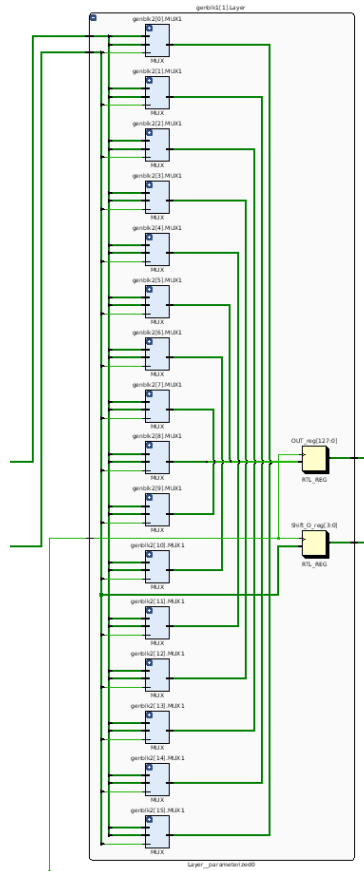


## 1.1.2.Schematics

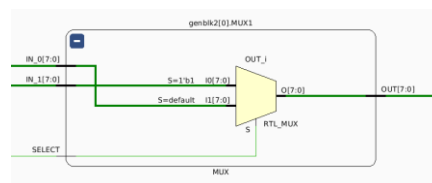
### 1.1.2.1. Big Picture



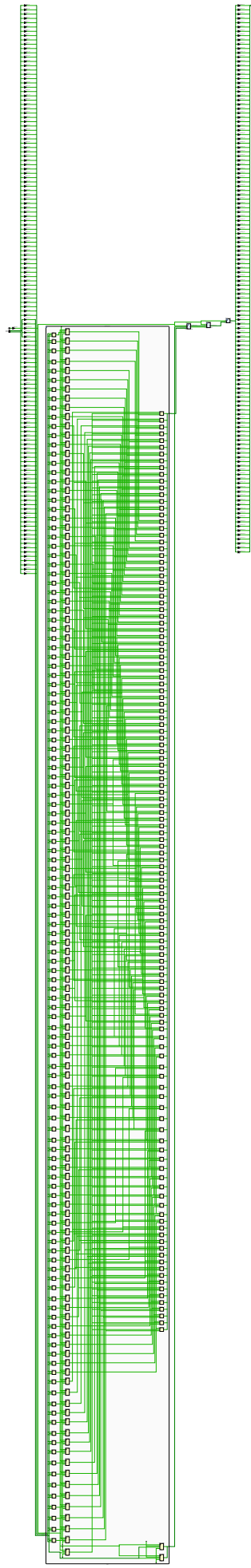
### 1.1.2.2. A Layer



### 1.1.2.3. A MUX



## 1.1.3. Synthesis



### 1.1.4.Resource Report

Utilization				
Hierarchy				
Hierarchy	Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)
Summary				BUFCTRL (32)
✓ Slice Logic	Barrel_Shifter	256	518	261
✓ Slice LUTs (2%)	genblk1 [0].Layer (Layer)	128	131	0
LUT as Logic (2%)	genblk1 [1].Layer (Layer__parameterized0)	64	130	0
✓ Slice Registers (2%)	genblk1 [2].Layer (Layer__parameterized1)	64	129	0
Register as Flip Flop (2%)	genblk1 [3].Layer (Layer__parameterized2)	0	128	0
Memory				
DSP				
✓ IO and GT Specific				
Bonded IOB (>100%)				
✓ Clocking				
BUFCTRL (3%)				

Slice LUTs: 2% used.

Name	Used
Barrel_Shifter	256
genblk1 [0].Layer (Layer)	128
genblk1 [1].Layer (Layer__parameterized0)	64
genblk1 [2].Layer (Layer__parameterized1)	64

Slice Registers: 2% used.

Name	Used
Barrel_Shifter	518
genblk1 [0].Layer (Layer)	131
genblk1 [1].Layer (Layer__parameterized0)	130
genblk1 [2].Layer (Layer__parameterized1)	129
genblk1 [3].Layer (Layer__parameterized2)	128

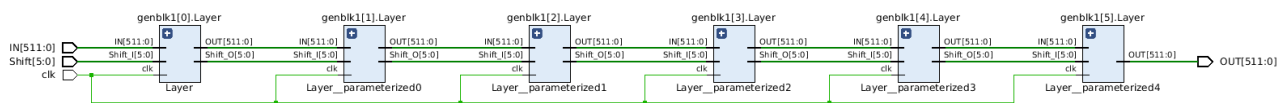
### 1.1.5.Timing Report

Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 3.609 ns	Worst Hold Slack (WHS): 0.127 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints:	0
Total Number of Endpoints: 387	Total Number of Endpoints: 387	Total Number of Endpoints:	519
All user specified timing constraints are met.			

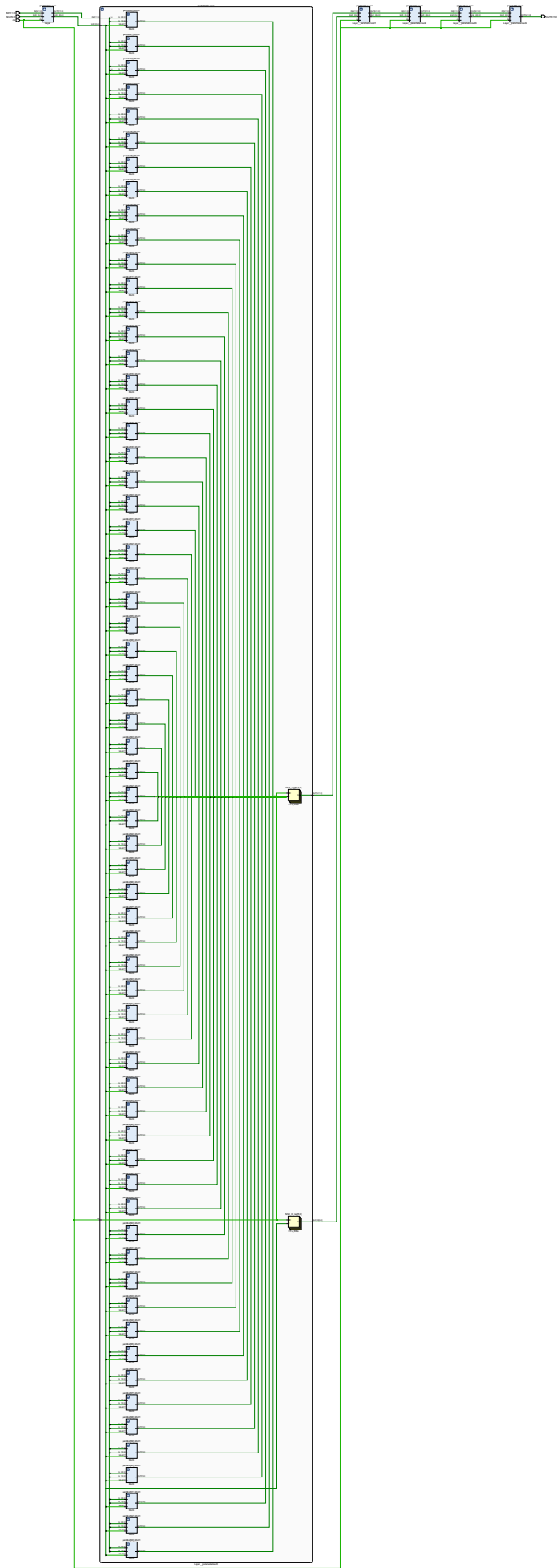
## 1.2. 64 elements

### 1.2.1.Schematics

#### 1.2.1.1. Big Picture



#### 1.2.1.2. A layer

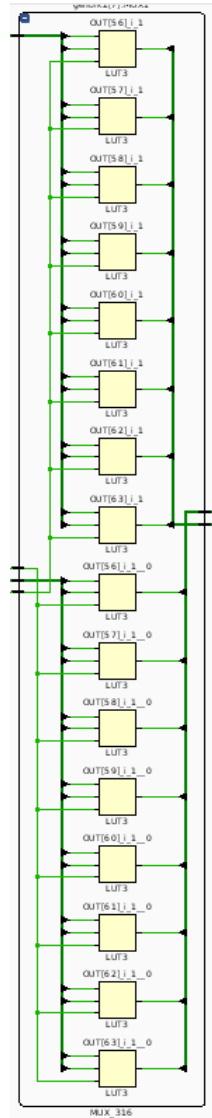


### 1.2.2.Synthesis

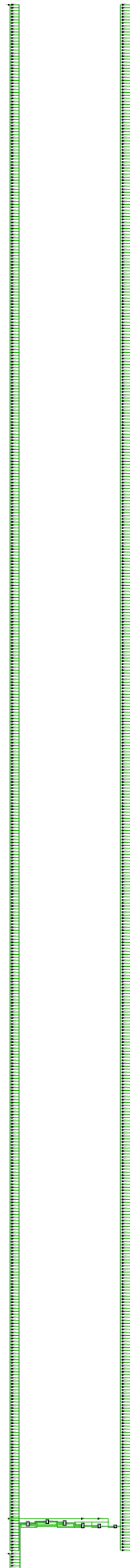
(1.) Big Picture and Layer

See next page please.

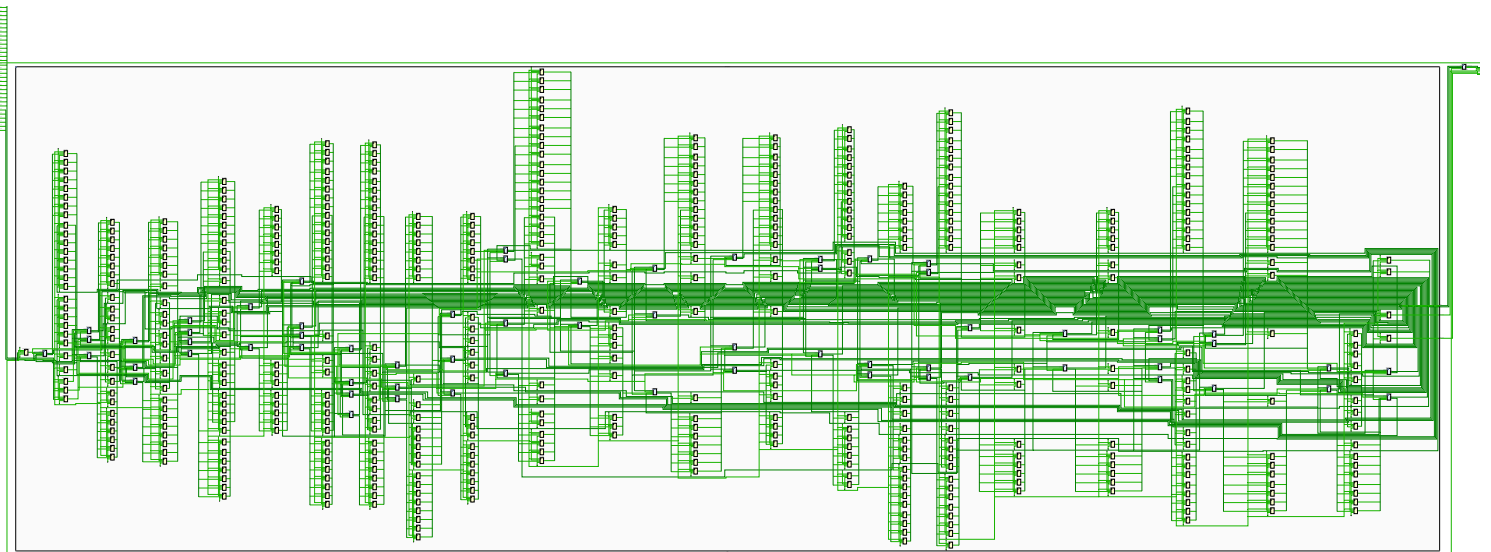
(2.) MUX



Big Picture:



A layer:





### 1.2.3.Resource Report

Hierarchy	Name	^ 1	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
Summary						
✓ Slice Logic	✓ Barrel_Shifter		1538	3091	1031	1
✓ Slice LUTs (11%)	> genblk1[0].Layer (Layer)		512	520	0	0
✓ LUT as Memory (<1%)	> genblk1[1].Layer (Layer__parameterized0)		256	517	0	0
LUT as Shift Register	> genblk1[2].Layer (Layer__parameterized1)		257	516	0	0
LUT as Logic (11%)	> genblk1[3].Layer (Layer__parameterized2)		257	513	0	0
✓ Slice Registers (11%)	> genblk1[4].Layer (Layer__parameterized3)		256	513	0	0
Register as Flip Flop (11%)	genblk1[5].Layer (Layer__parameterized4)		0	512	0	0
Memory						
DSP						
✓ IO and GT Specific						
Bonded IOB (>100%)						
✓ Clocking						
BUFGCTRL (3%)						

### 1.2.4.Timing Report

#### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.565 ns	Worst Hold Slack (WHS): 0.059 ns	Worst Pulse Width Slack (WPWS): 1.646 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 2573	Total Number of Endpoints: 2573	Total Number of Endpoints: 3094

All user specified timing constraints are met.

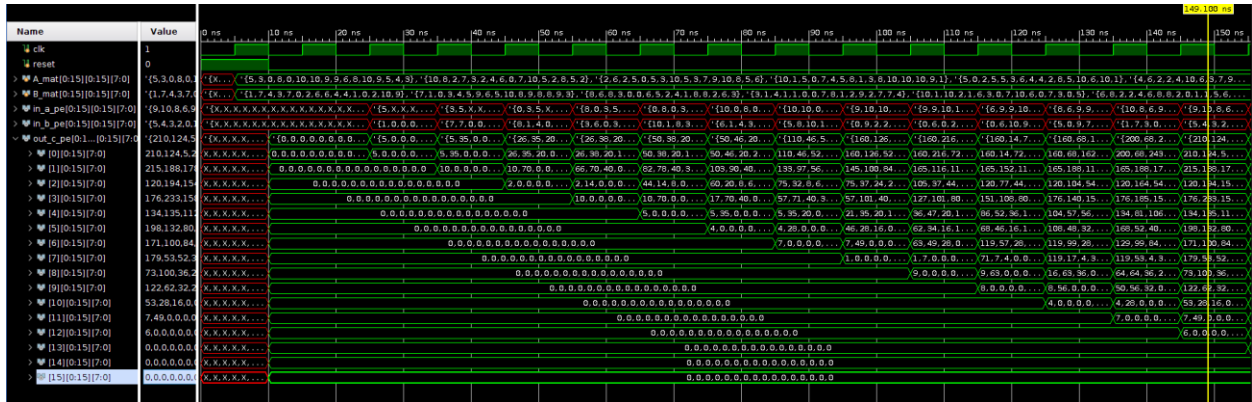
## 2. Systolic Array for Dense Matrix-Matrix Multiplication

### 2.1. 16 X 16 Matrices

#### 2.1.1. Waveforms

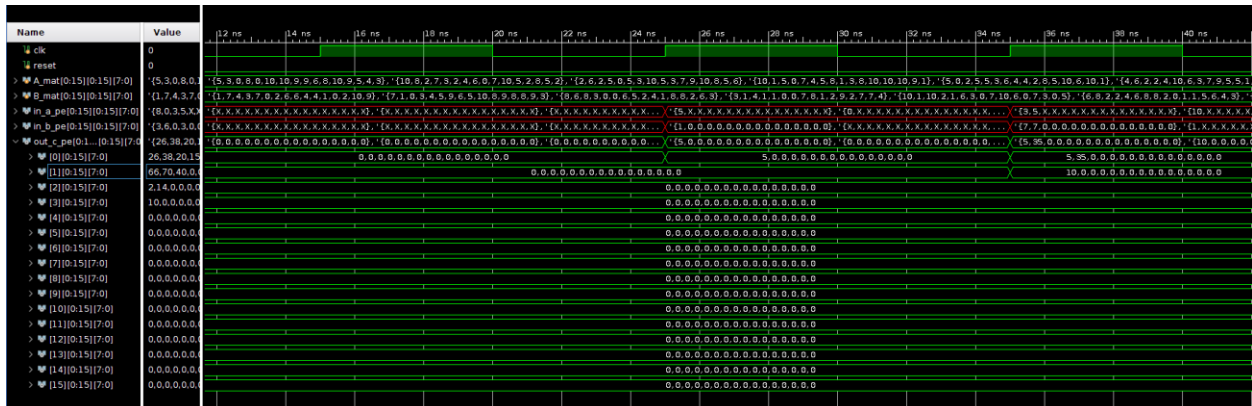
A\_mat is the input matrix, B\_mat is the output matrix. In\_a\_pe is the input value from A\_mat for each PE, in\_b\_pe is the input value from B\_mat for each PE. Out\_c\_pe is the output value of the result of matrix multiplication at each PE, each represent a result element.

##### 2.1.1.1. Pipeline



##### 2.1.1.2. Details

#### (1) The start of computation

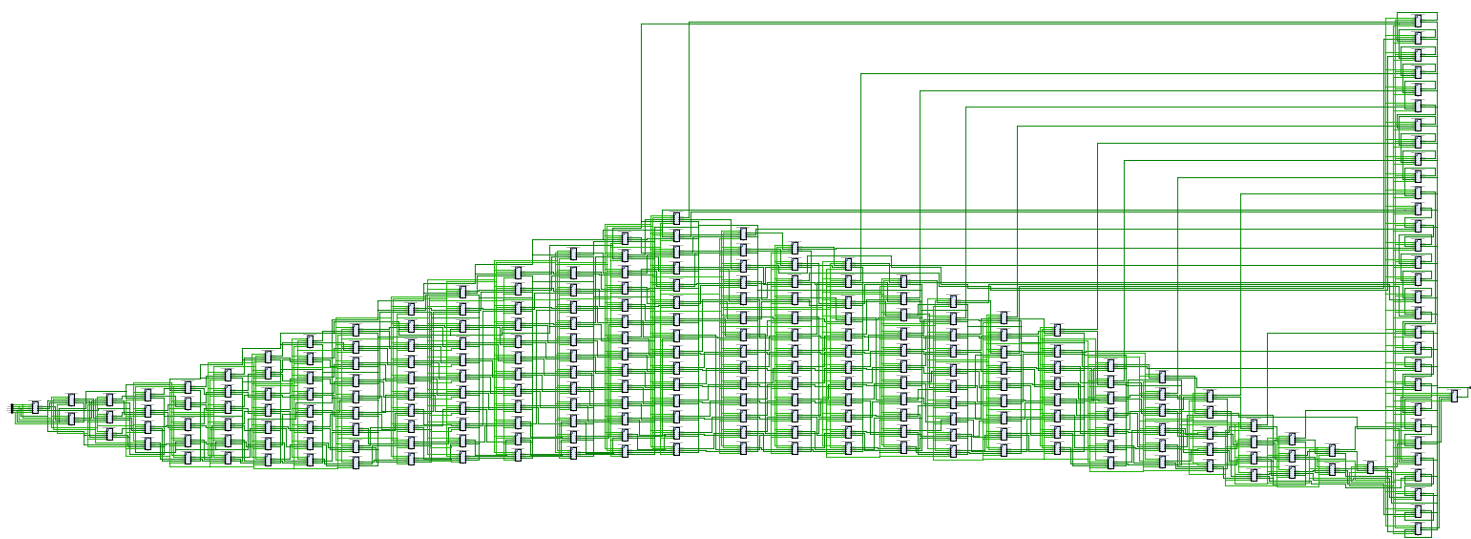


#### (2) During computation

(3) The last element calculation complete:

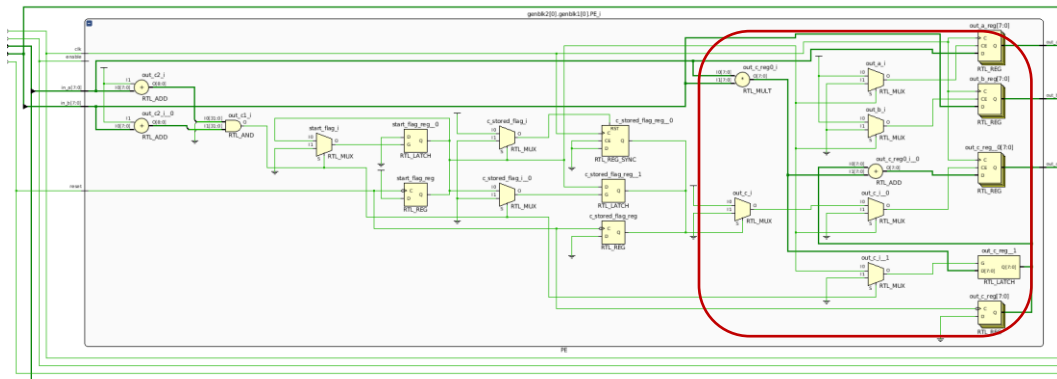
### 2.1.2.Schematics

### 2.1.2.1. Big Picture

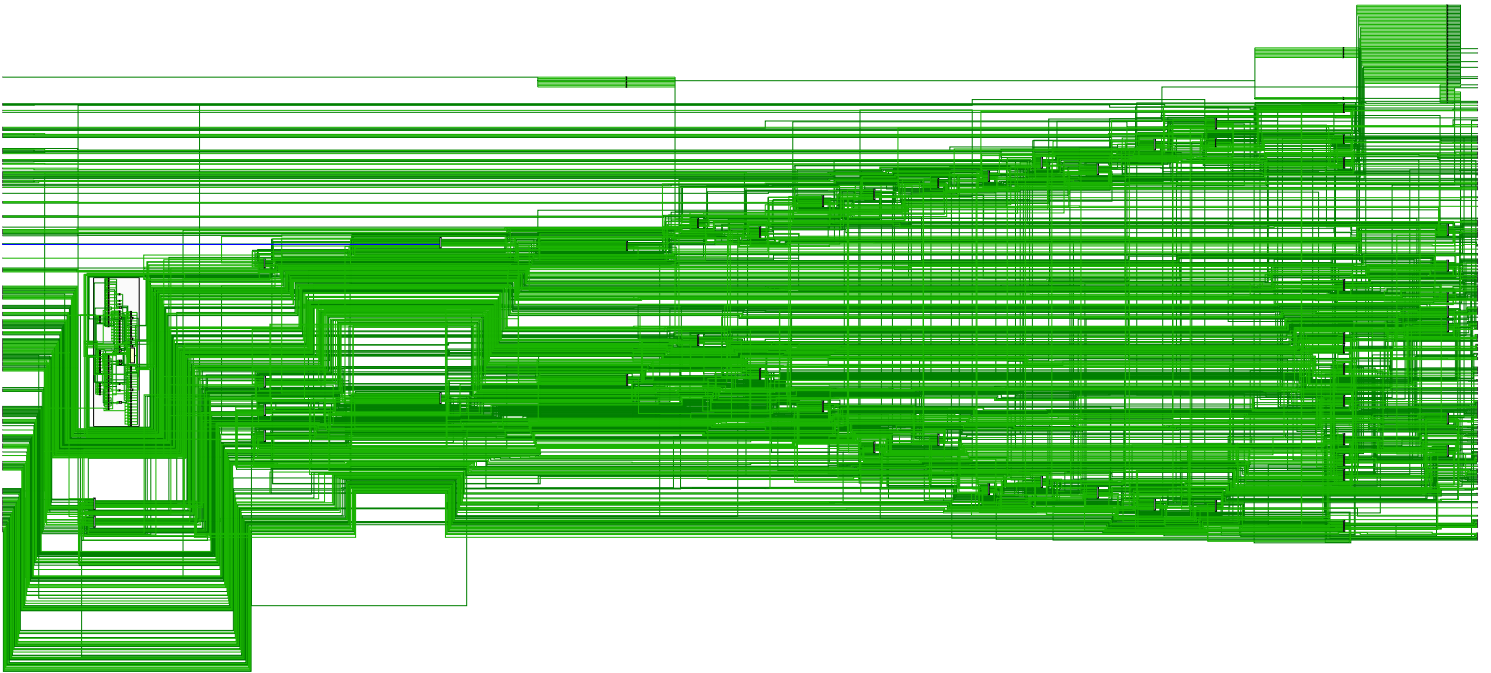


### 2.1.2.2. PE

Several flags are designed to start the computation for each PE, which is useful for avoiding random values accumulation before valid values come. The core part of a PE is shown in the red block.



### 2.1.3.Synthesis



## 2.1.4. Resource Report

Tcl Console	Messages	Log	Reports	Design Runs	Timing	Utilization					
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Slice LUT: 64% used

Name	Used
▼  Systolic_Array	9216
 genblk2[0].genblk1[0].PE_i (PE)	75
 genblk2[1].genblk1[0].PE_i (PE_111)	62
 genblk2[2].genblk1[0].PE_i (PE_127)	62
 genblk2[3].genblk1[0].PE_i (PE_143)	62
 genblk2[4].genblk1[0].PE_i (PE_159)	62
 genblk2[5].genblk1[0].PE_i (PE_175)	62
 genblk2[6].genblk1[0].PE_i (PE_191)	62
 genblk2[7].genblk1[0].PE_i (PE_207)	62
 genblk2[8].genblk1[0].PE_i (PE_223)	62
 genblk2[9].genblk1[0].PE_i (PE_239)	62
 genblk2[10].genblk1[0].PE_i (PE_15)	62
 genblk2[11].genblk1[0].PE_i (PE_31)	62
 genblk2[12].genblk1[0].PE_i (PE_47)	62
 genblk2[13].genblk1[0].PE_i (PE_63)	62
 genblk2[14].genblk1[0].PE_i (PE_79)	62
 genblk2[0].genblk1[1].PE_i (PE_6)	44
 genblk2[0].genblk1[2].PE_i (PE_7)	44
 genblk2[0].genblk1[3].PE_i (PE_8)	44
 genblk2[0].genblk1[4].PE_i (PE_9)	44
 genblk2[0].genblk1[5].PE_i (PE_10)	44

Slice Registers: 1% used

Name	Used
▼ N Systolic_Array	8448
genblk2[0].genblk1[0].PE_i (PE)	34
genblk2[0].genblk1[1].PE_i (PE_6)	34
genblk2[0].genblk1[2].PE_i (PE_7)	34
genblk2[0].genblk1[3].PE_i (PE_8)	34
genblk2[0].genblk1[4].PE_i (PE_9)	34
genblk2[0].genblk1[5].PE_i (PE_10)	34
genblk2[0].genblk1[6].PE_i (PE_11)	34
genblk2[0].genblk1[7].PE_i (PE_12)	34
genblk2[0].genblk1[8].PE_i (PE_13)	34
genblk2[0].genblk1[9].PE_i (PE_14)	34
genblk2[0].genblk1[10].PE_i (PE_0)	34
genblk2[0].genblk1[11].PE_i (PE_1)	34
genblk2[0].genblk1[12].PE_i (PE_2)	34

## 2.1.5.Timing Report

### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.284 ns	Worst Hold Slack (WHS): 0.145 ns	Worst Pulse Width Slack (WPWS): 1.728 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 6912	Total Number of Endpoints: 6912	Total Number of Endpoints: 4097

All user specified timing constraints are met.

## 2.1.6.Power Report

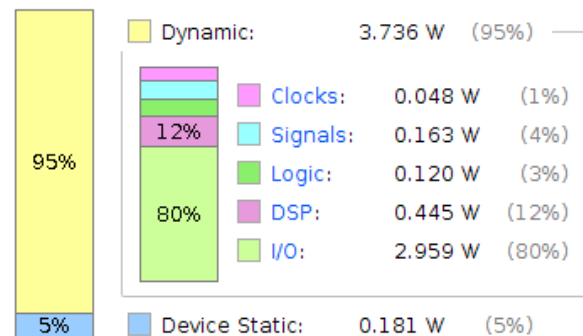
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

<b>Total On-Chip Power:</b>	<b>3.917 W</b>
<b>Design Power Budget:</b>	<b>Not Specified</b>
<b>Power Budget Margin:</b>	<b>N/A</b>
<b>Junction Temperature:</b>	<b>70.2°C</b>
Thermal Margin:	29.8°C (2.5 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

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### On-Chip Power





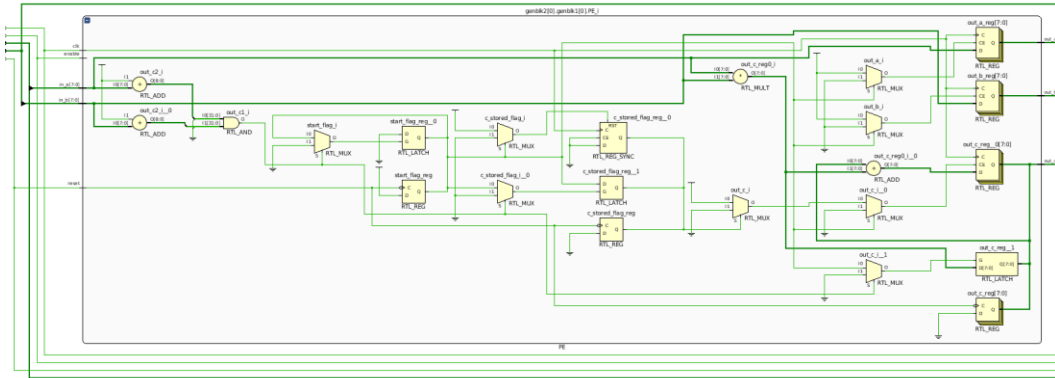
## 2.2. 32 X 32 Matrices

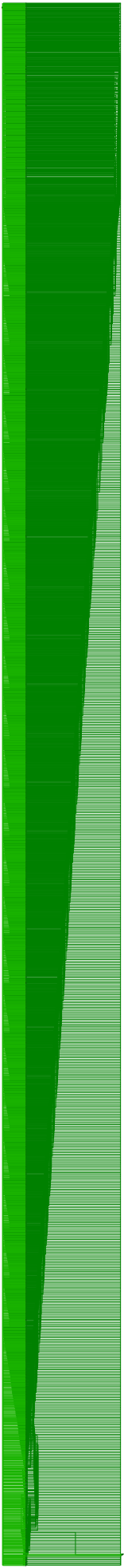
### 2.2.1.Schematics

#### 2.2.1.1. Big Picture

See next page please.

#### 2.2.1.2. PE





## 2.2.2.Synthesis

See next page please.

## 2.2.3.Resource Report

Utilization						
Hierarchy						
Hierarchy	Name	Slice LUTs ...	Slice Register...	DSPs (66)	Bonded IOB (54)	BUFGCTRL (32)
Summary						
▼ Slice Logic	▼ Systolic_Array	36864	34304	1024	8706	2
▼ Slice LUTs (>100%)	genblk2[0].genblk1[0].PE_i (PE)	74	34	1	0	0
LUT as Logic (>100%)	genblk2[0].genblk1[1].PE_i (PE_10)	44	34	1	0	0
▼ Slice Registers (>100%)	genblk2[0].genblk1[2].PE_i (PE_21)	44	34	1	0	0
Register as Latch (32%)	genblk2[0].genblk1[3].PE_i (PE_24)	44	34	1	0	0
Register as Flip Flop (87%)	genblk2[0].genblk1[4].PE_i (PE_25)	44	34	1	0	0
Memory	genblk2[0].genblk1[5].PE_i (PE_26)	44	34	1	0	0
▼ DSP	genblk2[0].genblk1[6].PE_i (PE_27)	44	34	1	0	0
▼ DSPs (>100%)	genblk2[0].genblk1[7].PE_i (PE_28)	44	34	1	0	0
DSP48E1 only	genblk2[0].genblk1[8].PE_i (PE_29)	44	34	1	0	0
▼ IO and GT Specific	genblk2[0].genblk1[9].PE_i (PE_30)	44	34	1	0	0
Bonded IOB (>100%)	genblk2[0].genblk1[10].PE_i (PE_0)	44	34	1	0	0
▼ Clocking	genblk2[0].genblk1[11].PE_i (PE_1)	44	34	1	0	0
BUFGCTRL (6%)	genblk2[0].genblk1[12].PE_i (PE_2)	44	34	1	0	0
Specific Feature	genblk2[0].genblk1[13].PE_i (PE_3)	44	34	1	0	0
Primitives	genblk2[0].genblk1[14].PE_i (PE_4)	44	34	1	0	0
Black Boxes	genblk2[0].genblk1[15].PE_i (PE_5)	44	34	1	0	0
Instantiated Netlists	genblk2[0].genblk1[16].PE_i (PE_6)	44	34	1	0	0
	genblk2[0].genblk1[17].PE_i (PE_7)	44	34	1	0	0

## 2.2.4.Timing Report

### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.284 ns	Worst Hold Slack (WHS): 0.145 ns	Worst Pulse Width Slack (WPWS): 1.728 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 30208	Total Number of Endpoints: 30208	Total Number of Endpoints: 16897

All user specified timing constraints are met.

## 2.2.5.Power Report

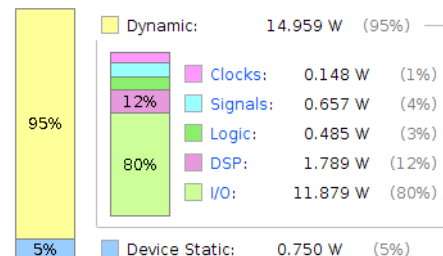
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

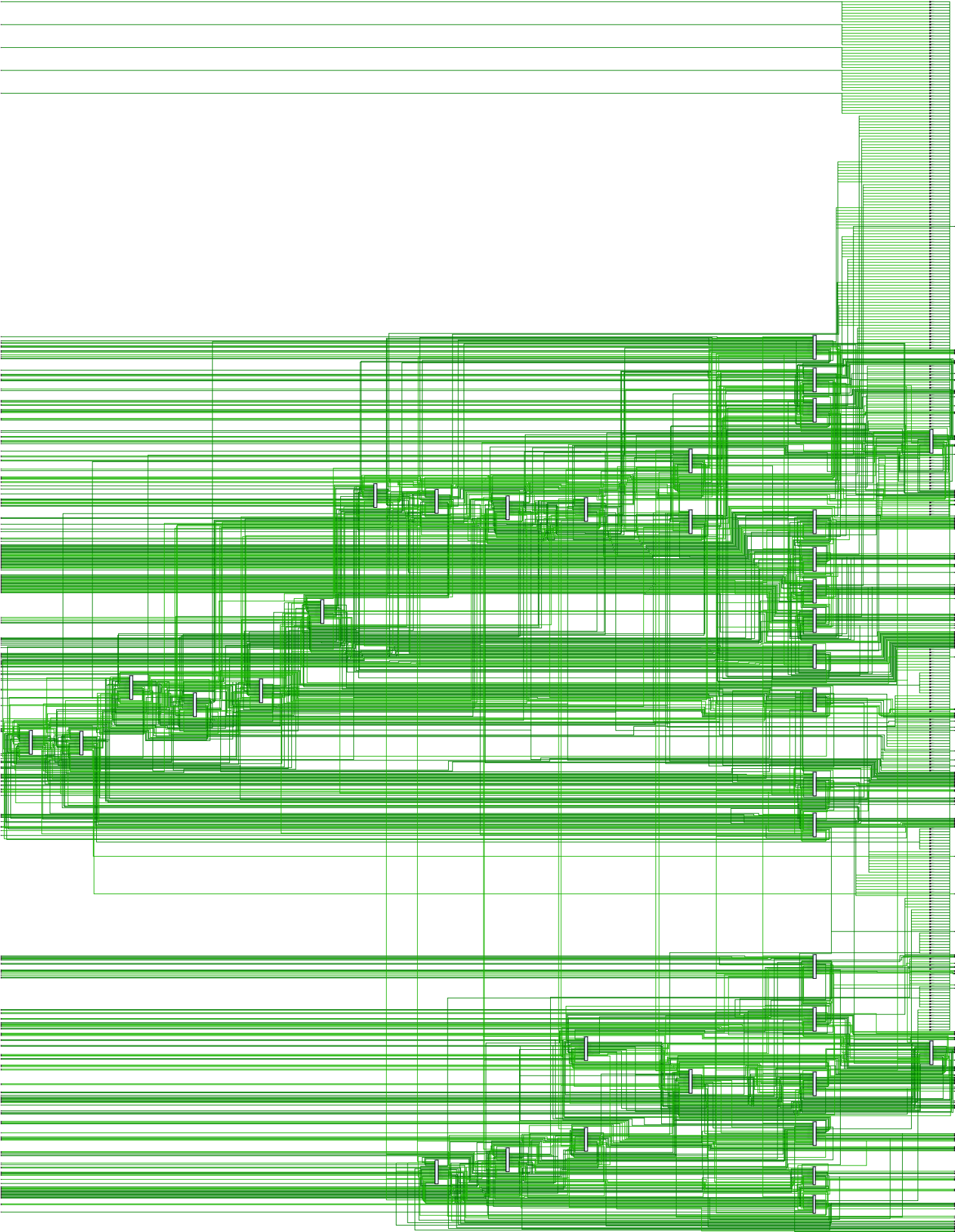
Total On-Chip Power:	15.709 W (Junction temp exceeded!)
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	125.0°C
Thermal Margin:	-106.2°C (-8.8 W)
Effective $\theta_{JA}$ :	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

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### On-Chip Power



Big Picture:



PE:

