EE 599
Spring 2020
Homework 1

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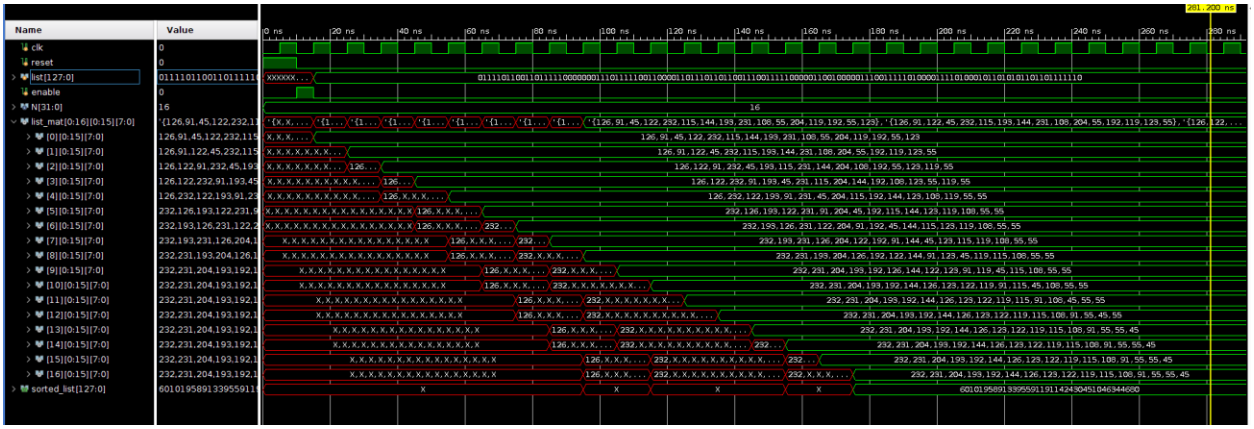
Github Repo: https://github.com/pengmiao-usc/EE-599_PengmiaoZhang_7865959675

1. Odd-even transposition sort

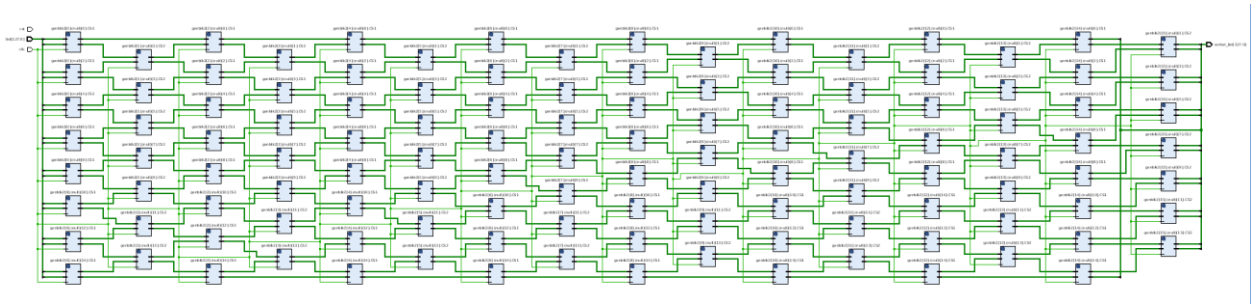
1.1. 16 elements

1.1.1.Waveforms

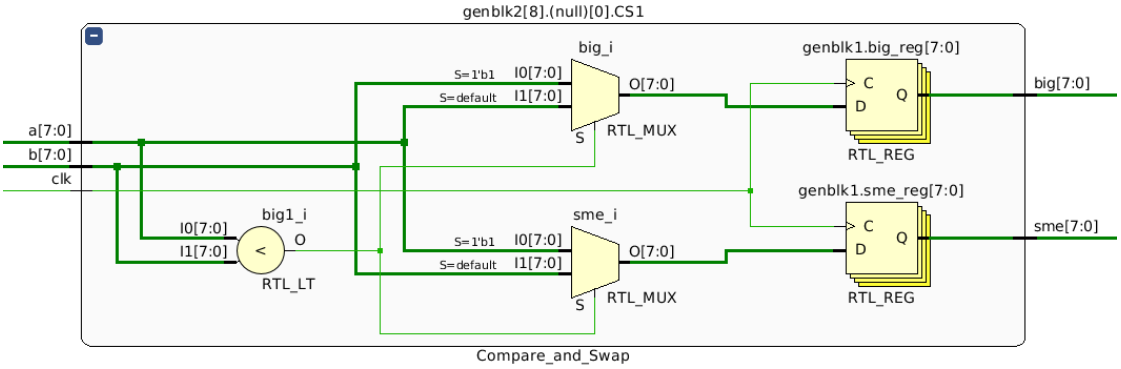


1.1.2.Schematics

1.1.2.1. OE_Sort

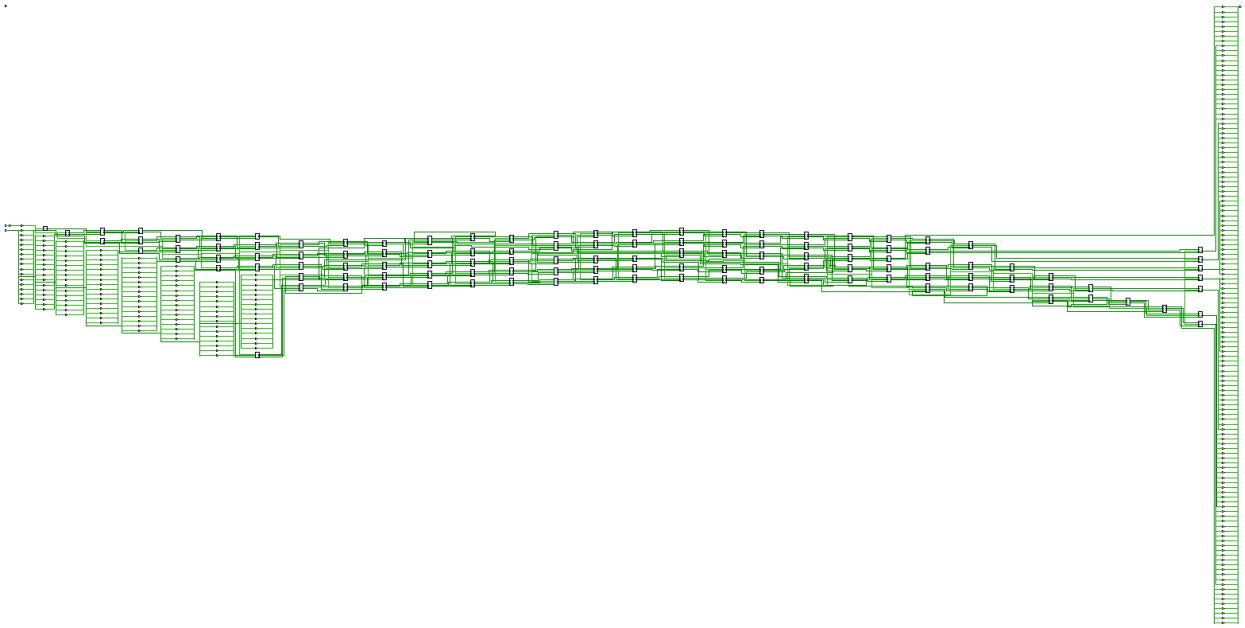


1.1.2.2. Compare_and_Swap

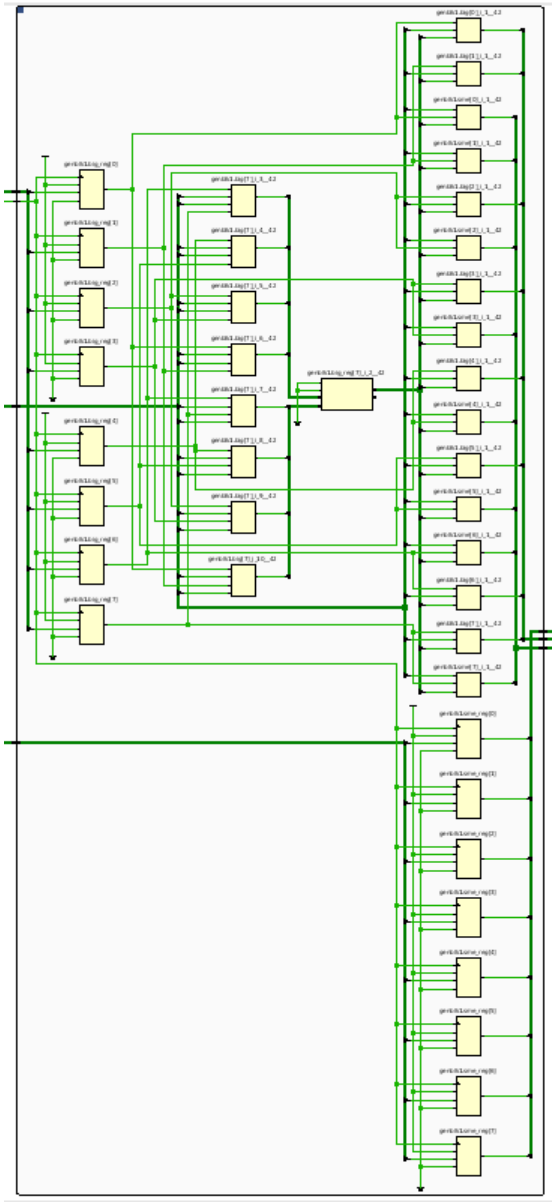


1.1.3.Synthesis

1.1.3.1. OE_Sort



1.1.3.2. Compare_and_Swap



1.1.4.Resource Report

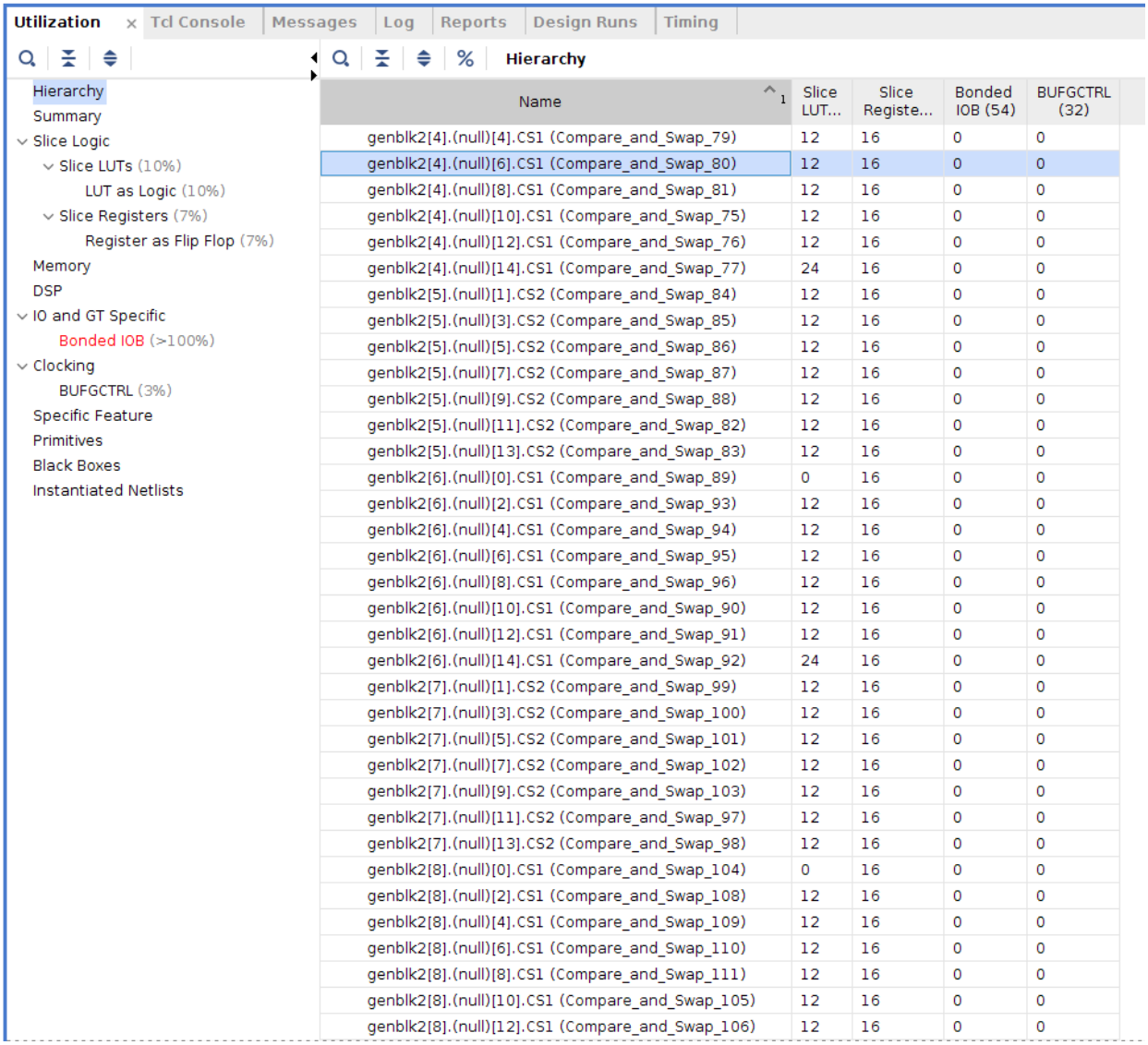
SYNTHESIZED DESIGN - xc7z007sclg225-2 (active)

Utilization | Tcl Console | Messages | Log | Reports | Design Runs | Timing

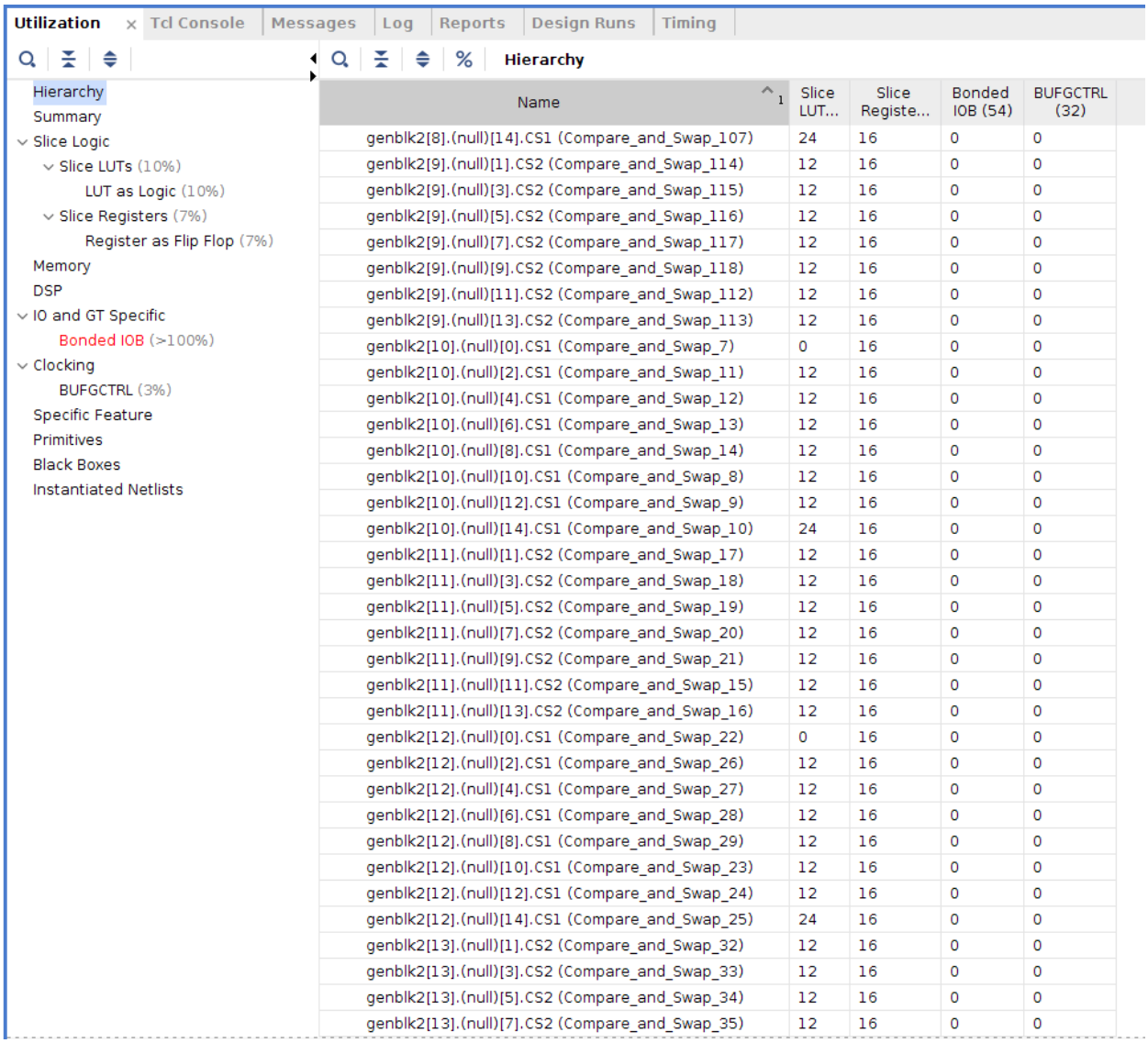
Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (10%)
    - LUT as Logic (10%)
  - Slice Registers (7%)
    - Register as Flip Flop (7%)
- Memory
- DSP
- IO and GT Specific
  - Bonded IOB (>100%)
- Clocking
  - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes
- Instantiated Netlists

Name	Slice LUT...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
OE_Sort	1440	1920	257	1
genblk2[0].(null)[0].CS1 (Compare_and_Swap)	12	16	0	0
genblk2[0].(null)[2].CS1 (Compare_and_Swap_3)	24	16	0	0
genblk2[0].(null)[4].CS1 (Compare_and_Swap_4)	24	16	0	0
genblk2[0].(null)[6].CS1 (Compare_and_Swap_5)	24	16	0	0
genblk2[0].(null)[8].CS1 (Compare_and_Swap_6)	24	16	0	0
genblk2[0].(null)[10].CS1 (Compare_and_Swap_0)	24	16	0	0
genblk2[0].(null)[12].CS1 (Compare_and_Swap_1)	24	16	0	0
genblk2[0].(null)[14].CS1 (Compare_and_Swap_2)	36	16	0	0
genblk2[1].(null)[1].CS2 (Compare_and_Swap_54)	12	16	0	0
genblk2[1].(null)[3].CS2 (Compare_and_Swap_55)	12	16	0	0
genblk2[1].(null)[5].CS2 (Compare_and_Swap_56)	12	16	0	0
genblk2[1].(null)[7].CS2 (Compare_and_Swap_57)	12	16	0	0
genblk2[1].(null)[9].CS2 (Compare_and_Swap_58)	12	16	0	0
genblk2[1].(null)[11].CS2 (Compare_and_Swap_52)	12	16	0	0
genblk2[1].(null)[13].CS2 (Compare_and_Swap_53)	12	16	0	0
genblk2[2].(null)[0].CS1 (Compare_and_Swap_59)	0	16	0	0
genblk2[2].(null)[2].CS1 (Compare_and_Swap_63)	12	16	0	0
genblk2[2].(null)[4].CS1 (Compare_and_Swap_64)	12	16	0	0
genblk2[2].(null)[6].CS1 (Compare_and_Swap_65)	12	16	0	0
genblk2[2].(null)[8].CS1 (Compare_and_Swap_66)	12	16	0	0
genblk2[2].(null)[10].CS1 (Compare_and_Swap_60)	12	16	0	0
genblk2[2].(null)[12].CS1 (Compare_and_Swap_61)	12	16	0	0
genblk2[2].(null)[14].CS1 (Compare_and_Swap_62)	24	16	0	0
genblk2[3].(null)[1].CS2 (Compare_and_Swap_69)	12	16	0	0
genblk2[3].(null)[3].CS2 (Compare_and_Swap_70)	12	16	0	0
genblk2[3].(null)[5].CS2 (Compare_and_Swap_71)	12	16	0	0
genblk2[3].(null)[7].CS2 (Compare_and_Swap_72)	12	16	0	0
genblk2[3].(null)[9].CS2 (Compare_and_Swap_73)	12	16	0	0
genblk2[3].(null)[11].CS2 (Compare_and_Swap_67)	12	16	0	0
genblk2[3].(null)[13].CS2 (Compare_and_Swap_68)	12	16	0	0
genblk2[4].(null)[0].CS1 (Compare_and_Swap_74)	0	16	0	0
genblk2[4].(null)[2].CS1 (Compare_and_Swap_78)	12	16	0	0
genblk2[4].(null)[4].CS1 (Compare_and_Swap_79)	12	16	0	0
genblk2[4].(null)[6].CS1 (Compare_and_Swap_80)	12	16	0	0

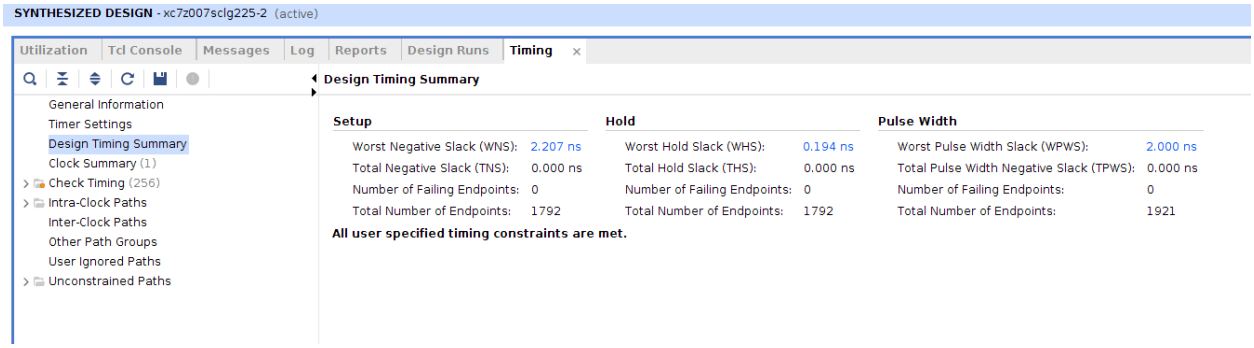


Name	Slice LUT...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
genblk2[4].(null)[4].CS1 (Compare_and_Swap_79)	12	16	0	0
genblk2[4].(null)[6].CS1 (Compare_and_Swap_80)	12	16	0	0
genblk2[4].(null)[8].CS1 (Compare_and_Swap_81)	12	16	0	0
genblk2[4].(null)[10].CS1 (Compare_and_Swap_75)	12	16	0	0
genblk2[4].(null)[12].CS1 (Compare_and_Swap_76)	12	16	0	0
genblk2[4].(null)[14].CS1 (Compare_and_Swap_77)	24	16	0	0
genblk2[5].(null)[1].CS2 (Compare_and_Swap_84)	12	16	0	0
genblk2[5].(null)[3].CS2 (Compare_and_Swap_85)	12	16	0	0
genblk2[5].(null)[5].CS2 (Compare_and_Swap_86)	12	16	0	0
genblk2[5].(null)[7].CS2 (Compare_and_Swap_87)	12	16	0	0
genblk2[5].(null)[9].CS2 (Compare_and_Swap_88)	12	16	0	0
genblk2[5].(null)[11].CS2 (Compare_and_Swap_82)	12	16	0	0
genblk2[5].(null)[13].CS2 (Compare_and_Swap_83)	12	16	0	0
genblk2[6].(null)[0].CS1 (Compare_and_Swap_89)	0	16	0	0
genblk2[6].(null)[2].CS1 (Compare_and_Swap_93)	12	16	0	0
genblk2[6].(null)[4].CS1 (Compare_and_Swap_94)	12	16	0	0
genblk2[6].(null)[6].CS1 (Compare_and_Swap_95)	12	16	0	0
genblk2[6].(null)[8].CS1 (Compare_and_Swap_96)	12	16	0	0
genblk2[6].(null)[10].CS1 (Compare_and_Swap_90)	12	16	0	0
genblk2[6].(null)[12].CS1 (Compare_and_Swap_91)	12	16	0	0
genblk2[6].(null)[14].CS1 (Compare_and_Swap_92)	24	16	0	0
genblk2[7].(null)[1].CS2 (Compare_and_Swap_99)	12	16	0	0
genblk2[7].(null)[3].CS2 (Compare_and_Swap_100)	12	16	0	0
genblk2[7].(null)[5].CS2 (Compare_and_Swap_101)	12	16	0	0
genblk2[7].(null)[7].CS2 (Compare_and_Swap_102)	12	16	0	0
genblk2[7].(null)[9].CS2 (Compare_and_Swap_103)	12	16	0	0
genblk2[7].(null)[11].CS2 (Compare_and_Swap_97)	12	16	0	0
genblk2[7].(null)[13].CS2 (Compare_and_Swap_98)	12	16	0	0
genblk2[8].(null)[0].CS1 (Compare_and_Swap_104)	0	16	0	0
genblk2[8].(null)[2].CS1 (Compare_and_Swap_108)	12	16	0	0
genblk2[8].(null)[4].CS1 (Compare_and_Swap_109)	12	16	0	0
genblk2[8].(null)[6].CS1 (Compare_and_Swap_110)	12	16	0	0
genblk2[8].(null)[8].CS1 (Compare_and_Swap_111)	12	16	0	0
genblk2[8].(null)[10].CS1 (Compare_and_Swap_105)	12	16	0	0
genblk2[8].(null)[12].CS1 (Compare_and_Swap_106)	12	16	0	0



Name	Slice LUT...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
genblk2[8].(null)[14].CS1 (Compare_and_Swap_107)	24	16	0	0
genblk2[9].(null)[1].CS2 (Compare_and_Swap_114)	12	16	0	0
genblk2[9].(null)[3].CS2 (Compare_and_Swap_115)	12	16	0	0
genblk2[9].(null)[5].CS2 (Compare_and_Swap_116)	12	16	0	0
genblk2[9].(null)[7].CS2 (Compare_and_Swap_117)	12	16	0	0
genblk2[9].(null)[9].CS2 (Compare_and_Swap_118)	12	16	0	0
genblk2[9].(null)[11].CS2 (Compare_and_Swap_112)	12	16	0	0
genblk2[9].(null)[13].CS2 (Compare_and_Swap_113)	12	16	0	0
genblk2[10].(null)[0].CS1 (Compare_and_Swap_7)	0	16	0	0
genblk2[10].(null)[2].CS1 (Compare_and_Swap_11)	12	16	0	0
genblk2[10].(null)[4].CS1 (Compare_and_Swap_12)	12	16	0	0
genblk2[10].(null)[6].CS1 (Compare_and_Swap_13)	12	16	0	0
genblk2[10].(null)[8].CS1 (Compare_and_Swap_14)	12	16	0	0
genblk2[10].(null)[10].CS1 (Compare_and_Swap_8)	12	16	0	0
genblk2[10].(null)[12].CS1 (Compare_and_Swap_9)	12	16	0	0
genblk2[10].(null)[14].CS1 (Compare_and_Swap_10)	24	16	0	0
genblk2[11].(null)[1].CS2 (Compare_and_Swap_17)	12	16	0	0
genblk2[11].(null)[3].CS2 (Compare_and_Swap_18)	12	16	0	0
genblk2[11].(null)[5].CS2 (Compare_and_Swap_19)	12	16	0	0
genblk2[11].(null)[7].CS2 (Compare_and_Swap_20)	12	16	0	0
genblk2[11].(null)[9].CS2 (Compare_and_Swap_21)	12	16	0	0
genblk2[11].(null)[11].CS2 (Compare_and_Swap_15)	12	16	0	0
genblk2[11].(null)[13].CS2 (Compare_and_Swap_16)	12	16	0	0
genblk2[12].(null)[0].CS1 (Compare_and_Swap_22)	0	16	0	0
genblk2[12].(null)[2].CS1 (Compare_and_Swap_26)	12	16	0	0
genblk2[12].(null)[4].CS1 (Compare_and_Swap_27)	12	16	0	0
genblk2[12].(null)[6].CS1 (Compare_and_Swap_28)	12	16	0	0
genblk2[12].(null)[8].CS1 (Compare_and_Swap_29)	12	16	0	0
genblk2[12].(null)[10].CS1 (Compare_and_Swap_23)	12	16	0	0
genblk2[12].(null)[12].CS1 (Compare_and_Swap_24)	12	16	0	0
genblk2[12].(null)[14].CS1 (Compare_and_Swap_25)	24	16	0	0
genblk2[13].(null)[1].CS2 (Compare_and_Swap_32)	12	16	0	0
genblk2[13].(null)[3].CS2 (Compare_and_Swap_33)	12	16	0	0
genblk2[13].(null)[5].CS2 (Compare_and_Swap_34)	12	16	0	0
genblk2[13].(null)[7].CS2 (Compare_and_Swap_35)	12	16	0	0
genblk2[13].(null)[9].CS2 (Compare_and_Swap_36)	12	16	0	0
genblk2[13].(null)[11].CS2 (Compare_and_Swap_30)	12	16	0	0
genblk2[13].(null)[13].CS2 (Compare_and_Swap_31)	12	16	0	0
genblk2[14].(null)[0].CS1 (Compare_and_Swap_37)	0	16	0	0
genblk2[14].(null)[2].CS1 (Compare_and_Swap_41)	12	16	0	0
genblk2[14].(null)[4].CS1 (Compare_and_Swap_42)	12	16	0	0
genblk2[14].(null)[6].CS1 (Compare_and_Swap_43)	12	16	0	0
genblk2[14].(null)[8].CS1 (Compare_and_Swap_44)	12	16	0	0
genblk2[14].(null)[10].CS1 (Compare_and_Swap_38)	12	16	0	0
genblk2[14].(null)[12].CS1 (Compare_and_Swap_39)	12	16	0	0
genblk2[14].(null)[14].CS1 (Compare_and_Swap_40)	12	16	0	0
genblk2[15].(null)[1].CS2 (Compare_and_Swap_47)	0	16	0	0
genblk2[15].(null)[3].CS2 (Compare_and_Swap_48)	0	16	0	0
genblk2[15].(null)[5].CS2 (Compare_and_Swap_49)	0	16	0	0
genblk2[15].(null)[7].CS2 (Compare_and_Swap_50)	0	16	0	0
genblk2[15].(null)[9].CS2 (Compare_and_Swap_51)	0	16	0	0
genblk2[15].(null)[11].CS2 (Compare_and_Swap_45)	0	16	0	0
genblk2[15].(null)[13].CS2 (Compare_and_Swap_46)	0	16	0	0

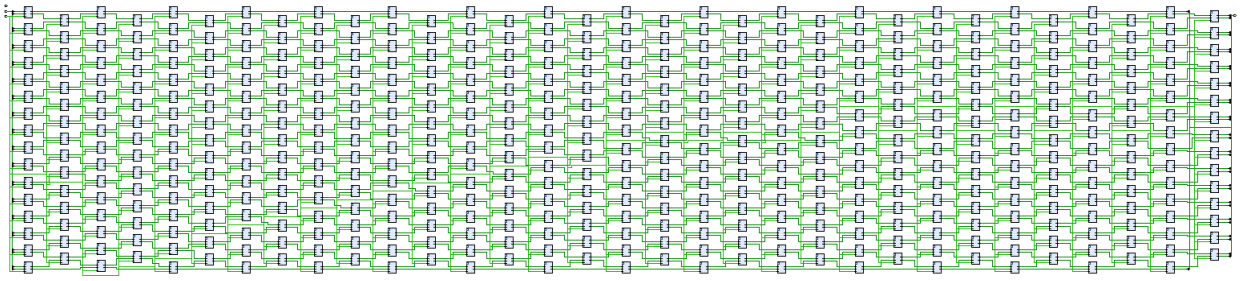
1.1.5.Timing Report



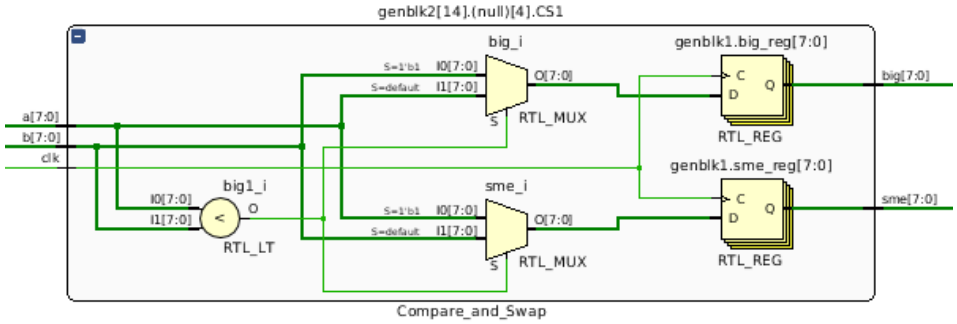
1.2. 32 elements

1.2.1.Schematics

1.2.1.1. OE_Sort

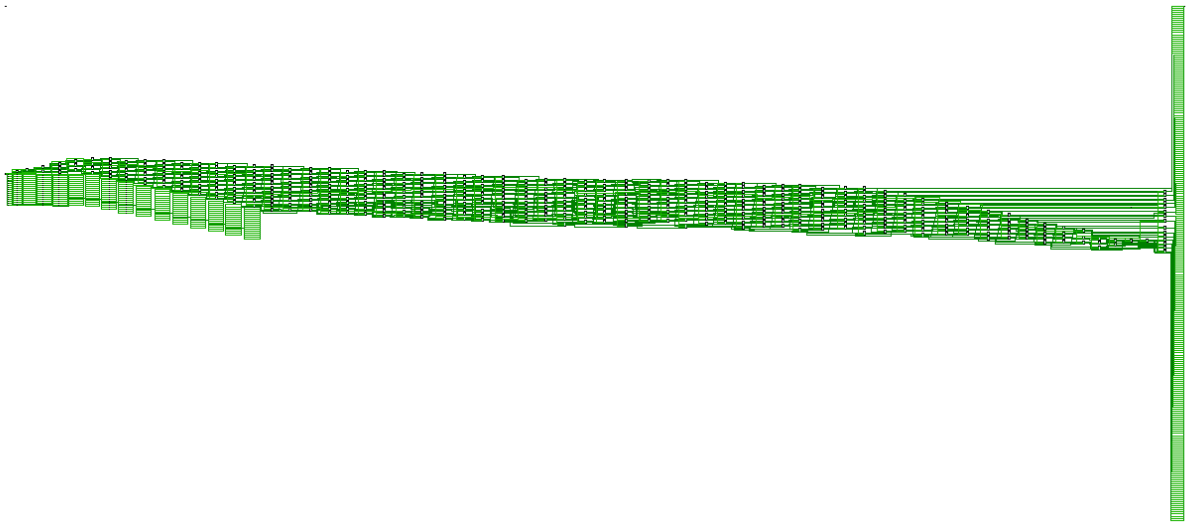


1.2.1.2. Compare_and_Swap

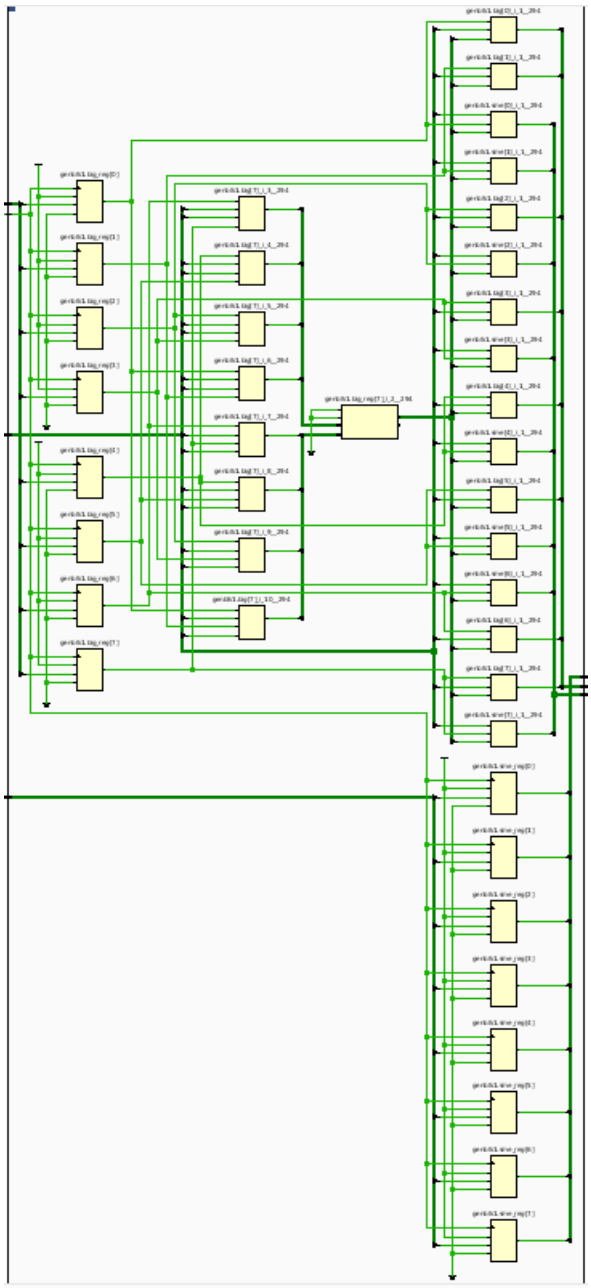


1.2.2.Synthesis

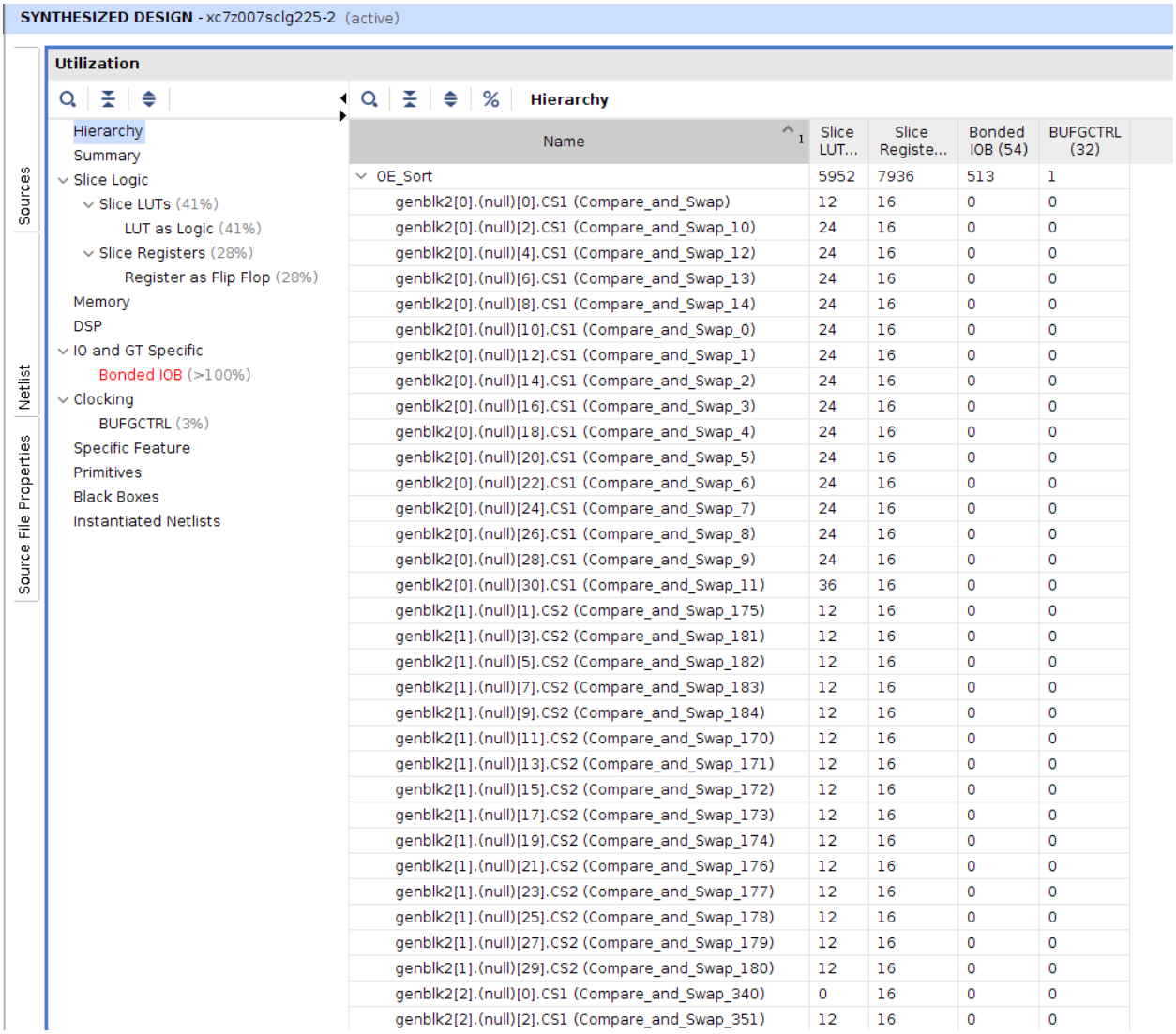
1.2.2.1. OE_Sort



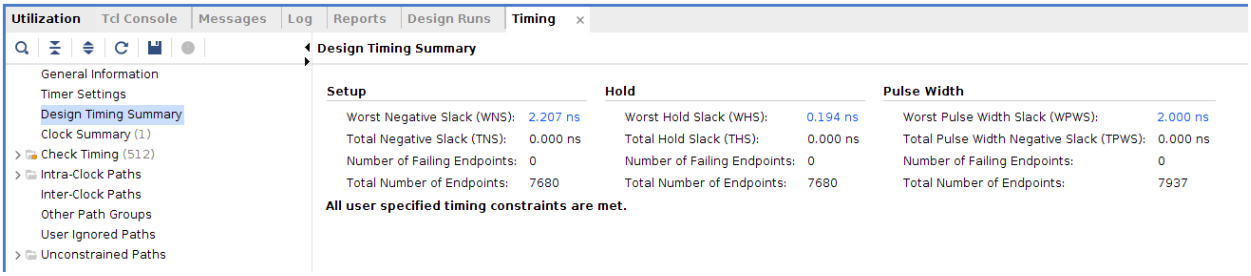
1.2.2.2. Compare_and_Swap



1.2.3.Resource Report



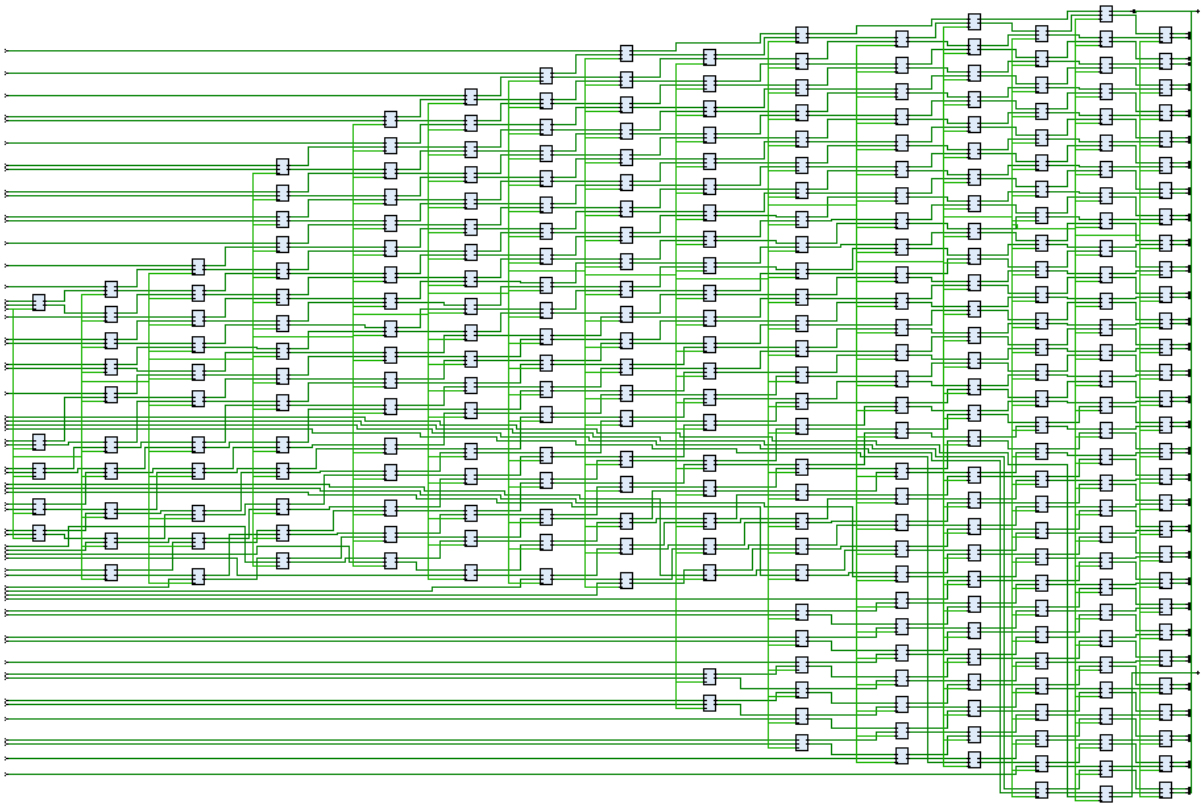
1.2.4.Timing Report



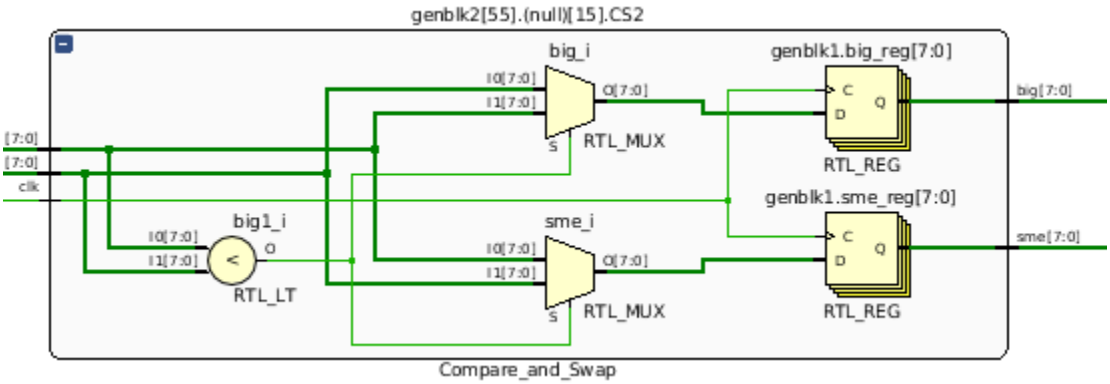
1.3. 64 elements

1.3.1.Schematics

1.3.1.1. OE_Sort

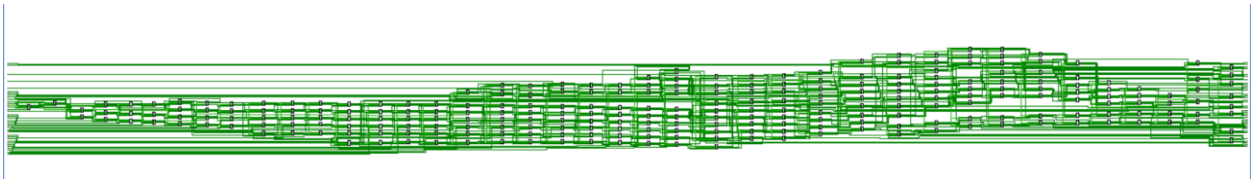


1.3.1.2. Compare_and_Swap

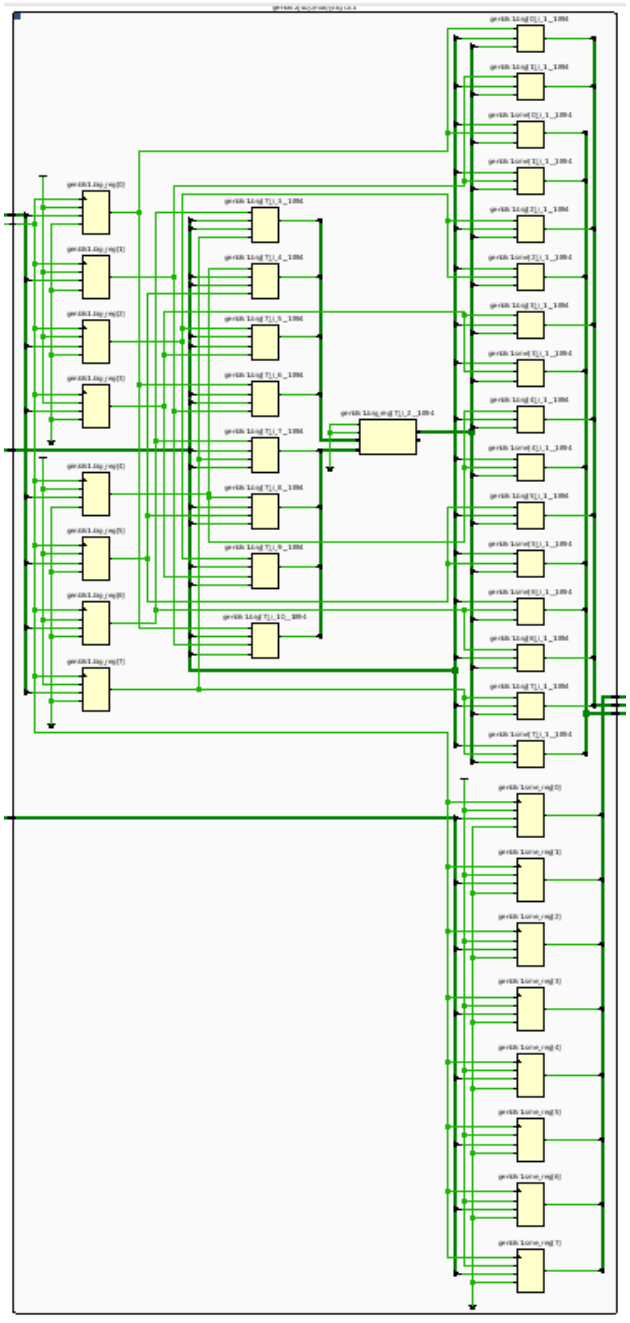


1.3.2.Synthesis

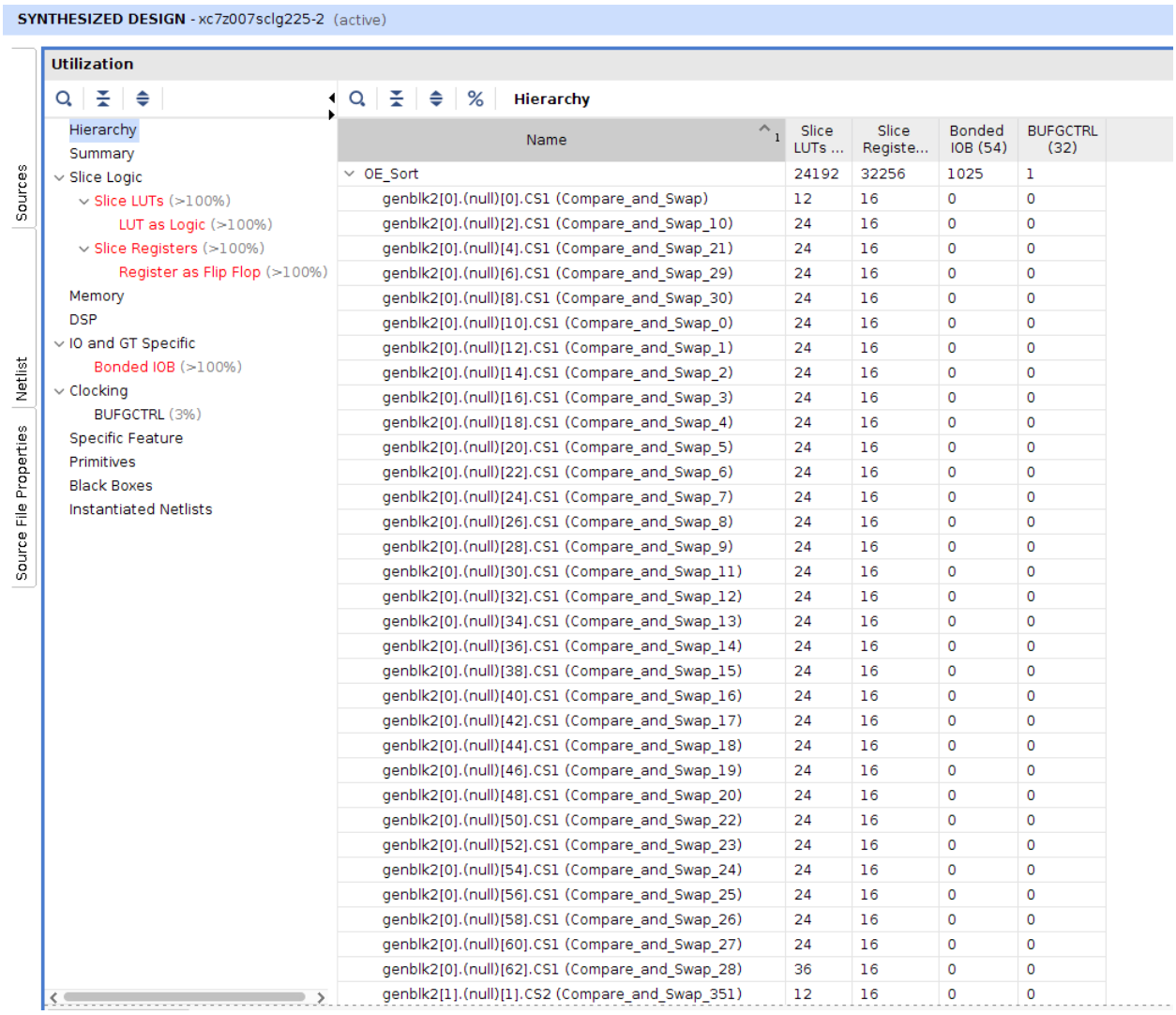
1.3.2.1. OE_Sort



1.3.2.2. Compare_and_Swap

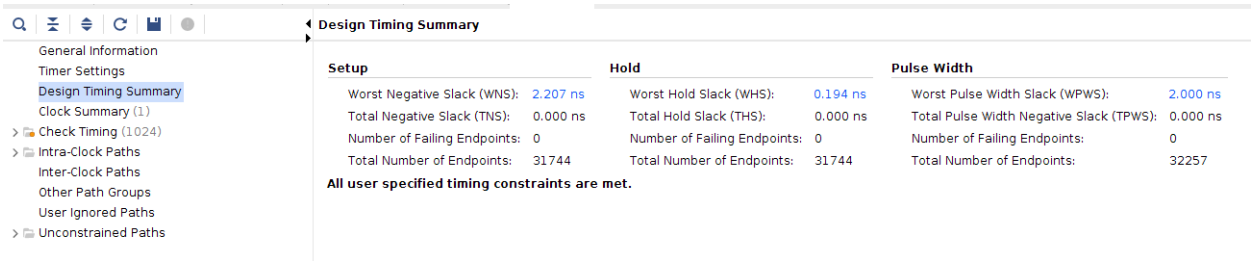


1.3.3.Resource Report



Name	Slice LUTs ...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
OE_Sort	24192	32256	1025	1
genblk2[0].(null)[0].CS1 (Compare_and_Swap)	12	16	0	0
genblk2[0].(null)[2].CS1 (Compare_and_Swap_10)	24	16	0	0
genblk2[0].(null)[4].CS1 (Compare_and_Swap_21)	24	16	0	0
genblk2[0].(null)[6].CS1 (Compare_and_Swap_29)	24	16	0	0
genblk2[0].(null)[8].CS1 (Compare_and_Swap_30)	24	16	0	0
genblk2[0].(null)[10].CS1 (Compare_and_Swap_0)	24	16	0	0
genblk2[0].(null)[12].CS1 (Compare_and_Swap_1)	24	16	0	0
genblk2[0].(null)[14].CS1 (Compare_and_Swap_2)	24	16	0	0
genblk2[0].(null)[16].CS1 (Compare_and_Swap_3)	24	16	0	0
genblk2[0].(null)[18].CS1 (Compare_and_Swap_4)	24	16	0	0
genblk2[0].(null)[20].CS1 (Compare_and_Swap_5)	24	16	0	0
genblk2[0].(null)[22].CS1 (Compare_and_Swap_6)	24	16	0	0
genblk2[0].(null)[24].CS1 (Compare_and_Swap_7)	24	16	0	0
genblk2[0].(null)[26].CS1 (Compare_and_Swap_8)	24	16	0	0
genblk2[0].(null)[28].CS1 (Compare_and_Swap_9)	24	16	0	0
genblk2[0].(null)[30].CS1 (Compare_and_Swap_11)	24	16	0	0
genblk2[0].(null)[32].CS1 (Compare_and_Swap_12)	24	16	0	0
genblk2[0].(null)[34].CS1 (Compare_and_Swap_13)	24	16	0	0
genblk2[0].(null)[36].CS1 (Compare_and_Swap_14)	24	16	0	0
genblk2[0].(null)[38].CS1 (Compare_and_Swap_15)	24	16	0	0
genblk2[0].(null)[40].CS1 (Compare_and_Swap_16)	24	16	0	0
genblk2[0].(null)[42].CS1 (Compare_and_Swap_17)	24	16	0	0
genblk2[0].(null)[44].CS1 (Compare_and_Swap_18)	24	16	0	0
genblk2[0].(null)[46].CS1 (Compare_and_Swap_19)	24	16	0	0
genblk2[0].(null)[48].CS1 (Compare_and_Swap_20)	24	16	0	0
genblk2[0].(null)[50].CS1 (Compare_and_Swap_22)	24	16	0	0
genblk2[0].(null)[52].CS1 (Compare_and_Swap_23)	24	16	0	0
genblk2[0].(null)[54].CS1 (Compare_and_Swap_24)	24	16	0	0
genblk2[0].(null)[56].CS1 (Compare_and_Swap_25)	24	16	0	0
genblk2[0].(null)[58].CS1 (Compare_and_Swap_26)	24	16	0	0
genblk2[0].(null)[60].CS1 (Compare_and_Swap_27)	24	16	0	0
genblk2[0].(null)[62].CS1 (Compare_and_Swap_28)	36	16	0	0
genblk2[1].(null)[1].CS2 (Compare_and_Swap_351)	12	16	0	0

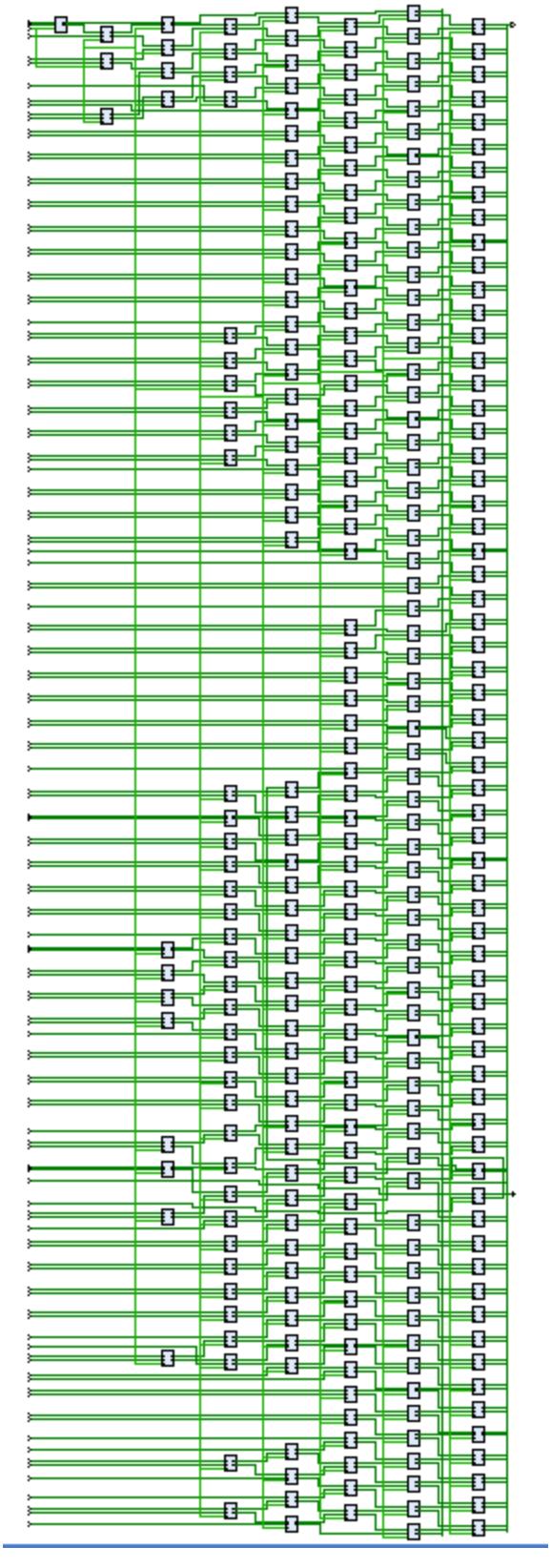
1.3.4.Timing Report



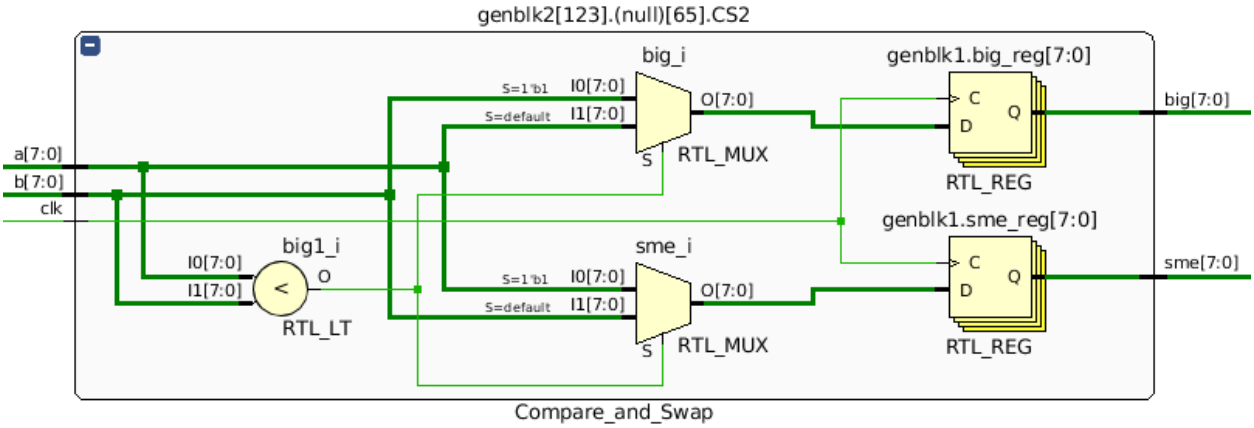
1.4. 128 elements

1.4.1.Schematics

1.4.1.1. OE_Sort

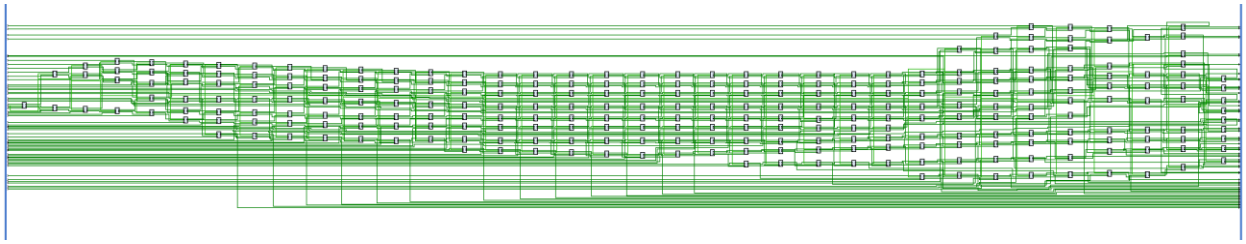


1.4.1.2. Campare_and_Swap

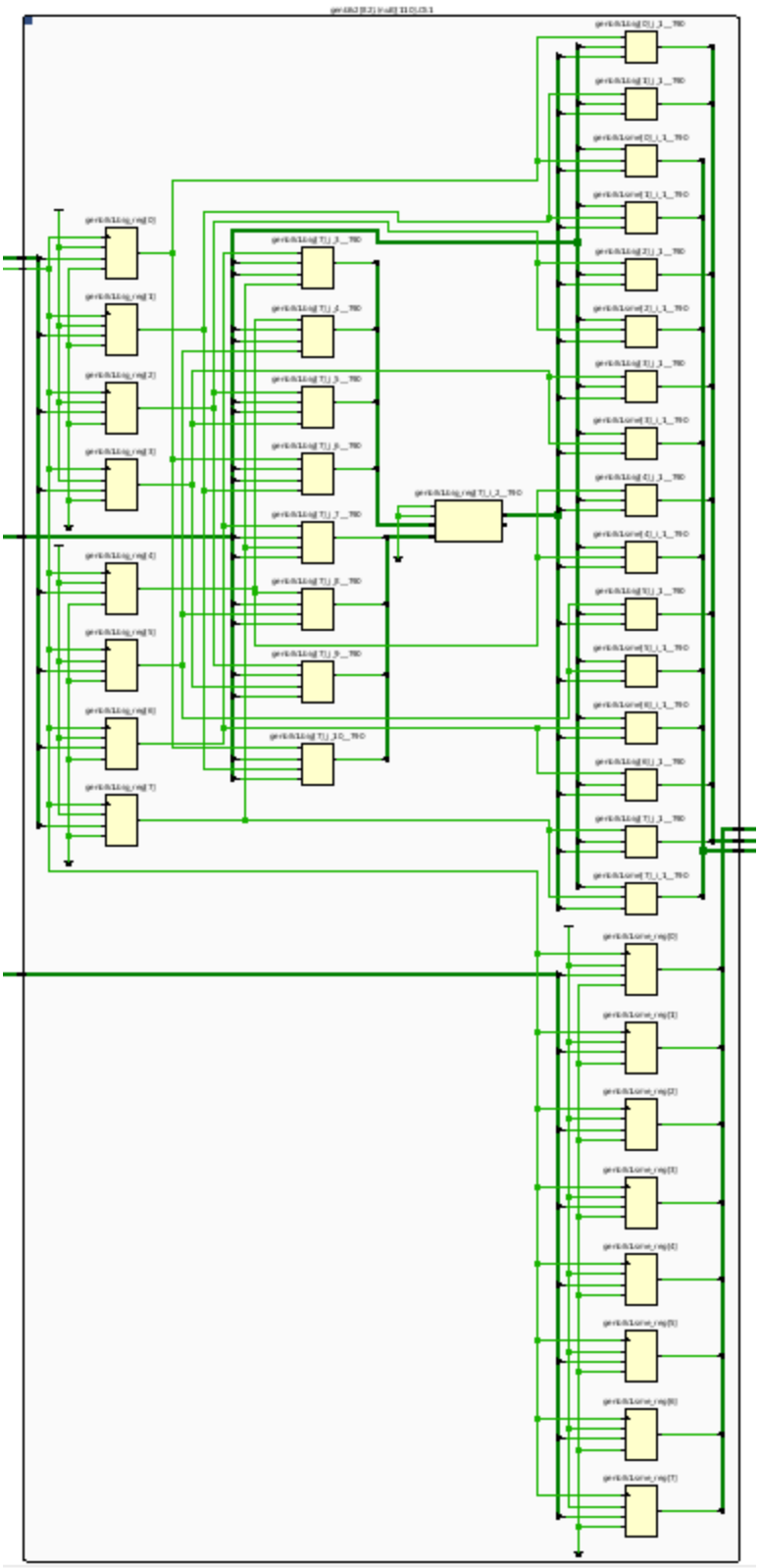


1.4.2.Synthesis

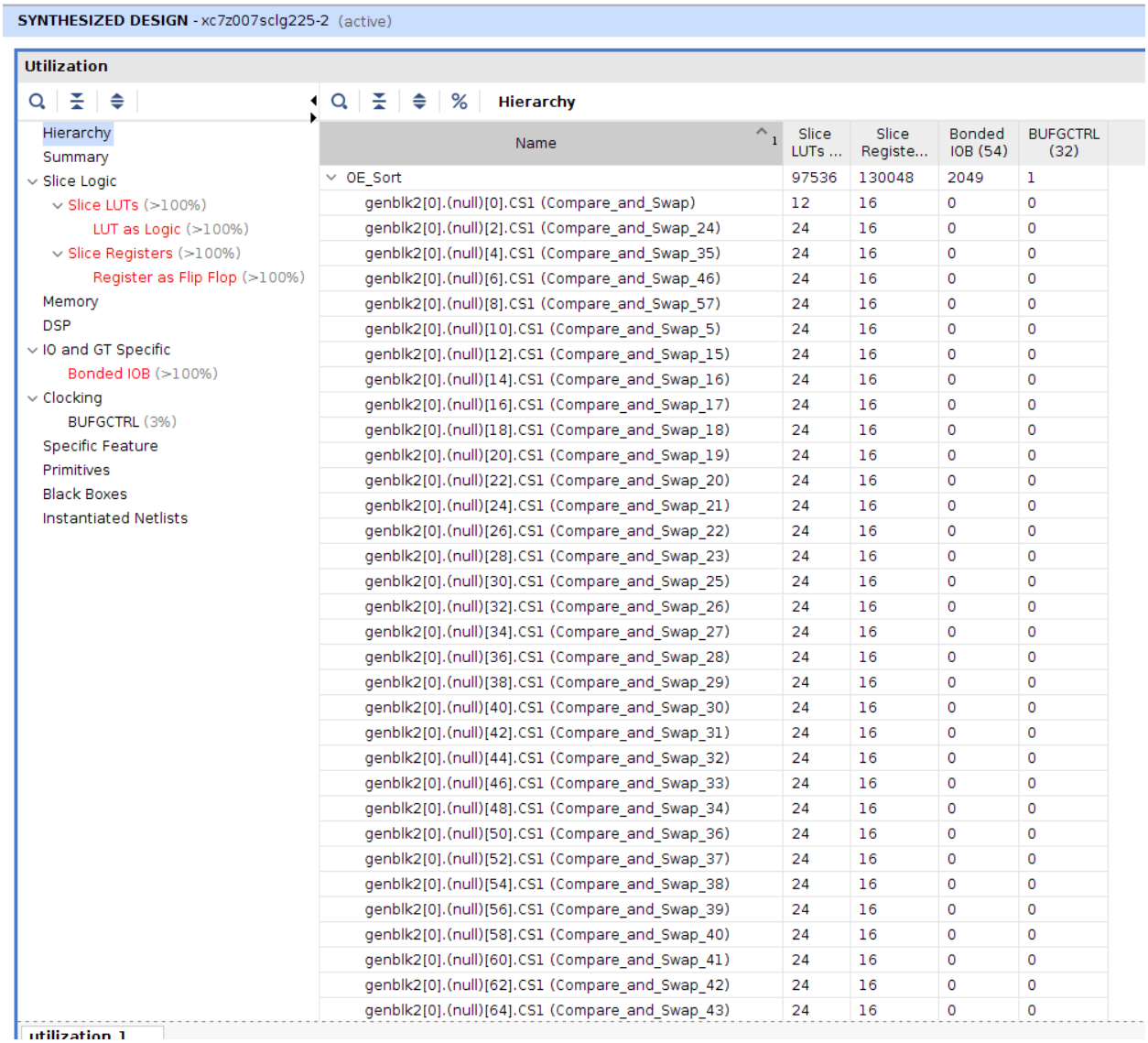
1.4.2.1. OE_Sort



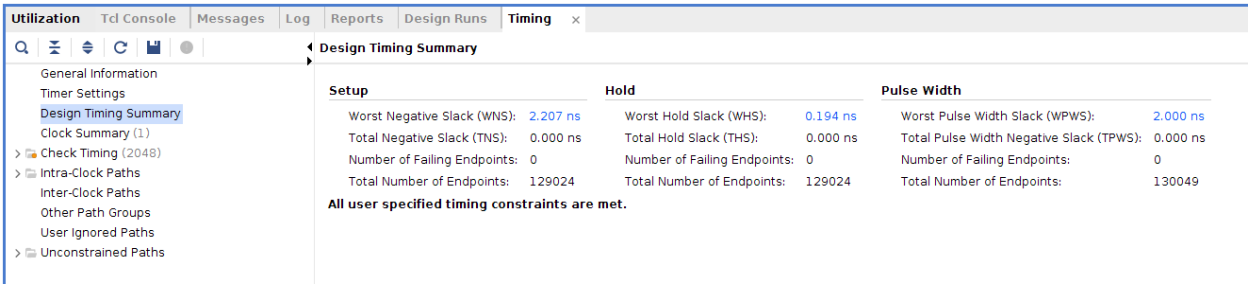
1.4.2.2. Campare_and_Swap



1.4.3.Resource Report



1.4.4.Timing Report

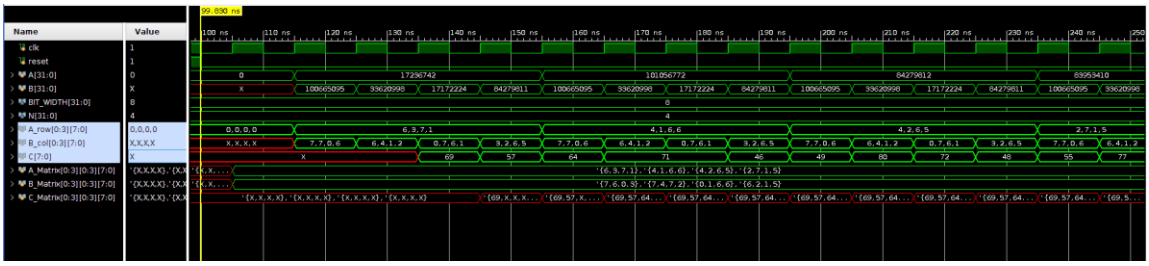


2. Dense Matrix-Matrix Multiplication

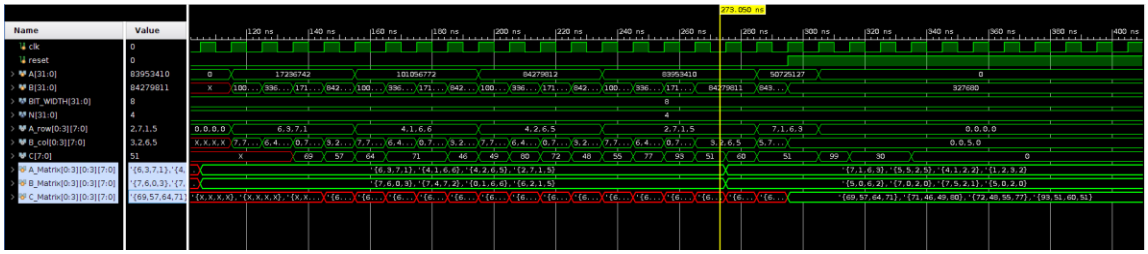
2.1. 4 X 4 Matrices

2.1.1. Waveforms

2.1.1.1. Input A_row and B_column, output element C, as highlighted.

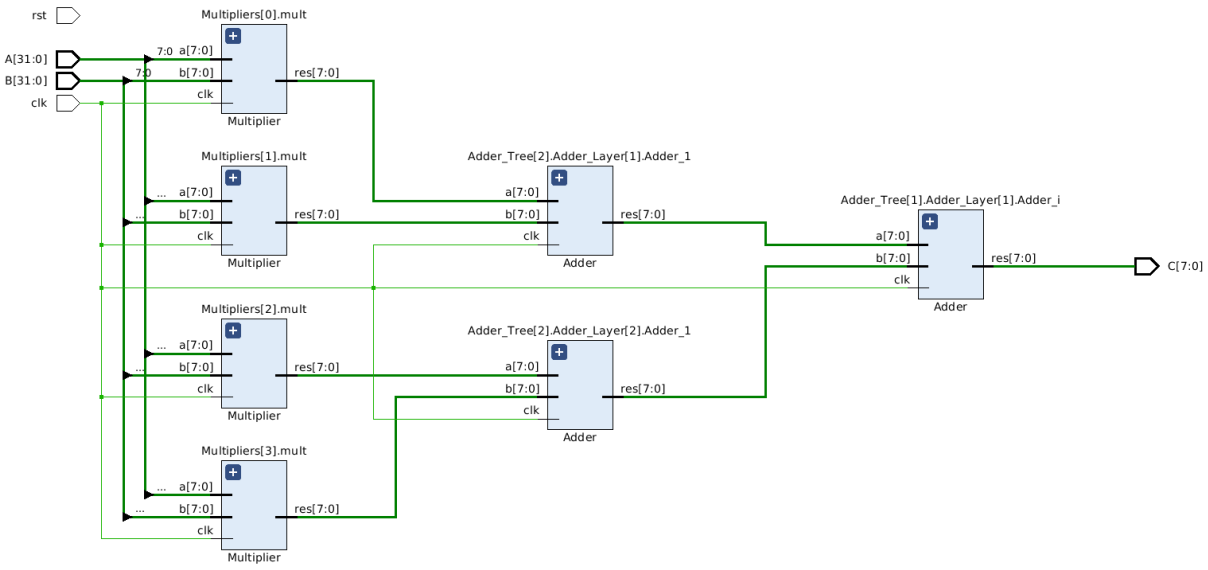


2.1.1.2. Matrix A, B and C, as highlighted.

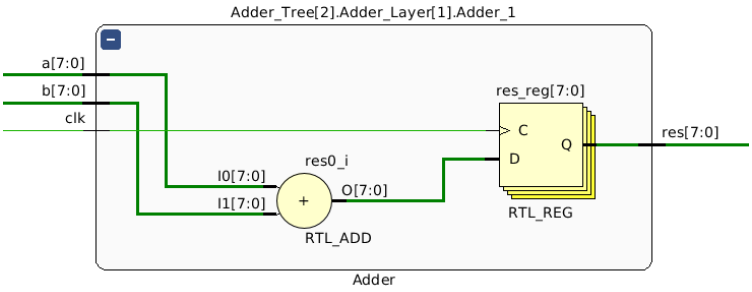


2.1.2.Schematics

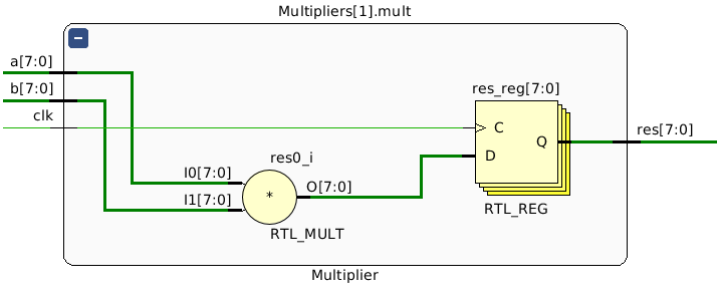
2.1.2.1. MulandAddTree



2.1.2.2. Adder

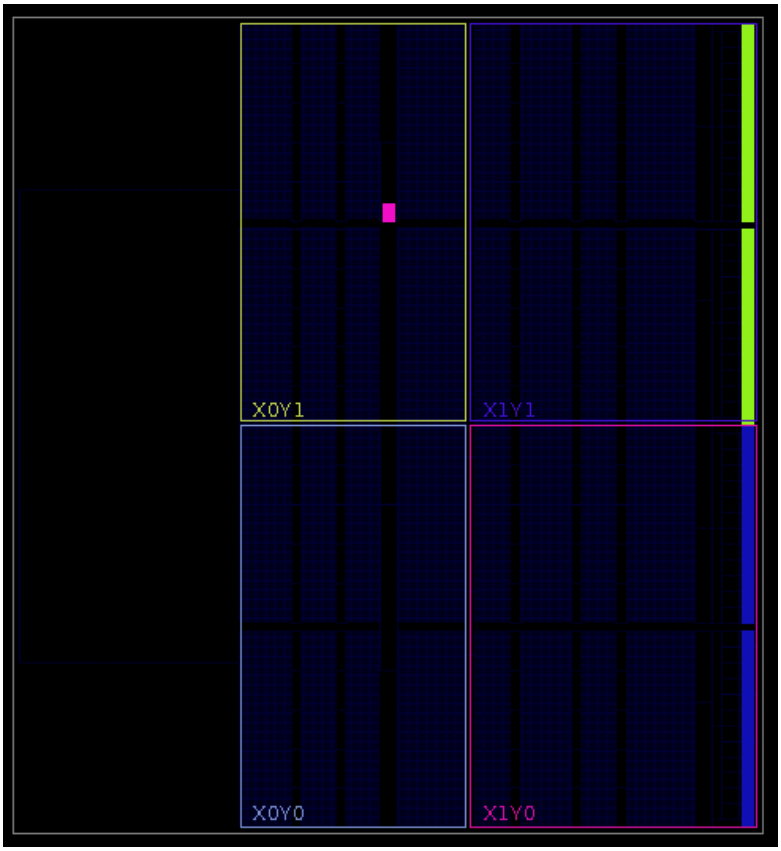


2.1.2.3. Multiplier

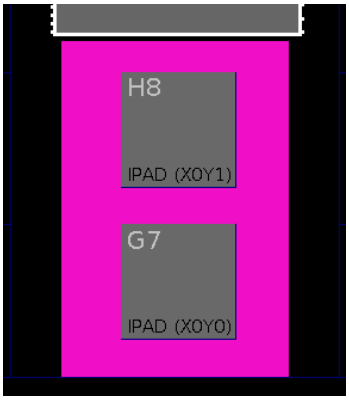


2.1.3.Synthesis

2.1.3.1. Big Picture

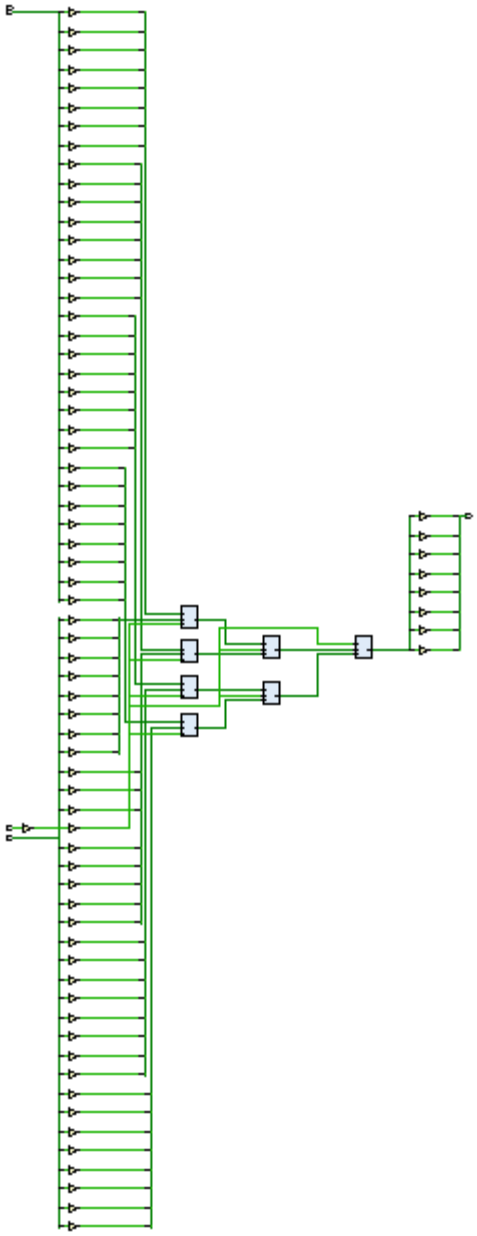


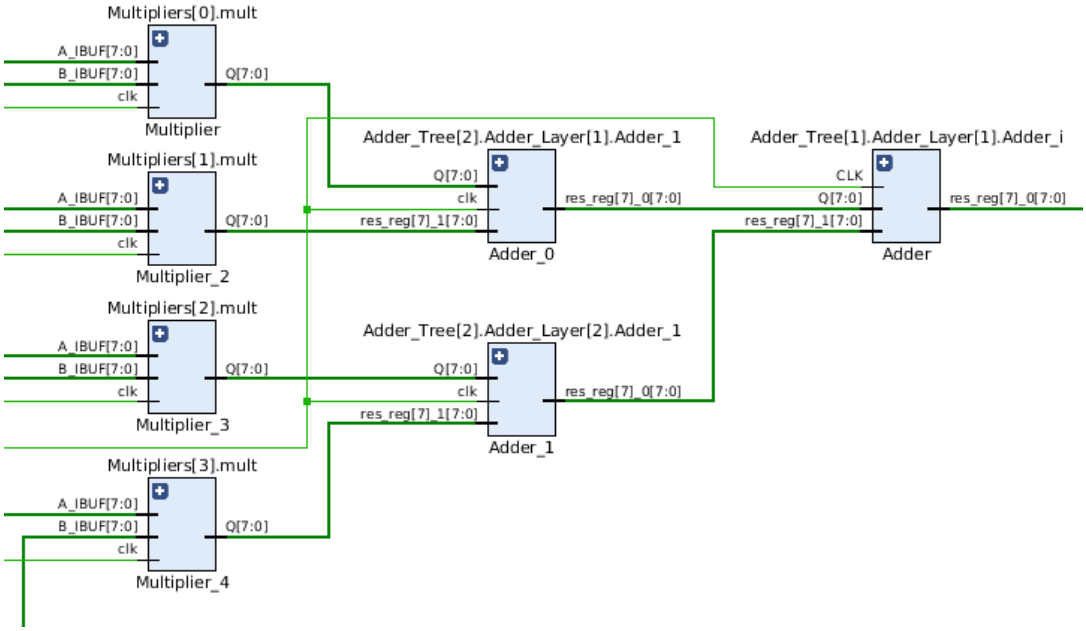
2.1.3.2. Detail

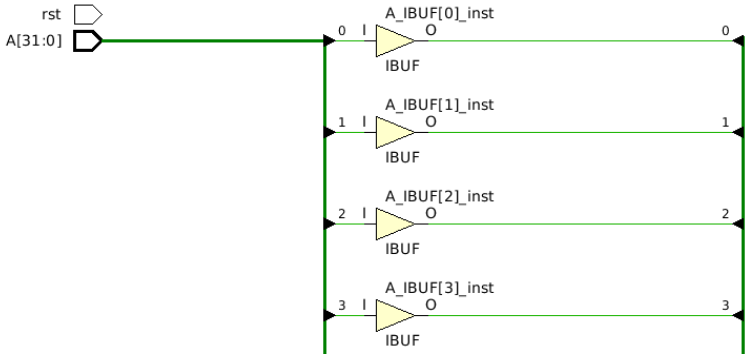


2.1.3.3. Schematic

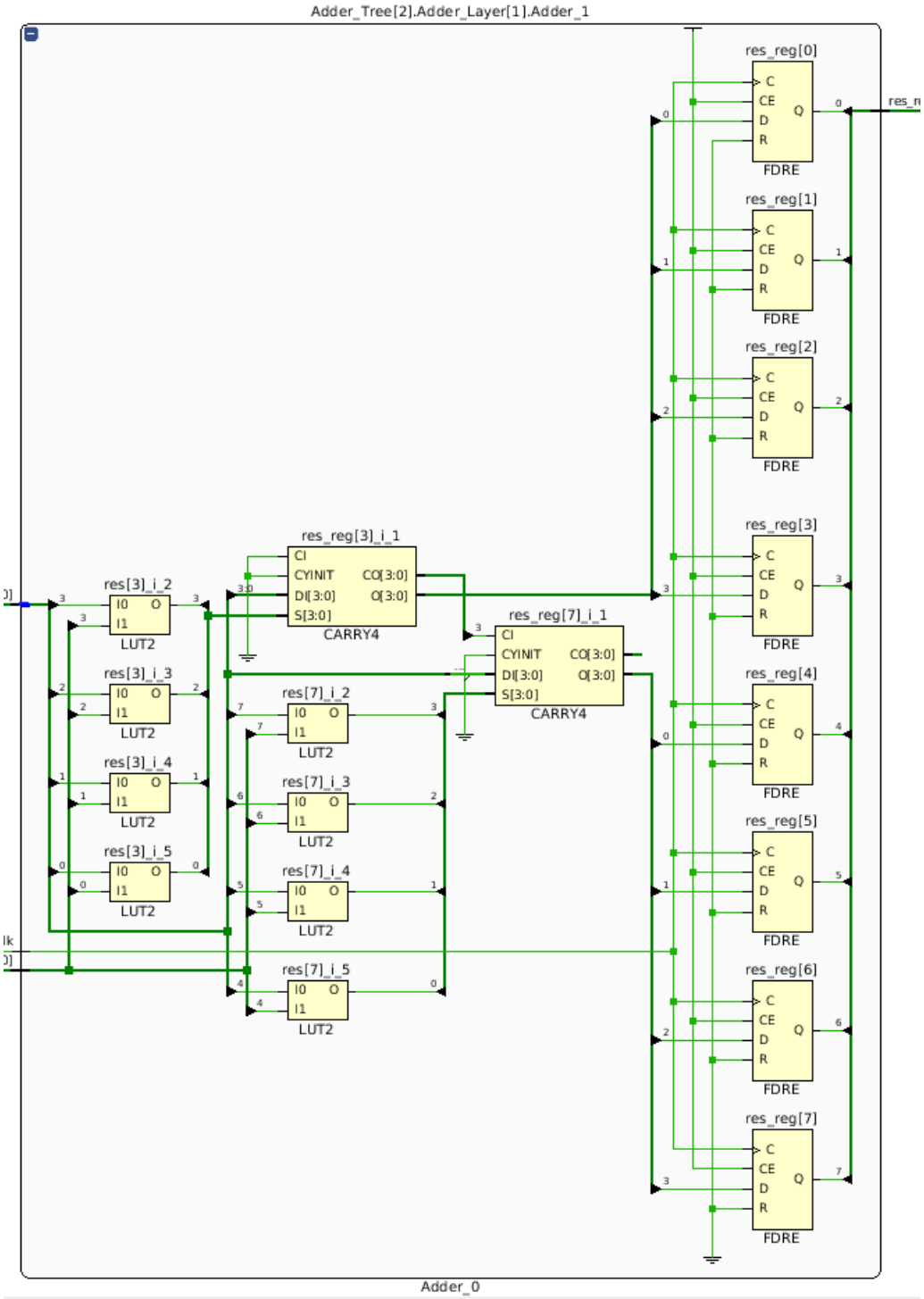
2.1.3.3.1. MulandAddTree



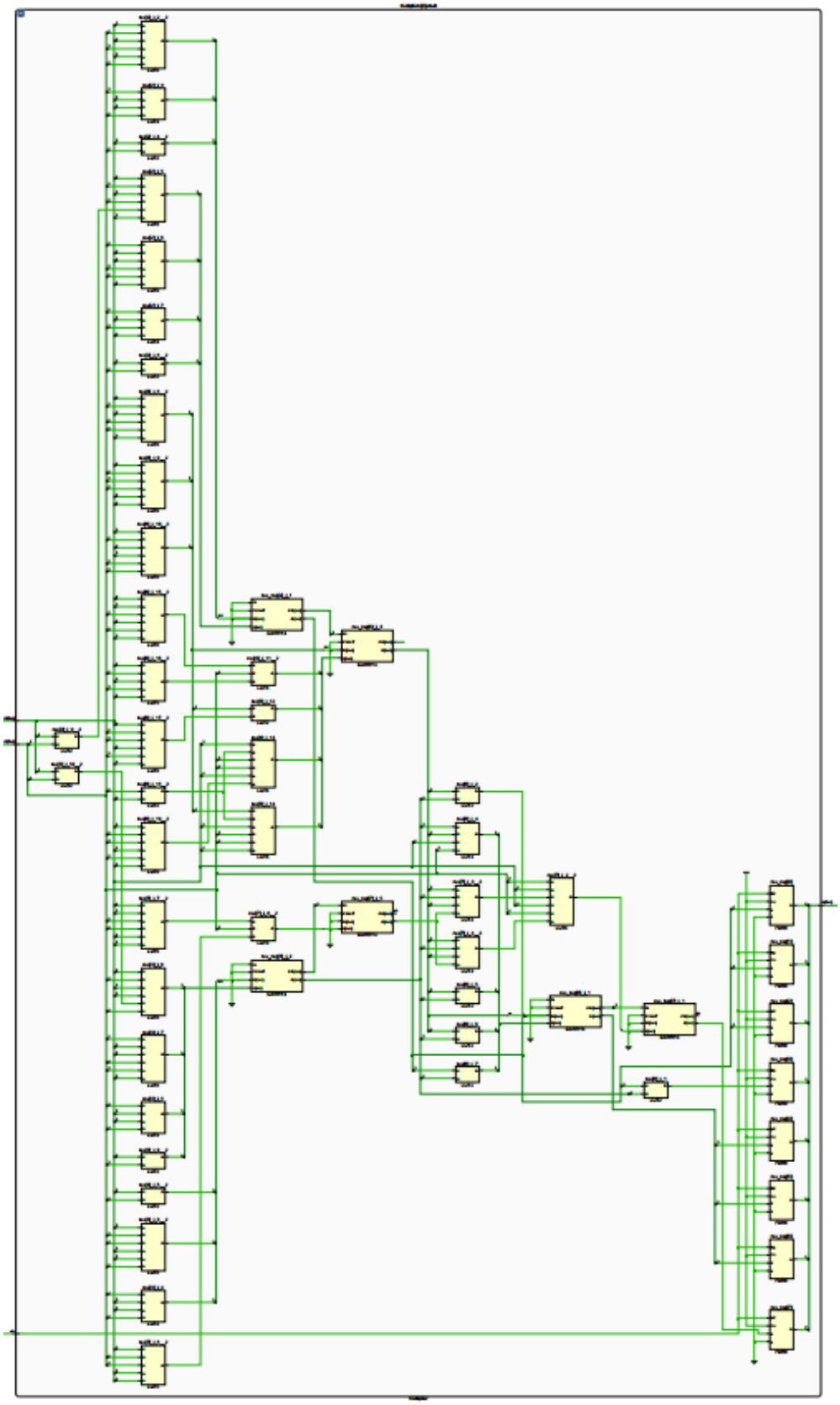

Multipliers[0].mult
A_IBUF[7:0]
B_IBUF[7:0]
clk
Q[7:0]
Multiplier
Multipliers[1].mult
Multiplier_2
Multipliers[2].mult
Multiplier_3
Multipliers[3].mult
Multiplier_4
Adder_Tree[2].Adder_Layer[1].Adder_1
Q[7:0]
clk
res_reg[7]_1[7:0]
res_reg[7]_0[7:0]
Adder_0
Adder_Tree[2].Adder_Layer[2].Adder_1
Adder_1
Adder_Tree[1].Adder_Layer[1].Adder_i
CLK
Adder

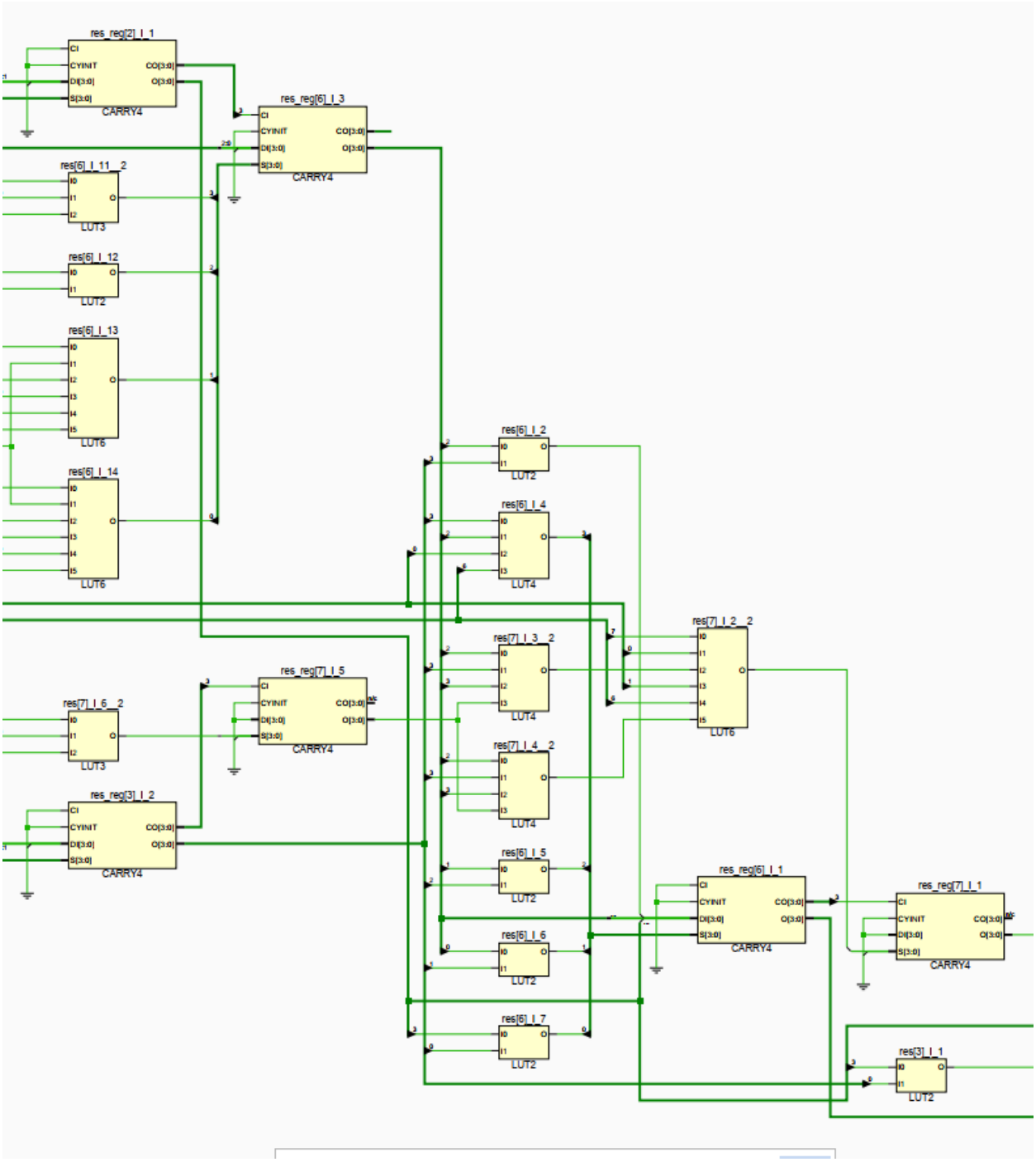

rst
A[31:0]
A_IBUF[0]_inst
A_IBUF[1]_inst
A_IBUF[2]_inst
A_IBUF[3]_inst
IBUF

2.1.3.3.2. Adder

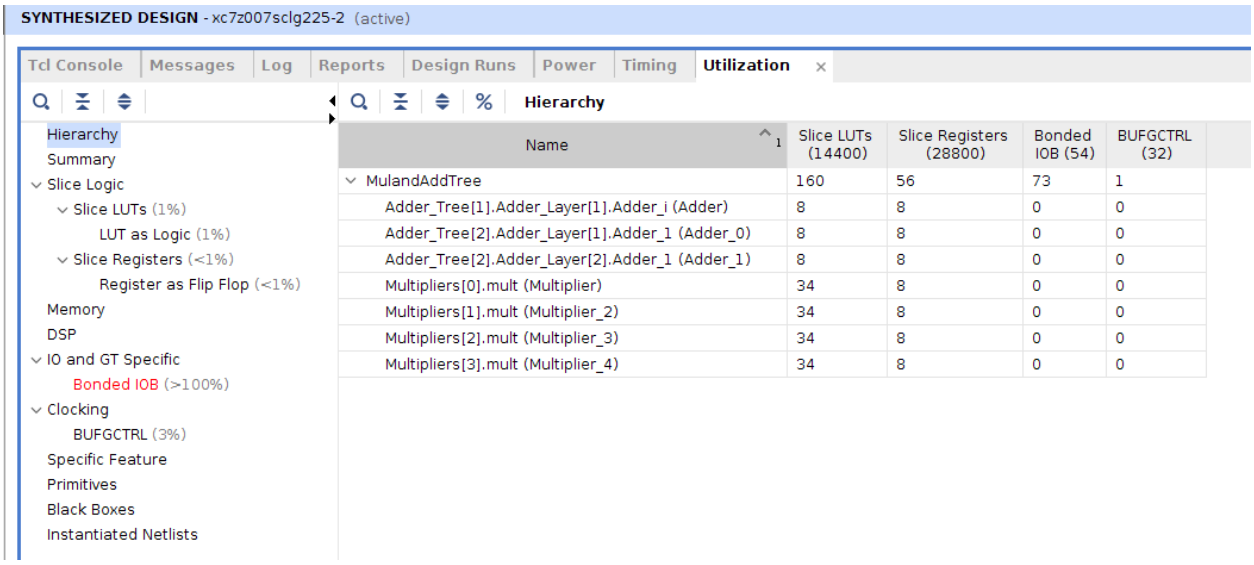


2.1.3.3.3. Multiplier

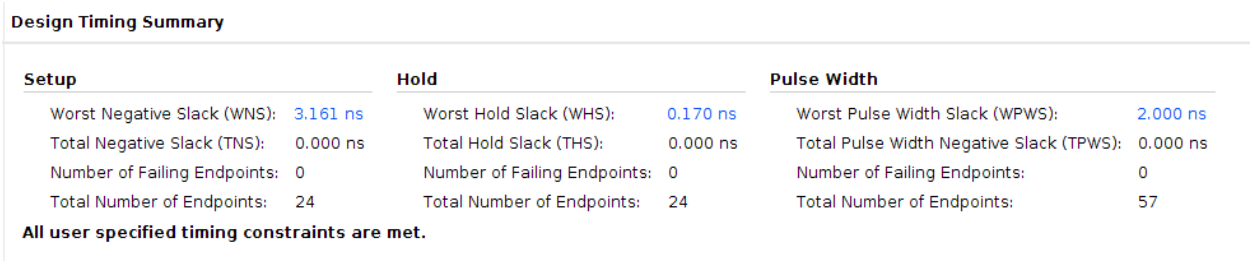




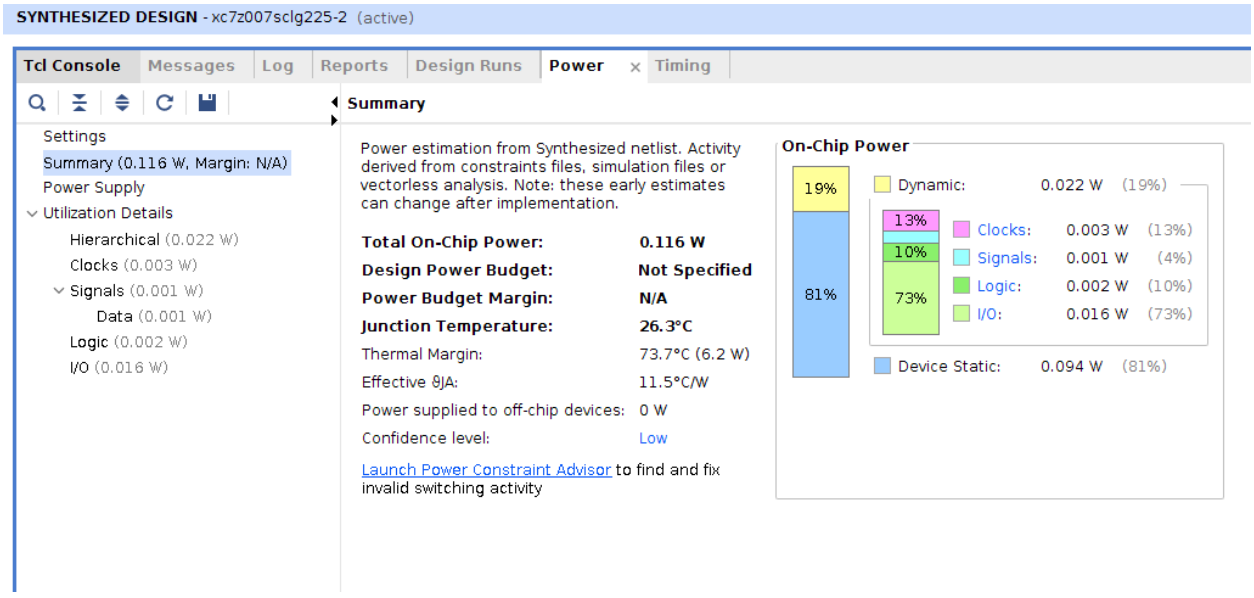
2.1.4.Resource Report



2.1.5.Timing Report



2.1.6.Power Report



2.1.7.How many of parallel *MulandAddTrees* can be implemented in this FPGA (Provide resource utilization reports with parallel *MulandAddTres*)?

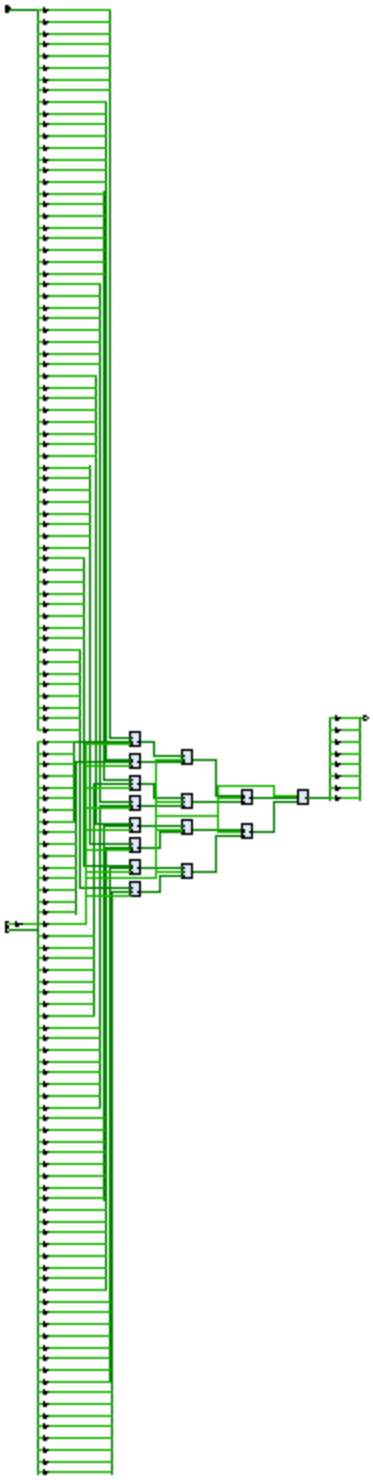
For this design, the Bonded IOB is out of range since I simulate the data feed from input IO bus. However, if the data is stored in memory and we don't use any IO bus. Then, for parallel MulanAddTrees, they can share one BUFGCTRL for clock buffer, thus LUTs and Registers become the limitation. For LUTs, 14400/160=90; for Registers, 28800/56=514.

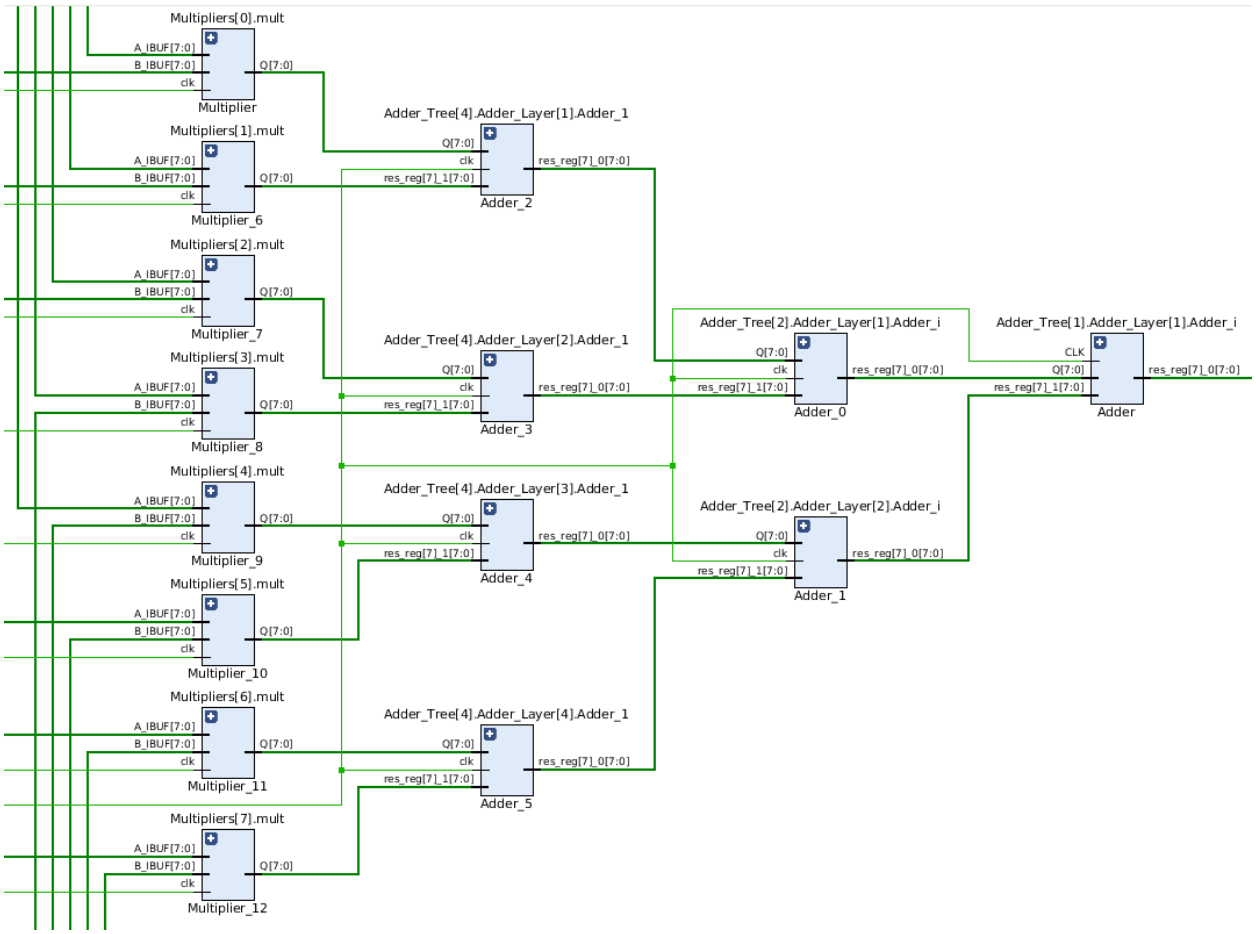
Therefore, the result is at most 90 parallel MulandAddTrees can be implemented.

2.2. 8 X 8 Matrices

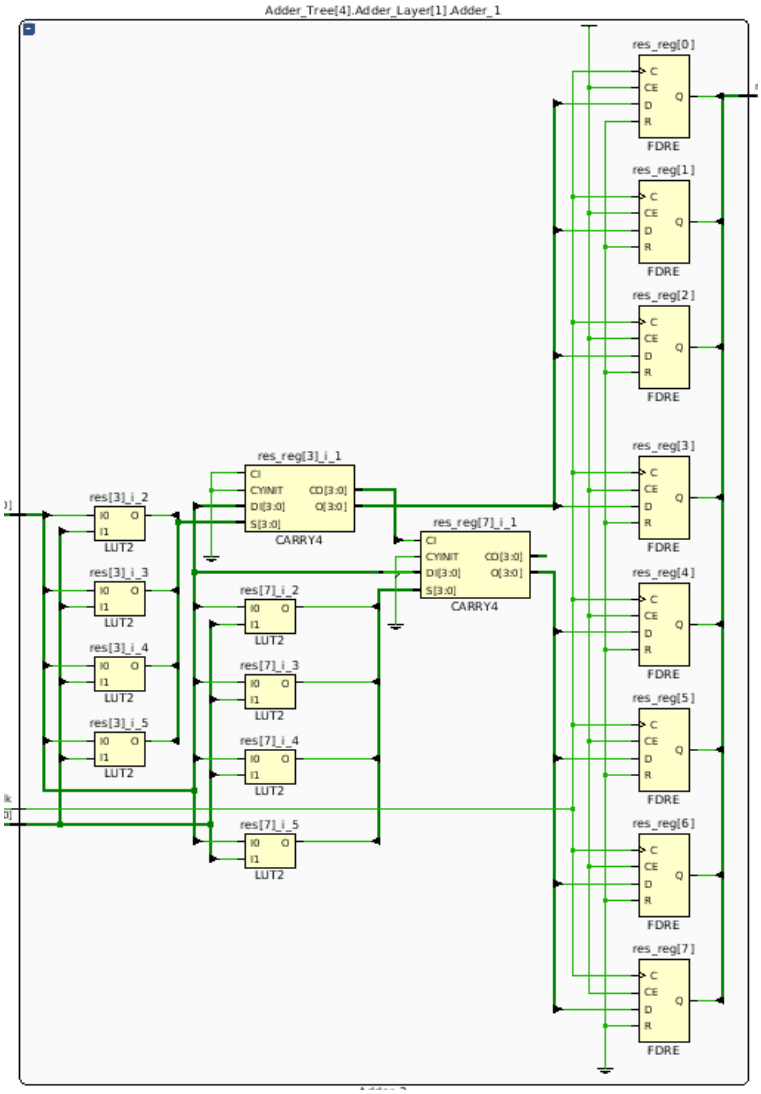
2.2.1.Synthesis

2.2.1.1. MulandAddTree

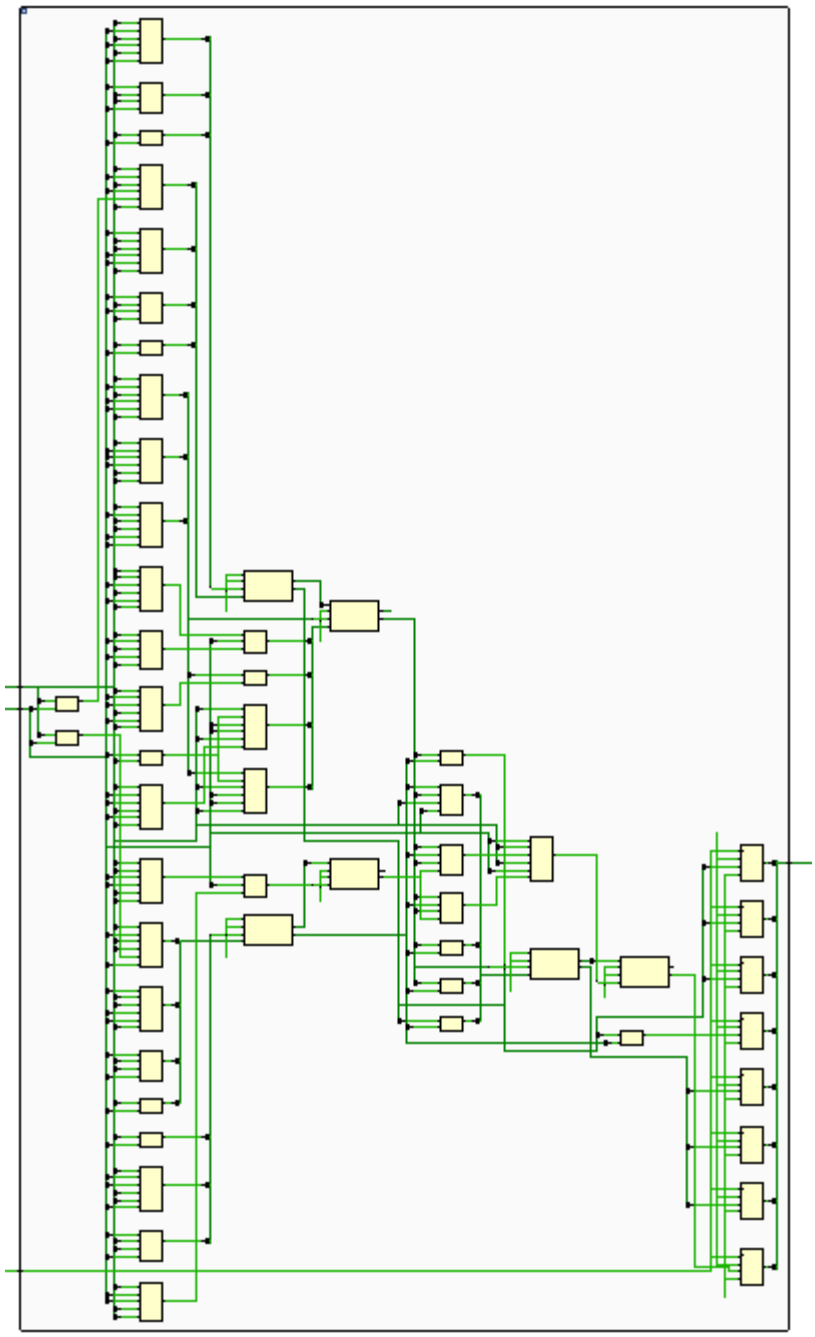


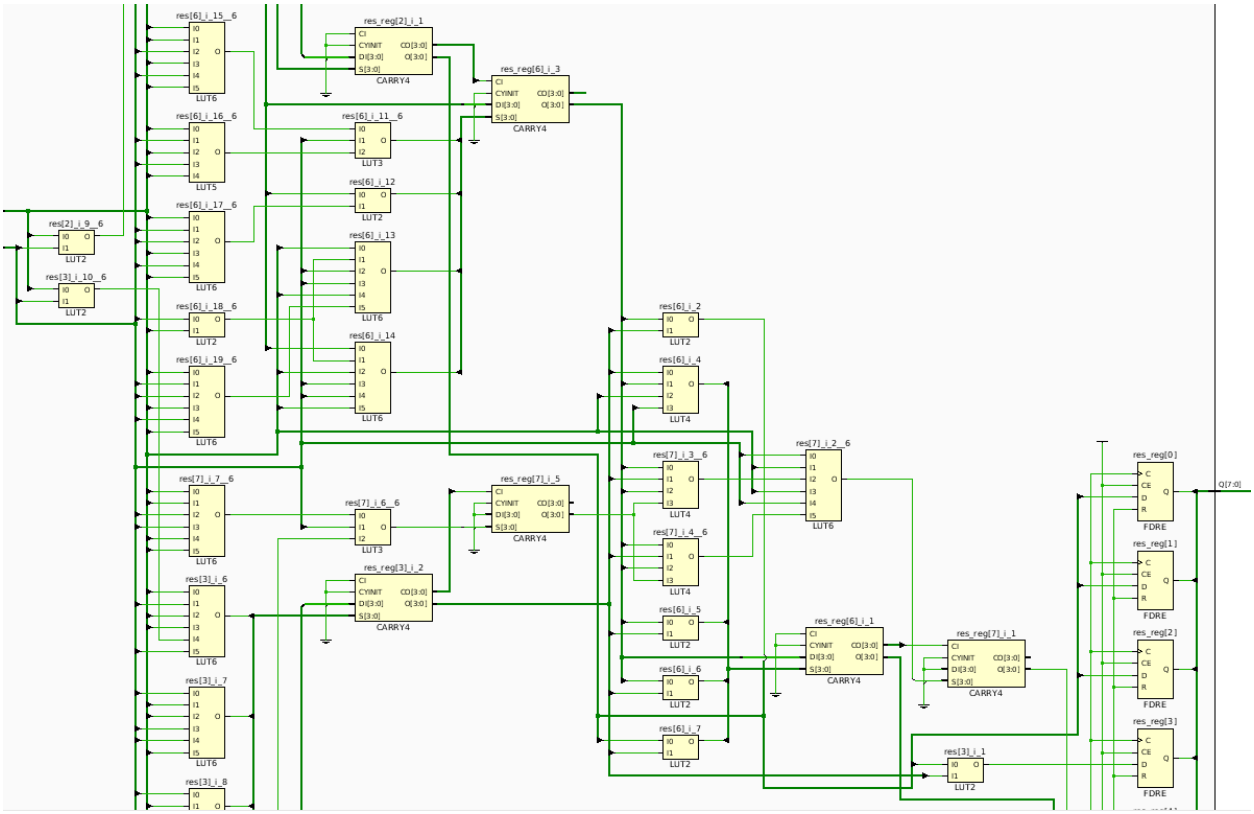

Multipliers[0].mult
A_IBUF[7:0]
B_IBUF[7:0]
clk
Q[7:0]
Multiplier
Multipliers[1].mult
Multiplier_6
Multipliers[2].mult
Multiplier_7
Multipliers[3].mult
Multiplier_8
Multipliers[4].mult
Multiplier_9
Multipliers[5].mult
Multiplier_10
Multipliers[6].mult
Multiplier_11
Multipliers[7].mult
Multiplier_12
Adder_Tree[4].Adder_Layer[1].Adder_1
res_reg[7]_1[7:0]
res_reg[7]_0[7:0]
Adder_2
Adder_Tree[4].Adder_Layer[2].Adder_1
Adder_3
Adder_Tree[4].Adder_Layer[3].Adder_1
Adder_4
Adder_Tree[4].Adder_Layer[4].Adder_1
Adder_5
Adder_Tree[2].Adder_Layer[1].Adder_i
Adder_0
Adder_Tree[2].Adder_Layer[2].Adder_i
Adder_1
Adder_Tree[1].Adder_Layer[1].Adder_i
CLK
Adder

2.2.1.2. Adder



2.2.1.3. Multiplier





2.2.2.Resource Report

SYNTHESIZED DESIGN - xc7z007sclg225-2 (active)

Tcl Console | Messages | Log | Reports | Design Runs | Power | Timing | **Utilization**

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (2%)
    - LUT as Logic (2%)
  - Slice Registers (1%)
    - Register as Flip Flop (1%)
- Memory
- DSP
- IO and GT Specific
  - Bonded IOB (>100%)
- Clocking
  - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes
- Instantiated Netlists

Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
MulandAddTree	328	120	137	1
Adder_Tree[1].Adder_Layer[1].Adder_i (Adder)	8	8	0	0
Adder_Tree[2].Adder_Layer[1].Adder_i (Adder_0)	8	8	0	0
Adder_Tree[2].Adder_Layer[2].Adder_i (Adder_1)	8	8	0	0
Adder_Tree[4].Adder_Layer[1].Adder_1 (Adder_2)	8	8	0	0
Adder_Tree[4].Adder_Layer[2].Adder_1 (Adder_3)	8	8	0	0
Adder_Tree[4].Adder_Layer[3].Adder_1 (Adder_4)	8	8	0	0
Adder_Tree[4].Adder_Layer[4].Adder_1 (Adder_5)	8	8	0	0
Multipliers[0].mult (Multiplier)	34	8	0	0
Multipliers[1].mult (Multiplier_6)	34	8	0	0
Multipliers[2].mult (Multiplier_7)	34	8	0	0
Multipliers[3].mult (Multiplier_8)	34	8	0	0
Multipliers[4].mult (Multiplier_9)	34	8	0	0
Multipliers[5].mult (Multiplier_10)	34	8	0	0
Multipliers[6].mult (Multiplier_11)	34	8	0	0
Multipliers[7].mult (Multiplier_12)	34	8	0	0

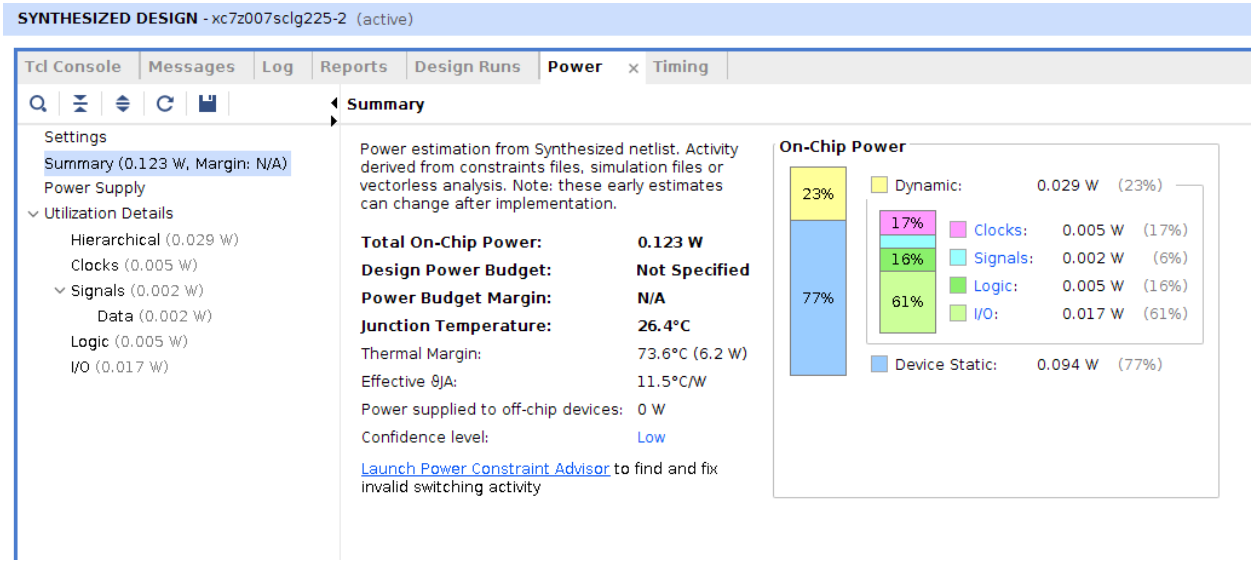
2.2.3.Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.161 ns	Worst Hold Slack (WHS):	0.170 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	56	Total Number of Endpoints:	56	Total Number of Endpoints:	121

All user specified timing constraints are met.

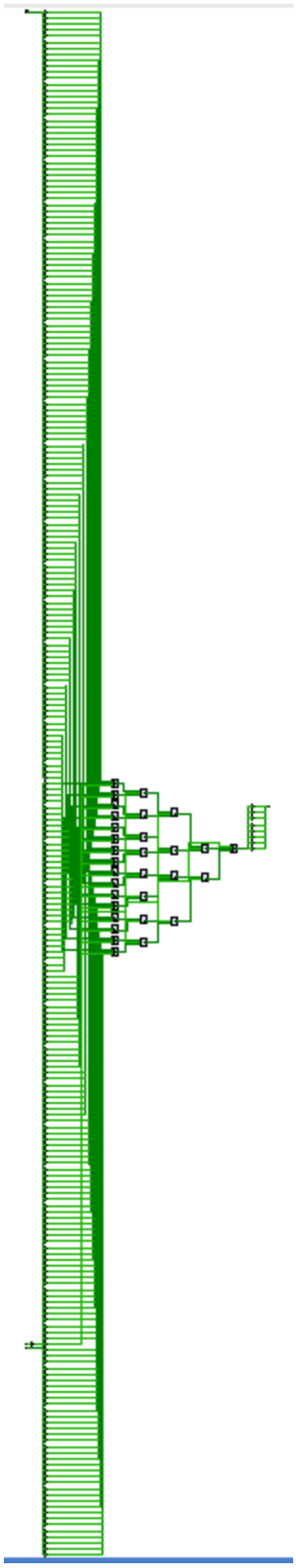
2.2.4.Power Report

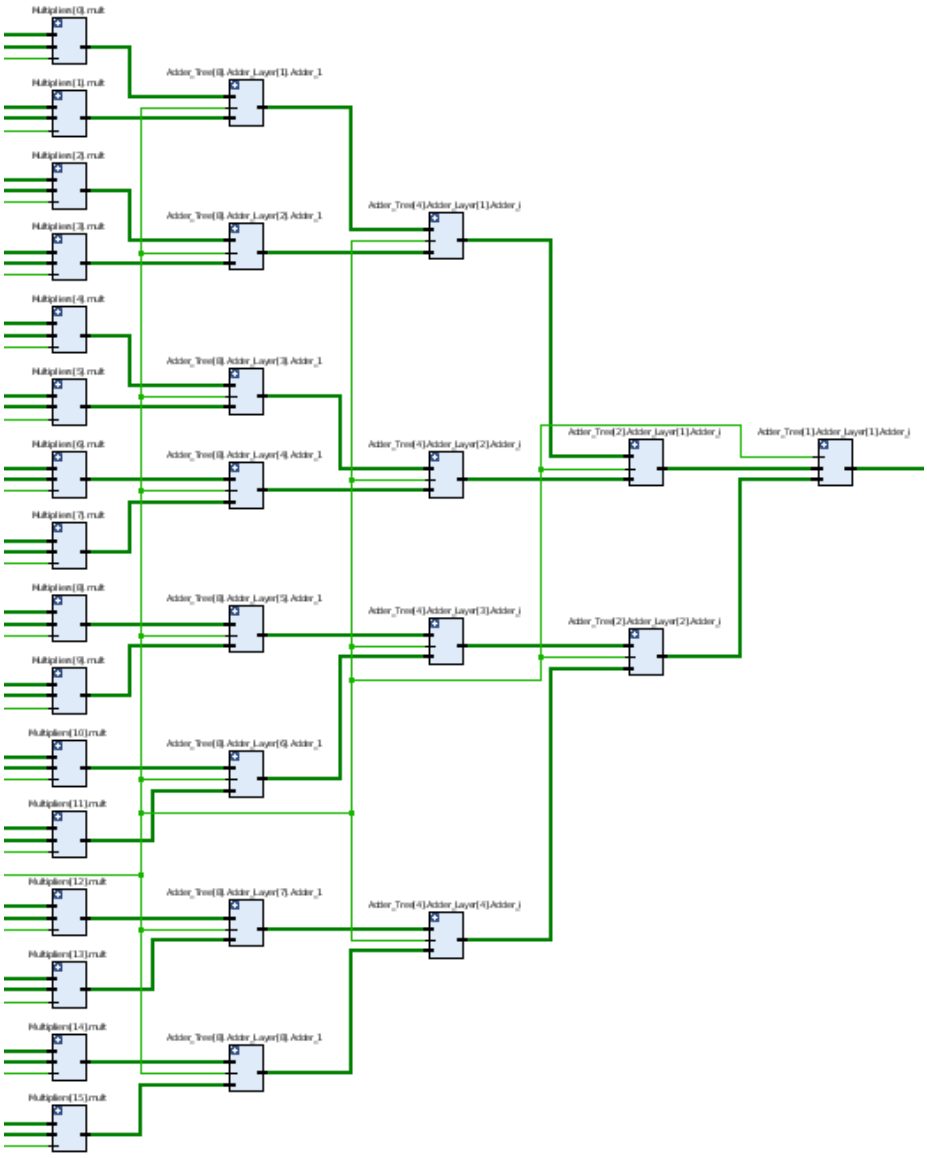


2.3. 16 X 16 Matrices

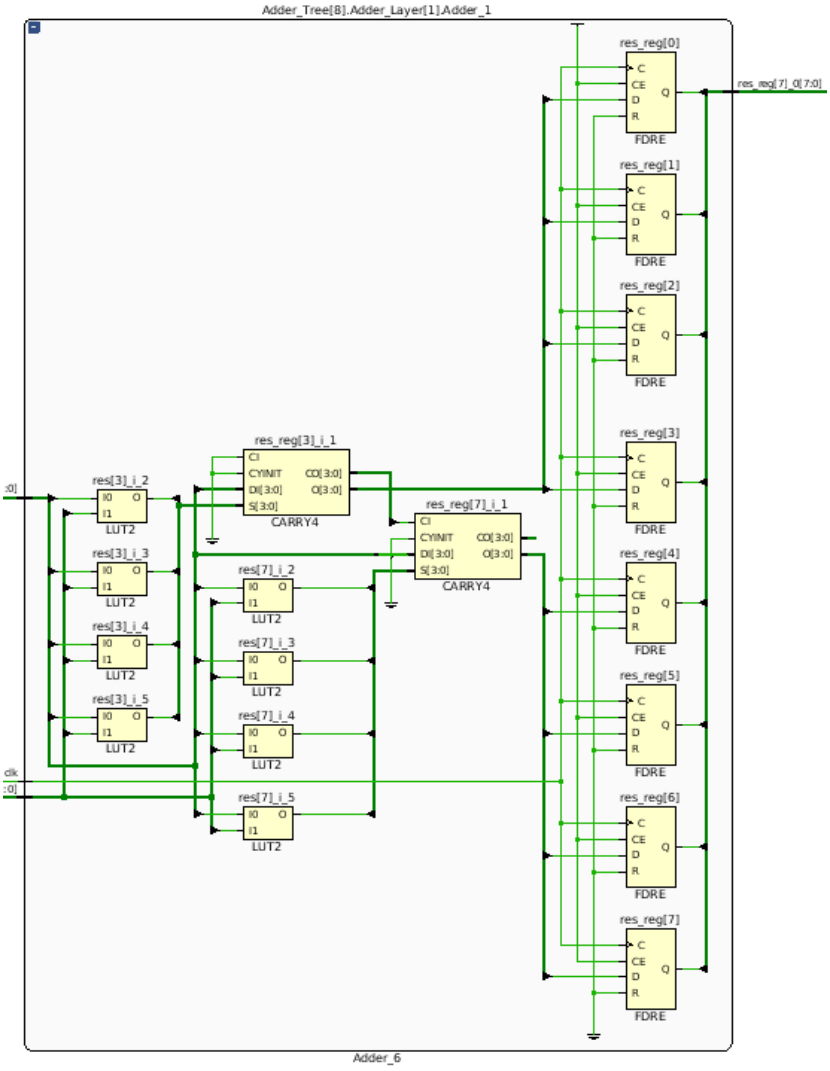
2.3.1.Synthesis

2.3.1.1. MulandAddTree

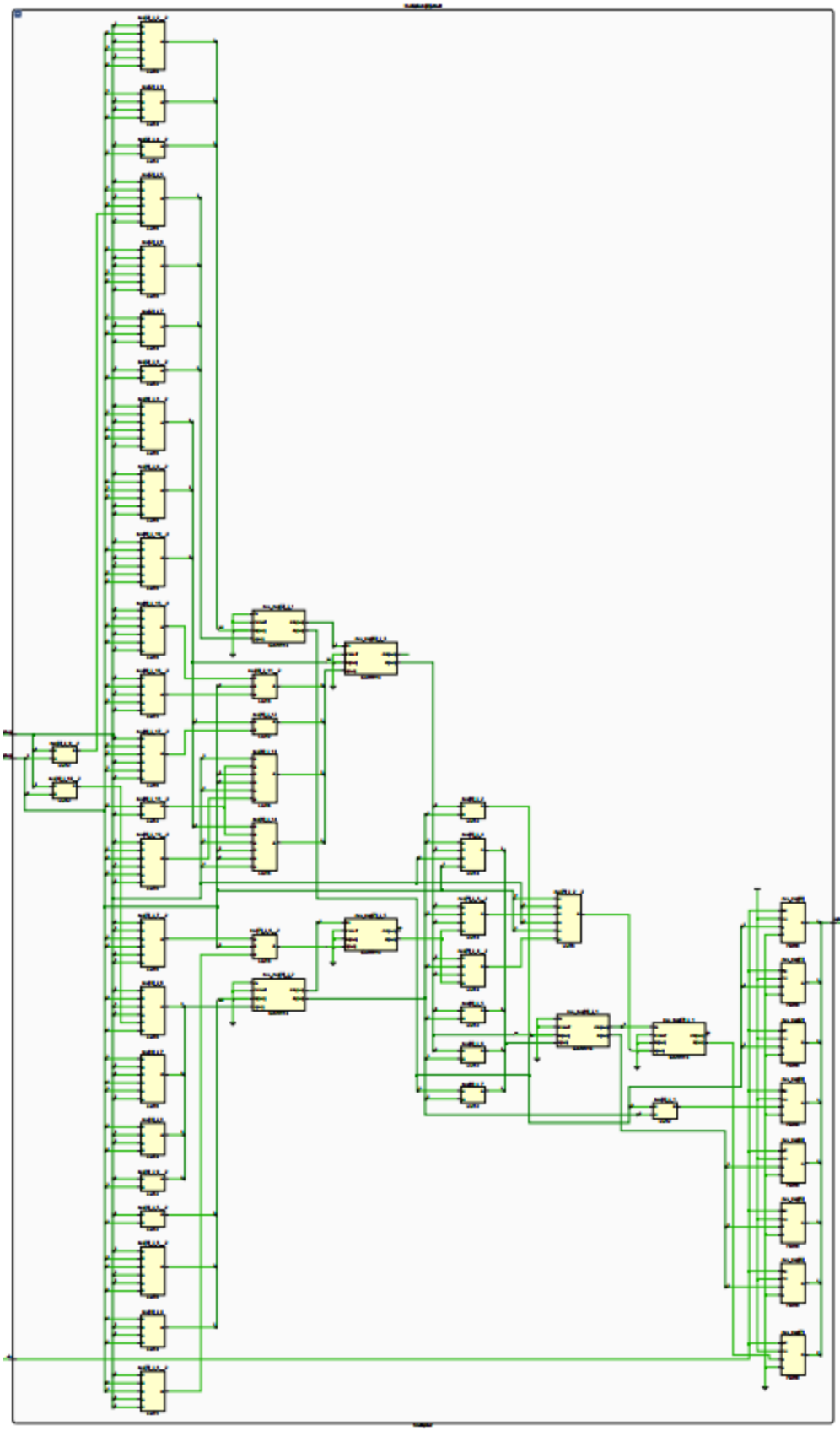




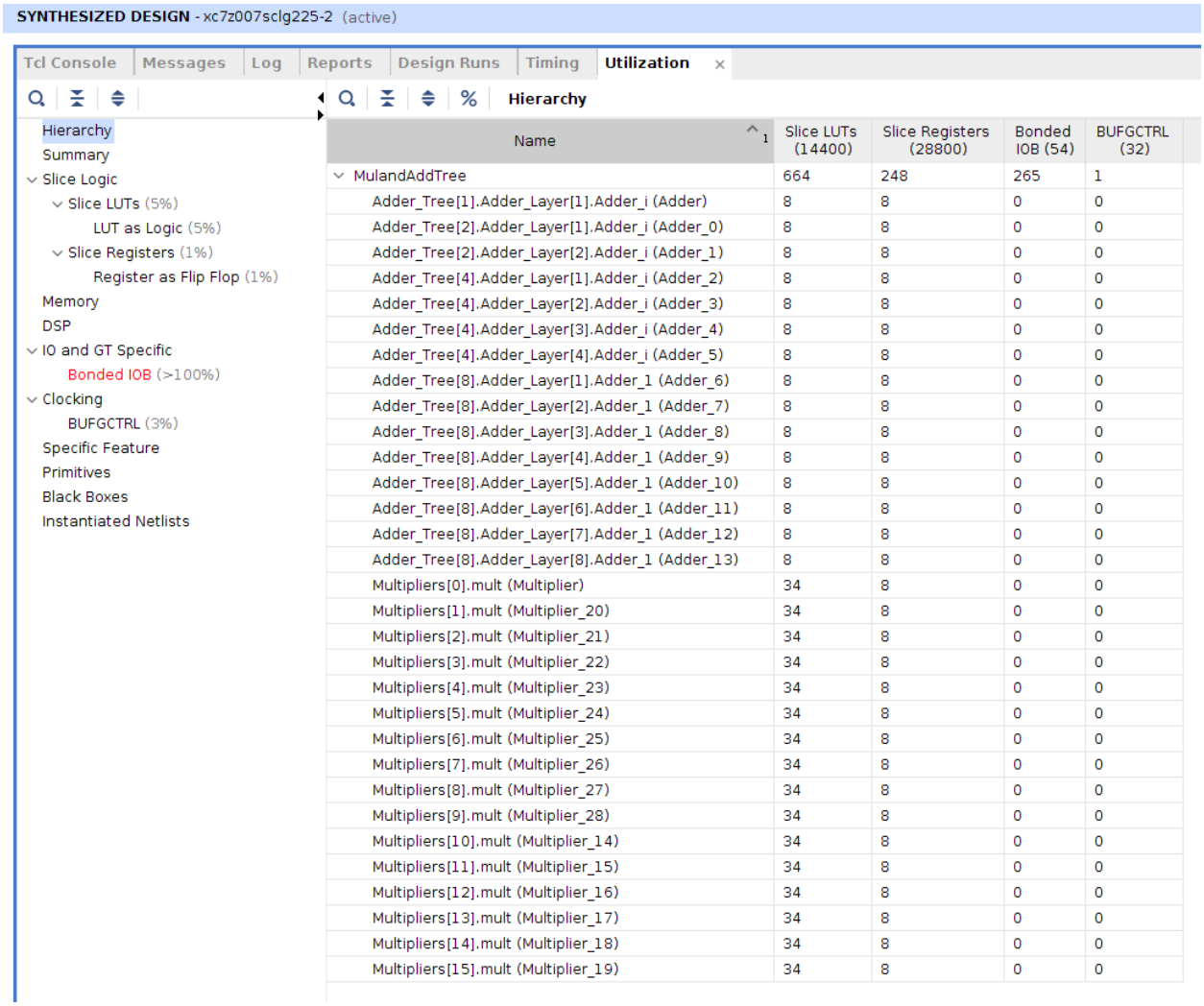
2.3.1.2. Adder



2.3.1.3. Multiplier



2.3.2.Resource Report



Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
MulandAddTree	664	248	265	1
Adder_Tree[1].Adder_Layer[1].Adder_i (Adder)	8	8	0	0
Adder_Tree[2].Adder_Layer[1].Adder_i (Adder_0)	8	8	0	0
Adder_Tree[2].Adder_Layer[2].Adder_i (Adder_1)	8	8	0	0
Adder_Tree[4].Adder_Layer[1].Adder_i (Adder_2)	8	8	0	0
Adder_Tree[4].Adder_Layer[2].Adder_i (Adder_3)	8	8	0	0
Adder_Tree[4].Adder_Layer[3].Adder_i (Adder_4)	8	8	0	0
Adder_Tree[4].Adder_Layer[4].Adder_i (Adder_5)	8	8	0	0
Adder_Tree[8].Adder_Layer[1].Adder_1 (Adder_6)	8	8	0	0
Adder_Tree[8].Adder_Layer[2].Adder_1 (Adder_7)	8	8	0	0
Adder_Tree[8].Adder_Layer[3].Adder_1 (Adder_8)	8	8	0	0
Adder_Tree[8].Adder_Layer[4].Adder_1 (Adder_9)	8	8	0	0
Adder_Tree[8].Adder_Layer[5].Adder_1 (Adder_10)	8	8	0	0
Adder_Tree[8].Adder_Layer[6].Adder_1 (Adder_11)	8	8	0	0
Adder_Tree[8].Adder_Layer[7].Adder_1 (Adder_12)	8	8	0	0
Adder_Tree[8].Adder_Layer[8].Adder_1 (Adder_13)	8	8	0	0
Multipliers[0].mult (Multiplier)	34	8	0	0
Multipliers[1].mult (Multiplier_20)	34	8	0	0
Multipliers[2].mult (Multiplier_21)	34	8	0	0
Multipliers[3].mult (Multiplier_22)	34	8	0	0
Multipliers[4].mult (Multiplier_23)	34	8	0	0
Multipliers[5].mult (Multiplier_24)	34	8	0	0
Multipliers[6].mult (Multiplier_25)	34	8	0	0
Multipliers[7].mult (Multiplier_26)	34	8	0	0
Multipliers[8].mult (Multiplier_27)	34	8	0	0
Multipliers[9].mult (Multiplier_28)	34	8	0	0
Multipliers[10].mult (Multiplier_14)	34	8	0	0
Multipliers[11].mult (Multiplier_15)	34	8	0	0
Multipliers[12].mult (Multiplier_16)	34	8	0	0
Multipliers[13].mult (Multiplier_17)	34	8	0	0
Multipliers[14].mult (Multiplier_18)	34	8	0	0
Multipliers[15].mult (Multiplier_19)	34	8	0	0

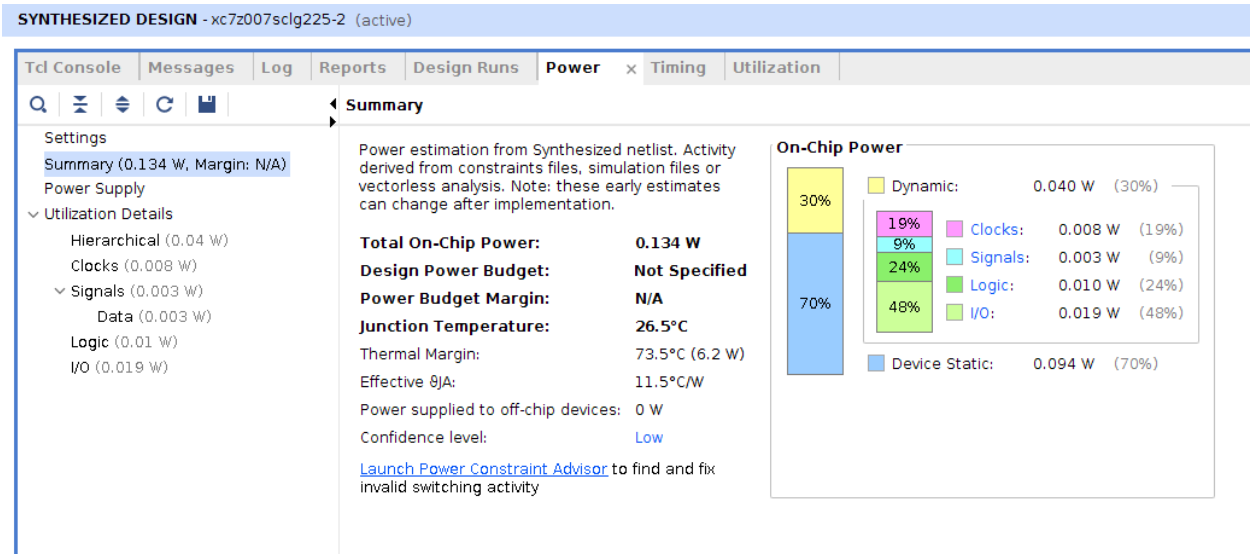
2.3.3.Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.161 ns	Worst Hold Slack (WHS):	0.170 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	120	Total Number of Endpoints:	120	Total Number of Endpoints:	249

All user specified timing constraints are met.

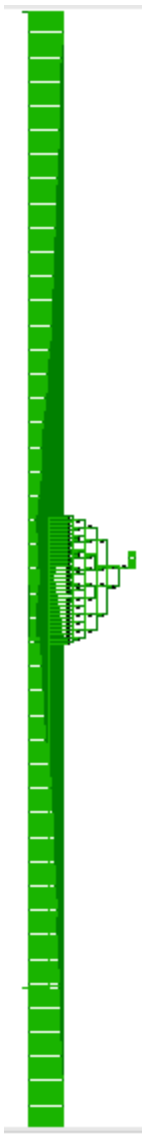
2.3.4.Power Report

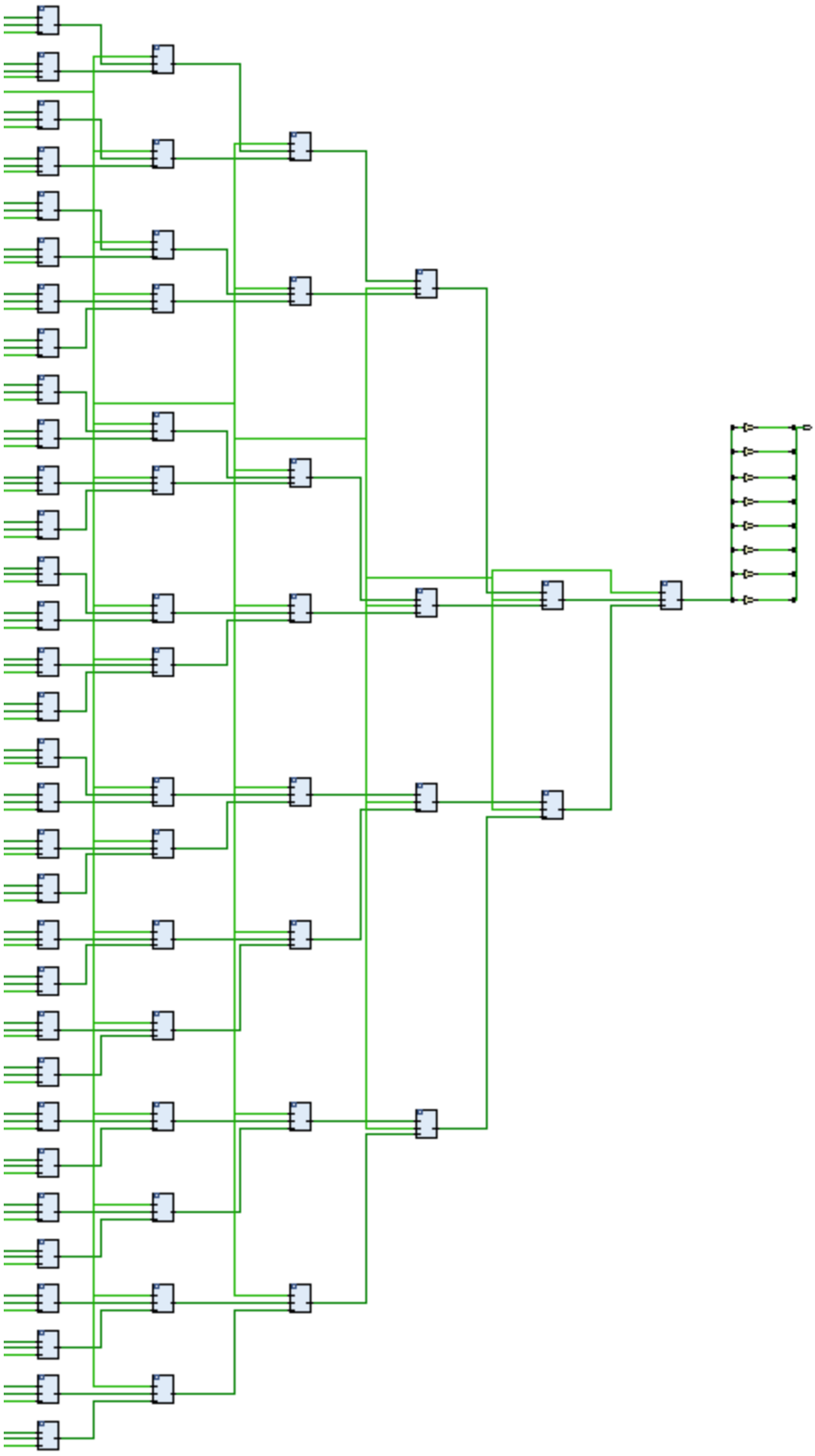


2.4. 32 X 32 Matrices

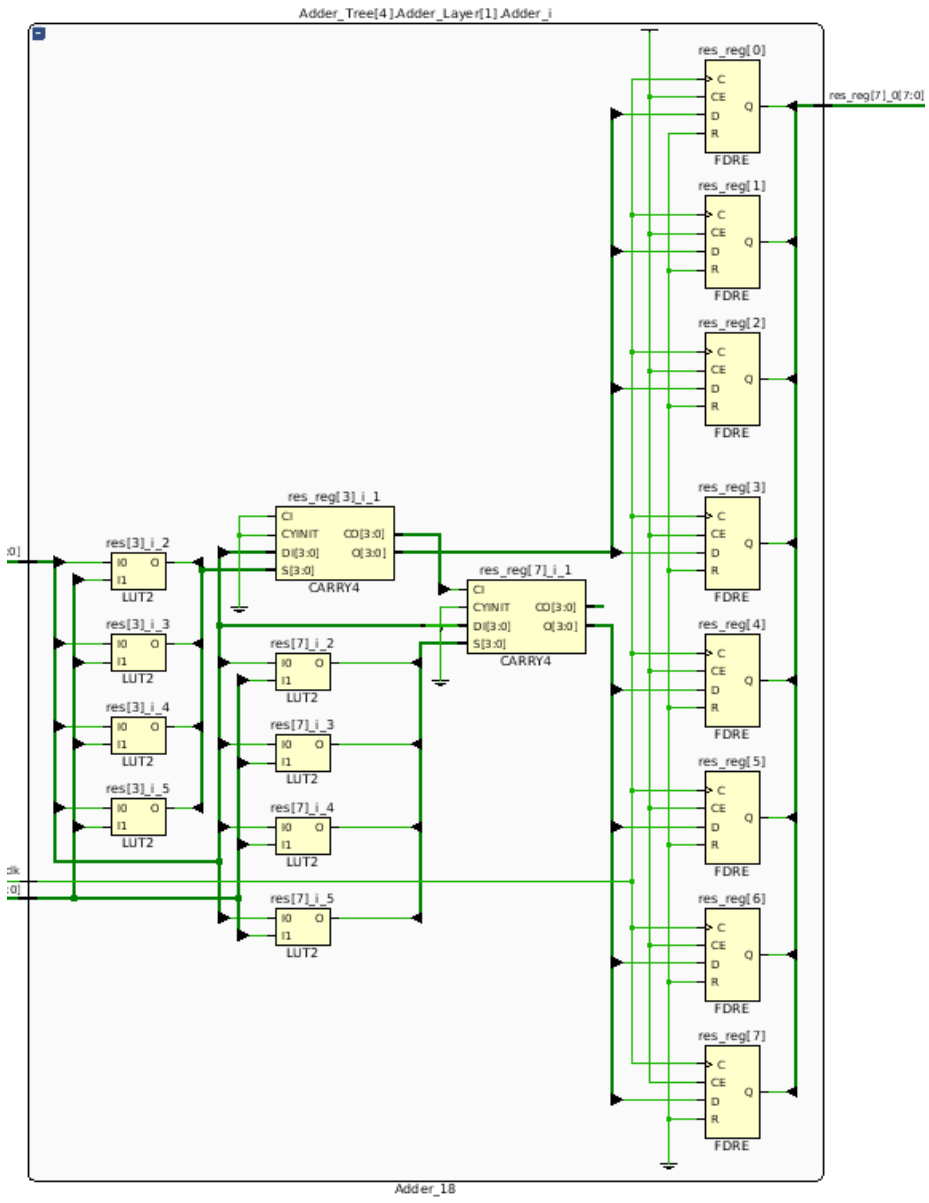
2.4.1.Synthesis

2.4.1.1. MulandAddTree

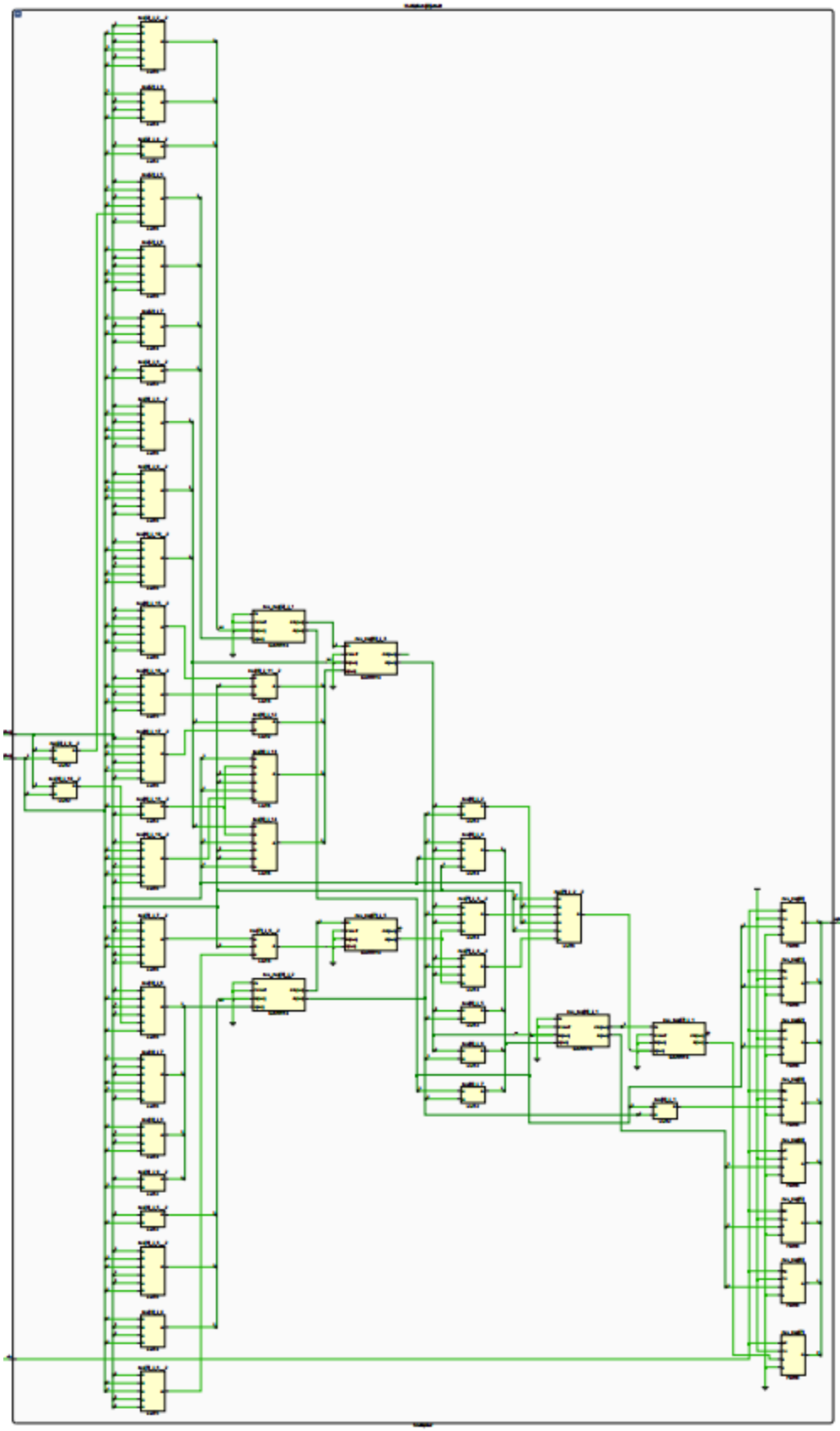




2.4.1.2. Adder



2.4.1.3. Multiplier



2.4.2.Resource Report

Utilization

Hierarchy
Summary
Slice Logic
Slice LUTs (9%)
LUT as Logic (9%)
Slice Registers (2%)
Register as Flip Flop (2%)
Memory
DSP
IO and GT Specific
Bonded IOB (>100%)
Clocking
BUFGCTRL (3%)
Specific Feature
Primitives
Black Boxes
Instantiated Netlists

Hierarchy

Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
MulandAddTree	1336	504	521	1
Adder_Tree[1].Adder_Layer[1].Adder_i (Adder_15)	8	8	0	0
Adder_Tree[2].Adder_Layer[1].Adder_i (Adder_16)	8	8	0	0
Adder_Tree[2].Adder_Layer[2].Adder_i (Adder_17)	8	8	0	0
Adder_Tree[4].Adder_Layer[1].Adder_i (Adder_18)	8	8	0	0
Adder_Tree[4].Adder_Layer[2].Adder_i (Adder_19)	8	8	0	0
Adder_Tree[4].Adder_Layer[3].Adder_i (Adder_20)	8	8	0	0
Adder_Tree[4].Adder_Layer[4].Adder_i (Adder_21)	8	8	0	0
Adder_Tree[8].Adder_Layer[1].Adder_i (Adder_22)	8	8	0	0
Adder_Tree[8].Adder_Layer[2].Adder_i (Adder_23)	8	8	0	0
Adder_Tree[8].Adder_Layer[3].Adder_i (Adder_24)	8	8	0	0
Adder_Tree[8].Adder_Layer[4].Adder_i (Adder_25)	8	8	0	0
Adder_Tree[8].Adder_Layer[5].Adder_i (Adder_26)	8	8	0	0
Adder_Tree[8].Adder_Layer[6].Adder_i (Adder_27)	8	8	0	0
Adder_Tree[8].Adder_Layer[7].Adder_i (Adder_28)	8	8	0	0
Adder_Tree[8].Adder_Layer[8].Adder_i (Adder_29)	8	8	0	0
Adder_Tree[16].Adder_Layer[1].Adder_1 (Adder_6)	8	8	0	0
Adder_Tree[16].Adder_Layer[2].Adder_1 (Adder_7)	8	8	0	0
Adder_Tree[16].Adder_Layer[3].Adder_1 (Adder_8)	8	8	0	0
Adder_Tree[16].Adder_Layer[4].Adder_1 (Adder_9)	8	8	0	0
Adder_Tree[16].Adder_Layer[5].Adder_1 (Adder_10)	8	8	0	0
Adder_Tree[16].Adder_Layer[6].Adder_1 (Adder_11)	8	8	0	0
Adder_Tree[16].Adder_Layer[7].Adder_1 (Adder_12)	8	8	0	0
Adder_Tree[16].Adder_Layer[8].Adder_1 (Adder_13)	8	8	0	0
Adder_Tree[16].Adder_Layer[9].Adder_1 (Adder_14)	8	8	0	0
Adder_Tree[16].Adder_Layer[10].Adder_1 (Adder)	8	8	0	0
Adder_Tree[16].Adder_Layer[11].Adder_1 (Adder_0)	8	8	0	0
Adder_Tree[16].Adder_Layer[12].Adder_1 (Adder_1)	8	8	0	0
Adder_Tree[16].Adder_Layer[13].Adder_1 (Adder_2)	8	8	0	0
Adder_Tree[16].Adder_Layer[14].Adder_1 (Adder_3)	8	8	0	0
Adder_Tree[16].Adder_Layer[15].Adder_1 (Adder_4)	8	8	0	0
Adder_Tree[16].Adder_Layer[16].Adder_1 (Adder_5)	8	8	0	0
Multipliers[0].mult (Multiplier)	34	8	0	0
Multipliers[1].mult (Multiplier_40)	34	8	0	0

Utilization

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (9%)
    - LUT as Logic (9%)
  - Slice Registers (2%)
    - Register as Flip Flop (2%)
- Memory
- DSP
- IO and GT Specific
  - Bonded IOB (>100%)
- Clocking
  - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes
- Instantiated Netlists

Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
Adder_Tree[16].Adder_Layer[15].Adder_1 (Adder_4)	8	8	0	0
Adder_Tree[16].Adder_Layer[16].Adder_1 (Adder_5)	8	8	0	0
Multipliers[0].mult (Multiplier)	34	8	0	0
Multipliers[1].mult (Multiplier_40)	34	8	0	0
Multipliers[2].mult (Multiplier_51)	34	8	0	0
Multipliers[3].mult (Multiplier_54)	34	8	0	0
Multipliers[4].mult (Multiplier_55)	34	8	0	0
Multipliers[5].mult (Multiplier_56)	34	8	0	0
Multipliers[6].mult (Multiplier_57)	34	8	0	0
Multipliers[7].mult (Multiplier_58)	34	8	0	0
Multipliers[8].mult (Multiplier_59)	34	8	0	0
Multipliers[9].mult (Multiplier_60)	34	8	0	0
Multipliers[10].mult (Multiplier_30)	34	8	0	0
Multipliers[11].mult (Multiplier_31)	34	8	0	0
Multipliers[12].mult (Multiplier_32)	34	8	0	0
Multipliers[13].mult (Multiplier_33)	34	8	0	0
Multipliers[14].mult (Multiplier_34)	34	8	0	0
Multipliers[15].mult (Multiplier_35)	34	8	0	0
Multipliers[16].mult (Multiplier_36)	34	8	0	0
Multipliers[17].mult (Multiplier_37)	34	8	0	0
Multipliers[18].mult (Multiplier_38)	34	8	0	0
Multipliers[19].mult (Multiplier_39)	34	8	0	0
Multipliers[20].mult (Multiplier_41)	34	8	0	0
Multipliers[21].mult (Multiplier_42)	34	8	0	0
Multipliers[22].mult (Multiplier_43)	34	8	0	0
Multipliers[23].mult (Multiplier_44)	34	8	0	0
Multipliers[24].mult (Multiplier_45)	34	8	0	0
Multipliers[25].mult (Multiplier_46)	34	8	0	0
Multipliers[26].mult (Multiplier_47)	34	8	0	0
Multipliers[27].mult (Multiplier_48)	34	8	0	0
Multipliers[28].mult (Multiplier_49)	34	8	0	0
Multipliers[29].mult (Multiplier_50)	34	8	0	0
Multipliers[30].mult (Multiplier_52)	34	8	0	0
Multipliers[31].mult (Multiplier_53)	34	8	0	0

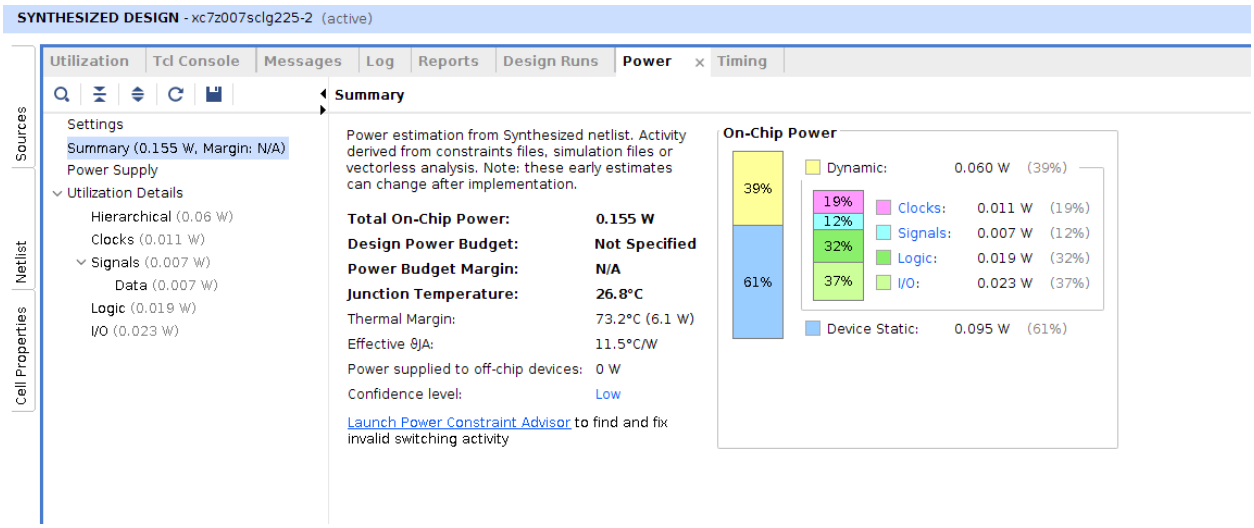
2.4.3.Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.161 ns	Worst Hold Slack (WHS):	0.170 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	248	Total Number of Endpoints:	248	Total Number of Endpoints:	505

All user specified timing constraints are met.

2.4.4.Power Report


SYNTHESIZED DESIGN - xc7z007sclg225-2 (active)
Sources
Netlist
Cell Properties
Utilization
Tcl Console
Messages
Log
Reports
Design Runs
Power
Timing
Settings
Summary (0.155 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.06 W)
Clocks (0.011 W)
Signals (0.007 W)
Data (0.007 W)
Logic (0.019 W)
I/O (0.023 W)
Summary
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.
Total On-Chip Power: 0.155 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 26.8°C
Thermal Margin: 73.2°C (6.1 W)
Effective θJA: 11.5°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
39%
61%
Dynamic: 0.060 W (39%)
19%
12%
32%
37%
Clocks: 0.011 W (19%)
Signals: 0.007 W (12%)
Logic: 0.019 W (32%)
I/O: 0.023 W (37%)
Device Static: 0.095 W (61%)