



RH850/D1x Evaluation Boards

Evaluation Boards for
the D1x Dashboard MCU Series

Main board manual

D1x Mango Main Board (Y-RH850-D1X-MB-T1-V1)

**Please use this manual together with the respective
adapter board manual.**

Preliminary Hardware User's Manual Main Board

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1 Introduction

This document is the Manual for the D1x Evaluation Boards, called D1x "Mango" boards. This includes the D1x Mango Main Board (Y-RH850-D1X-MB-T1-V1) and the Adapter Boards. For a list of available adapter boards, please see Table 1-1 below.

The RH850/D1x Application Board serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/D1x microcontrollers and provides a base for application software development.

This document describes the functionality provided by the application boards and guides the user through their operation. For details regarding the operation of the microcontroller, please refer to the specific RH850/D1x User's Manual. In case of problems with hardware or software of the board please contact us by mail (device_support.d1x-eu@lm.renesas.com).

1.1 Main and Adapter Board Concept

A working D1x Mango Development / Evaluation Environment always consists of the Mango Main Board and one D1x Adapter Board. Thus, the Main Board must be combined with one of several Adapter Boards. Each of the Adapter Board is dedicated to one D1x MCU derivative. The adapter board provides at least the connection to the device as well as the connection to the main board. There may also be certain device-specific features that were placed on the Adapter Board instead of the Main Board.

D1x Main Board is the same for all devices (D1L1 to D1M2H)

- Reduce maintenance effort vs. Save hardware development cost

Different D1x Adapter Boards

- For D1x devices package variants
- For population variants with device socket (on device footprint)
- For population variants with IECUBE POD (on device footprint)

The available boards are listed in Table 1-1 and Table 1-2.

Table 1-1: D1x "Mango" Main Board

Board Name	Order Code	Board Label
RH850/D1x main board	Y-RH850-D1X-MB-T1-V1	SBEV-RH850-MAIN

Table 1-2: D1x "Mango" Adapter Boards

Board Name	Order Code	Board Label
RH850/D1M2H with direct Device assembly	Y-RH850-D1M2H-PB-DEV-V1	SBEV-RH850-D1M2H
RH850/D1M2H with TET BS socket	Y-RH850-D1M2H-PB-TET-V1	SBEV-RH850-D1M2H
RH850/D1M2H with TET socket (w/o Mount adapter)	Y-RH850-D1M2H-PB-TET-V2	SBEV-RH850-D1M2H
RH850/D1M1H with direct Device assembly	Y-RH850-D1M1H-PB-DEV-V1	SBEV-RH850-D1M1H
RH850/D1M1H with TET socket	Y-RH850-D1M1H-PB-TET-V1	SBEV-RH850-D1M1H
RH850/D1L2H with TET LQFP176 socket	Y-RH850-D1L2H-PB-TET-V1	SBEV-RH850-D1L2H/D1M1
RH850/D1L2 with TET LQFP144 socket	Y-RH850-D1L2-PB-TET-V1	SBEV-RH850-D1L2

2 Board Overview

The figure below depicts one board set made of one D1x Mango Main Board and one D1x Mango Adapter Board. The functional blocks of the Mango Main Board are highlighted.

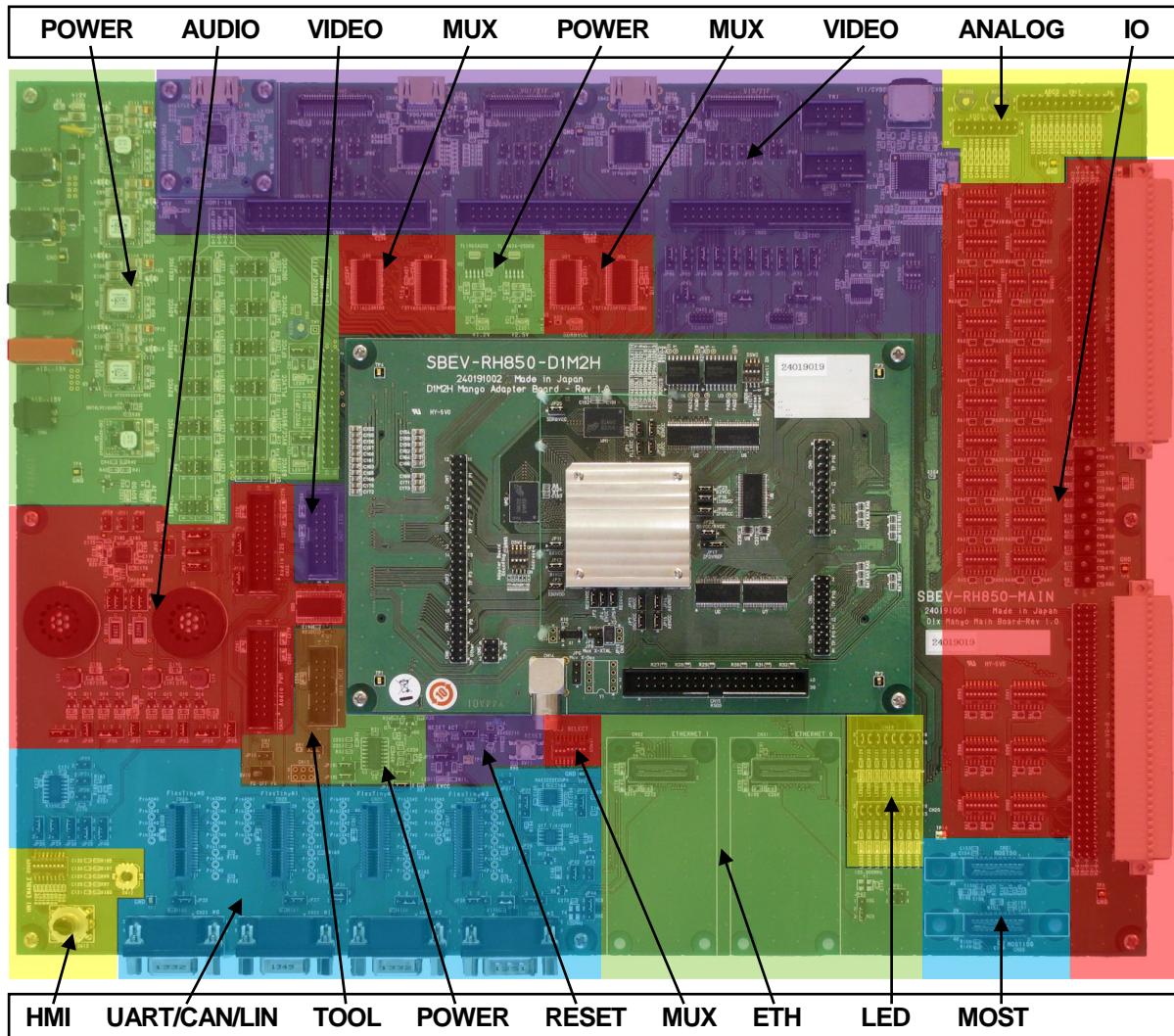


Figure 2-1: Photo of the main board with functional blocks highlighted

The following Figures are a schematic representation of the Image shown above.

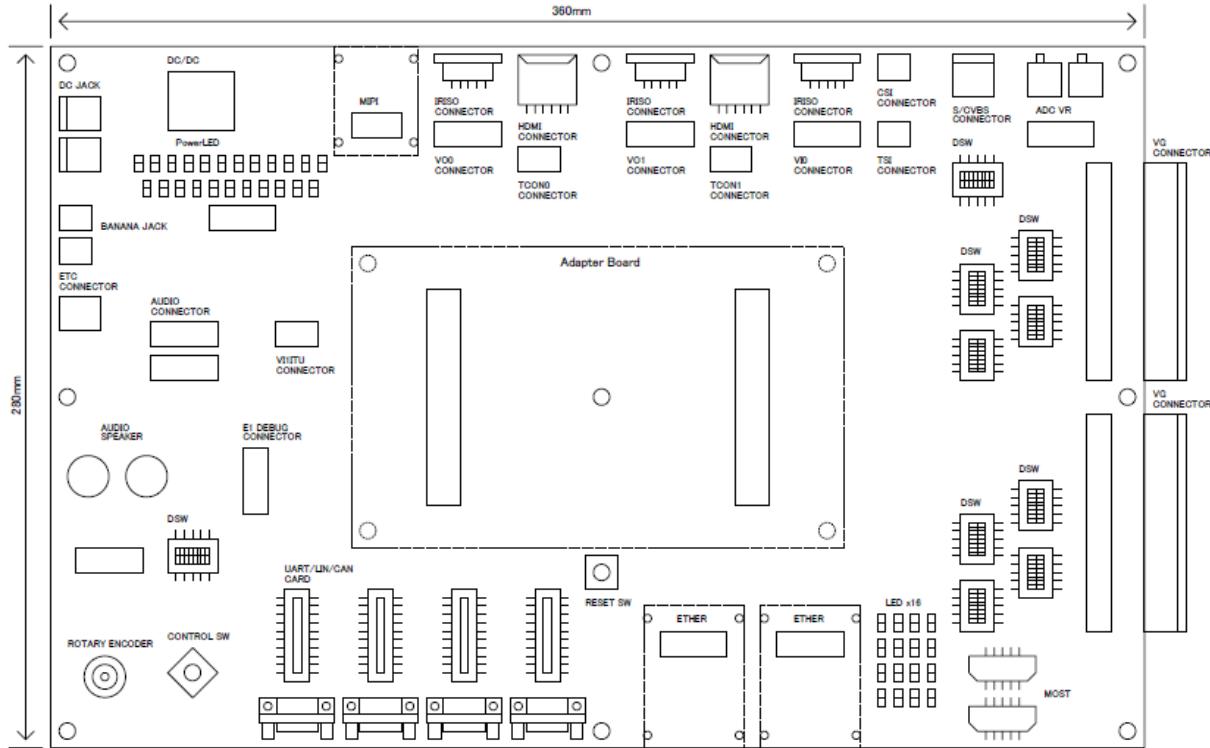


Figure 2-2: Main board

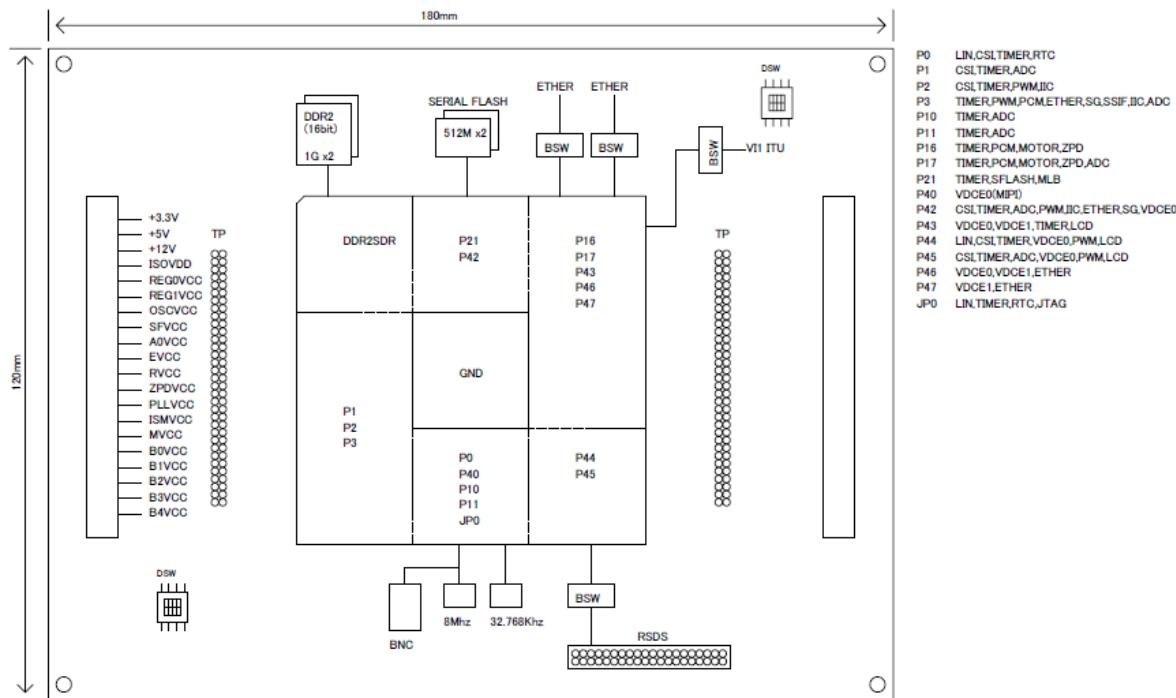


Figure 2-3: D1M2H adapter board

2.1 Main Board - Feature Overview

The D1x Mango Board tries to either make all features available directly on the board or to provide a connector for external evaluation of the features. The following features are covered by the Mango Board.

Feature	#	D1x Main Board
Power supply input connector (12V)		12V-15V input jack (banana jacks, ETC std. supply, barrel connector), reverse polarity protection, internal board supply ~6W + external output ~3W
Power supply external output connector (12V, 3W)		12V-15V output jack (barrel connector) ~3W
Power supply regulators 3.3VC / 5VC / 3.3V / 5V		Power supply groups with 3.3V / 5V constant and switchable voltages. Selectable for each port group of MCU by jumper. Jumpers to measure the current consumption of MCU only. Jumpers to select the supplies to be used for POWERGD signal generation.
Power supply connector		All power supply rails are available on one test connector. Quick check of correct power supply rails by measurement or status LED.
Debug I/F		RH850 series debug interface. (E1 debugger) Dedicated Pull-Up switches for the debug interface.
ADC input	2x	Potentiometer and R/C filter combination connectable to all ADC inputs
LEDs	16x	LEDs on low speed I/O pins
HMI area	1x	Buttons (up, down, left, right, ok) and Rotary Button
Audio HW	1x	1x H-bridge (for SG+PCMP), 1x Connector (external H-Bridge), 1x DAC (for I2S), 1x Connector (external I2S DAC), 1x Stereo Speaker
UART / LIN	4x	LIN/RS232 transceivers to be used with "FlexTiny card" PHY through special connection. LIN/RS232 are available on D-SUB connectors.
	1x	OnBoard LIN/RS232 Transceiver. Multiplexed on D-SUB connector.
CAN	3x	CAN transceivers to be used with "FlexTiny card" PHY through special connection. Multiplexed on D-SUB connectors.
	1x	OnBoard CAN Transceiver. Multiplexed on D-SUB connector.
MOST / MLB connector	1x	Each a MLB50 and a MLB150 connector that fits to SMSC development boards.
CSI Control connector	1x	CSI control connector for display initialization sequence.
Touch Screen Interface	1x	Touch Screen Interface for displays with resistive touch screen.
VG connectors	2x	All low speed I/O pins available on 96-pin VG-connectors for external connection of hardware.
2.54mm Header	2x	All low speed I/O pins available on 3*32-pin 2.54mm male header connectors
PU/PD by DIP switch		All low speed I/O pins have selectable Pull-Up and Pull-Down resistors of 22k Ohm. Selection is done manually by DIP switch.
Video Out: parallel 40pin	2x	Video output parallel on 40pin male header connector
Video Out: parallel Iriso	2x	Video output parallel on Iriso (ZIF) connector (in addition on this connector some I2C signals and power supply). Muxed between 40pin and Grafena.
Video Out: HDMI	2x	Video output on HDMI connector (Via conversion LSI). Muxed between parallel and HDMI.
Video Out: TCON	2x	All TCON signals available on one header (1.27mm) per video output
Video Input: Analog CVBS / S-Video	1x	Analog video input (S-Video/CVBS to ITU565 via conversion LSI)
Video Input: parallel 40pin	1x	Video input parallel on 40pin male header connector
Video Input: parallel Iriso	1x	Video input parallel on Iriso (ZIF) connector (in addition on this connector some I2C signals and power supply)
Video In: MIPI CSI-2	1x	Video input MIPI CSI-2 coming from HDMI connector (Via conversion LSI HDMI to MIPI CSI-2).
Ethernet PHY 100Mbit	1x	Ethernet AV: target board will be provided by 3 rd party Tessera. Two connector available to connect to two different port groups of MCU. Internally connects to the same instance.

2.2 Adapter Board - Feature Overview

The D1x Mango Adapter Board shall support the following features.

Feature	D1L1 Adapter	D1L2 Adapter	D1M1 Adapter	D1M1H Adapter	D1M2 Adapter	D1M2H Adapter
MCU*	D1L1	D1L1 or D1L2	D1L2H or D1M1			D1M2H
Device footprint Socket*	QFP100	QFP144	QFP176	BGA272	BGA376	BGA484
Test point area	Yes, all low-speed I/Os are routed to pin connectors					
Test points for high speed signals	Test points within high speed signal trace					
Serial NOR Flash	-	4bit, SDR 40MHz 1x S25FL512S (64MB)	8bit, DDR 80MHz 2x S25FL512S (128MB)			
SDRAM memory	-	-	-	32bit, 120MHz xxMB	-	-
SDRAM-DDR2 mem	-	-	-	-	16bit, 240MHz 32MB	32bit, 240MHz 32MB
SDRAM-DDR3 mem	-	-	-	-	-	-
USB 2.0	-	-	-	-	-	-
NAND Flash memory	-	-	-	-	-	-
Video IO	-	-	-	-	-	-
Power supply 1.2V (core voltages)	-	-	-	-	Yes, from main board	Yes, from main board
Power supply 1.5V/1.8V (DDR3/2 mem)	-	-	-	-	Yes, from main board	Yes, from main board
Power supplies 3.3V / 5V	Provided from main board					
Clock supply	1x 32k crystal, 1x 8MHz crystal					

* Population variants: MCU or socket / also used for IECUBE2 POD interconnection (on device footprint)

2.3 Interfaces and function blocks of the Mango Board

The following table lists the available interfaces and their position on the main / adapter board combination. The block diagram shown in Figure 2-4 below shows the interconnection of the blocks. Blue dotted lines show the parts that are located on the Adapter Board and red dotted lines highlight the parts that are placed on the Main Board.

Table 2-1: Function block list

Block	Function	Location
Audio	PCM-PWM or SG0 Audio output (speaker control with H-bridge) SSIF Audio output (speaker control with Audio DAC) PCM-PWM or SG0 Audio output (2x10 pin header) SSIF Audio output (2x10 pin header)	Main board
Video I/O	VOUT0 (LVTTL) Digital graphic output (HDIM connector) VOUT0 (LVTTL) Digital graphic output (40-pin pin header) VOUT0 (LVTTL) Digital graphic output (50-pin IRISO connector) Display control via CSI (10-pin pin header) Display control via TSI (10-pin pin header) VOUT1 (RSDS) Digital graphic output (HDIM connector) VOUT1 (LVTTL) Digital graphic output (LVTTL) (40-pin pin header) VOUT1 (LVTTL output) Digital graphic output (50-pin IRISO connector) VIN1(MIPI): Digital graphic input (HDMI) VIN1(LVTTL): Analog graphic input (CVBS)	Main board
Tool I/F	E1 emulator connector (14-pin) (debugger, Flash programming)	Main board
Reset	External reset switch	Main board
Power supply	Power supply 12V→1.2V, 1.8V, 2.5V, 3.3V, 5V Power supply sequence control by Power Supply Selection Matrix	Main board
Communication I/F	Ethernet AVB MOST50 (MOST50 44-pin connector) MOST150 (MOST150 44-pin connector) RLIN30-33 (FlexTiny 40-pin connector) RLIN30-33 (D-SUB9 connector) RLIN30 (on-board RS-232 and LIN driver circuit) RSCAN0-2 (FlexTiny 40-pin connector) RSCAN0-2 (D-SUB9) RSCAN0-2 (on-board CAN transceiver)	Tessera board Main board
I/O I/F	VG-Connector (2x 96pin Connectors) Pin-Header (2x Male 3x32pin Header) Pull-Up / Pull-Down DIP switches for GPIOs	Main board
User I/F	LEDs Pullup/down switch Rotary switch	Main board
MCU part	RH850D1x IC socket (The socket is individually specified for each Package of D1x Adapter Board)	Adapter board
Oscillator	Main OSC external crystal connection (8MHz) Sub OSC external crystal connection (32.768kHz)	Adapter board
External Memory	SDRAM DDR2 memory control Serial Flash Memory control	Adapter board

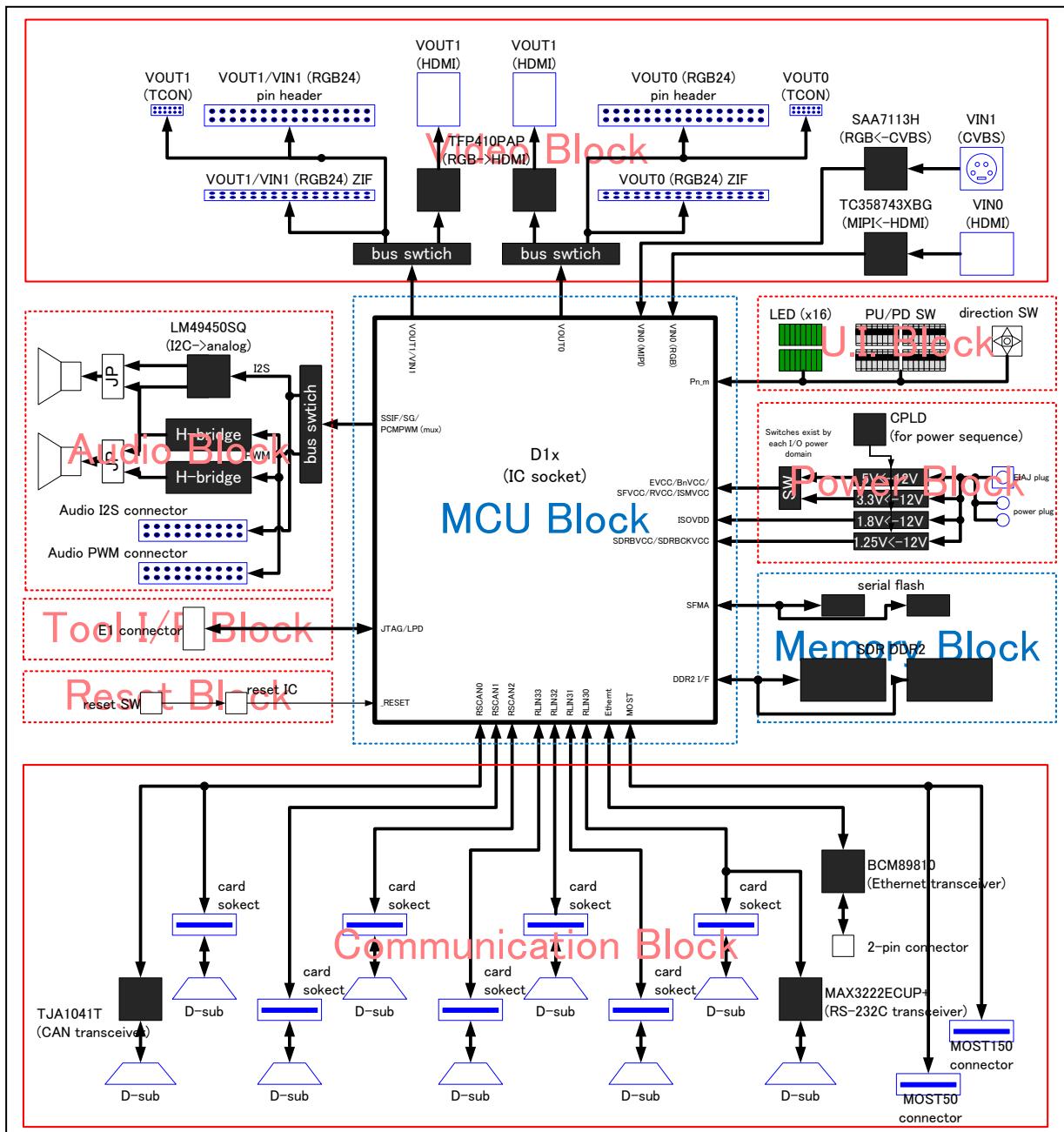


Figure 2-4: RH850/D1x application board block diagram

3 Audio function block

3.1 Overview

The RH850/D1x has the audio interfaces as listed in Table 3-1. The interfaces can either be connected to an on-board driver circuit and speaker or to an external circuit via dedicated connectors. The following subchapter show the required jumper configuration for the use of each mentioned interface. The speaker mounted on the board is an AST-02308MR-R from OUI AUDIO and has $8\Omega / 0.1W$.

Table 3-1: Audio Interfaces of the D1x MCU

Function	Interface	Output
SSIF (I2S)	I2S	Audio DAC + Speaker
SG	PWM control	H-bridge (half bridge) + Speaker
PCM-PWM	PWM control	H-bridge (full bridge) + Speaker

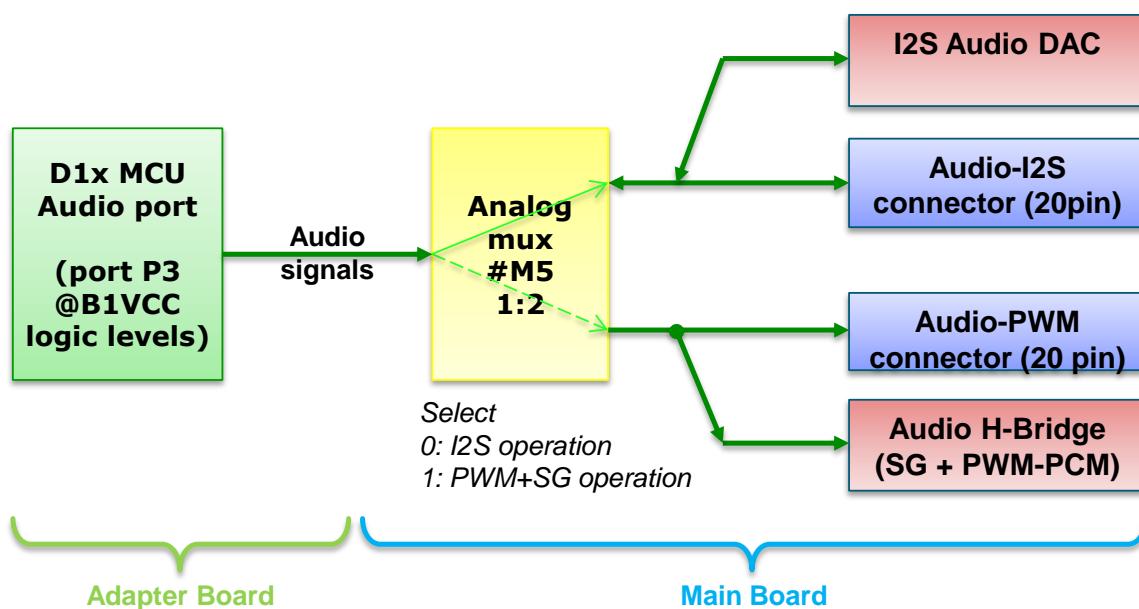


Figure 3-1: Audio multiplexing

Figure 3-2 shows block diagram of the audio functions.

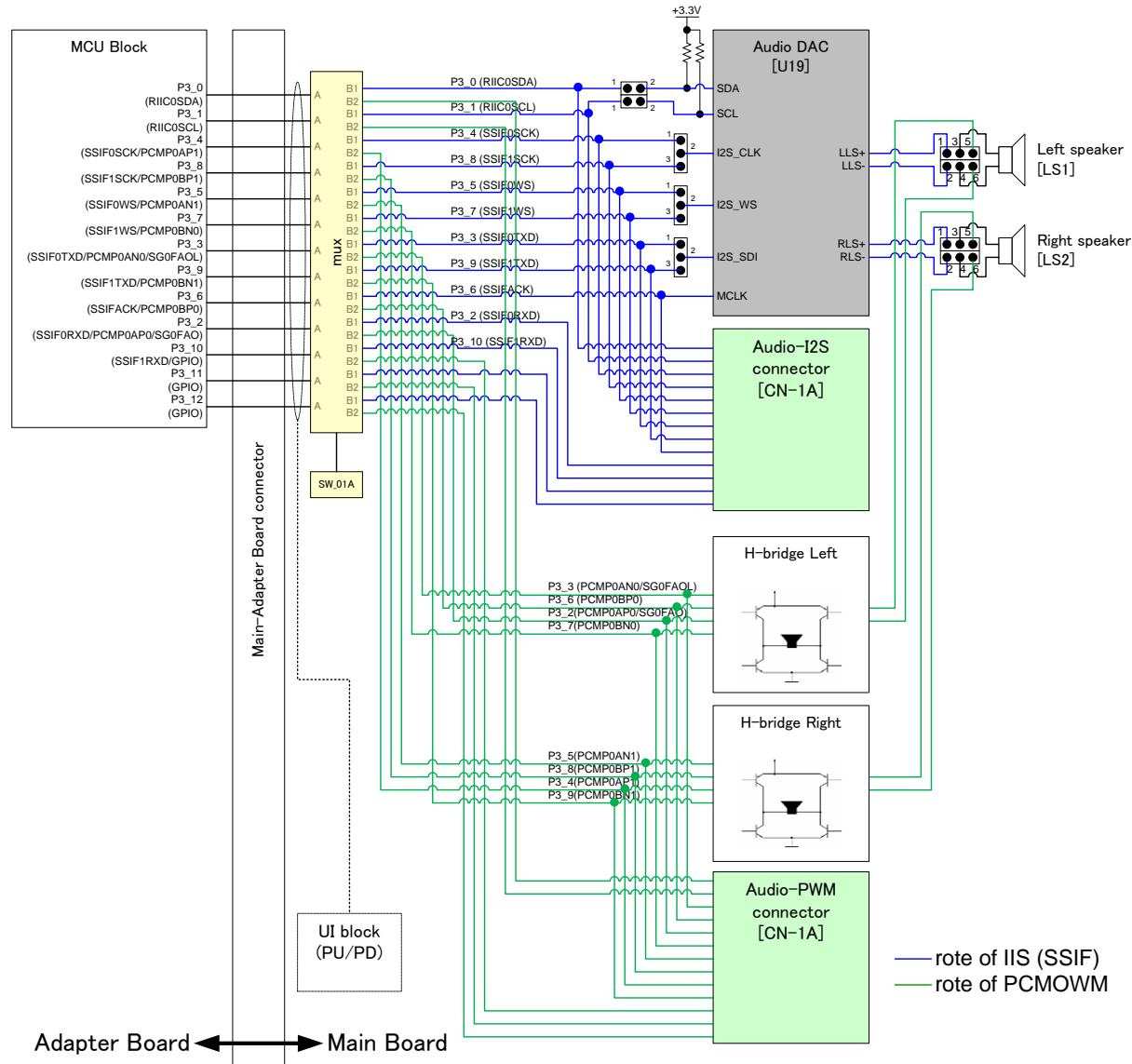


Figure 3-2: Audio System block diagram

3.2 Audio Function specification

3.2.1 Selection of Audio DAC and H-bridge

The Audio part of the Mango Board is designed in such way, that the stereo speakers can be connected to both the I2C Audio DAC and the H-Bridge. Additionally, there is the possibility to connect an external DAC or H-Bridge via the respective 20-pin connectors.

The configuration of the different options is done via Jumpers and DIP switches. Initially, please select either the PWM or the I2S functionality by setting DSW31.3 to the required position (See Table 3-2). This results in the signal routing as shown in Table 3-3 and Table 3-4. Afterwards, the respective function has to be configured by Jumper as described in the chapters 3.2.2 and 3.2.3.

Table 3-2: Selection of audio driver circuit via DSW31.3 (Audio mux)

Loc	Function	
DSW31.3 (AUDIO MUX)	ON (Low)	P3_m (m=0-12) connected to Audio DAC
	OFF (High)	P3_m (m=0-12) connected to H-bridge

Table 3-3: Audio signal routing with DSW31.3 turned ON

Port Pin	Port function to be used	Signal name at Audio DAC	Signal name at Audio I2S connector
P3_0	RIIC0SDA	SDA	I2S_GPIO1
P3_1	RIIC0SCL	SCL	I2S_GPIO2
P3_2	SSIF0RXD	n.c	SSIF0RXD
P3_3	SSIF0TXD	I2S_SDI (via JP610 - JP63) ¹⁾	SSIF0TXD
P3_4	SSIF0SCK	I2S_CLK (via JP57, JP58) ¹⁾	SSIF0SCK
P3_5	SSIF0WS	I2S_WS (via JP59) ¹⁾	SSIF0WS
P3_6	SSIFACK	MCLK	SSIFACK
P3_7	SSIF1WS	I2S_WS (via JP59) ¹⁾	SSIF1WS
P3_8	SSIF1SCK	I2S_CLK (via JP57) ¹⁾	SSIF1SCK
P3_9	SSIF1TXD/ SSIF1RXD	I2S_SDI (via JP62,JP63) ¹⁾	SSIF1TXD/ SSIF1RXD
P3_10	General I/O	n.c	I2S_GPIO3
P3_11	General I/O	n.c	I2S_GPIO4
P3_12	General I/O	n.c	I2S_GPIO5

1) The description of each I2S jumper function is shown in Chapter 3.2.2 and from Table 3-8 to Table 3-11 on the pages below.

Table 3-4: Audio signal routing with DSW31-3 turned OFF

Port Pin	Port Function to be used	Signal name at H-Bridge	Signal name at Audio PWM connector
P3_0	RIIC0SDA	n.c	PWM_GPIO1
P3_1	RIIC0SCL	n.c	PWM_GPIO2
P3_2	PCMP0AP0/ SG0FAO	Connect to (ch-0)	PCMP0AP0 SG0FAO
P3_3	PCMP0AN0/ SG0FAOL	Connect to (ch-0)	PCMP0AN0/ SG0FAOL
P3_4	PCMP0AP1	Connect to (ch-1) ^{*2}	PCMP0AP1
P3_5	PCMP0AN1	Connect to (ch-1) ^{*2}	PCMP0AN1
P3_6	PCMP0BP0	Connect to (ch-0)	PCMP0BP0
P3_7	PCMP0BN0	Connect to (ch-0)	PCMP0BN0
P3_8	PCMP0BP1	Connect to (ch-1)	PCMP0BP1
P3_9	PCMP0BN1	Connect to (ch-1)	PCMP0BN1
P3_10	General I/O	n.c	PWM_GPIO3
P3_11	General I/O	n.c	PWM_GPIO4
P3_12	General I/O	n.c	PWM_GPIO5

2) Although the D1x devices have more than one sound generator channel, only the SG-Channel is routed such that it can be used with the on-board Audio Function Block. To test the remaining SG-Channels, please use the GPIO header connectors.

3.2.2 Configuration of the I2S-DAC

To use the onboard I2S-DAC, please see Table 3-5 for the default jumper positions. The part in use is the 24-bit I2S DAC LM49450SQ from Texas Instruments. The onboard DAC can also be connected to the I2S signals SSIF1 and the HDMI input. Please check the schematic for further information on this connection.

NOTE: Before switching B1VCC to 5V, make sure that I2C-DAC is not connected to the MCU by switching DSW31.3 to OFF or by pulling Jumpers JP56 – JP63.
The I2C-DAC does not support 5V IO signals.

Table 3-5: Jumper configuration for onboard I2S DAC

Jumper	Position	Description
DSW31.3	ON (Low)	Configure the MUX to route MCU's audio signals to I2S part of the circuit.
JP56	1-2	Select ACK signal of MCU
JP57	1-2	Select SCK signal of SSIF0
JP58	Open	Disconnect SCK signal of HDMI input
JP59	1-2	Select WS signal of SSIF0
JP60	Open	Disconnect WS signal of HDMI input
JP61	Open	Disconnect TXD signal of HDMI input
JP62	2-3	Select TXD signal of SSIF0
JP63	1-2	Select TXD signal of SSIF0
JP47	1-2; 3-4	I2C interface for DAC configuration
JP45	1-3; 2-4	Connect the left speaker to the DAC
JP46	1-3; 2-4	Connect the right speaker to the DAC

3.2.3 Configuration of the H-Bridge

To use the onboard H-Bridge with the PCMP interface, please see Table 3-6 for the default jumper positions. The onboard DAC can also be connected to the SG interface, multiplexed to the PCMP interface pins. Please check the schematic for further information on this connection.

Table 3-6: Jumper configuration for onboard H-Bridge in Full-Bridge Mode for PCMP0

Jumper	Position	Description
DSW31.3	OFF (High)	Configure the MUX to route MCU's audio signals to H-Bridge part of the circuit.
JP48	Open / 1-2	Connect AN0
JP49	1-2	Connect BP0
JP50	Open / 1-2	Connect AP0
JP51	1-2	Connect BN0
JP52	Open / 1-2	Connect AN1
JP53	1-2	Connect BP1
JP54	Open / 1-2	Connect AP1
JP55	1-2	Connect BN1
JP45	3-5; 4-6	Connect the left speaker to the H-Bridge
JP46	3-5; 4-6	Connect the right speaker to the H-Bridge

Table 3-7: Jumper configuration for onboard H-Bridge in Half-Bridge Mode for SG0

Jumper	Position	Description
DSW31.3	OFF (High)	Configure the MUX to route MCU's audio signals to H-Bridge part of the circuit.
JP48	2-3	Connect SG0FAOL
JP49	Open	
JP50	2-3	Connect SG0FAO
JP51	Open	
JP52		
JP53		
JP54		
JP55		
JP45	3-5; 4-6	Connect the left speaker to the H-Bridge
JP46		

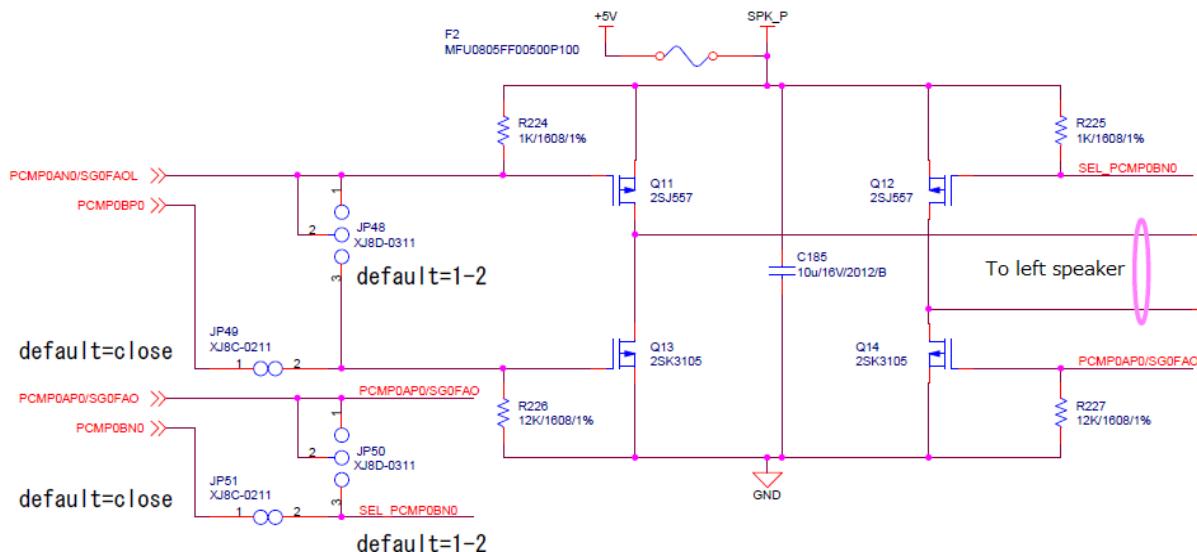


Figure 3-3: Schematic of the Left H-Bridge and its configuration jumpers

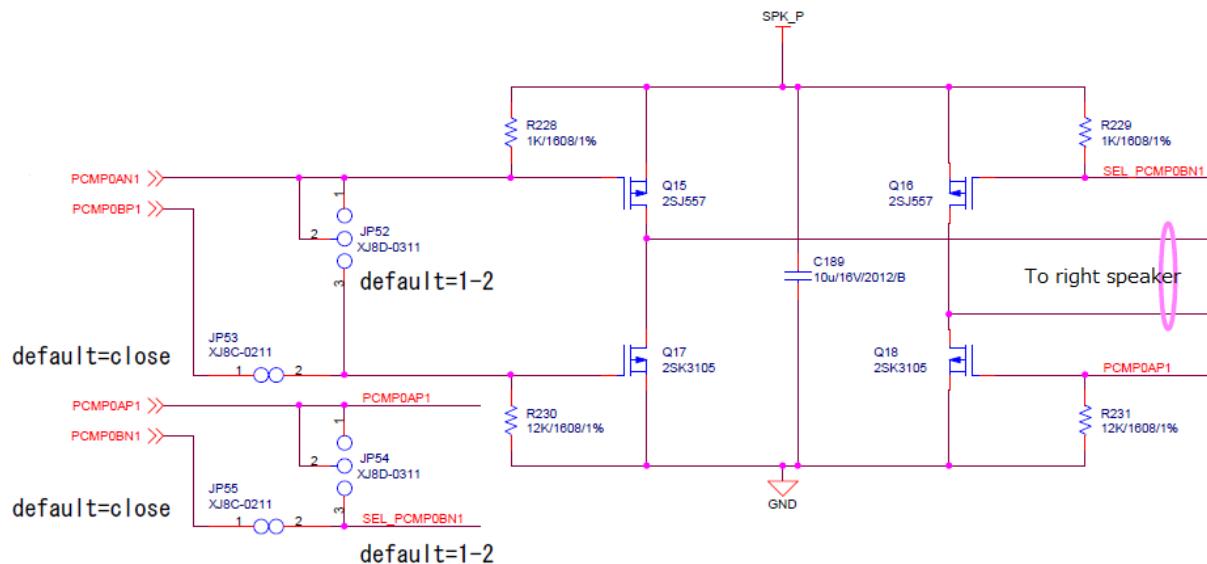


Figure 3-4: Schematic of the Right H-Bridge and its configuration jumpers

3.2.4 Jumper Settings Overview

I2S Audio DAC

For the I2S Audio-DAC you can chose from SSIF0, SSIF1 and HDMI-IN audio channel.

Table 3-8: ACK signal selection

Loc	Function	
JP56	1-2	Select ACK signal of MCU's SSIF
	2-3	Select HDMI_A_OSCK from the HDMI to MIPI I/F

Table 3-9: SCK signal selection

Loc	Function	
JP57	1-2	Select SCK signal from SSIF0
	2-3	Select SCK signal from SSIF1
JP58	1-2	Select HDMI_A_SCK from the HDMI to MIPI I/F

Table 3-10: WS signal selection

Loc	Function	
JP59	1-2	Select WS signal from SSIF0
	2-3	Select WS signal from SSIF1
JP60	1-2	Select HDMI_A_WFS from HDMI to MIPI I/F

Table 3-11: TxD signal selection

Loc	Function	
JP61	1-2	Select HDMI_A_SD from HDMI to MIPI I/F
JP62	1-2	Select RXD from SSIF0
	2-3	Select TXD from SSIF0
JP63	1-2	Select RXD/TXD from SSIF0
	2-3	Select RXD/TXD from SSIF1

H-Bridge

For the H-Bridge you can chose among different bridge configurations to realize full- and half-bridges. The full bridge can be used with the PCMP interface; the half-bridge can be used with the SG interface. The signals with ending zero are defined as left channel, whereas the signals with ending one are defied as right channel.

Table 3-12: Connection of AN0

Loc	Function	
JP48	1-2	Connect left High-side driver of left channel to AN0 (Full-Bridge configuration)
	2-3	Connect left Half-Bridge of left channel to AN0 (Half-Bridge configuration)

Table 3-13: Connection of BP0

Loc	Function	
JP49	1-2	Connect left Low-side driver of left channel to BP0 (Full-Bridge configuration)

Table 3-14: Connection of AP0

Loc	Function	
JP50	1-2	Connect right High-side driver of left channel to AP0 (Full-Bridge configuration)
	2-3	Connect right Half-Bridge of left channel to AP0 (Half-Bridge configuration)

Table 3-15: Connection of BN0

Loc	Function	
JP51	1-2	Connect right Low-side driver of left channel to BN0 (Full-Bridge configuration)

Table 3-16: Connection of AN1

Loc	Function	
JP52	1-2	Connect left High-side driver of right channel to AN1 (Full-Bridge configuration)
	2-3	Connect left Half-Bridge of right channel to AN1 (Half-Bridge configuration)

Table 3-17: Connection of BP1

Loc	Function	
JP53	1-2	Connect left Low-side driver of right channel to BP1 (Full-Bridge configuration)

Table 3-18: Connection of AP1

Loc	Function	
JP54	1-2	Connect right High-side driver of right channel to AP1 (Full-Bridge configuration)
	2-3	Connect right Half-Bridge of right channel to AP1 (Half-Bridge configuration)

Table 3-19: Connection of BN1

Loc	Function	
JP55	1-2	Connect right Low-side driver of right channel to BN1 (Full-Bridge configuration)

Speakers

The signal source for the stereo speakers can be selected between the I2S-DAC and the H-Bridges. Additionally the speaker could also be connected to an external driver circuit.

Table 3-20 Left speaker (Channel 0) connection switch

Loc	Function	
JP45	1-3; 2-4	Connect the left speaker to the left channel of the I2S Audio-DAC
	3-5; 4-6	Connect the left speaker to the (left) H-bridge 0
	3; 4	These terminals can be used to connect an external driver to the left speaker

Table 3-21 Right speaker (Channel 1) connection switch

Loc	Function	
JP46	1-3; 2-4	Connect the right speaker to the right channel of the I2S Audio-DAC
	3-5; 4-6	Connect the right speaker to the (right) H-bridge 1
	3; 4	These terminals can be used to connect an external driver to the right speaker

3.2.5 Connectors for external audio drivers

Next to the board driver circuits it is also possible to connect external driver circuits to the Audio function block of the Mango Board. There are two 20-pin connectors, each dedicated either to the I2S interface or the PCM-PWM and SG interface.

The Audio I2S connector is called CN33. The pin assignment is shown in Table 3-22. The Audio PWM connector is called CN34 and its pin assignment is shown in Table 3-23 below.

Table 3-22: Pin assignment of the Audio I2S connector (CN33)

Pin	Signal name	Connected to
1	SSIF1WS	P3_7 (via DSW31.3 "AUDIO MUX" = ON)
2	SSIF1SCK	P3_8 (via DSW31.3 "AUDIO MUX" = ON)
3	SSIF1TXD/SSIF1RXD	P3_9 (via DSW31.3 "AUDIO MUX" = ON)
4	GND	GND
5	SSIF0RXD	P3_2 (via DSW31.3 "AUDIO MUX" = ON)
6	SSIF0TXD	P3_3 (via DSW31.3 "AUDIO MUX" = ON)
7	SSIF0SCK	P3_4 (via DSW31.3 "AUDIO MUX" = ON)
8	SSIF0WS	P3_5 (via DSW31.3 "AUDIO MUX" = ON)
9	SSIFACK	P3_6 (via DSW31.3 "AUDIO MUX" = ON)
10	GND	GND
11	I2S_GPIO1(RIIC0SDAL)	P3_0 (via DSW31.3 "AUDIO MUX" = ON)
12	I2S_GPIO2(RIIC0SCL)	P3_1 (via DSW31.3 "AUDIO MUX" = ON)
13	I2S_GPIO3/SSIF1RXD	P3_10 (via DSW31.3 "AUDIO MUX" = ON)
14	I2S_GPIO4	P3_11 (via DSW31.3 "AUDIO MUX" = ON)
15	I2S_GPIO5	P3_12 (via DSW31.3 "AUDIO MUX" = ON)
16	GND	GND
17	+5V	+5V
18	GND	GND
19	+3.3V	+3.3V
20	B1VCC	B1VCC

Table 3-23: Pin assignment of the Audio PWM connector (CN34)

Pin	Signal name	Connected to
1	PCMP0AP0/SG0FAO	P3_2 (via DSW31.3 "AUDIO MUX" = OFF)
2	PCMP0AN0/SG0FAOL	P3_3 (via DSW31.3 "AUDIO MUX" = OFF)
3	PCMP0BP0	P3_4 (via DSW31.3 "AUDIO MUX" = OFF)
4	GND	GND
5	PCMP0BN0	P3_7 (via DSW31.3 "AUDIO MUX" = OFF)
6	PCMP0AP1	P3_4 (via DSW31.3 "AUDIO MUX" = OFF)
7	PCMP0AN1	P3_5 (via DSW31.3 "AUDIO MUX" = OFF)
8	PCMP0BP1	P3_8 (via DSW31.3 "AUDIO MUX" = OFF)
9	PCMP0BN1	P3_9 (via DSW31.3 "AUDIO MUX" = OFF)
10	GND	GND
11	PWM_GPIO1(RIIC0SDAL)	P3_0 (via DSW31.3 "AUDIO MUX" = OFF)
12	PWM_GPIO2(RIIC0SCL)	P3_1 (via DSW31.3 "AUDIO MUX" = OFF)
13	PWM_GPIO3	P3_10 (via DSW31.3 "AUDIO MUX" = OFF)
14	PWM_GPIO4	P3_11 (via DSW31.3 "AUDIO MUX" = OFF)
15	PWM_GPIO5	P3_12 (via DSW31.3 "AUDIO MUX" = OFF)
16	GND	GND
17	+5V	+5V
18	GND	GND
19	+3.3V	+3.3V
20	B1VCC	B1VCC

4 Video block

4.1 Overview

The Mango Board has the video interfaces as listed in Table 4-1 below. Not all of these video interfaces can be used in parallel, as some of them are muxed to common pins on the MCU. Please check Chapter 5 for the muxing scheme.

Table 4-1: Video block connector

Function	CN	I/F	Usage
VOUT0	CN44	2.54mm 2x20 male connector	TFT Display Board Video output
	CN45	2.54mm 2x25 ZIFconnector	Connection to LCD panel
	CN49	HDMI type A receptacle (female)	General display I/F
	CN46	2.54mm 2x5 male connector	TFT Display Board Touch screen input
	CN47	1.27mm 2x6 male connector	Connection to LCD panel (TCON)
	CN48	2.54mm 2x5 male connector	TFT Display Board command output
VOUT1	CN40	2.54mm 2x20 male connector	Connection to LCD panel (Shared with VIN1)
	CN41	2.54mm 2x25 ZIFconnector	Connection to LCD panel
	CN43	HDMI type A receptacle (female)	Connection to general display
	CN42	1.27mm 2x6 male connector	Connection to LCD panel (TCON)
VIN0	CN35	2.54mm 2x20 male connector	Video Input
	CN36	2.54mm 2x25 ZIFconnector	Video Input
	CN52	MIPI board connector The MIPI board contains a HDMI type A receptacle (female) connector.	Connection to general video input
VIN1	CN37	2x8 male connector	Connection to ITU video input
	CN38	CVBS (Composite Video, Blanking, and Sync)	Connection to analog video signal Jack
	CN40	2.54mm 2x20 male connector	Video Input (Shared with VOUT1)

4.2 Video signal structure

Video signal line is composed of VOUT0, VOUT1/VIN1, VIN0(MIPI), VIN1(CVBS, ITU).

▪ VOUT0

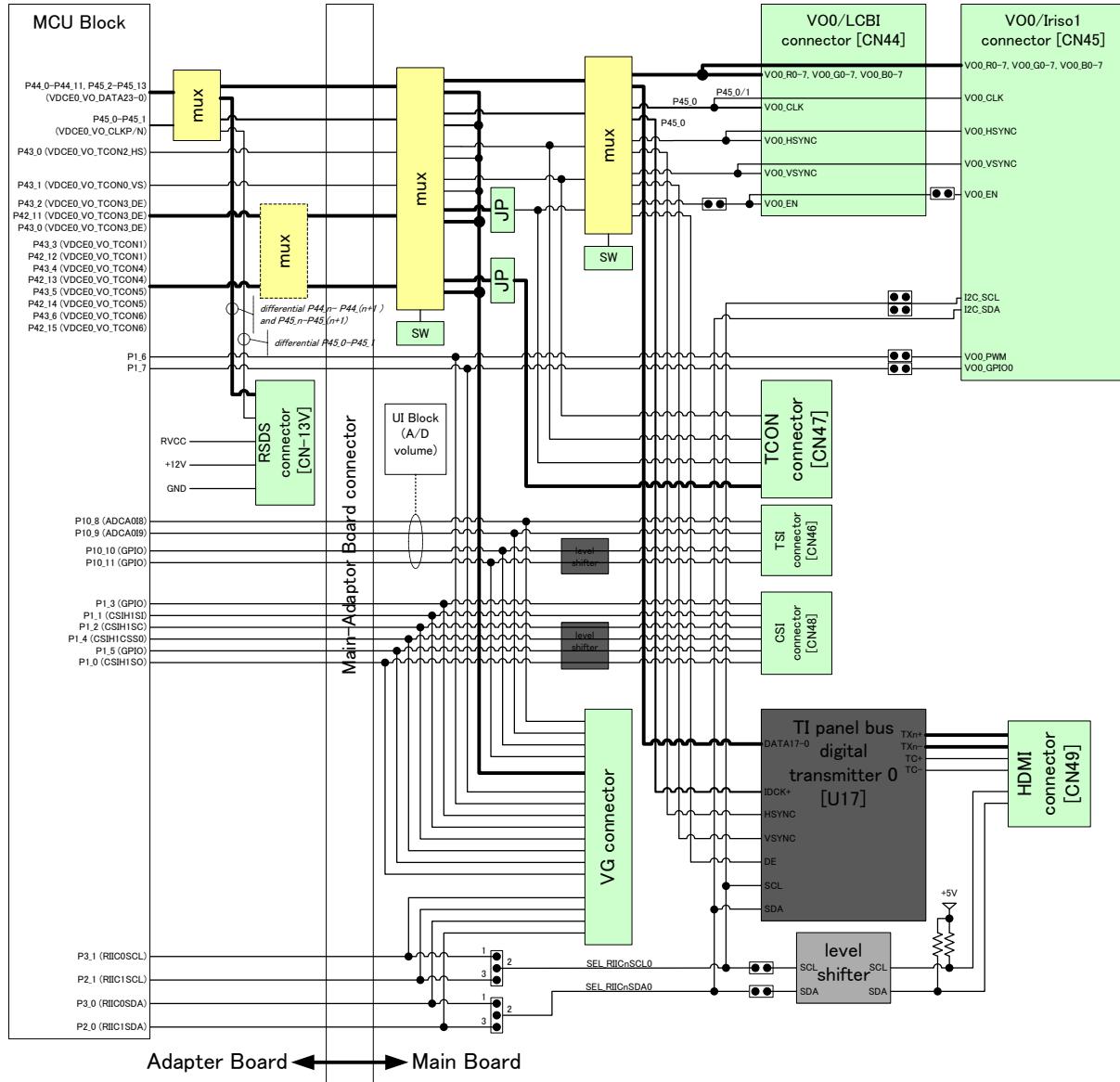


Figure 4-1: Video Block diagram (VOUT0)

▪ VOUT1/VIN1

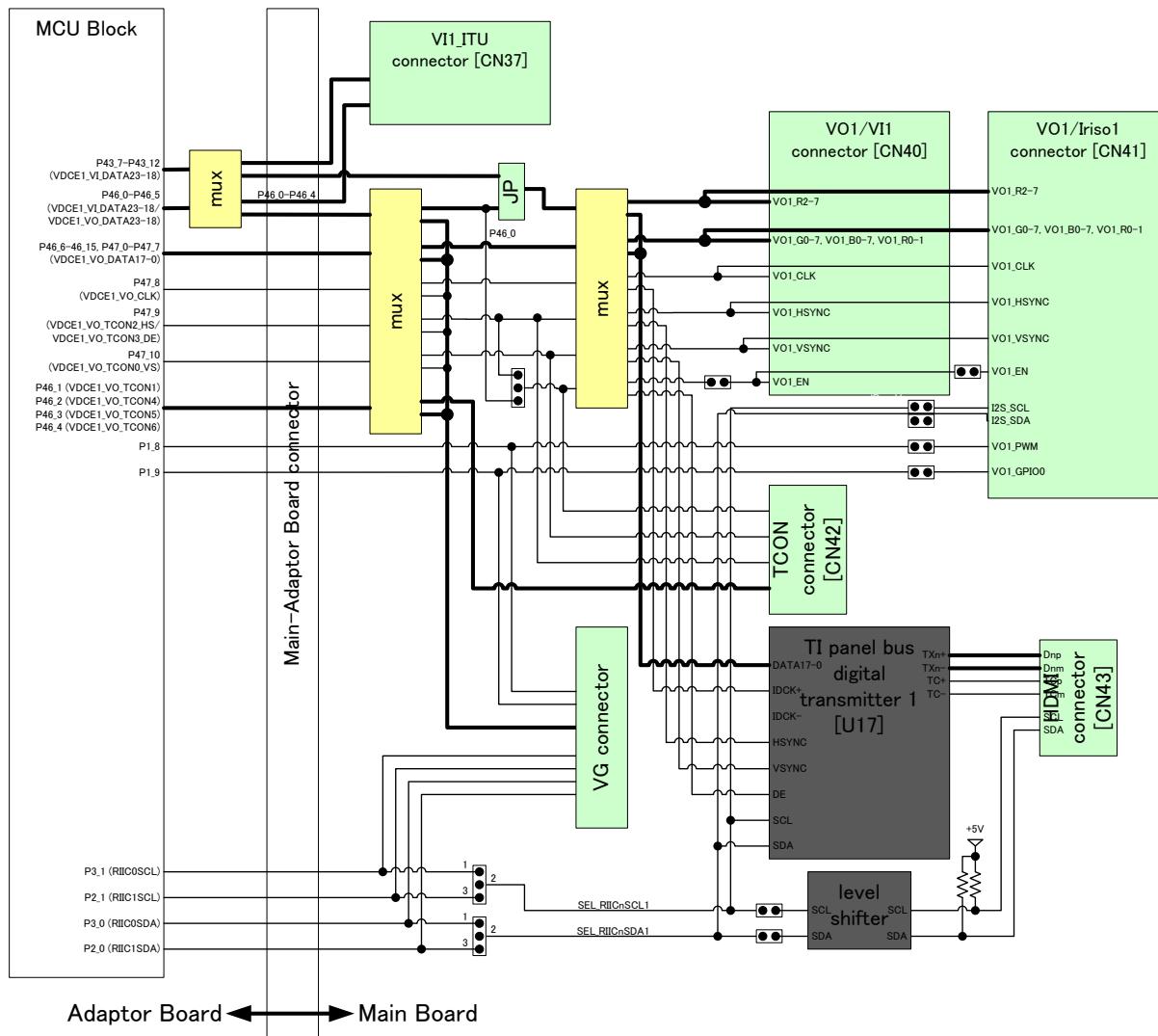


Figure 4-2: Video Block diagram (VOUT1/VIN1)

▪ **VIN0**

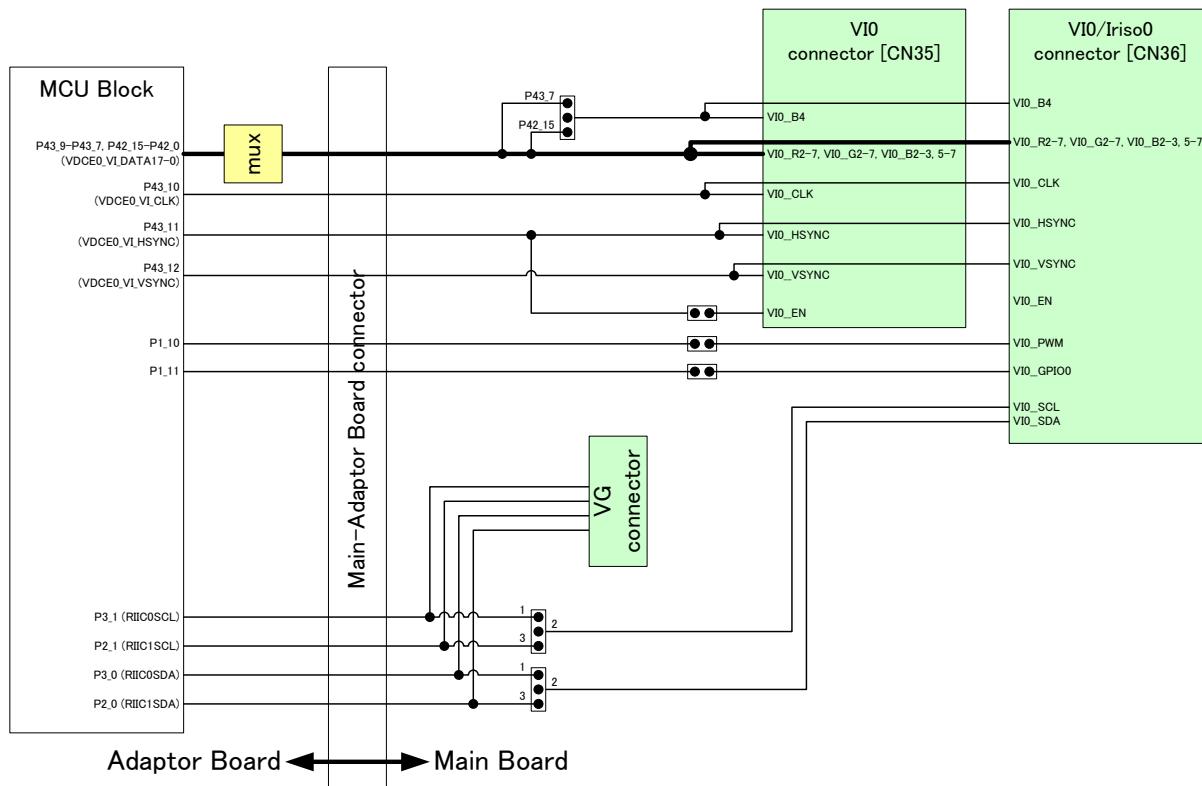


Figure 4-3: Video Block diagram (VIN0)

▪ **VIN0(MIPI)**

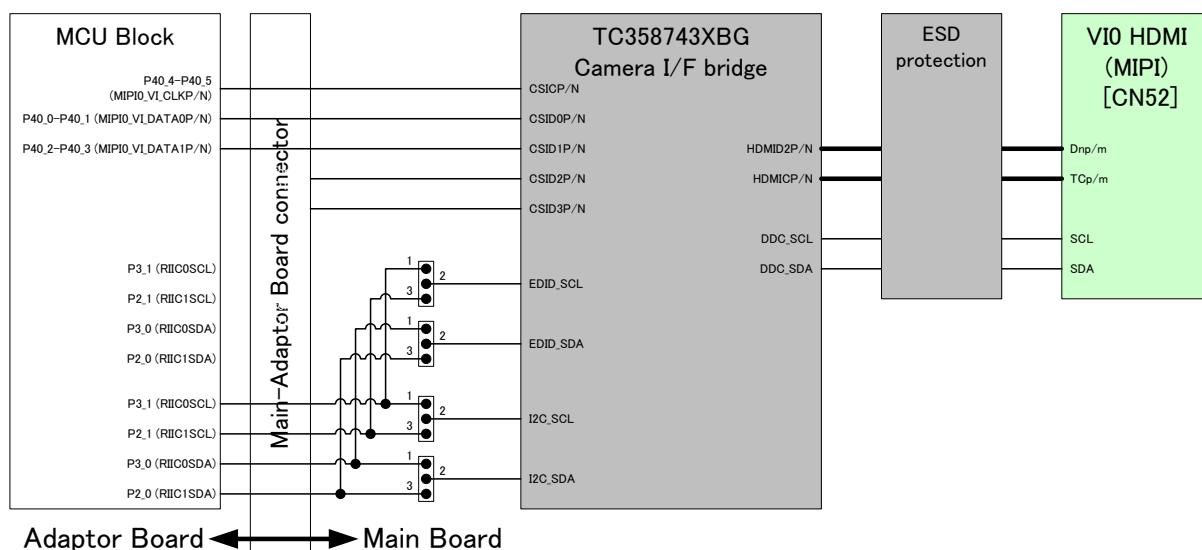


Figure 4-4: Video Block diagram (VIN0(MIPI))

• VIN1(CVBS)

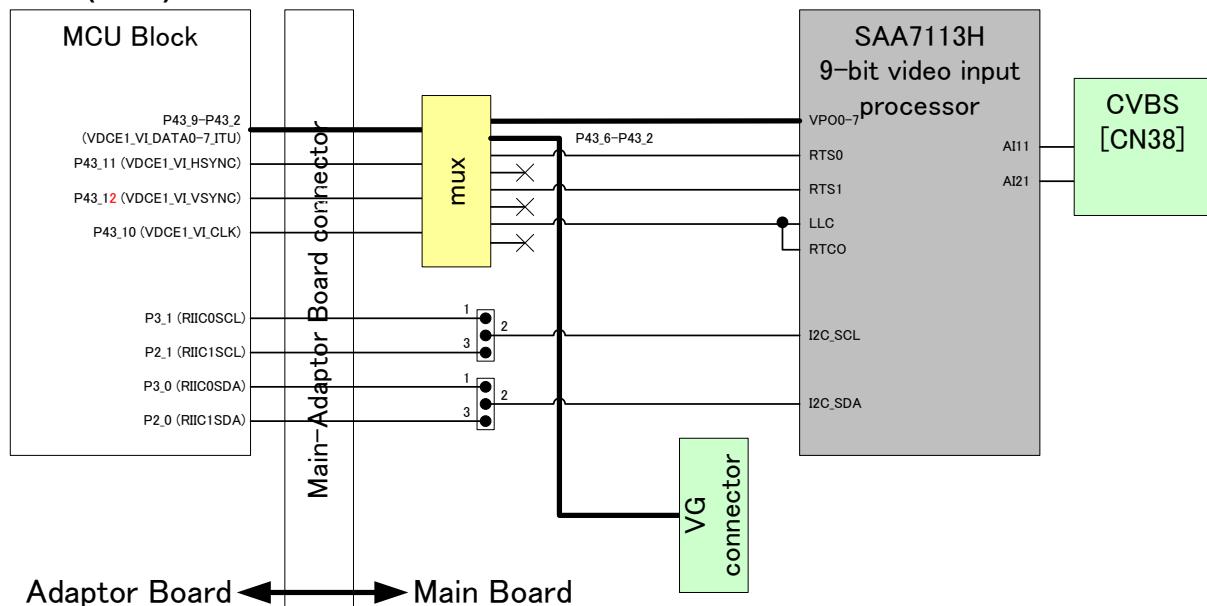


Figure 4-5: Video Block diagram (VIN0(CVBS))

4.3 Video signal connector list

For an overview of all video signal connectors, please see Table 4-1 in chapter 4.1 above. More details on each connector are shown in the following subchapters. For video mux and jumper configuration, please see chapter 5.

4.3.1 40pol TFT Display Board connector

This connector can be used to connect TFT Displays with RGB565 or RGB888 colour input.

The video output data lines may have a voltage level of 3.3V or 5V depending on the configuration of the power domains.

In Table 4-2, the pin assignment of the connector CN44 for VOUT0 is listed. Following this, the pin assignment of connector CN40 for VOUT1 is listed in Table 4-3.

Table 4-2: VO0/LCBI - TFT Display Board Connector (CN44) Pin assignment

Pin	Signal name	Connected to	Pin	Signal name	Connected to
1	VO0_R2	P44_5	2	VO0_B2	P45_11
3	+3.3V	+3.3V	4	N.C	-
5	VO0_B3	P45_10	6	VO0_B4	P45_9
7	VO0_B5	P45_8	8	VO0_B6	P45_7
9	VO0_B7	P45_6	10	GND	GND
11	VO0_G2	P45_3	12	VO0_G3	P45_2
13	VO0_G4	P44_11	14	VO0_G5	P44_10
15	VO0_G6	P44_9	16	VO0_G7	P44_8
17	GND	GND	18	VO0_R3	P44_4
19	VO0_R4	P44_3	20	VO0_R5	P44_2
21	VO0_R6	P44_1	22	VO0_R7	P44_0
23	+3.3V	+3.3V	24	N.C	-
25	VO0_HSYNC	P43_0	26	VO0_VSYNC	P43_1
27	VO0_CLK	P43_1	28	SEL_VO0_EN	P43_0 / P43_2 / P42_11
29	GND	GND	30	GND	GND
31	+3.3V	+3.3V	32	VO0_R0	P44_7
33	VO0_R1	P44_6	34	VO0_G0	P45_5
35	VO0_G1	P45_4	36	VO0_B0	P45_13
37	VO0_B1	P45_12	38	N.C	-
39	N.C	-	40	GND	GND

The following table lists the pin assignments of the VO1 40pin connector. The connector CN40 is at the same time the video input VI1. The direction of the video function has to be controlled by software.

Table 4-3: VO1/LCBI - TFT Display Board Connector (CN40) Pin assignment

Pin	Signal name	Connected to	Pin	Signal name	Connected to
1	VO1_R2	P43_12 / P46_5	2	VO1_B2	P47_5
3	+3.3V	+3.3V	4	N.C	-
5	VO1_B3	P47_4	6	VO1_B4	P47_3
7	VO1_B5	P47_2	8	VO1_B6	P47_1
9	VO1_B7	P47_0	10	GND	GND
11	VO1_G2	P46_13	12	VO1_G3	P46_12
13	VO1_G4	P46_11	14	VO1_G5	P46_10
15	VO1_G6	P46_9	16	VO1_G7	P46_8
17	GND	GND	18	VO1_R3	P43_11 / P46_4
19	VO1_R4	P43_10 / P46_3	20	VO1_R5	P43_9 / P46_2
21	VO1_R6	P43_8 / P46_1	22	VO1_R7	P43_7 / P46_0
23	+3.3V	+3.3V	24	N.C	-
25	VO1_HSYNC	P47_9	26	VO0_VSYNC	P47_10
27	VO1_CLK	P47_8	28	SEL_VO1_EN	P47_9 / P47_X2 / P43_7 / P46_0
29	GND	GND	30	GND	GND
31	+3.3V	+3.3V	32	VO1_R0	P46_7
33	VO1_R1	P46_6	34	VO1_G0	P46_15
35	VO1_G1	P46_14	36	VO1_B0	P47_7
37	VO1_B1	P47_6	38	N.C	-
39	N.C	-	40	GND	GND

Note: The connectors CN40 and CN44 have a fixed supply of +3.3V to power the connected display. Please make sure to switch B2VCC (CN40) and RVCC/B5VCC (CN44) to +3.3V if the display doesn't support a voltage level of +5V on the data lines!

The Mango board has a connector dedicated to displays that need a certain initialization sequence. This connector provides a connection to the MCU's Clocked Serial Interface (CSI) as well as some GPIO pins. The voltage levels signals on the connector CN48 "CSI" are level-shifted to +3.3V regardless of the power supply settings.

Table 4-4: Clocked Serial Interface for Display Boards (CN48) Pin assignment

Pin	Signal Name	Direction (MCU view)	Connected to
1	CSI_SO	Output	P1_0 (CSIH1SO) (via Level Shifter)
2	CSI_SI	Input	P1_1 (CSIH1SI)
3	CSI_SCK	Output	P1_2 (CSIH1SC) (via Level Shifter)
4	GND	-	GND
5	3.3V	-	3.3V
6	LIGHT_ENAB	Output	P1_3 (GPIO) (via Level Shifter)
7	CSI_CSZ	Output	P1_4 (CSIH1CSS0) (via Level Shifter)
8	GND	-	GND
9	CSI_RESZ	Output	P1_5 (GPIO) (via Level Shifter)
10	GND	-	GND

Another connector of the video block is dedicated to the connection of touch screen interfaces. The connector supports four-wire resistive touch screens.

Table 4-5: Touch Screen Interface for Display Boards (CN46) Pin Assignment

Pin	Signal Name	Direction (MCU View)	Connected to
1	X_OUT	Analog Input / Digital Output	P10_8 (ADCE0I8) (unshifted)
2	GND		GND
3	Y_OUT	Analog Input / Digital Output	P10_9 (ADCE0I9) (unshifted)
4	GND		GND
5	3.3V		3.3V
6	N.C.		N.C.
7	X_ACTZ	Digital Output	P10_10 (ADCE0I10) (via Level Shifter)
8	GND		GND
9	Y_ACTZ	Digital Output	P10_11 (ADCE0I11) (via Level Shifter)
10	GND		GND

4.3.2 TCON Video outputconnector (CN42, CN47)

This connector is used for LCD panel withs TCON and provides all timing signals of the respective video output channels and a dedicated connector.

Table 4-6: TCON0 connector for VO0 (CN47) Pin Assignment

Pin	Signal Name		Connected to
1	TCON0_0	VDCE0_VO_TCON0_0	P43_1
2	TCON0_1	VDCE0_VO_TCON0_1	P43_3 or P42_12
3	TCON0_2	VDCE0_VO_TCON0_2	P43_0
4	TCON0_3	VDCE0_VO_TCON0_3	P43_0 or P42_11 or P43_2
5	TCON0_4	VDCE0_VO_TCON0_4	P43_4 or P42_13
6	TCON0_5	VDCE0_VO_TCON0_5	P43_5 or P42_14
7	TCON0_6	VDCE0_VO_TCON0_6	P43_6 or P42_15
8	N.C.	N.C.	
9	N.C.	N.C.	
10	GND	GND	
11	B2VCC	B2VCC	
12	GND	GND	

Table 4-7: TCON1 connector for VO1 (CN42) Pin Assignment

Pin	Signal Name		Connected to
1	TCON1_0	VDCE1_VO_TCON0_0	P47_10
2	TCON1_1	VDCE1_VO_TCON0_1	P46_1
3	TCON1_2	VDCE1_VO_TCON0_2	P47_9
4	TCON1_3	VDCE1_VO_TCON0_3	P47_9 / P47_X2 / P43_7 / P46_0
5	TCON1_4	VDCE1_VO_TCON0_4	P46_2
6	TCON1_5	VDCE1_VO_TCON0_5	P46_3
7	TCON1_6	VDCE1_VO_TCON0_6	P46_4
8	N.C.	N.C.	
9	N.C.	N.C.	
10	GND	GND	
11	B2VCC	B2VCC	
12	GND	GND	

4.3.3 Parallel Video Output Iriso connector (CN45, CN41)

This connector is used to connect displays with IRISO connector. The connector has some pins coming from another voltage domain. Make sure, that the voltages are in the operating range of the connected display.

Table 4-8: Iriso Connector for VO0 (CN45) Pin Assignment

Pin	Ports	Signal name	Connected to
1	GND	GND	
2	+3.3V	+3.3V	
3	GND	GND	
4	VO0_EN	VDCE0_VO_TCON3	P43_0 / P43_2 / P42_11
5	+3.3V	+3.3V	
6	VO0_B7	VDCE0_VO_DATA7	P45_6
7	VO0_B6	VDCE0_VO_DATA6	P45_7
8	VO0_B5	VDCE0_VO_DATA5	P45_8
9	VO0_B4	VDCE0_VO_DATA4	P45_9
10	VO0_B3	VDCE0_VO_DATA3	P45_10
11	VO0_B2	VDCE0_VO_DATA2	P45_11
12	VO0_B1	VDCE0_VO_DATA1	P45_12
13	VO0_B0	VDCE0_VO_DATA0	P45_13
14	GND	GND	
15	VO0_G7	VDCE0_VO_DATA15	P44_8
16	VO0_G6	VDCE0_VO_DATA14	P44_9
17	VO0_G5	VDCE0_VO_DATA13	P44_10
18	VO0_G4	VDCE0_VO_DATA12	P44_11
19	VO0_G3	VDCE0_VO_DATA11	P45_2
20	VO0_G2	VDCE0_VO_DATA10	P45_3
21	VO0_G1	VDCE0_VO_DATA9	P45_4
22	VO0_G0	VDCE0_VO_DATA8	P45_5
23	GND	GND	
24	VO0_R7	VDCE0_VO_DATA16	P44_0
25	VO0_R6	VDCE0_VO_DATA17	P44_1
26	VO0_R5	VDCE0_VO_DATA18	P44_2
27	VO0_R4	VDCE0_VO_DATA19	P44_3
28	VO0_R3	VDCE0_VO_DATA20	P44_4
29	VO0_R2	VDCE0_VO_DATA21	P44_5
30	VO0_R1	VDCE0_VO_DATA22	P44_6
31	VO0_R0	VDCE0_VO_DATA23	P44_7
32	GND	GND	
33	VO0_CLK	VDCE0_VO_CLKP	P45_0
34	GND	GND	
35	VO0_VSYNC	VDCE0_VO_TCON0	P43_1
36	VO0_HSYNC	VDCE0_VO_TCON2	P43_0
37	VO0_CLKN	VDCE0_VO_CLKN	P45_1
38	GND	GND	
39	GND	GND	
40	+3.3V	+3.3V	
41	VO0_PWM	GPIO / TAUB0I1 / TAUB0O1	P1_6
42	N.C.	N.C.	
43	N.C.	N.C.	
44	GND	GND	
45	VO0_SDA	RIIC1SDA / RIIC0SDA	P2_0 / P3_0
46	VO0_SCL	RIIC1SCL / RIIC0SCL	P2_1 / P3_1
47	N.C.	N.C.	
48	N.C.	N.C.	
49	VO0_GPIO0	GPIO / TAUB0I2 / TAUB0O2	P1_7
50	GND	GND	

Table 4-9: Iriso Connector for VO1 (CN41) Pin Assignment

Pin	Function	Signal name	Connected to
1	GND	GND	
2	+3.3V	+3.3V	
3	GND	GND	
4	VO1_EN	VDCE1_VO_TCON3	P47_9 / P47_X2 / P43_7 / P46_0
5	+3.3V	+3.3V	
6	VO1_B7	VDCE1_VO_DATA7 / VDCE1_VI_DATA7	P47_0
7	VO1_B6	VDCE1_VO_DATA6 / VDCE1_VI_DATA6	P47_1
8	VO1_B5	VDCE1_VO_DATA5 / VDCE1_VI_DATA5	P47_2
9	VO1_B4	VDCE1_VO_DATA4 / VDCE1_VI_DATA4	P47_3
10	VO1_B3	VDCE1_VO_DATA3 / VDCE1_VI_DATA3	P47_4
11	VO1_B2	VDCE1_VO_DATA2 / VDCE1_VI_DATA2	P47_5
12	VO1_B1	VDCE1_VO_DATA1 / VDCE1_VI_DATA1	P47_6
13	VO1_B0	VDCE1_VO_DATA0 / VDCE1_VI_DATA0	P47_7
14	GND		
15	VO1_G7	VDCE1_VO_DATA15 / VDCE1_VI_DATA15	P46_8
16	VO1_G6	VDCE1_VO_DATA14 / VDCE1_VI_DATA14	P46_9
17	VO1_G5	VDCE1_VO_DATA13 / VDCE1_VI_DATA13	P46_10
18	VO1_G4	VDCE1_VO_DATA12 / VDCE1_VI_DATA12	P46_11
19	VO1_G3	VDCE1_VO_DATA11 / VDCE1_VI_DATA11	P46_12
20	VO1_G2	VDCE1_VO_DATA10 / VDCE1_VI_DATA10	P46_13
21	VO1_G1	VDCE1_VO_DATA9 / VDCE1_VI_DATA9	P46_14
22	VO1_G0	VDCE1_VO_DATA8 / VDCE1_VI_DATA8	P46_15
23	GND		
24	VO1_R7	VDCE1_VO_DATA16 / VDCE1_VI_DATA16	P43_7 / P46_0
25	VO1_R6	VDCE1_VO_DATA17 / VDCE1_VI_DATA17	P43_8 / P46_1
26	VO1_R5	VDCE1_VO_DATA18 / VDCE1_VI_DATA18	P43_9 / P46_2
27	VO1_R4	VDCE1_VO_DATA19 / VDCE1_VI_DATA19	P43_10 / P46_3
28	VO1_R3	VDCE1_VO_DATA20 / VDCE1_VI_DATA20	P43_11 / P46_4
29	VO1_R2	VDCE1_VO_DATA21 / VDCE1_VI_DATA21	P43_12 / P46_5
30	VO1_R1	VDCE1_VO_DATA22 / VDCE1_VI_DATA22	P46_6
31	VO1_R0	VDCE1_VO_DATA23 / VDCE1_VI_DATA23	P46_7
32	GND	GND	
33	VO1_CLK		P47_8
34	GND	GND	
35	VO1_VSYNC	VDCE1_VO_TCON0 / VDCE1_VI_VSYNC	P47_10
36	VO1_HSYNC	VDCE1_VO_TCON2 / VDCE1_VI_HSYNC	P47_9
37	N.C.	N.C.	
38	GND	GND	
39	GND	GND	
40	+3.3V	+3.3V	
41	VO1_PWM	GPIO / TAUB0I3 / TAUB0O3	P1_8
42	N.C.	N.C.	
43	N.C.	N.C.	
44	GND	GND	
45	VO1_SDA	RIIC1SDA / RIIC0SDA	P2_0 / P3_0
46	VO1_SCK	RIIC1SCL / RIIC0SCL	P2_1 / P3_1
47	N.C.	N.C.	
48	N.C.	N.C.	
49	VO1_GPIO0	P1_9 (JP78)	P1_9
50	GND	GND	

Note: The connectors CN41 and CN45 have a fixed supply of +3.3V to power the connected display. Please make sure to switch B2VCC (CN41) and RVCC/B5VCC (CN45) to +3.3V if the display doesn't support a voltage level of +5V on the data lines!

4.3.4 HDMI Video Output connector (CN49, CN43)

The following connectors are used for HDMI video output (24bit RGB data) from VO0 and VO1. The internal Pin assignment of the RGB video to HDMI converters 0 and 1 is equal to the Pin assignment of the Irliso connectors CN45 and CN1 with exception of the GPIO signals.

Table 4-10: HDMI connector pin assignment for CN49 and CN43

Pin	CN49 (VO0)	CN43 (VO1)
1	D2p (red data+)	D2p (red data+)
2	GND	GND
3	D2m (red data-)	D2m (red data-)
4	D1p (green data+)	D1p (green data+)
5	GND	GND
6	D1m (green data-)	D1m (green data-)
7	D0p (blue data+)	D0p (blue data+)
8	GND	GND
9	D0m (blue data-)	D0m (blue data-)
10	TCp (DVI +)	TCp (DVI +)
11	GND	GND
12	TCm (DVI -)	TCm (DVI -)
13	n.c	n.c
14	n.c	n.c
15	VO0HDMI_SCL	VO1HDMI_SCL
16	VO0HDMI_SDA	VO1HDMI_SDA
17	GND	GND
18	+5V	+5V
19	n.c	n.c

The parallel RGB video to HDMI converter IC in use is the TFP410PAP from Texas Instruments. The following tables show the connection of both ICs to the video output signals of the MCU.

Table 4-11: Signal assignment of the RGB to HDMI video converter ICs

Pin Name	Function	Connections of VO0 (Converter IC U32 for CN49)	Connections of VO1 (Converter IC U24 for CN43)
DATA0	VO0HDMI_B0	P45_13	P47_7
DATA1	VO0HDMI_B1	P45_12	P47_6
DATA2	VO0HDMI_B2	P45_11	P47_5
DATA3	VO0HDMI_B3	P45_10	P47_4
DATA4	VO0HDMI_B4	P45_9	P47_3
DATA5	VO0HDMI_B5	P45_8	P47_2
DATA6	VO0HDMI_B6	P45_7	P47_1
DATA7	VO0HDMI_B7	P45_6	P47_0
DATA8	VO0HDMI_G0	P45_5	P46_15
DATA9	VO0HDMI_G1	P45_4	P46_14
DATA10	VO0HDMI_G2	P45_3	P46_13
DATA11	VO0HDMI_G3	P45_2	P46_12
DATA12	VO0HDMI_G4	P44_11	P46_11
DATA13	VO0HDMI_G5	P44_10	P46_10
DATA14	VO0HDMI_G6	P44_9	P46_9
DATA15	VO0HDMI_G7	P44_8	P46_8
DATA16	VO0HDMI_R0	P44_7	P43_7 / P46_0
DATA17	VO0HDMI_R1	P44_6	P43_8 / P46_1
DATA18	VO0HDMI_R2	P44_5	P43_9 / P46_2
DATA19	VO0HDMI_R3	P44_4	P43_10 / P46_3
DATA20	VO0HDMI_R4	P44_3	P43_11 / P46_4
DATA21	VO0HDMI_R5	P44_2	P43_12 / P46_5
DATA22	VO0HDMI_R6	P44_1	P46_6
DATA23	VO0HDMI_R7	P44_0	P46_7
IDCK+	VO0HDMI_CLK	P45_0	P47_8
DE	VO0HDMI_EN	P43_0 / P43_2 / P42_11	P47_9 / P47_X2 / P43_7 / P46_0
VSYNC	VO0HDMI_VSYNC	P43_1	P47_10
HSYNC	VO0HDMI_HSYNC	P43_0	P47_9
BSEL/SCL	I2C_SCL	P2_1 / P3_1	P2_1 / P3_1
DSEL/SDA	I2C_SDA	P2_0 / P3_0	P2_0 / P3_0

4.3.5 HDMI Video input connector (CN52)

This connector is used for HDMI video input. The connector is placed on a dedicated converter board that is delivered together with the Main Board. The converter IC in use is the TC358743XBG from Toshiba Electronics.

Table 4-12: Pin assignment of the HDMI to MIPI converter board connector CN52.

Pin	Function	Connected to	Pin	Function	Connected to
1	+1.2V		2	+3.3V	
3	+1.2V		4	+3.3V	
5	+2.5V		6	+5V	
7	+2.5V		8	+5V	
9	MVCC		10	n.c	
11	MVCC		12	n.c	
13	MIPI0_VI_DATA0P	P40_0	14	n.c	
15	MIPI0_VI_DATA0N	P40_1	16	n.c	
17	MIPI0_VI_DATA1P	P40_2	18	GND	
19	MIPI0_VI_DATA1N	P40_3	20	BOARD_RESET	Reset Circuit
21	GND		22	I2C_SCL	P2_1 / P3_1
23	GND		24	I2C_SDA	P2_0 / P3_0
25	MIPI0_VI_CLKP	P40_4	26	GND	
27	MIPI0_VI_CLKN	P40_5	28	GND	
29	CSID2P	CSID2P	30	HDMI_A_OSCK	I2S-Audio Block
31	CSID2N	CSID2N	32	HDMI_A_SCK	I2S-Audio Block
33	GND		34	HDMI_A_WFS	I2S-Audio Block
35	GND		36	HDMI_A_SD	I2S-Audio Block
37	CSID3P	CSID3P	38	GND	
39	CSID3N	CSID3N	40	GND	
41	GND		42	GND	
43	GND		44	GND	

4.3.6 Parallel Video Input 0 connector (CN35)

This parallel 40pin connector can be used for camera modules or other parallel video sources.

Table 4-13: VI0 – Video Input Connector 0 (CN35) Pin assignment

Pin	Signal name	Connected to	Pin	Signal name	Connected to
1	VI0_R2	P42_5	2	VI0_B2	P43_9
3	+3.3V	+3.3V	4	N.C	-
5	VI0_B3	P43_8	6	VI0_B4	P43_7 / P42_15
7	VI0_B5	P42_14	8	VI0_B6	P42_13
9	VI0_B7	P42_12	10	GND	GND
11	VI0_G2	P42_11	12	VI0_G3	P42_10
13	VI0_G4	P42_9	14	VI0_G5	P42_8
15	VI0_G6	P42_7	16	VI0_G7	P42_6
17	GND	GND	18	VI0_R3	P42_4
19	VI0_R4	P42_3	20	VI0_R5	P42_2
21	VI0_R6	P42_1	22	VI0_R7	P42_0
23	+3.3V	+3.3V	24	N.C	-
25	VI0_HSYNC	P43_11	26	VI0_VSYNC	P43_12
27	VI0_CLK	P43_10	28	SEL_VI0_EN	P43_11
29	GND	GND	30	GND	GND
31	+3.3V	+3.3V	32	VI0_R0	N.C. (Reserved)
33	VI0_R1	N.C. (Reserved)	34	VI0_G0	N.C. (Reserved)
35	VI0_G1	N.C. (Reserved)	36	VI0_B0	N.C. (Reserved)
37	VI0_B1	N.C. (Reserved)	38	N.C	-
39	N.C	-	40	GND	GND

4.3.7 CVBS Analog video input connector (CN38)

This connector is used for CVBS analog video input signals. The signals are converted by an external IC before routing the video signals to RH850/D1x VIN0_ITU.

Table 4-14: CVBS connector (CN38)

Pin	Function	Comment
1	GND	
2	GND	
3	Y (Intensity)	Connected to SAA7113H AI11
4	C (Color)	Connected to SAA7113H AI21

Table 4-15: Signal assignment of the CVBS to ITU video converter IC

Pin Name	Function	Connected to
VPO0	V1CVBS_D0	P43_9
VPO1	V1CVBS_D1	P43_8
VPO2	V1CVBS_D2	P43_7
VPO3	V1CVBS_D3	P43_6
VPO4	V1CVBS_D4	P43_5
VPO5	V1CVBS_D5	P43_4
VPO6	V1CVBS_D6	P43_3
VPO7	V1CVBS_D7	P43_2
SDA	I2C_SDA	P2_0 / P3_0
SCL	I2C_SCL	P2_1 / P3_1
LLC	V1CVBS_CLK	P43_10
RTCO	V1CVBS_CLK	P43_10
RTS1	V1CVBS_VSYNC	P43_12
RTS0	V1CVBS_HSYNC	P43_11

Note: In the default configuration, the CVBS Input (routed to VIN0 ITU) and the VOUT0 connectors share a signal on P43_2. For the CVBS input it is the essential signal V1CVBS_D7. For VOUT0 it is the optional signal DATA_ENABLE.

The following configuration is required if you intend to use the CVBS input in parallel to a display connected to VOUT0, that requires Data Enable (DE). Please use the alternative signal path P42_11 for SEL_VO0DE by connecting JP98-2 and JP99 and change the pin configuration in your software accordingly.

Please check Table 5-6 for a description of the jumper.

4.3.8 Parallel Video input0 Irisoconnector (CN36)

This connector can be used for video input sources supporting this kind of connector.

Table 4-16: pin assignment of IRISO connector0 (CN36)

Pin	Function	Signal name	Connected to
1	GND	GND	
2	+3.3V	+3.3V	
3	GND	GND	
4	VI0_EN	VDCE0_VI_TCON3	P43_11
5	+3.3V	+3.3V	
6	VI0_B7	VDCE0_VI_DATA5	P42_12
7	VI0_B6	VDCE0_VI_DATA4	P42_13
8	VI0_B5	VDCE0_VI_DATA3	P42_14
9	VI0_B4	VDCE0_VI_DATA2	P43_7 / P42_15
10	VI0_B3	VDCE0_VI_DATA1	P43_8
11	VI0_B2	VDCE0_VI_DATA0	P43_9
12	VI0_B1		N.C. (Reserved)
13	VI0_B0		N.C. (Reserved)
14	GND	GND	
15	VI0_G7	VDCE0_VI_DATA11	P42_6
16	VI0_G6	VDCE0_VI_DATA10	P42_7
17	VI0_G5	VDCE0_VI_DATA9	P42_8
18	VI0_G4	VDCE0_VI_DATA8	P42_9
19	VI0_G3	VDCE0_VI_DATA7	P42_10
20	VI0_G2	VDCE0_VI_DATA6	P42_11
21	VI0_G1		N.C. (Reserved)
22	VI0_G0		N.C. (Reserved)
23	GND	GND	
24	VI0_R7	VDCE0_VI_DATA17	P42_0
25	VI0_R6	VDCE0_VI_DATA16	P42_1
26	VI0_R5	VDCE0_VI_DATA15	P42_2
27	VI0_R4	VDCE0_VI_DATA14	P42_3
28	VI0_R3	VDCE0_VI_DATA13	P42_4
29	VI0_R2	VDCE0_VI_DATA12	P42_5
30	VI0_R1		N.C. (Reserved)
31	VI0_R0		N.C. (Reserved)
32	GND	GND	
33	VI0_CLK	VDCE0_VI_CLKP	P43_10
34	GND	GND	
35	VI0_VSYNC	VDCE0_VI_VSYNC	P43_12
36	VI0_HSYNC	VDCE0_VI_HSYNC	P43_11
37	VI0_CLKN		N.C.
38	GND	GND	
39	GND	GND	
40	+3.3V	+3.3V	
41	VI0_PWM	GPIO / TAUB0I6 / TAUB0O6	P1_10
42	N.C.	N.C.	
43	N.C.	N.C.	
44	GND	GND	
45	VI0_SDA	RIIC1SDA / RIIC0SDA	P2_0 / P3_0
46	VI0_SCL	RIIC1SCL / RIIC0SCL	P2_1 / P3_1
47	N.C.	N.C.	
48	N.C.	N.C.	
49	VI0_GPIO0	GPIO / TAUB0I7 / TAUB0O7	P1_11
50	GND	GND	

4.3.9 VIN1 ITUconnector (CN37)

This connector is used for Camera module or equipment with ITU video input.

Table 4-17: VIN1 ITU connector (CN37)

Pin	Function	Signal name	Connected to
1	+12V	+12V	
2	VI1ITU_D0	VDCE1_VI_DATA0_ITU	P43_9
3	GND	GND	
4	VI1ITU_D1	VDCE1_VI_DATA1_ITU	P43_8
5	+3.3V	+3.3V	
6	VI1ITU_D2	VDCE1_VI_DATA2_ITU	P43_7
7	GND	GND	
8	VI1ITU_D3	VDCE1_VI_DATA3_ITU	P46_4
9	GND	GND	
10	VI1ITU_D4	VDCE1_VI_DATA4_ITU	P46_3
11	VI1ITU_CLK	VDCE1_VI_CLK	P43_10
12	VI1ITU_D5	VDCE1_VI_DATA5_ITU	P46_2
13	VI1ITU_HSYNC	VDCE1_VI_HSYNC	P43_11
14	VI1ITU_D6	VDCE1_VI_DATA6_ITU	P46_1
15	VI1ITU_VSYNC	VDCE1_VI_VSYNC	P43_12
16	VI1ITU_D7	VDCE1_VI_DATA7_ITU	P46_0

4.4 Example: How to configure the board for a display on VO0/LCBI

The following procedure should show, what switches have to be configured to connect a display to the parallel 40pin video output 0. The display to be used in this example does not need a data enable signal. The display to be used has an integrated controller that needs to be programmed via CSI before use.

1. Set up the multiplexers
 - o Turn ON the Mux “RSDS_SEL” on the Adapter Board to connect the MCU to the Main Board rather than to the RSDS connector. (Applies to D1M2(H) Adapter Board only.)
 - o Turn ON the Mux “VO0MUX_SEL1” on the Main Board to connect the MCU Pins to the Video function block rather than the VG connector
 - o Turn ON the Mux “VO0MUX_SEL2” on the Main Board to connect the MCU Pins to the parallel Video connectors (CN44 and CN45) rather than the HDMI video output (CN49).
2. Configure the jumpers
 - o As we do not need the Data Enable signals, either leave open JP90, JP91 or both.
3. Connect the display
 - o Connect the CSI connector, so the display can be configured before use.
 - o Connect the 40-pin parallel video connector for video data and timing signals.

5 Multiplex Control

5.1 Overview

Due to the amount of different functions provided by the MCU, many pins are used for two or more functions. In order to test all of these functions, it is required to multiplex the function blocks on the Mango Board. The multiplexing scheme of the main board is controlled by a dedicated DIP switch (DSW31). The DIP switch DSW31 has eight switches. Their function is described in Table 5-1. Please note the Video Output Muxing switches for each VO0 and VO1 are cascaded. If the Video Output is selected on the first muxer “_SEL1”, it is also required to configure the following muxer “_SEL2”.

Table 5-1: Function of each of the eight switches of DSW31

SW	Function name	Source block	Target block	
			SW “OFF”	SW “ON”
1	N.C.			
2	N.C.			
3	AUDIOMUX_SEL	MCU	H-Bridge	I2S-DAC
4	VINMUX_SEL	MCU	VG-Connector	V1CVBS
5	VO1MUX_SEL2	VO1MUX_SEL1	HDMI-Output	Parallel Video Input / Output (40pol / Iriso connectors)
6	VO1MUX_SEL1	MCU	VG-Connector	VO1-Mux “VO1MUX_SEL2”
7	VO0MUX_SEL2	VO0MUX_SEL1	HDMI-Output	Parallel Video Output (40pol / Iriso connectors)
8	VO0MUX_SEL1	MCU	VG-Connector	VO0-Mux “VO0MUX_SEL2”

Note: Another switch may be located on the adapter boards. For the D1M2H, these are DSW1 and DSW2. Please also consider the position of these switches when configuring the Mango Board!

In addition to the “main” multiplexers, which switch between the function blocks, there are more jumpers that are available within each function block. These jumpers are used to select alternative functions of certain signals and are described in the respective chapters.

5.2 Video MUX

The following chapter contains information about the signal paths though the muxes.

5.2.1 Muxing of VO0

For the signals P43_0, P43_1, P44_0 to P44_11 and P45_0 to P45_13, there are three different muxing-targets available. The signals can be muxed to the VG-connector in order to use them as low-speed GPIOs, or they can either be routed to the parallel video output connectors “VO0/LCBI” and “VO0/ZIF” or the the HDMI video ouput “VO0 HDMI”.

Table 5-2: Part (A) of Signal list for Mux “VO0MUX_SEL1” DSW31.8 (U36)

Pin	VO0MUX_SEL1: ON		OFF
	Function	Signal name	Function
P44_0	SEL_P44_0	VDCE0_VO_DATA23	VG_P44_0
P44_1	SEL_P44_1	VDCE0_VO_DATA22	VG_P44_1
P44_2	SEL_P44_2	VDCE0_VO_DATA21	VG_P44_2
P44_3	SEL_P44_3	VDCE0_VO_DATA20	VG_P44_3
P44_4	SEL_P44_4	VDCE0_VO_DATA19	VG_P44_4
P44_5	SEL_P44_5	VDCE0_VO_DATA18	VG_P44_5
P44_6	SEL_P44_6	VDCE0_VO_DATA17	VG_P44_6
P44_7	SEL_P44_7	VDCE0_VO_DATA16	VG_P44_7
P44_8	SEL_P44_8	VDCE0_VO_DATA15	VG_P44_8
P44_9	SEL_P44_9	VDCE0_VO_DATA14	VG_P44_9
P44_10	SEL_P44_10	VDCE0_VO_DATA13	VG_P44_10
P44_11	SEL_P44_11	VDCE0_VO_DATA12	VG_P44_11
P45_0	SEL_P45_0	VDCE0_VO_CLKP	VG_P45_0
P45_1	SEL_P45_1	VDCE0_VO_CLKN	VG_P45_1
P45_2	SEL_P45_2	VDCE0_VO_DATA11	VG_P45_2
P45_3	SEL_P45_3	VDCE0_VO_DATA10	VG_P45_3

Table 5-3: Part (B) of Signal list for Mux “VO0MUX_SEL1” DSW31.8 (U37)

Pin	VO0MUX_SEL1: ON		OFF
	Function	Signal name	Function
P45_4	SEL_P45_4	VDCE0_VO_DATA9	VG_P45_4
P45_5	SEL_P45_5	VDCE0_VO_DATA8	VG_P45_5
P45_6	SEL_P45_6	VDCE0_VO_DATA7	VG_P45_6
P45_7	SEL_P45_7	VDCE0_VO_DATA6	VG_P45_7
P45_8	SEL_P45_8	VDCE0_VO_DATA5	VG_P45_8
P45_9	SEL_P45_9	VDCE0_VO_DATA4	VG_P45_9
P45_10	SEL_P45_10	VDCE0_VO_DATA3	VG_P45_10
P45_11	SEL_P45_11	VDCE0_VO_DATA2	VG_P45_11
P45_12	SEL_P45_12	VDCE0_VO_DATA1	VG_P45_12
P45_13	SEL_P45_13	VDCE0_VO_DATA0	VG_P45_13
P43_0	SEL_P43_0	VDCE0_VO_HSYNC	VG_P43_0
P43_1	SEL_P43_1	VDCE0_VO_VSYNC	VG_P43_1
N.C.			

Table 5-4: Part (A) of Signal list for Mux “VO0MUX_SEL2” DSW31.7 (U34)

Pin	VO0MUX_SEL2: ON		OFF
	Function		Function
SEL_P45_13	VO0_B0		VO0HDMI_B0
SEL_P45_12	VO0_B1		VO0HDMI_B1
SEL_P45_11	VO0_B2		VO0HDMI_B2
SEL_P45_10	VO0_B3		VO0HDMI_B3
SEL_P45_9	VO0_B4		VO0HDMI_B4
SEL_P45_8	VO0_B5		VO0HDMI_B5
SEL_P45_7	VO0_B6		VO0HDMI_B6
SEL_P45_6	VO0_B7		VO0HDMI_B7
SEL_P45_5	VO0_G0		VO0HDMI_G0
SEL_P45_4	VO0_G1		VO0HDMI_G1
SEL_P45_3	VO0_G2		VO0HDMI_G2
SEL_P45_2	VO0_G3		VO0HDMI_G3
SEL_P44_11	VO0_G4		VO0HDMI_G4
SEL_P44_10	VO0_G5		VO0HDMI_G5
SEL_P44_9	VO0_G6		VO0HDMI_G6
SEL_P44_8	VO0_G7		VO0HDMI_G7

Table 5-5: Part (B) of Signal list for Mux “VO0MUX_SEL2” DSW31.7 (U35)

Pin	VO0MUX_SEL2: ON		OFF
	Function		Function
SEL_P44_7	VO0_R0		VO0HDMI_R0
SEL_P44_6	VO0_R1		VO0HDMI_R1
SEL_P44_5	VO0_R2		VO0HDMI_R2
SEL_P44_4	VO0_R3		VO0HDMI_R3
SEL_P44_3	VO0_R4		VO0HDMI_R4
SEL_P44_2	VO0_R5		VO0HDMI_R5
SEL_P44_1	VO0_R6		VO0HDMI_R6
SEL_P44_0	VO0_R7		VO0HDMI_R7
SEL_P43_0	VO0_HSYNC		VO0HDMI_HSYNC
SEL_P43_1	VO0_VSYNC		VO0HDMI_VSYNC
SEL_P45_0	VO0_CLKP		VO0HDMI_CLKP
SEL_P45_1	VO0_CLKN		
SEL_VO0DE	VO0_EN		VO0HDMI_EN
N.C.			
N.C.			
N.C.			

Single-Jumper Settings for VO0

The following table provides a list of single jumpers for the configuration of VO0 signals or the selection of alternative functions. Jumper positions that are **printed in bold**, highlight signals, that are routed over another muxer than VO0MUX or over no mux at all. For these signals, please make sure, that the voltage levels and signal directions match the intended use.

Table 5-6: Single jumpers to select alternative functions for signals of VO0

Jumper	Name	Default Position	Alternative Positions	Description
JP98 / JP99 (SEL_VO0DE)	VO0 Select Data Enable 1	JP98 2-3 (P43_2)	JP98 2-1 (SEL_P43_0) JP98-2 JP99 (P42_11)	Select among different sources of the Data Enable signal.
JP96 (VO0HDMI_EN)	VO0/HDMI DataEnable	open	VO0HDMI_EN	Activate Data Enable Signal for VO0 HDMI
JP97 (I2C_SCL/SDA)	VO0/HDMI I2C	open	I2C_SCL / _SDA	Activate I2C-connection to HDMI connector
JP91 (SEL_VO0_EN)	VO0 Select Data Enable 2	2-3 (SEL_VO0DE)	1-2 (VO0_HSYNC)	Select among different sources of the Data Enable signal.
JP90 (SEL_VO0_EN)	VO0/LCBI DataEnable	open	SEL_VO0_EN	Activate Data Enable Signal for VO0/LCBI
JP92 (SEL_VO0_EN)	VO0/ZIF DataEnable	open	SEL_VO0_EN	Activate Data Enable Signal for VO0/ZIF
JP93 (VO0_PWM)	VO0/ZIF PWM	open	P1_6	Activate PWM signal for VO0/ZIF
JP94 (VO0_GPIO)	VO0/ZIF GPIO	open	P1_7	Activate GPIO signal for VO0/ZIF
JP95 (I2C_SCL/SDA)	VO0/ZIF I2C	open	I2C_SCL / _SDA	Activate I2C-connection to VO0/ZIF

5.2.2 Muxing of VO1

For the signals P46_0 to P46_15 and P47_0 to P47_X2, there are three different muxing-targets available. The signals can be muxed to the VG-connector in order to use them as low-speed GPIOs, or they can either be routed to the parallel video output connectors “VO1/V1” and “VO1/ZIF” or the the HDMI video ouput “VO1 HDMI”.

Table 5-7: Part (A) of Signal list for Mux “VO1MUX_SEL1” DSW31.6 (U28)

Pin	VO1MUX_SEL1: ON		OFF
	Function	Signal name	Function
P46_0	SEL_P46_0	VDCE1_VO_DATA23	VG_P46_0
P46_1	SEL_P46_1	VDCE1_VO_DATA22	VG_P46_1
P46_2	SEL_P46_2	VDCE1_VO_DATA21	VG_P46_2
P46_3	SEL_P46_3	VDCE1_VO_DATA20	VG_P46_3
P46_4	SEL_P46_4	VDCE1_VO_DATA19	VG_P46_4
P46_5	SEL_P46_5	VDCE1_VO_DATA18	VG_P46_5
P46_6	SEL_P46_6	VDCE1_VO_DATA17	VG_P46_6
P46_7	SEL_P46_7	VDCE1_VO_DATA16	VG_P46_7
P46_8	SEL_P46_8	VDCE1_VO_DATA15	VG_P46_8
P46_9	SEL_P46_9	VDCE1_VO_DATA14	VG_P46_9
P46_10	SEL_P46_10	VDCE1_VO_DATA13	VG_P46_10
P46_11	SEL_P46_11	VDCE1_VO_DATA12	VG_P46_11
P46_12	SEL_P46_12	VDCE1_VO_DATA11	VG_P46_12
P46_13	SEL_P46_13	VDCE1_VO_DATA10	VG_P46_13
P46_14	SEL_P46_14	VDCE1_VO_DATA9	VG_P46_14
P46_15	SEL_P46_15	VDCE1_VO_DATA8	VG_P46_15

Table 5-8: Part (B) of Signal list for Mux “VO1MUX_SEL1” DSW31.6 (U29)

Pin	Function	VO1MUX_SEL1: ON	OFF
		Signal name	Function
P47_0	SEL_P47_0	VDCE1_VO_DATA7	VG_P47_0
P47_1	SEL_P47_1	VDCE1_VO_DATA6	VG_P47_1
P47_2	SEL_P47_2	VDCE1_VO_DATA5	VG_P47_2
P47_3	SEL_P47_3	VDCE1_VO_DATA4	VG_P47_3
P47_4	SEL_P47_4	VDCE1_VO_DATA3	VG_P47_4
P47_5	SEL_P47_5	VDCE1_VO_DATA2	VG_P47_5
P47_6	SEL_P47_6	VDCE1_VO_DATA1	VG_P47_6
P47_7	SEL_P47_7	VDCE1_VO_DATA0	VG_P47_7
P47_8	SEL_P47_8	VDCE1_VO_CLK	VG_P47_8
P47_9	SEL_P47_9	VDCE1_VO_HSYNC	VG_P47_9
P47_10	SEL_P47_10	VDCE1_VO_VSYNC	VG_P47_10
P47_X1	SEL_P47_X1		VG_P47_X1
P47_X2	SEL_P47_X2		VG_P47_X2
N.C.			
N.C.			
N.C.			

Table 5-9: Part (A) of Signal list for Mux “VO1MUX_SEL2” DSW31.5 (U26)

Pin	VO1MUX_SEL2: ON	OFF
	Function	Function
SEL_P47_7	VO1_B0	VO1HDMI_B0
SEL_P47_6	VO1_B1	VO1HDMI_B1
SEL_P47_5	VO1_B2	VO1HDMI_B2
SEL_P47_4	VO1_B3	VO1HDMI_B3
SEL_P47_3	VO1_B4	VO1HDMI_B4
SEL_P47_2	VO1_B5	VO1HDMI_B5
SEL_P47_1	VO1_B6	VO1HDMI_B6
SEL_P47_0	VO1_B7	VO1HDMI_B7
SEL_P46_15	VO1_G0	VO1HDMI_G0
SEL_P46_14	VO1_G1	VO1HDMI_G1
SEL_P46_13	VO1_G2	VO1HDMI_G2
SEL_P46_12	VO1_G3	VO1HDMI_G3
SEL_P46_11	VO1_G4	VO1HDMI_G4
SEL_P46_10	VO1_G5	VO1HDMI_G5
SEL_P46_9	VO1_G6	VO1HDMI_G6
SEL_P46_8	VO1_G7	VO1HDMI_G7

Table 5-10: Part (B) of Signal list for Mux “VO1MUX_SEL2” DSW31.5 (U27)

Pin	VO1MUX_SEL2: ON	OFF
	Function	Function
SEL_P46_7	VO1_R0	VO1HDMI_R0
SEL_P46_6	VO1_R1	VO1HDMI_R1
SEL_VIO1_5	VO1_R2	VO1HDMI_R2
SEL_VIO1_4	VO1_R3	VO1HDMI_R3
SEL_VIO1_3	VO1_R4	VO1HDMI_R4
SEL_VIO1_2	VO1_R5	VO1HDMI_R5
SEL_VIO1_1	VO1_R6	VO1HDMI_R6
SEL_VIO1_0	VO1_R7	VO1HDMI_R7
SEL_P47_9	VO1_HSYNC	VO1HDMI_HSYNC
SEL_P47_10	VO1_VSYNC	VO1HDMI_VSYNC
SEL_P47_8	VO1_CLK	VO1HDMI_CLK
SEL_VO1DE	VO1_EN	VO1HDMI_EN
N.C.		

Single-Jumper Settings for VO1

The following table provides a list of single jumpers for the configuration of VO0 signals or the selection of alternative functions. Jumper positions that are printed in bold, highlight signal, that are routed over another muxer than VO0MUX or over no mux at all. For these signals, please make sure, that the voltage levels and signal directions match the intended use.

Table 5-11: Single jumpers to select alternative functions for signals of VO0

Jumper	Name	Default Position	Alternative Positions	Description
JP84 (SEL_VIO1_0)	SEL_VIO1_0	2-3 (SEL_P46_0)	1-2 (P43_7)	Select among different sources of the Data signal.
JP85 (SEL_VIO1_1)	SEL_VIO1_1	2-3 (SEL_P46_1)	1-2 (P43_8)	Select among different sources of the Data signal.
JP86 (SEL_VIO1_2)	SEL_VIO1_2	2-3 (SEL_P46_2)	1-2 (P43_9)	Select among different sources of the Data signal.
JP87 (SEL_VIO1_3)	SEL_VIO1_3	2-3 (SEL_P46_3)	1-2 (P43_10)	Select among different sources of the Data signal.
JP88 (SEL_VIO1_4)	SEL_VIO1_4	2-3 (SEL_P46_4)	1-2 (P43_11)	Select among different sources of the Data signal.
JP89 (SEL_VIO1_5)	SEL_VIO1_5	2-3 (SEL_P46_5)	1-2 (P43_12)	Select among different sources of the Data signal.
JP82 / JP83 (SEL_VO1DE)	VO1 Select Data Enable 1	JP83-1 JP82-2 (SEL_VIO1_0)	JP82 2-1 (SEL_P47_9) JP82 2-3 (SEL_P47_X2)	Select among different sources of the Data Enable signal.
JP80 (VO1HDMI_EN)	VO1/HDMI DataEnable	open	VO1HDMI_EN	Activate Data Enable Signal for VO1 HDMI
JP81 (I2C_SCL/SDA)	VO1/HDMI I2C	open	I2C_SCL / _SDA	Activate I2C-connection to HDMI connector
JP75 (SEL_VO1_EN)	VO1 Select Data Enable 2	2-3 (VO1EN)	1-2 (VO1_HSYNC)	Select among different sources of the Data Enable signal.
JP74 (SEL_VO1_EN)	VO1/VI1 DataEnable	open	SEL_VO1_EN	Activate Data Enable Signal for VO1/VI1
JP76 (SEL_VO1_EN)	VO1/ZIF DataEnable	open	SEL_VO1_EN	Activate Data Enable Signal for VO1/ZIF
JP77 (VO0_PWM)	VO1/ZIF PWM	open	P1_8	Activate PWM signal for VO1/ZIF
JP78 (VO0_GPIO0)	VO1/ZIF GPIO	open	P1_9	Activate GPIO signal for VO1/ZIF
JP79 (I2C_SCL/SDA)	VO1/ZIF I2C	open	I2C_SCL / _SDA	Activate I2C-connection to VO1/ZIF

5.2.3 Muxing of VI1/CVBS

For the signals P43_2 to P43_12 there are two different muxing-targets available. The signals can be muxed to the VG-connector in order to use them as low-speed GPIOs or they can be routed to the video input converter IC on VI1 to convert CVBS signals to ITU signals.

To use the video input converter IC, one additional step has to be done. As the signals P43_3 to P43_6 may also be used for other video function blocks of the mango board, these signals are detachable by a DIP switch (DSW30). To use the video input, please turn on all four switches of DSW30.

Table 5-12: Signal list for Mux “VINMUX_SEL” DSW31.4 (U23)

Pin	Function	VINMUX_SEL1: ON	OFF
		Signal name	Function
P43_2	V1CVBS_D7	VDCE1_VI_DATA7	VG_P43_2
P43_3	V1CVBS_D6	VDCE1_VI_DATA6	VG_P43_3
P43_4	V1CVBS_D5	VDCE1_VI_DATA5	VG_P43_4
P43_5	V1CVBS_D4	VDCE1_VI_DATA4	VG_P43_5
P43_6	V1CVBS_D3	VDCE1_VI_DATA3	VG_P43_6
P43_7	V1CVBS_D2	VDCE1_VI_DATA2	VG_P43_7
P43_8	V1CVBS_D1	VDCE1_VI_DATA1	VG_P43_8
P43_9	V1CVBS_D0	VDCE1_VI_DATA0	VG_P43_9
P43_10	V1CVBS_CLK	VDCE1_VI_CLK	VG_P43_10
P43_11	V1CVBS_HSYNC	VDCE1_VI_HSYNC	VG_P43_11
P43_12	V1CVBS_VSYNC	VDCE1_VI_VSYNC	VG_P43_12
N.C.			

Single-Jumper Settings for VI1/CVBS

The following table provides a list of single jumpers for the configuration of VI1 signals or the selection of alternative functions. Jumper positions that are printed in bold, highlight signal, that are routed over another muxer than VINMUX or over no mux at all. For these signals, please make sure, that the voltage levels and signal directions match the intended use.

Table 5-13: Single jumpers to select alternative functions for signals of VI1/CVBS

Jumper	Name	Default Position	Alternative Positions	Description
JP70 (SEL_TCON0_1)	SEL_TCON0_1	1-2 (P43_3)	2-3 (P42_12)	Select among different sources of the TCON0_1 signal.
JP71 (SEL_TCON0_4)	SEL_TCON0_4	1-2 (P43_4)	2-3 (P42_13)	Select among different sources of the TCON0_4 signal.
JP72 (SEL_TCON0_5)	SEL_TCON0_5	1-2 (P44_5)	2-3 (P42_14)	Select among different sources of the TCON0_5 signal.
JP73 (SEL_TCON0_6)	SEL_TCON0_6	1-2 (P44_6)	2-3 (P42_115)	Select among different sources of the TCON0_6 signal.

5.2.4 Muxing of VIO/MIPI

The MCU Pins P40_0 to P40_X4 are dedicated to be used only for the MIPI Interface, so no muxing is required.

5.2.5 Muxing of VIO/Parallel Input

For the signals P42_0 to P42_15 and P43_7 to P43_12 there is only one muxing-target available. So there is no muxing IC. The signals of the connectors VIO and VIO/ZIF are routed directly to the MCU. For six signals, the lower two bits of R, G and B, the connection is kept open, as the parallel VIO was designed as RGB666 video input. Nevertheless, these signals are routed to the adapter board connector to be available for future versions of the D1x devices.

Single-Jumper Settings for VO0

The following table provides a list of single jumpers for the configuration of VIO signals or the selection of alternative functions. Jumper positions that are printed in bold, highlight signals that are routed over a muxer. For these signals, please make sure, that the voltage levels and signal directions match the intended use.

Table 5-14: Single jumpers to select alternative functions for signals of VO0

Jumper	Name	Default Position	Alternative Positions	Description
JP65 (VIO_EN)	VIO Select Data Enable 1	open	P43_11	Select select HSYNC line as target of the Data Enable signal.
JP64 (VIO_EN)	VIO DataEnable	open	VIO_EN	Activate Data Enable Signal for VIO
JP66 (VIO_EN)	VIO/ZIF DataEnable	open	VIO_EN	Activate Data Enable Signal for VIO/ZIF
JP106 (VIO_B4)	VIO B4	2-3 (P42_15)	1-2 (P43_7)	Select among different targets for the Blue Data signal.
JP67 (VIO_PWM)	VIO/ZIF PWM	open	P1_10	Activate PWM signal for VIO/ZIF
JP68 (VIO_GPIO0)	VIO/ZIF GPIO	open	P1_11	Activate GPIO signal for VIO/ZIF
JP69 (I2C_SCL/SDA)	VIO/ZIF I2C	open	I2C_SCL / _SDA	Activate I2C-connection to VIO/ZIF

5.2.6 Muxing of VI1/ITU

For the ITU signals there is only one muxing-target available on the main board. So there is no muxing IC. The signals of the connectors VI1/ITU to the adapter board. On the adapter board, the ITU signals are muxed with P43_7 to P43_12 and P46_0 to P46_4. The signals P43_7 to P43_12 and P46_0 to P46_4 are routed to the main board for further muxing, if required.

Table 5-15: Signal list for Mux “VI1ITU_SEL” on the Adapter Board

Pin	Function	VINMUX_SEL= OFF	ON
		Signal name	Function
MCU_P43_7	VI1ITU_D2	VDCE0_VI_DATA2	P43_7
MCU_P43_8	VI1ITU_D1	VDCE0_VI_DATA1	P43_8
MCU_P43_9	VI1ITU_D0	VDCE0_VI_DATA0	P43_9
MCU_P43_10	VI1ITU_CLK	VDCE0_VI_CLK	P43_10
MCU_P43_11	VI1ITU_HSYNC	VDCE0_VI_HSYNC	P43_11
MCU_P43_12	VI1ITU_VSYNC	VDCE0_VI_VSYNC	P43_12
MCU_P46_0	VI1ITU_D7	VDCE0_VI_DATA7	P46_0
MCU_P46_1	VI1ITU_D6	VDCE0_VI_DATA6	P46_1
MCU_P46_2	VI1ITU_D5	VDCE0_VI_DATA5	P46_2
MCU_P46_3	VI1ITU_D4	VDCE0_VI_DATA4	P46_3
MCU_P46_4	VI1ITU_D3	VDCE0_VI_DATA3	P46_4
N.C.			

6 Tool I/F function Block

6.1 Overview

The Tool I/F function Block is composed of the E1 connector (CN16) and the pull-up / pull-down Control switches. The E1 connector can be used to connect the Renesas E1 emulator and the Renesas Flash Programmer PG-FP5.

The E1 connector is designed to support different programming and debug interfaces and protocols of the MCU.

- Software debug by E1 emulator (LPD 1-pin or LPD 4-pin interface)
- Renesas Flash programmer PG-FP5 in order to program targeted MCU internal Flash (UART 1-pin or UART 2-pin or CSI 3-pin interface)
- Software debug by 3rd party JTAG emulator

For the latest software for the Renesas programming tools, please visit the Renesas website.

NOTE: For Renesas Flash Programmer V2.04.00 (2014-04-07) or newer, please visit the following link.

http://japan.renesas.com/products/tools/flash_programming/rfp/downloads.jsp

http://www.renesas.eu/products/tools/flash_prom_programming/rfp/downloads.jsp

(Alternative)

6.2 Schematic

Figure 6-1 shows the schematic of the tool interface function block. The switches shown in the schematic below are 3-position switches (Pull-Up / Open / Pull-Down). The default position of each switch for the connection of the programming tools is written next to each switch symbol and also shown in Table 6-1. The schematic shows two connectors. The E1 connector is CN16. The connector CN15 gives access to the two Mode-Pins of the MCU. This connector is not required for normal programming or operation.

In order to deactivate the reset signal of the debugger, the Jumper JP19 can be opened. A reset can still be triggered by manually pressing the reset button SW11.

Table 6-1: Default Switch positions for debugging and programming the MCU

Switch (sorted top to bottom)	Location	Switch Position
SW3	Between VG connectors (top)	Pull-Up
SW5	Between VG connectors (below SW3)	Open
SW9	Between VG connectors (below SW5)	Open
SW2	Between VG connectors (below SW9)	Pull-Up
SW7	Between VG connectors (below SW2)	Pull-Down
SW1	Between VG connectors (below SW7)	Open
SW4	Between VG connectors (below SW1)	Open
SW6	Between VG connectors (below SW4)	Pull-Down
SW8	Between VG connectors (below SW6)	Open
SW10	Next to E1 connector	Pull-Down

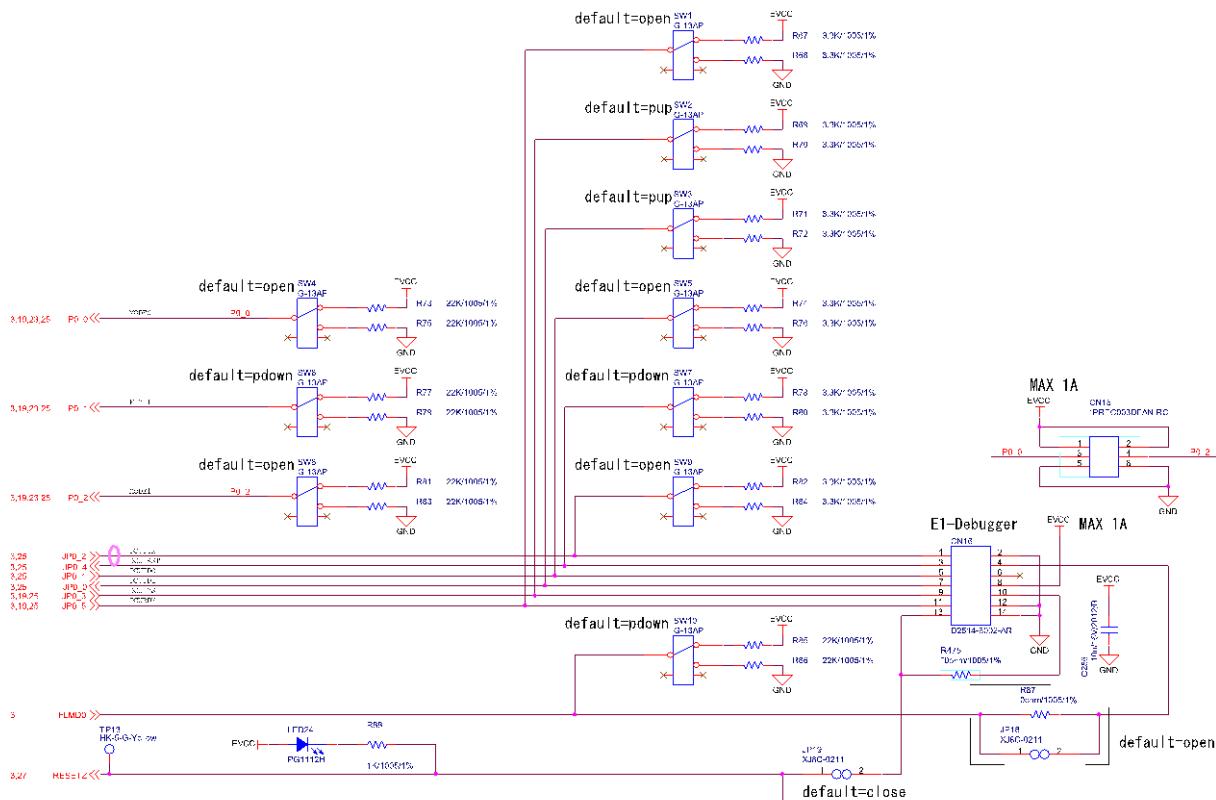


Figure 6-1: Schematic of tool I/F function block

6.3 E1 Connector interface

Table 6-2 and Figure 6-2 show the pin assignment of the E1 connector with respect to the different protocols supported by the MCU.

Table 6-2: E1 connector (CN16) pin assignment

Pin	Connected to	E1 emulator LPD I/O	Function	JTAG I/F I/O	Function	Serial programming I/O	Function
1	JP0_2	O	LPCLK	O	TCK	O	FPCK
2	GND	-	GND	-	GND	-	GND
3	JP0_4	O	TRST	O	TRST	-	N.C.
4	FLMD0	-	N.C.	-	N.C.	O	FPMD0
5	JP0_1	I	LPDO	I	TDO	I	FPDT
6	N.C.	-	N.C.	-	N.C.	O	FPMD1
7	JP0_0	I/O	LPDIO	O	TDI	I/O	FPDR
8	EVCC	I	TVDD	I	TVDD	I/O	TVDD
9	JP0_3	-	N.C.	O	TMS	-	N.C.
10	N.C.	-	N.C.	-	N.C.	-	N.C.
11	JP0_5	I	LPDCLKO	I	RDY	-	N.C.
12	GND	-	GND	-	GND	-	GND
13	_RESET	I/O	RESET	I/O	RESET	I/O	RESET
14	GND	-	GND	-	GND	-	GND

Figure 6-2 shows the same pull-up / pull-down configuration as the schematic above.

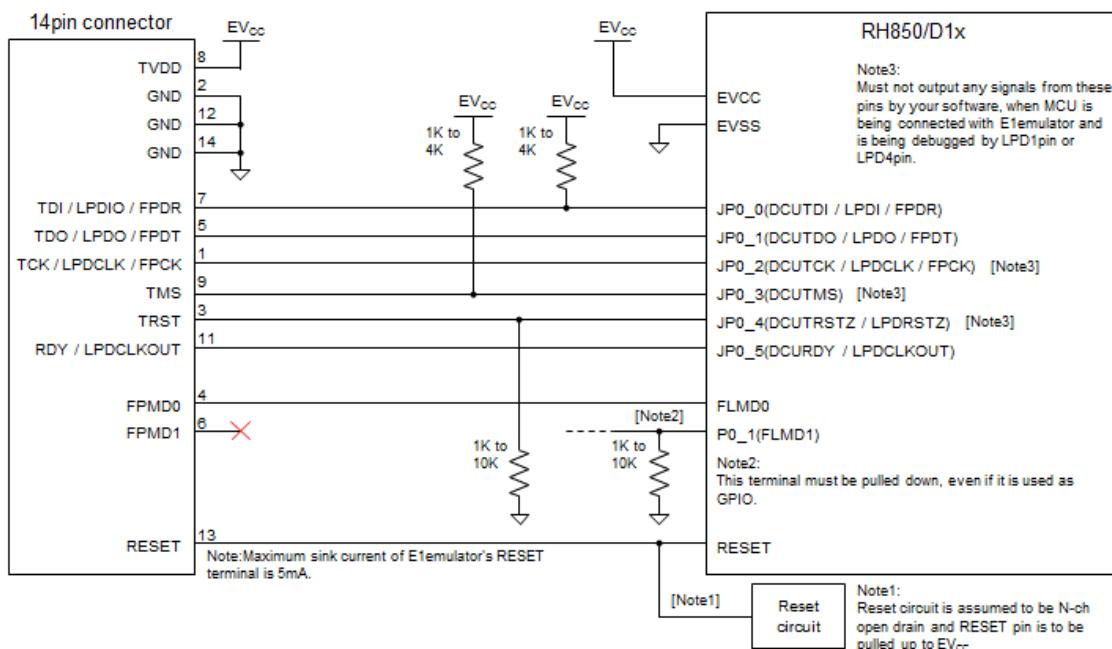


Figure 6-2: Tool connection with RH850/D1x

For latest and detailed information about the E1 Connector Interface, please check the “E1/E20 Emulator Users Manual” as well as the additional document “Notes on Connection of RH850/D1L and RH850/D1M”. Both Documents can be found in the documentation Section of “E1 [R0E000010KCE00]” on the Renesas webpage.

7 Reset function

The reset of the Mango board is splitted into two parts that are combined at the reset circuit. The parts are the MCU reset and the Board reset. Both resets can be triggered by a dedicated button that is connected to a dedicated reset generation IC. The MCU reset can be detached from the on board reset circuit by opening a jumper.

7.1 Overview

- Hardware reset button SW11 (micro switch)
- Open-drain reset signal generator U15 with 100ms hold-time and automatic reset generation for a supply voltage below 2.7V
- LED24 to indicate the reset pin level (LED is on, when reset is asserted)
- Jumper JP20 to decouple the MCU reset from the reset logic.
- Pull-up resistor on reset pin (to hold reset inactive when the reset logic is decoupled)
- Debug I/F is able to assert the reset with the possibility to decouple the reset by jumper JP19

Figure 7-1 shows schematic of the reset signal connection.

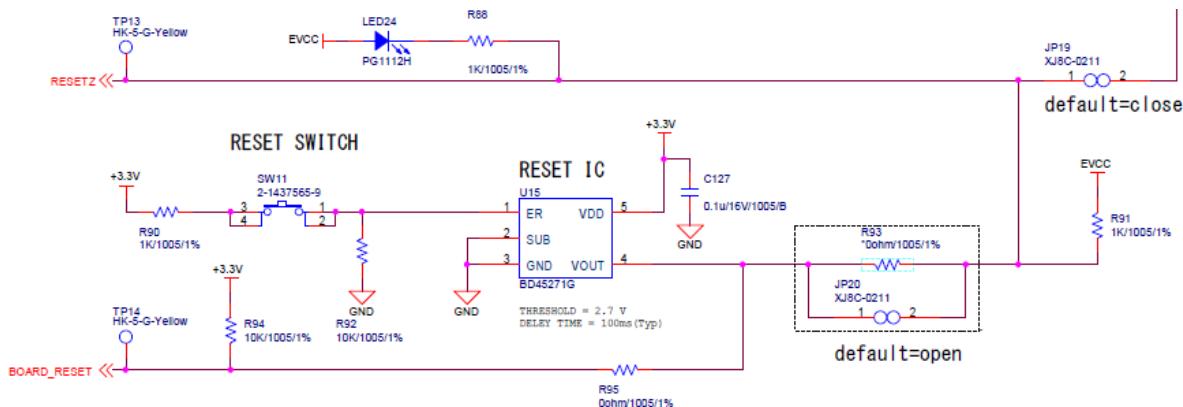


Figure 7-1: Schematic of the on-board reset logic

8 Power supply block

The D1x Mango board has several power domains that can be configured individually. There are four main supply voltages that can be distributed to each of the power domain as required for the desired application. The available voltages are 3.3V and 5V either as Always-On (AWO) voltage or as switched (ISO) voltages that is controlled by the MCU's PWRCTL pin.

8.1 Power supply structure

There are several supply pin in RH850/D1x as shown below.

- Logic supply (ISOVDD)
- Internal regulator supply (REG0VCC, REG1VCC, PLLVCC)
- I/O supply (EVCC, BnVCC(n=0-4), RVCC, MVCC, SFVCC, ISMVCC)
- Analog function supply (A0VCC, A0VREF, ZPDVCC, ZPDVREF)

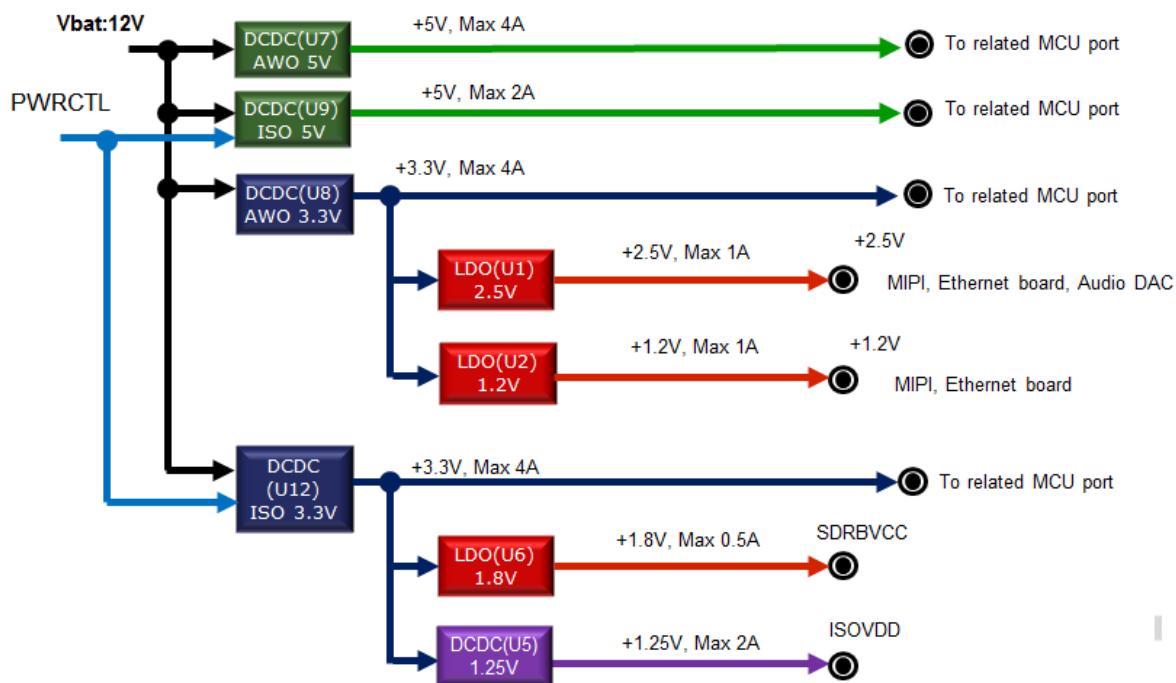


Figure 8-1: Power supply block diagram

The following Table 8-1 and Table 8-2 list all available power domains, separated by I/O port and non-I/O port power supplies.

Table 8-1: MCU Power domains excluding I/O port power domains

Name of Supply	Position	Function
REG0VCC	JP11	AWO digital circuits via on-chip voltage regulator; nominal 3.3 V and 5 V
OSCVCC	JP12	MainOsc and SubOsc; nominal 3.3 V and 5 V
REG1VCC	JP	Flash memory, nominal 3.3 V and 5 V ¹
PLLVCC	JP	PLL, 3.3 V and 5 V
ISOVDD	JP	ISO digital circuits, nominal 1.25 V
ZPDVCC	JP13	Zero point detection circuit; nominal 5 V
ZPDVREF		Reference voltage of Zero Point detection, nominal 5V
A0VREF	JP16	Reference voltage of A/D Converter, nominal 3.3V and 5V

Table 8-2: I/O port power domains

Name of Supply	Position	Ports	Function
EVCC	JP14	P0, JP0	Port buffers supply, nominal 3.3 V and 5 V
B0VCC	JP4	P1, P2	Port buffers supply, nominal 3.3 V and 5 V
B1VCC	JP5	P3	Port buffers supply, nominal 3.3 V and 5 V
B2VCC	JP6	P43_0 to _6, P46, P47	Port buffers supply, nominal 3.3 V and 5 V
B3VCC	JP7	P43_7 to _12	Port buffers supply, nominal 3.3 V and 5 V
B4VCC	JP8	P42	Port buffers supply, nominal 3.3 V and 5 V
RVCC	JP3	P44, P45	RSDS Port buffers supply, nominal 3.3 V and 5V.
MVCC	JP10	P40	MIPI I/F Port buffers supply, nominal 3.3 V
SFVCC	JP15	P21	Serial flash and MLB Port buffers supply, nominal 3.3 V and 5V.
ISMVCC	JP9	P16, P17	Stepper Motor Controller/Driver Port buffers supply • nominal 5 V when used for stepper motor operation • nominal 3.3 V and 5 V when not used for stepper motor operation
A0VCC	JP16	P10, P11	A/D Converter analog circuits and input port buffers supply, nominal 3.3 V and 5 V
SDRBVCC	None	SDRB	SD-RAM (except SDRBCK, SDRBCKB) Port buffers supply, nominal 1.8 V

¹ D1M1, D1Lx have no ISOVDD, but internal voltage from REG1VCC is used to supply ISO digital circuit.

8.2 Power supply

8.2.1 Main power supply structure

The main power supply domain has to be connected to an external power adapter or laboratory supply. The voltage is expected to be between +12V and +15V. There are different connectors to support a variety of available power supplies. Additionally, there is a dedicated power output connector, to supply several boards from the same power adapter.

Table 8-3: Power Supply connectors

Loc	Name	Direction	Function
CN5	ETC	Input	Main power supply connector
J1	+12V	Input	Main power supply connector
CN7 / CN8	RED / BLACK	Input	Main power supply connector
J2	ExOUT	Output	12V Power supply for an external board

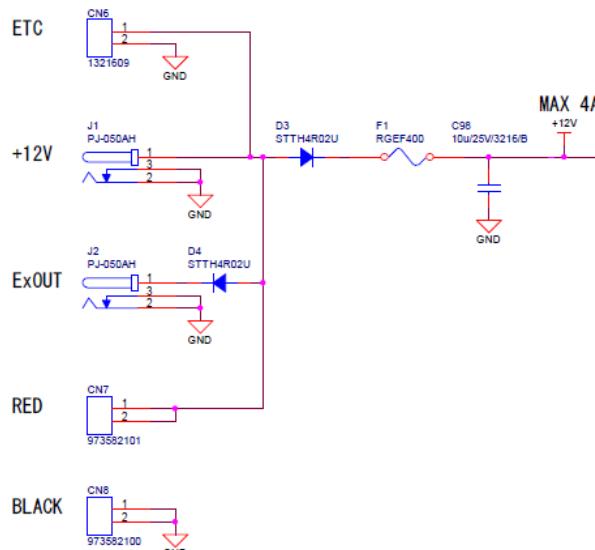


Figure 8-2: Main Power supply block diagram

8.2.2 Power supply structure on the board

The following table shows all available power supplies as well as their maximum supported currents.

Table 8-4: On board voltage regulators and DC-DC converters

IC	Input voltage	Output voltage	Net name	Spec
U7	12V	5V	+5V	Max 4A
U8	12V	3.3V	+3.3V	Max 4A
U9	12V	5V	ISO+5V	Max 2A
U12	12V	3.3V	ISO+3.3V	Max 4A
U5	ISO+3.3V	1.25V	+1.25V	Max 2A
U6	ISO+3.3V	1.8V	+1.8V	Max 0.5A
U1	+3.3V	2.5V	+2.5V	Max 1A
U2	+3.3V	1.2V	+1.2V	Max 1A

Table 8-5: Component list of the voltage regulators and DC-DC converters

Position	manufacturer	Device	Spec
U5, U7, U8, U12	GE Critical Power	APXK004A0X	DC-DC converter (Input 8V-16V, Output 0.6V-8V DC, Current 4A)
U9	GE Critical Power	APXK002A0X	DC-DC converter (Input 8V-16V, Output 0.6V-8V DC, Current 2A)
U1, U2, U6	Linear Technology	TL1963EQ	Voltage regulator (Input 1.21V-20V, Output 1.8V, 2.5V, 1.2V)

8.2.3 Configuration of the power domains of the RH850/D1x

Each configurable MCU core voltage domain can be configured by a Jumper matrix from all (applicable) supply voltage rails. Please check Table 8-6 for all power domains and their configuration possibilities. If no Jumper switch is available for a certain power supply, this voltage is fixed to a single level.

Table 8-6: Power supply selection within this evaluation board

Power supply	Voltage level	JP switch	LED	Source / Selection
REG0VCC	3.3V or 5V	JP11	LED4	+3.3V , + 5V
OSCVCC	3.3V or 5V	JP12	LED5	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
REG1VCC	3.3V or 5V	JP1	LED7	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
PLLVCC	3.3V or 5V	JP2	LED10	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
ISOVDD	1.25V	None	LED23	+1.25V
ZPDVCC/ ZPDVREF	3.3V or 5V	JP13	LED9	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
EVCC	3.3V or 5V	JP14	LED11	+3.3V , + 5V
B0VCC	3.3V or 5V	JP4	LED13	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
B1VCC	3.3V or 5V	JP5	LED14	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
B2VCC	3.3V or 5V	JP6	LED15	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
B3VCC	3.3V or 5V	JP7	LED16	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
B4VCC	3.3V or 5V	JP8	LED17	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
RVCC/B5VCC	3.3V or 5V (Note 1)	JP3	LED12	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
MVCC	3.3V	JP10	LED19	+3.3V , ISO+3.3V
SFVCC	3.3V or 5V (Note 2)	JP15	LED8	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
ISMVCC	3.3V or 5V	JP9	LED18	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
A0VCC	3.3V or 5V	JP16	LED6	+3.3V , + 5V, ISO+3.3V , ISO+ 5V
A0VREF				
SDRBVCC	+1.8V	None	LED22	+1.8V
+1.2V	+1.2V	None	LED20	+3.3V
+1.25V	+1.25V	None	(ISOVDD)	ISO+3.3V
+1.8V	+1.8V	None	(SDRBVCC)	ISO+3.3V
+2.5V	+2.5V	None	LED21	+3.3V
+3.3V	+3.3V	None	LED1	+12V
+5V	+5V	None	LED2	+12V
ISO+3.3V	ISO+3.3V	None	LED1	+12V
ISO+5V	ISO+5V	None	LED2	+12V
+12V	+12V to +15V	None	LED3	Power Input Connectors

Note: 1) RVCC (D1M2) should be 3.3V only. B5VCC can be both 3.3V and 5V.

2) SFVCC (D1M2, D1M1 and D1L2) should be 3.3V only.

SFVCC (D1L1) can be both 3.3V and 5V

The following Figure 8-3 shows a power supply selection jumper for a power supply that supports four different settings. By setting the Jumper either to 1-2, 3-4, 5-6 or 7-8 the respective voltage will be selected as supply voltage.

Note: It is not intended to leave a power supply selection jumper unpopulated. Unpowering single single power domains by pulling the jumpers happens on own risk.

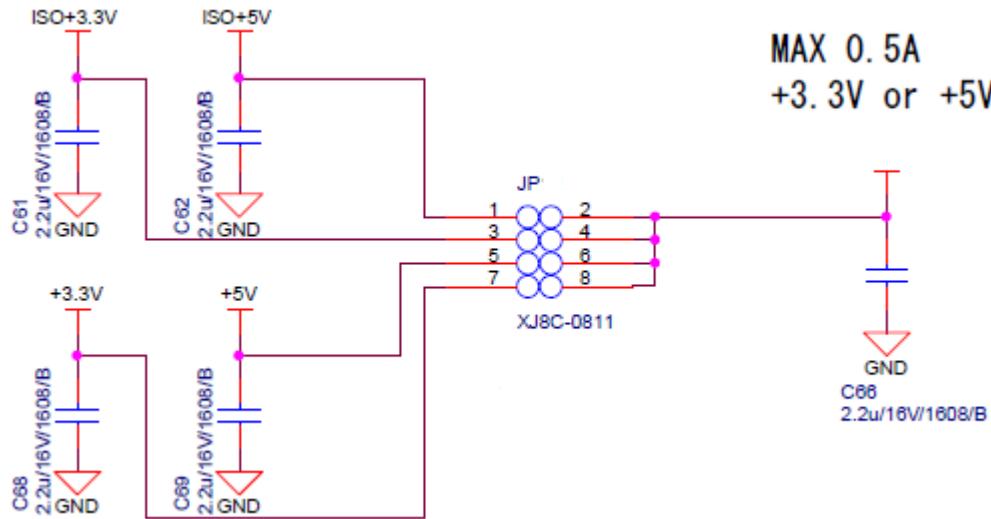


Figure 8-3: Example of Power supply Jumper structure

Power Supply Selection Matrix

As the different devices of the D1x family support different voltage section, there are jumper positions that are allowed for one device and forbidden for another device. In the Table 8-7 shown below, the possible jumper settings for each member of the D1x family is shown. The abbreviation “awo” denotes an Always-On Voltage domain. These voltages are always supplied, regardless of the level of the MCU’s PWRCTL signal. The abbreviation “iso” denotes an Isolated Voltage domain. These voltages are turned on or off with respect to the level of the MCU’s PWRCTL signal.

Table 8-7: Possible settings of the power supply selection matrix

	D1L1				D1L2 (H)				D1M1 (H)				D1M2(H)				
	awo		iso		awo		iso		awo		iso		iso	awo		iso	
	3v3	5v	3v3	5v	3v3	5v	3v3	5v	3v3	5v	3v3	5v		3v3	5v	3v3	5v
REG0VCC	x	D			x	D			x	D				x	D		
OSCVCC	x	x	x	D	x	x	D	x	x	x	D	x		x	x	D	x
EVCC	x	D			x	D			x	D				x	D		
REG1VCC	x	x	x	D	x	x	D	x	x	x	D	x		x	x	D	x
ISOVDD													1v25				
PLLVCC														x	x	D	x
B0VCC	x	x	x	D	x	x	D	x	x	x	D	x		x	x	D	x
B1VCC	x	x	x	D	x	x	D	x	x	x	D	x		x	x	D	x
B2VCC														x	x	D	x
B3VCC/ (SDRAVCC)									x		D			x	x	D	x
B4VCC					x	x	D	x	x	x	D	x		x	x	D	x
B5VCC/RVCC	x	x	x	D	x	x	D	x	x	x	D	x		x		D	
MVCC														D		x ²	
SFVCC	x	x	D	x	x		D		x		D			x		D	
SDRBVCC													1v8				
ISMVCC	x	x	x	D	x	x	x	D	x	x	x	D		x	x	x	D
ZPDVCC	x	D	x	x	x	D	x	x	x	D	x	x		x	D	x	x
A0VCC	x	x	x	D	x	x	D	x	x	x	D	x		x	x	D	x

x: Possible Setting

D: Default Setting

Note: Certain modules on the mango Board may not support the +5V domains, so before changing the configuration, please check the functions blocks shown in Table 8-8 as well as your own connected hardware.

² Please disconnect the VIO/HDMI I/F Board before setting MVCC to iso3v3.

Notes before switching to 5V or changing the muxing scheme of a power domain configured to 5V

The following checkpoints are possible point of failures when changing the voltage levels to a higher voltage. Please note that there might be more peripherals to be checked before switching the voltage levels.

Table 8-8: Possible Point-of-failures when switching to 5V

Power domain	Function to be checked	Comment
EVCC	ETH-PHY	Check connected ethernet module for support of 5V levels
B1VCC	I2S-DAC	I2D DAC is +3.3V only. Switch Audio-Mux to H-Bridge or pull Jumpers JP56 to 63
	Ext-Audio HW	Check HW on Audio-I2S/PWM connector for support of 5V levels
B2VCC	CVBS-IC	CVBS to ITU converter IC is +3.3V only. Set VINMUX_SEL to VG-Port
	HDMI-VO1	Parallel video to HDMI converter IC is +3.3V only. Set VO1MUX_SEL2 to parallel video
B3VCC	CVBS-IC	CVBS to ITU converter IC is +3.3V only. Set VINMUX_SEL to VG-Port
B4VCC	ETH-PHY	Check connected ethernet module for support of 5V levels
B5VCC/RVCC	HDMI-VO0	Parallel video to HDMI converter IC is +3.3V only. Set VO0MUX_SEL2 to parallel video
	RSDS-HW	Check connected RSDS module for support of 5V levels
SFVCC	sFlash	Do not switch to 5V if serial flash is soldered on adapter board
	MOST-HW	Check connected MOST/MLB module for support of 5V levels

8.2.4 Power supply sequencing, supervision and PWRGOOD signal generation

The D1x MCUs require a certain voltage ramp-up / ramp-down sequence. This board is designed such that these requirements are fulfilled in a simple way. The following Figure 8-4 and Figure 8-5 show power sequences for the MCU's power supplies.

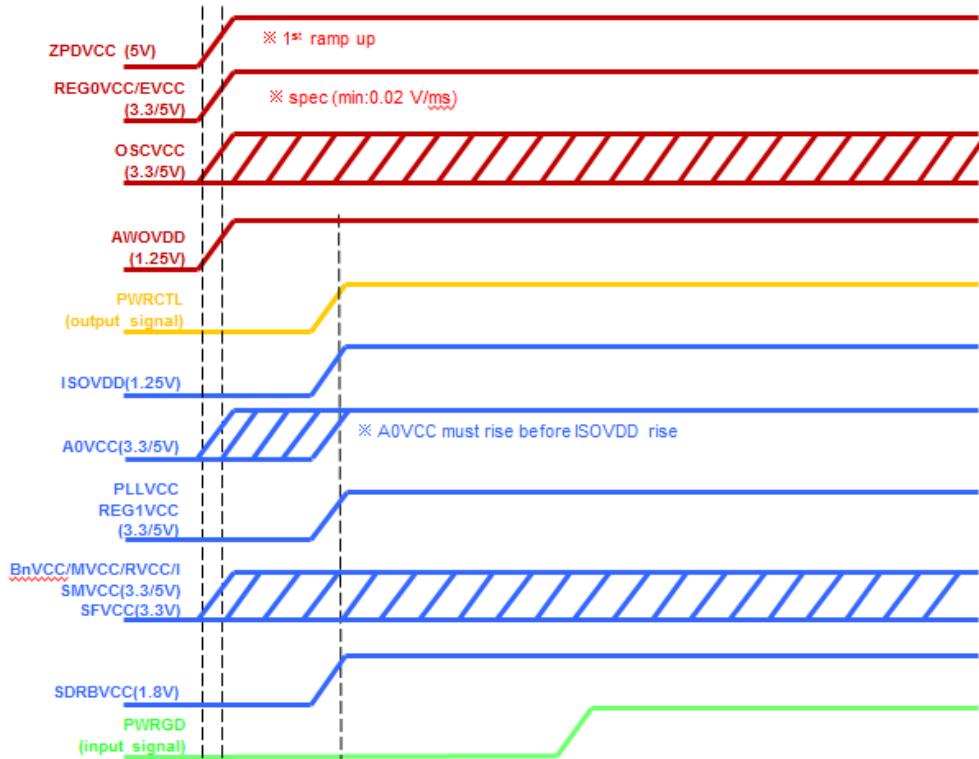


Figure 8-4: Power up sequence behavior

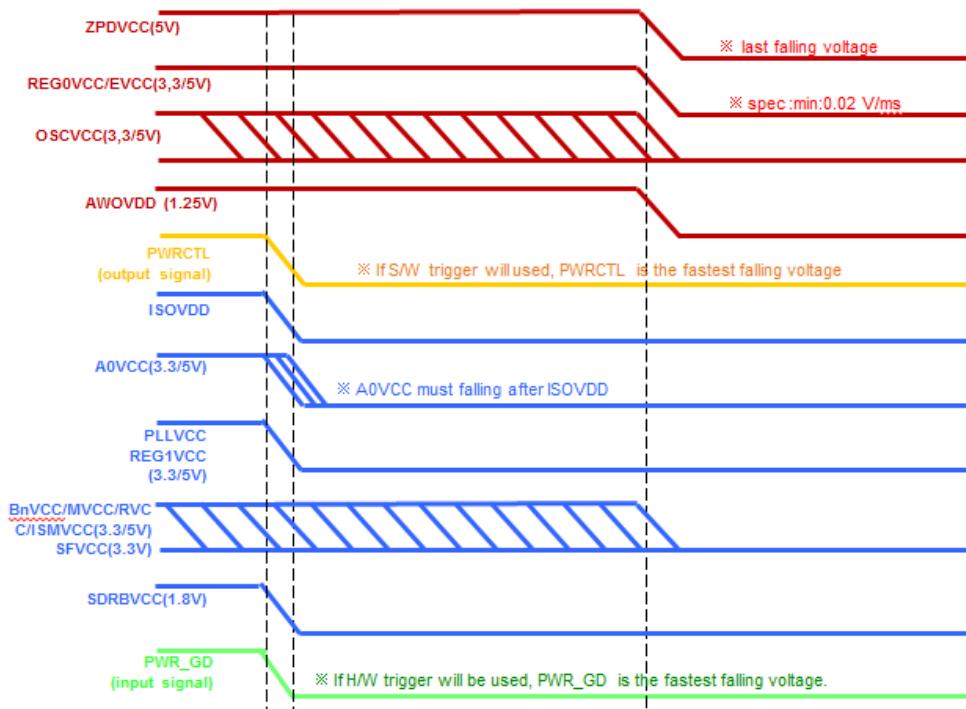


Figure 8-5: Power down sequence behavior

PWRGOOD signal generation

The MCU requires a PWRGOOD signal to start operation after entering its full-powered run mode. The signals that contribute to the generation of that signals can be selected with the Jumpers JP100 to JP103. As all other voltages that are supplied to the the MCU are generated from these four voltages, the supervision of these voltages is sufficient.

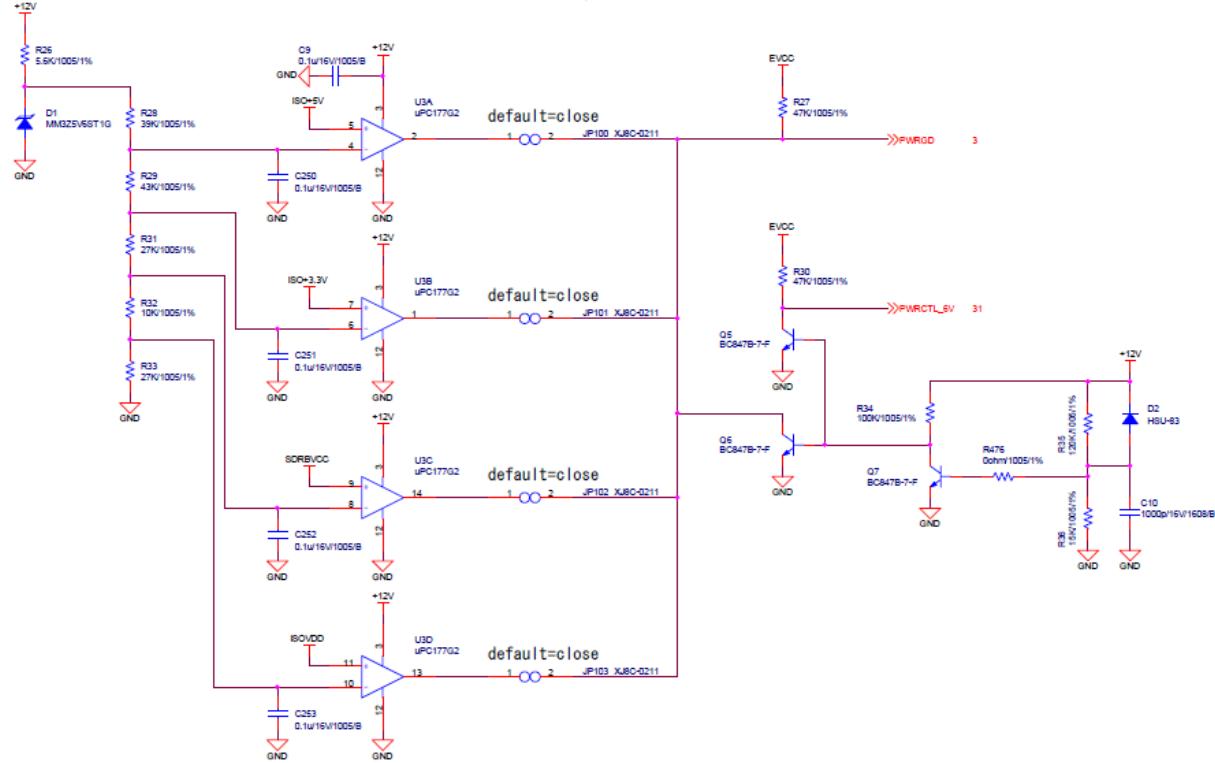


Figure 8-6: Power good signal generation circuit

Power Supply supervision

The D1x Mango Board has a dedicated header (CN5) for the connection of voltage monitors. The pin assignment can be found in Table 8-9.

Table 8-9: Power supply connector pin assignment

Pin	Supply line	Pin	Supply line
1	+1.2V	2	+2.5V
3	+3.3V	4	+5V
5	+12V	6	OSCVCC
7	REG0VCC	8	REG1VCC
9	A0VCC	10	ZPDVCC
11	SFVCC	12	ISOVDD
13	SDRBVCC	14	EVCC
15	PLLVCC	16	B0VCC
17	RVCC/B5VCC	18	B2VCC
19	B1VCC	20	B4VCC
21	B3VCC	22	MVCC
23	ISMVCC	24	n.c.
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND

9 Communication I/F block

9.1 Overview

RH850/D1x has several communication interfaces as listed below.

Table 9-1: Connector for below communication I/F

I/F	Protocol	Connector
Ethernet	Ethernet, AVB	64-pin connector I/F for an external Ethernet PHY supplied by Tessera Technology
MOST	MOST50	MOST50: 44-pin connector for an external MOST50 PHY
	MOST150	MOST150: 44-pin connector for an external MOST150 PHY
RLIN30-33	LIN, RS232	9-pin D-SUB (3 female, 1 male) connector with 40-pin connector for FlexTiny PHY
RLIN30	LIN, RS232	9-pin D-SUB (1 male) connector with on-board PHY
RSCAN0-2	CAN	9-pin D-SUB (3 female) connector with 40-pin connector for FlexTiny PHY
RSCAN3	CAN	9-pin D-SUB (female) connector with on-board PHY

9.2 Ethernet PHY

The Ethernet PHY “EEB-BRPHY” of Tessera Technolgy supports AVB features. Is is equipped with a BCM89810A2MLG from Broadcom.

Vendor: TESSERA TECHNOLOGY INC.

**2710-1 4F, Noborito, Tama-ku, Kawasaki-shi
Kanagawa, 214-0014 JAPAN**

TEL +81-44-271-7533 FAX +81-44-271-7534

E-Mail: info@tessera.co.jp

URL: http://www.tessera.co.jp

Part Name: EEB-BRPHY

The D1x mango Board has two Ethernet PHY connectors. Both connectors are routed to different pins of the D1x, but both pins connect to the same Ethernet macro instance. So it is only possible to use one connector.

The Ethernet pins are multiplexed with regular pin functions. To decouple them from the low speed I/Os, multiplexing is done close to the MCU on the adapter board.

For the connector ETH0, the port pins are P42_0 to P42_15. Multiplexing is controlled with the Switch DSW2.4 “P42_ETHER_SEL” on the adapter board. For each PHY connector, a dedicated clock source may be soldered onto the board (default unpopulated). By setting Jumper JP43 to 2-3, the Ethernet clock is supplied by the MCU.

Table 9-2: Connector CN31 for Ethernet0 (P42)

Pin	Signal name	Connected to	Pin	Signal name	Connected to
1			2	ETNB0RXDV_0	P42_14
3	GND		4	ETNB0RXD3_0	P42_10
5			6	ETNB0RXD2_0	P42_11
7	GND		8		
9	GND		10	ETNB0RXD1_0	P42_12
11	GND		12	ETNB0RXD0_0	P42_13
13	GND		14	GND	
15	GND		16	ETNB0RXCLK_0	P42_9
17			18	GND	
19	ETNB0TXEN_0	P42_4	20		
21			22		
23	ETNB0TXD3_0	P42_0	24		
25	GND		26	ETNB0CRSDV_0	P42_7
27	ETNB0TXD2_0	P42_1	28	ETNB0RXER_0	P42_15
29	GND		30	ETNB0COL_0	P42_6
31	ETNB0TXD1_0	P42_2	32	GND	
33			34	ETNB0TXCLK_0	P42_8
35	ETNB0TXD0_0	P42_3	36	GND	
37	GND		38	ETNB0TXER_0	P42_5
39	GECLK0	P42_8 / OSC	40		
41	GND		42		
43	BOARD RESET		44		
45	GND		46		
47	MDIO	P47_6	48		
49	GND		50		
51	MDC	P47_7	52		
53			54	+3.3V	
55	P0_8		56	+3.3V	
57	+1.2V		58	+3.3V	
59	+1.2V		60	+3.3V	
61	GND		62	GND	
63	GND		64	GND	

For the connector ETH1, the port pins are P46_6 to P46_15 and P47_0 to P47_5. Multiplexing of these pins is controlled by DSW2.3 “P467_ETHER_SEL” on the adapter board. For each PHY connector, a dedicated clock source may be soldered onto the board (default unpopulated). By setting Jumper JP44 to 2-3, the Ethernet clock is supplied by the MCU.

Table 9-3: Connector CN32 for Ethernet1 (P46 and P47)

Pin	Signal name	Connected to	Pin	Signal name	Connected to
1			2	ETNB0RXDV_1	P47_4
3	GND		4	ETNB0RXD3_1	P47_0
5			6	ETNB0RXD2_1	P47_1
7	GND		8		
9	GND		10	ETNB0RXD1_1	P47_2
11	GND		12	ETNB0RXD0_1	P47_3
13	GND		14	GND	
15	GND		16	ETNB0RXCLK_1	P46_15
17			18	GND	
19	ETNB0TXEN_0	P46_10	20		
21			22		
23	ETNB0TXD3_1	P46_6	24		
25	GND		26	ETNB0CRSDV_1	P46_13
27	ETNB0TXD2_1	P46_7	28	ETNB0RXER_1	P47_5
29	GND		30	ETNB0COL_1	P46_12
31	ETNB0TXD1_1	P46_8	32	GND	
33			34	ETNB0TXCLK_1	P46_14
35	ETNB0TXD0_1	P46_9	36	GND	
37	GND		38	ETNB0TXER_1	P46_11
39	GECLK1	P46_14 / OSC	40		
41	GND		42		
43	BOARD RESET		44		
45	GND		46		
47	MDIO	P47_6	48		
49	GND		50		
51	MDC	P47_7	52		
53			54	+3.3V	
55	P0_8		56	+3.3V	
57	+1.2V		58	+3.3V	
59	+1.2V		60	+3.3V	
61	GND		62	GND	
63	GND		64	GND	

The control signals MDIO (P47_6) and MDC (P47_7) are only available on P47 and can be muxed to both ethernet connectors by a dedicated muxer with the Switch DSW1.4 “MD_ETHER_SEL” on the adapter board.

9.3 MOST / MLB connector

The MOST MLB50/150 connectors are designed to fit to SMSC development boards

- SMSC Physical+ Interface Boards 0S81092 ePhy (MOST50) and
- SMSC Physical+ Interface Boards 0S81110/2+0 ePhy (MOST150).

The Pin assignment for MLB50 and MLB150 so both have been implemented. The pin assignments are shown in Table 9-4 below. The MOST interface is on the MCU Port P21 next to the serial flash interface.

Both MLB connectors have pins for an I2C connection. These pins can be connected to the on-board I2C-Bus by setting Jumper JP21.

Table 9-4: Pin assignment MOST50 and MOST150 connectors

Pin	Function on MLB50 connector (CN21)	Function on MLB150 connector (CN22)
1		GND
2	MLBCLK	MLBCLK
3		GND
4		MLBSIG/MLBSO/SR1
5		GND
6	MLBSIG	MLBDAT/MLBDO/SX1
7		GND
8		MLBSI/SR0
9		GND
10	MLBDAT	MLBSI/SX0
11		3.3V
12		3.3V
13		5.0V continuos
14		3.3V continuos
15		GND
16		
17		
18		
19		SDA (via JP21)
20		SCL (via JP21)
21		INT_N (Interrupt)
22		GND
23		GND
24		
25	RST_N (RSTIN_N)	
26		
27		
28		
29		
30		
31		
32		
33	SCL (via JP21)	
34	INT	
35	SDA (via JP21)	RST_N (RSTIN_N)
36		
37	3.3V switched	
38	3.3V switched	
39	3.3V switched	GND
40	12V continuos	GND

*Pin41 to 44 shown in the Schematic belong to the shielding of the connector and are connected GND.

9.4 UART / LIN

To use the UART/RS232 or the LIN-Bus, there is either the possibility to use the on-board PHYs or external PHYs produced by the company Eberspächer.

For all RS232, LIN (and CAN) connections, there are four D-SUB9 connector available, that can be multiplexed according to the required connections.

9.4.1 External FlexTiny PHYs

There are four slots looking similar to a PCI-Express connector. These are the connectors for the FlexTiny Cards. The basic functionality required to use the PHY is available via Jumpers. For extended configuration, all important connections are available on test pins that can be connected to a GPIO of the MCU.

UART and LIN functionality is available on all four slots. The following table shows the Jumper configuration required to use the interfaces.

Table 9-5: Configuration of the FlexTiny Interfaces for UART / LIN

FlexTiny # D-SUB9 #	Macro Instance	Protocol	FlexTiny Card	Jumper on MCU side	Jumper on D-SUB9 side	D-SUB9 Pins
#0	RLIN3_0 (P0_8/9)	RS232	RS232 PHY	None	JP32 2-3	2 (RXD) 3 (TXD)
#0	RLIN3_0 (P0_8/9)	LIN	LIN PHY	None	JP32 1-2	7 (LIN)
#1	RLIN3_3 (JP0_3/5)	RS232	RS232 PHY	JP39 2-3 JP40 2-3	JP37 2-3	2 (RXD) 3 (TXD)
#1	RLIN3_3 (JP0_3/5)	LIN	LIN PHY	JP39 2-3 JP40 2-3	JP37 1-2	7 (LIN)
#1	RLIN3_0 (P0_6/7)	RS232	RS232 PHY	JP39 1-2 JP40 1-2	JP37 2-3	2 (RXD) 3 (TXD)
#1	RLIN3_0 (P0_6/7)	LIN	LIN PHY	JP39 1-2 JP40 1-2	JP37 1-2	7 (LIN)
#2	RLIN3_2 (P0_2/3)	RS232	RS232 PHY	JP34 2-3 JP35 2-3	JP33 2-3	2 (RXD) 3 (TXD)
#2	RLIN3_2 (P0_2/3)	LIN	LIN PHY	JP34 2-3 JP35 2-3	JP33 1-2	7 (LIN)
#3	RLIN3_1 (P0_0/1)	RS232	RS232 PHY	None	JP38 2-3 JP41 open JP42 open	2 (RXD) 3 (TXD)
#3	RLIN3_1 (P0_0/1)	LIN	LIN PHY	None	JP38 1-2 JP41 open JP42 open	7 (LIN)

The following pictures, Figure 9-1 and Figure 9-2 are sample images of a FlexTiny card and how they are installed.



Figure 9-1: Eberspächer 3-0015-0Fxx FlexTiny RS232 module

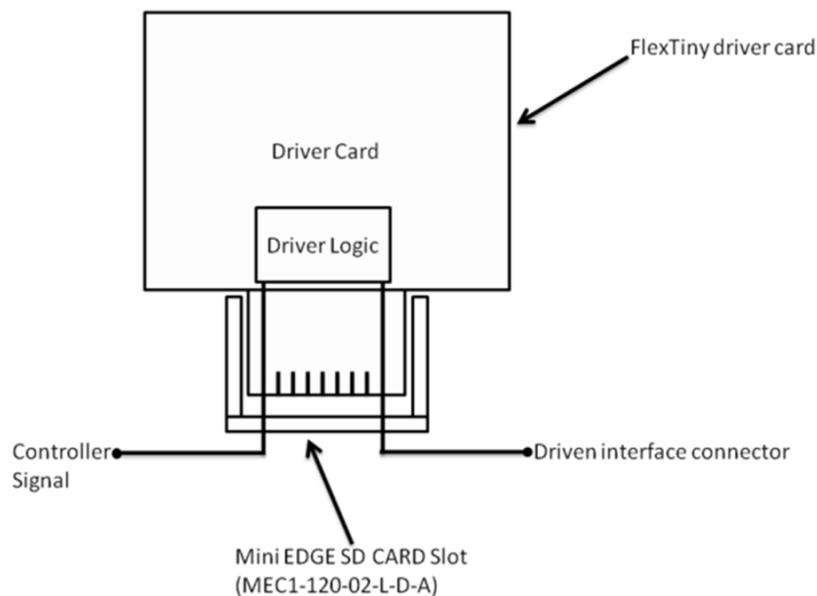


Figure 9-2: Mini Edge Card slot (MEC1-120-02-L-D-A)

Vendor: Eberspächer Electronics GmbH & Co. KG

Robert Bosch Str. 6
D-73037 Göppingen
TEL +49 7161 9559-0 FAX +49 7161 9559-455
URL: <http://www.eberspaecher.com>

Part Name: 3-00150G01-01 (FlexTiny LIN TH8082)
Part Name: 3-00150F01-01 (FlexTiny RS232 MAX3227)

Table 9-6 shows the general pin assignment of a FlexTiny connector. MCU_TXD/_RXD and RLC_TXD/_RXD/_LIN are specific to each connector. For specific pin assignments, please check Table 9-5 and the schematics. Pins described as PAD are available as breakout pins next to the connector.

**Table 9-6: General Pin assignment of the UART/LIN/CAN FlexTiny Card Slots
(Connectors CN24, CN25, CN28, and CN29)**

Pin	Connected to	Pin	Connected to
1	GND	2	GND
3		4	RLC_RXD
5		6	RLC_TXD or RLC_LIN
7	Pin7 / Pull-Up to EVCC	8	
9	Pin9	10	
11	Pin11 / Pull-Up to EVCC	12	
13		14	
15		16	
17	MCU_TXD	18	
19		20	
21	MCU_RXD	22	EVCC
23		24	GND
25		26	+5V
27	Pin27	28	GND
29	Pin29	30	+12V
31	Pin31	32	GND
33	Pin33	34	Pin34
35		36	Pin36
37		38	Pin38
39		40	Pin40

Note: No FlexTiny RS232 modules and no FlexTiny LIN modules are delivered with the Mango Board. They need to be ordered separately, when operation of more than one UART / LIN is needed.

9.4.2 On-Board UART / LIN PHYs

To use the on-board PHYs, please configure the Jumpers as follows.

The equipped PHYs are for UART a MAX3222ECWN+ from Maxim on port pins P0_8/9 and for LIN a TJA1020T from NXP Semiconductors on port pins P0_8/9. The LIN transceiver has additional control pins for LIN NSLP- and LIN WAKE- signal on port pins P0_6/7, both detachably by jumpers. The schematic of the on-board PHYs is shown in Figure 9-3.

Table 9-7: Configuration of the on-board Interfaces for UART / LIN

FlexTiny # D-SUB9 #	Macro Instance	Protocol	FlexTiny Card	Jumper on MCU side	Jumper on D-SUB9 side	D-SUB9 Pins
#3	RLIN3_0 (P0_8/9)	RS232	None (on-Board)	JP22 2-3	JP41 closed	2 (RXD) 3 (TXD)
#3	RLIN3_0 (P0_8/9)	LIN	None (on-Board)	JP22 1-2 JP26 optional JP27 optional	JP42 closed	7 (LIN)

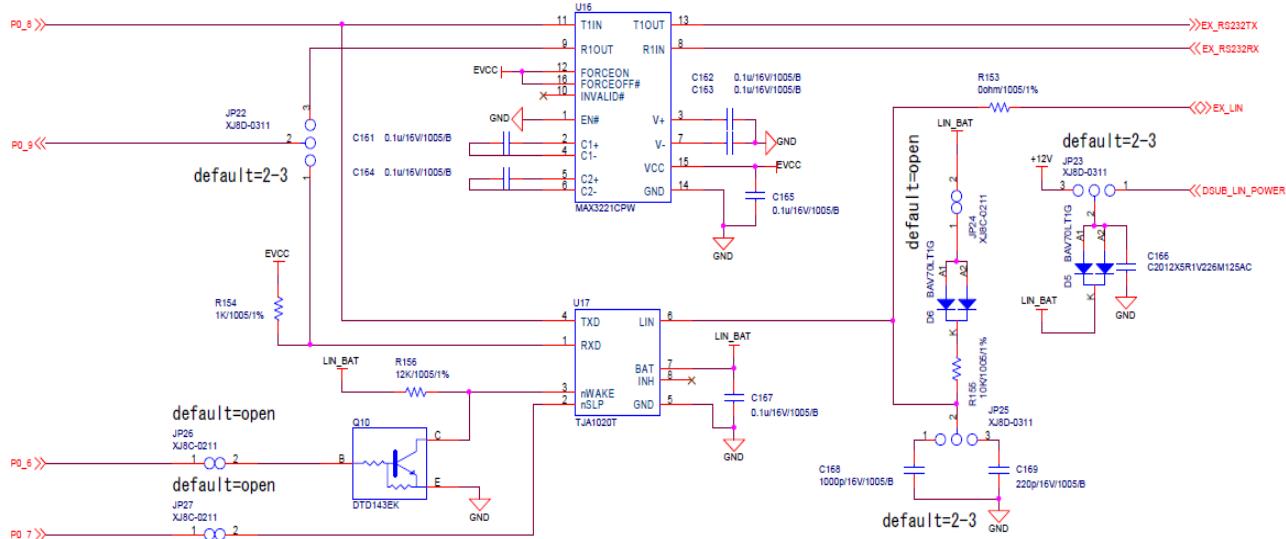


Figure 9-3: UART / LIN transceiver circuit on Mango board

9.4.3 D-SUB9 Connector Pin Assignment

Table 9-8 shows the pin assignment of the 3 female D-SUB9 connectors. The signals with the prefix RLC_ are connected to the respective FlexTiny slots. Table 9-9 shows the pin assignment of the male D-SUB9 connector.

**Table 9-8: D-SUB9 female connector pin assignment
(CN23 / CN26 / CN27) (UART/LIN/CAN)**

Pin	Function
1	
2	RLC _{n=0,1,2} _RXD
3	RLC _{n=0,1,2} _TXD (JP32, JP33, JP37)*
4	Connected to pin6
5	GND
6	Connected to pin4
7	RLC _{n=0,1,2} _LIN
8	
9	

*These jumpers can select either the UART TxD or LIN-Bus pin of the FlexTiny card. For CAN, they need to be set to position 1-2.

Table 9-9: D-SUB9 male connector pin assignment (CN30) (UART/LIN)

Pin	Function
1	
2	RLC ₃ _RXD
3	RLC ₃ _TXD (JP38)*
4	Connected to pin6
5	GND
6	Connected to pin4
7	RLC ₃ _LIN
8	
9	D-sub_LIN_POWER

*This jumper can select either UART TxD or LIN-Bus pin of the FlexTiny card.

9.5 CAN

To use the CAN-Bus, there is either the possibility to use the on-board PHYs or the external PHYs produced by the company Eberspächer.

For all RS232, LIN and CAN connections, there are three D-SUB9 connectors available, that can be multiplexed according to the required connections. (There are actually four D-SUB9 connectors, but only three of them are available for CAN)

9.5.1 External FlexTiny PHYs

There are four slots looking similar to a PCI-Express connector. These are the connectors for the FlexTiny Cards. The basic functionality required to use the PHY is available via Jumpers. For extended configuration, all important connections are available on test pins that can be connected to a GPIO of the MCU.

UART and LIN functionality is available on all four slots. For CAN, only slots #0 to #2 are described. The following table shows the Jumper configuration required to use the CAN interfaces.

Table 9-10: Configuration of the FlexTiny Interfaces for UART / LIN

FlexTiny # D-SUB9 #	Macro Instance	Protocol	FlexTiny Card	Jumper on MCU side	Jumper on D-SUB9 side	D-SUB9 Pins
#0	CAN2 (P0_8/9)	CAN	CAN PHY	None	JP32 1-2	2 (CAN-L) 7 (CAN-H)
#1	CAN1 (P0_6/7)	CAN	CAN PHY	JP39 1-2 JP40 1-2	JP37 1-2	2 (CAN-L) 7 (CAN-H)
#2	CAN0 (P0_4/5)	CAN	CAN PHY	JP34 1-2 JP35 1-2 JP30 1-2	JP33 1-2 JP36 open	2 (CAN-L) 7 (CAN-H)

Vendor: Eberspächer Electronics GmbH & Co. KG

Robert Bosch Str. 6
D-73037 Göppingen
TEL +49 7161 9559-0 FAX +49 7161 9559-455
URL: <http://www.eberspaecher.com>

Part Name: 3-00150H01-01 (FlexTiny CAN HS TJA1041)

Note: No FlexTiny CAN modules and no FlexTiny LIN modules are delivered with the Mango Board. They need to be ordered separately, when operation of more than one CAN is needed.

9.5.2 On-Board CAN PHY

To use the on-board PHY, please configure the Jumpers as follows.

The equipped PHYs are TJA1041T from NXP Semiconductors on port pins P0_4/5. The schematic of the on-board PHYs is shown in Figure 9-4.

In order to use the termination, please close the jumpers JP29 and JP31. To get a SPLIT signal for the on-board PHY, please also close JP28.

Table 9-11: Configuration of the on-board Interfaces for CAN

FlexTiny # D-SUB9 #	Macro Instance	Protocol	FlexTiny Card	Jumper on MCU side	Jumper on D-SUB9 side	D-SUB9 Pins
#2	CAN0 (P0_4/5)	CAN	None (on-Board)	JP30 2-3	JP36 1-2 JP36 3-4 JP33 open	2 (RXD) 7 (TXD)

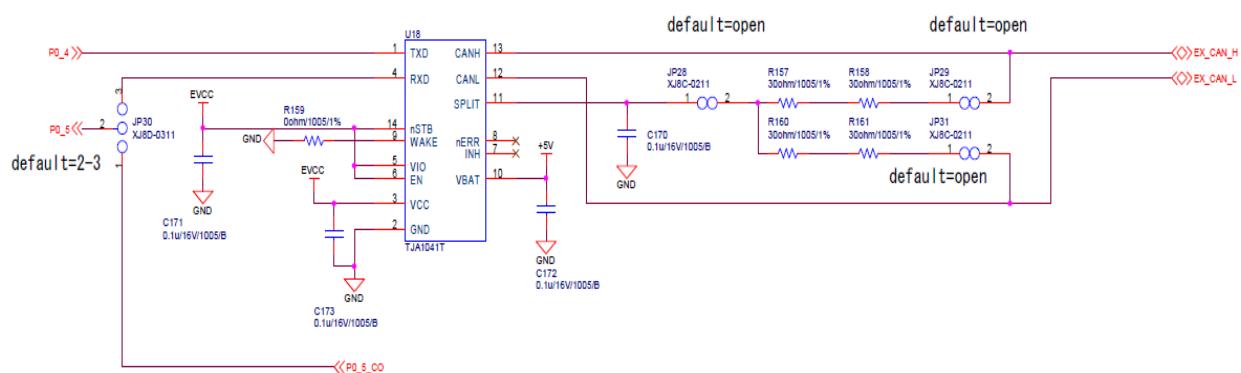


Figure 9-4: CAN transceiver circuit on Mango board

9.5.3 D-SUB9 Connector Pin Assignment

For the pin assignment, please check Table 9-8. As the connector are shared, the assignemtn is identical to the one shown above. The signals with the prefix RLC_ are connected to the respective FlexTiny slots.

10 User interface

10.1 Overview

This board has the following user interface functions

- 16 LEDs
- One joystick-button switch (Up, Down, Left, Right, OK)
- One rotary encoder (Left, Right, Press)
- Two potentiometers to supply the ADC pins of the MCU

10.2 HMI LEDs

To use the HMI LEDs, connect the LEDs to the respective GPIO line of P16. This can be done by setting jumpers in CN19 and CN20.

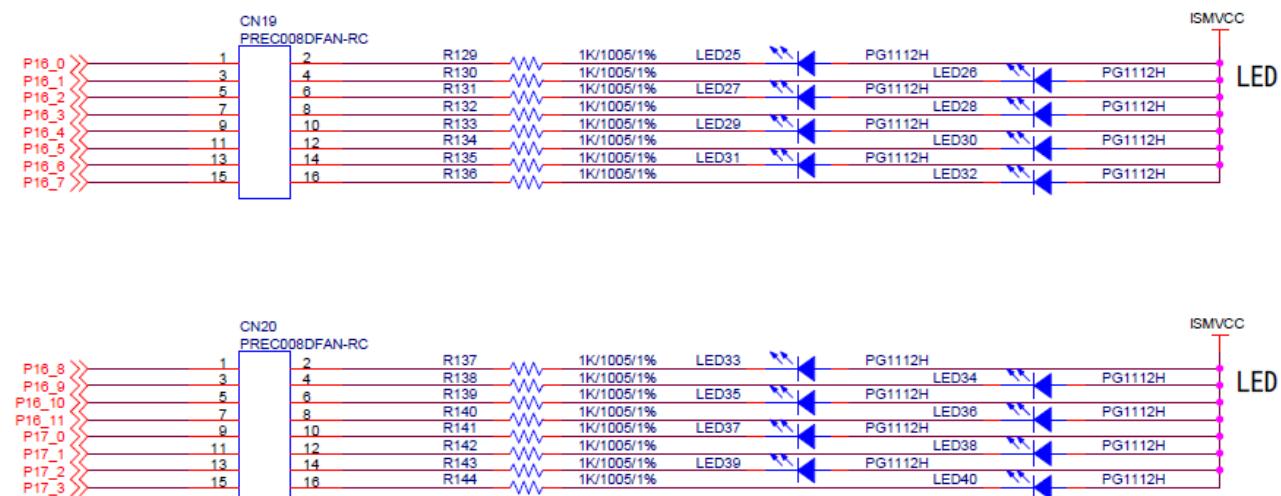


Figure 10-1: LED HMI interface on the Mango board

The LEDs will be turned ON by driving the MCUs pin to low level.

Table 10-1: LEDn Function specification

Loc LEDn	Function	
	LED Port indicator	
Low level	LED ON	
High level	LED OFF	

Table 10-2: LED and MCU ports

LED	MCU port	LED	MCU port
LED25	P16_0	LED33	P16_8
LED26	P16_1	LED34	P16_9
LED27	P16_2	LED35	P16_10
LED28	P16_3	LED36	P16_11
LED29	P16_4	LED37	P17_0
LED30	P16_5	LED38	P17_1
LED31	P16_6	LED39	P17_2
LED32	P16_7	LED40	P17_3

10.3 HMI switches

The Buttons are connected such that they can be used to trigger an interrupt. The Rotary-Knob supports press, rotate left and rotate right, the buttons support up, down, left, right and center. The buttons are detachable by DIP switch DSW29. In the default board configuration, the signal P0_5 (down button) is driven by the on board CAN driver. Before using the DOWN Button by activating DSW29.5, please open Jumper JP30

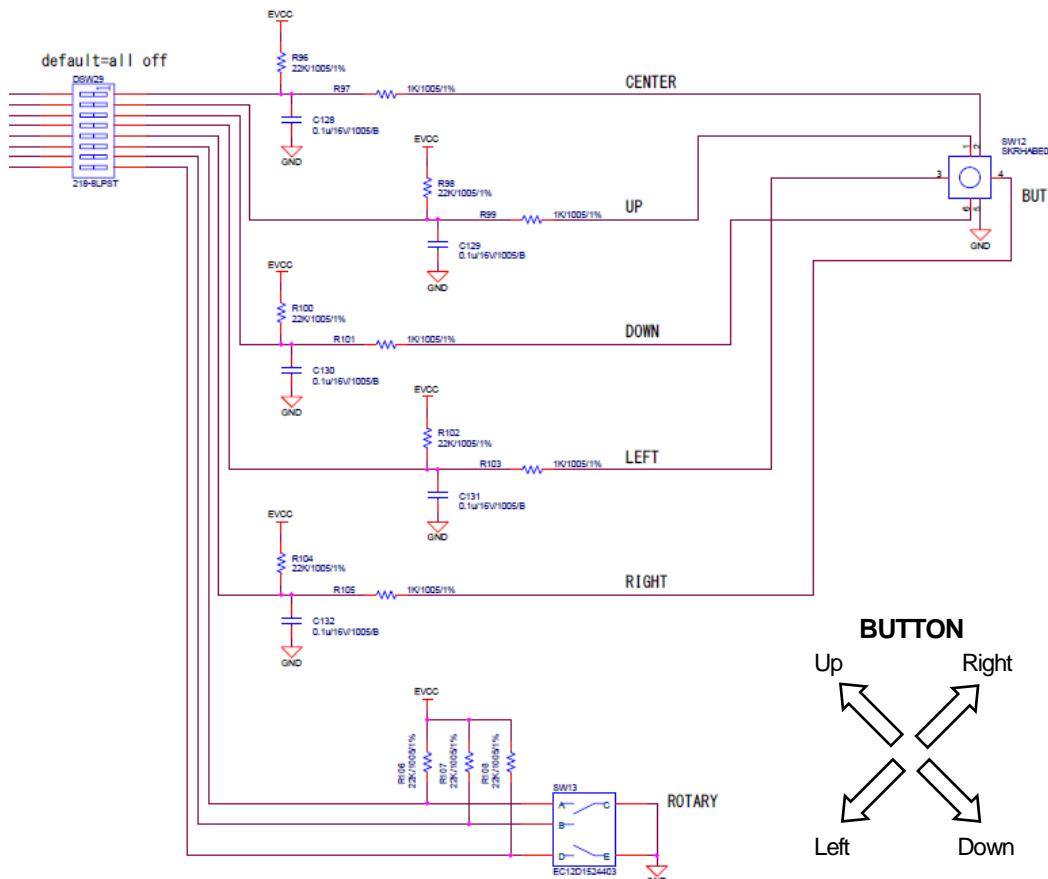


Figure 10-2: BUTTON & ROTARY switch

Based on the directions noted in the schematics, the Button SW12 is turned 135° CCW. This means the button direction connected to the wire called "UP" points down-left on the mango board. Please use the descriptions shown in Table 10-3 below for using the button.

Table 10-3: BUTTON switch (SW12) & ROTARY switch (SW13)

Port	Interrupt	Switch	Function	Original text in schematic
P0_0	NMI	DSW29.8	Rotary D	
P0_1	INTP0	DSW29.6	Rotary A	
P0_2	INTP1	DSW29.7	Rotary B	
P0_3	INTP2	DSW29.2	LEFT Button (Down-Left)	"UP"
P0_4	INTP5	DSW29.3	RIGHT Button (Up-Right)	"DOWN"
P0_5	INTP6	DSW29.4	DOWN Button (Down-Right)	"LEFT"
P0_6	INTP7	DSW29.5	UP Button (Up-Left)	"RIGHT"
P0_7	INTP8	DSW29.1	CENTER Button	

10.4 Analog Input

The Mango Board is equipped with two potentiometers that can be used to select a voltage between GND and A0VCC. The equipped connectors CN17 and CN18 can be used to patch these voltages to the ADC pins of the MCU. CN17 is used to connect Potentiometer VR1 to the Pins P10_0 to P10_11 and CN18 is used to connect VR2 to the Pins P11_0 to P11_7.

Table 10-4: Pin assignment of CN17, the patch connector for VR1

Pin	Connection via CN17
P10_0	1-2
P10_1	3-4
P10_2	5-6
P10_3	7-8
P10_4	9-10
P10_5	11-12
P10_6	13-14
P10_7	15-16
P10_8	17-18
P10_9	19-20
P10_10	21-22
P10_11	23-24

Table 10-5: Pin assignment of CN18, the patch connector for VR2

Pin	Connection via CN18
P11_0	1-2
P11_1	3-4
P11_2	5-6
P11_3	7-8
P11_4	9-10
P11_5	11-12
P11_6	13-14
P11_7	15-16

Each Pin has a dedicated RC filter, made of $2,2\text{k}\Omega$ and 22nF . It is also possible to connect other voltages to the pins of the patch connectors. Please make sure, that external voltages do not exceed the level of A0VCC. The external signals will also be RC filtered.

10.5 VG Connector

All low speed I/O pins are available on VG-connectors for the external connection of hardware. There are two VG96 connectors with each having 96 pins in three rows (3x32pins).

For each low-speed GPIO pin that is available on a VG connector, there are dedicated pull-up/down resistors that can be selected by DIP switches.

In addition to the VG connector, the same pin layout is routed to two 3x32pin 2.54mm pin headers that are placed in parallel to the VG connectors.

10.5.1 Pull Up/Pull Down resistor by DIP switch

There is a Pull-Up / Pull-Down resistor for all low speed I/O pins on the 2.54mm header (respectively VG-connector). The Pull-Up / Pull-Down resistors are selectable by DIP switch for each I/O pin. The resistor value is 22kOhm.

10.5.2 Pin assignment of the VG connectors

The following tables show the pin assignment of each DIP switch, VG-Connector pin and Header-pin.

Table 10-6: VG Connector 1-A (CN3A) / Header Connector (CN14) / DIP Switch Pin Assignment

VG-Pin	Signal-Name	Pull-Up SW	Pull-Down SW
A01	GND		
A02	5V		
A03	5V		
A04	n.c		
A05	P1_0	DSW21.1	DSW23.4
A06	P1_1	DSW21.2	DSW23.3
A07	P1_2	DSW21.3	DSW23.2
A08	P1_3	DSW21.4	DSW23.1
A09	P1_4	DSW25.1	DSW27.8
A10	P1_5	DSW25.2	DSW27.7
A11	P1_6	DSW25.3	DSW27.6
A12	P1_7	DSW25.4	DSW27.5
A13	P1_8	DSW25.5	DSW27.4
A14	P1_9	DSW25.6	DSW27.3
A15	P1_10	DSW25.7	DSW27.2
A16	P1_11	DSW25.8	DSW27.1
A17	JP0_0	DSW22.1	DSW24.8
A18	JP0_1	DSW22.2	DSW24.7
A19	JP0_2	DSW22.3	DSW24.6
A20	JP0_3	DSW22.4	DSW24.5
A21	JP0_4	DSW22.5	DSW24.4
A22	JP0_5	DSW22.6	DSW24.3
A23	P0_0	DSW22.7	DSW24.2
A24	P0_1	DSW22.8	DSW24.1
A25	P0_2	DSW26.1	DSW28.8
A26	P0_3	DSW26.2	DSW28.7
A27	P0_4	DSW26.3	DSW28.6
A28	P0_5	DSW26.4	DSW28.5
A29	P0_6	DSW26.5	DSW28.4
A30	P0_7	DSW26.6	DSW28.3
A31	P0_8	DSW26.7	DSW28.2
A32	P0_9	DSW26.8	DSW28.1

Table 10-7: VG Connector 1-B (CN3B) / Header Connector (CN13) / DIP Switch Pin Assignment

VG-Pin	Signal-Name	Pull-Up SW	Pull-Down SW
B01	P2_0	DSW13.1	DSW15.8
B02	P2_1	DSW13.2	DSW15.7

B03	P2_2	DSW13.3	DSW15.6
B04	P2_3	DSW13.4	DSW15.5
B05	P2_4	DSW13.5	DSW15.4
B06	P2_5	DSW13.6	DSW15.3
B07	P2_6	DSW13.7	DSW15.2
B08	P2_7	DSW13.8	DSW15.1
B09	P2_8	DSW17.1	DSW19.4
B10	P2_9	DSW17.2	DSW19.3
B11	P2_10	DSW17.3	DSW19.2
B12	P2_11	DSW17.4	DSW19.1
B13	Reserved0		
B14	Reserved1		
B15	Reserved2		
B16	Reserved3		
B17	P3_0	DSW14.1	DSW16.8
B18	P3_1	DSW14.2	DSW16.7
B19	P3_2	DSW14.3	DSW16.6
B20	P3_3	DSW14.4	DSW16.5
B21	P3_4	DSW14.5	DSW16.4
B22	P3_5	DSW14.6	DSW16.3
B23	P3_6	DSW14.7	DSW16.2
B24	P3_7	DSW14.8	DSW16.1
B25	P3_8	DSW18.1	DSW20.8
B26	P3_9	DSW18.2	DSW20.7
B27	P3_10	DSW18.3	DSW20.6
B28	P3_11	DSW18.4	DSW20.5
B29	P3_12	DSW18.5	DSW20.4
B30	P3_13	DSW18.6	DSW20.3
B31	Reserved4		
B32	Reserved5		

Table 10-8: VG Connector 1-C (CN3C) / Header Connector (CN12) / DIP Switch Pin Assignment

VG-Pin	Signal-Name	Pull-Up SW	Pull-Down SW
C01	P10_0	DSW7.1	DSW9.8
C02	P10_1	DSW7.2	DSW9.7
C03	P10_2	DSW7.3	DSW9.6
C04			
C05	RESETZ		
C06	+12V (CN12: n.c.)		
C07	P10_4	DSW7.7	DSW9.2
C08	P10_5	DSW7.8	DSW9.1
C09	P10_6	DSW11.1	DSW12.8
C10	P10_7	DSW11.2	DSW12.7
C11	P10_8	DSW11.3	DSW12.6
C12	P10_9	DSW11.4	DSW12.5
C13	P10_10	DSW11.5	DSW12.4
C14	P10_11	DSW11.6	DSW12.3
C15	P11_0	DSW11.7	DSW12.2
C16	P11_1	DSW11.8	DSW12.1
C17	P11_2	DSW5.1	DSW10.8
C18	P11_3	DSW5.2	DSW10.7
C19	P11_4	DSW5.3	DSW10.6
C20	P11_5	DSW5.4	DSW10.5
C21	P11_6	DSW5.5	DSW10.4
C22	P11_7	DSW5.6	DSW10.3
C23			
C24			
C25			
C26			

VG-Pin	Signal-Name	Pull-Up SW	Pull-Down SW
C27			
C28			
C29			
C30			
C31			
C32			

Table 10-9: VG Connector 2-A (CN4A) / Header Connector (CN11) / DIP Switch Pin Assignment

VG-Pin	Signal-Name	Pull-Up SW	Pull-Down SW
A01			
A02			
A03			
A04			
A05			
A06			
A07	P16_0	DSW1.1	DSW3.8
A08	P16_1	DSW1.2	DSW3.7
A09	P16_2	DSW1.3	DSW3.6
A10	P16_3	DSW1.4	DSW3.5
A11	P16_4	DSW1.5	DSW3.4
A12	P16_5	DSW1.6	DSW3.3
A13	P16_6	DSW1.7	DSW3.2
A14	P16_7	DSW1.8	DSW3.1
A15	P16_8	DSW5.1	DSW6.8
A16	P16_9	DSW5.2	DSW6.7
A17	P16_10	DSW5.3	DSW6.6
A18	P16_11	DSW5.4	DSW6.5
A19	P17_0	DSW5.5	DSW6.4
A20	P17_1	DSW5.6	DSW6.3
A21	P17_2	DSW5.7	DSW6.2
A22	P17_3	DSW5.8	DSW6.1
A23	P17_4	DSW2.1	DSW4.8
A24	P17_5	DSW2.2	DSW4.7
A25	P17_6	DSW2.3	DSW4.6
A26	P17_7	DSW2.4	DSW4.5
A27	P17_8	DSW2.5	DSW4.4
A28	P17_9	DSW2.6	DSW4.3
A29	P17_10	DSW2.7	DSW4.2
A30	P17_11	DSW2.8	DSW4.1
A31			
A32			

Note: P16_0 to P16_11 and P17_0 to P17_11 can be used for ISM operation.

Table 10-10: VG Connector 2-B (CN4B) / Header Connector (CN10) / DIP Switch Pin Assignment

VG-Pin	Signal-Name	Pull-Up SW	Pull-Down SW
B01	P43_0		
B02	P43_2		
B03	P43_1		
B04	P43_3		
B05	P43_4		
B06	P43_5		
B07	P43_6		
B08	P44_0		
B09	P44_1		
B10	P44_2		
B11	P44_3		
B12	P44_4		
B13	P44_5		
B14	P44_6		

VG-Pin	Signal-Name	Pull-Up SW	Pull-Down SW
B15	P44_7		
B16	P44_8		
B17	P44_9		
B18	P44_10		
B19	P44_11		
B20	P45_0		
B21	P45_1		
B22	P45_2		
B23	P45_3		
B24	P45_4		
B25	P45_5		
B26	P45_6		
B27	P45_7		
B28	P45_8		
B29	P45_9		
B30	P45_10		
B31	P45_11		
B32	P45_12		

Table 10-11: VG Connector 2-C (CN4C) / Header Connector (CN9) / DIP Switch Pin Assignment

VG-Pin	Signal-Name	Pull-Up SW	Pull-Down SW
C01	P45_13		
C02	P46_0		
C03	P46_1		
C04	P46_2		
C05	P46_3		
C06	P46_4		
C07	P46_5		
C08	P46_6		
C09	P46_7		
C10	P46_8		
C11	P46_9		
C12	P46_10		
C13	P46_11		
C14	P46_12		
C15	P46_13		
C16	P46_14		
C17	P46_15		
C18	P47_0		
C19	P47_1		
C20	P47_2		
C21	P47_3		
C22	P47_4		
C23	P47_5		
C24	P47_6		
C25	P47_7		
C26	P47_8		
C27	P47_9		
C28	P47_10		
C29			
C30			
C31	P47_X1		
C32	P47_X2		

11 Appendix

11.1 Default jumper positions

The following table lists all available jumpers and switches and their default position for the first start-up. For Jumpers and Switches on the Adapter Boards, please consult the respective Apater Board manual. The jumper positions for the power supply selection matrix is shown in chapter 8.2.3.

Table 11-1: Default position of all Jumpers and Switches on the Mango Main Board

Part No.	Description	Default Position	Part No.	Description	Default Position
JP1	REG1VCC	Power Supply Selection Matrix is shown in chapter 8.2.3 and on the backside of the Mango Main Board PCB.	JP67	V10/ZIF PWM	open
JP2	PLLVCC		JP68	V10/ZIF GPIO	open
JP3	B5VCC/RVCC		JP69	V10/ZIF I2C	open
JP4	B0VCC		JP106	V10 Select B4	2-3
JP5	B1VCC		DSW30	CVBS Data Mux	open
JP6	B2VCC		JP104	I2C1 Enable	open
JP7	B3VCC		JP105	I2C0 Enable	open
JP8	B4VCC		JP70	SEL_TCON0_1	1-2
JP9	ISMVCC		JP71	SEL_TCON0_4	1-2
JP10	MVCC		JP72	SEL_TCON0_5	1-2
JP11	REG0VCC		JP73	SEL_TCON0_6	1-2
JP12	OSCVCC		JP82/83	VO1 Select Data	JP83-1 - JP82-2
JP13	ZPDVCC		JP84	SEL_VIO1_0	2-3
JP14	EVCC		JP85	SEL_VIO1_1	2-3
JP15	SFVCC		JP86	SEL_VIO1_2	2-3
JP16	A0VCC		JP87	SEL_VIO1_3	2-3
JP90	VO0/LCBI DataEnable	open	JP88	SEL_VIO1_4	2-3
JP91	VO0 Select Data Enable 2	2-3	JP89	SEL_VIO1_5	2-3
JP92	VO0/ZIF DataEnable	open	JP98/99	VO0 Select Data	JP98-2-3
JP93	VO0/ZIF PWM	open	DSW1	PU12	open
JP94	VO0/ZIF GPIO0	open	DSW2	PU14	open
JP95	VO0/ZIF I2C	open	DSW3	PD12	open
JP96	VO0/HDMI DataEnable	open	DSW4	PD14	open
JP97	VO0/HDMI I2C	open	DSW5	PU15	open
JP74	VO1/VI1 DataEnable	open	DSW6	PD15	open
JP75	VO1 Select Data Enable 2	2-3	DSW7	PU09	open
JP76	VO1/ZIF DataEnable	open	DSW8	PU11	open
JP77	VO1/ZIF PWM	open	DSW9	PD09	open
JP78	VO1/ZIF GPIO0	open	DSW10	PD11	open
JP79	VO1/ZIF I2C	open	DSW11	PU10	open
JP80	VO1/HDMI DataEnable	open	DSW12	PD10	open
JP81	VO1/HDMI I2C	open	DSW13	PU05	open
JP64	V10 Data Enable	open	DSW14	PU07	open
JP65	V10 Data Enable	open	DSW15	PD05	open
JP66	V10/ZIF Data Enable	open	DSW16	PD07	open

Part No.	Description	Default Position	Part No.	Description	Default Position
DSW17	PU06	open	JP63	SEL_SSIFTXD 1	1-2
DSW18	PU08	open	JP47	SSIF I2C	open
DSW19	PD06	open	JP45	Left Speaker Source	3-5; 4-6
DSW20	PD08	open	JP46	Right Speaker Source	3-5; 4-6
DSW21	PU01	open	JP48	Left AN	1-2
DSW22	PU03	open	JP49	Left BP	closed
DSW23	PD01	open	JP50	Left AP	1-2
DSW24	PD03	open	JP51	Left BN	closed
DSW25	PU02	open	JP52	Right AN	1-2
DSW26	PU04	open	JP53	Right BP	closed
DSW27	PD02	open	JP54	Right AP	1-2
DSW28	PD04	open	JP55	Right BN	closed
SW1	DCURDY	open	JP32	FT#0 Mode Select	1-2
SW2	DCUTMS	PU	JP33	FT#2 Mode Select	1-2
SW3	DCUTDI	PU	JP34	FT#2 Source Select	1-2
SW5	DCUTDO	open	JP35	FT#2 Source Select	1-2
SW7	DCURST	PD	JP36	FT#2 Mux	closed
SW9	DCUTCK	open	JP37	FT#1 Mode Select	1-2
SW4	MODE0	open	JP38	FT#3 Mode Select	2-3
SW8	MODE1	open	JP39	FT#1 Source Select	1-2
SW6	FLMD1	PD	JP40	FT#1 Source Select	1-2
SW10	FLMD0	PD	JP41	FT#3 Mux	closed
JP18	Debugger FLMD0	open	JP42	FT#3 Mux	closed
JP19	Debugger Reset	closed	JP22	RS232/LIN Mux	2-3
JP20	Enable Reset Switch	closed	JP23	LIN Power	2-3
JP21	MOST I2C	open	JP24	LIN Master Select	open
JP43	Ethernet 0 Clock Select	2-3	JP25	LIN Termination	2-3
JP44	Ethernet 1 Clock Select	2-3	JP26	LIN Wake EN	open
JP100	ISO+5V Select	PWRGD	JP27	LIN SLP EN	open
JP101	ISO+3.3V Select	PWRGD	JP28	CAN Split	open
JP102	SDRBVCC Select	PWRGD	JP29	CAN Termination	open
JP103	ISOVDD Select	PWRGD	JP30	CAN Mux	2-3
JP56	SEL_SSIFACK	1-2	JP31	CAN Termination	open
JP57	SEL_SSIFSCK0	1-2	DSW29	HMI Select	open
JP58	SEL_SSIFSCK1	open	DSW31	MUX Select	
JP59	SEL_SSIFWS0	1-2	.8	VO0MUX_SEL1	ON (Low)
JP60	SEL_SSIFWS1	open	.7	VO0MUX_SEL2	ON (Low)
JP61	SEL_SSIFTXD2	open	.6	VO1MUX_SEL1	ON (Low)
JP62	SEL_SSIFTXD0	2-3	.5	VO1MUX_SEL2	ON (Low)
			.4	VINMUX_SEL	ON (Low)
			.3	AUDIOMUX_SEL	OFF (High)
			.2	n.c.	-
			.1	n.c.	-

11.2 Components list

Table 11-2: Components list of the D1x Mango Main Board

Item	Ref	Components	Type	Manufacturer	Name
1	CN4, CN3	5148292-5	←	TE	Connector
2	CN5	PREC015DFAN-RC	←	SULLINS	Pin header
3	CN6	1321609	←	FRIWO	Connector
4	CN7	973582101	←	Hirschmann	Banana jack
5	CN8	973582100	←	Hirschmann	Banana jack
6	CN9, CN10, CN11, CN12, CN13, CN14	PREC032SAAN-RC	←	SULLINS	Pin header
7	CN15	*PREC003DFAN-RC	←	SULLINS	Pin header
8	CN16	D2514-6002-AR	←	3M	Connector
9	CN17	PREC012DFAN-RC	←	SULLINS	Connector
10	CN18, CN19, CN20	PREC008DFAN-RC	←	SULLINS	Connector
11	CN21, CN22, CN52	QSH-020-01-L-D-DP-A	←	SAMTEC	Connector
12	CN23, CN26, CN27	10090099-S094VLF	←	FCI	D-SUB
13	CN24, CN25, CN28, CN29	MEC1-120-02-L-D-A	←	SAMTEC	Card slot
14	CN30	10090097-P094VLF	←	FCI	D-SUB
15	CN32, CN31	QSH-030-01-L-D-A	←	SAMTEC	Connector
16	CN33, CN34	302-S201	←	ON SHORE	Connector
17	CN35, CN40, CN44	302-S401	←	ON SHORE	Connector
18	CN36, CN41, CN45	IMSA-9827B-50Y929	←	IRISO	Connector
19	CN37	302-S161	←	ON SHORE	Connector
20	CN38	TCS7927-5441177	←	Hosiden	S Connector
21	CN42, CN47	20021111-00012T4LF	←	FCI	Pin header
22	CN43, CN49	10029449-001RLF	←	FCI	HDMI Connector
23	CN48, CN46	302-S101	←	ON SHORE	Connector
24	CN51, CN50	QSH-090-01-L-D-A	←	SAMTEC	Connector
25	C1, C2, C5, C6, C88, C89, C90, C91, C156, C160, C177, C181, C185, C189, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C294, C296, C300, C305, C306, C307, C308, C309	10u/16V/2012/B	GRM21BB3 1C106KE15 L	MURATA	Ceramic chip capacitor
26	C3, C7, C86, C95, C102, C109, C117	1u/16V/1608/B	GRM188B3 1C105KA92 D	MURATA	Ceramic chip capacitor

Item	Ref	Components	Type	Manufacturer	Name
27	C4, C8, C9, C85, C108, C114, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C153, C154, C155, C157, C158, C159, C161, C162, C163, C164, C165, C167, C170, C171, C172, C173, C174, C175, C176, C178, C179, C182, C183, C193, C200, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249, C250, C251, C252, C253, C273, C297, C298, C299, C301, C302, C303, C304	0.1u/16V/1005/B	GRM155B3 1C104KA87 D	MURATA	Ceramic chip capacitor
28	C10	1000p/16V/1608/B	←	MURATA	Ceramic chip capacitor
29	C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C180, C184	2.2u/16V/1608/B	GRM188B3 1C225KE14 D	MURATA	Ceramic chip capacitor
30	C87, C96, C97, C103, C104, C110, C111, C118, C119	47u/16V/3225/B	GRM32EB1 C476KE15L	MURATA	Ceramic chip capacitor
31	C92, C93, C98, C99, C100, C105, C106, C112, C113, C120, C121	10u/25V/3216/B	GRM31CB3 1E106KE75 L	MURATA	Ceramic chip capacitor
32	C94, C101, C107, C115, C122, C194, C195, C196, C197, C198, C199	4700p/50V/1005/B	GRM155B1 1H472KA01 D	MURATA	Ceramic chip capacitor
33	C116	0.022u/16V/1608/B	←	MURATA	Ceramic chip capacitor
34	C133, C134, C135, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152	0.022u/16V/1005/B	←	MURATA	Ceramic chip capacitor
35	C166	C2012X5R1V226M125 AC	←	TDK	Ceramic chip capacitor
36	C168	1000p/16V/1005/B	←	MURATA	Ceramic chip capacitor
37	C169	220p/16V/1005/B	←	MURATA	Ceramic chip capacitor
38	C190, C186	0.47u/16V/2012/B	←	MURATA	Ceramic chip

Item	Ref	Components	type	Manufacturer	Name
					capacitor
39	C187, C188, C191, C192	0.047u/16V/1005/B	←	MURATA	Ceramic chip capacitor
40	DSW1, DSW2, DSW3, DSW4, DSW5, DSW6, DSW7, DSW8, DSW9, DSW10, DSW11, DSW12, DSW13, DSW14, DSW15, DSW16, DSW18, DSW20, DSW22, DSW24, DSW25, DSW26, DSW27, DSW28, DSW29, DSW31	218-8LPST	←	CTS	DIPswitch
41	DSW17, DSW19, DSW21, DSW23, DSW30	218-4LPST	←	CTS	DIPswitch
42	D1	MM3Z5V6ST1G	←	ON SEMI	Diode
43	D2, D7, D9, D11, D12, D14, D15	HSU-83	←	RENESAS	Diode
44	D4, D3	STTH4R02U	←	ST MICRO	Diode
45	D6, D5	BAV70LT1G	←	ON SEMI	Diode
46	D10, D13	MBR0520LT1G	←	ON SEMI	Diode
47	F1	RGEF400	←	TE	Fuse
48	F2	MFU0805FF00500P100	←	VISHAY	Fuse
49	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP12, JP13, JP15, JP16	XJ8C-0811	←	OMRON	Jumper
50	JP10, JP11, JP14, JP22, JP23, JP25, JP30, JP32, JP33, JP34, JP35, JP37, JP38, JP39, JP40, JP43, JP44, JP48, JP50, JP52, JP54, JP56, JP57, JP59, JP62, JP63, JP70, JP71, JP72, JP73, JP75, JP82, JP84, JP85, JP86, JP87, JP88, JP89, JP91, JP98, JP106	XJ8D-0311	←	OMRON	Jumper
51	JP18, JP19, JP20, JP24, JP26, JP27, JP28, JP29, JP31, JP41, JP42, JP49, JP51, JP53, JP55, JP58, JP60, JP61, JP64, JP65, JP66, JP67, JP68, JP74, JP76, JP77, JP78, JP80, JP90, JP92, JP93, JP94, JP96, JP100, JP101, JP102, JP103, JP104, JP105	XJ8C-0211	←	OMRON	Jumper
52	JP21, JP36, JP47, JP69, JP79, JP81, JP95, JP97	XJ8C-0411	←	OMRON	Jumper
53	JP45, JP46	XJ8D-0611	←	OMRON	Jumper
54	JP83, JP99	XJ8B-0111	←	OMRON	Jumper
55	J1, J2	PJ-050AH	←	CUI	Jumper

Item	Ref	Components	type	Manufacturer	Name
56	LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11, LED12, LED13, LED14, LED15, LED16, LED17, LED18, LED19, LED20, LED21, LED22, LED23, LED24, LED25, LED26, LED27, LED28, LED29, LED30, LED31, LED32, LED33, LED34, LED35, LED36, LED37, LED38, LED39, LED40	PG1112H	←	STANLEY	LED
57	LS2, LS1	AST-02308MR-R	←	PUI AUDIO	Speaker
58	L1, L2, L15, L22, L23	BLM21PG300SN1D	←	MURATA	Filter
59	L3, L4, L5, L6, L7, L8, L9, L10	NFE31PT222Z1E9	←	MURATA	Filter
60	L11, L12, L13, L14	SRN6045-100M	←	BOURNS	Coil
61	PAD1, PAD4, PAD23, PAD26	PIN11	←		
62	PAD2, PAD5, PAD24, PAD27	PIN9	←		
63	PAD3, PAD6, PAD25, PAD28	PIN7	←		
64	PAD7, PAD8, PAD29, PAD30	PIN27	←		
65	PAD9, PAD10, PAD31, PAD32	PIN29	←		
66	PAD11, PAD12, PAD33, PAD34	PIN31	←		
67	PAD13, PAD15, PAD35, PAD37	PIN33	←		
68	PAD14, PAD16, PAD36, PAD38	PIN34	←		
69	PAD17, PAD18, PAD39, PAD40	PIN36	←		
70	PAD19, PAD20, PAD41, PAD42	PIN38	←		
71	PAD21, PAD22, PAD43, PAD44	PIN40	←		
72	Q1, Q2, Q3, Q4, Q8, Q9, Q10	DTD143EK	←	ROHM	Transistor
73	Q5, Q6, Q7	BC847B-7-F	←	DIODES	Transistor
74	Q11, Q12, Q15, Q16	2SJ557	←	RENESAS	FET
75	Q13, Q14, Q17, Q18	2SK3105	←	RENESAS	FET
76	RA1, RA2, RA3, RA4, RA5, RA6, RA7, RA8, RA9, RA10, RA11, RA12, RA13, RA14, RA15, RA16, RA17, RA18, RA19, RA20, RA21, RA22, RA23, RA24, RA25, RA26, RA27, RA28, RA29, RA30, RA31, RA32, RA33, RA34, RA35, RA36, RA37, RA38, RA39, RA40, RA41, RA42, RA43, RA44, RA45, RA46, RA47, RA48, RA49, RA50, RA51, RA52	CN1E4ATD223J	←	KOA	Resistor array

Item	Ref	Components	Type	Manufacturer	Name
77	R1, R2, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23	5.1K/1005/1%	RK73H1ETT D5101F	KOA	Chip resistor
78	R3, R226, R227, R230, R231	12K/1608/1%	RK73H1JTT D1202F	KOA	Chip resistor
79	R24, R39, R43, R47, R52, R58, R62, R87, R95, R153, R159, R166, R167, R168, R173, R217, R219, R220, R221, R306, R307, R383, R470, R476	0ohm/1005/1%	←		Chip resistor
80	R25, R93, R191, R212, R311, R387, R472, R475	*0ohm/1005/1%	←	KOA	Chip resistor
81	R26	5.6K/1005/1%	RK73H1ETT D5601F	KOA	Chip resistor
82	R27, R30, R145, R146, R147, R149, R150	47K/1005/1%	RK73H1ETT D4702F	KOA	Chip resistor
83	R28	39K/1005/1%	RK73H1ETT D3902F	KOA	Chip resistor
84	R29	43K/1005/1%	RK73H1ETT D4302F	KOA	Chip resistor
85	R31, R33	27K/1005/1%	RK73H1ETT D2702F	KOA	Chip resistor
86	R32, R37, R38, R51, R57, R65, R66, R92, R94, R152, R155, R162, R163, R164, R165, R169, R170, R171, R172, R214, R215, R232, R233, R303, R304, R308, R313, R318, R319, R379, R380, R381, R384, R389, R393, R394, R395, R457, R458, R459, R460, R471, R473, R474	10K/1005/1%	RK73H1ETT D1002F	KOA	Chip resistor
87	R34	100K/1005/1%	RK73H1ETT D1003F	KOA	Chip resistor
88	R35	120K/1005/1%	RK73H1ETT D1203F	KOA	Chip resistor
89	R36	15K/1005/1%	RK73H1ETT D1502F	KOA	Chip resistor
90	R40, R44, R48, R53, R59	220ohm/1005/1%	RK73H1ETT D2200F	KOA	Chip resistor
91	R41	750ohm/1608/1%	RK73H1JTT D7500F	KOA	Chip resistor
92	R461, R42	8.2K/1608/1%	RK73H1JTT D8201F	KOA	Chip resistor
93	R55, R45	240ohm/1608/1%	RK73H1JTT D2400F	KOA	Chip resistor
94	R56, R46	1.1K/1608/1%	RK73H1JTT D1101F	KOA	Chip resistor
95	R49, R60	180ohm/1608/1%	RK73H1JTT D1800F	KOA	Chip resistor
96	R50, R61	2K/1608/1%	RK73H1JTT D2001F	KOA	Chip resistor
97	R54	100K/1608/1%	RK73H1JTT D1003F	KOA	Chip resistor

Item	Ref	Components	Type	Manufacturer	Name
98	R63, R64, R67, R68, R69, R70, R71, R72, R74, R76, R78, R80, R82, R84, R222, R223, R284, R321, R322, R397, R398	3.3K/1005/1%	RK73H1ETT D3301F	KOA	Chip resistor
99	R73, R75, R77, R79, R81, R83, R85, R86, R96, R98, R100, R102, R104, R106, R107, R108	22K/1005/1%	RK73H1ETT D2202F	KOA	Chip resistor
100	R88, R90, R91, R97, R99, R101, R103, R105, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R154, R314	1K/1005/1%	RK73H1ETT D1001F	KOA	Chip resistor
101	R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123, R124, R125, R126, R127, R128	2.2K/1005/1%	RK73H1ETT D2201F	KOA	Chip resistor
102	R151, R148	0ohm/2012/1%	←	KOA	Chip resistor
103	R156	12K/1005/1%	RK73H1ETT D1202F	KOA	Chip resistor
104	R157, R158, R160, R161	30ohm/1005/1%	RK73H1ETT P30R0F	KOA	Chip resistor
105	R192, R213	0ohm/1608/1%	←	KOA	Chip resistor
106	R218, R216	ERJ-1TNF22R0U	←	PANASONIC	Chip resistor
107	R224, R225, R228, R229	1K/1608/1%	RK73H1JTT D1001F	KOA	Chip resistor
108	R261, R263, R264, R266, R267, R269, R270, R272, R279, R280, R282, R283	33ohm/1005/1%	RK73H1ETT P33R0F	KOA	Chip resistor
109	R262, R265, R268, R271	18ohm/1005/1%	RK73H1ETT P18R0F	KOA	Chip resistor
110	R273, R274, R275, R276	56ohm/1005/1%	RK73H1ETT P56R0F	KOA	Chip resistor
111	R277	4.7K/1005/1%	RK73H1ETT D4701F	KOA	Chip resistor
112	R278	75ohm/1005/1%	RK73H1ETT P75R0F	KOA	Chip resistor
113	R281	*33ohm/1005/1%	←	KOA	Chip resistor
114	R305, R382	510ohm/1005/1%	RK73H1ETT D5100F	KOA	Chip resistor
115	R309, R320, R385, R396	100ohm/1005/1%	RK73H1ETT D1000F	KOA	Chip resistor
116	R310, R317, R386	*10K/1005/1%	←	KOA	Chip resistor
117	R312, R315, R316, R388, R390, R391, R392	*1K/1005/1%	←	KOA	Chip resistor
118	SW1, SW2, SW3, SW4, SW5, SW6, SW7, SW8, SW9, SW10	G-13AP	←	NKK switches	Toggle switch
119	SW11	2-1437565-9	←	TE	Tactical switch
120	SW12	SKRHABE010	←	ALPS	Button switch
121	SW13	EC12D1524403	←	ALPS	Rotary switch
122	TH1	VR+12V	←		
123	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	HK-5-G-Black	←	MAC8	Test pin

Item	Ref	Components	Type	Manufacturer	Name
124	TP9, TP10, TP11, TP12	HK-5-G-Red	←	MAC8	Test pin
125	TP14, TP13	HK-5-G-Yellow	←	MAC8	Test pin
126	U1	TL1963A-25DCQ	←	TI	Regulator
127	U2	TL1963ADCQ	←	TI	Regulator
128	U3	uPC177G2	←	RENESAS	Comparator
129	U4	SN74LVC1G04DCK	←	TI	Logic IC
130	U5, U7, U8, U12	APXK004A0X-SRZ	←	GE	DC/DC
131	U6	TL1963A-18DCQ	←	TI	Regulator
132	U9	APXS002A0X-SRZ	←	GE	DC/DC
133	U10	SN74LVC1G08DCK	←	TI	Logic IC
134	U11	SN74LVC1G34DCK	←	TI	Logic IC
135	U13, U14, U25, U33	PCA9306DP1	←	NXP	Level convert IC
136	U15	BD45271G	←	ROHM	RESET IC
137	U16	MAX3221CPW	←	TI	RS232 IC
138	U17	TJA1020T	←	NXP	LIN IC
139	U18	TJA1041T	←	NXP	CAN IC
140	U19	LM49450SQ	←	NS	Audio CODEC
141	U20, U23, U26, U27, U28, U29, U34, U35, U36, U37	FST16233MTDX	←	FAIRCHILD	Bus switch
142	U21	SAA7113H	←	NXP	CVBS receiver
143	U24, U32	TFP410PAP	←	TI	HDMI driver
144	U38	SN74LVC541APW	←	TI	Logic IC
145	VR1, VR2, VR3	TM-7EP 10K	←	COPAL	Variable resistor
146	Y1, Y4	*ASFL1-125.000MHZ-EC-T	←	ABRACON	Oscillator
147	Y2	ASFL1-24.576MHZ-EC-T	←	ABRACON	Oscillator
148	Schematic Ref=1.0	240191001	←	Hartec	PCB
149	JPxx	XJ8A-0211	←	OMRON	Jumper socket
150		ASB-308E	←	Hirosugi keiki	Spacer
151		B-0305-S1	←	Hirosugi keiki	Screw

11.3 Schematics of the D1x Mango Main Board

The following pages contain the full schematics of the Mango Main Board. This also includes the schematic of the separate MIPI Board Interface PCB.

For the schematics of the Adapter Boards, please see the dedicated adapter board manuals.

RH850(mango) Main Board Rev1.4

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5	VOUT0 MUX2	1.3
6	VOUT0 HDMI	1.0
7	VOUT0 CONNECTOR	1.0
8	VOUT1 MUX1	1.3
9	VOUT1 MUX2	1.3
10	VOUT1 HDMI	1.0
11	VOUT1 CONNECTOR	1.0
12	VIN MUX	1.3
13	VIN HDMI	1.0
14	CVBS	1.0
15	VIN CONNECTOR	1.0
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18	ETHER	1.0
19	UART/LIN/CAN(card)	1.0
20	UART/LIN/CAN(onboard)	1.1
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22	POTENTIOMETER & LED	1.0
23	BUTTON & ROTARY	1.0
24	DEBUG	1.2
25	VG CONNECTOR1A	1.2
26	VG CONNECTOR1B	1.2
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28	VG CONNECTOR2A	1.2
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30	VG CONNECTOR2C	1.2
31	POWER(input)	1.0
32	POWER(cpu1)	1.1
33	POWER(cpu2)	1.0
34	POWER(pgOOD)	1.0
35	POWER(ext)	1.0
36	POWER(p_matrix)	1.0

Revision History

DATE	Rev	Page	DESCRIPTION
2014.03.22	1.0		release version
2014.04.28	1.1		U5 Model number change R91,R94 -> NoMount R85 -> 1.1Kohm change R88 -> 5.1Kohm change C162,C163,C164 -> 0.47u change Wire add CN50 60pin <-> R94.1pin(BOARD_RESET)
2014.05.07	1.2		CN3,CN4 Model number change R91 -> 10Kohm change R88 -> 10Kohm change
2014.12.18	1.3		U20,U23,U26,U27,U28,U29,U34,U35,U36,U37 Model number change D7,D9,D11,D12,D14,D15 -> NoMount
2015.12.10	1.4		Q13,Q14,Q17,Q18 -> Symbol change

The schematics in this document are provided "AS IS" and any use will be at the customer's own risk. SHIMAFUJI Electric Inc. provides no representation or warranty (i) for the contents of the schematics or their accuracy; (ii) as to the performance of any product made from any one or more of the schematics; or (iii) that the schematics or any product made from the schematics is or will be free from claims of infringement of patent, copyright, mask work rights and other forms of intellectual property.

Note

*All resistors 1% accuracy

*For more information check the bill of materials

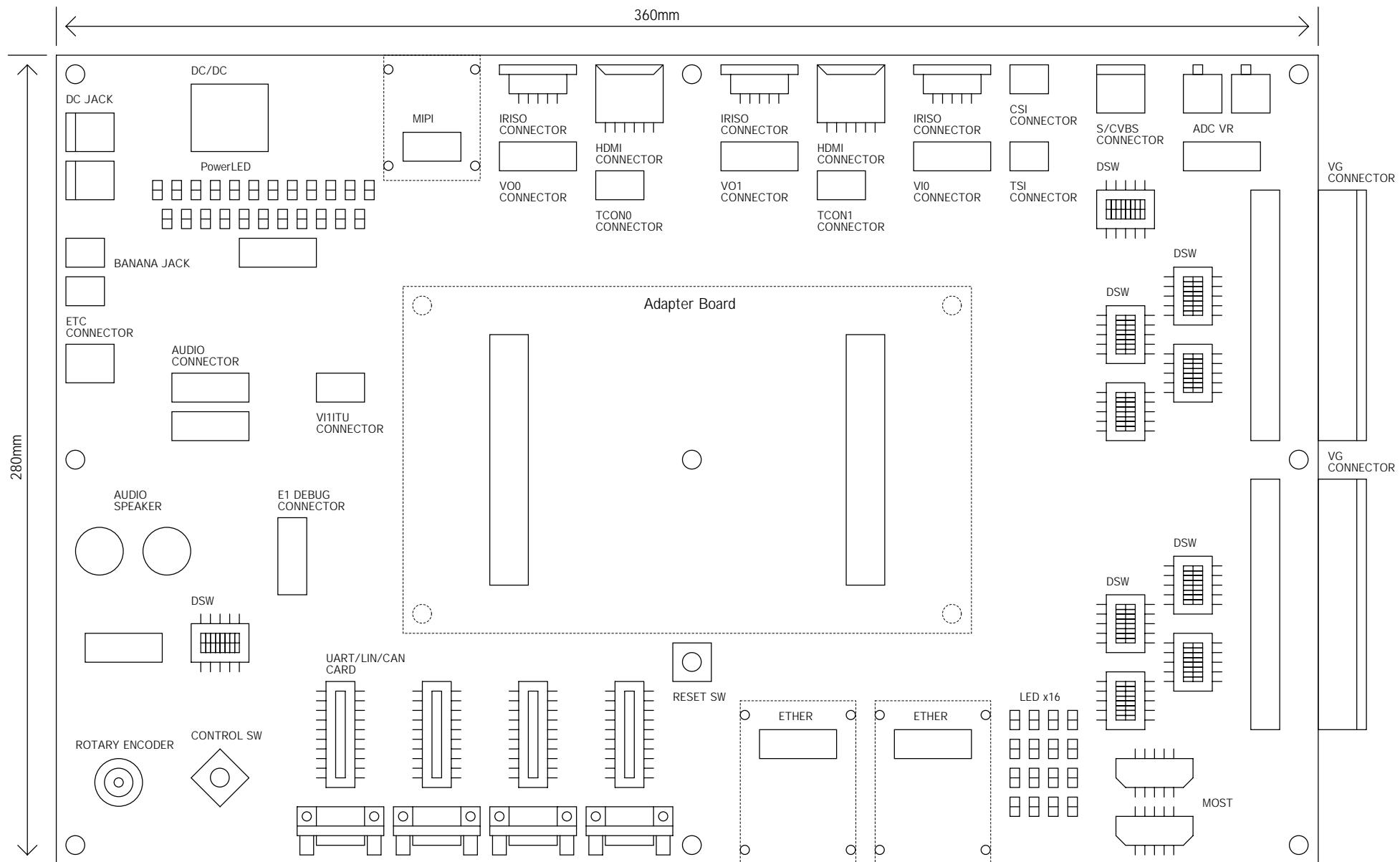
*GND guard  *Equal-length wiring  *Impedance  *No Mount 

NetList Result
1002 Parts, 67 Library Parts, 1265 Nets, 5098 Pins

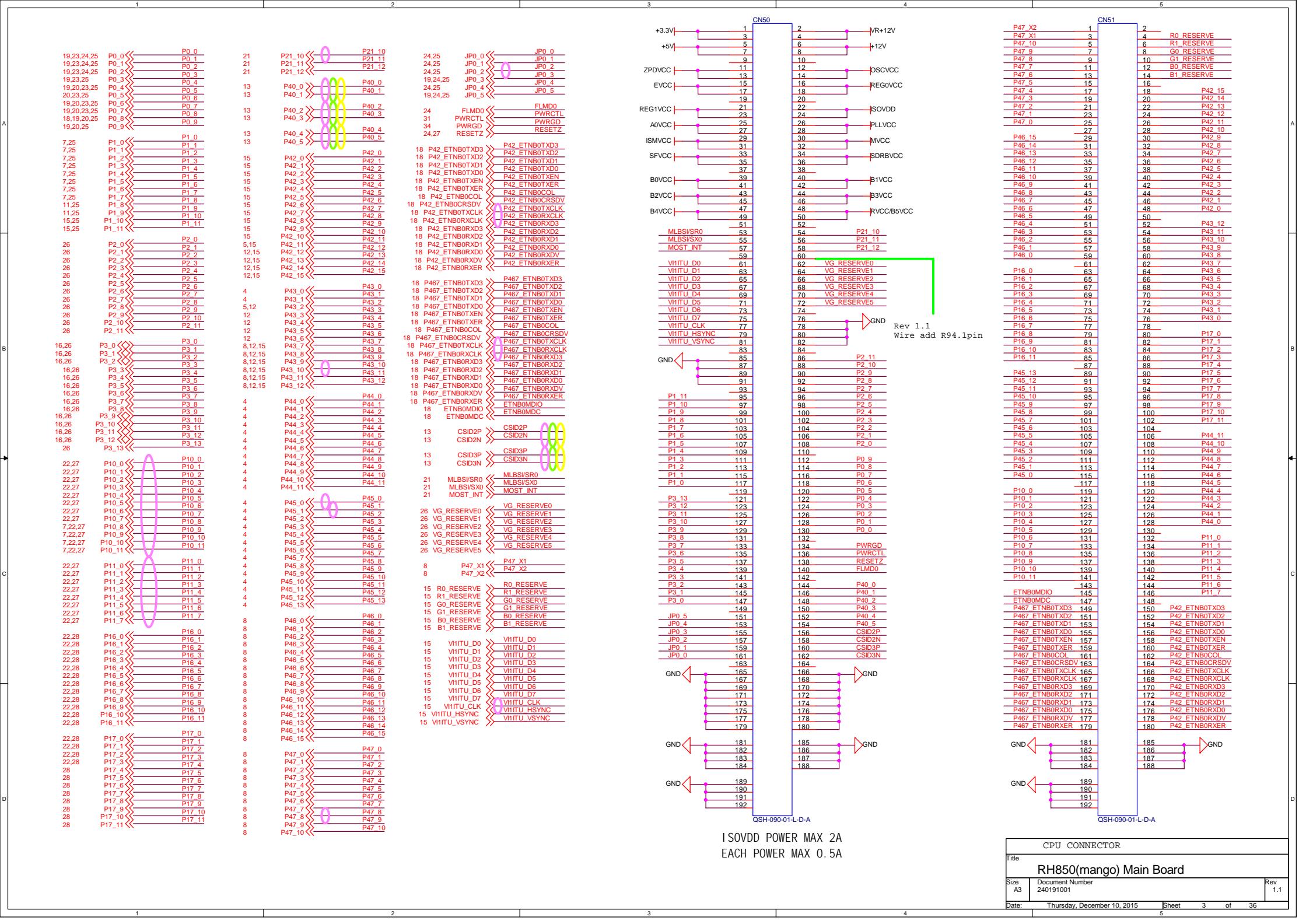
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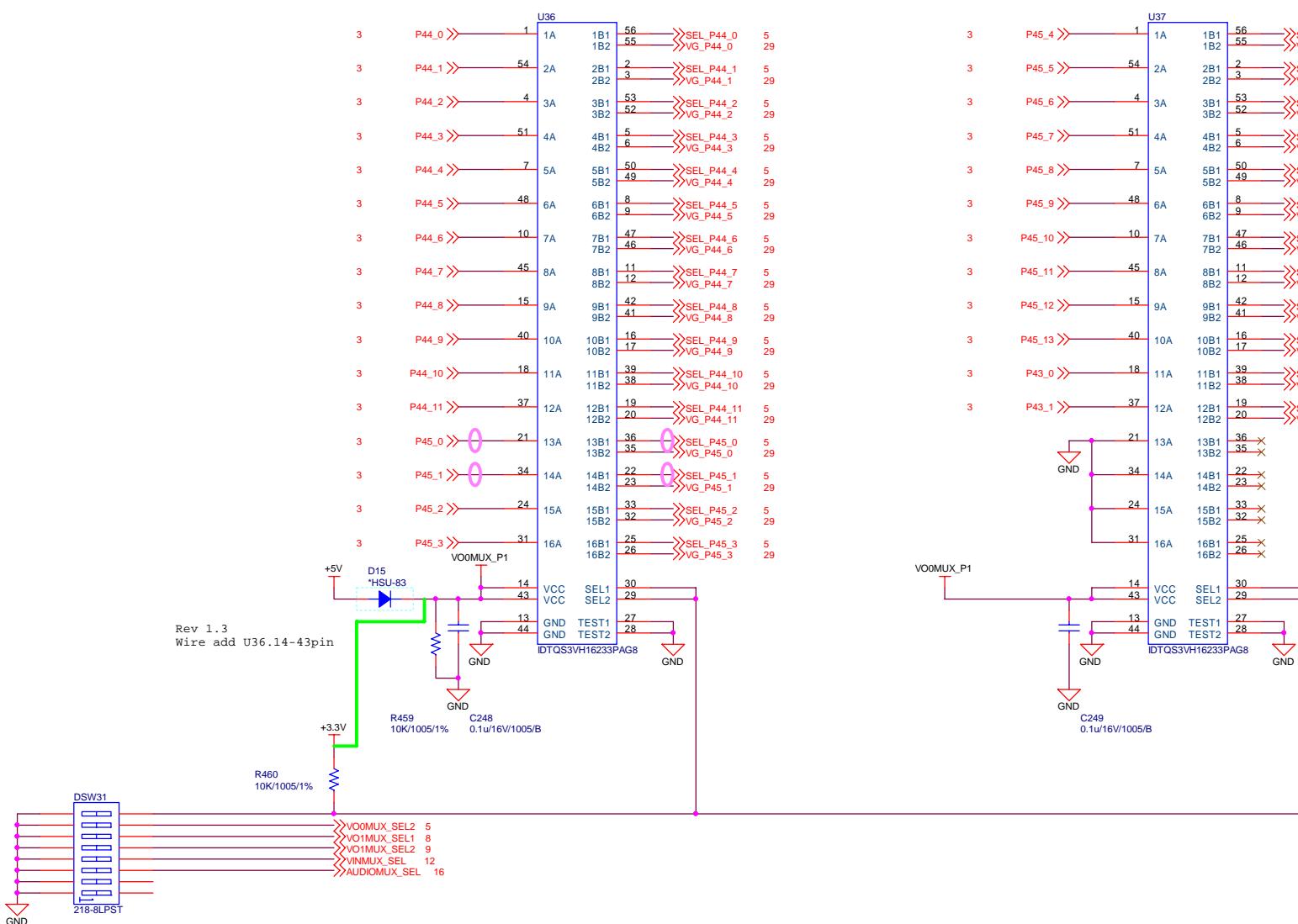
RH850(mango) Main Board Block Diagram



BLOCK DIAGRAM		
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[V0 0]



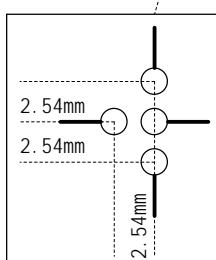
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VideoOUT0 MUX1		
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[V0 0]

SEL_P44_0	VDC_E0_VO_DATA23	SEL_P44_0
SEL_P44_1	VDC_E0_VO_DATA22	SEL_P44_1
SEL_P44_2	VDC_E0_VO_DATA21	SEL_P44_2
SEL_P44_3	VDC_E0_VO_DATA20	SEL_P44_3
SEL_P44_4	VDC_E0_VO_DATA19	SEL_P44_4
SEL_P44_5	VDC_E0_VO_DATA18	SEL_P44_5
SEL_P44_6	VDC_E0_VO_DATA17	SEL_P44_6
SEL_P44_7	VDC_E0_VO_DATA16	SEL_P44_7
SEL_P44_8	VDC_E0_VO_DATA15	SEL_P44_8
SEL_P44_9	VDC_E0_VO_DATA14	SEL_P44_9
SEL_P44_10	VDC_E0_VO_DATA13	SEL_P44_10
SEL_P44_11	VDC_E0_VO_DATA12	SEL_P44_11
SEL_P45_0	VDC_E0_VO_CLKP	SEL_P45_0
SEL_P45_1	VDC_E0_VO_CLKN	SEL_P45_1
SEL_P45_2	VDC_E0_VO_DDATA11	SEL_P45_2
SEL_P45_3	VDC_E0_VO_DDATA10	SEL_P45_3
SEL_P45_4	VDC_E0_VO_DDATA9	SEL_P45_4
SEL_P45_5	VDC_E0_VO_DDATA8	SEL_P45_5
SEL_P45_6	VDC_E0_VO_DDATA7	SEL_P45_6
SEL_P45_7	VDC_E0_VO_DDATA6	SEL_P45_7
SEL_P45_8	VDC_E0_VO_DDATA5	SEL_P45_8
SEL_P45_9	VDC_E0_VO_DDATA4	SEL_P45_9
SEL_P45_10	VDC_E0_VO_DDATA3	SEL_P45_10
SEL_P45_11	VDC_E0_VO_DDATA2	SEL_P45_11
SEL_P45_12	VDC_E0_VO_DDATA1	SEL_P45_12
SEL_P45_13	VDC_E0_VO_DDATA0	SEL_P45_13
SEL_P43_0	LCB10HSYNC	SEL_P43_0
SEL_P43_1	LCB10VSYNC	SEL_P43_1

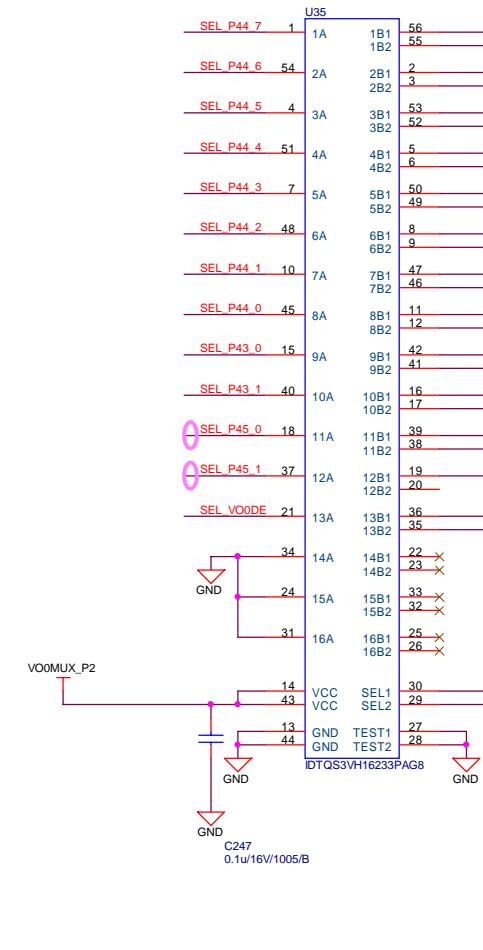
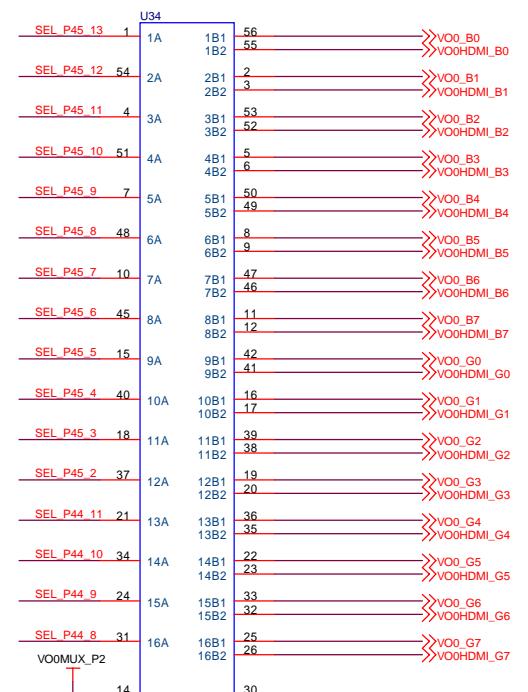
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R458
10K/1005/1%

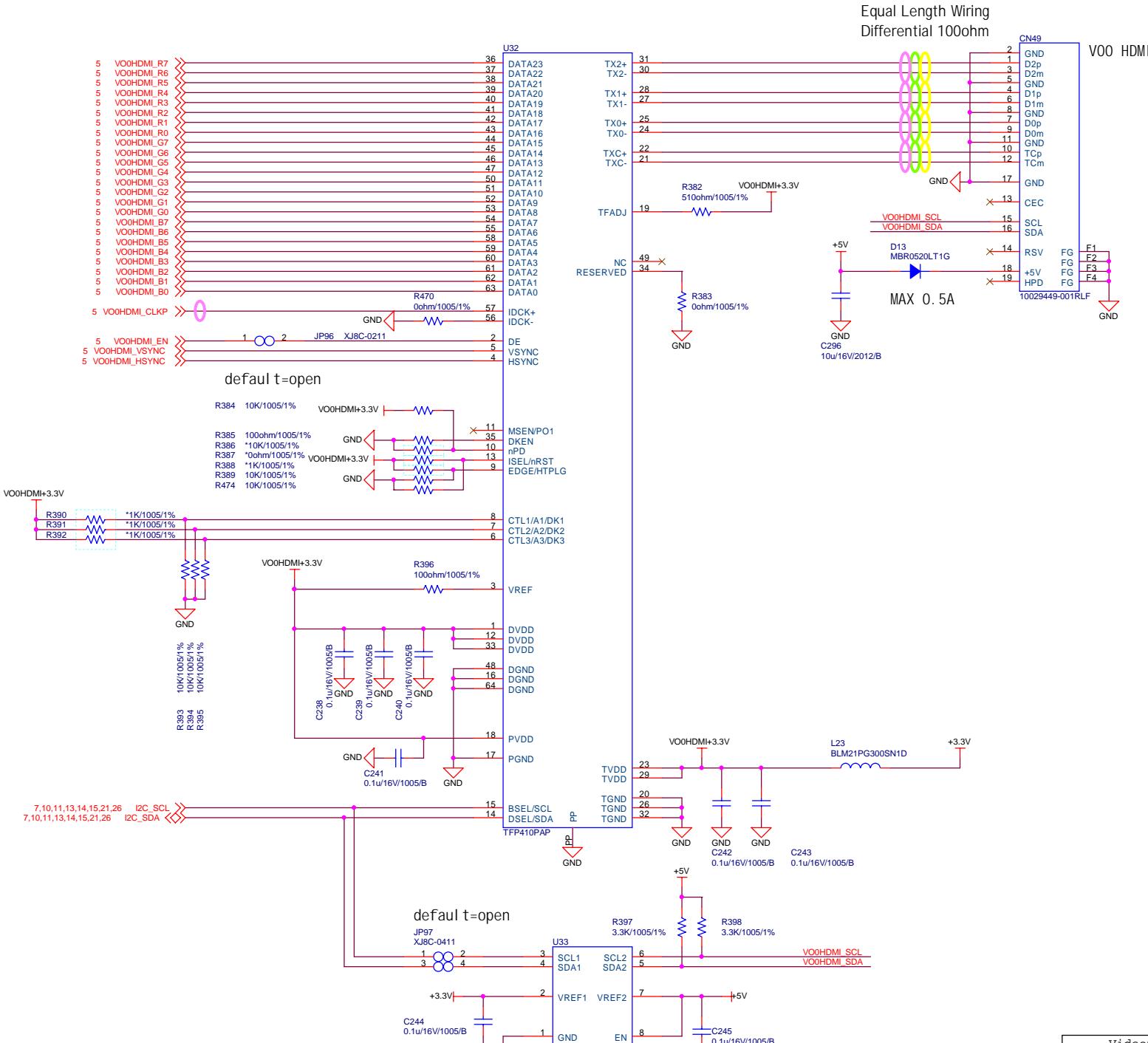
Rev 1.3
Wire add U34.14-43pin

4 VOOMUX_SEL2 >>



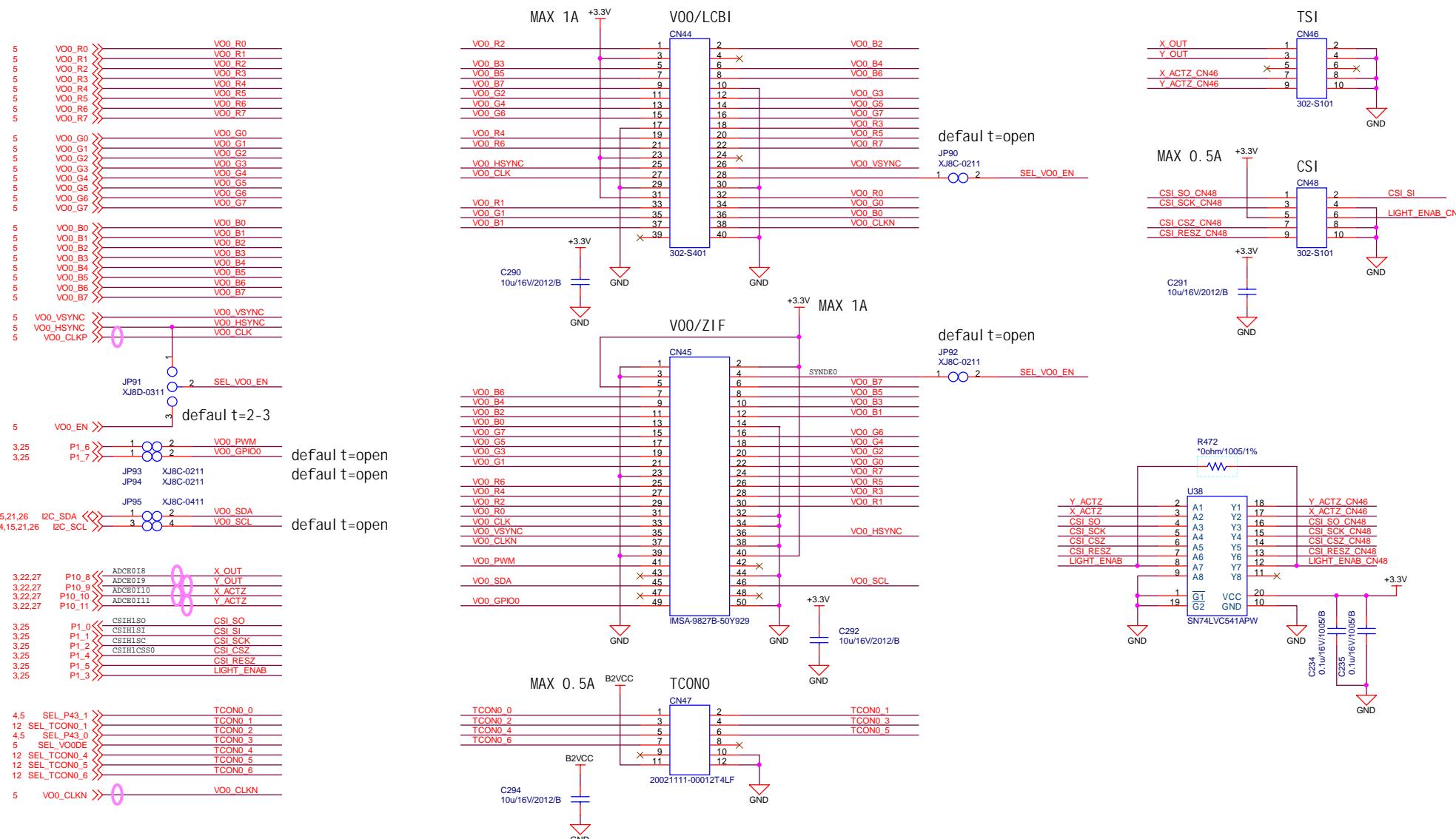
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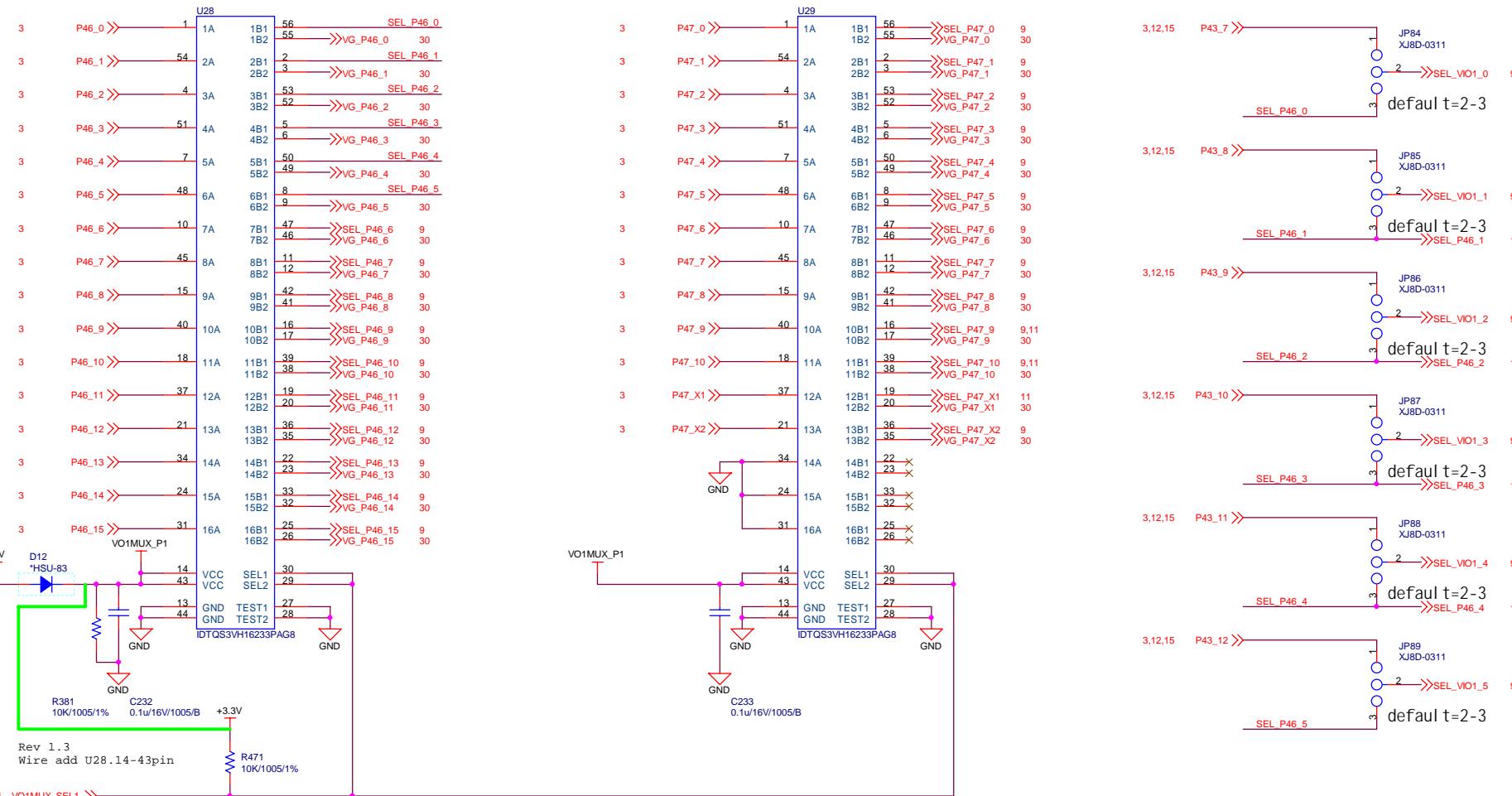


VideoOUT0 HDMI		
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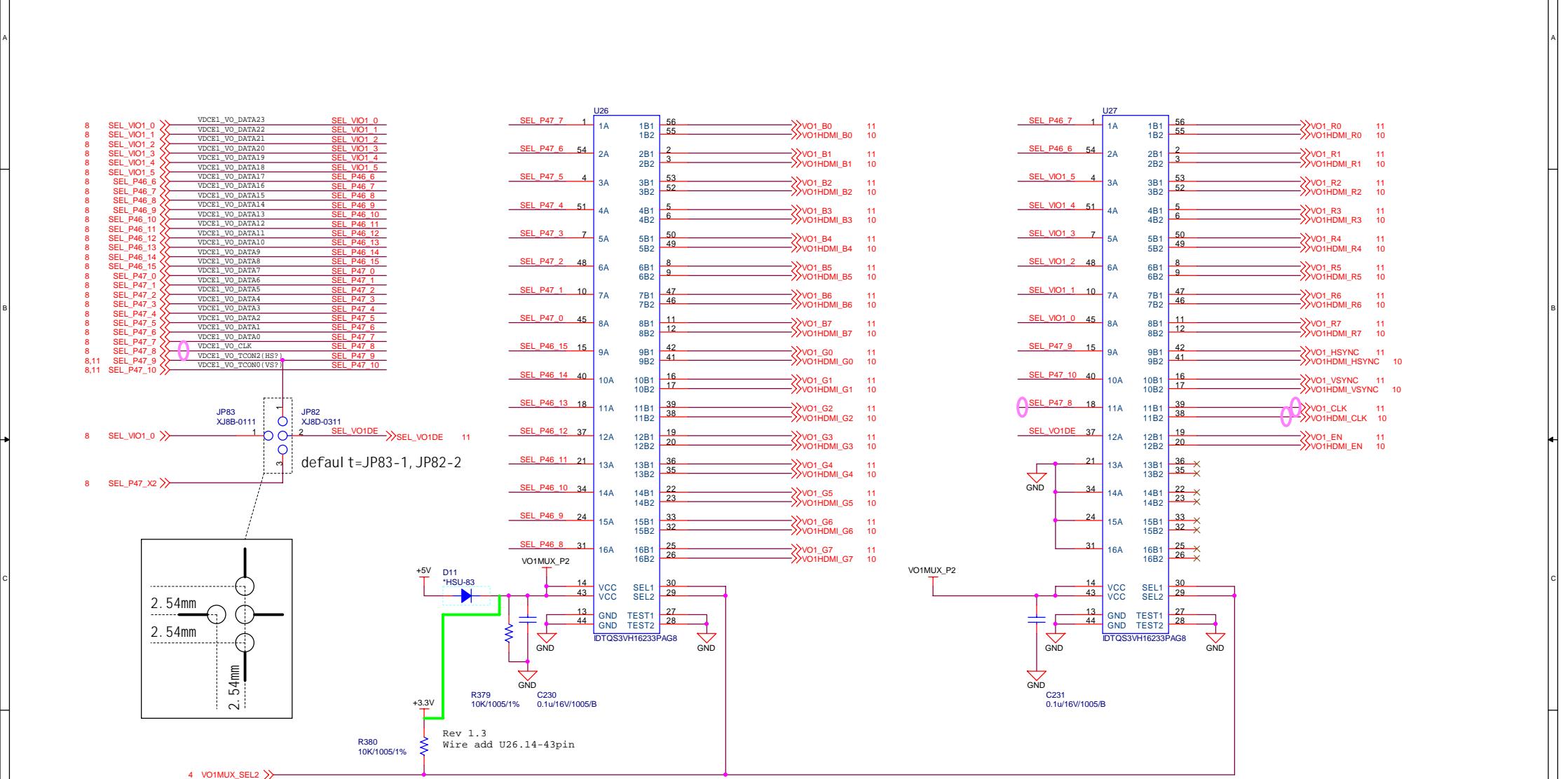


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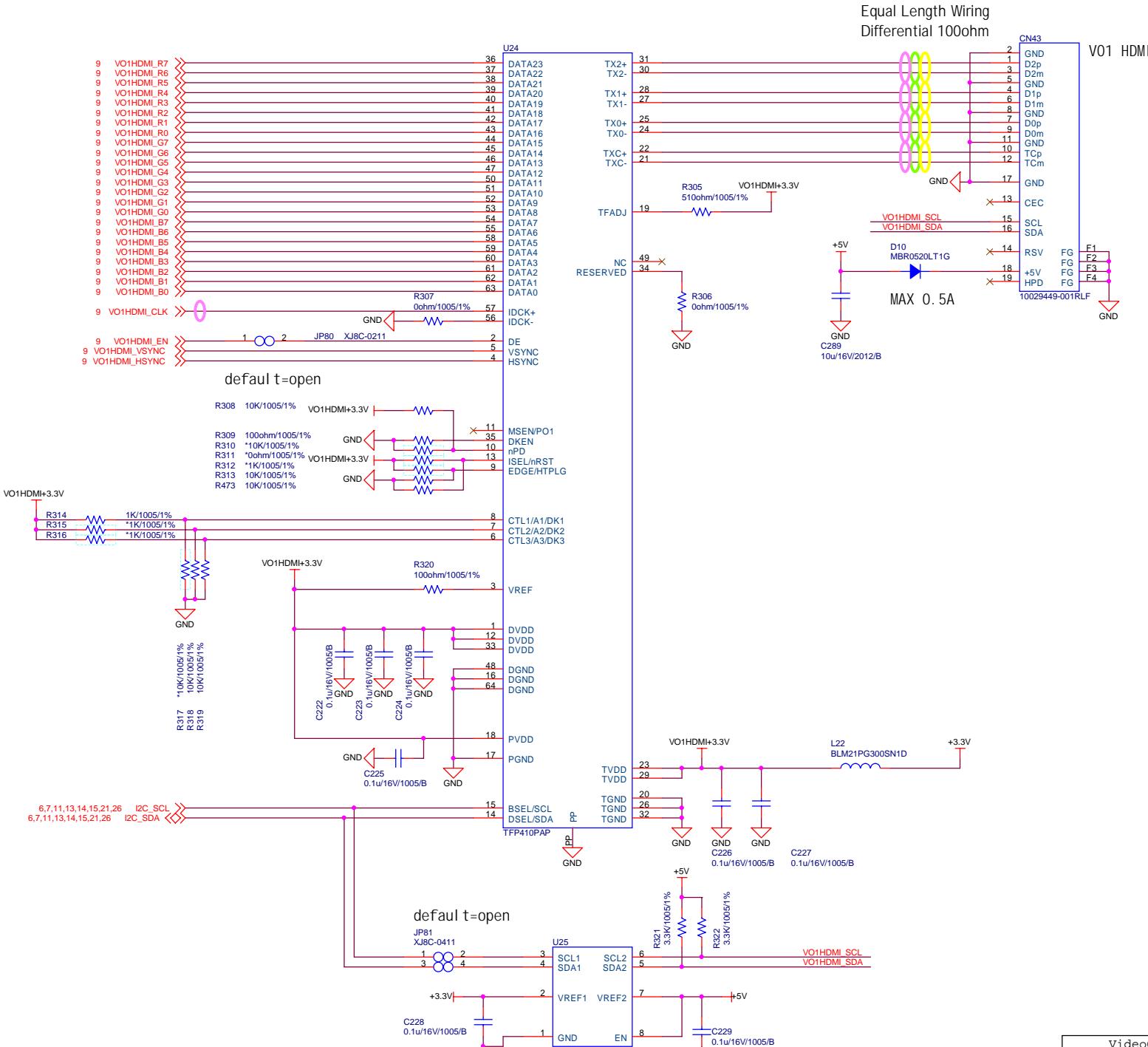
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[V0 1]



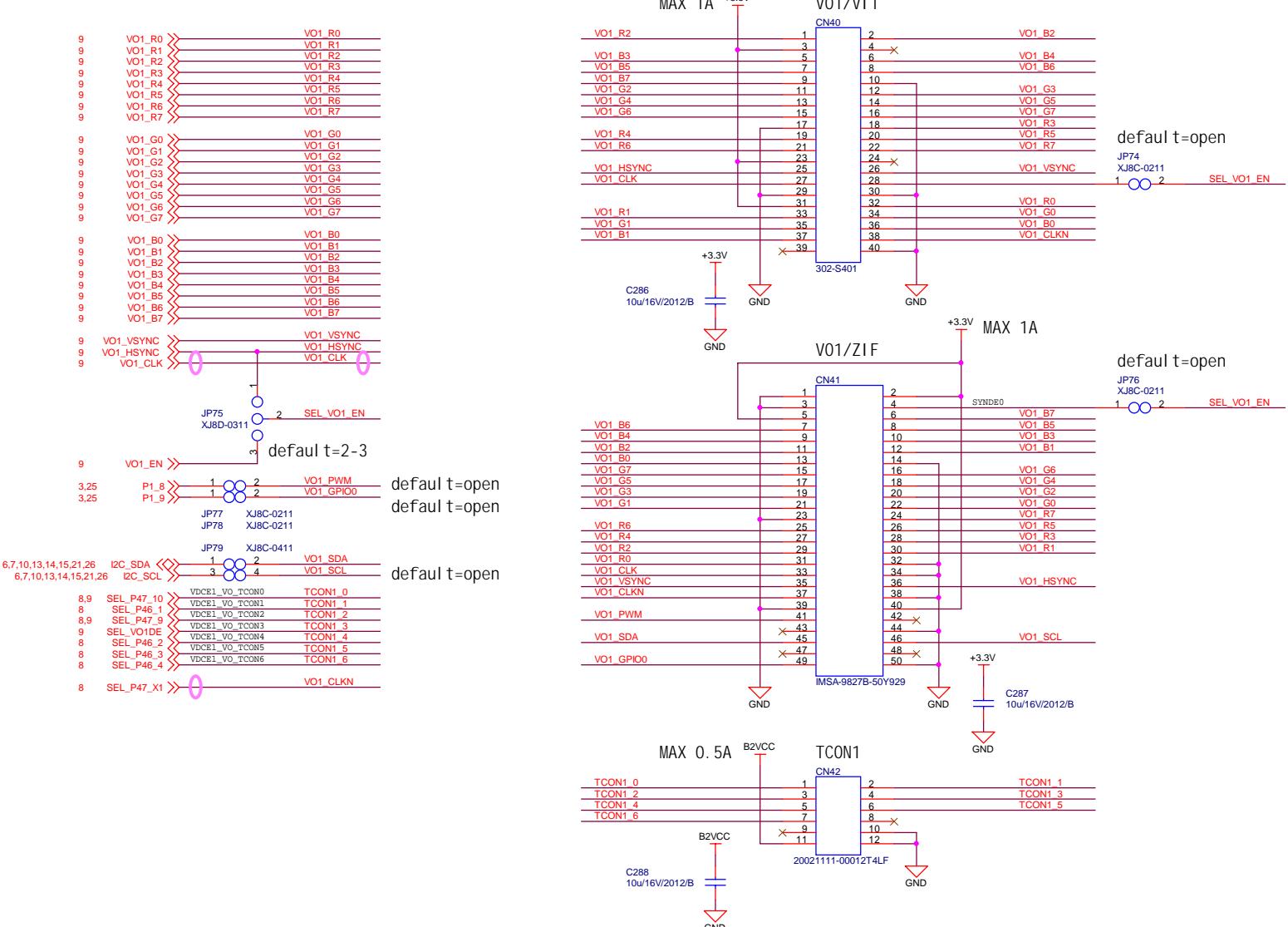
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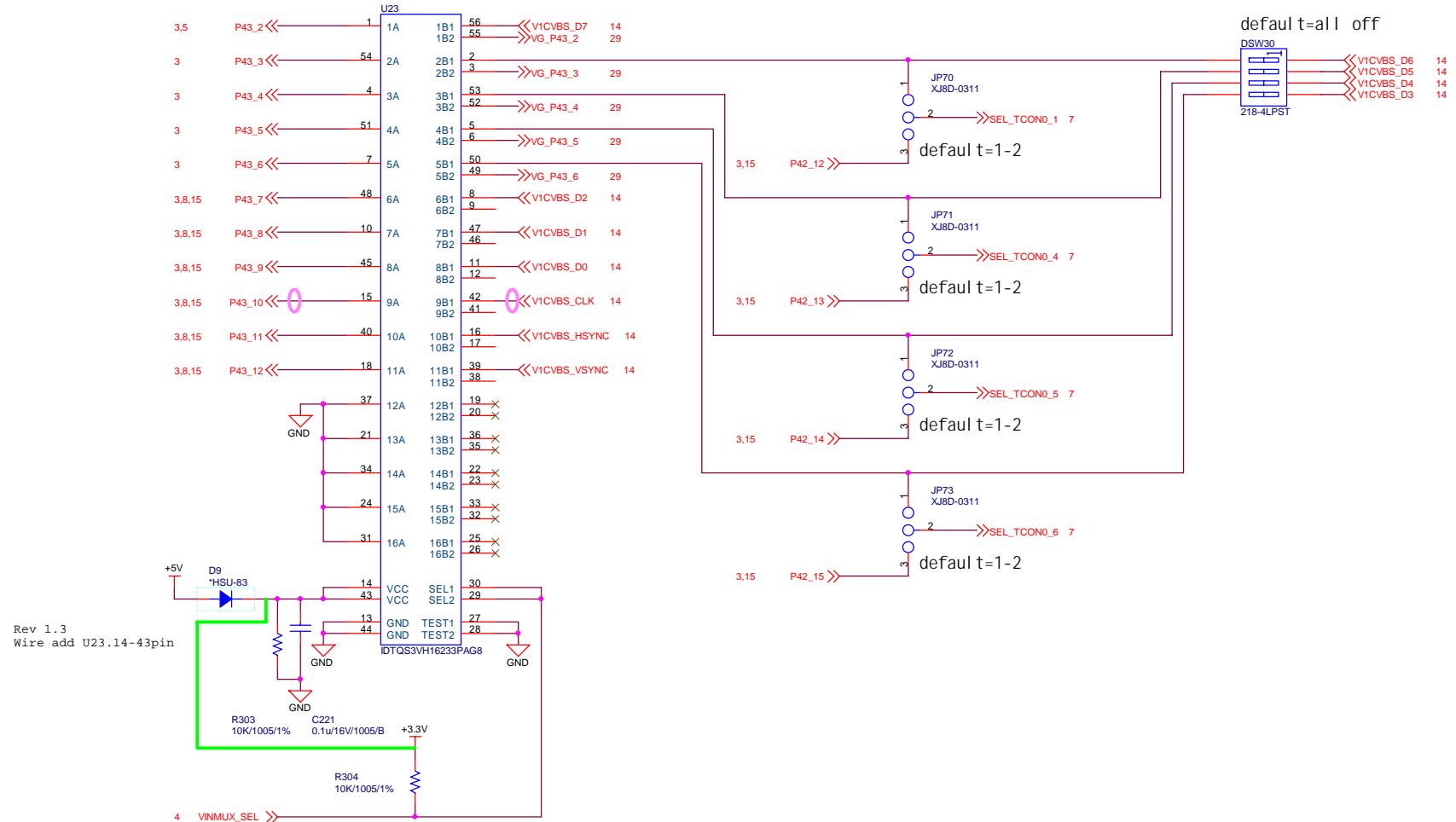
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[V0 1]



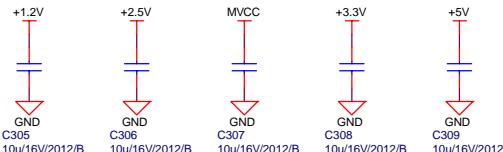
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[VI 0, 1]

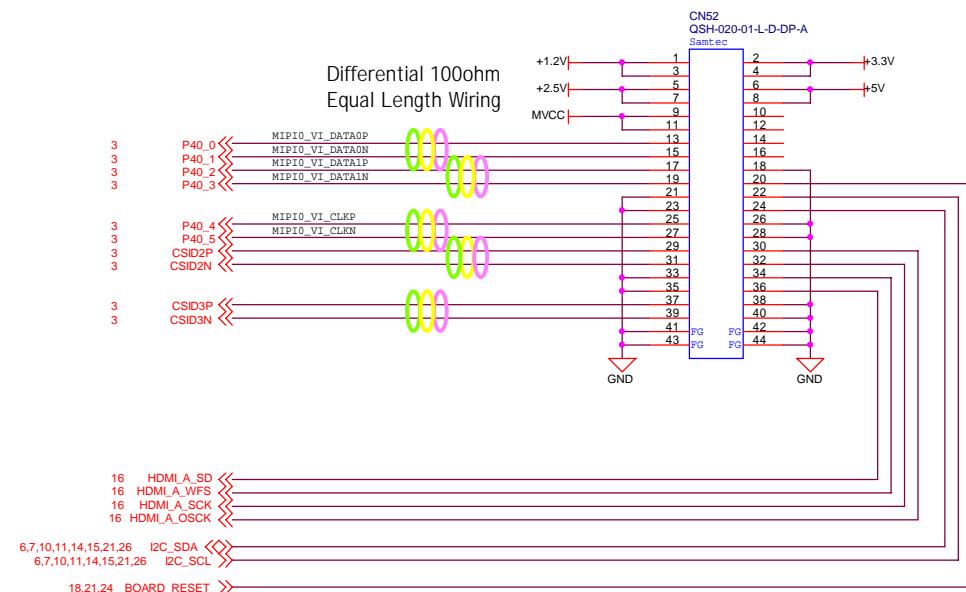


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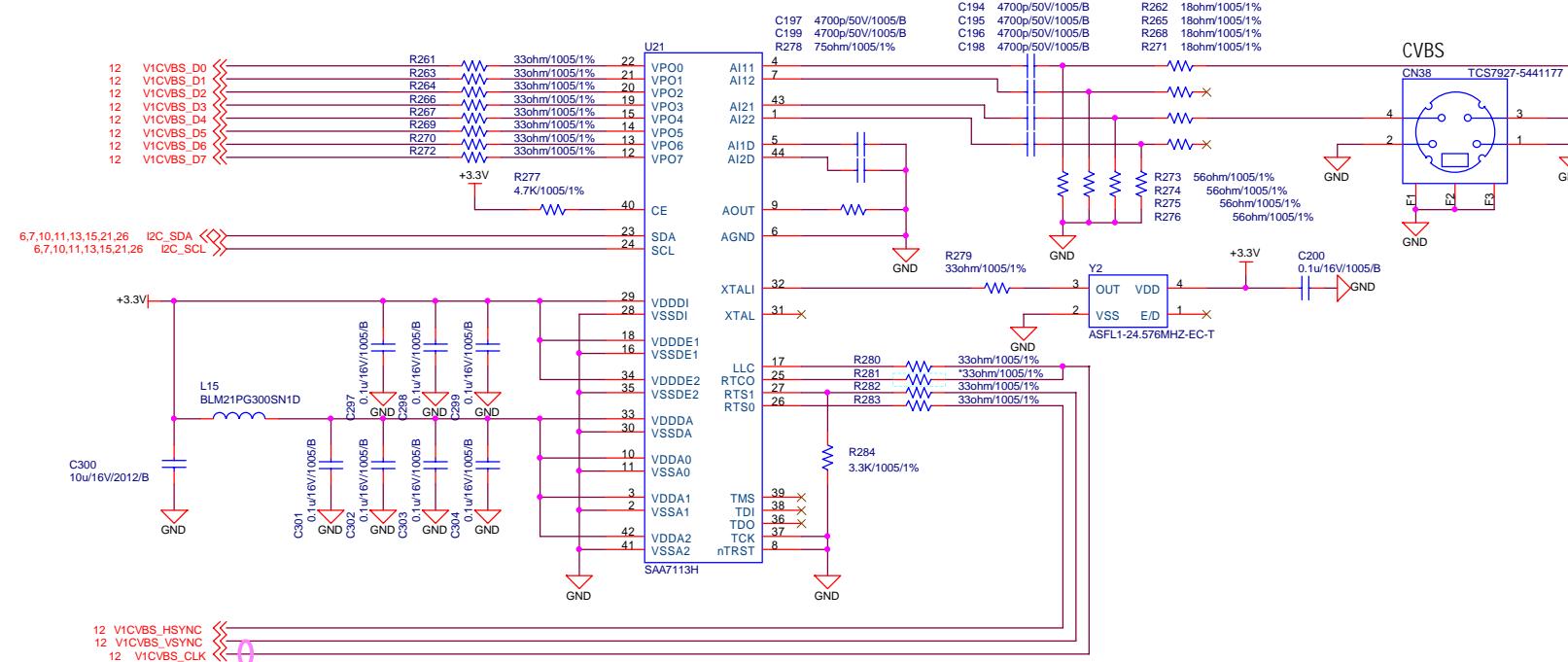
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EACH POWER MAX 0.5A

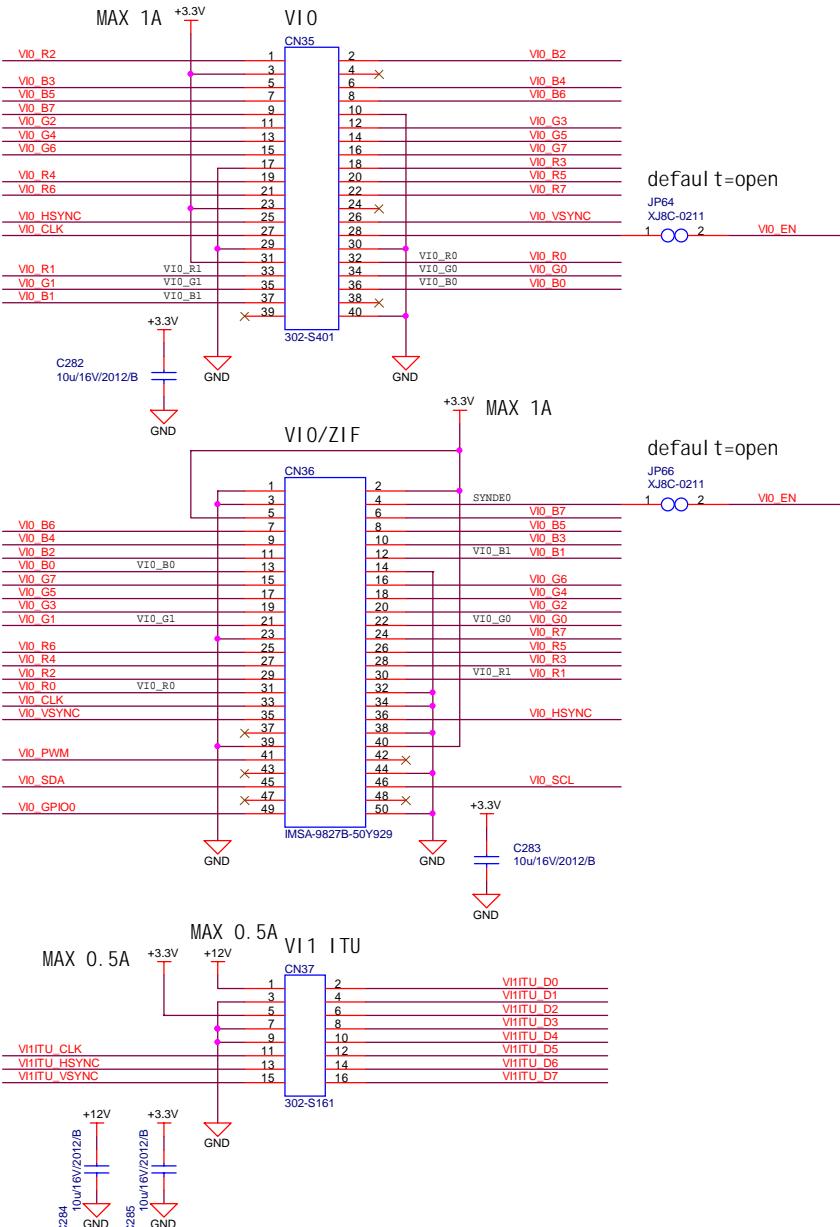
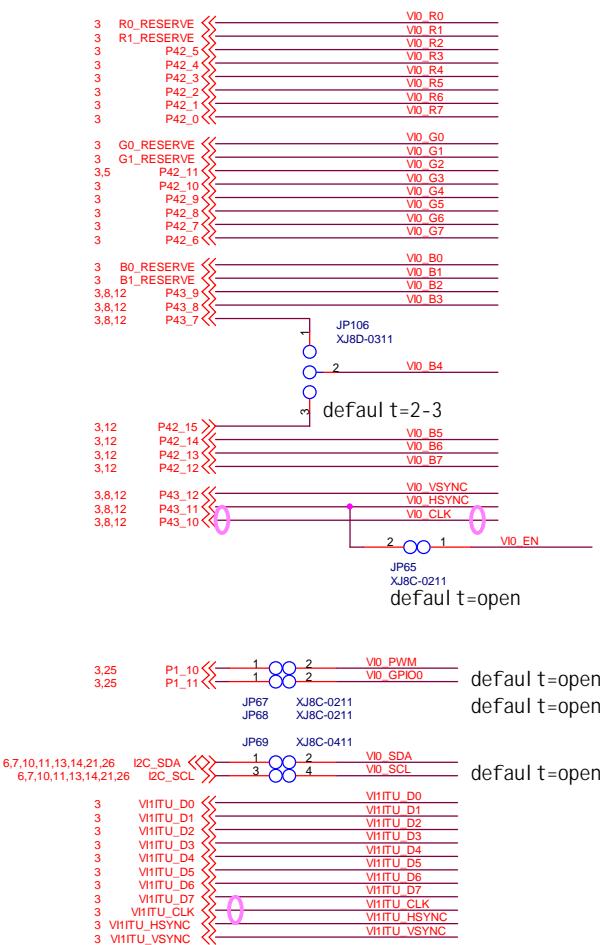


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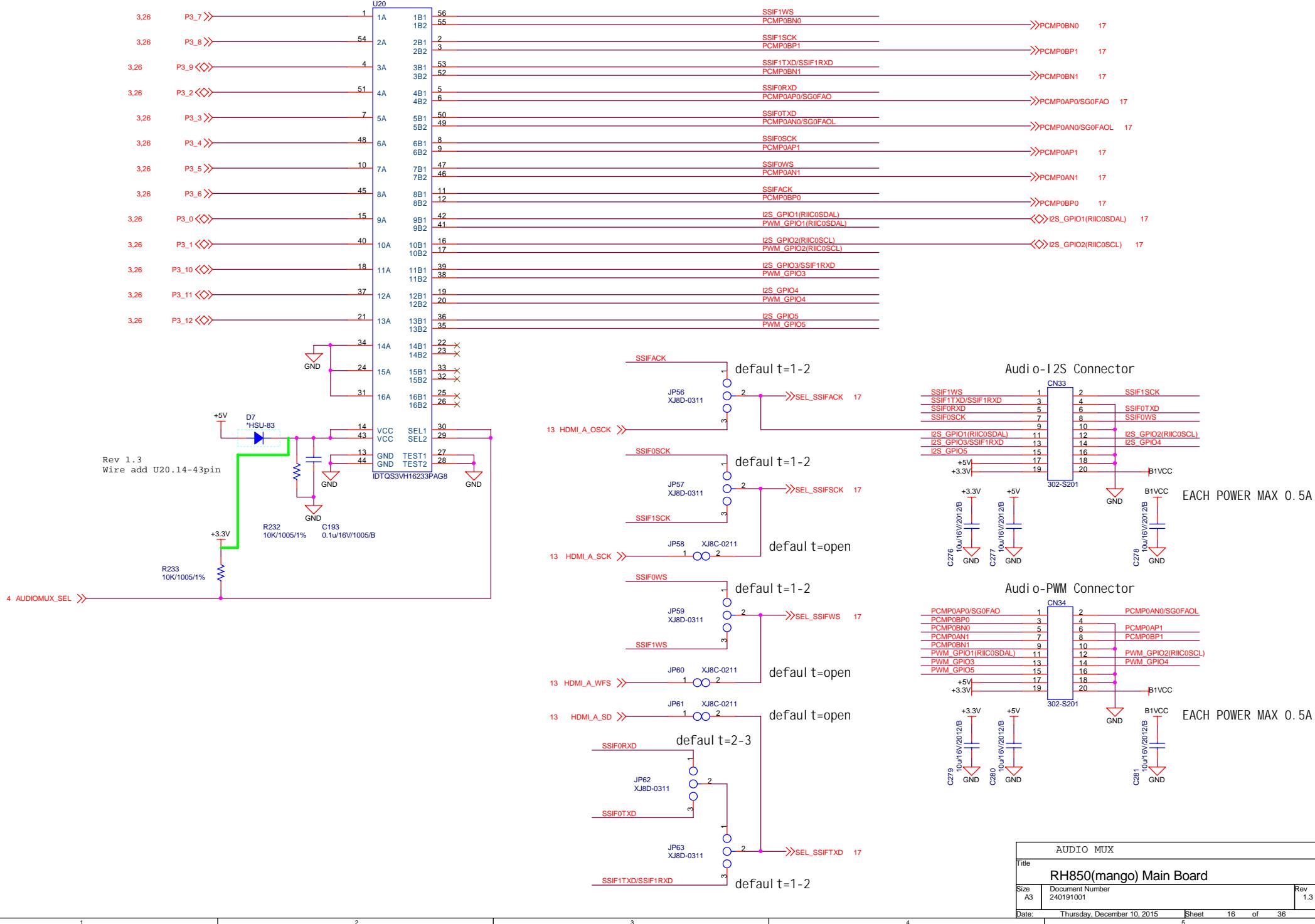


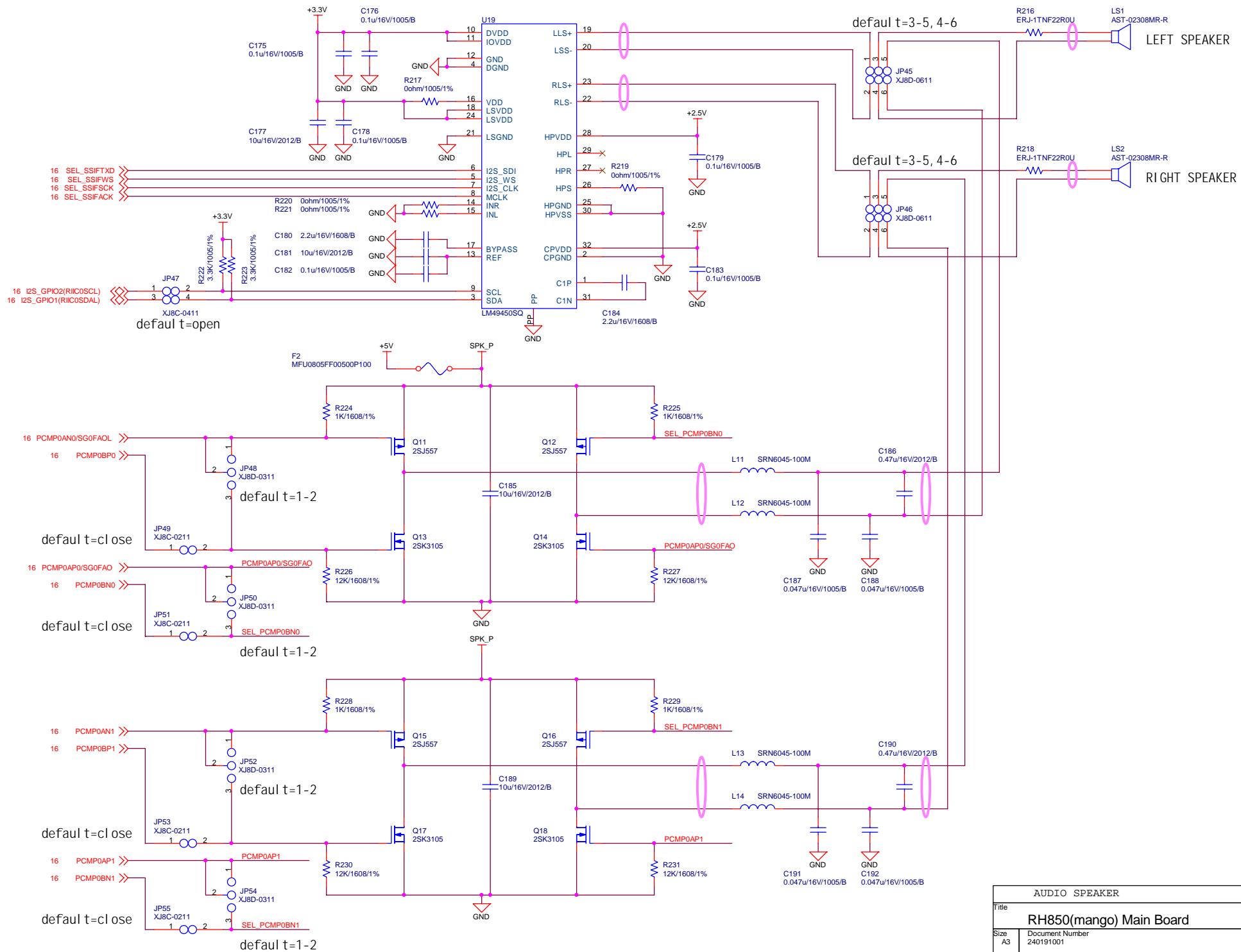
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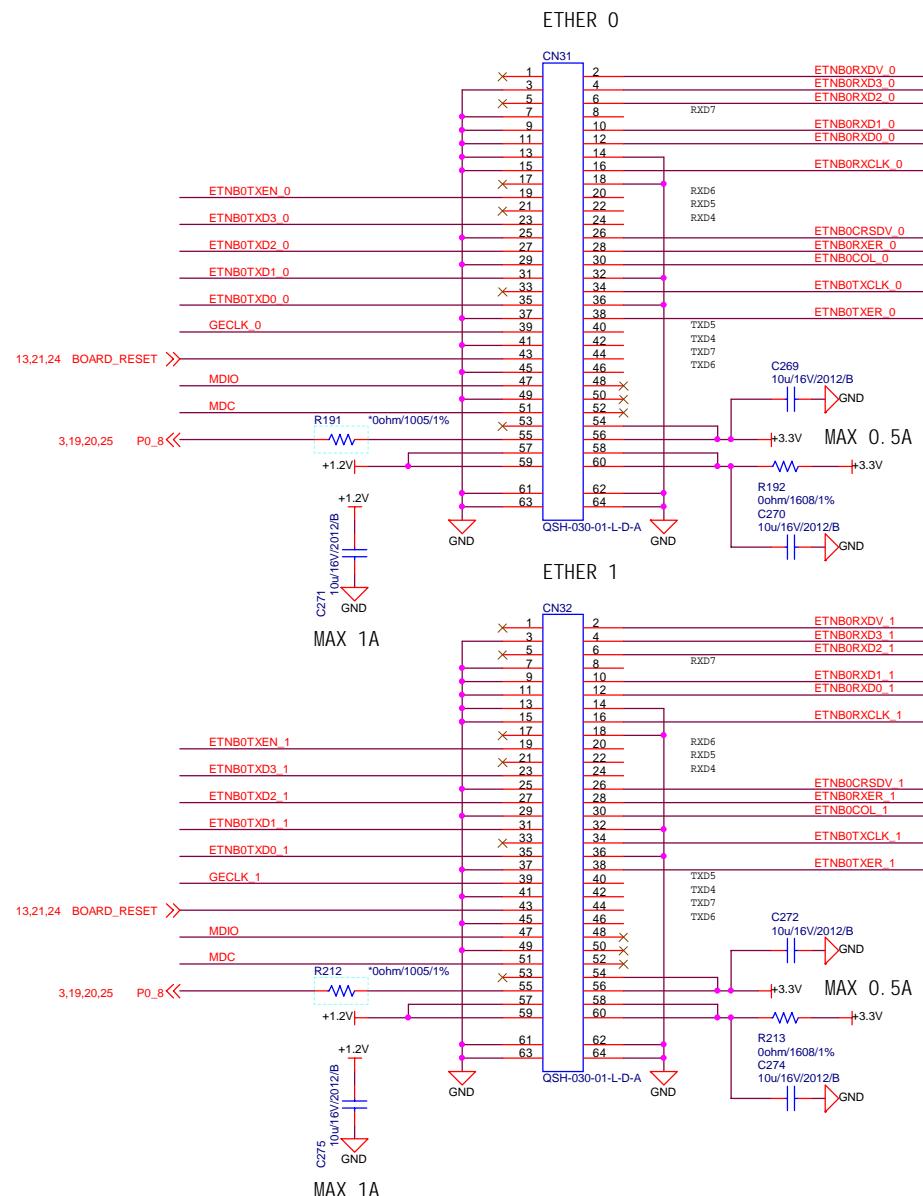
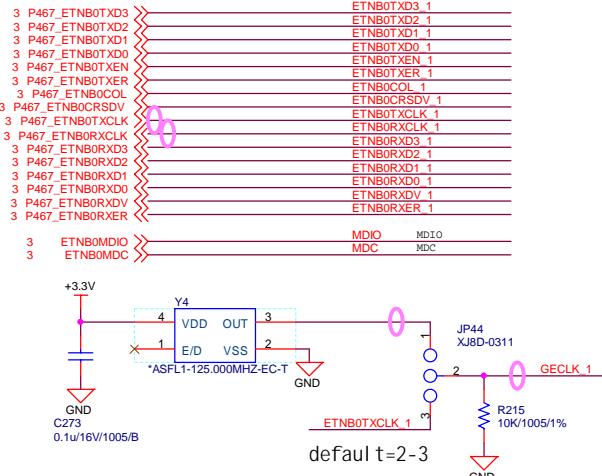
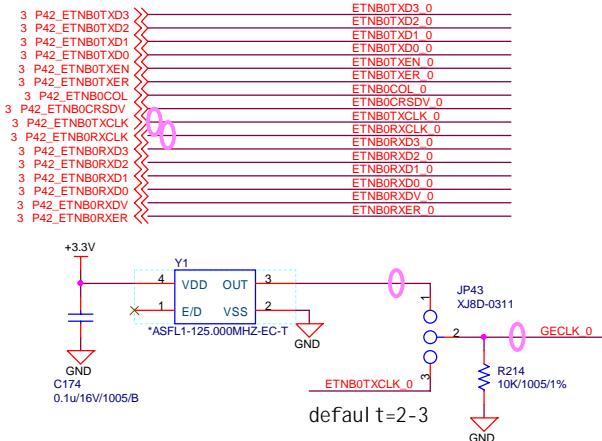


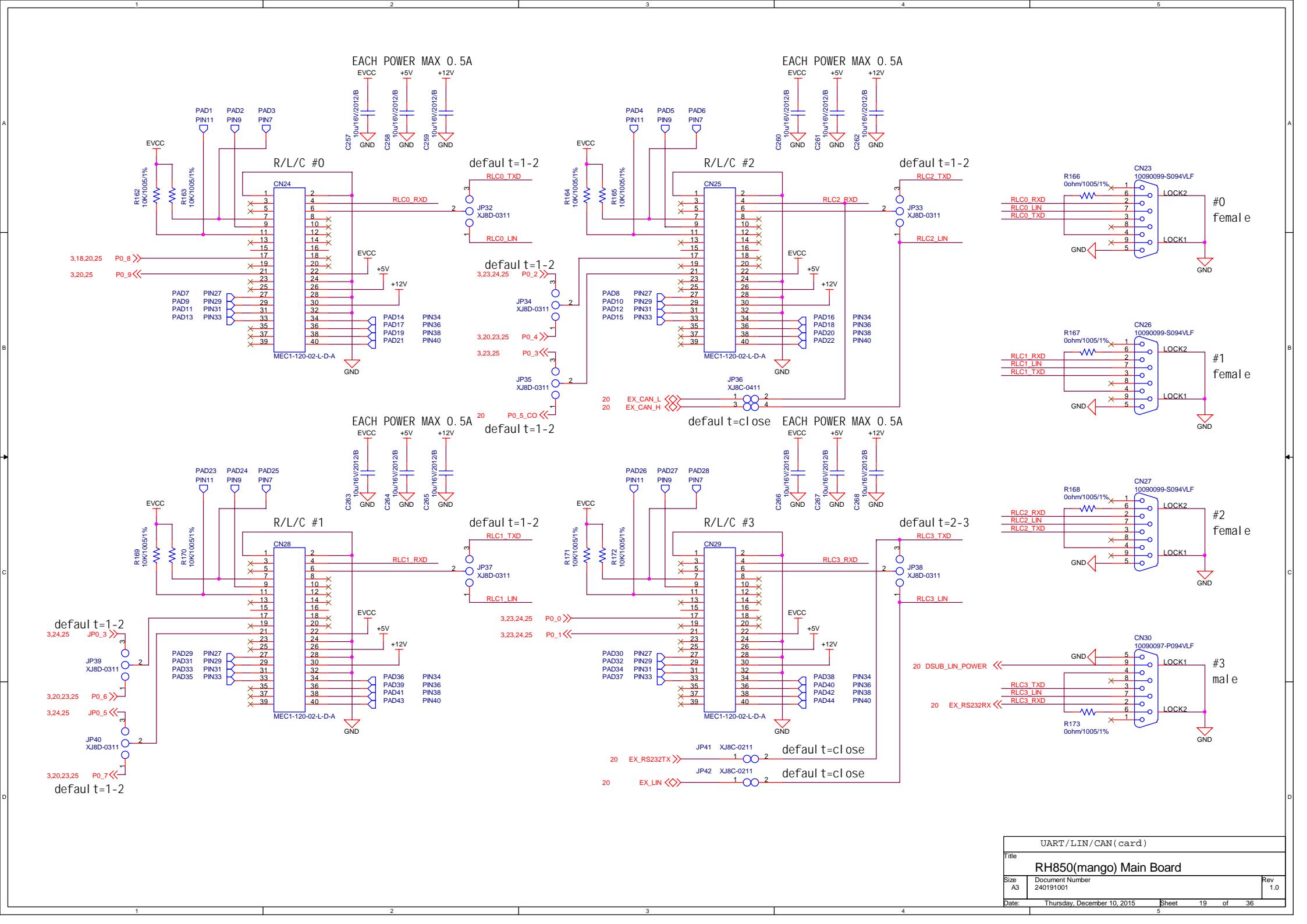
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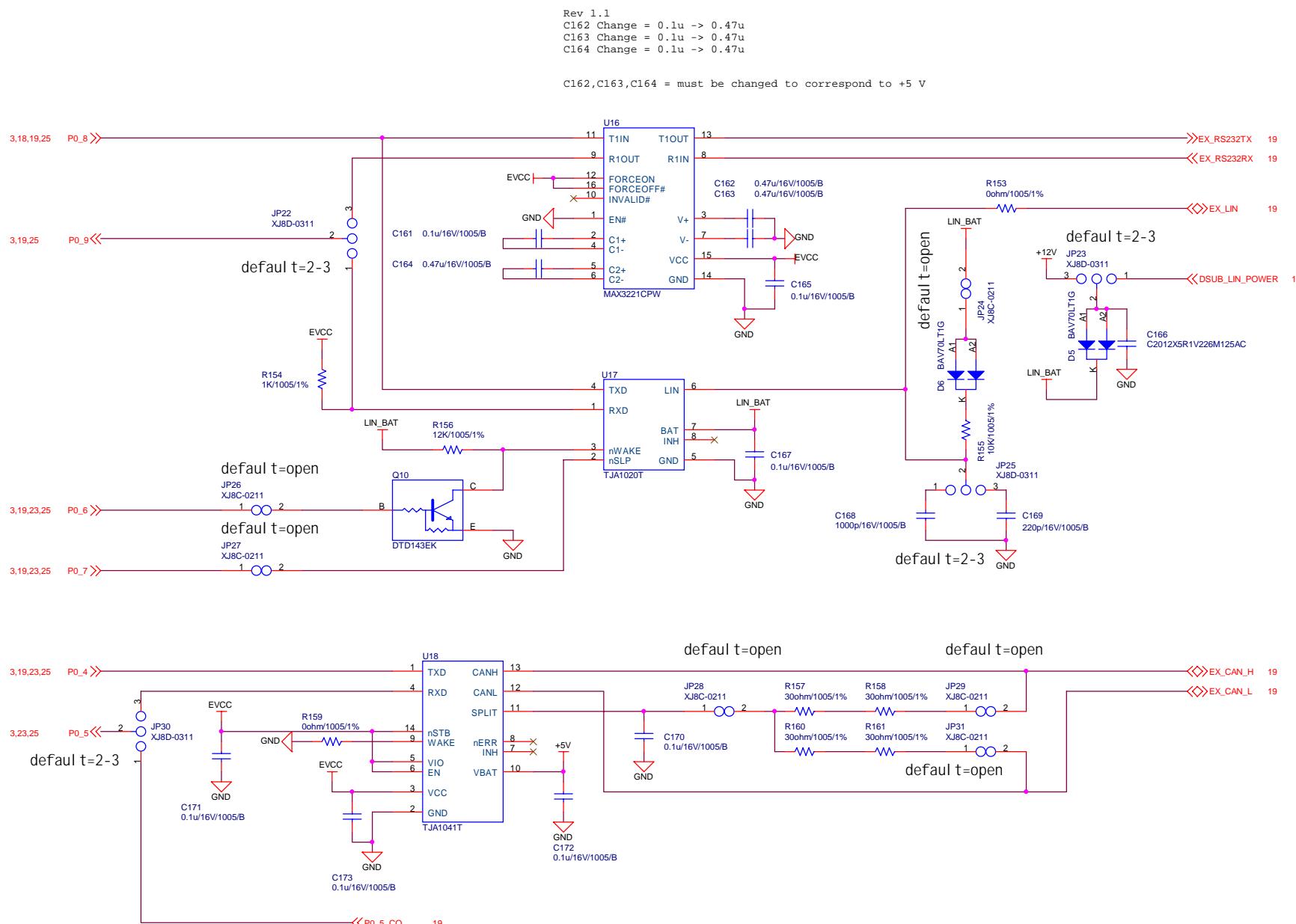




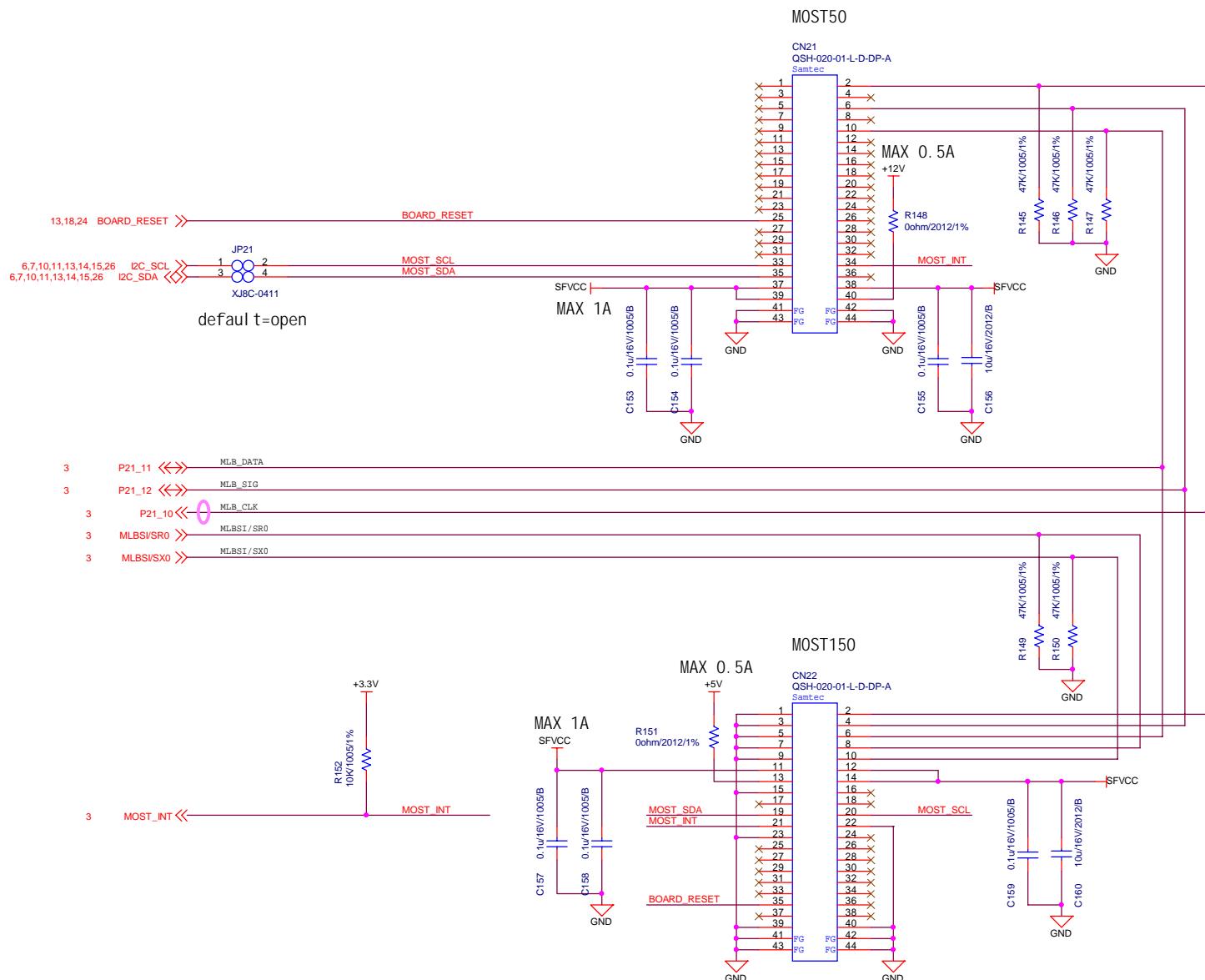
AUDIO SPEAKER			
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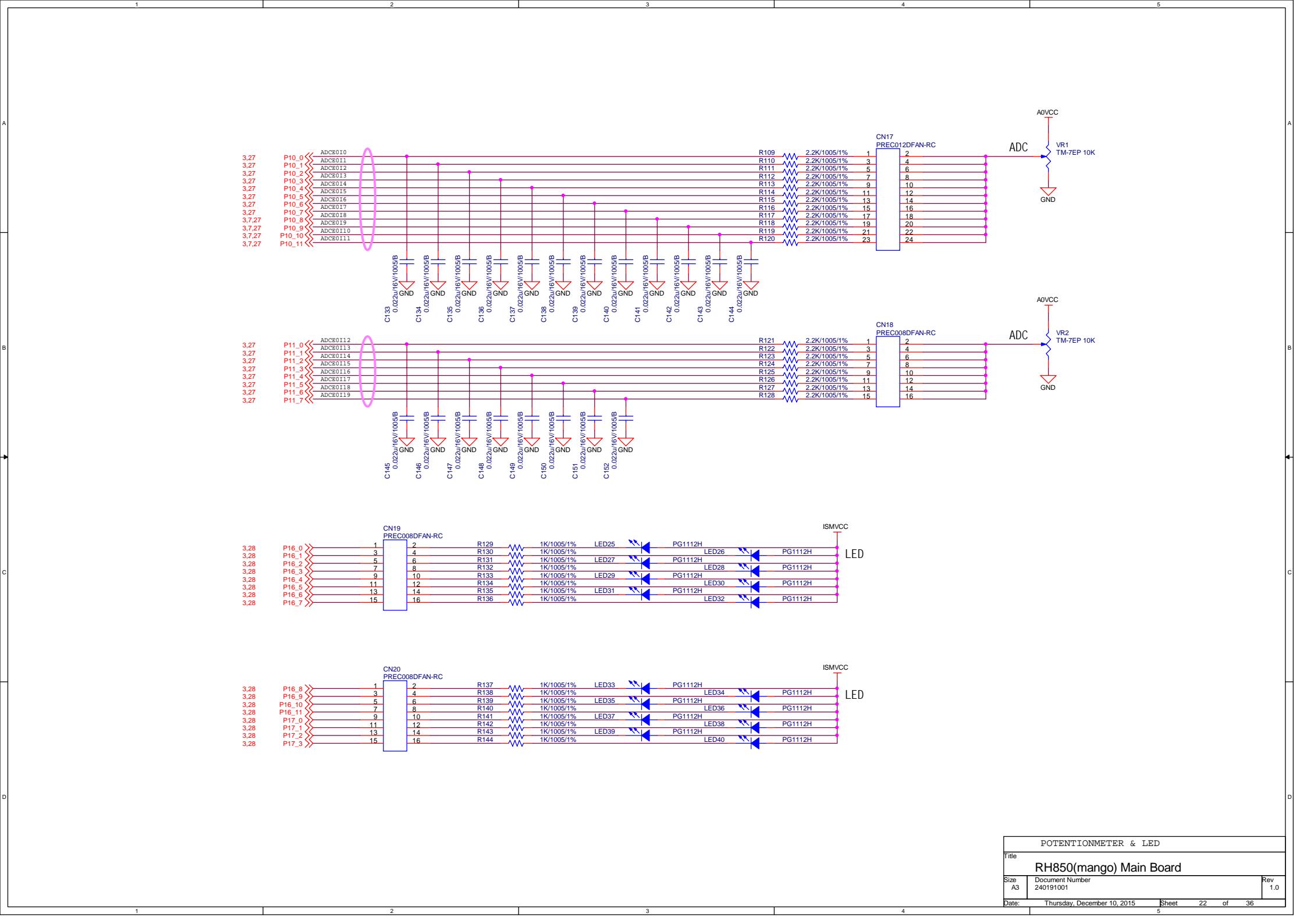


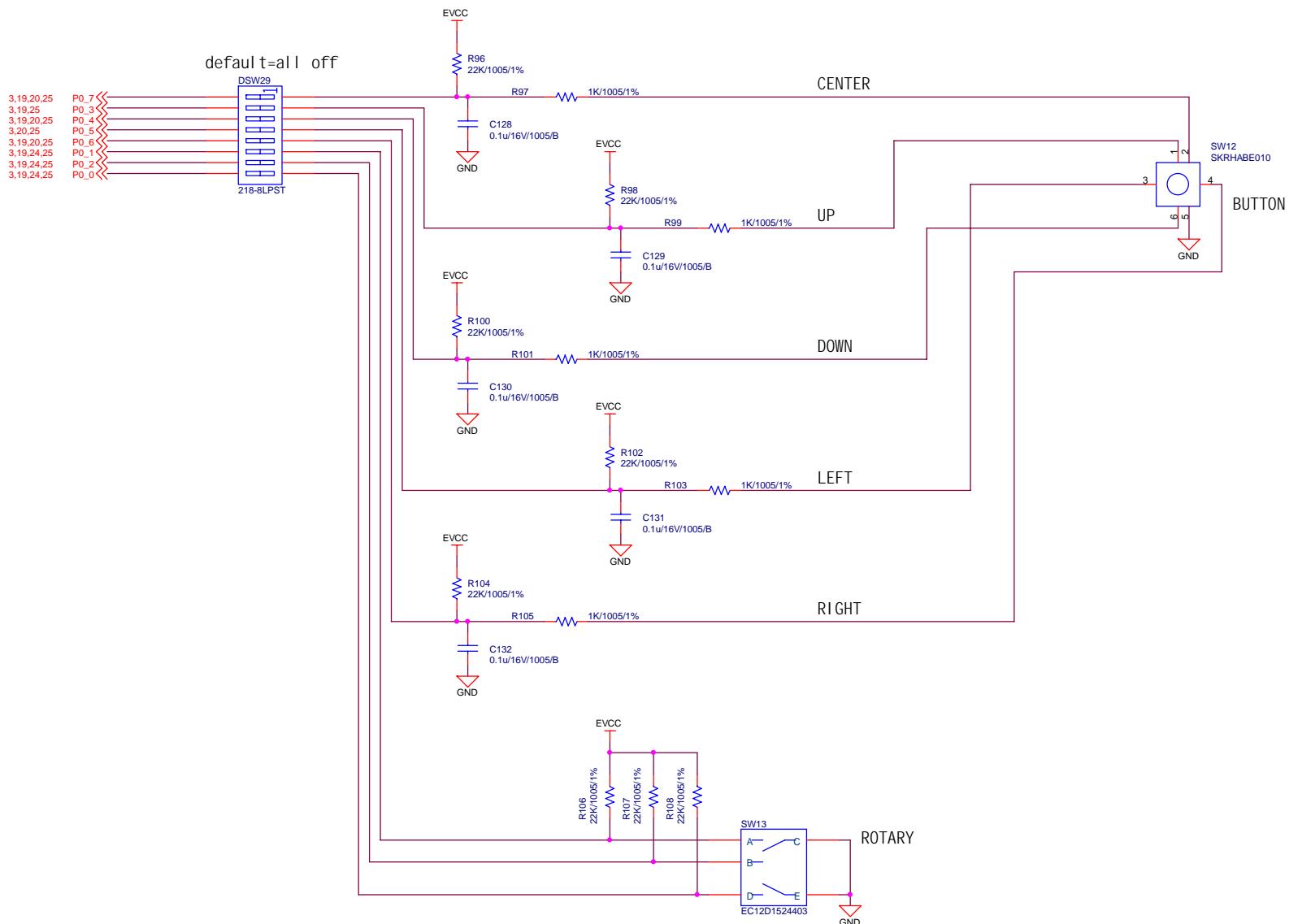


UART/LIN/CAN(onboard)		
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MOST		
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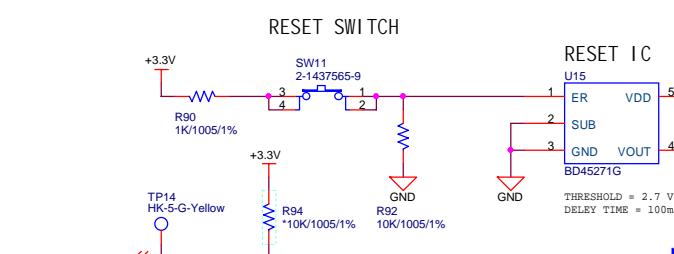
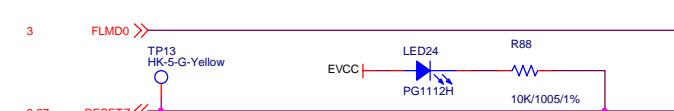
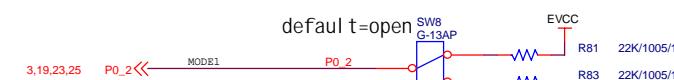
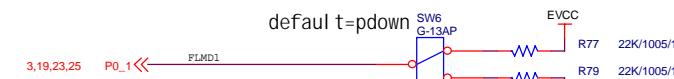
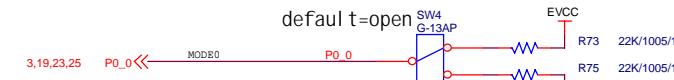


BUTTON & ROTARY		
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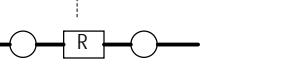
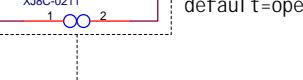
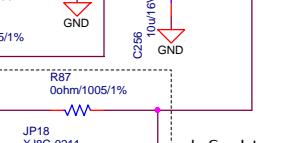
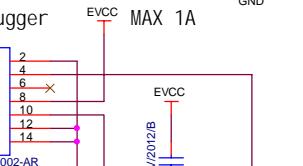
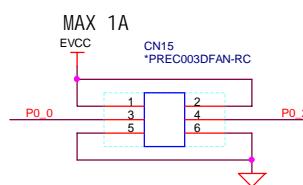
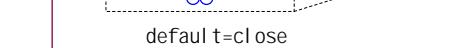
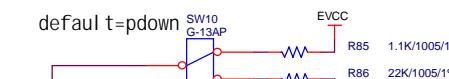
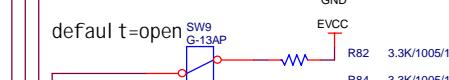
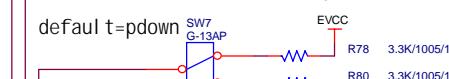
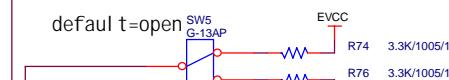
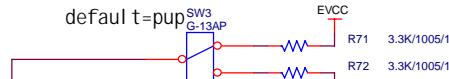
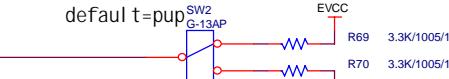
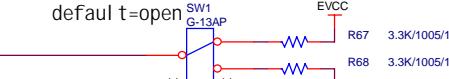
Rev 1.1
R85 Change = 22Kohm -> 1.1Kohm
R88 Change = 1Kohm -> 5.1Kohm
R91 Change = 1Kohm -> NoMount
R94 Change = 10Kohm -> NoMount
R95 Change = 0ohm -> Diode(BAS40LP)

R85 = Because there is a internal pull-down to the CPU
R88,R91 = Because there is a series resistor to the E1
R94,R95 = necessary because there is a wire remodeling

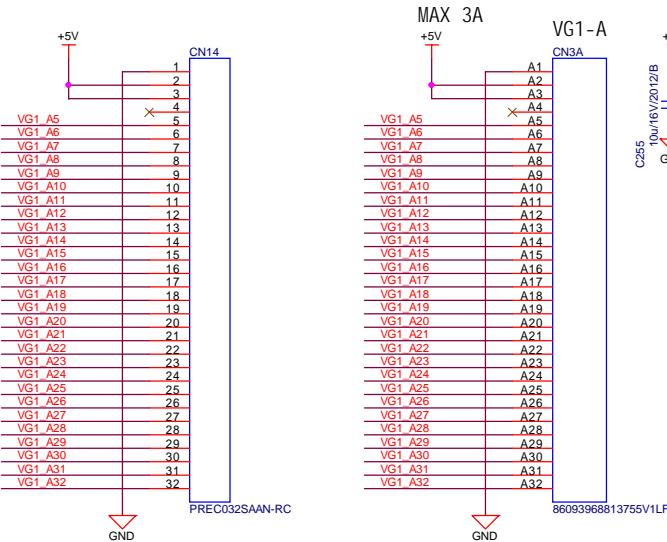
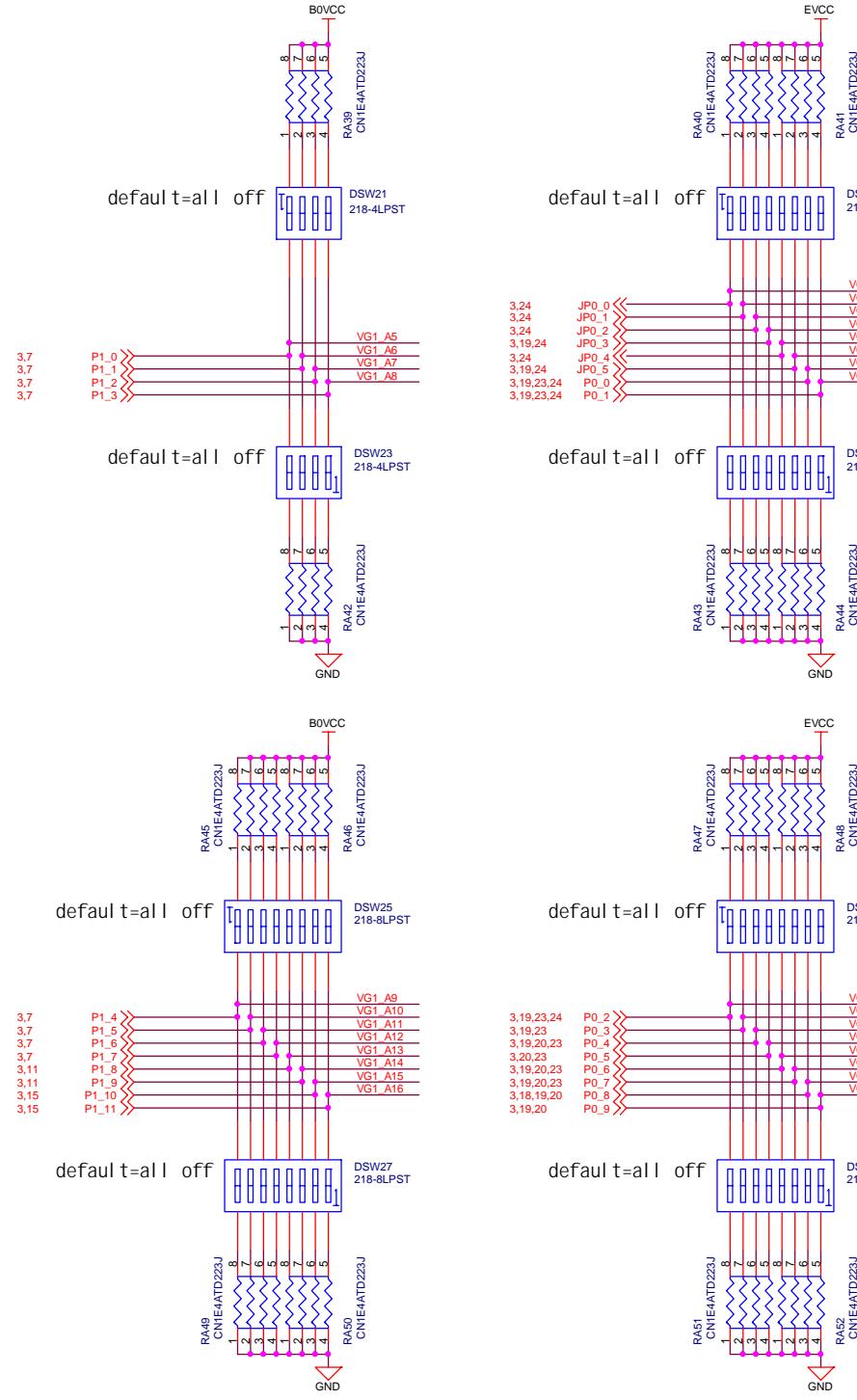
Rev 1.2
R88 Change = 5.1Kohm -> 10Kohm
R91 Change = NoMount -> 10Kohm



Rev 1.1
Wire add CN50.60pin

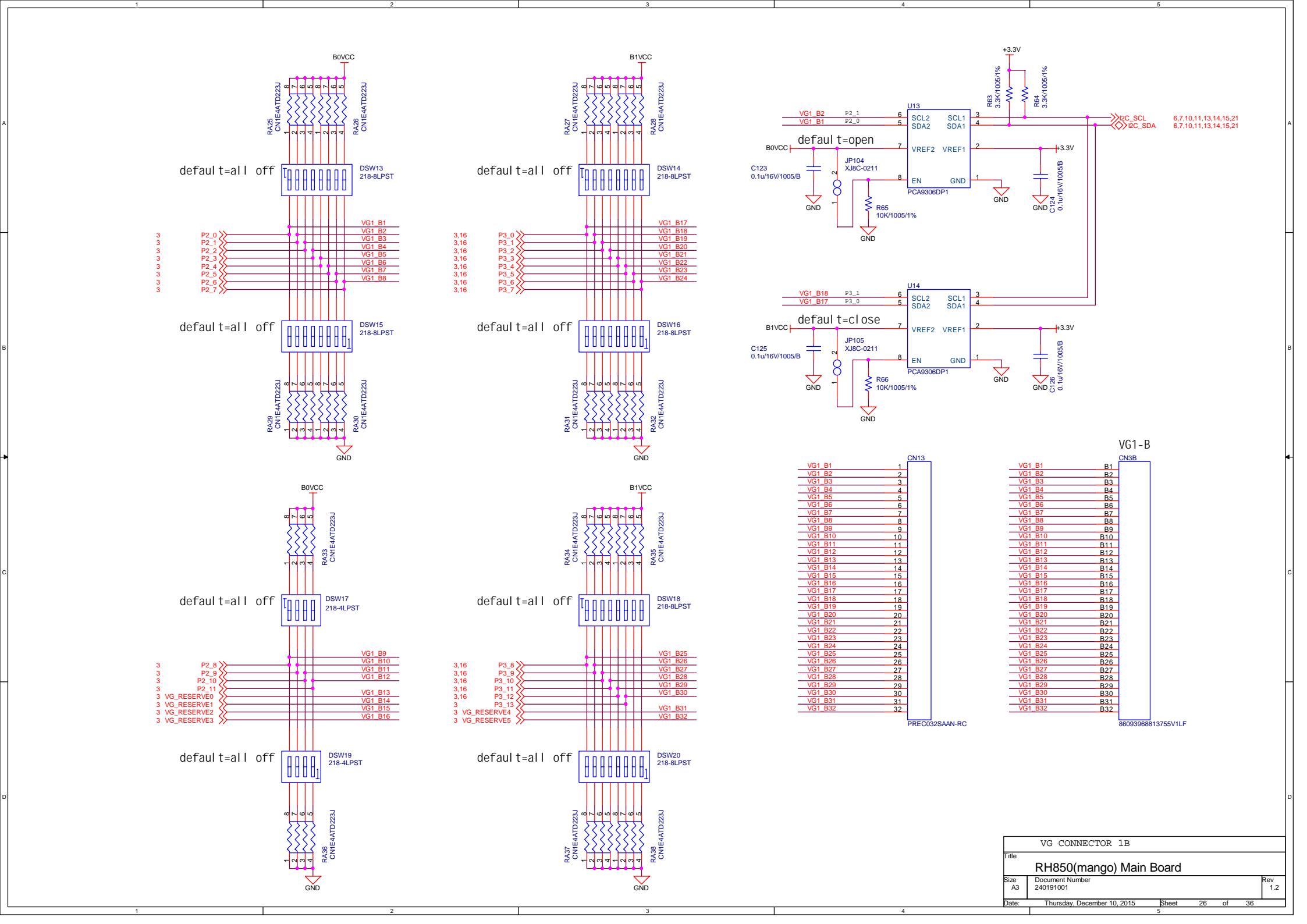


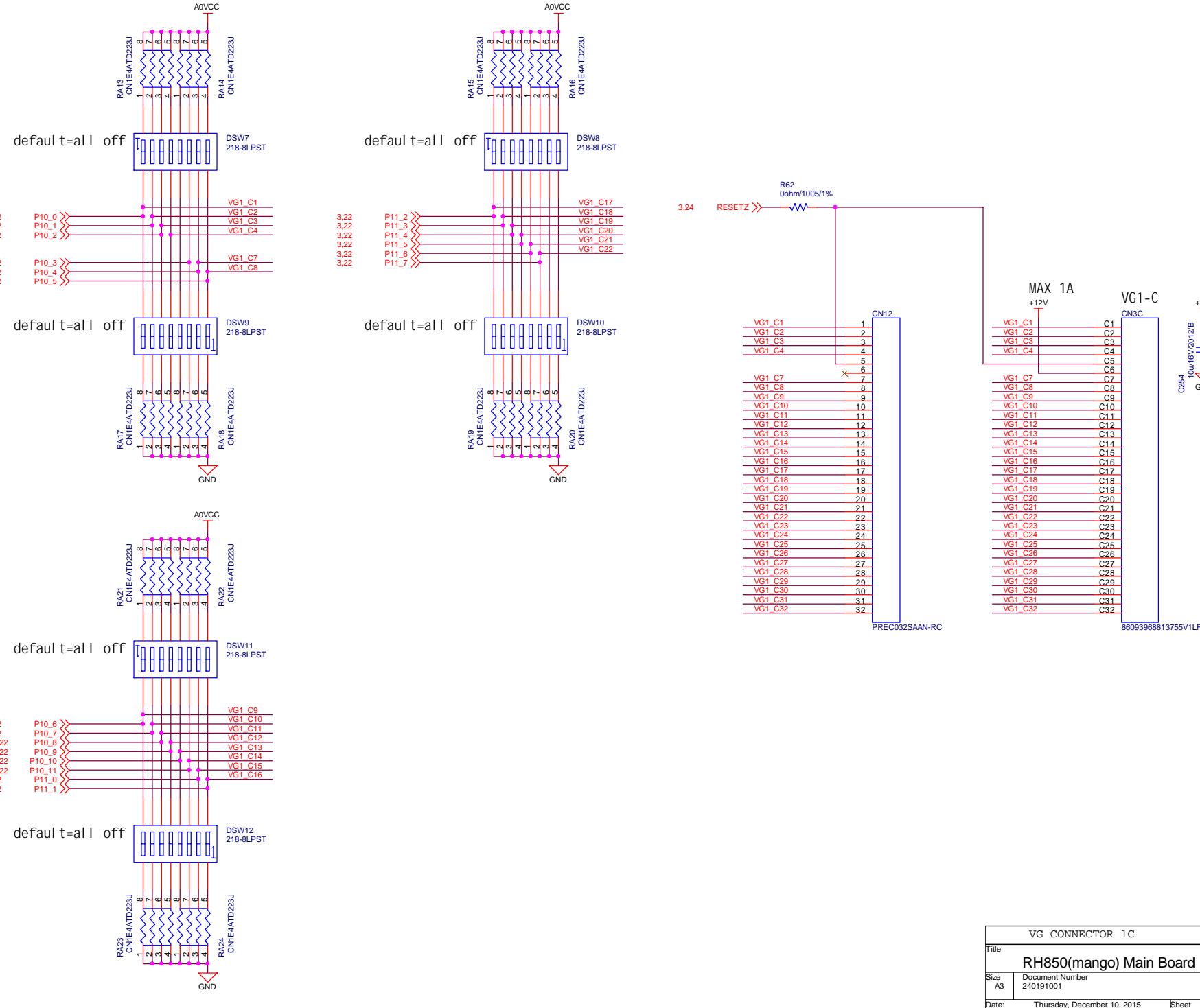
DEBUG		
Title	RH850(mango) Main Board	Rev 1.2
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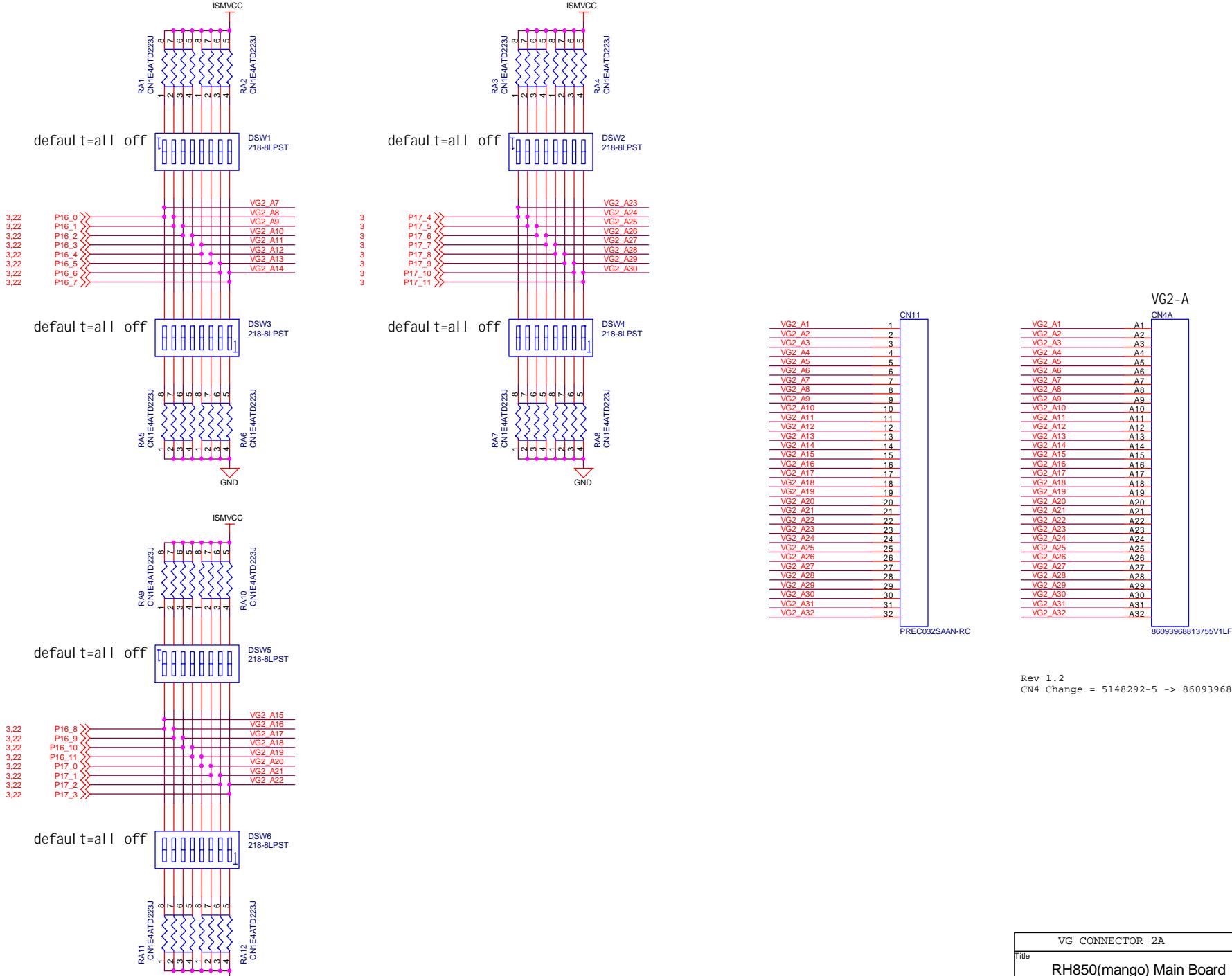


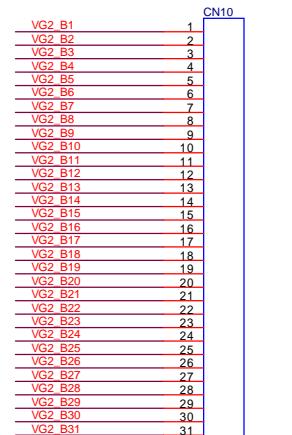
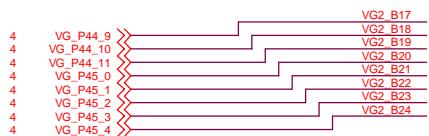
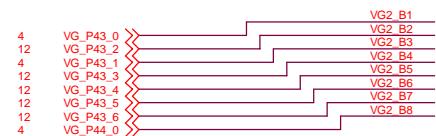
Rev 1.2
CN3 Change = 5148292-5 -> 86093968813755V1LF

VG CONNECTOR 1A	
Title	RH850(mango) Main Board
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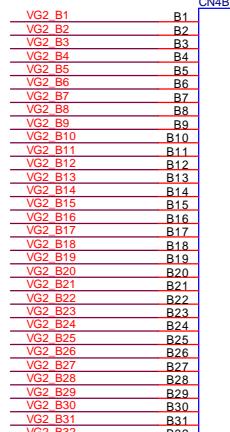




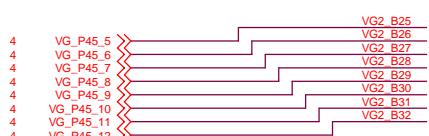
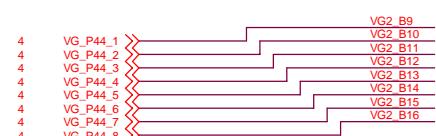




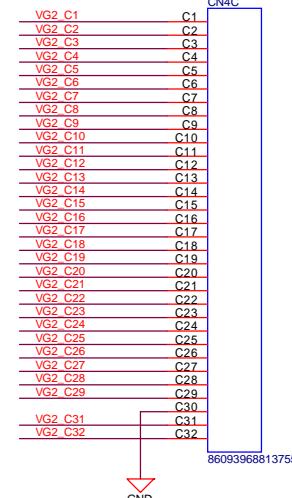
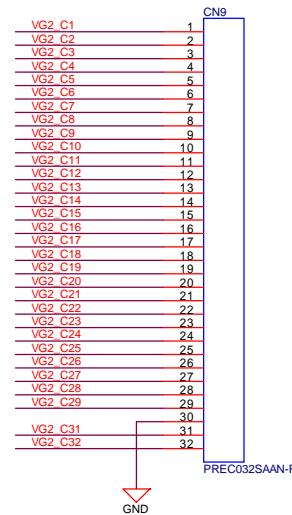
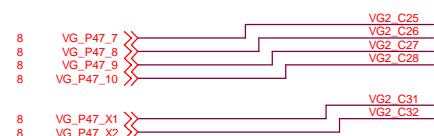
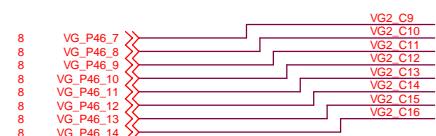
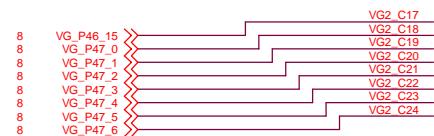
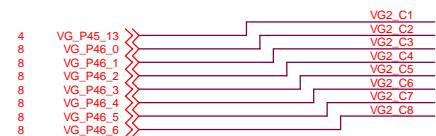
PREC032SAAN-RC



86093968813755V1LF

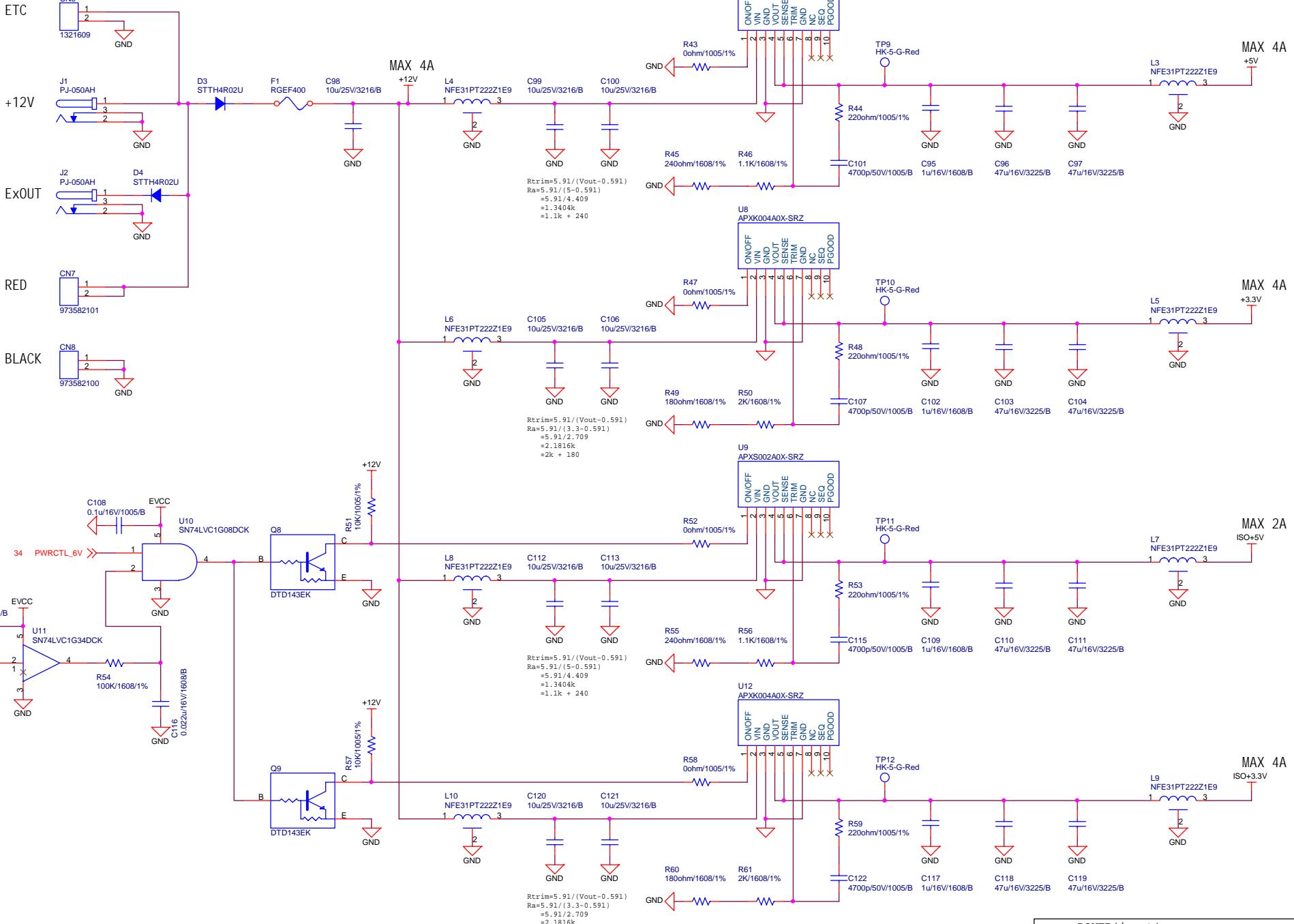


VG CONNECTOR 2B		
Title		Rev 1.2
RH850(mango) Main Board		
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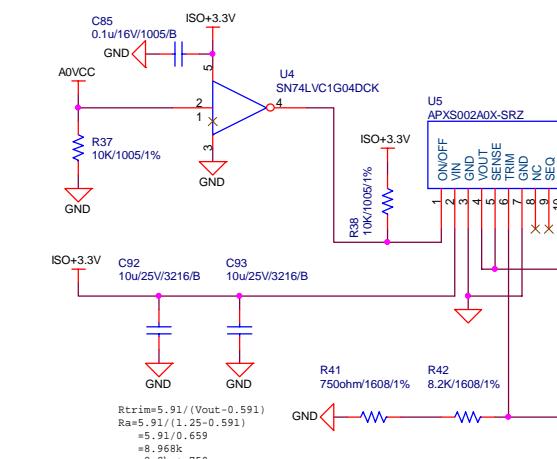
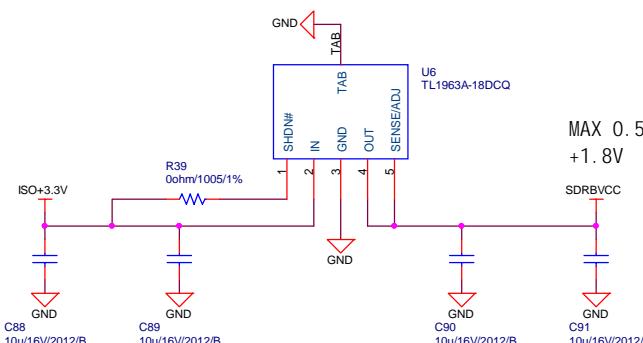
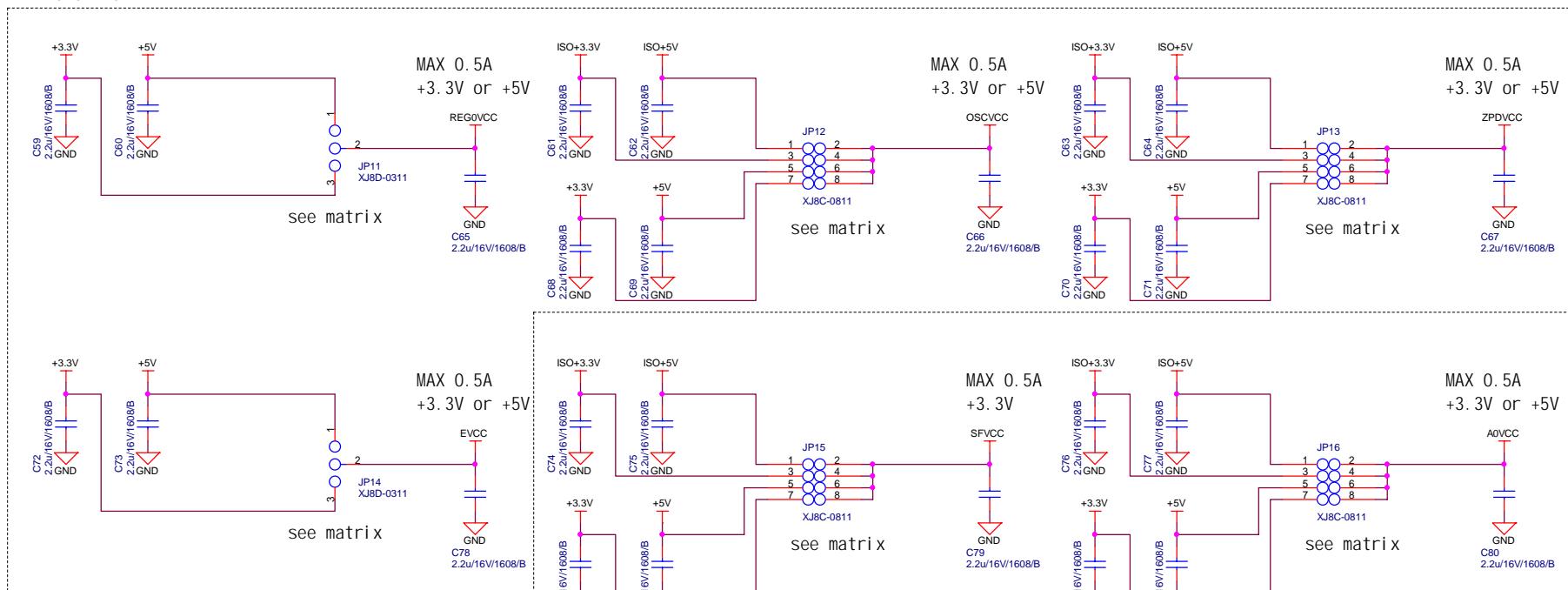
VG CONNECTOR 2C		
Title		
RH850(mango) Main Board		
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EACH CONNECTOR MAX 4A



POWER (input)	
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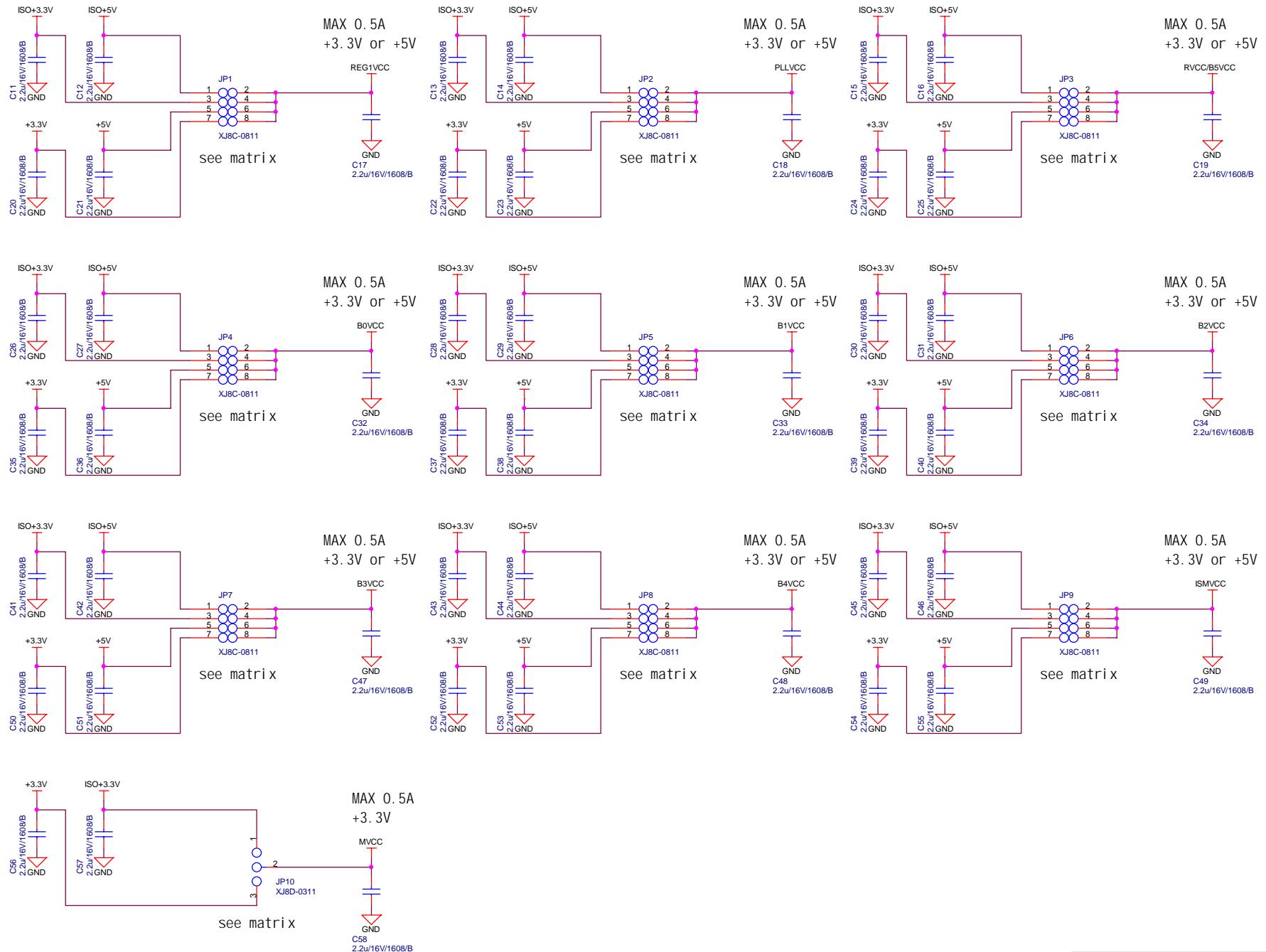
ALWAYS ON POWER



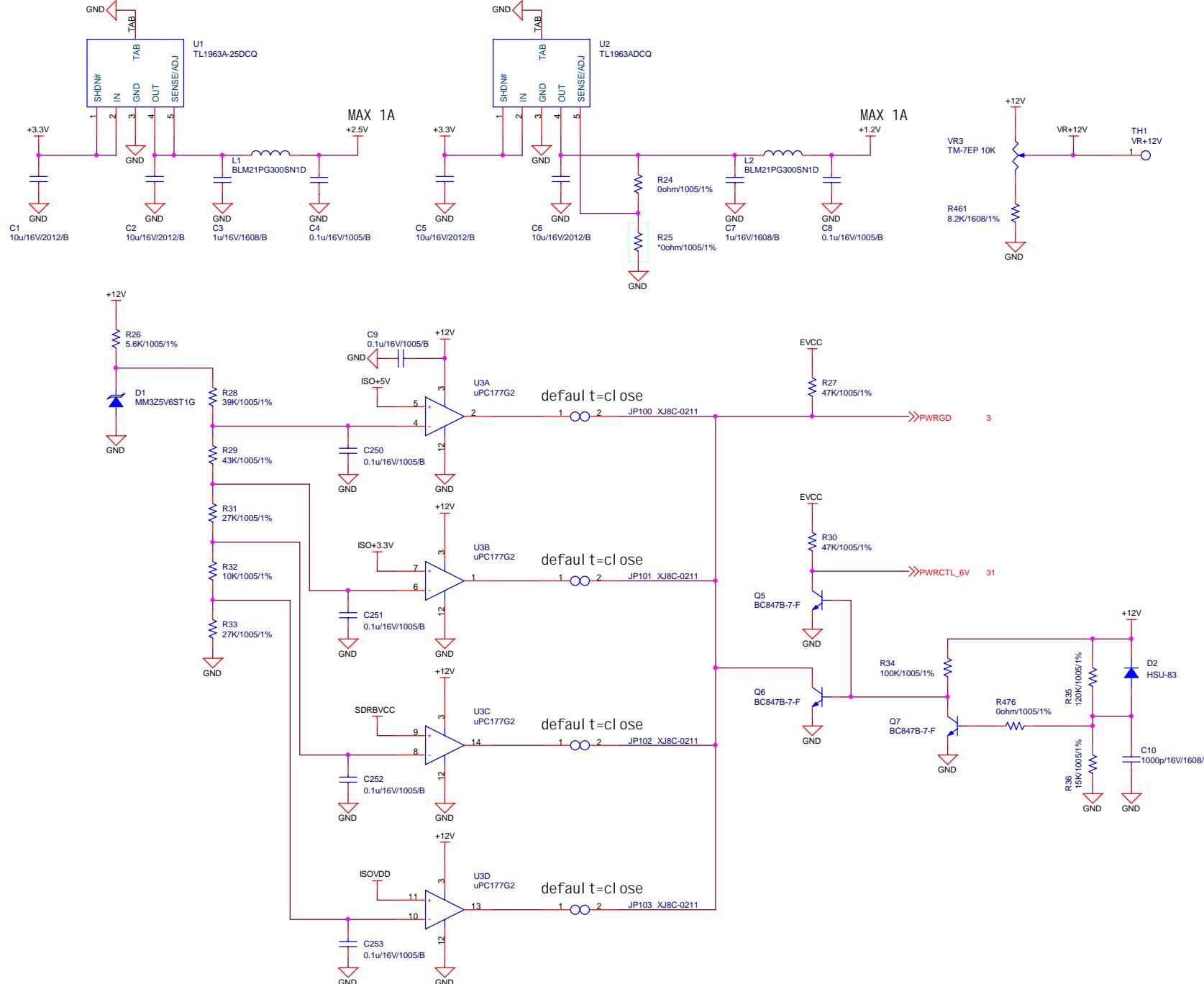
Rev 1.1
U5 Change = APXS004A0X-SRZ -> APXS002A0X-SRZ

U5 = Must be changed to correspond to +3.3 V

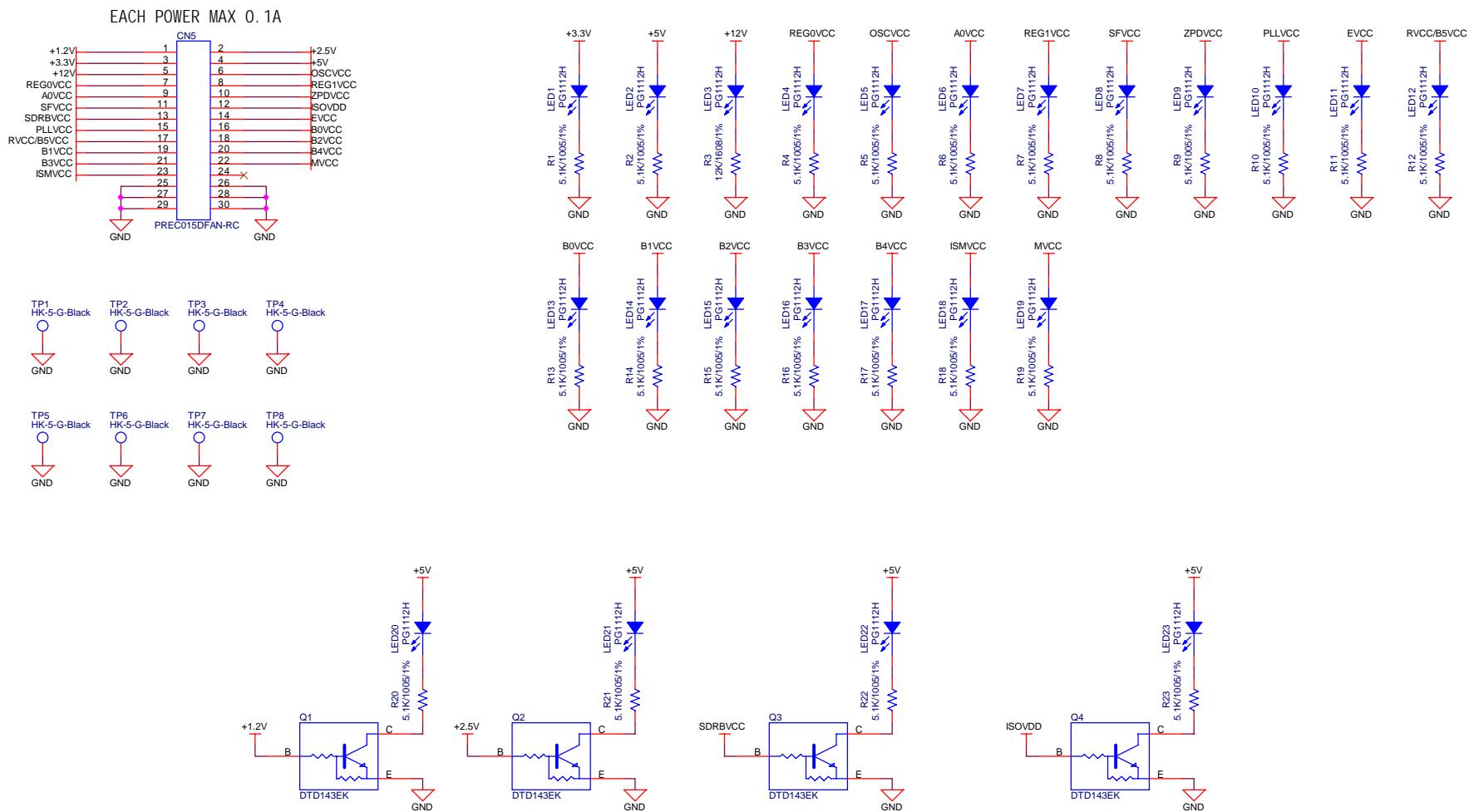
POWER(cpu1)	
Title	
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Rev 1.1	



POWER (cpu2)			
Title			
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POWER (ext)		
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Power Supply Selection Matrix

	D1L1				D1L2(H)				D1M1(H)				D1M2(H)			
	+3.3V	+5V	ISO+3.3V	ISO+5V	+3.3V	+5V	ISO+3.3V	ISO+5V	+3.3V	+5V	ISO+3.3V	ISO+5V	+3.3V	+5V	ISO+3.3V	ISO+5V
REG0VCC	ok	default	unuse		ok	default	unuse		ok	default	unuse		ok	default	unuse	
OSCVCC	ok	ok	ok	default	ok	ok	default	ok	ok	ok	default	ok	ok	ok	default	ok
EVCC	ok	default	unuse		ok	default	unuse		ok	default	unuse		ok	default	unuse	
REG1VCC	ok	ok	ok	default	ok	ok	default	ok	ok	ok	default	ok	ok	ok	default	ok
ISOVDD	unuse				unuse				unuse				+1.25V			
PLLVCC													ok	ok	default	ok
BOVCC	ok	ok	ok	default	ok	ok	default	ok	ok	ok	default	ok	ok	ok	default	ok
B1VCC	ok	ok	ok	default	ok	ok	default	ok	ok	ok	default	ok	ok	ok	default	ok
B2VCC	unuse				unuse				unuse				ok	ok	default	ok
B3VCC									ok	unuse	default	unuse	ok	ok	default	ok
B4VCC					ok	ok	default	ok	ok	ok	default	ok	ok	ok	default	ok
RVCC/B5VCC	ok	ok	ok	default	ok	ok	default	ok	ok	ok	default	ok	ok	unuse	default	unuse
MVCC	unuse				unuse				unuse				ok	unuse	default	unuse
SFVCC	ok	ok	default	ok	ok	unuse	default	unuse	ok	unuse	default	unuse	ok	unuse	default	unuse
SDRBVCC	unuse				unuse				unuse				+1.8V			
ISMVCC	ok	ok	ok	default	ok	ok	default	ok	ok	ok	ok	default	ok	ok	ok	default
ZPDVCC	ok	default	ok	ok	ok	default	ok	ok	ok	default	ok	ok	ok	default	ok	ok
AOVCC	ok	ok	ok	default	ok	ok	default	ok	ok	ok	default	ok	ok	ok	default	ok

PowerNAME	Applied Voltage	PowerNAME	Applied Voltage	PowerNAME	Applied Voltage
REG0VCC	3.3V or 5V	B1VCC	3.3V or 5V	A0VCC	3.3V or 5V
OSCVCC	3.3V or 5V	B2VCC	3.3V or 5V	SDRBVCC	1.8V
REG1VCC	3.3V or 5V	B3VCC	3.3V or 5V		
PLLVCC	3.3V or 5V	B4VCC	3.3V or 5V		
ISOVDD	1.25V	RVCC	3.3V or 5V		
ZPDVCC	3.3V or 5V	MVCC	3.3V		
EVCC	3.3V or 5V	SFVCC	3.3V or 5V		
BOVCC	3.3V or 5V	ISMVCC	3.3V or 5V		

POWER(p_matrix)			
Title		Rev. 1.0	
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RH850(mango) MIPI Board Rev1.3

PAGE	SCHEMATIC PAGE TITLE	Rev
1	TABLE of CONTENTS(This Page)	1.3
2	VIN HDMI	1.3

Revision History

DATE	Rev	Page	DESCRIPTION
2014.03.26	1.0		release version
2014.04.11	1.1		CN1 Model number change
2014.05.20	1.2		R1-8 -> 49.9ohm change Wire add CN2.19pin <--> R13.1pin
2014.08.21	1.3		R1-8 -> NoMount HDP modification (remove R14, connect HPDO to HPDI)

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Note

*All resistors 1% accuracy

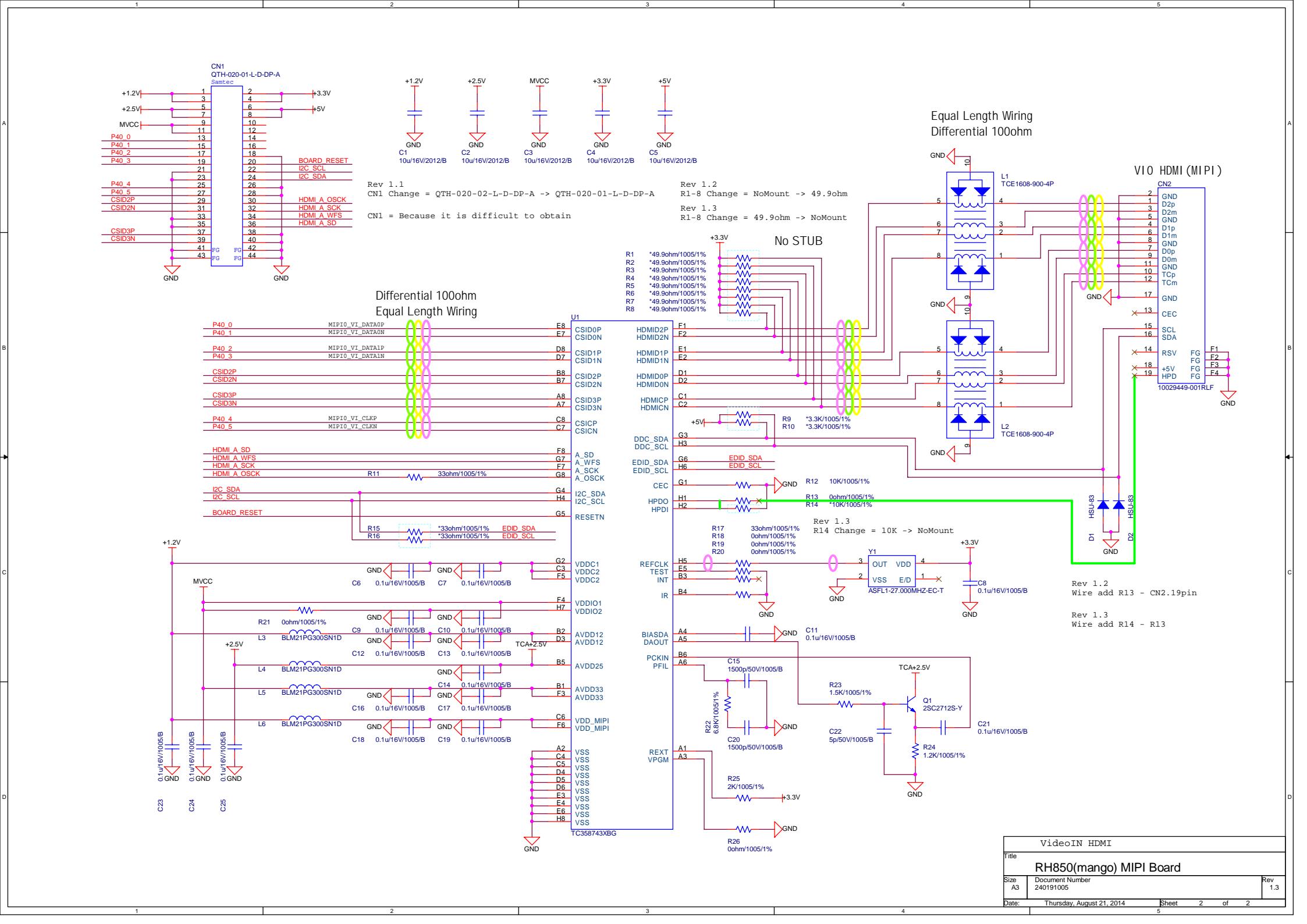
*For more information check the bill of materials

*GND guard  *Equal-length wiring  *Impedance  *No Mount 

NetList Result
64 Parts, 10 Library Parts, 66 Nets, 261 Pins

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12 Revision history

Rev.	Release date	Revised contents	
		Page	Subject
Rev.0.01	2014.April		Draft version created
Rev.0.02	2014-Apr-29		Full review of document. Some open points to be corrected
Rev.0.03	2014-May		Fixed Typos and changed chapters/pages: Front Page, Analog Input, VG Connectors, Schematics
Rev.0.04	2014-May		Fixed typos, Included components list
Rev.0.05	2014-June	59,67,71,72	Changed MVCC default voltage, fixed typos
Rev.0.06	2014-October	37, 60, 64	Fixed typos
Rev.0.07	2015-June	9,13,53,59	Fixed typos, extended list of boards
Rev.0.08	2015-Dec	73	Extended description
Rev.1.00	2016-Dec-23		E1 Debugger description, Schematics Update, Document release

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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