

# RH850/D1x Evaluation Boards

Evaluation Boards for the D1x Dashboard MCU Series

D1M2H Mango Adapter Board (SBEV-RH850-D1M2H),

Please use this manual together with the respective main board manual.

# Preliminary Hardware User's Manual Adapter Board D1M2H

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#### 1 Introduction

The RH850/D1x Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/D1x microcontrollers.

Since the adapter board can not be used as a standalone board, this board has to be mated with a mainboard for full functionality.

Main features of the adapter board:

- Socket for mounting a device
- Power supply from main board
- Device programming capability (Connector on main board)
- Device debugging capability (Connector on main board)
- Pin headers for direct access to each device pin
- MainOSC and SubOSC circuitry
- Connectors to MainBoard
- SDRAM and Serial Flash Memory

This document describes the functionality provided by the adapter board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the RH850/D1x User Manual.

# 2 Board Overview

The figure below depicts the D1M2H Mango Adapter Board. Functional blocks are highlighted.

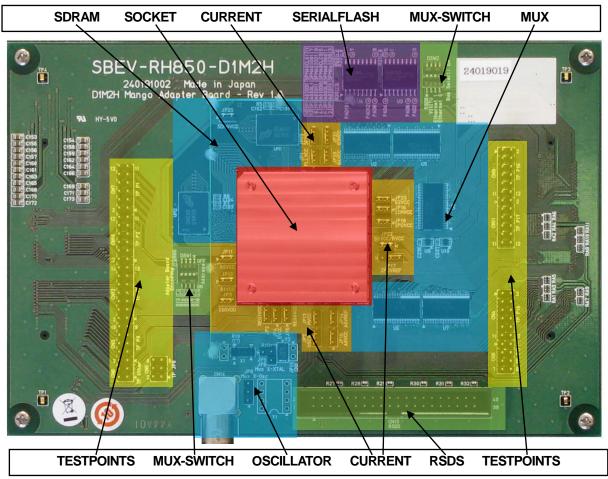


Figure 2-1: Adapter board for RH850/D1M2H

#### 2.1 Mounting devices

The board is designed for reference use with the following device: RH850/D1M2H-484pin

# 3 Power supply

#### 3.1 Power supply structure

#### 3.1.1 Current Measurement Jumpers

Each power supply of the MCU is routed through a single Jumper before connecting it to the MCU. This makes it possible to measure the current consumption of the MCU for each power supply domain in separate.

Table 3-1: Current measuements jumpers (excluding I/O ports supply)

			3 · · · · · · · · · · · · · · · · · · ·
Name of Jumper Supply		Jumper	Function
REG0VCC		JP5	AWO digital circuits via on-chip voltage regulator; nominal 3.3 V and 5 V
OSCVCC		JP7	MainOsc and SubOsc; nominal 3.3 V and 5 V
REG1VCC		JP2	Flash memory, nominal 3.3 V and 5 V $\%$ 1
PLLVCC		JP1	PLL, 3.3 V and 5 V
ISOVDD		JP3	ISO digital circuits, nominal 1.25 V
<b>ZPDVCC</b> JP17		JP17,	Zero point detection circuit; nominal 5 V
ZPDVREF		JP18	Reference voltage of Zero Point detection, normal 5V
A0VREF		JP14	Reference voltage of A/D Converter, normal 3.3V and 5V

※1 D1M1, D1Lx have no ISOVDD, but internal voltage from REG1VCC is also supplied to ISO digital circuit.

Table 3-2: Current measurement jumpres for I/O port supply

Name of	Jumper	Function		
Supply				
EVCC	JP4	Port buffers P0 and JP0; nominal 3.3 V and 5 V		
B0VCC	JP11	Port buffers port group P1, and P2; nominal 3.3 V and 5 V		
B1VCC	JP12	Port buffers port group P3; nominal 3.3 V and 5 V		
B2VCC	JP23	Port buffers ports P43_0 to P43_6, port groups 46, 47; nominal 3.3 V and 5 V		
B3VCC	JP21	Port buffers ports P43_7 to P43_12; nominal 3.3 V and 5 V		
B4VCC	JP20	Port buffers port group P42; nominal 3.3 V and 5 V		
RVCC	C JP22 Port buffers port groups P44, P45 (VO0 RSDS); nominal 3.3 V and 5V.			
MVCC	JP13	Port buffers port group P40 (VI0 MIPI I/F); nominal 3.3 V		
SFVCC	JP19	Port buffers port group P21 (serial flash and MLB); nominal 3.3 V and 5V.		
ISMVCC	JP16	Port buffers port groups P16 and P17 (Stepper Motor Controller/Driver); • nominal 5 V when used for stepper motor operation • nominal 3.3 V and 5 V when not used for stepper motor operation		
A0VCC	JP15	Ports buffers port groups P10 and P11 (A/D Converter analog circuits and input buffers); nominal 3.3 V and 5 V		
SDRBVCC	JP25	DDR2-SDRAM I/F (except SDRBCK, SDRBCKB); nominal 1.8 V		

#### Notes on current measurement:

Currently, the reset line is not pulled-up to full EVCC voltage. This is caused by the drop out voltage of LED24 "RESET ACT" ( $V_{RESET}$  is only ~3.7V when EVCC is 5V). This leads to an EVCC leakage current caused by the RESETZ input buffer. To correctly measure the EVCC current, please add a 6.2k $\Omega$  resistor in parallel to LED24 "RESET ACT" on the Mango Main Board.

#### 3.1.2 Voltage regulators and DC-DC converters

The power domains on the adapter board are supplied by the main board. The following voltages are generated on the main board.

Table 3-3: Main Power supply Source IC output voltage (from Main board)

IC	Input voltage	Voltage	Net name	Spec
U7	12V	5V	+5V	Max 4A
U8	12V	3.3V	+3.3V	Max 4A
U9	12V	5V	ISO+5V	Max 2A
U12	12V	3.3V	ISO+3.3V	Max 4A
U5	U12	1.25V	+1.25V	Max 2A
U6	U12	1.8V	+1.8V	Max 0.5A
U1	U8	2.5V	+2.5V	Max 1A
U2	U8	1.25V	+1.2V	Max 1A

#### 3.1.3 Power Supply Selection Matrix

The voltages that can be selected to power each of the domains of the MCU differ for each device type. For D1M2H the following voltages can be configured for each power domain.

Table 3-4: Main Power supply Source IC output voltage

	D1M2H				
	other	3v3	5v	iso3v3	iso5v
REG0VCC		Х	D		
OSCVCC		X	Х	D	Х
EVCC		X	D		
REG1VCC		Х	Х	D	Х
ISOVDD	1.25V				
PLLVCC		Х	Х	D	Х
B0VCC		X	X	D	Χ
B1VCC		X	X	D	Χ
B2VCC		X	X	D	Χ
B3VCC		X	X	D	Χ
B4VCC		X	X	D	Χ
B5VCC/RVCC		X		D	
MVCC		X		D	
SFVCC		X		D	
SDRBVCC	1.8V				
ISMVCC		Х	Х	Х	D
ZPDVCC		Х	D	Х	Х
A0VCC		Х	Х	D	Χ

X: Possible Setting, D: Default Setting

#### 4 Clock source

#### 4.1 Overview

There are 3 options for main clock input to target MCU.

- · Crystal (8MHz)
- Crystal oscillator (8MHz)
- · Clock input from pulse generator

The default option is to use the soldered crystals for the high speed and the low speed oscillator.

#### 4.2 Oscillator circuit

This figure shows schematic of oscillator block.

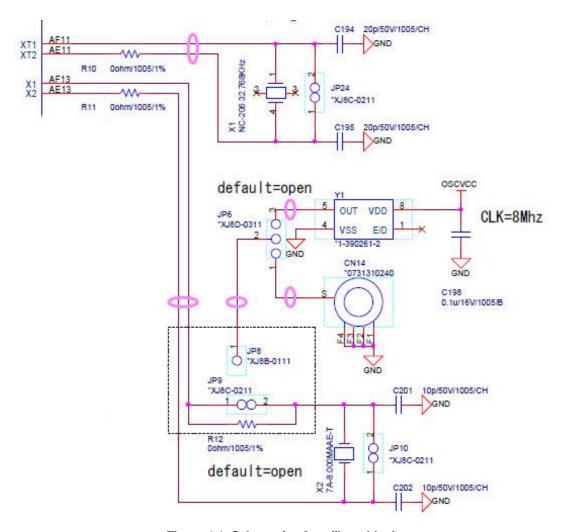


Figure 4-1: Schematic of oscillator block

## 4.3 Function specification

Main oscillator

Terminals: X1/X2 clock selection

- o Crystal (8MHz)
- o Ceralock (8MHz)
- o Direct clock input from external pulse generator

Table 4-1: Sub-Selection of external oscillator

Loc		Function		
JP6	External oscilla	External oscillator sub-selection		
	1-2 select	Use BNC connector (CN14).		
	2-3 select	Use crystal oscillator Y1		

Table 4-2: Selection of crystal or external oscillator

Loc		Function	
JP8/	External oscillator select		
JP9	JP8/JP9 open R12 soldered	Use on-board crystal	
	JP9 1-2 closed R12 unsoldered	Use on-board crystal	
	JP8 JP9-1 closed R12 unsoldered	Use external oscillator (JP6)	

Sub oscillator

Terminals: XT1/XT2

o Crystal (32.768KHz)

# 5 External Memory function

#### 5.1 Serial NOR Flash

2x 512Mbit with total density of 1Gbit (128MB) 2x Flash devices MX25L51245G (Macronix) 8bit, DDR@80MHz Device in SO-16W package

A compatilbe Product is S25FL512S (Spansion).

#### 5.2 DDR2-SDRAM

1 x 16bit or 1x 32bit DDR2-SDRAM of the density 2Gbit Type MT47H128M16 of Micron in BGA package 16/32bit, DDR@240MHz 512MB

#### 5.3 Mounting devices

Table 5-1: Mounted devices

Loc.	Manufacturer	Product name	Note
UM1, UM2	Micron	MT47H128M16RT-25E IT	2Gbit: x4, x8, x16 DDR2 SDRAM
U3, U4	Macronix	MX25L51245G	1Gbit: DDR@80MHz, Serial Flash Memory

# 5.4 Memory connection

Memory block consists of DDR2-SDRAM memory and Serial Flash.

#### DDR2-SDRAM memory

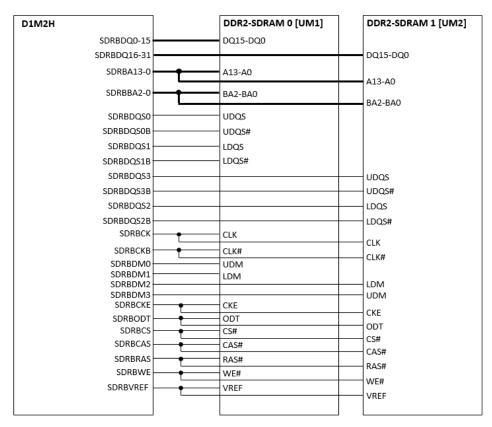


Figure 5-1 DDR2-SDRAM memory block diagram

#### Serial Flash Memory

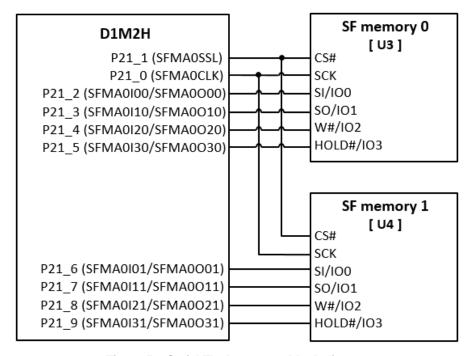


Figure 5-2 Serial Flash memory block diagram

# 6 Multiplex Control

#### 6.1 Overview

Multiplexers (mainly for Video I/O and Ethernet) shall be manually controlled by the user themselves via DIP switches (DSW1 and DSW2). Thus the user has responsibility to avoid misconfiguration of the multiplexers that might destroy the device.

The following multiplexers are placed onto the adapter board. This has been done for all high-speed I/O signals in order to avoid unnecessary routing on the main board and for signals that are directly used on the adapter board. For the RSDS-Interface, the connector is placed onto the adapter board, all other signals will be routed to the main board, independent from the switch position.

Table 6-1: Signal Assignment and function of DSW1

Switch Position	Signal name	ON Function	OFF Function
DSW1.1	Adapter Board Encoding Address (ABEA) 2		
DSW1.2	Adapter Board Encoding Address 1	Connect ABEA to MCU	Disconnect ABEA from MCU
DSW1.3	Adapter Board Encoding Address 0		
DSW1.4	MD_ETHER_SEL	Connect P47_6 and P47_7 Pins to Video / GPIO Blocks	Connect P47_6 and P47_7 Pins to Ethernet Blocks

Table 6-2: Signal Assignment and function of DSW2

Switch Position	Signal name	ON Function	OFF Function
DSW2.1	RSDS_SEL	Connect MCU Pins to Video / GPIO Blocks	Connect MCU Pins to RSDS Connector
DSW2.2	VI1ITU_SEL		Connect MCU Pins to ITU Connector
DSW2.3	P467_ETHER_SEL		Connect MCU Pins to Ethernet 1 Connector
DSW2.4	P42_ETHER_SEL		Connect MCU Pins to Ethernet 0 Connector

The following tables show the signal assignment of the multiplexers with respect to the switch positions.

Table and Table 6-4 are multiplexers that route the MCU signals either to the Main Board or to the Adapter Board according to the switch position.

Table 6-3: Multiplex control table (U6) RSDS\_SEL (DSW2.1)

Table 0-3. Maniplex control table (00) NODO_OLL (DOW2.1)					
Pin	IN	OL	IT		
		RSDS_SEL:OFF	RSDS_SEL:ON		
1A	SEL_P45_0	RSDS_CLKP	P45_0		
2A	SEL_P44_0	RSDS_R0P	P44_0		
3A	SEL_P45_1	RSDS_CLKN	P45_1		
4A	SEL_P44_1	RSDS_R0N	P44_1		
5A	SEL_P45_2	RSDS_G2P	P45_2		
6A	SEL_P44_2	RSDS_R1P	P44_2		
7A	SEL_P45_3	RSDS_G2N	P45_3		
8A	SEL_P44_3	RSDS_R1N	P44_3		
9A	SEL_P45_4	RSDS_G3P	P45_4		
10A	SEL_P44_4	RSDS_R2P	P44_4		
11A	SEL_P45_5	RSDS_G3N	P45_5		
12A	SEL_P44_5	RSDS_R2N	P44_5		
13A	SEL_P45_6	RSDS_B0P	P45_6		
14A					
15A	SEL_P45_7	RSDS_B0N	P45_7		
16A					

Table 6-4: Multiplex control table (U7) RSDS\_SEL (DSW2.1)

Pin	IN	OUT	
		RSDS_SEL:OFF	RSDS_SEL:ON
1A	SEL_P45_8	RSDS_B1P	P45_8
2A	SEL_P44_6	RSDS_R3P	P44_6
3A	SEL_P45_9	RSDS_B1N	P45_9
4A	SEL_P44_7	RSDS_R3N	P44_7
5A	SEL_P45_10	RSDS_B2P	P45_10
6A	SEL_P44_8	RSDS_G0P	P44_8
7A	SEL_P45_11	RSDS_B2N	P45_11
8A	SEL_P44_9	RSDS_G0N	P44_9
9A	SEL_P45_12	RSDS_B3P	P45_12
10A	SEL_P44_10	RSDS_G1P	P44_10
11A	SEL_P45_13	RSDS_B3N	P45_13
12A	SEL_P44_11	RSDS_G1N	P44_11
13A			
14A			
15A			
16A			

For the following interfaces, the function blocks and connectors are on the main board. All multiplexed signals are routed through dedicated lines on the main/adapter board connector.

Table 6-5: Multiplex control table (U9) MD\_ETHER\_SEL (DSW1.4)

Pin	IN	OUT	
		MD_ETHER_SEL:OFF	MD_ETHER_SEL:ON
1A	SEL_P47_6	ETNB0MDIO	P47_6

Table 6-6: Multiplex control table (U10) MD\_ETHER\_SEL (DSW1.4)

	· · · · · · · · · · · · · · · · · · ·		,
Pin	IN	OUT	
		MD_ETHER_SEL:OFF	MD_ETHER_SEL:ON
1A	SEL_P47_7	ETNB0MDC	P47_7

Table 6-7: Multiplex control table (U8) VI1ITU\_SEL (DSW2.2)

Pin	IN	OL	JT
		VI1ITU_SEL:OFF	VI1ITU_SEL:ON
1A	SEL_P43_7	VI1ITU_D2	P43_7
2A	SEL_P43_8	VI1ITU_D1	P43_8
3A	SEL_P43_9	VI1ITU_D0	P43_9
4A	SEL_P43_10	VI1ITU_CLK	P43_10
5A	SEL_P43_11	VI1ITU_HSYNC	P43_11
6A	SEL_P43_12	VI1ITU_VSYNC	P43_12
7A	SEL_P46_0	VI1ITU_D7	P46_0
8A	SEL_P46_1	VI1ITU_D6	P46_1
9A	SEL_P46_2	VI1ITU_D5	P46_2
10A	SEL_P46_3	VI1ITU_D4	P46_3
11A	SEL_P46_4	VI1ITU_D3	P46_4
12A			
13A			
14A			
15A			
16A			

Table 6-8: Multiplex control table (U5) P467\_ETHER\_SEL (DSW2.3)

Pin	IN	IN OUT	
		P467_ETHER_SEL:OFF	P467_ETHER_SEL:ON
1A	SEL_P46_6	P467_ETNB0TXD3	P46_6
2A	SEL_P46_7	P467_ETNB0TXD2	P46_7
3A	SEL_P46_8	P467_ETNB0TXD1	P46_8
4A	SEL_P46_9	P467_ETNB0TXD0	P46_9
5A	SEL_P46_10	P467_ETNB0TXEN	P46_10
6A	SEL_P46_11	P467_ETNB0TXER	P46_11
7A	SEL_P46_12	P467_ETNB0COL	P46_12
8A	SEL_P46_13	P467_ETNB0CRSDV	P46_13
9A	SEL_P46_14	P467_ETNB0TXCLK	P46_14
10A	SEL_P46_15	P467_ETNB0RXCLK	P46_15
11A	SEL_P47_0	P467_ETNB0RXD3	P47_0
12A	SEL_P47_1	P467_ETNB0RXD2	P47_1
13A	SEL_P47_2	P467_ETNB0RXD1	P47_2
14A	SEL_P47_3	P467_ETNB0RXD0	P47_3
15A	SEL_P47_4	P467_ETNB0RXDV	P47_4
16A	SEL_P47_5	P467_ETNB0RXER	P47_5

Table 6-9: Multiplex control table (U2) P42\_ETHER\_SEL (DSW2.4)

Pin	IN	OUT		
		P42_ETHER_SEL:OFF	P42_ETHER_SEL:ON	
1A	SEL_P42_0	P42_ETNB0TXD3	P42_0	
2A	SEL_P42_1	P42_ETNB0TXD2	P42_1	
3A	SEL_P42_2	P42_ETNB0TXD1	P42_2	
4A	SEL_P42_3	P42_ETNB0TXD0	P42_3	
5A	SEL_P42_4	P42_ETNB0TXEN	P42_4	
6A	SEL_P42_5	P42_ETNB0TXER	P42_5	
7A	SEL_P42_6	P42_ETNB0COL	P42_6	
8A	SEL_P42_7	P42_ETNB0CRSDV	P42_7	
9A	SEL_P42_8	P42_ETNB0TXCLK	P42_8	
10A	SEL_P42_9	P42_ETNB0RXCLK	P42_9	
11A	SEL_P42_10	P42_ETNB0RXD3	P42_10	
12A	SEL_P42_11	P42_ETNB0RXD2	P42_11	
13A	SEL_P42_12	P42_ETNB0RXD1	P42_12	
14A	SEL_P42_13	P42_ETNB0RXD0	P42_13	
15A	SEL_P42_14	P42_ETNB0RXDV	P42_14	
16A	SEL P42 15	P42_ETNB0RXER	P42 15	

#### 7 Socket

This chapter lists all connectors of the D1M2H adapter board. There are mainly three groups of connectors.

#### 7.1 Overview

Adapter boards of MCU block cosists of below components.

- IC socket
- Test pin area and external connectors
- Main board connectors

D1x series have several package variant, therefore the IC socket depends upon the package variant.

#### 7.2 RH850/D1M2H adapter board structure

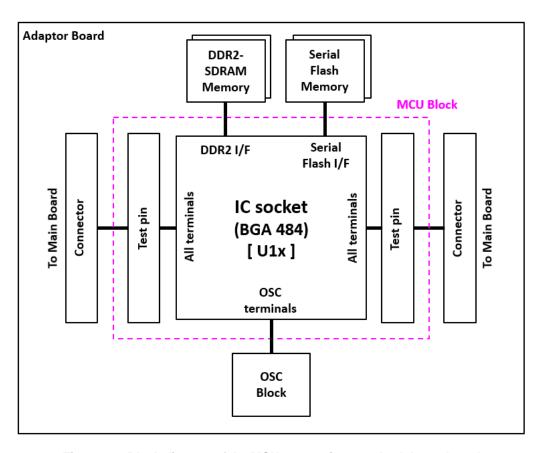


Figure 7-1: Block diagram of the MCU connections on the Adapter board

## 7.3 Mounting socket

This board will be fitted with one of the socket types as shown below.

Table 7-1: IC socket Option 1 (For the BGA484 Adaptor Board)

	• •	• •
Manufacturer	Product name	Note
TOKYO ELETECH CORP.	BSSOCKET484Z2627RE21N	BGA to Pin adapter. To be soldered. BSSOCKET connects to CSSOCKET or LSPACK
TOKYO ELETECH CORP.	LSPACK484Z2627RE01	Can be plugged into the BGA to Pin adapter. Device will be inserted into the LSPACK

Table 7-2: IC socket Option 2 (For the BGA484 Adaptor Board)

	,	
Manufacturer	Product name	Note
IRONWOOD ELECTRONICS	C9803	BGA to Pin adapter. To be soldered. This is the board mounted socket
E-TEC	BPW484-1070-26AA55A	Can be plugged into the BGA to Pin adapter. Device will be inserted into this socket.

## 7.4 Connection with the In-Circuit Emulator (ICE)

When using the "IC socket Option 1", it is possible to connect the ICE to the BSSOCKET.

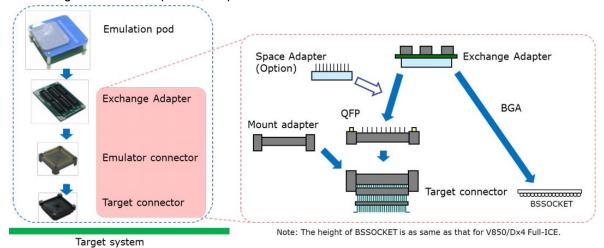


Figure 7-2: Connection with ICE

# 8 Connectors of the D1M2H adapter board

Connection to each pin of the device is possible via the connectors CN1 to CN12 and CN15.

## 8.1 Main Board to Adapter Board connectors

Signal names that are highlighted in dark grey, are not used by the D1M2H adapter board.

Table 8-1: Pin assignment of connector (CN1)

Table 8-1: Pin assignment of connector (CN1)			
Pin	Function / Port	Pin	Function / Port
1	+3.3V	2	VR+12V
3	+3.3V	4	VR+12V
5	+5V	6	+12V
7	+5V	8	+12V
9		10	
11	ZPDVCC	12	OSCVCC
13	ZPDVCC	14	OSCVCC
15	EVCC	16	REG0VCC
17	EVCC	18	REG0VCC
19	2,00	20	NEGOVOO
21	REG1VCC	22	ISOVDD
23	REG1VCC	24	ISOVDD
25	AOVCC	26	PLLVCC
27	AOVCC	28	PLLVCC
29	ISMVCC	30	MVCC
31	ISMVCC	32	MVCC
33	SFVCC	34	SDRBVCC
			SDRBVCC
35	SFVCC	36	SURBVCC
37	D0) (00	38	D41/00
39	B0VCC	40	B1VCC
41	B0VCC	42	B1VCC
43	B2VCC	44	B3VCC
45	B2VCC	46	B3VCC
47	B4VCC	48	RVCC/B5VCC
49	B4VCC	50	RVCC/B5VCC
51		52	_
53	MLBSI/SR0	54	P21_10
55	MLBSI/SX0	56	P21_11
57	MOST_INT	58	P21_12
59		60	SF_RESET
61	VI1ITU_D0	62	VG_RESERVE0
63	VI1ITU_D1	64	VG_RESERVE1
65	VI1ITU_D2	66	VG_RESERVE2
67	VI1ITU_D3	68	VG_RESERVE3
69	VI1ITU_D4	70	VG_RESERVE4
71	VI1ITU_D5	72	VG_RESERVE5
73	VI1ITU_D6	74	
75	VI1ITU_D7	76	GND
77	VI1ITU_CLK	78	GND
79	VI1ITU_HSYNC	80	GND
81	VI1ITU_VSYNC	82	GND
83		84	
85	GND	86	P2_11
87	GND	88	P2_10
89	GND	90	P2_9
91	GND	92	P2_8
93		94	P2_7
95	P1_11	96	P2_6
97	P1_10	98	P2_5
99	P1 9	100	P2 4

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Pin	Function / Port	Pin	Function / Port
101	P1_8	102	P2_3
103	P1_7	104	P2_2
105	P1_6	106	P2_1
107	P1_5	108	P2_0
109	P1_4	110	
111	P1_3	112	P0_9
113	P1_2	114	P0_8
115	P1_1	116	P0_7
117	P1_0	118	P0_6
119		120	P0_5
121	P3_13	122	P0_4
123	P3_12	124	P0_3
125	P3_11	126	P0_2
127	P3_10	128	P0_1
129	P3_9	130	P0_0
131	P3_8	132	
133	P3_7	134	PWRGD
135	P3_6	136	PWRCTL
137	P3_5	138	RESETZ
139	P3_4	140	FLMD0
141	P3_3	142	
143	P3_2	144	P40_0
145	P3_1	146	P40_1
147	P3_0	148	P40_2
149		150	P40_3
151	JP0_5	152	P40_4
153	JP0_4	154	P40_5
155	JP0_3	156	CSID2P
157	JP0_2	158	CSID2N
159	JP0_1	160	CSID3P
161	JP0_0	162	CSID3N
163		164	
165	GND	166	GND
167	GND	168	GND
169	GND	170	GND
171	GND	172	GND
173	GND	174	GND
175	GND	176	GND
177	GND	178	GND
179	GND	180	GND
181	GND	182	GND
183	GND		

Table 8-2: Pin assignment of connector (CN2)

	able 8-2: Pin assignme	nt of c	onnector (CN2)
Pin	Function / Port	Pin	Function / Port
1	P47_X2	2	
3	P47_X1	4	R0 RESERVE
5	P47_10	6	R1 RESERVE
7	P47 9	8	G0_RESERVE
9	P47 8	10	G1_RESERVE
11	P47_7	12	B0 RESERVE
13	P47_6	14	B1 RESERVE
15	P47_0	16	DI_INLOLINVL
17	P47_5		D40 45
		18	P42_15
19	P47_3	20	P42_14
21	P47_2	22	P42_13
23	P47_1	24	P42_12
25	P47_0	26	P42_11
27		28	P42_10
29	P46_15	30	P42_9
31	P46_14	32	P42_8
33	P46_13	34	P42_7
35	P46_12	36	P42_6
37	P46_11	38	P42_5
39	P46_10	40	P42_4
41	P46_9	42	P42_3
43	P46_8	44	P42_2
45	P46 7	46	P42 1
47	P46 6	48	P42_0
49	P46_5	50	
51	P46 4	52	P43 12
53	P46_3	54	P43 11
55	P46_2	56	P43_10
57	P46 1	58	P43 9
59	P46_0	60	P43_8
61	1 40_0	62	P43_7
63	P16 0	64	P43_6
65	P16_0	66	P43_5
67	P16_2	68	P43_3
69	P16_3	70	P43_4
71			
	P16_4	72	P43_2
73	P16_5	74	P43_1
75	P16_6	76	P43_0
77	P16_7	78	D47.0
79	P16_8	80	P17_0
81	P16_9	82	P17_1
83	P16_10	84	P17_2
85	P16_11	86	P17_3
87		88	P17_4
89	P45_13	90	P17_5
91	P45_12	92	P17_6
93	P45_11	94	P17_7
95	P45_10	96	P17_8
97	P45_9	98	P17_9
99	P45_8	100	P17_10
101	P45_7	102	P17_11
103	P45_6	104	
105	P45_5	106	P44_11
107	P45_4	108	P44_10
109	P45_3	110	P44_9
111	P45_2	112	P44_8
113	P45_1	114	P44_7
115	P45_0	116	P44_6
117	1 TO_U	118	P44_5
117		110	1 44_0

Pin	Function / Port	Pin	Function / Port
119	P10_0	120	P44_4
121	P10_1	122	P44_3
123	P10_2	124	P44_2
125	P10_3	126	P44_1
127	P10_4	128	P44_0
129	P10_5	130	
131	P10_6	132	P11_0
133	P10_7	134	P11_1
135	P10_8	136	P11_2
137	P10_9	138	P11_3
139	P10_10	140	P11_4
141	P10_11	142	P11_5
143		144	P11_6
145	ETNB0MDIO	146	P11_7
147	ETNB0MDC	148	
149	P467_ETNB0TXD3	150	P42_ETNB0TXD3
151	P467_ETNB0TXD2	152	P42_ETNB0TXD2
153	P467_ETNB0TXD1	154	P42_ETNB0TXD1
155	P467_ETNB0TXD0	156	P42_ETNB0TXD0
157	P467_ETNB0TXEN	158	P42_ETNB0TXEN
159	P467_ETNB0TXER	160	P42_ETNB0TXER
161	P467_ETNB0COL	162	P42_ETNB0COL
163	P467_ETNB0RSDV	164	P42_ETNB0RSDV
165	P467_ETNB0TXCLK	166	P42_ETNB0TXCLK
167	P467_ETNB0RXCLK	168	P42_ETNB0RXCLK
169	P467_ETNB0RXD3	170	P42_ETNB0RXD3
171	P467_ETNB0RXD2	172	P42_ETNB0RXD2
173	P467_ETNB0RXD1	174	P42_ETNB0RXD1
175	P467_ETNB0RXD0	176	P42_ETNB0RXD0
177	P467_ETNB0RXDV	178	P42_ETNB0RXDV
179	P467_ETNB0RXER	180	P42_ETNB0RXER
181	GND	182	GND
183	GND		

## 8.2 Test pin connectors

Note: The test-pin headers CN3 to CN12 are directly connected to the MCU pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

Table 8-3: Pin assignment of connector (CN3) P0

Pin	Power Domain	Port	Pin	Power Domain	Port
1	EVCC	P0_0	2	EVCC	P0_1
3	EVCC	P0_2	4	EVCC	P0_3
5	EVCC	P0_4	6	EVCC	P0_5
7	EVCC	P0_6	8	EVCC	P0_7
9	EVCC	P0_8	10	EVCC	P0_9

Table 8-4: Pin assignment of connector (CN4) P10

Pin	Power Domain	Port	Pin	Power Domain	Port		
1	A0VCC	P10_0	2	A0VCC	P10_1		
3	A0VCC	P10_2	4	A0VCC	P10_3		
5	A0VCC	P10_4	6	A0VCC	P10_5		
7	A0VCC	P10_6	8	A0VCC	P10_7		
9	A0VCC	P10_8	10	A0VCC	P10_9		
11	A0VCC	P10_10	12	A0VCC	P10_11		

Table 8-5: Pin assignment of connector (CN5) JP0

Pin	Power Domain	Port	Pin	Power Domain	Port
1	EVCC	JP0_0	2	EVCC	JP0_1
3	EVCC	JP0_2	4	EVCC	JP0_3
5	EVCC	JP0_4	6	EVCC	JP0_5

Table 8-6: Pin assignment of connector (CN6) System Function Pins

Pin	Power Domain	Port	Pin	Power Domain	Port
1	EVCC	FLMD0	2	EVCC	PWRCTL
3	EVCC	PWRGD	4	EVCC	RESETZ

Table 8-7: Pin assignment of connector (CN7) P1

Pin	Power Domain	Port	Pin	Power Domain	Port
1	B0VCC	P1_0	2	B0VCC	P1_1
3	B0VCC	P1_2	4	B0VCC	P1_3
5	B0VCC	P1_4	6	B0VCC	P1_5
7	B0VCC	P1_6	8	B0VCC	P1_7
9	B0VCC	P1_8	10	B0VCC	P1_9
11	B0VCC	P1_10	12	B0VCC	P1_11

Table 8-8: Pin assignment of connector (CN8) P11 / Analog Pins

Pin	Power Domain	Port	Pin	Power Domain	Port
1	A0VCC	P11_0	2	A0VCC	P11_1
3	A0VCC	P11_2	4	A0VCC	P11_3
5	A0VCC	P11_4	6	A0VCC	P11_5
7	A0VCC	P11_6	8	A0VCC	P11_7

Table 8-9: Pin assignment of connector (CN9) P16 / ISM Pins

				_ ,	
Pin	Power Domain	Port	Pin	Power Domain	Port
1	ISMVCC	P16_0	2	ISMVCC	P16_1
3	ISMVCC	P16_2	4	ISMVCC	P16_3
5	ISMVCC	P16_4	6	ISMVCC	P16_5
7	ISMVCC	P16_6	8	ISMVCC	P16_7
9	ISMVCC	P16_8	10	ISMVCC	P16_9
11	ISMVCC	P16_10	12	ISMVCC	P16_11

Table 8-10: Pin assignment of connector (CN10) P2

Pin	Power Domain	Port	Pin	Power Domain	Port			
1	B0VCC	P2_0	2	B0VCC	P2_1			
3	B0VCC	P2_2	4	B0VCC	P2_3			
5	B0VCC	P2_4	6	B0VCC	P2_5			
7	B0VCC	P2_6	8	B0VCC	P2_7			
9	B0VCC	P2_8	10	B0VCC	P2_9			
11	B0VCC	P2_10	12	B0VCC	P2_11			

Table 8-11: Pin assignment of connector (CN11) P17 / ISM Pins

·u	rable of the in accignment of connector (citri). If the interior							
Pin	Power Domain	Port	Pin	Power Domain	Port			
1	ISMVCC	P17_0	2	ISMVCC	P17_1			
3	ISMVCC	P17_2	4	ISMVCC	P17_3			
5	ISMVCC	P17_4	6	ISMVCC	P17_5			
7	ISMVCC	P17_6	8	ISMVCC	P17_7			
9	ISMVCC	P17_8	10	ISMVCC	P17_9			
11	ISMVCC	P17_10	12	ISMVCC	P17_11			

Table 8-12: Pin assignment of connector (CN12) P3

		•		` ,	
Pin	Power Domain	Port	Pin	Power Domain	Port
1	B1VCC	P3_0	2	B1VCC	P3_1
3	B1VCC	P3_2	4	B1VCC	P3_3
5	B1VCC	P3_4	6	B1VCC	P3_5
7	B1VCC	P3_6	8	B1VCC	P3_7
9	B1VCC	P3_8	10	B1VCC	P3_9
11	B1VCC	P3_10	12	B1VCC	P3_11
12	B1VCC	P3_12	14	B1VCC	P3_13

## 8.3 Connectors for external components

CN15 is used for 24bit RGB data output with RSDS signal from VO0. This connector can be connected to an LCD panel with RSDS I/F. The RSDS connector only has RGB data and power supply. The SYNC signal have to be connected from the TCON0.

Table 8-13: Connector (CN15) pin assignment

rable 0-13. Connector (CN13) pin assignment							
Pin	Function	port	Pin	Function	port		
1	+12V		2	RSDS_CLKP	P45_0		
3	RVCC/B5VCC		4	RSDS_CLKN	P45_1		
5	GND		6	GND			
7	RSDS_R0P	P44_0	8	RSDS_G2P	P45_2		
9	RSDS_R0N	P44_1	10	RSDS_G2N	P45_3		
11	GND		12	GND			
13	RSDS_R1P	P44_2	14	RSDS_G3P	P45_4		
15	RSDS_R1N	P44_3	16	RSDS_G3N	P45_5		
17	GND		18	GND			
19	RSDS_R2P	P44_4	20	RSDS_B0P	P45_6		
21	RSDS_R2N	P44_5	22	RSDS_B0N	P45_7		
23	GND		24	GND			
25	RSDS_R3P	P44_6	26	RSDS_B1P	P45_8		
27	RSDS_R3N	P44_7	28	RSDS_B1N	P45_9		
29	GND		30	GND			
31	RSDS_G0P	P44_8	32	RSDS_B2P	P45_10		
33	RSDS_G0N	P44_9	34	RSDS_B2N	P45_11		
35	GND		36	GND			
37	RSDS_G1P	P44_10	38	RSDS_B3P	P45_12		
39	RSDS_G1N	P44_11	40	RSDS_B3N	P45_13		

# 9 Adapter board Encoding Address

As also mentioned in chapter 6, three pins of the MCU ports are populated with weak PU/PD resistors that encode the adapter board type. These PU/PD resistors can be unconnected with the DIP switch DSW1 The Adapter Board Encoding Address can be used by the MCU software in order to allow Adapter-Board specific setup (e.g. set the multiplexers on the adapter- and main- board right, as they might differ a bit depending on the adapter board.)

Table 9-1: Adapter board encoding address setting

Adapter Board Encoding Address settings							
Board	Encoding						
	P1_0	P1_1	P1_2	Comment			
D1M2H Adapter	PD (0)	PU (1)	PD (0)	Code "2"			

# 10 Appendix

# 10.1 Components list

Item	Ref	Components name	Manufacturer	
1	CN1, CN2	QTH-090-02-L-D-A	SAMTEC	
2	CN3	PREC005DFAN-RC	SULLINS	
3	CN4, CN7, CN9, CN10, CN11	PREC006DFAN-RC	SULLINS	
4	CN5	PREC003DFAN-RC	SULLINS	
5	CN6	PREC002DFAN-RC	SULLINS	
6	CN8	PREC004DFAN-RC	SULLINS	
7	CN12	PREC007DFAN-RC	SULLINS	
8	CN14	731310240	MOLEX	
9	CN15	302-S401	ON SHORE	
10	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C192, C193, C196, C197, C198, C199, C200, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C236,	GRM155B31C104KA87D 0.1u/16V/1005/B	MURATA	
11	C237 C152	10u/16V/1608/B	MURATA	
12	C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C173, C190, C191, C238, C239	GRM21BB31C106KE15L 10u/16V/2012/B	MURATA	
13	C195, C194	GRM1552C1H200JZ01D 20p/50V/1005/CH	MURATA	
14	C201, C202	GRM1552C1H100JZ01D 10p/50V/1005/CH	MURATA	
15	DSW1, DSW2	218-4LPST	CTS	
16	D1, D2, D3, D6,	HSU-83	RENESAS	
17	D4, D5, D8, D9	* HSU-83	RENESAS	
18	JP1, JP2, JP3, JP4, JP5, JP7, JP11, JP12, JP13, JP14, JP15, JP16, JP18, JP19, JP20, JP21, JP22, JP23, JP25	XJ8C-0211	OMRON	
19	JP17,	XJ8D-0311	OMRON	
20	JP8	*XJ8B-0111	OMRON	
21	JP9, JP10, JP24	*XJ8C-0211	OMRON	
22	JP6	* XJ8D-0311	OMRON	
23	PAD1	SFMA_IO00		
24	PAD2	SFMA_IO10		
25	PAD3	SFMA_IO20		
26	PAD4	SFMA_IO30		
27	PAD5	SFMA_CLK0		
28	PAD6	SFMA_SSL0		
29	PAD7	SFMA_IO01		
30	PAD8	SFMA_IO11		

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31	PAD9	SFMA_IO21	
32	PAD10	SFMA_IO31	
33	PAD11	SFMA_CLK1	
34	PAD12	SFMA_SSL1	
35	RA1, RA2, RA3, RA4, RA5, RA6, RA7, RA8, RA9, RA10, RA11	*CN1E4ATD223J	KOA
36	R1, R2, R5, R6, R7, R8	RK73H1ETTD1001F 1K/1005/1%	KOA
37	R9	RK73H1ETTD1500F 150ohm/1005/1%	KOA
38	R10, R11, R12, R21, R22, D9	0ohm/1005/1%	KOA
39	R13, R16, R17	*470K/1005/1%	KOA
40	R14, R15, R18	RK73H1ETTD4703F 470K/1005/1%	KOA
41	R19	RK73H1ETTP22R0F 22ohm/1005/1%	KOA
42	R20	RK73H1ETTD2202F 22K/1005/1%	KOA
43	R23, R24, R25, R26, R58, R60, R61, R62, R64, R65	RK73H1ETTD1002F 10K/1005/1%	KOA
44	R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R39, R41, R42	RK73H1ETTD1000F 100ohm/1005/1%	KOA
45	R63	*10K/1005/1%	KOA
46	TP1, TP2, TP3, TP4	HK-5-G-Black	MAC8
47	UM1, UM2	MT47H128M16RT-25E IT	MICRON
48	U1	RH850/D1M2H	RENESAS
49	U2, U5, U8	IDTQS3VH16233PAG8	IDT
50	U6, U7	FST16233MTDX	FAIRCHILD
51	U3, U4	MX25L51245GMI-10G	MACRONIX
52	U9, U10	FSA4159P6X	FAIRCHILD
53	X1	NC-206 32.768KHz	KYUSHU DENTSU
54	X2	7A-8.000MAAE-T	TXC
55	Y1	*1-390261-2	TE

## 10.2 Schematics of the D1x Mango D1M2H Adapter Board

The following pages contain the full schematics of the Mango D1M2H Adapter Board. For the schematics of the Main Board, please see the dedicated Main Board manual.

# RH850(mango) D1M2H Adapter Board Rev1.5

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1	TABLE of CONTENTS(This Page)	1.5
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3	CPU CONNECTOR	1.5
4	TEST POINT	1.0
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8	P01-P02-P03	1.0
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10	P16-P17	1.0
11	P21-P42	1.4
12	P43-P46-P47	1.3
13	P44-P45	1.0

# **Revision History**

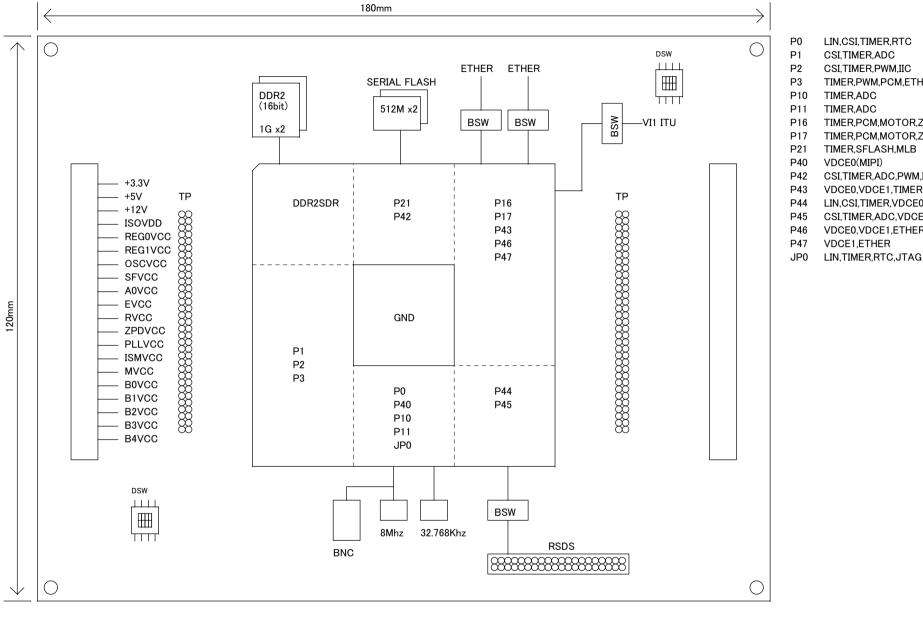
DATE	Rev	Page	DESCRIPTION
2014.3.20	1.0		release version
2014.4.28	1.1		wire add CN1.60pin <> U3.U4.3pin pattern cut CN1.138pin(RESETZ) <> U3.U4.3pin
2014.5.7	1.2		CN14,JP6,JP8,JP9 -> NoMount
2014.12.18	1.3		U2,U5,U8,U9,U10 Model number change D4,D5,D8,D9 -> NoMount
2016.12.15	1.4		Add 10Kohm Pull-up
2017.6.2	1.5		change FLMD0

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Note
*All resistors 1% accuracy  *For more information check the bill of materials  *GND guard  *Equal-length wiring  *Impedance  *No Mount **
NetList Result 269 Parts, 27 Library Parts, 487 Nets, 1941 Pins

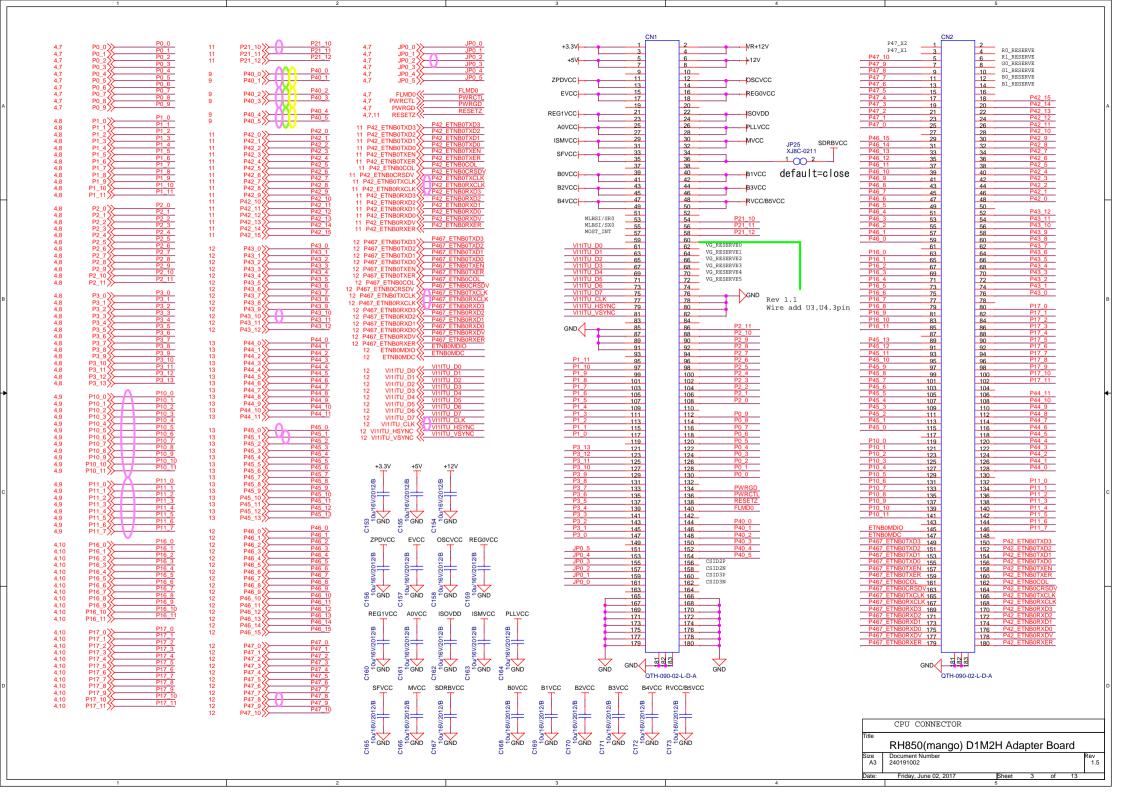
	TALBE of CONTENT	TS(This Page)			
Title	RH850(mango) D	1M2H Adapte	r Boa	rd	
Size A3	Document Number 240191002				Rev 1.5
Date:	Friday, June 02, 2017	Sheet 1	of	13	

# RH850(mango) D1M2H Adapter Board Block Diagram

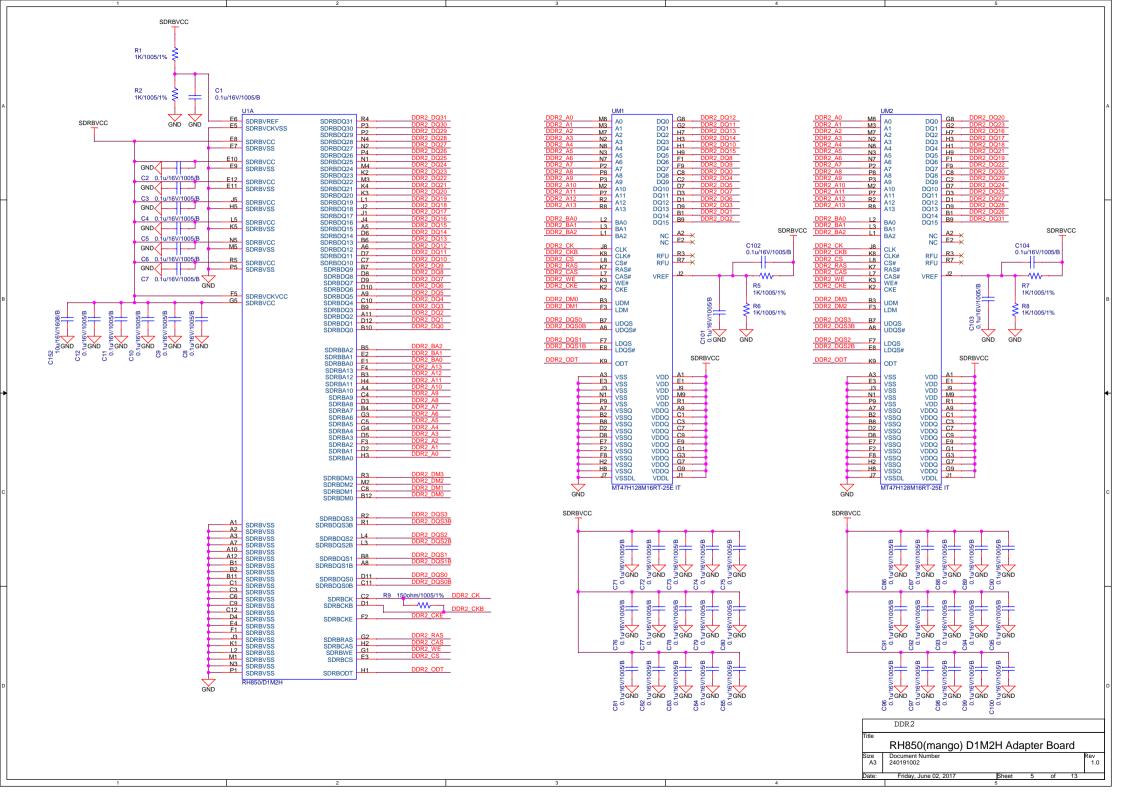


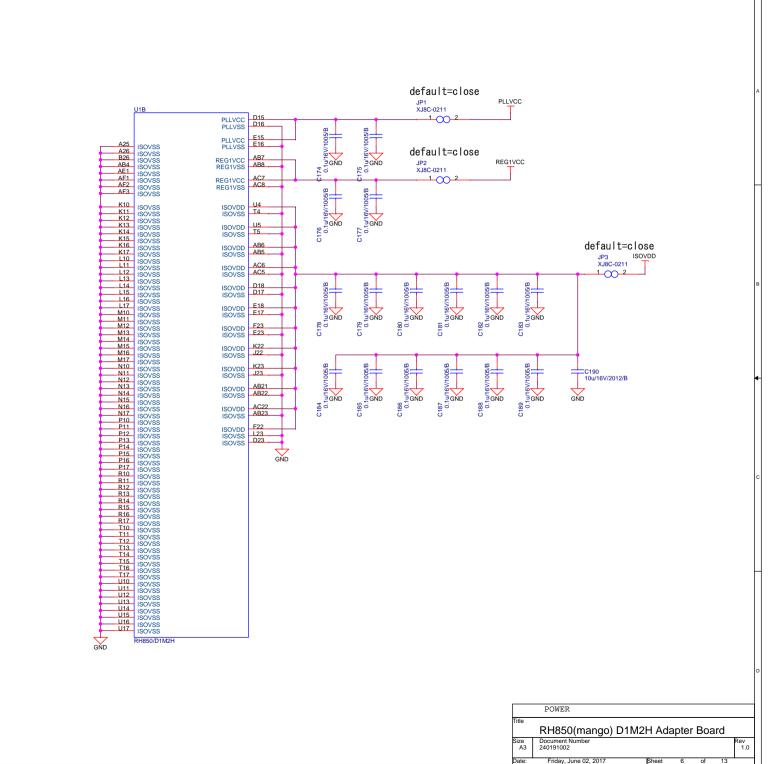
CSI.TIMER.ADC CSI,TIMER,PWM,IIC TIMER,PWM,PCM,ETHER,SG,SSIF,IIC,ADC TIMER,ADC TIMER,ADC TIMER,PCM,MOTOR,ZPD TIMER,PCM,MOTOR,ZPD,ADC TIMER.SFLASH.MLB VDCE0(MIPI) CSI.TIMER.ADC.PWM.IIC.ETHER.SG.VDCE0 VDCE0, VDCE1, TIMER, LCD LIN, CSI, TIMER, VDCE0, PWM, LCD CSI,TIMER,ADC,VDCE0,PWM,LCD VDCE0, VDCE1, ETHER VDCE1,ETHER

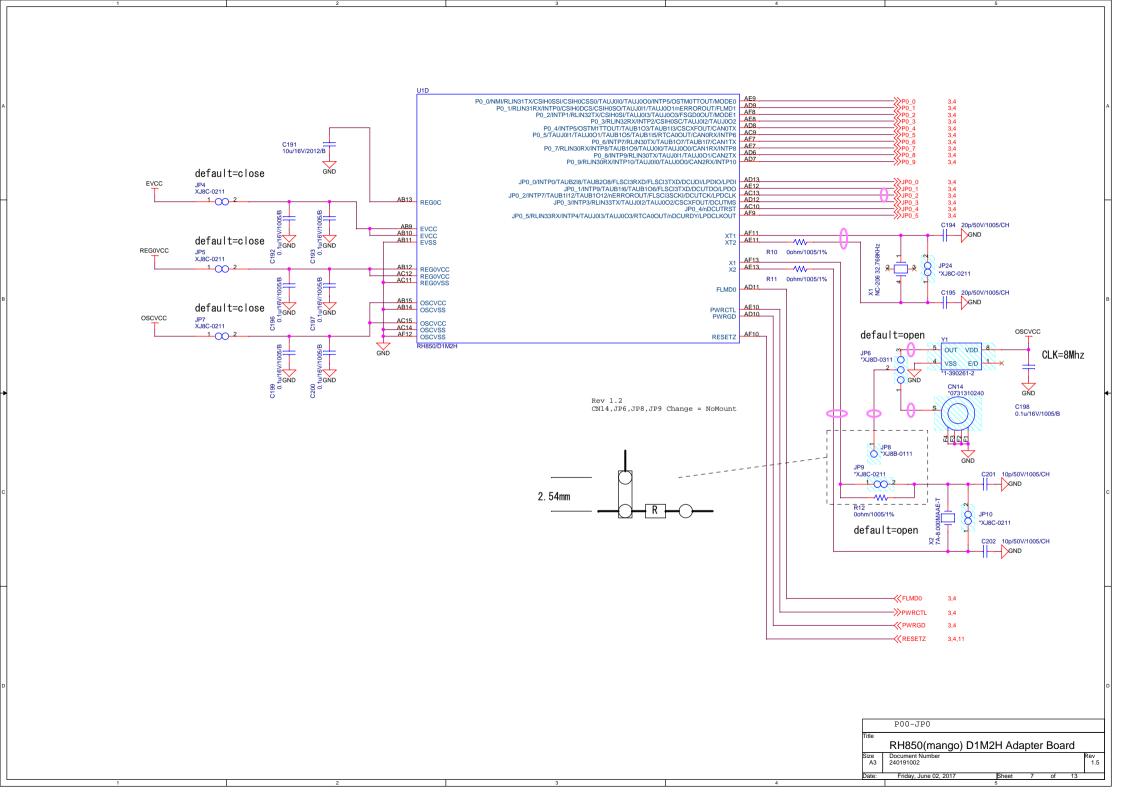
BLOCK DIAGRAM RH850(mango) D1M2H Adapter Board Document Number 240191002

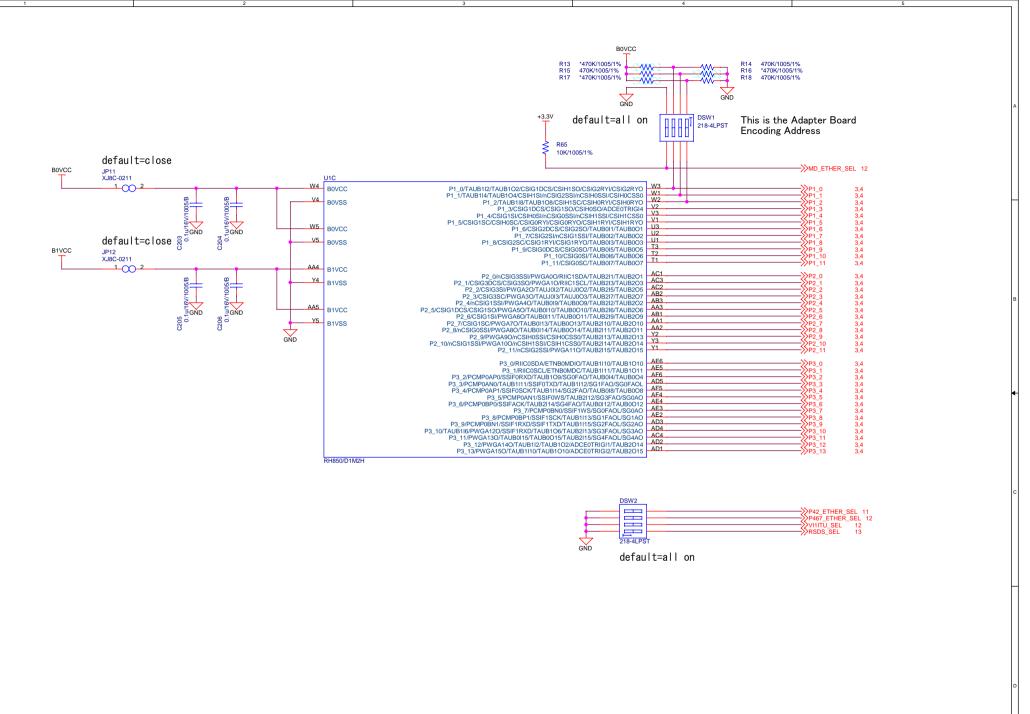




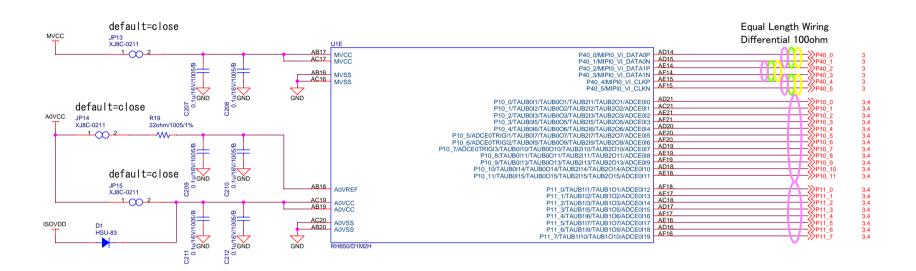




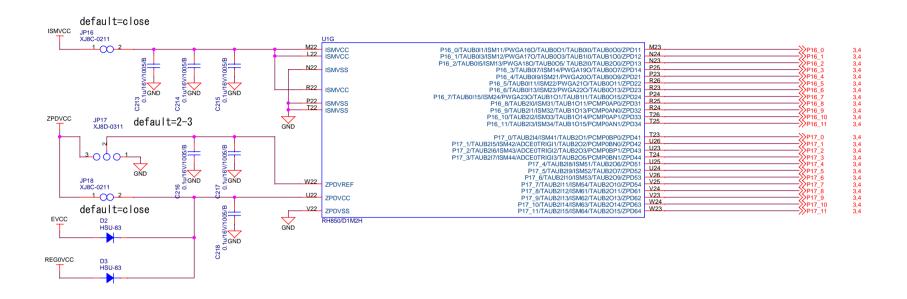




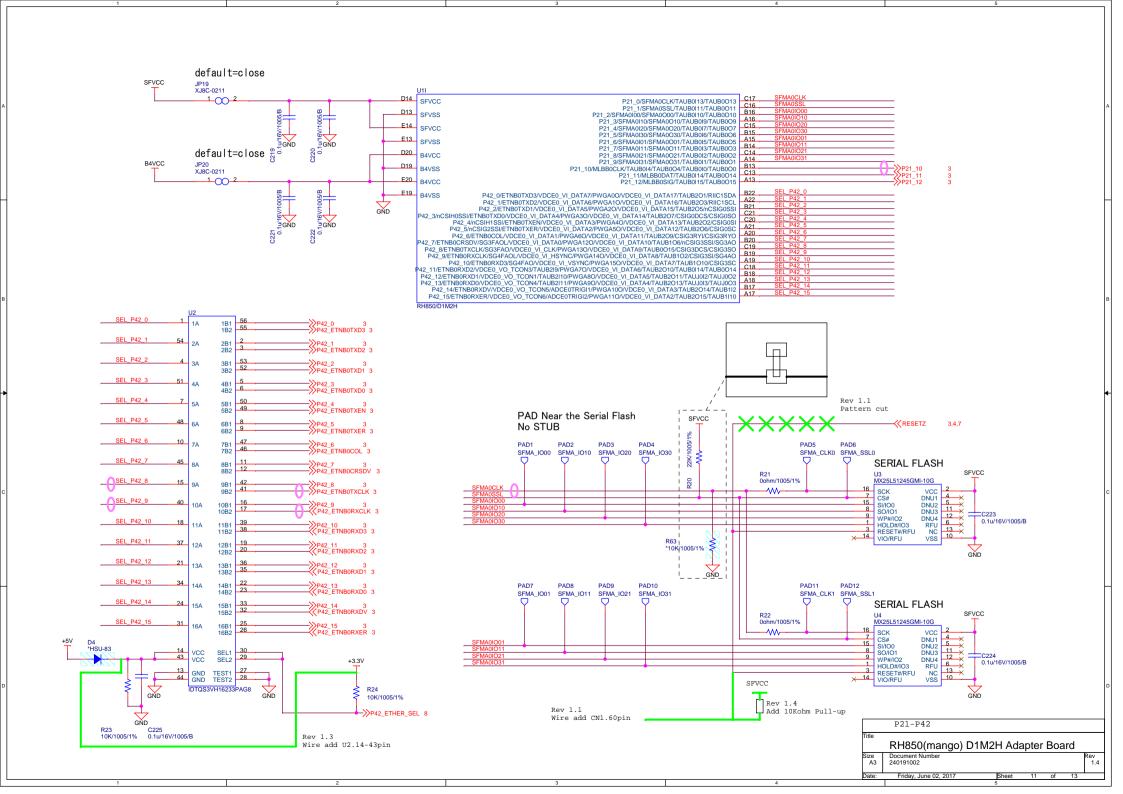
P01-P02-P03 RH850(mango) D1M2H Adapter Board Document Numbe Friday, June 02, 2017

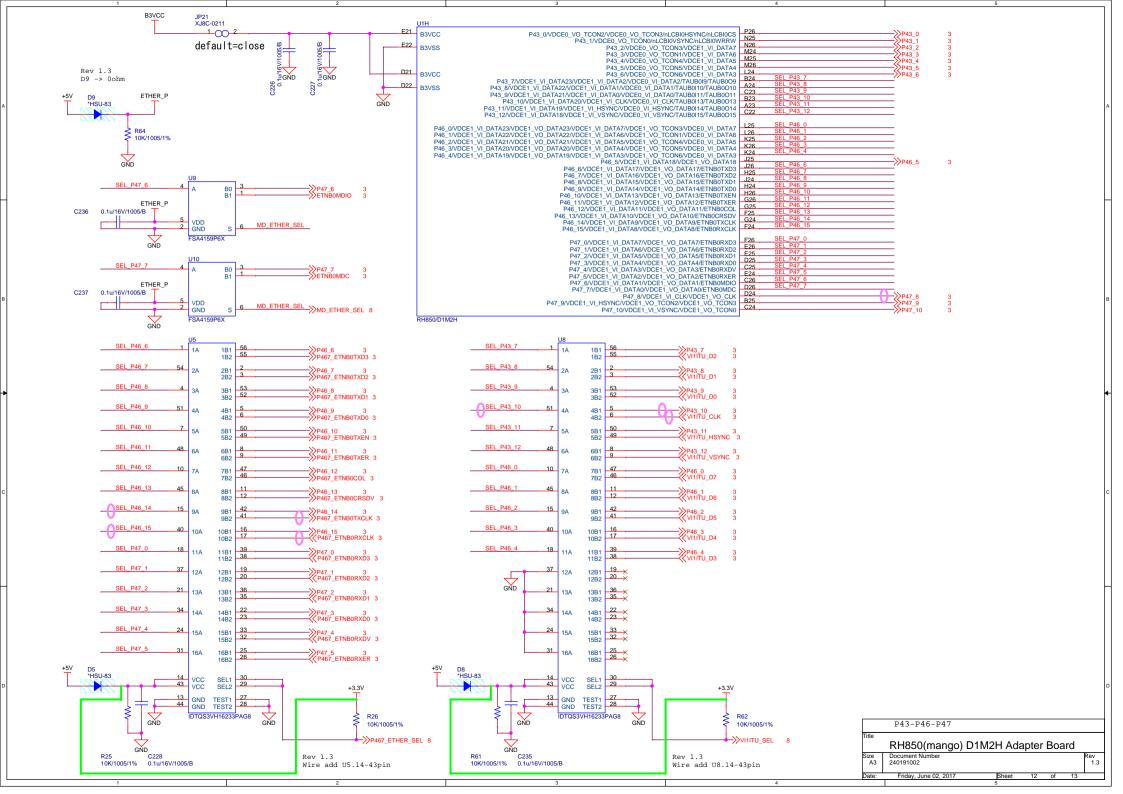


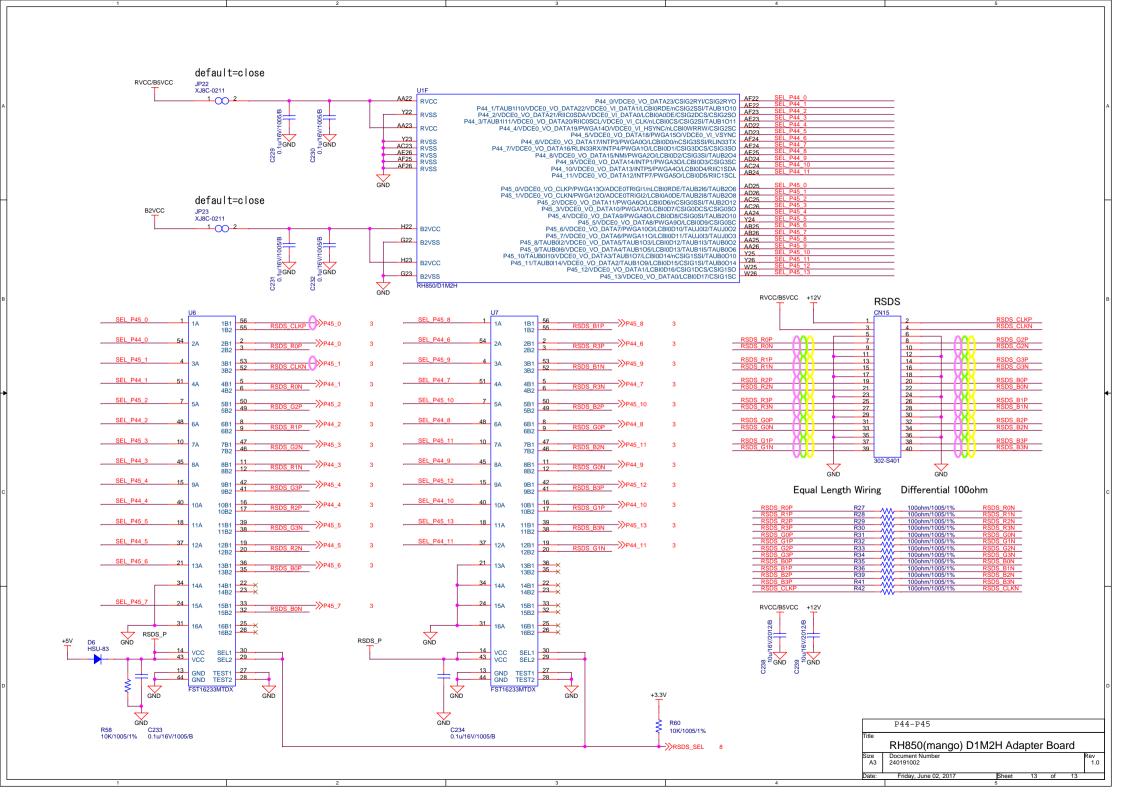
P10-P11-P40 RH850(mango) D1M2H Adapter Board Document Number 240191002 Friday, June 02, 2017



P16-P17 RH850(mango) D1M2H Adapter Board Document Number 240191002 Friday, June 02, 2017







# 11 Revision history

		Revised contents	
Rev.	Release date	Page	Subject
Rev.0.01	2014-April		Draft version created
Rev.0.02	2014-April-30		Full review of document. Some open points to be corrected
Rev.0.03	2014-May-06		Fixed typos and changed chapters/pages: Multiplexers, Schematics
Rev.0.04	2014-May-07		Fixed typos, Component List
Rev.0.05	2014-June-03	16, 17	Fixed typos
Rev.0.06	2014-October-20	10, 11, 13	Fixed typos
Rev.0.07	2015-April-15		Fixed typos, component list, tables and figures Changed chapters/pages
Rev.1.00	2016-Dec-23		Schematics update, Document release
Rev.1.01	2017-Jun-06		Schematics update

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

#### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

— The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

#### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

— The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

#### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

— The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

#### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

#### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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