Hardware Specification

RH850/D1x Evaluation Boards

Evaluation Boards for
the D1x Dashboard MCU Series

D1M1A Mango Adapter Board (SBEV-RH850-D1M1A)

Please use this manual together with the respective main board manual.

Preliminary Hardware User's Manual Adapter Board D1M1A

-DRAFT VERSION-

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1 Introduction

The RH850/D1x Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/D1x microcontrollers.
Since the adapter board cannot be used as a standalone board, this board has to be mated with a mainboard for full functionality.

Main features of the adapter board:

- Socket for mounting a device
- Power supply from main board
- Device programming capability (Connector on main board)
- Device debugging capability (Connector on main board)
- Pin headers for direct access to each device pin
- MainOSC and SubOSC circuitry
- Connectors to MainBoard
- SDR-SDRAM, NAND Flash, Serial Flash and Octa MCP

This document describes the functionality provided by the adapter board and guides the user through its operation.
For details regarding the operation of the microcontroller, refer to the RH850/D1x User Manual.

2 Board Overview

The figure below depicts the D1M1A Mango Adapter Board. Functional blocks are highlighted.

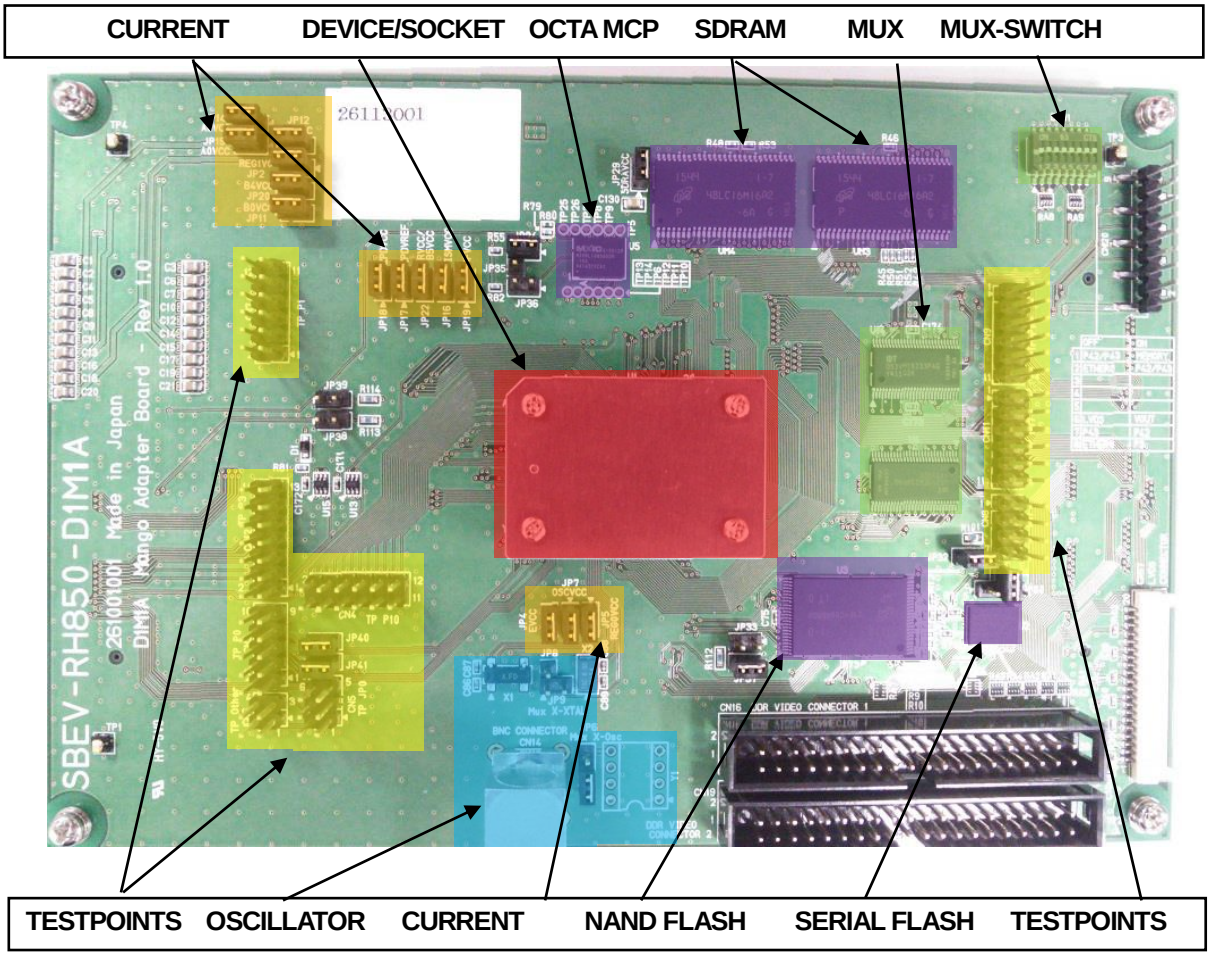

Figure 2-1: Adapter board for RH850/D1M1A

2.1 Mounting devices

The board is designed for reference use with the following device:
RH850/D1M1A (BGA272)

3 Power supply

3.1 Power supply structure

3.1.1 Current Measurement Jumpers

Each power supply of the MCU is routed through a single Jumper before connecting it to the MCU. This makes it possible to measure the current consumption of the MCU for each power supply domain in separate.

Table 3-1: Current measurement jumpers (excluding I/O ports supply)

Name of Supply	Jumper	Function
REG0VCC	JP5	AWO digital circuits via on-chip voltage regulator; nominal 3.3 V and 5 V
OSCVCC	JP7	MainOsc and SubOsc; nominal 3.3 V and 5 V
REG1VCC	JP2	Flash memory and PLL circuits; nominal 3.3 V
ZPDVCC	JP17,	Zero point detection circuit; nominal 5 V
ZPDVREF	JP18	Reference voltage of Zero Point detection, normal 5V
A0VREF	JP14	*Reference voltage of A/D Converter, normal 3.3V and 5V*

Table 3-2: Current measurement jumpres for I/O port supply

Name of Supply	Jumper	Function
EVCC	JP4	Port buffers P0 and JP0; nominal 3.3 V and 5 V
B0VCC	JP11	Port buffers port group P1; nominal 3.3 V and 5 V
B1VCC	JP12	Port buffers port group P3; nominal 3.3 V and 5 V
B4VCC	JP20	Port buffers port group P42; nominal 3.3 V and 5 V
B5VCC	JP22	Port buffers port groups P43_0, P43_1, P44 and P45; nominal 3.3 V and 5V.
SFVCC	JP19	Port buffers port group P21 (Serial Flash); nominal 3.3 V.
ISMVCC	JP16	Port buffers port groups P16 and P17 (Stepper Motor Controller/Driver) ; • nominal 5 V when used for stepper motor operation • nominal 3.3 V and 5 V when not used for stepper motor operation
A0VCC	JP15	Ports buffers port groups P10 and P11 (A/D Converter analog circuits and input buffers); nominal 3.3 V and 5 V
SDRAVCC(MVCC)	JP29	SDR-SDRAM I/F port buffers; norminal 3.3 V.

Notes on current measurement:

Currently, the reset line is not pulled-up to full EVCC voltage. This is caused by the drop out voltage of LED24 “RESET ACT” (V_{RESET} is only ~3.7V when EVCC is 5V). This leads to an EVCC leakage current caused by the RESETZ input buffer. To correctly measure the EVCC current, please add a 6.2kΩ resistor in parallel to LED24 “RESET ACT” on the Mango Main Board.

3.1.2 Voltage regulators and DC-DC converters

The power domains on the adapter board are supplied by the main board. The following voltages are generated on the main board.

Table 3-3: Main Power supply Source IC output voltage (from Main board)

IC	Input voltage	Voltage	Net name	Spec
U7	12V	5V	+5V	Max 4A
U8	12V	3.3V	+3.3V	Max 4A
U9	12V	5V	ISO+5V	Max 2A
U12	12V	3.3V	ISO+3.3V	Max 4A
U5	U12	1.25V	+1.25V	Max 2A
U6	U12	1.8V	+1.8V	Max 0.5A
U1	U8	2.5V	+2.5V	Max 1A
U2	U8	1.25V	+1.2V	Max 1A

3.1.3 Power Supply Selection Matrix

The voltages that can be selected to power each of the domains of the MCU differ for each device type. For D1M1A the following voltages can be configured for each power domain.

Table 3-4: Main Power supply Source IC output voltage

	D1M1A				
	other	3v3	5v	iso3v3	iso5v
REG0VCC		x	D		
OSCVCC		x	x	D	x
EVCC		x	D		
REG1VCC		x		D	
ISOVDD	1.25V				
PLLVCC					
B0VCC		x	x	D	x
B1VCC		x	x	D	x
B2VCC					
B3VCC					
B4VCC		x	x	D	x
B5VCC/RVCC		x	x	D	x
SDRAVCC(MVCC)		x		D	
SFVCC		x		D	
SDRBVCC	1.8V				
ISMVCC		x	x	x	D
ZPDVCC		x	D	x	x
A0VCC		x	x	D	x

X: Possible Setting, D: Default Setting

4 Clock source

4.1 Overview

There are 3 options for main clock input to target MCU.

- Crystal (8MHz)
- Crystal oscillator (8MHz)
- Clock input from pulse generator

The default option is to use the soldered crystals for the high speed and the low speed oscillator.

4.2 Oscillator circuit

This figure shows schematic of oscillator block.

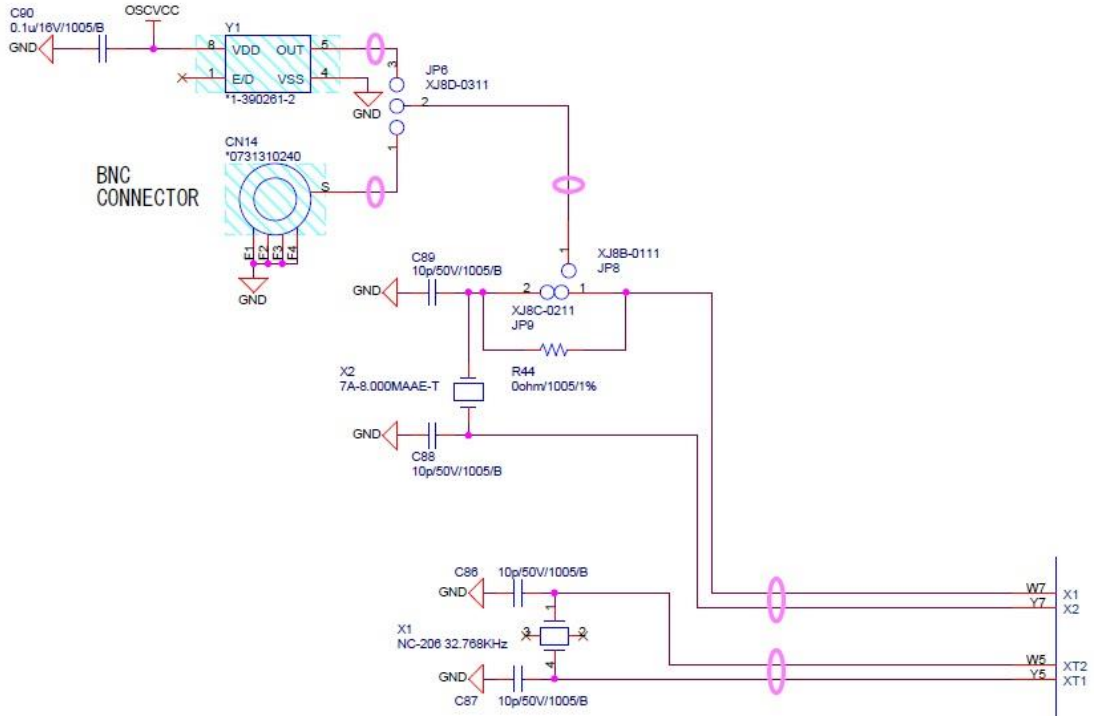

Figure 4-1: Schematic of oscillator block

4.3 Function specification

- **Main oscillator**
  Terminals: X1/X2 clock selection
  - Crystal (8MHz)
  - Ceralock (8MHz)
  - Direct clock input from external pulse generator

Table 4-1: Sub-Selection of external oscillator

Loc	Function	
JP6	**External oscillator sub-selection**	
	1-2 select	Use BNC connector (CN14).
	2-3 select	Use crystal oscillator Y1

Table 4-2: Selection of crystal or external oscillator

Loc	Function	
JP8 / JP9	**External oscillator select**	
	JP8/JP9 open R44 soldered	Use on-board crystal
	JP9 1-2 closed R44 unsoldered	Use on-board crystal
	JP8 JP9-1 closed R44 unsoldered	Use external oscillator (JP6)

- **Sub oscillator**
  Terminals: XT1/XT2
  - Crystal (32.768KHz)

5 External Memory function

5.1 Serial Flash

The serial flash can be used by setting DSW1.1=ON and by closing JP32 and opening JP33. It cannot be used simulaneuously with NAND Flash.

Type	Size	Interface / Speed	Package
1x MX66L1G85G (Macronix)	1Gbit (128MB)	8bit, DDR@80MHz	TFBGA-24

5.2 NAND Flash

The NAND flash can be used by setting DSW1.1=ON and by opening JP32 and closing JP33. It cannot be used simulaneuously with Serial Flash.

Type	Size	Package
1x MT29F4G08ABADAWP-IT (Micron)	4Gbit (512MB)	TSOP-48

5.3 Octa MCP

Port P21 is equipped with with OctaBus type memory. To use both RAM and Flash of the device, please close jumpers JP34, JP36 and JP37.

Type	Size	Package
1x MX65L12A64AA (Macronix)	512Mbit (64MB)	TFBGA-24

5.4 SDR-SDRAM

Type	Size	Interface / Speed	Package
2x MT48LC16M16A2P-6A (Micron)	2 x 256Mbit (32MB)	32bit, SDR@120MHz	TSOP-54

5.5 Mounted devices

Table 5-1: Mounted devices

Loc.	Manufacturer	Product name	Note
U2	Macronix	MX66L1G85G	1Gbit: DDR@80MHz, Dual Quad Serial Flash Memory JP32 closed and JP33 opened
U3	Micron	MT29F4G08ABADAWP-IT	4Gbit NAND Flash Memory JP32 opened and JP33 closed (default)
U5	Macronix	MX65L12A64AA	512Mbit Flash and 64Mbit RAM Octa MCP Memory JP34, JP36 and JP37 closed
UM3 **UM4**	Micron	MT48LC16M16A2P-6A	256Mbit x 2: SDR@120MHz, SDR-SDRAM Memory

5.6 Memory connection

Memory block consists of Serial Flash, NAND Flash, Octa MCP and SDR-SDRAM.

- **Serial Flash and NAND Flash Memory**

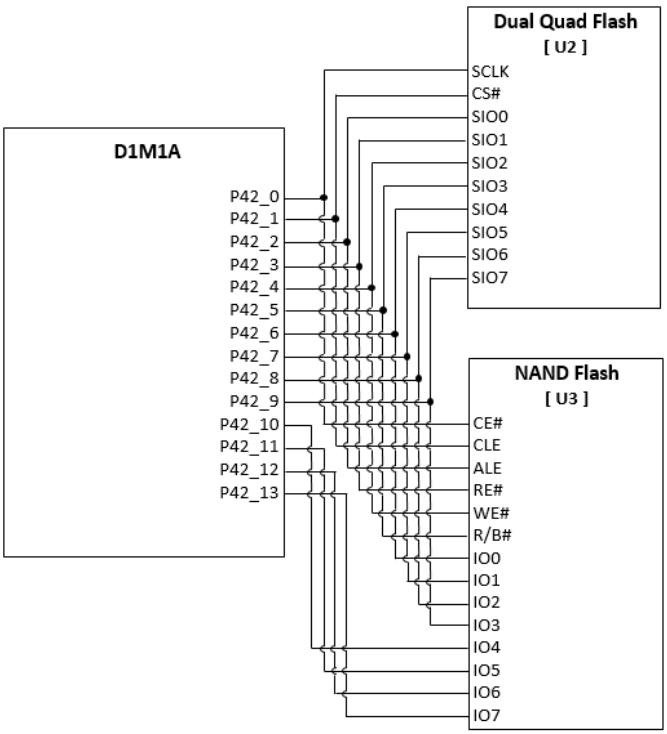

Figure 5-1: Serial Flash and NAND Flash memory block diagram

- **Octa MCP**

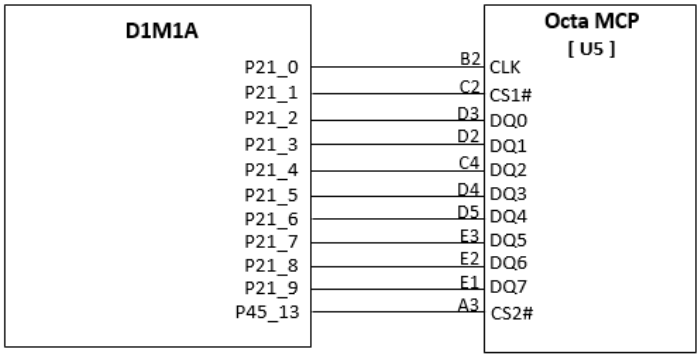

Figure 5-2: Octa MCP memory block diagram

▪ **SDR-SDRAM**

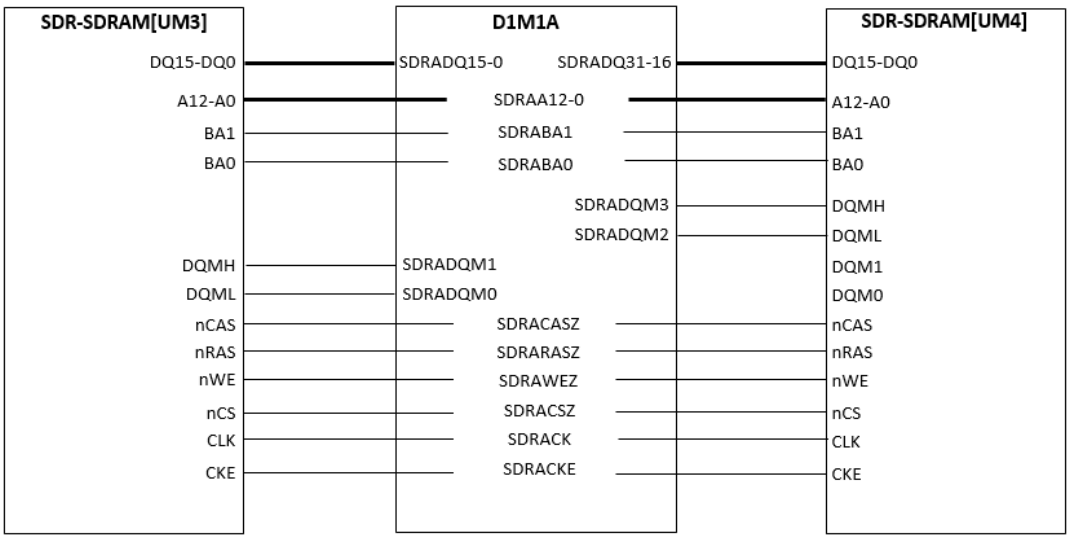

Figure 5-3 SDR-SDRAM memory block diagram

6 Multiplex Control

6.1 Overview

Multiplexers (mainly for Memory, Video I/O and Ethernet) shall be manually controlled by the user themselves via DIP switches (DSW1). Thus, the user has responsibility to avoid misconfiguration of the multiplexers that might destroy the device.

The following multiplexers are placed onto the adapter board.

Table 6-1: Signal Assignment and function of DSW1

Switch Position	Signal name	ON Function	OFF Function
DSW1.1	MUX_CONTROL1	Connect to Memories (Dual Quad and NAND Flash) *1	Connect to Main board
DSW1.2	MUX_CONTROL2	Conect to P42 or P43 *2	Connect ot Ether *3
DSW1.3	-	-	-
DSW1.4	-	-	-
DSW1.5	-	-	-
DSW1.6	MUX_CONTROL6	Connect to Vout	Connect to LVDS
DSW1.7	MUX_CONTROL7	Connect to P42 *2	Connect to P43 *2
DSW1.8	MUX_CONTROL8	Connect to P3_0 and P3_1	Connect to Ether *3

*1: When using NAND Flash, JP33 is closed and JP32 is open (Default).
When using Dual Quad, JP33 is open and JP32 is closed.
*2: It is combination setting DSW1.2 and DSW1.7.
*3: It is combination setting DSW1.2 and DSW1.8.

The following tables show the signal assignment of the multiplexers with respect to the switch positions.

From Table 6-2 to Table 6-7 are multiplexers that route the MCU signals either to the Main Board or to the Adapter Board according to the switch position.

Table 6-2: Multiplex control table (U11) MUX_CONTROL1 (DSW1.1)

Pin	IN	OUT	
		MUX_CONTROL1: OFF	MUX_CONTROL1: ON
1A	CPU_P42_0	BOTTOM_P42_0	MEMORY_P42_0
2A	CPU_P42_15	BOTTOM_P42_15	-
3A	CPU_P42_1	BOTTOM_P42_1	MEMORY_P42_1
4A	CPU_P42_14	BOTTOM_P42_14	-
5A	CPU_P42_2	BOTTOM_P42_2	MEMORY_P42_2
6A	CPU_P42_13	BOTTOM_P42_13	MEMORY_P42_13
7A	CPU_P42_3	BOTTOM_P42_3	MEMORY_P42_3
8A	CPU_P42_12	BOTTOM_P42_12	MEMORY_P42_12
9A	CPU_P42_4	BOTTOM_P42_4	MEMORY_P42_4
10A	CPU_P42_11	BOTTOM_P42_11	MEMORY_P42_11
11A	CPU_P42_5	BOTTOM_P42_5	MEMORY_P42_5
12A	CPU_P42_10	BOTTOM_P42_10	MEMORY_P42_10
13A	CPU_P42_6	BOTTOM_P42_6	MEMORY_P42_6
14A	CPU_P42_9	BOTTOM_P42_9	MEMORY_P42_9
15A	CPU_P42_7	BOTTOM_P42_7	MEMORY_P42_7
16A	CPU_P42_8	BOTTOM_P42_8	MEMORY_P42_8

Table 6-3: Multiplex control table (U4) MUX_CONTROL2 (DSW1.2)

Pin	IN	OUT	
		MUX_CONTROL2: OFF	MUX_CONTROL2: ON
1A	BOTTOM_P42_0	P42_ETNB0TXD3	SEL_P42_0_P43_2
2A	BOTTOM_P42_15	P42_ETNB0RXER	P42_15
3A	BOTTOM_P42_1	P42_ETNB0TXD2	SEL_P42_1_P43_3
4A	BOTTOM_P42_14	P42_ETNB0RXDV	P42_14
5A	BOTTOM_P42_2	P42_ETNB0TXD1	SEL_P42_2_P43_4
6A	BOTTOM_P42_13	P42_ETNB0RXD0	P42_13
7A	BOTTOM_P42_3	P42_ETNB0TXD0	SEL_P42_3_P43_5
8A	BOTTOM_P42_12	P42_ETNB0RXD1	P42_12
9A	BOTTOM_P42_4	P42_ETNB0TXEN	SEL_P42_4_P43_6
10A	BOTTOM_P42_11	P42_ETNB0RXD2	P42_11
11A	BOTTOM_P42_5	P42_ETNB0TXER	SEL_P42_5_P43_7
12A	BOTTOM_P42_10	P42_ETNB0RXD3	SEL_P42_10_P43_12
13A	BOTTOM_P42_6	P42_ETNB0COL	SEL_P42_6_P43_8
14A	BOTTOM_P42_9	P42_ETNB0RXCLK	SEL_P42_9_P43_11
15A	BOTTOM_P42_7	P42_ETNB0CRSDV	SEL_P42_7_P43_9
16A	BOTTOM_P42_8	P42_ETNB0TXCLK	SEL_P42_8_P43_10

Table 6-4: Multiplex control table (U12) MUX_CONTROL6 (DSW1.6)

Pin	IN	OUT	
		MUX_CONTROL6: OFF	MUX_CONTROL6: ON
1A	CPU_P45_2	LVDS0_CH1_P	VO_P45_2
2A	-	-	-
3A	CPU_P45_3	LVDS0_CH1_N	VO_P45_3
4A	-	-	-
5A	CPU_P45_4	LVDS0_CH2_P	VO_P45_4
6A	-	-	-
7A	CPU_P45_5	LVDS0_CH2_N	VO_P45_5
8A	-	-	-
9A	CPU_P45_6	LVDS0_CH3_P	VO_P45_6
10A	-	-	-
11A	CPU_P45_7	LVDS0_CH3_N	VO_P45_7
12A	-	-	-
13A	CPU_P45_0	LVDS0_CH0_P	VO_P45_0
14A	CPU_P45_9	LVDS0_CH4_N	VO_P45_9
15A	CPU_P45_1	LVDS0_CH0_N	VO_P45_1
16A	CPU_P45_8	LVDS0_CH4_P	VO_P45_8

Table 6-5: Multiplex control table (U14) MUX_CONTROL7 (DSW1.7)

Pin	IN	OUT	
		MUX_CONTROL7: OFF	MUX_CONTROL7: ON
1A	SEL_P42_0_P43_2	P43_2	P42_0
2A	-	-	-
3A	SEL_P42_1_P43_3	P43_3	P42_1
4A	-	-	-
5A	SEL_P42_2_P43_4	P43_4	P42_2
6A	-	-	-
7A	SEL_P42_3_P43_5	P43_5	P42_3
8A	-	-	-
9A	SEL_P42_4_P43_6	P43_6	P42_4
10A	-	-	-
11A	SEL_P42_5_P43_7	P43_7	P42_5
12A	SEL_P42_10_P43_12	P43_12	P42_10
13A	SEL_P42_6_P43_8	P43_8	P42_6
14A	SEL_P42_9_P43_11	P43_11	P42_9
15A	SEL_P42_7_P43_9	P43_9	P42_7
16A	SEL_P42_8_P43_10	P43_10	P42_8

Table 6-6: Multiplex control table (U13) MUX_CONTROL8 (DSW1.8)

Pin	IN	OUT	
		MUX_CONTROL8: OFF	MUX_CONTROL8: ON
A	SEL_P3_0	ETNB0MDIO	P3_0

Table 6-7: Multiplex control table (U15) MD_ETHER_SEL (DSW1.8)

Pin	IN	OUT	
		MUX_CONTROL8: OFF	MUX_CONTROL8: ON
A	SEL_P3_1	ETNB0MDC	P3_1

7 Socket

This chapter lists all connectors of the D1M1A adapter board. There are mainly three groups of connectors.

7.1 Overview

Adapter boards of MCU block cosists of below components.

- IC socket
- Test pin area and external connectors
- Main board connectors

D1x series have several package variant, therefore the IC socket depends upon the package variant.

7.2 RH850/D1M1A adapter board structure

Figure 7-1 shows D1M1A adapter board block diagram.

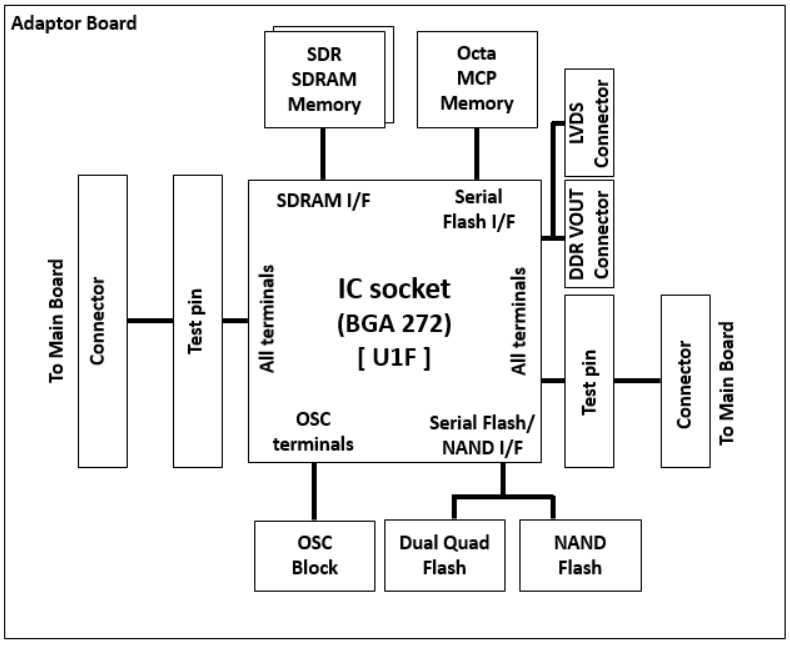

Figure 7-1: Block diagram of the MCU connections on the D1M1A Adapter board

7.3 Mounting socket

This board will be fitted with one of the socket types as shown below.

Table 7-1: IC socket (For the BGA272 Adaptor Board)

Manufacturer	Product name	Note
TOKYO ELETECH CORP.	LSPACK272Z2021RE12	Can be plugged into the BGA to Pin adapter. Device will be inserted into the LSPACK
TOKYO ELETECH CORP.	BSSOCKET272Z2021RE21N	BGA to Pin adapter. To be soldered. BSSOCKET connects to LSPACK

8 Connectors of the D1M1A adapter board

Connection to each pin of the device is possible via the connectors CN1 to CN12.

8.1 Main Board to Adapter Board connectors

Signal names that are highlighted in dark grey, are not used by the D1M1A adapter board.

Table 8-1: Pin assignment of connector (CN1)

Pin	Function / Port	Pin	Function / Port
1	+3.3V	2	VR+12V
3	+3.3V	4	VR+12V
5	+5V	6	+12V
7	+5V	8	+12V
9		10	
11	ZPDVCC	12	OSCVCC
13	ZPDVCC	14	OSCVCC
15	EVCC	16	REG0VCC
17	EVCC	18	REG0VCC
19		20	
21	REG1VCC	22	ISOVDD
23	REG1VCC	24	ISOVDD
25	A0VCC	26	PLLVCC
27	A0VCC	28	PLLVCC
29	ISMVCC	30	MVCC(SDRAVCC)
31	ISMVCC	32	MVCC(SDRAVCC)
33	SFVCC	34	SDRBVCC
35	SFVCC	36	SDRBVCC
37		38	
39	B0VCC	40	B1VCC
41	B0VCC	42	B1VCC
43	B2VCC	44	B3VCC
45	B2VCC	46	B3VCC
47	B4VCC	48	RVCC/B5VCC
49	B4VCC	50	RVCC/B5VCC
51		52	
53	MLBSI/SR0	54	P21_10
55	MLBSI/SX0	56	P21_11
57	MOST_INT	58	P21_12
59		60	SF_RESET
61	VI1ITU_D0	62	VG_RESERVE0
63	VI1ITU_D1	64	VG_RESERVE1
65	VI1ITU_D2	66	VG_RESERVE2
67	VI1ITU_D3	68	VG_RESERVE3
69	VI1ITU_D4	70	VG_RESERVE4
71	VI1ITU_D5	72	VG_RESERVE5
73	VI1ITU_D6	74	
75	VI1ITU_D7	76	GND
77	VI1ITU_CLK	78	GND
79	VI1ITU_HSYNC	80	GND
81	VI1ITU_VSYNC	82	GND
83		84	
85	GND	86	P2_11
87	GND	88	P2_10
89	GND	90	P2_9
91	GND	92	P2_8
93		94	P2_7
95	P1_11	96	P2_6
97	P1_10	98	P2_5
99	P1_9	100	P2_4

Pin	Function / Port	Pin	Function / Port
101	P1_8	**102**	P2_3
103	P1_7	**104**	P2_2
105	P1_6	**106**	P2_1
107	P1_5	**108**	P2_0
109	P1_4	**110**	
111	P1_3	**112**	P0_9
113	P1_2	**114**	P0_8
115	P1_1	**116**	P0_7
117	P1_0	**118**	P0_6
119		**120**	P0_5
121	P3_13	**122**	P0_4
123	P3_12	**124**	P0_3
125	P3_11	**126**	P0_2
127	P3_10	**128**	P0_1
129	P3_9	**130**	P0_0
131	P3_8	**132**	
133	P3_7	**134**	PWRGD
135	P3_6	**136**	PWRCTL
137	P3_5	**138**	RESETZ
139	P3_4	**140**	FLMD0
141	P3_3	**142**	
143	P3_2	**144**	P40_0
145	P3_1	**146**	P40_1
147	P3_0	**148**	P40_2
149		**150**	P40_3
151	JP0_5	**152**	P40_4
153	JP0_4	**154**	P40_5
155	JP0_3	**156**	CSID2P
157	JP0_2	**158**	CSID2N
159	JP0_1	**160**	CSID3P
161	JP0_0	**162**	CSID3N
163		**164**	
165	GND	**166**	GND
167	GND	**168**	GND
169	GND	**170**	GND
171	GND	**172**	GND
173	GND	**174**	GND
175	GND	**176**	GND
177	GND	**178**	GND
179	GND	**180**	GND
181	GND	**182**	GND
183	GND		

Table 8-2: Pin assignment of connector (CN2)

Pin	Function / Port	Pin	Function / Port
1	P47_X2	2	
3	P47_X1	4	R0_RESERVE
5	P47_10	6	R1_RESERVE
7	P47_9	8	G0_RESERVE
9	P47_8	10	G1_RESERVE
11	P47_7	12	B0_RESERVE
13	P47_6	14	B1_RESERVE
15	P47_5	16	
17	P47_4	18	P42_15
19	P47_3	20	P42_14
21	P47_2	22	P42_13
23	P47_1	24	P42_12
25	P47_0	26	P42_11
27		28	P42_10
29	P46_15	30	P42_9
31	P46_14	32	P42_8
33	P46_13	34	P42_7
35	P46_12	36	P42_6
37	P46_11	38	P42_5
39	P46_10	40	P42_4
41	P46_9	42	P42_3
43	P46_8	44	P42_2
45	P46_7	46	P42_1
47	P46_6	48	P42_0
49	P46_5	50	
51	P46_4	52	P43_12
53	P46_3	54	P43_11
55	P46_2	56	P43_10
57	P46_1	58	P43_9
59	P46_0	60	P43_8
61		62	P43_7
63	P16_0	64	P43_6
65	P16_1	66	P43_5
67	P16_2	68	P43_4
69	P16_3	70	P43_3
71	P16_4	72	P43_2
73	P16_5	74	P43_1
75	P16_6	76	P43_0
77	P16_7	78	
79	P16_8	80	P17_0
81	P16_9	82	P17_1
83	P16_10	84	P17_2
85	P16_11	86	P17_3
87		88	P17_4
89	P45_13	90	P17_5
91	P45_12	92	P17_6
93	P45_11	94	P17_7
95	P45_10	96	P17_8
97	P45_9	98	P17_9
99	P45_8	100	P17_10
101	P45_7	102	P17_11
103	P45_6	104	
105	P45_5	106	P44_11
107	P45_4	108	P44_10
109	P45_3	110	P44_9
111	P45_2	112	P44_8
113	P45_1	114	P44_7
115	P45_0	116	P44_6
117		118	P44_5

Pin	Function / Port	Pin	Function / Port
119	P10_0	**120**	P44_4
121	P10_1	**122**	P44_3
123	P10_2	**124**	P44_2
125	P10_3	**126**	P44_1
127	P10_4	**128**	P44_0
129	P10_5	**130**	
131	P10_6	**132**	P11_0
133	P10_7	**134**	P11_1
135	P10_8	**136**	P11_2
137	P10_9	**138**	P11_3
139	P10_10	**140**	P11_4
141	P10_11	**142**	P11_5
143		**144**	P11_6
145	ETNB0MDIO	**146**	P11_7
147	ETNB0MDC	**148**	
149	P467_ETNB0TXD3	**150**	P42_ETNB0TXD3
151	P467_ETNB0TXD2	**152**	P42_ETNB0TXD2
153	P467_ETNB0TXD1	**154**	P42_ETNB0TXD1
155	P467_ETNB0TXD0	**156**	P42_ETNB0TXD0
157	P467_ETNB0TXEN	**158**	P42_ETNB0TXEN
159	P467_ETNB0TXER	**160**	P42_ETNB0TXER
161	P467_ETNB0COL	**162**	P42_ETNB0COL
163	P467_ETNB0RSDV	**164**	P42_ETNB0RSDV
165	P467_ETNB0TXCLK	**166**	P42_ETNB0TXCLK
167	P467_ETNB0RXCLK	**168**	P42_ETNB0RXCLK
169	P467_ETNB0RXD3	**170**	P42_ETNB0RXD3
171	P467_ETNB0RXD2	**172**	P42_ETNB0RXD2
173	P467_ETNB0RXD1	**174**	P42_ETNB0RXD1
175	P467_ETNB0RXD0	**176**	P42_ETNB0RXD0
177	P467_ETNB0RXDV	**178**	P42_ETNB0RXDV
179	P467_ETNB0RXER	**180**	P42_ETNB0RXER
181	GND	**182**	GND
183	GND		

8.2 Test pin connectors

Note: **The test-pin headers CN3 to CN12 are directly connected to the MCU pins, therefore special care must be taken to avoid any electrostatic discharge or other damage to the device.**

Table 8-3: Pin assignment of connector (CN3) P0

Pin	Power Domain	Port	Pin	Power Domain	Port
1	EVCC	P0_0	2	EVCC	P0_1
3	EVCC	P0_2	4	EVCC	P0_3
5	EVCC	P0_4	6	EVCC	P0_5
7	EVCC	P0_6	8	EVCC	P0_7
9	EVCC	P0_8	10	EVCC	P0_9

Table 8-4: Pin assignment of connector (CN4) P10

Pin	Power Domain	Port	Pin	Power Domain	Port
1	A0VCC	P10_0	2	A0VCC	P10_1
3	A0VCC	P10_2	4	A0VCC	P10_3
5	A0VCC	P10_4	6	A0VCC	P10_5
7	A0VCC	P10_6	8	A0VCC	P10_7
9	A0VCC	P10_8	10	A0VCC	P10_9
11	A0VCC	P10_10	12	A0VCC	P10_11

Table 8-5: Pin assignment of connector (CN5) JP0

Pin	Power Domain	Port	Pin	Power Domain	Port
1	EVCC	JP0_0	2	EVCC	JP0_1
3	EVCC	JP0_2	4	EVCC	JP0_3
5	EVCC	JP0_4	6	EVCC	JP0_5

Table 8-6: Pin assignment of connector (CN6) System Function Pins

Pin	Power Domain	Port	Pin	Power Domain	Port
1	EVCC	FLMD0	2	EVCC	PWRCTL
3	EVCC	PWRGD	4	EVCC	RESETZ

Table 8-7: Pin assignment of connector (CN7) P1

Pin	Power Domain	Port	Pin	Power Domain	Port
1	B0VCC	P1_0	2	B0VCC	P1_1
3	B0VCC	P1_2	4	B0VCC	P1_3
5	B0VCC	P1_4	6	B0VCC	P1_5
7			8		
9			10		
11			12		

Table 8-8: Pin assignment of connector (CN8) P11 / Analog Pins

Pin	Power Domain	Port	Pin	Power Domain	Port
1	A0VCC	P11_0	2	A0VCC	P11_1
3	A0VCC	P11_2	4	A0VCC	P11_3
5			6		
7			8		

Table 8-9: Pin assignment of connector (CN9) P16 / ISM Pins

Pin	Power Domain	Port	Pin	Power Domain	Port
1	ISMVCC	P16_0	**2**	ISMVCC	P16_1
3	ISMVCC	P16_2	**4**	ISMVCC	P16_3
5	ISMVCC	P16_4	**6**	ISMVCC	P16_5
7	ISMVCC	P16_6	**8**	ISMVCC	P16_7
9	ISMVCC	P16_8	**10**	ISMVCC	P16_9
11	ISMVCC	P16_10	**12**	ISMVCC	P16_11

Table 8-10: Pin assignment of connector (CN11) P17 / ISM Pins

Pin	Power Domain	Port	Pin	Power Domain	Port
1	ISMVCC	P17_0	**2**	ISMVCC	P17_1
3	ISMVCC	P17_2	**4**	ISMVCC	P17_3
5	ISMVCC	P17_4	**6**	ISMVCC	P17_5
7	ISMVCC	P17_6	**8**	ISMVCC	P17_7
9	ISMVCC	P17_8	**10**	ISMVCC	P17_9
11	ISMVCC	P17_10	**12**	ISMVCC	P17_11

Table 8-11: Pin assignment of connector (CN12) P3

Pin	Power Domain	Port	Pin	Power Domain	Port
1	B1VCC	P3_0	**2**	B1VCC	P3_1
3	B1VCC	P3_2	**4**	B1VCC	P3_3
5	B1VCC	P3_4	**6**	B1VCC	P3_5
7	B1VCC	P3_6	**8**	B1VCC	P3_7
9	B1VCC	P3_8	**10**	B1VCC	P3_9
11			**12**		
12			**14**		

9 Appendix

9.1 Components list

Item	Ref	Components name	Manufacturer
1	CN2,CN1	QTH-090-02-L-D-A	SAMETC
2	CN3	PREC005DFAN-RC	SULLINS
3	CN4,CN7,CN9,CN11	PREC006DFAN-RC	SULLINS
4	CN5	PREC003DFAN-RC	SULLINS
5	CN6	PREC002DFAN-RC	SULLINS
6	CN8	PREC004DFAN-RC	SULLINS
7	CN12	PREC007DFAN-RC	SULLINS
8	CN14	*0731310240	MOLEX
9	CN16,CN19	302-S401	On Shore
10	CN17	DF14A-20P-1.25H(55)	Hirose
11	CN20	NREC009SABC-M30RC	Sullins
12	C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C12,C13, C14,C15,C16,C17,C18,C19,C20,C21,C130,C166,	GRM21BB31C106KE15L 10u/16V/2012/B	Murata
13	C56,C57,C58,C59,C60,C62,C63,C64,C65,C66,C68, C69,C70,C71,C73,C74,C75,C76,C77,C78,C79,C85, C90,C100,C117,C118,C123,C124,C131,C132,C133, C134,C135,C136,C137,C138,C139,C140,C141,C142, C146,C147,C148,C149C150,C151,C153,C154,C155, C156,C157,C158,C159,C160,C161,C162,C163,C167, C168,C169,C170,C171,C172,C173,C174	GRM155B31C104KA87D 0.1u/16V/1005/B	Murata
14	C86,C87,C88,C89,	10p/50V/1005/B	Murata
15	C175,C176,C177,C178	0.22u/16V/1005/B	Murata
16	C166	10u/16V/2012/B	Murata
17	DSW1	218-4LPST	CTS
18	D1	HSU-83	RENESAS
19	L1	BLM18HE102SN1D	Murata
20	JP2,JP4,JP5,JP6,JP7,JP8,JP9,JP11,JP12,JP14,JP15, JP16,JP17,JP18,JP19,JP20,JP22,JP29,JP33,JP34, JP35,JP37,JP40,JP41	XJ8C-0211	OMRON
21	JP30,JP31,JP32,JP36,JP38,JP39	* XJ8C-0211	OMRON
22	RA8,RA9	CN1E4ATD103J	KOA
23	RA1,RA2,RA3,RA4,RA5,RA6,RA7	CN1E4ATD330J	KOA
24	R44,R71,R72,R73,R74,R76,R80	0ohm/1005/1%	KOA
25	R38,R39,R40,R41,R42,R61	*0ohm/1005/1%	KOA
26	R8,R9,R10,R11,R12,R45,R46,R47,R48,R49,R50, R51,R52,R53,R54,R55,R59,R60,R79,R82	4.7K/1005/1%	KOA
27	R83,R84,R85,R86,R87,R88,R89,R90,R91,R92,R93,R94, R95,R96,R97,R98,R99R100,R102,R103,R111,R104, R105,R106,R107,R108,R109,R110,R112,R113,R114	33ohm/1608/1%	KOA
28	R101,	22ohm/1608/1%	KOA
29	R26,R27	22ohm/1005/1%	KOA
30	R81	10K/1005/1%	KOA
31	TP1,TP2,TP3,TP4	HK-5-G-Black	MAC8
32	U1	RH850/D1M1A	RENESAS
33	U2	MX66L1G85G	MACRONIX
34	U3	MT29F4G08ABADAWP-IT	Micron
35	U4,U11,U12,U14,	IDTQS3VH16233PAG8	IDT
36	U5	MX65L12A64AA	MACRONIX
37	UM3,UM4	MT48LC16M16A2P-6A	Micron
38	U13,U15	FSA4159P6X	FAIRCHILD
39	X1	NC-206 32.768KHz	KYUSHU DENTSU
40	X2	7A-8.000MAAE-T	TXC
41	Y1	*1-390261-2	TE

9.2 Schematics of the D1x Mango D1M1A Adapter Board

The following pages contain the full schematics of the Mango D1M1A Adapter Board. For the schematics of the Main Board, please see the dedicated Main Board manual.

RH850 D1M1A Adapter Board Rev1.2

Revision History

DATE	Rev	Page	DESCRIPTION
2016.10.05	1.0		Release version
2016.12.15	1.1		Repeat version
2017.6.2	1.2		change FLMD0,PWRCTL

Note

*All resistors 1% accuracy

*For more information check the bill of materials

*GND guard *Equal-length wiring *Impedance *No Mount

NetList Result
253 Parts, 32 Library Parts, 526 Nets, 1643 Pins

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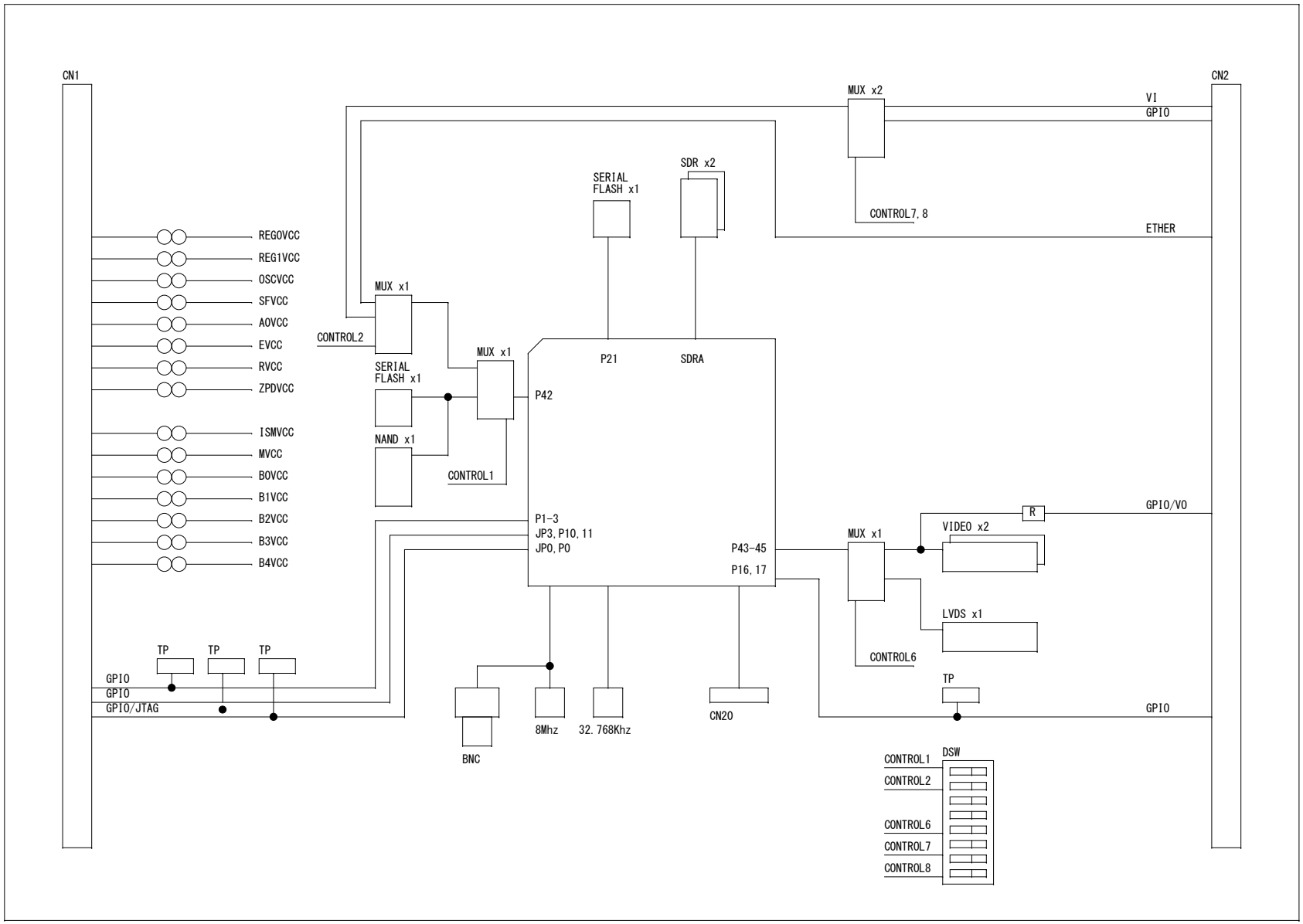
Title: RH850 D1M1A Adapter Board		
Size: A2	Document Number: 261001001	Rev: 1.2
Date: Friday, June 02, 2017	Sheet 1 of 8	



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Size: A2	Document Number: 2610001001	Rev: 1.0
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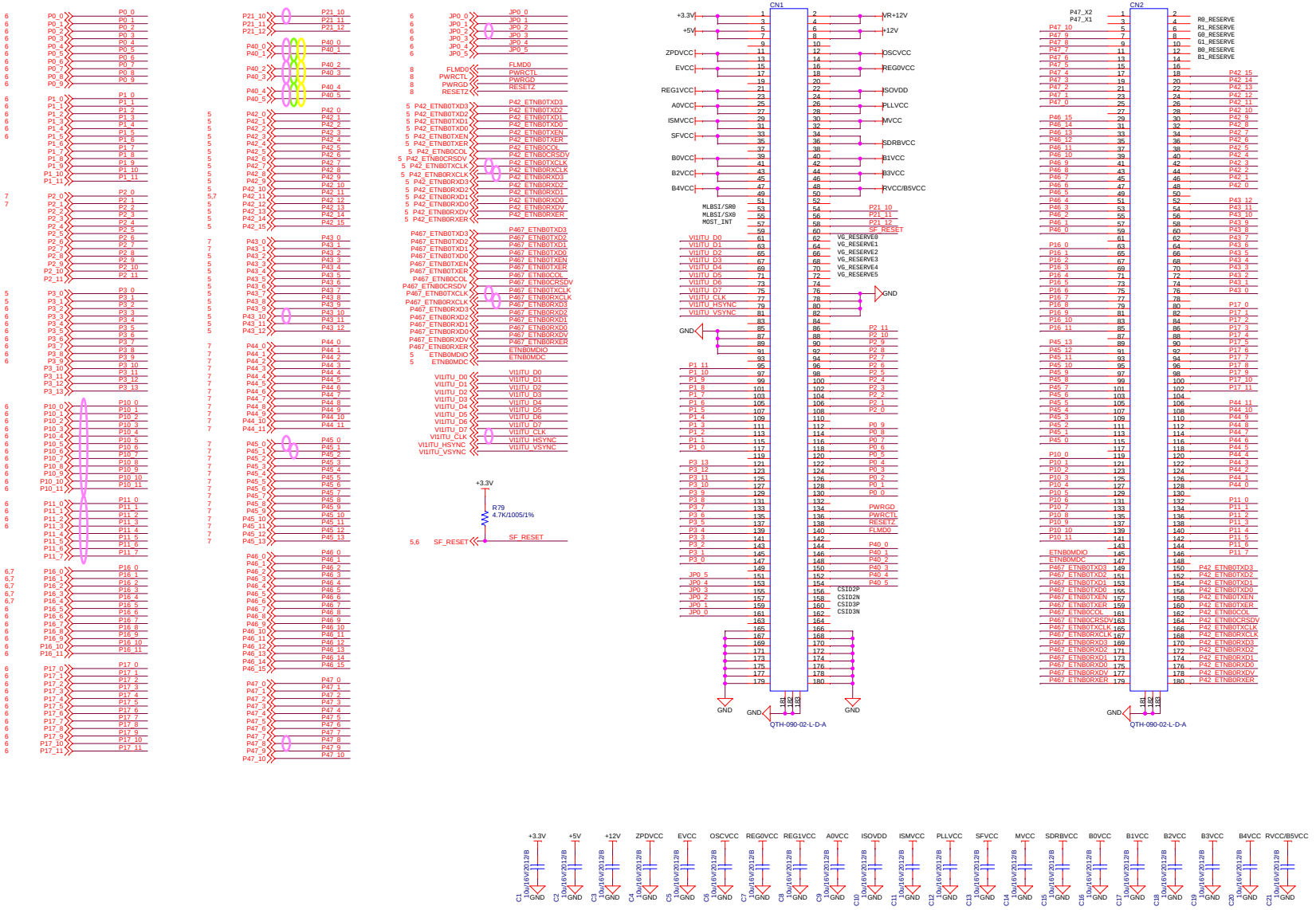

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	CONNECTOR
Size	A2
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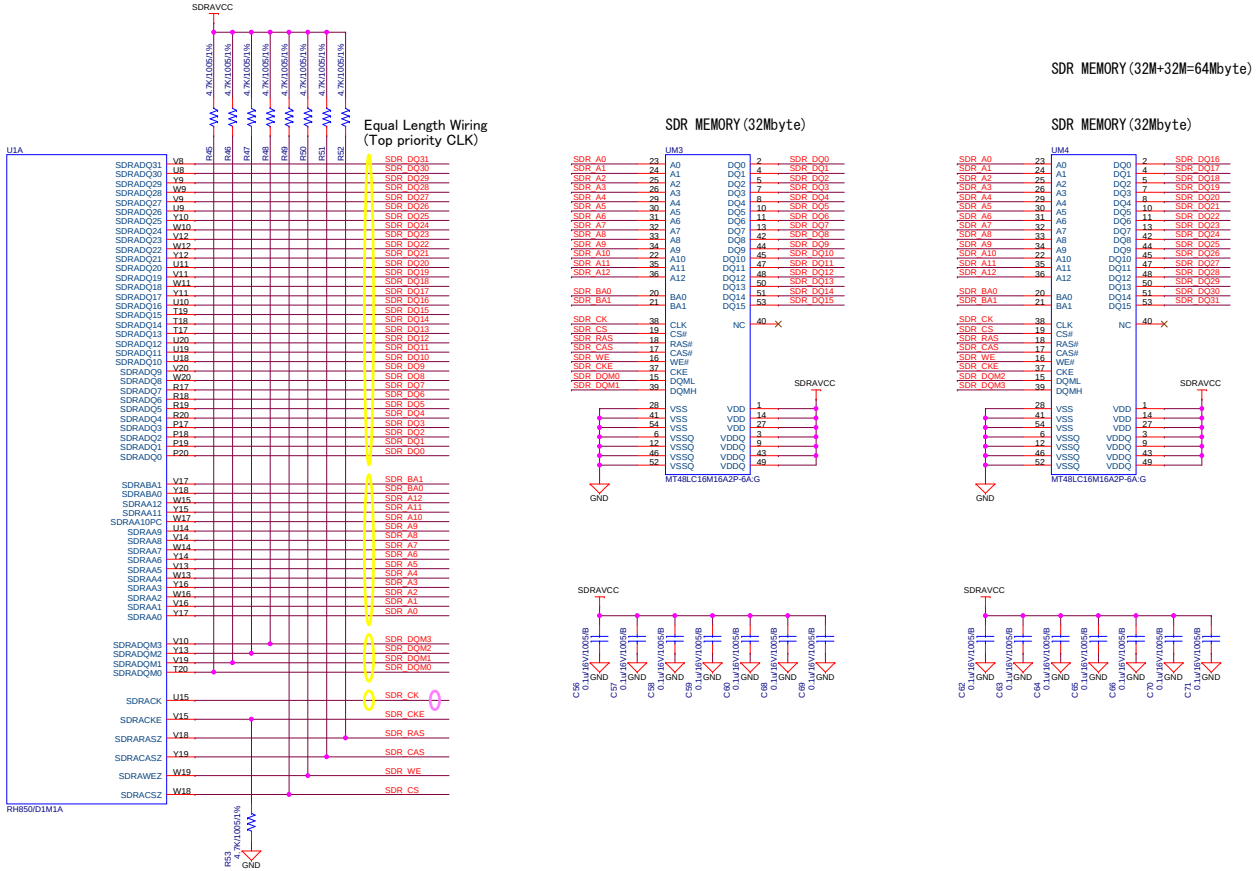

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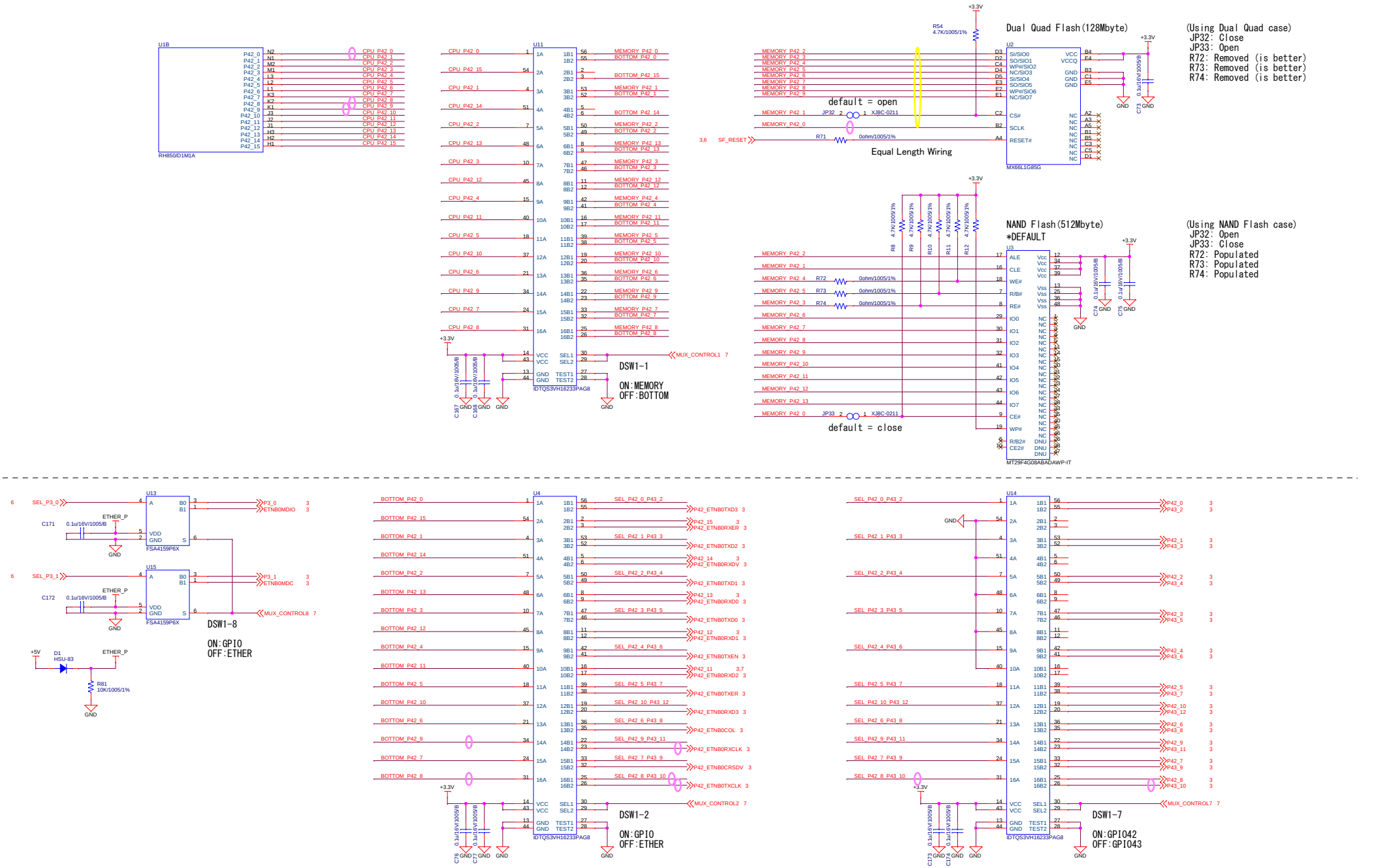

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Size	A2
Document Number	2610001001
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Date:	Friday, June 02, 2017
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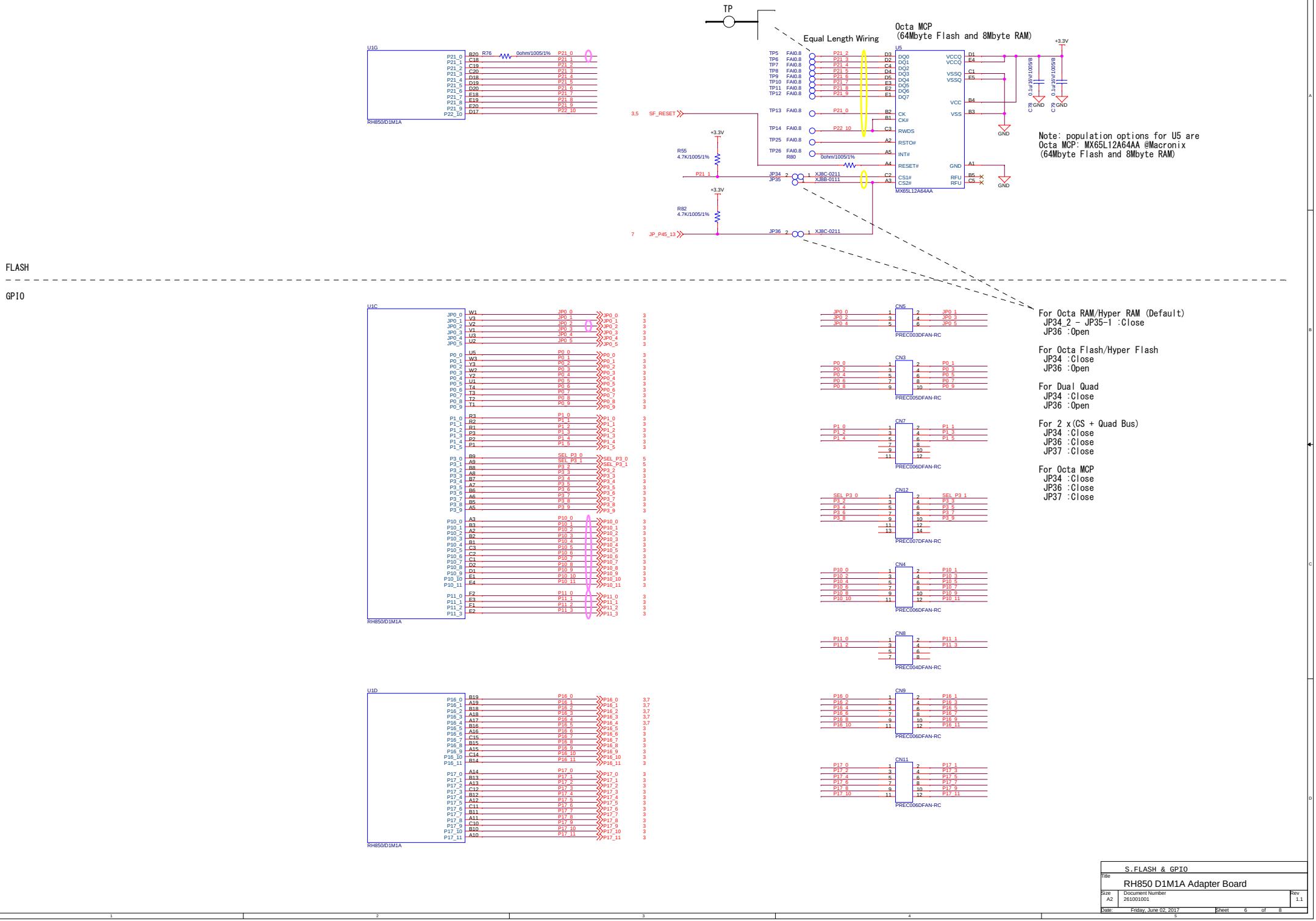

S.FLASH & GPIO			
Title	RH850 D1M1A Adapter Board		
Size A2	Document Number 2610001001		Rev 1.1
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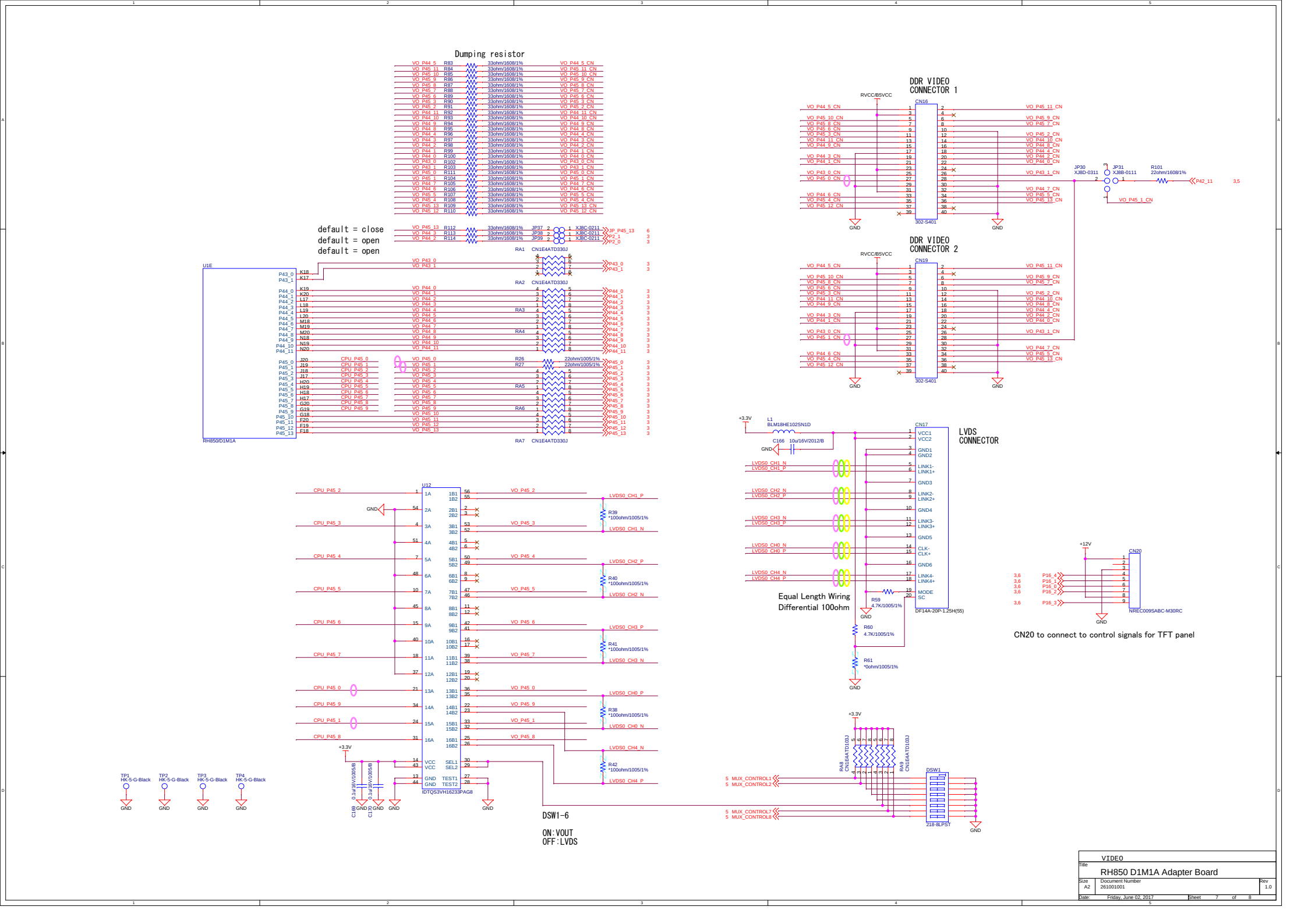
Dumping resistor
default = close
default = open
default = open
DDR VIDEO CONNECTOR 1
DDR VIDEO CONNECTOR 2
LVDS CONNECTOR
Equal Length Wiring
Differential 100ohm
CN20 to connect to control signals for TFT panel
DSW1-6
ON:VOUT
OFF:LVDS
VIDEO
RH850 D1M1A Adapter Board
Document Number 2610001001
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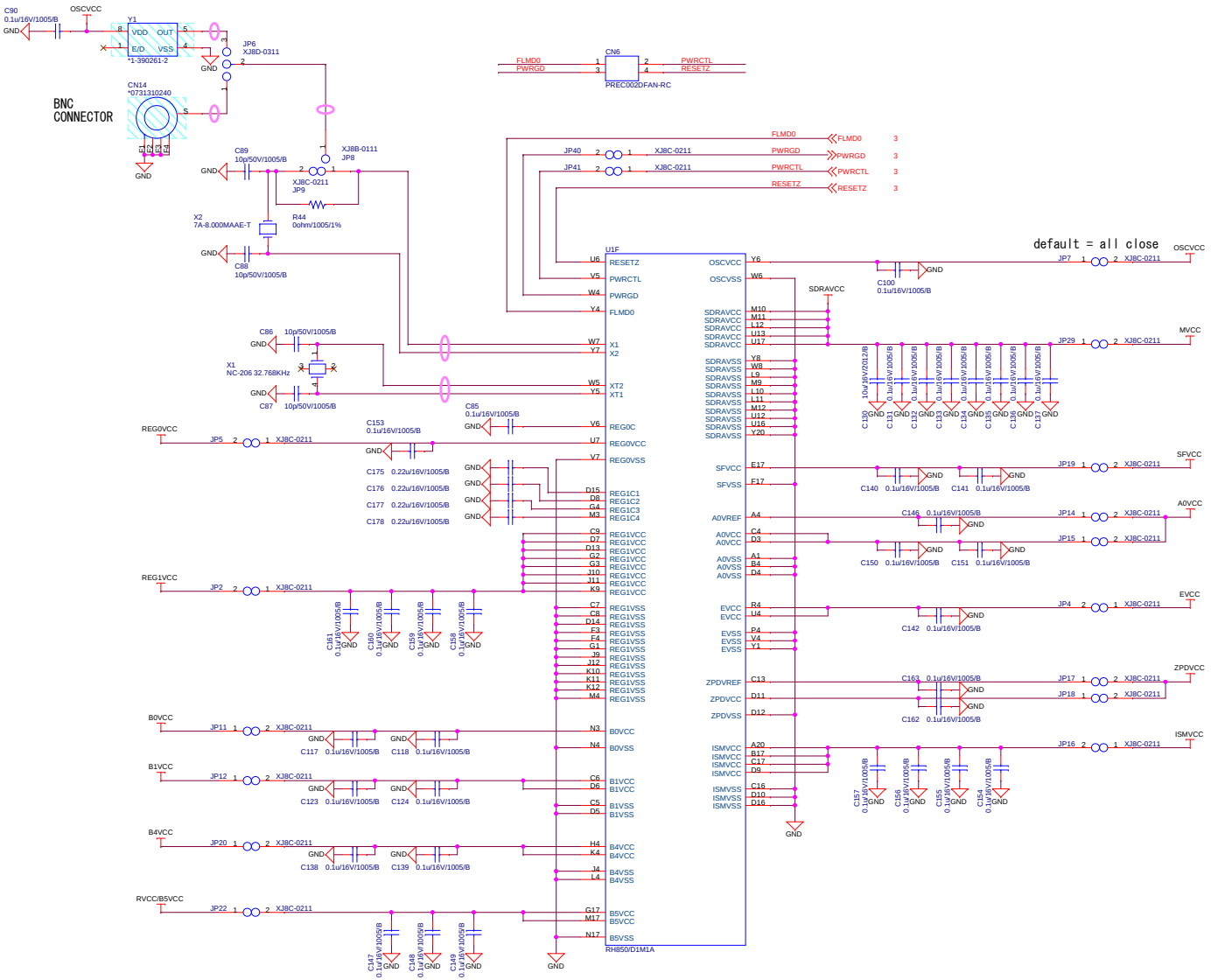

	POWER		
Title	RH850 D1M1A Adapter Board		
Size A2	Document Number 2610001001		Rev 1.2
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10 Revision history

Rev.	Release date	Revised contents	
		Page	Subject
Rev.0.01	2017-Jan-25		Draft version
Rev.0.02	2017-Jun-06		Schematics update

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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