Application Note

32

Application Board Default Settings

RH850/D1x

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Table of Contents

Chapter 1 Introduction

This document is intended to provide D1x specific information on the device usage. It should be used in conjunction with the appropriate D1x Users Manual and – if available - Operating Precautions Document (OPC).

This document provides information about the default jumper settings of the following application boards:

- RH850/D1x main board Y-RH850-D1X-MB-T1-V1
- Y-RH850-D1M2H-PB-TET-V1
- Y-RH850-D1M2H-PB-TET-V2
  (use same settings as for Y-RH850-D1M2H-PB-TET-V1)
- Y-RH850-D1M2H-PB-DEV-V1
  (to be included in a later version of this document)

Chapter 2 Reference Documents

This chapter contains information about the application board documentation.

2.1 Y-RH850-D1X-MB-T1-V1

RH850/D1x main board Y-RH850-D1X-MB-T1-V1,
board imprint "SBEV-RH850-MAIN".

The latest version of the Main Board Users Manual is
AIB3-H-14-0052 Rev. 0.05 (Preliminary)

2.2 Y-RH850-D1M2H-PB-DEV-V1

RH850/D1M2H adapter board with direct Device assembly.
Board imprint "SBEV-RH850-D1M2H".

The latest version of the Adapter Board Users Manual is
AIB3-H-14-0053 Rev. 0.05 (Preliminary)

2.3 Y-RH850-D1M2H-PB-TET-V1

RH850/D1M2H adapter board with TET BS socket and mount adapter.
For use with device and emulator.
Board imprint "SBEV-RH850-D1M2H".

The latest version of the Adapter Board Users Manual is
AIB3-H-14-0053 Rev. 0.05 (Preliminary)

2.4 Y-RH850-D1M2H-PB-TET-V2

RH850/D1M2H adapter board with TET BS socket, no mount adapter.
For use with emulator.
Board imprint "SBEV-RH850-D1M2H".

The latest version of the Adapter Board Users Manual is
AIB3-H-14-0053 Rev. 0.05 (Preliminary)

Please contact your Renesas sales representative for a copy of the above mentioned manuals.

Chapter 3 Default Settings

This Chapter shows the default configurations of jumpers and DIP switches of the D1x application boards as they are configured when delivered form Renesas.

3.1 Default Settings of Y-RH850-D1X-MB-T1-V1 (RH850/D1x main board)

The following table lists all available jumpers and switches and their default position for the first start-up.

Table 3-1: Default positions of jumpers and switches on Y-RH850-D1X-MB-T1-V1 (RH850/D1x main board)

Part No.	Description	Default Position
JP1	REG1VCC	3-4
JP2	PLLVCC	3-4
JP3	B5VCC/RVCC	3-4
JP4	B0VCC	3-4
JP5	B1VCC	3-4
JP6	B2VCC	3-4
JP7	B3VCC	3-4
JP8	B4VCC	3-4
JP9	ISMVCC	1-2
JP10	MVCC	2-3 (Note1)
JP11	REG0VCC	1-2
JP12	OSCVCC	3-4
JP13	ZPDVCC	5-6
JP14	EVCC	1-2
JP15	SFVCC	3-4 (Note2)
JP16	A0VCC	3-4
JP90	VO0/LCBI DataEnable	open
JP91	VO0 Select Data Enable 2	2-3
JP92	VO0/ZIF DataEnable	open
JP93	VO0/ZIF PWM	open
JP94	VO0/ZIF GPIO0	open
JP95	VO0/ZIF I2C	open
JP96	VO0/HDMI DataEnable	open
JP97	VO0/HDMI I2C	open
JP74	VO1/VI1 DataEnable	open
JP75	VO1 Select Data Enable 2	2-3
JP76	VO1/ZIF DataEnable	open
JP77	VO1/ZIF PWM	open

Part No.	Description	Default Position
JP78	VO1/ZIF GPIO0	open
JP79	VO1/ZIF I2C	open
JP80	VO1/HDMI DataEnable	open
JP81	VO1/HDMI I2C	open
JP64	VI0 Data Enable	open
JP65	VI0 Data Enable	open
JP66	VI0/ZIF Data Enable	open
JP67	VI0/ZIF PWM	open
JP68	VI0/ZIF GPIO	open
JP69	VI0/ZIF I2C	open
JP106	VI0 Select B4	2-3
DSW30	CVBS Data Mux	open
JP104	I2C1 Enable	open
JP105	I2C0 Enable	open
JP70	SEL_TCON0_1	1-2
JP71	SEL_TCON0_4	1-2
JP72	SEL_TCON0_5	1-2
JP73	SEL_TCON0_6	1-2
JP82/83	VO1 Select Data Enable 1	JP83-1 - JP82-2
JP84	SEL_VIO1_0	2-3
JP85	SEL_VIO1_1	2-3
JP86	SEL_VIO1_2	2-3
JP87	SEL_VIO1_3	2-3
JP88	SEL_VIO1_4	2-3
JP89	SEL_VIO1_5	2-3
JP98/99	VO0 Select Data Enable 1	JP98 2-3
DSW1	PU12	all open
DSW2	PU14	all open

Part No.	Description	Default Position
DSW3	PD12	all open
DSW4	PD14	all open
DSW5	PU15	all open
DSW6	PD15	all open
DSW7	PU09	all open
DSW8	PU11	all open
DSW9	PD09	all open
DSW10	PD11	all open
DSW11	PU10	all open
DSW12	PD10	all open
DSW13	PU05	all open
DSW14	PU07	all open
DSW15	PD05	all open
DSW16	PD07	all open
DSW17	PU06	all open
DSW18	PU08	all open
DSW19	PD06	all open
DSW20	PD08	all open
DSW21	PU01	all open
DSW22	PU03	all open
DSW23	PD01	all open
DSW24	PD03	all open
DSW25	PU02	all open
DSW26	PU04	all open
DSW27	PD02	all open
DSW28	PD04	all open
SW1	DCURDY	open
SW2	DCUTMS	PU
SW3	DCUTDI	PU
SW5	DCUTDO	open
SW7	DCURST	PD
SW9	DCUTCK	open
SW4	MODE0	open
SW8	MODE1	open
SW6	FLMD1	PD
SW10	FLMD0	PD
JP18	Debugger FLMD0	open
JP19	Debugger Reset	closed
JP20	Enable Reset Switch	closed
JP21	MOST I2C	open
JP43	Ethernet 0 Clock Select	2-3
JP44	Ethernet 1 Clock Select	2-3
JP100	ISO+5V PWRGD Select	closed
JP101	ISO+3.3V PWRGD Select	closed

Part No.	Description	Default Position
JP102	SDRBVCC PWRGD Select	closed
JP103	ISOVDD PWRGD Select	closed
JP56	SEL_SSIFACK	1-2
JP57	SEL_SSIFSCK 0	1-2
JP58	SEL_SSIFSCK 1	open
JP59	SEL_SSIFWS 0	1-2
JP60	SEL_SSIFWS 1	open
JP61	SEL_SSIFTXD 2	open
JP62	SEL_SSIFTXD 0	2-3
JP63	SEL_SSIFTXD 1	1-2
JP47	SSIF I2C	open
JP45	Left Speaker Source	3-5/4-6
JP46	Right Speaker Source	3-5/4-6
JP48	Left AN	1-2
JP49	Left BP	closed
JP50	Left AP	1-2
JP51	Left BN	closed
JP52	Right AN	1-2
JP53	Right BP	closed
JP54	Right AP	1-2
JP55	Right BN	closed
JP32	FT#0 Mode Select	1-2
JP33	FT#2 Mode Select	1-2
JP34	FT#2 Source Select	1-2
JP35	FT#2 Source Select	1-2
JP36	FT#2 Mux	1-2/3-4
JP37	FT#1 Mode Select	1-2
JP38	FT#3 Mode Select	2-3
JP39	FT#1 Source Select	1-2
JP40	FT#1 Source Select	1-2
JP41	FT#3 Mux	closed
JP42	FT#3 Mux	closed
JP22	RS232/LIN Mux	2-3
JP23	LIN Power	2-3
JP24	LIN Master Select	open
JP25	LIN Termination	2-3
JP26	LIN Wake EN	open
JP27	LIN SLP EN	open
JP28	CAN Split	open
JP29	CAN Termination	open
JP30	CAN Mux	2-3
JP31	CAN Termination	open
DSW29	HMI Select	all open

Part No.	Description	Default Position
DSW31	MUX Select	
.8	VO0MUX_SEL1	ON (Low)
.7	VO0MUX_SEL2	ON (Low)
.6	VO1MUX_SEL1	ON (Low)
.5	VO2MUX_SEL2	ON (Low)
.4	VINMUX_SEL	ON (Low)
.3	AUDIOMUX_SEL	OFF (High)
.2	N.C.	OFF
.1	N.C.	OFF

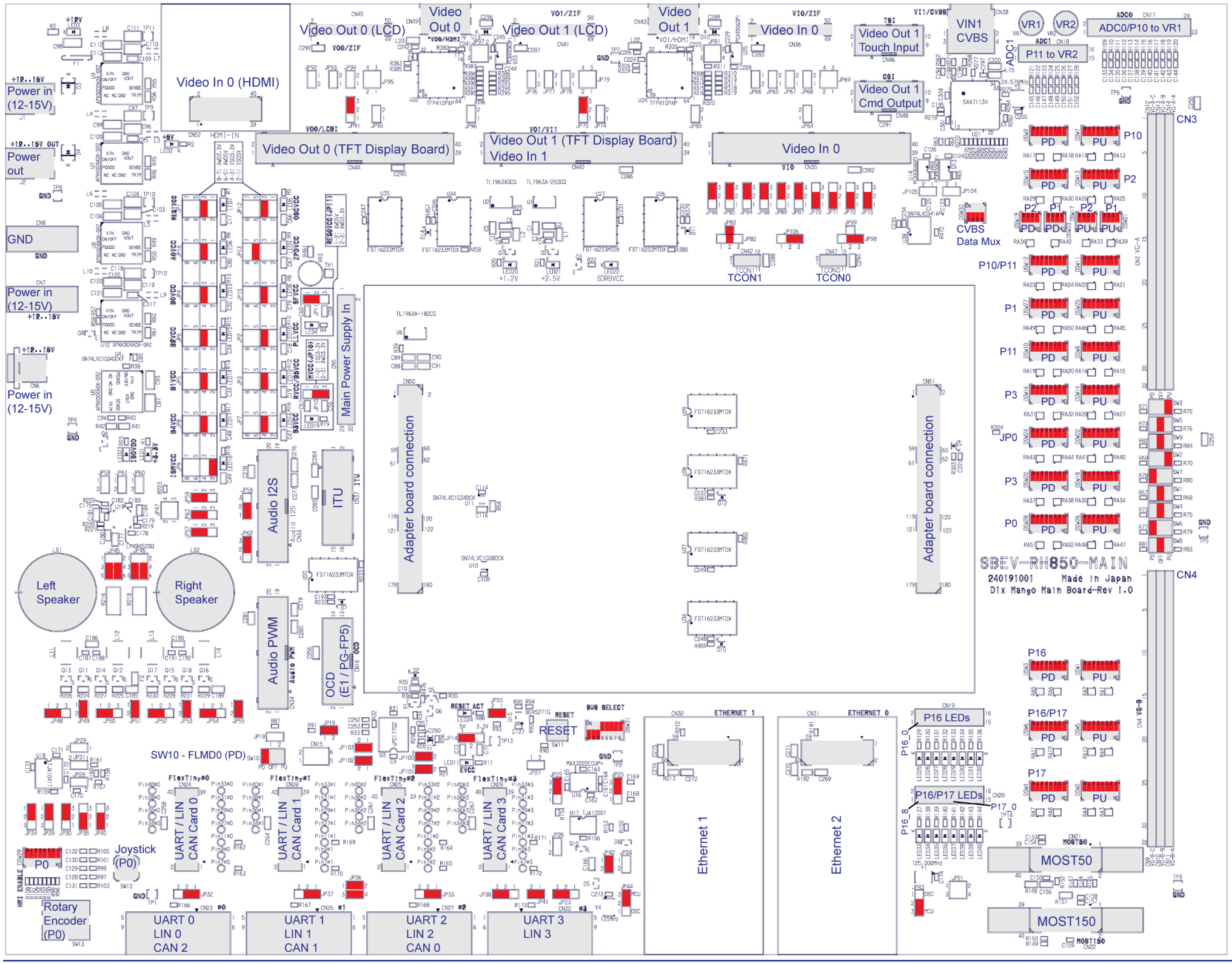
Note1: JP10: 2-3 (MVCC = AWO 3V3), Note: Board version V1.0 has JP10: 1-3 (MVCC = ISO 3V3)

Note2: JP15: 3-4 (SFVCC = ISO 3V3), Note: Board version V1.0 has JP15: 7-8 (SFVCC = AWO 3V3)

The following schematic shows all available jumpers and switches on Y-RH850-D1X-MB-T1-V1 (RH850/D1x main board) and their default position for the first start-up.

Next Page:

Figure 1: Default positions of jumpers and switches on Y-RH850-D1X-MB-T1-V1 (RH850/D1x main board) - Red block indicates position of Jumper or DIP-Switch



SW3 - DCUTDI (PU)
SW5 - DCUTDO (open)
SW9 - DCUTCK (open)
SW2 - DCUTMS (PU)
SW7 - DCURST (PD)
SW1 - DCURDZ (open)
SW4 - MODE0 (open)
SW6 - FLMD1 (PD)
SW8 - MODE1 (open)

3.2 Default Settings of Y-RH850-D1M2H-PB-TET-V1 (RH850/D1M2H adapter board with TET BS socket)

Table 3-2: Default positions of jumpers and switches on Y-RH850-D1M2H-PB-TET-V1 (RH850/D1M2H adapter board with TET BS socket)

Part No.	Description	Default Position
JP25	Current Meas SDRBVCC	closed
JP1	Current Meas PLLVCC	closed
JP2	Current Meas REG1VCC	closed
JP3	Current Meas ISOVDD	closed
JP4	Current Meas EVCC	closed
JP5	Current Meas REG0VCC	closed
JP7	Current Meas OSCVCC	closed
JP6	Main-Oscillator Mux	open
JP8/9	Main-Crystal Mux	open
JP10	Main Crystal	N/A
JP24	Sub Crystal	N/A
JP11	Current Meas B0VCC	closed
JP12	Current Meas B1VCC	closed
DSW1	Encoding Address Enable	closed
DSW2	Bus Select	closed (all LOW)
JP13	Current Meas MVCC	closed
JP14	A0VREF	closed
JP15	Current Meas A0VCC	closed
JP16	Current Meas ISMVCC	closed
JP17	ZPDVREF	2-3
JP18	Current Meas ZPDVCC	closed
JP19	Current Meas SFVCC	closed
JP20	Current Meas B4VCC	closed
JP21	Current Meas B3VCC	closed
JP22	Current Meas B5VCC/RVCC	closed
JP23	Current Meas B2VCC	closed

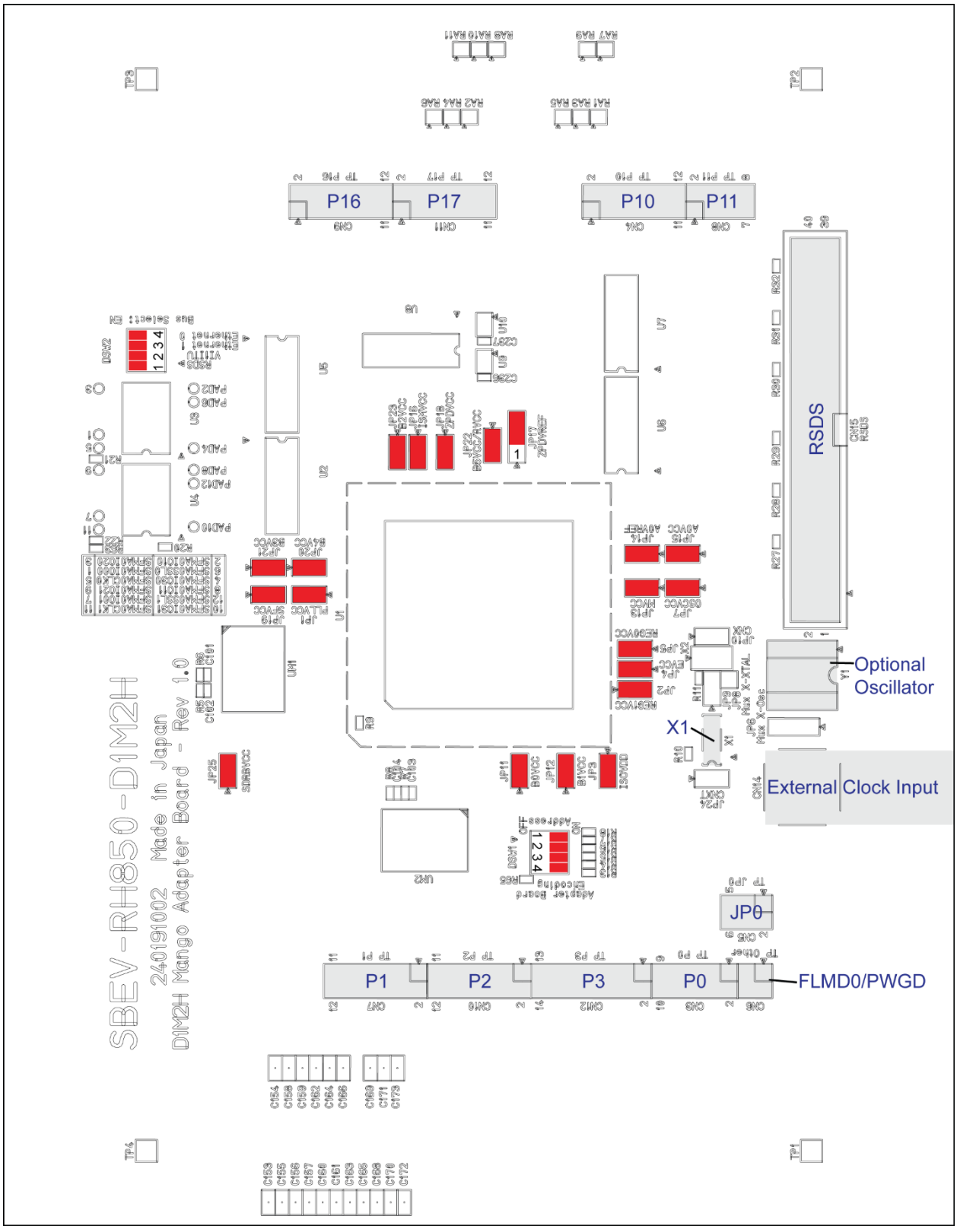


Figure 2: Default positions of jumpers and switches on Y-RH850-D1M2H-PB-TET-V1 (RH850/D1M2H adapter board with TET BS socket) - Red block indicates position of Jumper or DIP-Switch

Chapter 4 Alternative Settings

This Chapter shows an alternative configuration of jumpers and DIP switches of the D1x application.

4.1 Alternative Settings of Y-RH850-D1X-MB-T1-V1 (RH850/D1x main board)

The following table lists all available jumpers and switches and their position for an alternative configuration.

Table 4-1: Alternative positions of jumpers and switches on Y-RH850-D1X-MB-T1-V1 (RH850/D1x main board)

Part No.	Description	Alternative Position
JP1	REG1VCC	3-4
JP2	PLLVCC	3-4
JP3	B5VCC/RVCC	3-4
JP4	B0VCC	3-4
JP5	B1VCC	3-4
JP6	B2VCC	3-4
JP7	B3VCC	3-4
JP8	B4VCC	3-4
JP9	ISMVCC	1-2
JP10	MVCC	2-3 (Note1)
JP11	REG0VCC	1-2
JP12	OSCVCC	3-4
JP13	ZPDVCC	5-6
JP14	EVCC	1-2
JP15	SFVCC	3-4 (Note2)
JP16	A0VCC	3-4
JP90	VO0/LCBI DataEnable	open
JP91	VO0 Select Data Enable 2	2-3
JP92	VO0/ZIF DataEnable	open
JP93	VO0/ZIF PWM	open
JP94	VO0/ZIF GPIO0	open
JP95	VO0/ZIF I2C	open
JP96	VO0/HDMI DataEnable	open
JP97	VO0/HDMI I2C	open
JP74	VO1/VI1 DataEnable	open
JP75	VO1 Select Data Enable 2	2-3
JP76	VO1/ZIF DataEnable	open
JP77	VO1/ZIF PWM	open

Part No.	Description	Alternative Position
JP78	VO1/ZIF GPIO0	open
JP79	VO1/ZIF I2C	open
JP80	VO1/HDMI DataEnable	open
JP81	VO1/HDMI I2C	open
JP64	VI0 Data Enable	open
JP65	VI0 Data Enable	open
JP66	VI0/ZIF Data Enable	open
JP67	VI0/ZIF PWM	open
JP68	VI0/ZIF GPIO	open
JP69	VI0/ZIF I2C	open
JP106	VI0 Select B4	2-3
DSW30	CVBS Data Mux	open
JP104	I2C1 Enable	open
JP105	I2C0 Enable	open
JP70	SEL_TCON0_1	1-2
JP71	SEL_TCON0_4	1-2
JP72	SEL_TCON0_5	1-2
JP73	SEL_TCON0_6	1-2
JP82/83	VO1 Select Data Enable 1	JP83-1 - JP82-2
JP84	SEL_VIO1_0	2-3
JP85	SEL_VIO1_1	2-3
JP86	SEL_VIO1_2	2-3
JP87	SEL_VIO1_3	2-3
JP88	SEL_VIO1_4	2-3
JP89	SEL_VIO1_5	2-3
JP98/99	VO0 Select Data Enable 1	JP98 2-3
DSW1	PU12	all open
DSW2	PU14	all open

Part No.	Description	Alternative Position
DSW3	PD12	all open
DSW4	PD14	all open
DSW5	PU15	all open
DSW6	PD15	all open
DSW7	PU09	all open
DSW8	PU11	all open
DSW9	PD09	all open
DSW10	PD11	all open
DSW11	PU10	all open
DSW12	PD10	all open
DSW13	PU05	all open
DSW14	PU07	all open
DSW15	PD05	all open
DSW16	PD07	all open
DSW17	PU06	all open
DSW18	PU08	all open
DSW19	PD06	all open
DSW20	PD08	all open
DSW21	PU01	all open
DSW22	PU03	all open
DSW23	PD01	all open
DSW24	PD03	all open
DSW25	PU02	all open
DSW26	PU04	all open
DSW27	PD02	all open
DSW28	PD04	all open
SW1	DCURDY	open
SW2	DCUTMS	PU
SW3	DCUTDI	PU
SW5	DCUTDO	open
SW7	DCURST	PD
SW9	DCUTCK	open
SW4	MODE0	open
SW8	MODE1	open
SW6	FLMD1	PD
SW10	FLMD0	PD
JP18	Debugger FLMD0	open
JP19	Debugger Reset	closed
JP20	Enable Reset Switch	closed
JP21	MOST I2C	open
JP43	Ethernet 0 Clock Select	2-3
JP44	Ethernet 1 Clock Select	2-3
JP100	ISO+5V PWRGD Select	closed
JP101	ISO+3.3V PWRGD Select	closed

Part No.	Description	Alternative Position
JP102	SDRBVCC PWRGD Select	closed
JP103	ISOVDD PWRGD Select	closed
JP56	SEL_SSIFACK	1-2
JP57	SEL_SSIFSCK 0	1-2
JP58	SEL_SSIFSCK 1	open
JP59	SEL_SSIFWS 0	1-2
JP60	SEL_SSIFWS 1	open
JP61	SEL_SSIFTXD 2	open
JP62	SEL_SSIFTXD 0	2-3
JP63	SEL_SSIFTXD 1	1-2
JP47	SSIF I2C	open
JP45	Left Speaker Source	3-5/4-6
JP46	Right Speaker Source	3-5/4-6
JP48	Left AN	1-2
JP49	Left BP	closed
JP50	Left AP	1-2
JP51	Left BN	closed
JP52	Right AN	1-2
JP53	Right BP	closed
JP54	Right AP	1-2
JP55	Right BN	closed
JP32	FT#0 Mode Select	1-2
JP33	FT#2 Mode Select	1-2
JP34	FT#2 Source Select	1-2
JP35	FT#2 Source Select	1-2
JP36	FT#2 Mux	1-2/3-4
JP37	FT#1 Mode Select	1-2
JP38	FT#3 Mode Select	2-3
JP39	FT#1 Source Select	1-2
JP40	FT#1 Source Select	1-2
JP41	FT#3 Mux	closed
JP42	FT#3 Mux	closed
JP22	RS232/LIN Mux	2-3
JP23	LIN Power	2-3
JP24	LIN Master Select	open
JP25	LIN Termination	2-3
JP26	LIN Wake EN	open
JP27	LIN SLP EN	open
JP28	CAN Split	open
JP29	CAN Termination	open
JP30	CAN Mux	2-3
JP31	CAN Termination	open
DSW29	HMI Select	all open

Part No.	Description	Alternative Position
DSW31	MUX Select	
.8	VO0MUX_SEL1	ON (Low)
.7	VO0MUX_SEL2	ON (Low)
.6	VO1MUX_SEL1	ON (Low)
.5	VO2MUX_SEL2	ON (Low)
.4	VINMUX_SEL	ON (Low)
.3	AUDIOMUX_SEL	OFF (High)
.2	N.C.	OFF
.1	N.C.	OFF

Note1: JP10: 2-3 (MVCC = AWO 3V3), Note: Board version V1.0 has JP10: 1-3 (MVCC = ISO 3V3)

Note2: JP15: 3-4 (SFVCC = ISO 3V3), Note: Board version V1.0 has JP15: 7-8 (SFVCC = AWO 3V3)

4.2 Pin assignment of CN3 and CN4 of Y-RH850-D1X-MB-T1-V1 (RH850/D1x main board) for alternative configuration

The following table lists the pin assignment of CN3 and CN4 (main board) for alternative configuration. To set this configuration set DSW31.4, DSW31.6 and DSW31.8 to off position.

Table 4-2: CN3 (main board) pin assignment for alternative configuration (changes compared to default settings in **green**)

	A	B	C
1	GND	P2_0	P10_0
2	5V	P2_1	P10_1
3	5V	P2_2	P10_2
4	n.c	P2_3	
5	P1_0	P2_4	RESETZ
6	P1_1	P2_5	+12V
7	P1_2	P2_6	P10_4
8	P1_3	P2_7	P10_5
9	P1_4	P2_8	P10_6
10	P1_5	P2_9	P10_7
11	P1_6	P2_10	P10_8
12	P1_7	P2_11	P10_9
13	P1_8		P10_10
14	P1_9		P10_11
15	P1_10		P11_0
16	P1_11		P11_1
17	JP0_0	P3_0	P11_2
18	JP0_1	P3_1	P11_3
19	JP0_2	P3_2	P11_4
20	JP0_3	P3_3	P11_5
21	JP0_4	P3_4	P11_6
22	JP0_5	P3_5	P11_7
23	P0_0	P3_6	
24	P0_1	P3_7	
25	P0_2	P3_8	
26	P0_3	P3_9	
27	P0_4	P3_10	
28	P0_5	P3_11	
29	P0_6	P3_12	
30	P0_7	P3_13	
31	P0_8		
32	P0_9		

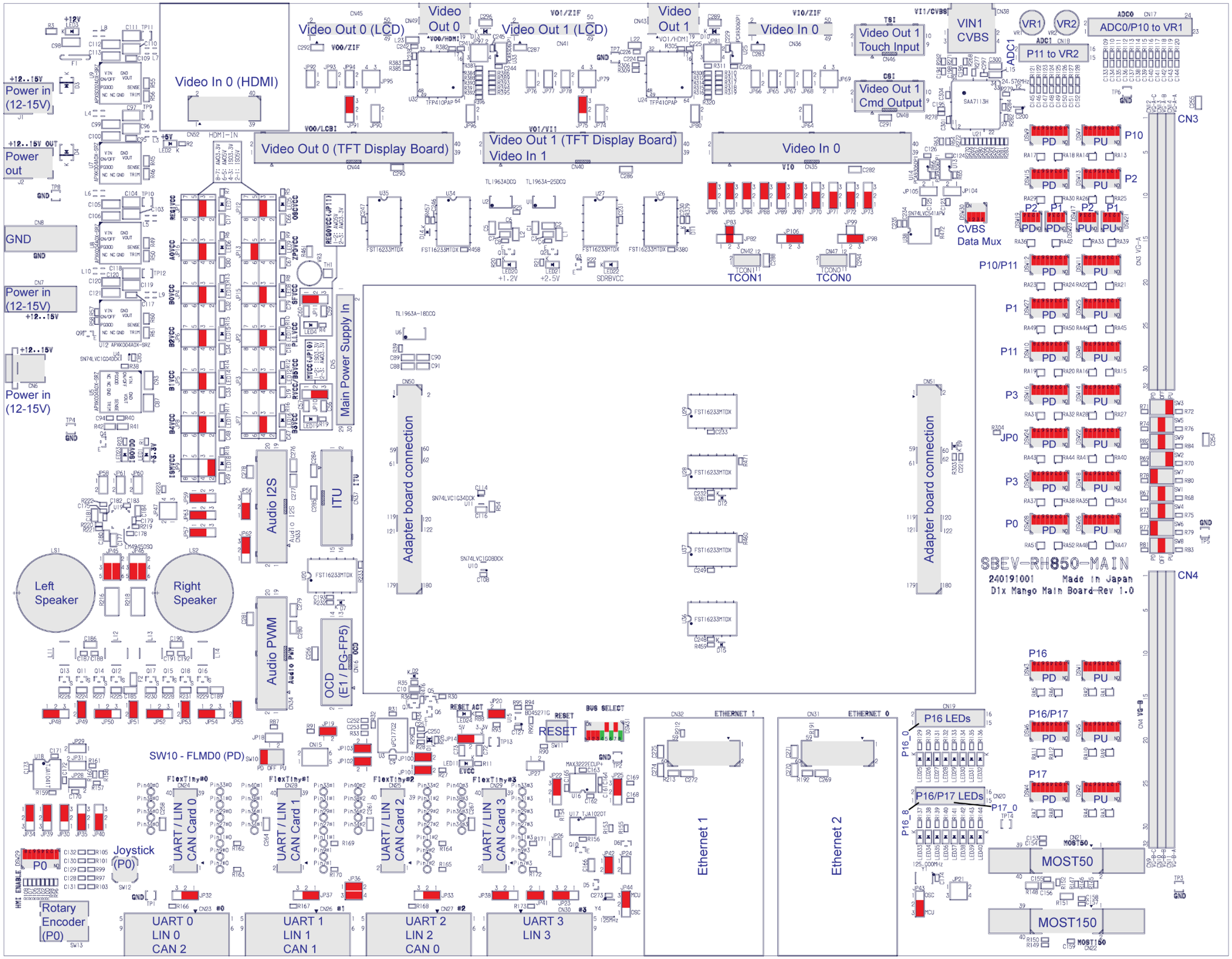
Table 4-3: CN4 (main board) pin assignment for alternative configuration
(changes compared to default settings in **green**)

	A	B	C
1		P43_0	P45_13
2		P43_2	P46_0
3		P43_1	P46_1
4		P43_3	P46_2
5		P43_4	P46_3
6		P43_5	P46_4
7	P16_0	P43_6	P46_5
8	P16_1	P44_0	P46_6
9	P16_2	P44_1	P46_7
10	P16_3	P44_2	P46_8
11	P16_4	P44_3	P46_9
12	P16_5	P44_4	P46_10
13	P16_6	P44_5	P46_11
14	P16_7	P44_6	P46_12
15	P16_8	P44_7	P46_13
16	P16_9	P44_8	P46_14
17	P16_10	P44_9	P46_15
18	P16_11	P44_10	P47_0
19	P17_0	P44_11	P47_1
20	P17_1	P45_0	P47_2
21	P17_2	P45_1	P47_3
22	P17_3	P45_2	P47_4
23	P17_4	P45_3	P47_5
24	P17_5	P45_4	P47_6
25	P17_6	P45_5	P47_7
26	P17_7	P45_6	P47_8
27	P17_8	P45_7	P47_9
28	P17_9	P45_8	P47_10
29	P17_10	P45_9	
30	P17_11	P45_10	
31		P45_11	P47_X1
32		P45_12	P47_X2

The following schematic shows all available jumpers and switches on Y-RH850-D1X-MB-T1-V1 (RH850/D1x main board) and their position for the alternative set-up.

Next Page:

Figure 3: Alternative positions of jumpers and switches on Y-RH850-D1X-MB-T1-V1 (RH850/D1x main board) - Red block indicates position of Jumper or DIP-Switch


Video In 0 (HDMI)
Video Out 0 (LCD)
Video Out 0
Video Out 1 (LCD)
Video Out 1
Video In 0
Video Out 1 Touch Input
Video Out 1 Cmd Output
VIN1 CVBS
ADC0/P10 to VR1
P11 to VR2
Video Out 0 (TFT Display Board)
Video Out 1 (TFT Display Board) Video In 1
Video In 0
Power in (12-15V)
Power out
GND
Main Power Supply In
Audio I2S
ITU
Audio PWM
OCD (E1 / PG-FP5)
Adapter board connection
Left Speaker
Right Speaker
SW10 - FLMD0 (PD)
Joystick (P0)
Rotary Encoder (P0)
UART / LIN CAN Card 0
UART / LIN CAN Card 1
UART / LIN CAN Card 2
UART / LIN CAN Card 3
UART 0 LIN 0 CAN 2
UART 1 LIN 1 CAN 1
UART 2 LIN 2 CAN 0
UART 3 LIN 3
RESET
BUS SELECT
Ethernet 1
Ethernet 2
CVBS Data Mux
TCON1
TCON0
P10
P2
P10/P11
P1
P11
P3
P0
P16
P16/P17
P17
P16 LEDs
P16/P17 LEDs
MOST50
MOST150
SBEV-RH850-MAIN
24019001 Made in Japan
D1x Mango Main Board Rev 1.0
CN3
CN4
SW3 - DCUTDI (PU)
SW5 - DCUTDO (open)
SW9 - DCUTCK (open)
SW2 - DCUTMS (PU)
SW7 - DCURST (PD)
SW1 - DCURDZ (open)
SW4 - MODE0 (open)
SW6 - FLMD1 (PD)
SW8 - MODE1 (open)

4.3 Alternative Settings of Y-RH850-D1M2H-PB-TET-V1 (RH850/D1M2H adapter board with TET BS socket)

Table 4-4: Positions of jumpers and switches on Y-RH850-D1M2H-PB-TET-V1 (RH850/D1M2H adapter board with TET BS socket) for alternative configuration

Part No.	Description	Default Position
JP25	Current Meas SDRBVCC	closed
JP1	Current Meas PLLVCC	closed
JP2	Current Meas REG1VCC	closed
JP3	Current Meas ISOVDD	closed
JP4	Current Meas EVCC	closed
JP5	Current Meas REG0VCC	closed
JP7	Current Meas OSCVCC	closed
JP6	Main-Oscillator Mux	open
JP8/9	Main-Crystal Mux	open
JP10	Main Crystal	N/A
JP24	Sub Crystal	N/A
JP11	Current Meas B0VCC	closed
JP12	Current Meas B1VCC	closed
DSW1	Encoding Address Enable	closed
DSW2	Bus Select	closed (all LOW)
JP13	Current Meas MVCC	closed
JP14	A0VREF	closed
JP15	Current Meas A0VCC	closed
JP16	Current Meas ISMVCC	closed
JP17	ZPDVREF	2-3
JP18	Current Meas ZPDVCC	closed
JP19	Current Meas SFVCC	closed
JP20	Current Meas B4VCC	closed
JP21	Current Meas B3VCC	closed
JP22	Current Meas B5VCC/RVCC	closed
JP23	Current Meas B2VCC	closed

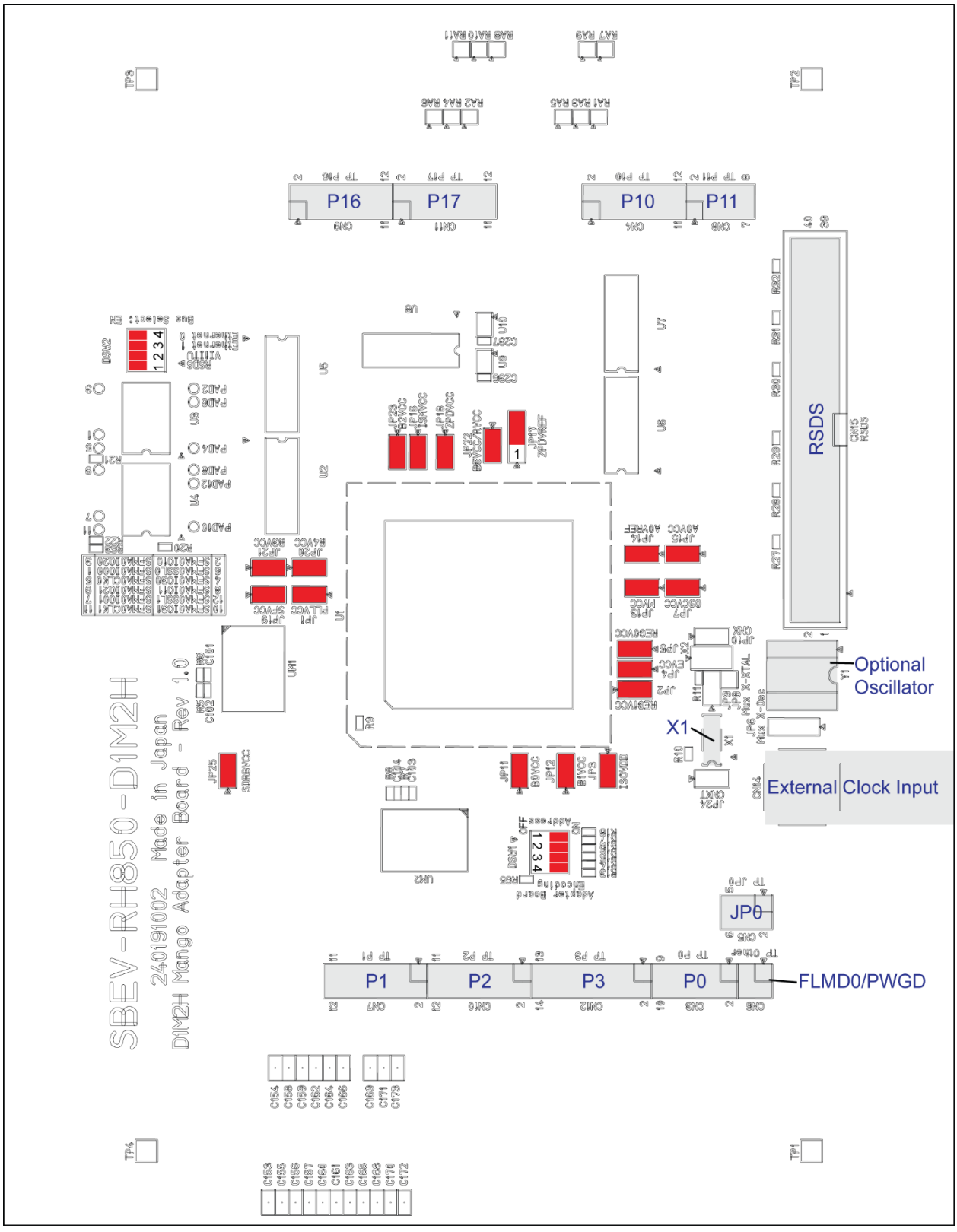


Figure 4: Alternative positions of jumpers and switches on Y-RH850-D1M2H-PB-TET-V1 (RH850/D1M2H adapter board with TET BS socket) - Red block indicates position of Jumper or DIP-Switch

Chapter 5 Revision History

Version / Document Number	Date [YYYY-MM-DD]	Description
V 0.1 R01AN2124ED0001	2014-05-30	Initial release
V 0.2 R01AN2124ED0002	2014-09-05	Updated chapter 2 - Reference Documents