AW2015 3 Channel LED Drivers with Auto Charging Indication

FEATURES

- 3-channel constant current LED drivers
  - 4- level I_{MAX} selections: 3/6/12/25mA
  - 256 current levels setting for each LED
  - Supports 256*256*256 color-mixing
- 256-level PWM dimming, 12-bit PWM resolution
- Support charging indication under low battery voltage condition
  - Directly start up LED1 via pulling pin CHRG_F up to high
  - AW2015: LED1 Breathing period: 5s, Max output current: 6mA
  - AW2015A: LED1 always on, output current: 3mA
- Automatic breathing light with flexible pattern configuration and running mode
  - three independent pattern controllers
  - pulses repeating, multiple colors alternative
  - multiple patterns running successively or cyclically
- 400kHz fast I²C interface , 1.8V ~ 3.3V
- Single power supply, 2.4V~5.5V
- Low power consumption
  - Less than 1μA in shut down mode
  - Less than 10μA in standby mode
- FC-QFN8L 1.2mmx1.2mmx0.37mm package

GENERAL DESCRIPTION

AW2015 is a three channels constant current LED driver with auto charging indication function. The max output current is 4-level selectable among 3mA, 6mA, 12mA and 25mA. Each LED is 256 current levels configurable so as to achieve 256*256*256 color mixing. The 256-level dimming and 12 bits PWM resolution create fine and smooth dimming effect even in low brightness.

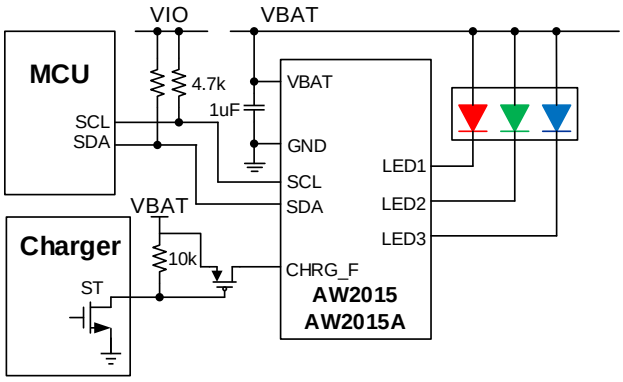
AW2015 can provide auto charging indication under the condition of low battery voltage. When the voltage of battery is too low, and the I²C interface can't work, the internal pattern controller will be activated if CHRG_F pin is high. LED1 of AW2015 will output breathing effect with period of 5s and 6mA max current. LED1 of AW2015A will hold LED on with 3mA output current.

In shut down mode, AW2015 turn off all internal circuit and the consumption is less than 1μA. In standby mode, I²C interface works and the consumption is less than 10μA.

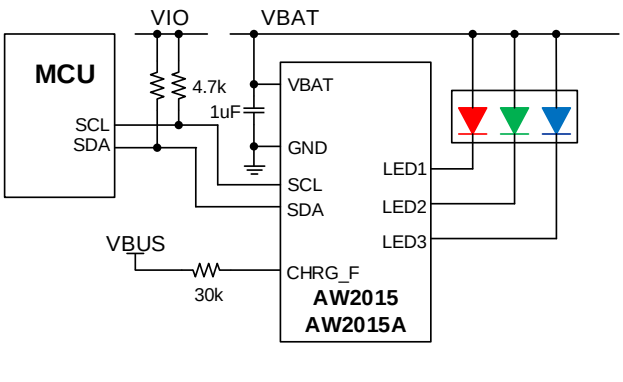
The device requires only 2.4V~5.5V single power supply. An I²C compatible interface in 400kHz fast mode is provided, the device address is 64h.

AW2015 is available in a ultra-thin 8 pin FC-QFN 1.2mm×1.2mm×0.37mm package.

TYPICAL APPLICATION CIRCUIT

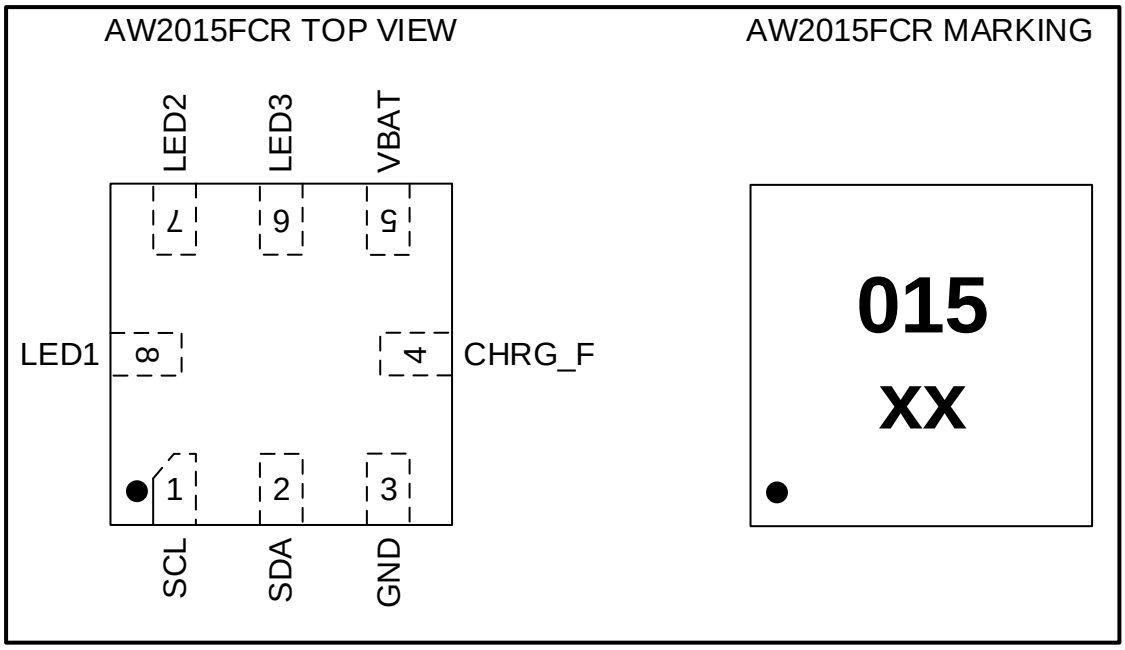


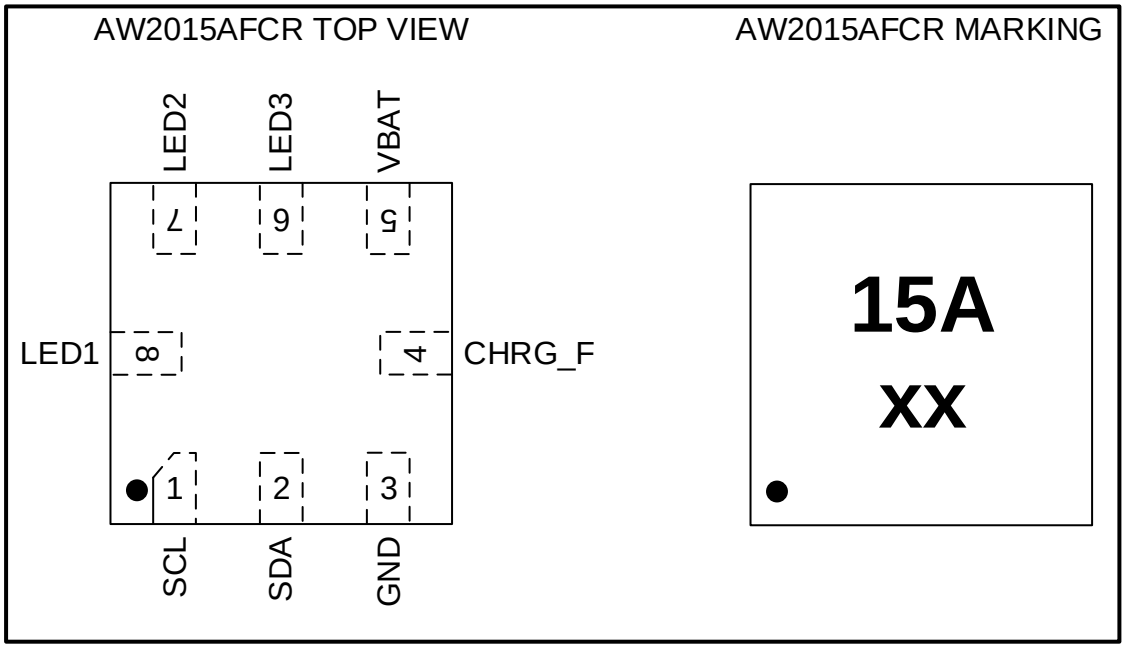
Charging Indicator Application



Adapter Plug In Indicator Application

PIN CONFIGURATION AND TOP MARK

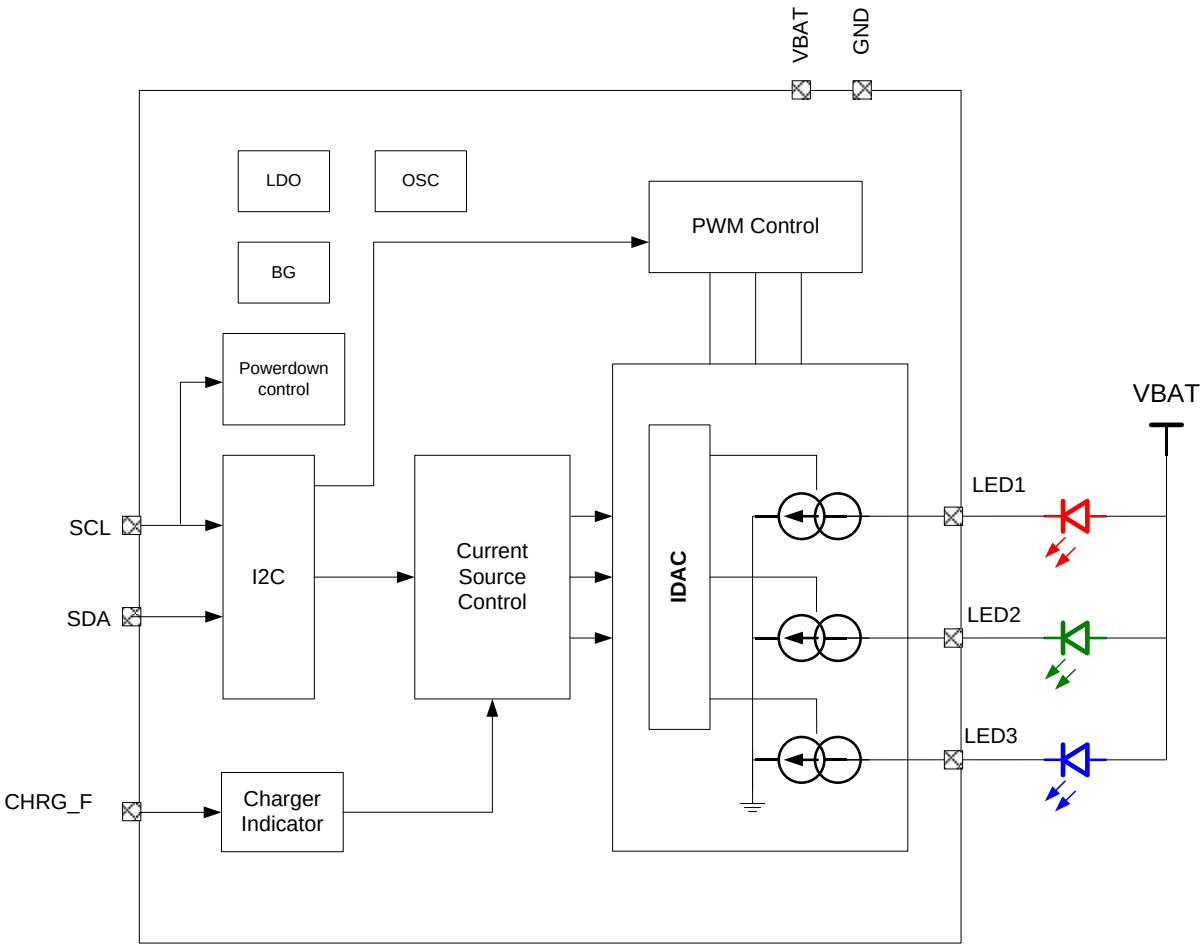




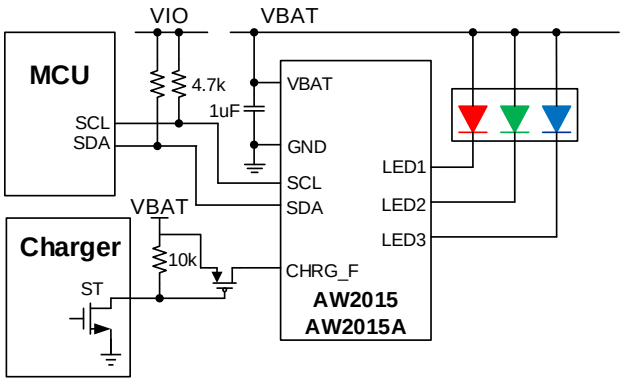
PIN DEFINITION

No.	NAME	DESCRIPTION
1	SCL	Serial Clock Input for I²C Interface
2	SDA	Serial Data I/O for I²C Interface
3	GND	GND
4	CHRG_F	Charge Indicator Input
5	VBAT	Power Supply (2.4V-5.5V)
6	LED3	LED3 Cathode Driver, anode connected to VBAT
7	LED2	LED2 Cathode Driver, anode connected to VBAT
8	LED1	LED1 Cathode Driver, anode connected to VBAT

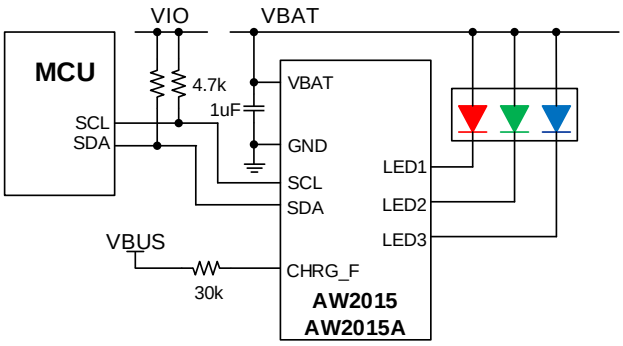
FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUITS



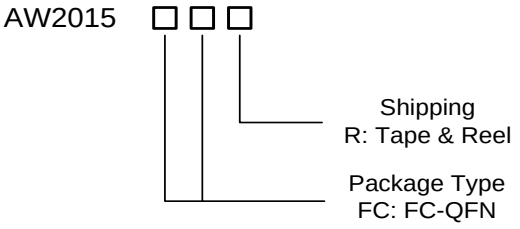
Charging Indicator Application

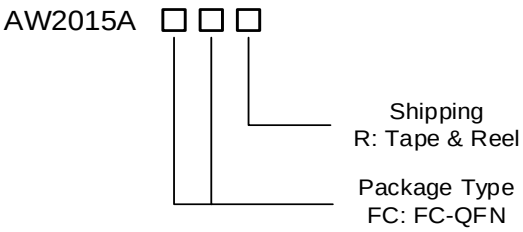


Adapter Plug In Indicator Application

ORDERING INFORMATION

Part Number	Auto Charging Indication	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW2015FCR	LED1 Breath	-40℃～85℃	1.2×1.2×0.37 FC-QFN-8L	015 XX	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW2015AFCR	LED1 Always On	-40℃～85℃	1.2×1.2×0.37 FC-QFN-8L	15A XX	MSL3	ROHS+HF	3000 units/ Tape and Reel





ABSOLUTE MAXIMUM RATING(NOTE 1)

PARAMETERS		RANGE
Supply voltage range V_{BAT}		-0.3V to 6.0V
Input voltage range	SCL, SDA,	-0.3V to 6.0V
	CHRG_F	-0.3V to 6.0V
	LED1~LED3	-0.3V to 6.0V
Output voltage range	SDA	-0.3V to 6.0V
Junction-to-ambient thermal resistance θ_{JA}		122℃/W
Operating free-air temperature range		-40℃ to 85℃
Maximum Junction temperature T_{JMAX}		150℃
Storage temperature T_{STG}		-55℃ to 125℃
Lead Temperature (Soldering 10 Seconds)		260℃
ESD(NOTE 2)		
HBM (human body model)		8000V
Latch-up		
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008		450mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7

ELECTRICAL CHARACTERISTICS

V_{BAT}=3.8V, T_A=25℃ for typical values (unless otherwise noted)

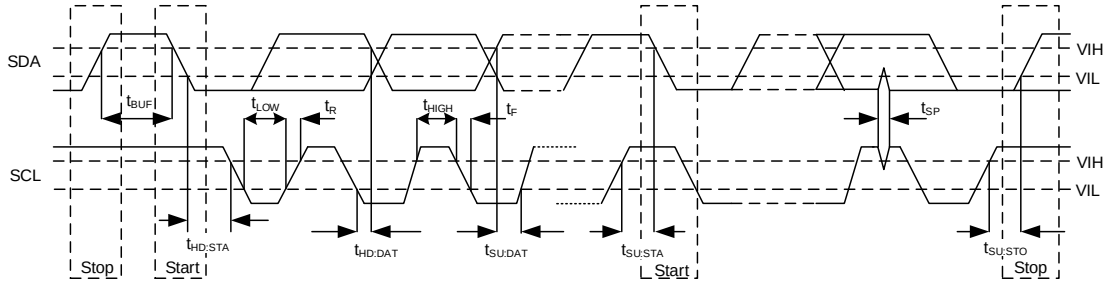
Symbol	Description	Test Conditions	Min	Typ	Max	Units
Power supply						
V_{BAT}	Input operation voltage	-	2.4		5.5	V
$I_{SHUTDOWN}$	Current in Shutdown mode	SCL/ SDA =0V CHRG_F=0V (over 130ms)		0.1	1	μA
$I_{STANDBY}$	Current in Standby mode	SCL/SDA=1.8V CHRG_F=0V		5	10	μA
I_Q	Quiescent Current in Active mode	register CHIPEN=1 all LED off		80	100	μA
I_{ACTIVE}	Current in Active mode	All channel set to 12.75mA		368		μA
		LED1 set to 12.75mA LED2,LED3 off		203		
		All channel set to 12.75mA T_{RISE}=2.1s,T_{ON}=0.04s T_{FALL}=2.1s, T_{OFF}=1s		140		
		LED1 set to 12.75mA LED2,LED3 off T_{RISE}=2.1s,T_{ON}=0.04s T_{FALL}=2.1s, T_{OFF}=1s		106		
Digital Logical Interface						
V_{IL}	Logic input low level	SDA,SCL			0.4	V
		CHRG_F			0.4	
V_{IH}	Logic input high level	SDA,SCL	1.3			V
		CHRG_F	V_{BAT} -0.2			
I_{IL}	Low level input current	SDA,SCL		5		nA
I_{IH}	High level input current	SDA,SCL		5		nA
V_{OL}	Logic output low level	SDA, I_{OUT}=3mA			0.4	V
I_L	Output leakage current	SDA open drain			1	nA
I^2C Interface						
F_{SCL}	I^2C-BUS clock frequency				400	kHz
$T_{DEGLITCH}$	SCL deglitch time			200		ns
	SDA deglitch time			250		ns
LED Driver						

I_{ACC}	Current accuracy	I_{LED}=12.75mA	-5%		+5%	%
I_{MATCH}	Matching accuracy	I_{LED}=12.75mA	-5%		+5%	%
V_{DROP}	Dropout voltage	I_{LED}=12.75mA		50	80	mV
F_{PWM}	PWM frequency	Register PWM_F=0	115	122	128	Hz
		Register PWM_F=1	230	244	256	Hz

NOTE5：The value is tested in default configuration.

I²C INTERFACE TIMING

Parameter Name			Min	Typ	Max	Units
F_{SCL}	Interface Clock frequency				400	kHz
$T_{DEGLITCH}$	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs



FUNCTIONAL DESCRIPTION

POWER_ON RESET

AW2015 provides a power-on reset feature that is controlled by VBAT supply voltage. When the VBAT supply voltage rises from 0V to 2.4V, the internal LDO starts to work. The reset signal will be generated to perform a power-on reset operation, which will reset all control circuits and configuration registers until the internal power voltage become stable.
The status bit STATUS.PUIS (register: 0x02 bit4) will be set to 1 when power-on reset operation occurs, which will be cleared by a read operation of STATUS register. Usually the STATUS.PUIS bit can be used to check whether an unexpected power-on event has taken place.

OPERATING MODE

In AW2015, pin SCL provides power down control. There are three work modes available: Shut-down, Standby and Active mode.

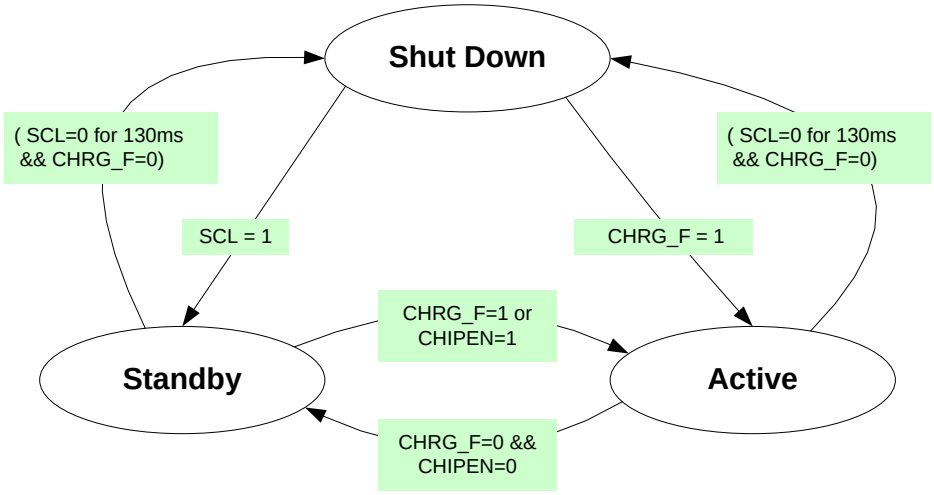


Figure 1. AW2015 operating mode transition

Shut-down Mode

AW2015 enters into the shut-down mode when CHRG_F is low and SCL level is pulled to low for over 130ms (prevents system against wrong resets caused by electromagnetically influences)
In shut-down mode, AW2015 will reset all internal circuits and configuration register, all blocks inside AW2015 are basically switched off except the power on reset circuit and the SCL level detect circuit, and the current consumption is very low (< 1μA).

Standby Mode

AW2015 enters into standby mode when SCL level is pulled high from shut-down mode or CHRG_F is low and CHIPEN is 0 from active mode. In standby mode, only part of internal circuit can work, the OSC still keep closed so that there is not internal clock, the LDO operates in low power state. The current consumption is less than 10μA.
In stand-by mode, the I^2C interface is accessible, but only registers RSTIDR and GCR can be operated.

Active mode

When bit CHIPEN of GCR register is set to 1in standby mode or CHRG_F is high in shut down mode, AW2015 enters into active mode.
In active mode, the internal OSC starts to work to provide clock signal. User can configure the device to produce the pre-defined pattern lighting effects in pattern mode or turn each LED on or off directly.
When PWM level is low in fade-in and fade-out, only the OSC module works and the consumption is about 80uA(I_Q). So the average consumption of breathing is every low.

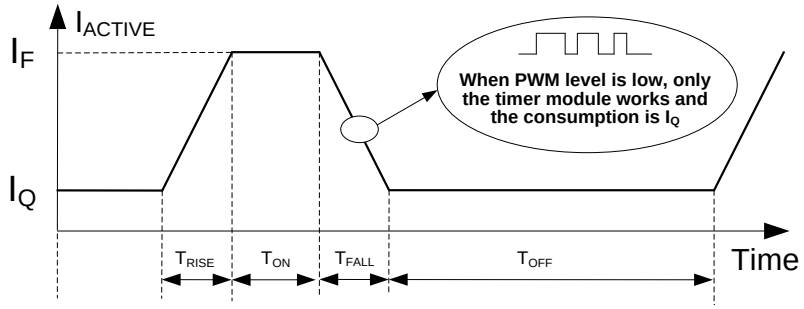


Figure 2. AW2015 consumption in active mode

Refer the following detailed formula (LED1/LED2/LED3 on)

$$I_{ACTIVE} = (I_F - I_Q) * \frac{(T_{RISE} + T_{FALL}) * 25\% + T_{ON}}{T_{RISE} + T_{ON} + T_{FALL} + T_{OFF}} + I_Q$$

IMAX	3.1875mA	6.375mA	12.75mA	25.5mA
I_F	223μA	272μA	368μA	565μA
I_Q	80μA	80μA	80μA	80μA

SOFTWARE RESET

Writing 0x55 to register RSTIDR (register: 0x00) via I²C interface will reset the AW2015 internal circuits and all configuration registers.

I²C INTERFACE

AW2015 supports the I²C serial bus and data transmission protocol in fast mode at 400 KHz. AW2015 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW2015 can support different high level (1.8V~3.3V) of this I²C interface.

Device Address

The I²C device address (7-bit) of AW2015 is 0x64, followed by the R/W bit (Read=1/Write=0).

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

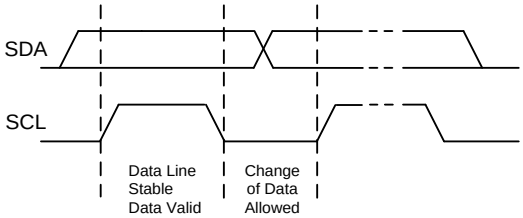


Figure 3. Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

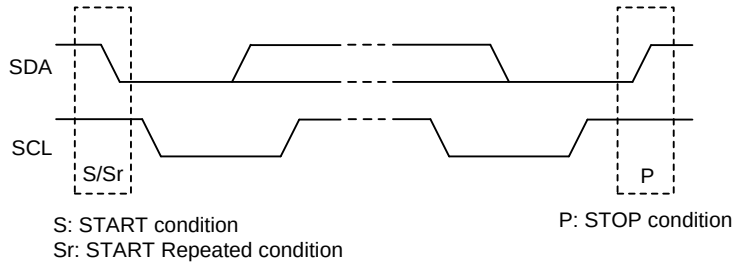


Figure 4. I²C Start/Stop Condition Timing

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

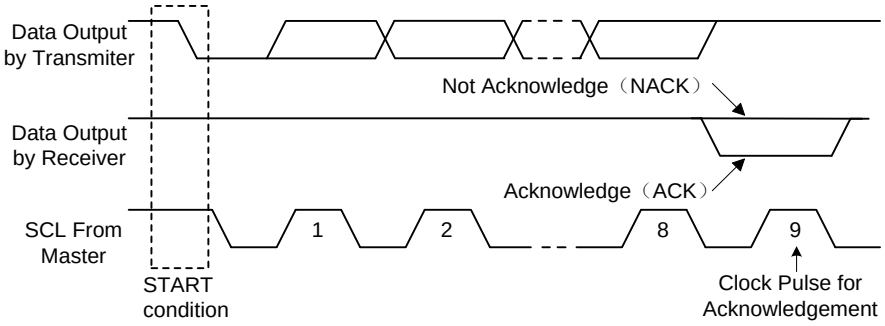


Figure 5. I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6,7)

i) Master generates STOP condition to indicate write cycle end

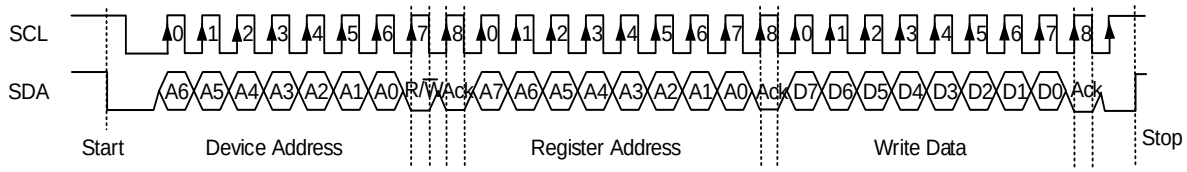


Figure 6. I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

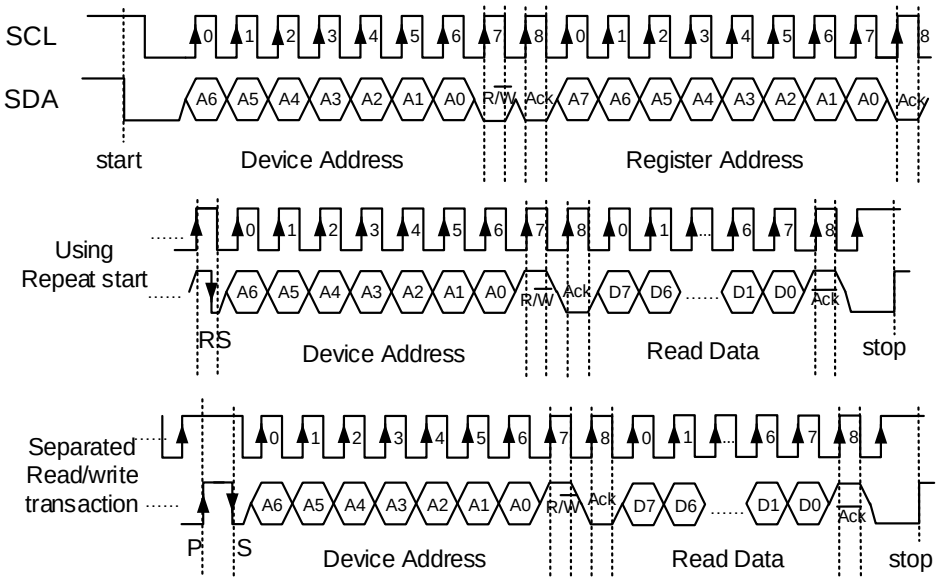


Figure 7. I²C Read Byte Cycle

LED DRIVER

AW2015 has three LED drivers to drive one RGB LED or three single-color LEDs. Each LED is driven by common-anode mode constant current source with duty cycle controlled by PWM. Both current and PWM can be configured via I²C interface.

LED Current

Globally, the maximum output current for three LEDs is 4-level selectable among 3.1875mA, 6.375mA, 12.75mA and 25.5mA via register IMAX (register: 0x03). In general, IMAX is used to set the max brightness of LED output. For each LED, there is 256 current levels configurable via 8-bit register groups ILEDx_y (x=1~3, y=1~4). So in RGB application it is possible to combine into 256x256x256 color-mixing schemes totally to achieve so-called true-color effect.
Generally the current level register is used to form specified LED color for RGB application. AW2015 has 4 groups pre-defined current registers capable of forming 4 dedicated colors in true-color pattern scheme, in which up to 4 pre-defined colors can be configured to represent 4 kinds of message, more than one color can flash one by one successively in the same pattern when it's necessary to transmit more than one messages.

PWM Dimming Control

In AW2015, each LED current source is gated by a 256-level, 12bit resolution PWM signal to create fine dimming effect.
Each LED has an 8 bit PWM register PWMx (register: 0x1c, 0x1d, 0x1e) to control the duty cycle of constant current source. The ramp up and down are automatically implemented by PWM duty continuously adjusted to form a smooth LED current transition between ON and OFF state. The ramp slope, for rise and fall, are separately set via configuring the bit4~bit7 in pattern registers PATx_1 and PATx_2.
The ramping can be configured as linear and logarithmic curve by setting bit0~1 (PWMLOG) in register LEDCTR (register 0x08).

LED Control

Each LED of AW2015 can be independently configured to work or not via control bit LEDxEN.

- LEDxEN = 0, LEDx channel is disabled and no current output.
- LEDxEN = 1, LEDx channel is enabled to output lighting effect in different work mode.

By register configuration, AW2015 provides two types of LED control modes:

- Pattern control mode.

AW2015 contains three independent pattern controller and three groups of pattern parameter register to generate user-defined breathing lighting effect. In RGB application, one pattern controller control 3 LED simultaneously to produce true-color breathing lighting, and three groups of pattern parameter can be executed successively or cyclically. For LED-independent application, three pattern controller are allocated to three different LEDs respectively, each operates with individual pattern parameter, user can start or stop each pattern independently

- Manual control mode.
  User directly set the brightness level of each LED by configuring relative current level register and PWM level register via I^2C interface. Usually it's recommended to modify the PWM level to set on or off. For each variation of PWM level register, the smoothly ramping effect is supported by setting FADE_IN bit and/or FADE_OUT bit in register LCFGx (x=1~3).

Pattern Control Mode

Breathing Lighting Control

When register bit LCFGx.LEDMD (register: 0x04, 0x05, 0x06 bit0) is set to 1, the corresponding LEDx operates in pattern mode.
User should configure the related pattern parameter registers according to actual timing requirements via I2C interface before starting pattern. The repeating times of pattern is configurable also, which may be 1~ 2048 or infinite according to setting of register PATx_T5 (x=1~4).

Single Pulse mode

Basically one pattern contains only one blinking, it's called as single pulse mode. In single pulse mode, the pattern parameters includes delay time, rise time, on time, fall time, off time and repeat times can be set by corresponding configuration registers (PATx_T1~T5), The meanings of basic single-pulse pattern parameters are shown in Figure and table below.

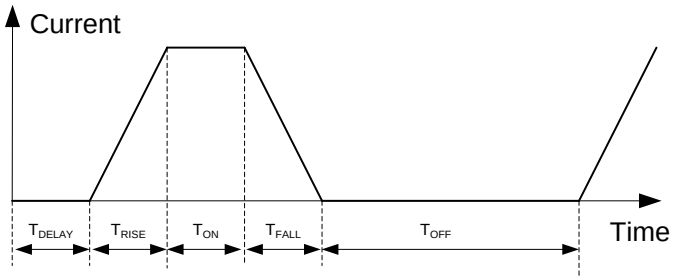


Figure 8. Basic single-pulse pattern parameter definition

Symbol	Parameters	Min	Typ	Max	Unit
T_{DELAY}	Delay time until pattern start	0		8	s
T_{RISE}	Rise time for dimming up	0		8	s
T_{ON}	On time	0.04		8	s
T_{FALL}	Fall time for dimming down	0		8	s
T_{OFF}	Off time	0.04		8	s

Multi-pulse mode

A serial fast pulse blinking can be used to transmit message different from that carried by single pulse. In multi-pulse mode, up to 4 pulses are allowed during one color blinking. Besides the basic timing parameter defined in single-pulse mode, there are 2 additional parameter need to be set:
The number of multi-pulse is defined by setting bit4~5 (MPULSE) in register PATx_T4 (register: 0x33/0x38/ 0x3D) , the actual blinking times is MPULSE+1.
The interval time between two adjacent pulses is defined by TSLOT, bit5~7 in PATx_T4 (register: 0x32/0x37/0x3C).

Symbol	Parameter	Min	Typ	Max	Unit
T_{SLOT}	Pause time between multiple pulses	0		1.024	s

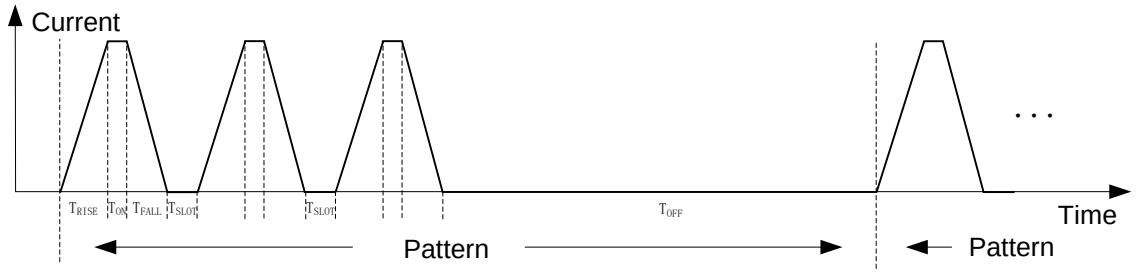


Figure 9. Multi-pulse pattern parameter definition

An example of multi-pulse pattern is shown below:

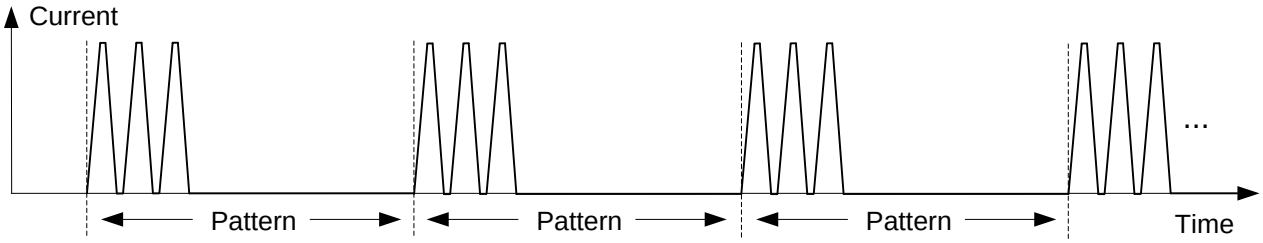


Figure 10. multi-pulse pattern example

Multi-color mode

Blinking with multiple different colors is allowed in one pattern period in RGB LED application, if different color is expected to carry different message.

In AW2015, the LED color is defined by LED current configure register ILEDx_y (x=1~3, y=1~4), there are 4 RGB current combination to generate 4 pre-defined colors for display. More than one of the 4 pre-defined colors can be chosen by setting CE1~CE4 , bit0~bit3 in PATx_T4 (register:x32/0x37/0x3C), when CEx is set to 1, the color#x is allow to be displayed in current pattern.

If the color setting on CE1~CE4 is modified during current pattern is running, the updating of new color setting will not occur until present pattern period is over.

If both multi-pulse and multi-color is enabled simultaneously, every selected color will blink specified times before switching to another color, and the display order of color is always from color #1 to color #4.

An example of 4-color /single-pulse pattern is shown below, in which the CE1~CE4 are changed twice during pattern is running.

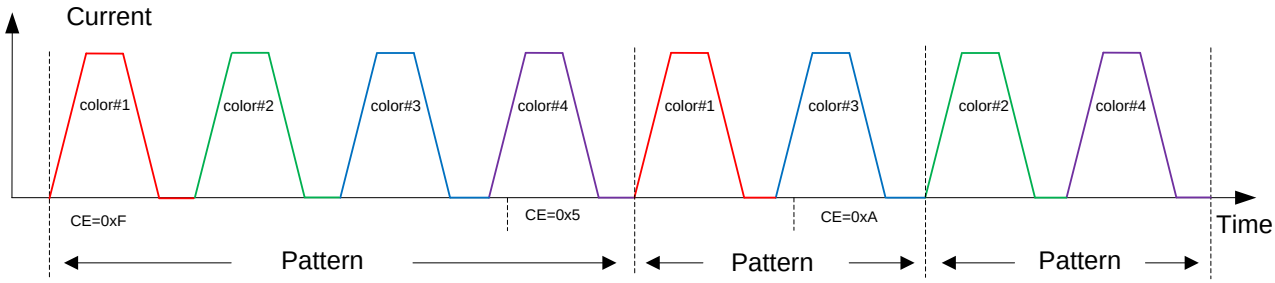


Figure 11. Example of multi-color mode and color scheme modification

True -color Breathing Lighting

In true-color breathing lighting application, the LEDMD, bit0 in LCFGx (register: 0x04, 0x05, 0x06), and the SYNC, bit3 in LEDCTR (register: 0x08 bit3) should be set to 1, three LED output share the same pattern controller to generate PWM dimming simultaneously. Multi-pulse, multi-color and multi-pattern modes are supported fully in this mode.

The RGB color is defined by LED current setting register ILEDx_y (x=1~3, y=1~4), there are 4 RGB current combination to generate 4 pre-defined color for display.

In true-color mode (SYNC=1), 3 groups of pattern timer parameters could be applied to defined 3 different breathing lighting effects, which can be executed successively or keep looping forever, without external processor involved to control every pattern switching. For each pattern, if PATx_T4.SW (register: 0x33, 0x38, 0x3E) is set to 1, the next pattern parameter will be loaded and started automatically after current pattern has finished.

The following table gives the current, pattern and the start/stop control source for each LED channel in true-color pattern mode.

Channel	Current Configuration Register	Pattern used	Pattern Start	Pattern Stop
LED1	ILED1_y	pattern #1, pattern #2, pattern #3	Write 1 to register PATRUN bit0	Write 1 to register PATRUN bit4
LED2	ILED2_y			
LED3	ILED3_y			

Note: Y=1~4, denotes 4 pre-defined color code (color #1, color #2, color #3 and color #4).

An example of single pulse and color pattern repeating in true-color pattern mode is depicted in the figure below.

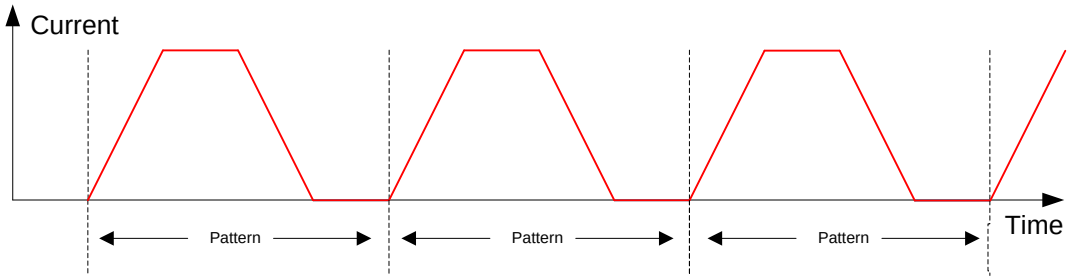


Figure 12. Example of single-pulse/single-color true-color pattern

The following figure is an example of multi pulse and multi color pattern repeating in true-color pattern mode.

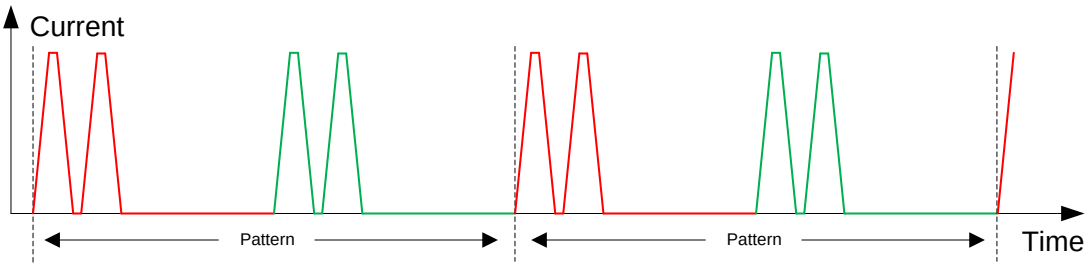


Figure 13. Example of 2-pulse/2-color in true-color pattern

The following figure is another example of three patterns running successively in true-color pattern mode.

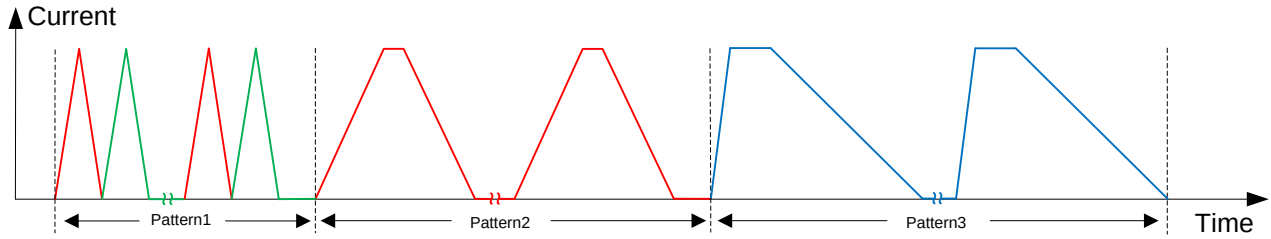


Figure 14. Example of 3 pattern running successively in true-color mode

Individual Breathing Lighting

In some application where three LED need blinking individually. When register bit LCFGx.LEDMD (register: 0x04, 0x05, 0x06 bit0) is set to 1, the corresponding LEDx operates in pattern mode. If register bit LEDCTR.SYNC

(register: 0x08 bit3) is 0, all pattern run in individually. In this mode, the 3 internal pattern controllers and 3 groups of pattern parameters are distributed to 3 LED channel respectively. Each LED can be controlled independently to blink according to its own pattern definition.

In this mode, multi-pulse pattern is supported, but multi-color is not supported, the bits CE1~CE4 in register PATx_T4 are ignored. Only registers ILEDx_1 is active for LED current setting, the other register including ILEDx_2, ILEDx_3 and ILEDx_4 are all useless.

The following table gives the current, pattern parameter and the start/stop control source selection for each LED channel in individual breathing lighting mode.

Channel	Current Setting Register	Pattern used	Pattern Start	Pattern Stop
LED1	ILED1_1 (register: 0x10)	pattern #1	write 1 to PATRUN bit0	write 1 to PATRUN bit4
LED2	ILED2_1 (register: 0x11)	pattern #2	write 1 to PATRUN bit1	write 1 to PATRUN bit5
LED3	ILED3_1 (register: 0x12)	pattern #3	write 1 to PATRUN bit2	write 1 to PATRUN bit6

The following figure shows an example of 3 patterns run individually with different pattern parameters.

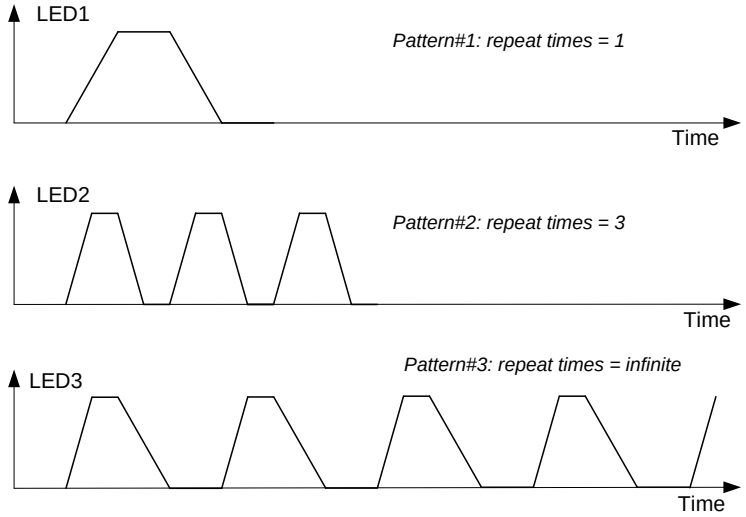


Figure 15. Example of Individual Pattern Mode

Manual Control Mode

When control bit LCFGx.LEDMD (register: 0x04, 0x05, 0x06 bit0) is set to 0, the corresponding LEDx is work in manual control mode.
In manual control mode, the LED lighting effects including color-mixed and brightness is directly configured by setting current/ PWM level register via I²C interface.
When LEDCTR.SYNC (register: 0x08, bit3) is set to 0, three LED are controlled individually, the PWM level and current for each is defined by PWM1/PWM2/PWM3 (register: 0x1C/0x1D/0x1E) and ILEDx_1 (register 0x10/0x11/0x12) respectively.
When LEDCTR.SYNC (register: 0x08, bit3) is set to 1, the output currents of three LED are defined by register ILEDx_1 respectively, but their PWM level are determined commonly by register PWM1. So user can change the brightness of all LED simultaneously by modifying the value of register PWM1 only.

Channel	Current	Brightness		Trise and Tfall time	
		SYNC=0	SYNC=1	SYNC=0	SYNC=1
LED1	ILED1_1	PWM1	PWM1	PAT1_T1/T2	PAT1_T1/T2
LED2	ILED2_1	PWM2		PAT2_T1/T2	
LED3	ILED3_1	PWM3		PAT3_T1/T2	

In manual control mode, auto dimming is supported. If LCFGx.FADE_OUT (register: 0x04, 0x05 0x06 bit2) is set to 1, automatic fade-out is enabled. If LCFGx.FADE_IN (register: 0x04, 0x05, 0x06 bit2) is set to 1, automatic fade-in is enabled. If a new value is set on PWMx register and auto dimming is enabled, the brightness of LED output ramp up/down smoothly, with its Trise and Tfall time defined by corresponding pattern configuration (PATx_T1 and PATx_T2).

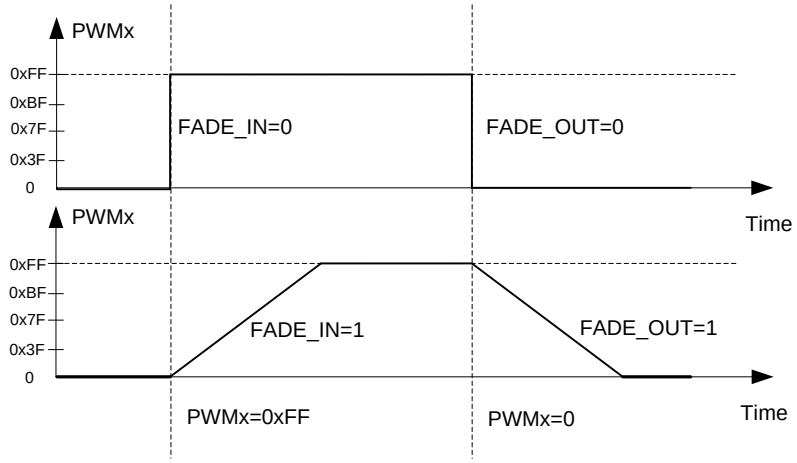


Figure 16. Manual Control Mode

Auto Charging Indication

In application of mobile phone, when battery voltage is too low and the PMU cannot work, the LED driver cannot be controlled by application processor via I²C interface. In this case, extra LED control circuit is necessary to be built in for charging status indication.
AW2015 provides the auto charging indication function for low battery voltage application. When the external USB power is inserts to phone, the pin CHRG_F is pulled high, AW2015 will enter active state automatically. The predefined pattern output only on pin LED1, the LED2 and LED3 keep off status.

AW2015:
The pattern parameter of AW2015 is showed in figure below. The maximum current is 6.375mA, breathing period is about 5s.

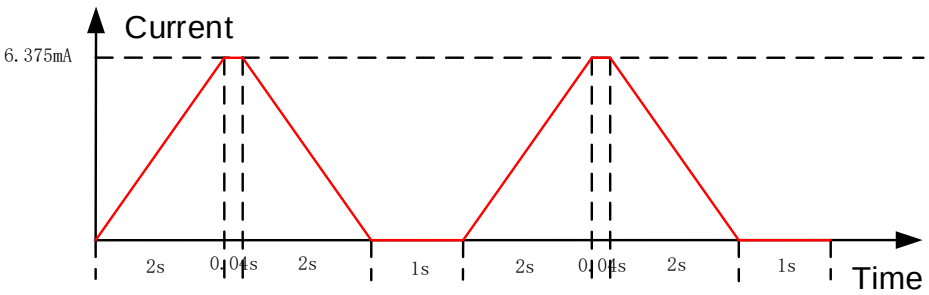


Figure 17. AW2015 Auto Charging Indication Pattern Parameter

AW2015A:
The pattern parameter of AW2015A is showed in figure below. The maximum current is 3.1875mA.

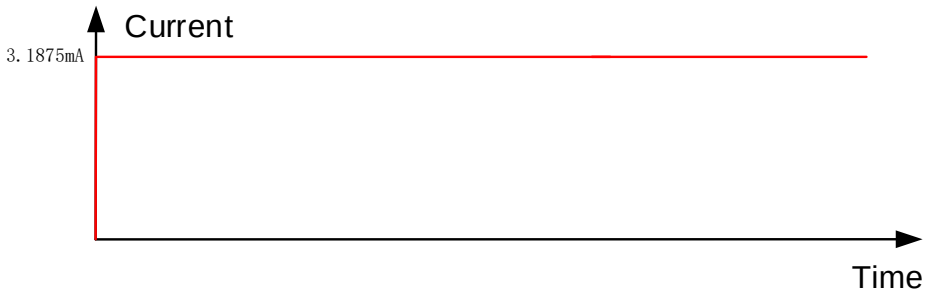


Figure 18. AW2015A Auto Charging Indication Pattern Parameter

Once the CHRG_F pin goes low, AW2015 comes back to shut-down state again and stops LED1 output.

The auto charging indication function should be closed by configured register GCR.CHGDIS (register: 0x01 bit2) to 1 when the processor is able to configure AW2015 via I²C interface, then the lighting effects will have no relation with the CHRG_F status.

When special charger IC is used and pin CHRG_F is recommend to be connected to status pin of charger IC, the pin LED1 of AW2015 can indicate the real battery charging status.

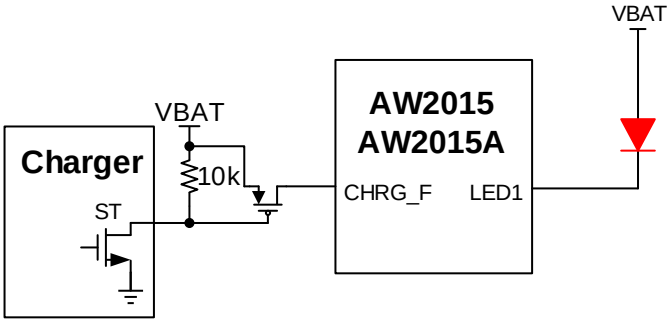


Figure 19. Real Charging Status Indication in special charger IC application

When no charger IC is applied, and battery charging is managed by PMU, no real charging status signal can be adapted, so the LED1 status can only indicate whether the USB power is plugged in or not.
When the pull-up resistance is 30KΩ, VBUS range can be 5V - 15V.

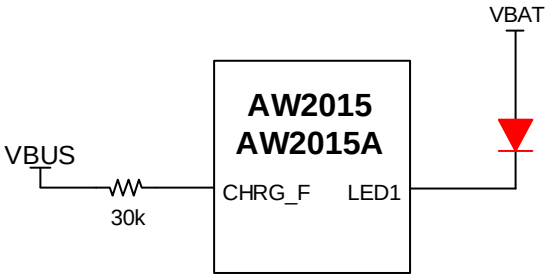


Figure 20. USB power Insertion status Indication in PMU charging control application

REGISTER DESCRIPTION

REGISTER LIST

Addr (Hex)	Name	W/R	7	6	5	4	3	2	1	0
00	RSTIDR	R	0	0	1	1	0	0	0	1
01	GCR	WR						PWM_F	CHGDIS	CHIPEN
02	STATUS	R				PUIS	-	LS2	LS1	LS0
03	IMAX	WR					-		IMAX	
04	LCFG1	WR	-	-	-	-		FADE_OUT	FADE_IN	LEDMD
05	LCFG2	WR	-	-	-	-		FADE_OUT	FADE_IN	LEDMD
06	LCFG3	WR	-	-	-	-		FADE_OUT	FADE_IN	LEDMD
07	LEDEN	WR		-	-	-	-	LED3EN	LED2EN	LED1EN
08	LEDCTR	WR			-	-	SYNC	-	PWMLOG	
09	PATRUN	WR	-	STOP3	STOP2	STOP1	-	RUN3	RUN2	RUN1
10	ILED1_1	WR	ILED1_1							
11	ILED2_1	WR	ILED2_1							
12	ILED3_1	WR	ILED3_1							
13	ILED1_2	WR	ILED1_2							
14	ILED2_2	WR	ILED2_2							
15	ILED3_2	WR	ILED3_2							
16	ILED1_3	WR	ILED1_3							
17	ILED2_3	WR	ILED2_3							
18	ILED3_3	WR	ILED3_3							
19	ILED1_4	WR	ILED1_4							
1A	ILED2_4	WR	ILED2_4							
1B	ILED3_4	WR	ILED3_4							
1C	PWM1	WR	PWM1							
1D	PWM2	WR	PWM2							
1E	PWM3	WR	PWM3							
30	PAT1_T1	WR	TRISE				TON			
31	PAT1_T2	WR	TFALL				TOFF			
32	PAT1_T3	WR	TSLOT				TDELAY			
33	PAT1_T4	WR	PATCTR	PATSW	MPULSE		CE4	CE3	CE2	CE1
34	PAT1_T5	WR	REPTIM							
35	PAT2_T1	WR	TRISE				TON			
36	PAT2_T2	WR	TFALL				TOFF			
37	PAT2_T3	WR	TSLOT				TDELAY			
38	PAT2_T4	WR	PATCTR	PATSW	MPULSE		CE4	CE3	CE2	CE1
39	PAT2_T5	WR	REPTIM							
3A	PAT3_T1	WR	TRISE				TON			
3B	PAT3_T2	WR	TFALL				TOFF			
3C	PAT3_T3	WR	-				TDELAY			
3D	PAT2_T4	WR	PATCTR	PATSW	MPULSE		CE4	CE3	CE2	CE1
3E	PAT3_T5	WR	REPTIM							

DETAILED REGISTER DESCRIPTION

RSTIDR, Chip ID and Software Reset Register

Address: 0x00, R/W, default: 0x31

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Symbol	Description
7:0	IDR	Chip ID, 0x31 Reset: write 0x55 to RSTIDR, reset internal logic and register

GCR, Global Control Register

Address: 0x01, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	PWM_F	CHGDIS	CHIPEN

Bit	Symbol	Description
2	PWM_F	PWM Modulation Frequency Select 0: 122Hz PWM modulation 1: 245Hz PWM modulation
1	CHGDIS	Charge Indication Function Disable control 0: enable 1: disable
0	CHIPEN	Device operating Enable 0: Disable, the device is in standby state 1: Enable, the device enters active state

STATUS Register

Address: 0x02, R/W, default: 0x10

7	6	5	4	3	2	1	0
0	0	0	PUIS	-	LS3	LS2	LS1

Bit	Symbol	Description
4	PUIS	Power Up Interrupt Status 0: No power-up reset has taken place 1: Power-up reset has taken place
2	LS3	operating status indication for pattern controller 3 0: stop state 1: running state
1	LS2	operating status indication for pattern controller 2 0: stop state 1: running state

0	LS1	operating status indication for pattern controller 1 0: stop state 1: running state

IMAX, LED Maximum Current Register

Address: 0x03, R/W, default: 0x01

7	6	5	4	3	2	1	0
-	-	-	-	-	IMAX		

Bit	Symbol	Description
1:0	IMAX	Maximum LED output Current Select 00：3.1875mA 01：6.375mA 10：12.75mA 11：25.5mA

LCFG1-3 LED Configure Register

LCFG1: Address: 0x04, R/W, default: 0x01
LCFG2: Address: 0x05, R/W, default: 0x00
LCFG3: Address: 0x06, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	FADE_OUT	FADE_IN	LEDMD

Bit	Symbol	Description
2	FADE_OUT	Fade-out enable control, only active in manual mode 0: PWM fade-out is disable, 1: PWM fade-out is enable, the dimming time decide by T_{FALL}
1	FADE_IN	Fade-in enable control, only active in manual mode 0: PWM fade-in is disable, 1: PWM fade-in is enable, the dimming time decide by T_{RISE}
0	LEDMD	LED Operating Mode Select. 0: Manual mode, LEDx is control directly by register ILEDx_1 and PWMx 1: Pattern mode

LEDEN, LED Channel Enable Register

Address: 0x07, R/W, default: 0x01

7	6	5	4	3	2	1	0
-	-	-	-	-	LED3EN	LED2EN	LED1EN

Bit	Symbol	Description
2	LED3EN	LED3 Enable 0: LED3 module stop work and LED3 out disable 1: LED3 output is enabled

1	LED2EN	LED2 Enable 0: LED3 module stop work and LED3 out disable 1: LED2 output is enabled
0	LED1EN	LED1 Enable 0: LED3 module stop work and LED3 out disable 1: LED1 output is enabled

LEDCTR, LED Control Register

Address: 0x08, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	SYNC	-	PWMLOG	

Bit	Symbol	Description
3	SYNC	LED Breathing Synchronous Mode Select 0: 3 LED work in asynchronous mode with independent control 1: 3 LED work in synchronous mode for RGB application.
1:0	PWMLOG	PWM Logarithmic curve select 0x: Log60 10: Log10 11: Linearity

PATRUN, Pattern Run/Stop Register

Address: 0x09, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	STOP3	STOP2	STOP1	-	RUN3	RUN2	RUN1

Bit	Symbol	Description
6	STOP3	Write 1, LED3 pattern stop if independent mode; The bit clears to 0 automatically after write 1.
5	STOP2	Write 1, LED2 pattern stop if independent mode; The bit clears to 0 automatically after write 1.
4	STOP1	Write 1, LED1 pattern stop if independent mode; Write 1, pattern stop if pattern mode; The bit clears to 0 automatically after write 1.
2	RUN3	Write 1, LED3 pattern run if independent mode; The bit clears to 0 automatically after write 1.
1	RUN2	Write 1, LED2 pattern run if independent mode; The bit clears to 0 automatically after write 1.
0	RUN1	Write 1, LED1 pattern run if independent mode; Write 1, pattern run if pattern mode; The bit clears to 0 automatically after write 1.

ILED1_y, LED1 Current Register

ILED1_1: Address: 0x10, R/W, default: 0xFF
ILED1_2: Address: 0x13, R/W, default: 0x00
ILED1_3: Address: 0x16, R/W, default: 0x00
ILED1_4: Address: 0x19, R/W, default: 0x00

7	6	5	4	3	2	1	0
ILED1_y							

Bit	Symbol	Description
2:0	ILED1_y	LED1 Current Configure Register for 4 pre-defined colors, The LED1 output current value is IMAX * ILED1_y / 255.

ILED2_y, LED2 Current Register

ILED2_1: Address: 0x11, R/W, default: 0x00
ILED2_2: Address: 0x14, R/W, default: 0x00
ILED2_3: Address: 0x17, R/W, default: 0x00
ILED2_4: Address: 0x1A, R/W, default: 0x00

7	6	5	4	3	2	1	0
ILED2_y							

Bit	Symbol	Description
7:0	ILED2_y	LED2Current Configure Register for 4 pre-defined colors, The LED2 output current value is IMAX * ILED2_y / 255.

ILED3_y, LED3 Current Register

ILED3_1: Address: 0x12, R/W, default: 0x00
ILED3_2: Address: 0x15, R/W, default: 0x00
ILED3_3: Address: 0x18, R/W, default: 0x00
ILED3_4: Address: 0x1B, R/W, default: 0x00

7	6	5	4	3	2	1	0
ILED3_y							

Bit	Symbol	Description
7:0	ILED3_y	LED3 Current Configure Register, for 4 pre-defined colors The LED3 output current value is IMAX * ILED3_y / 255.

PWM1/PWM2/PWM3 , PWM duty level Register

PWM1: Address: 0x1C, R/W, default:0xFF
PWM2: Address: 0x1D, R/W, default:0x00
PWM3: Address: 0x1E, R/W, default:0x00

7	6	5	4	3	2	1	0
PWMx							

Bit	Symbol	Description
7:0	PWMx	PWM level for LEDx (x=1,2,3)

PATx_T1, Time Parameter of Pattern x Register

PAT1_T1: Address: 0x30, R/W, default: 0x80
PAT2_T1: Address: 0x35, R/W, default: 0x00
PAT3_T1: Address: 0x3A, R/W, default: 0x00

7	6	5	4	3	2	1	0
TRISE				TON			

Bit	Symbol	Description
7:4	TRISE	Rise Time of pattern:

TRISE	Time	TRISE	Time
0000	0s	1000	2.1s
0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

3:0 TON On Time of pattern:

TON	Time	TON	Time
0000	0.04s	1000	2.1s
0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

PATx_T2, Time Parameter of Pattern x Register

PAT1_T2: Address: 0x31, R/W, default: 0x86
PAT2_T2: Address: 0x36, R/W, default: 0x00
PAT3_T2: Address: 0x3B, R/W, default: 0x00

7	6	5	4	3	2	1	0
TFALL				TOFF			

Bit	Symbol	Description
6:4	TFALL	Fall Time of pattern:

TFALL	Time	TFALL	Time

0000	0s	1000	2.1s
0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

2:0 TOFF Off Time of pattern:

TOFF	Time	TOFF	Time
0000	0.04s	1000	2.1s
0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

PATx_T3, Time Parameter of Pattern x Register

PAT1_T3: Address: 0x32, R/W, default: 0x00
PAT2_T3: Address: 0x37, R/W, default: 0x00
PAT3_T3: Address: 0x3C, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	TSLOT			TDELAY			

Bit Symbol Description

6:4 TSLOT Slot Time Between Pulses:

TSLOT	Time
000	0ms
001	130ms
010	260ms
011	380ms
100	540ms
101	670ms
110	800ms
111	1024ms

3:0 TDELAY Startup Delay Time of Pattern:

TDELAY	Time	TDELAY	Time
0000	0.04s	1000	2.1s

0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

PATx_T4, Time Parameter of Pattern x Register

PAT1_T4: Address: 0x33, R/W, default: 0x00
PAT2_T4: Address: 0x38, R/W, default: 0x00
PAT3_T4: Address: 0x3D, R/W, default: 0x00

7	6	5	4	3	2	1	0
PAT_CTR	PAT_SW	MPULSE		CE4	CE3	CE2	CE1

Bit	Symbol	Description
7	PAT_CTR	Pattern running forever control 0: pattern run forever 1: pattern stop or switch to next pattern after repeating specified times.
6	PAT_SW	Pattern Switch enable, active only in true-color pattern mode. 0: Pattern switch is disabled 1: Pattern switch is enabled
5:4	MPULSE	Multiple Pulse mode selection. 00: single pulse 01: pulse repeats 2 times 10: pulse repeats 3 times 11: pulse repeats 4 times
3	CE4	Color #4 display enable 0: Color#4 is masked 1: Color#4 is allow to display
2	CE3	Color #3 display enable 0: Color#3 is masked 1: Color#3 is allow to display
1	CE2	Color #2 display enable 0: Color#2 is masked 1: Color#2 is allow to display
0	CE1	Color #1 display enable 0: Color#1 is masked 1: Color#1 is allow to display Note: if CE1~CE4 are all set to 0, Color #1 is displayed by default

PATx_T5, Time Parameter of Pattern x Register

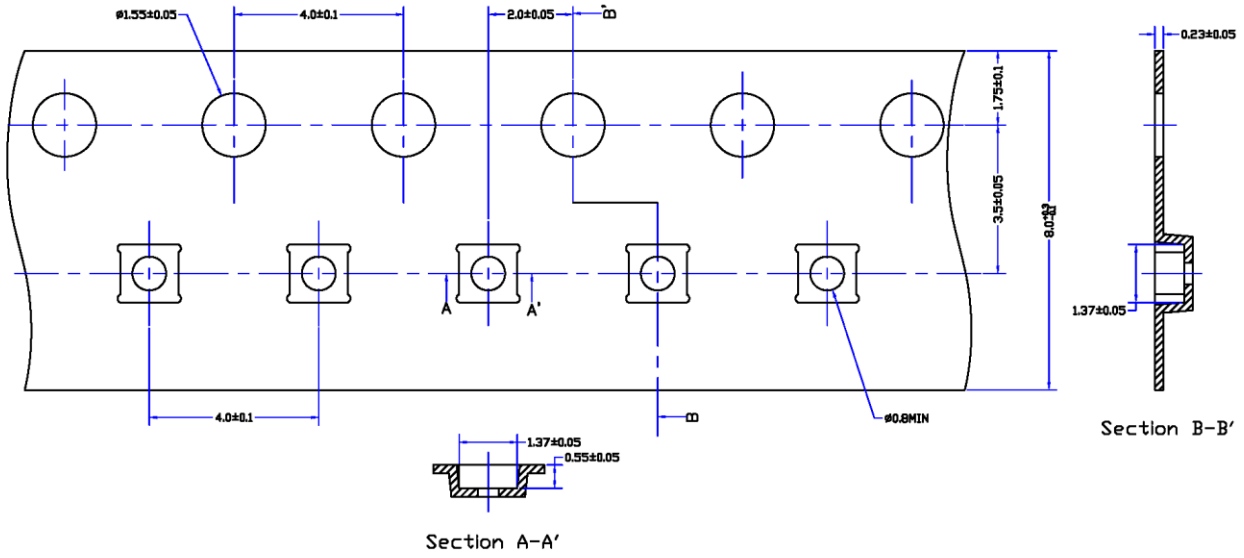
PAT1_T5: Address: 0x34, R/W, default: 0x00
PAT2_T5: Address: 0x39, R/W, default: 0x00
PAT3_T5: Address: 0x3E, R/W, default: 0x00

7	6	5	4	3	2	1	0
REPTIM							

Bit	Symbol	Description
7:0	REPTIM	PATTERN Repeat Times REPTIM [7] = 0: Pattern repeats REPTIM[6:0]+1 times REPTIM [7] = 1: Pattern repeats (REPTIM[6:0]+1) * 16 times

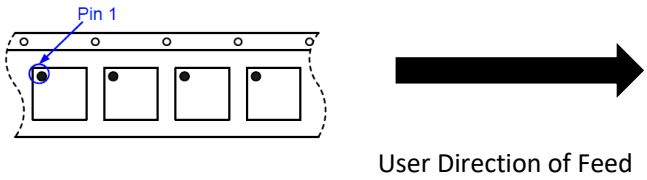
TAPE AND REEL INFORMATION

Carrier Tape

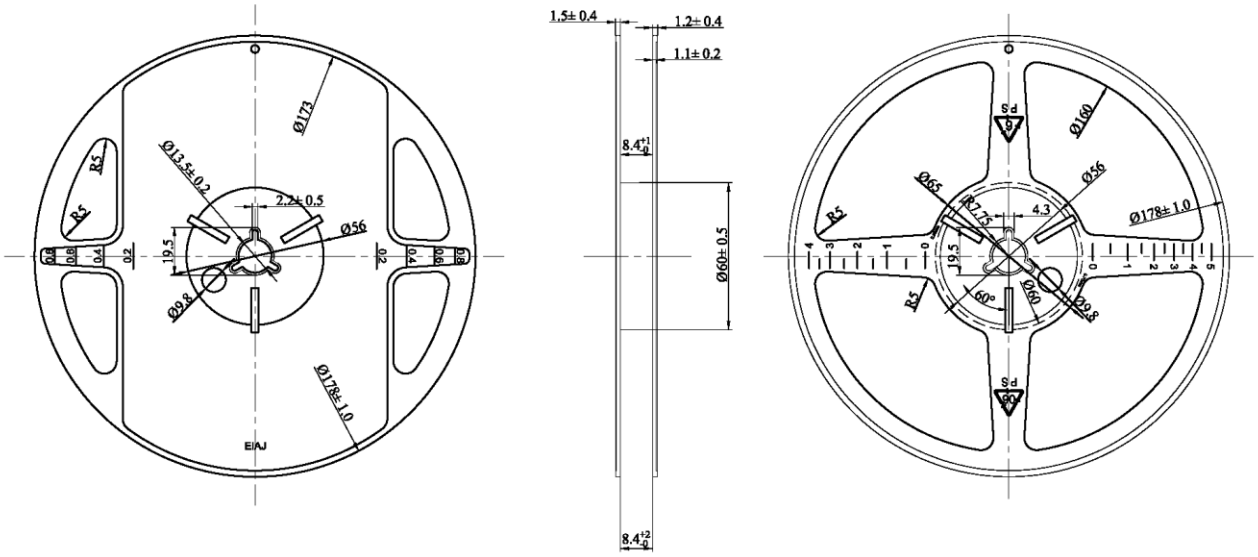


NOTES:
1.10 procket hole pitch cumulative tolerance ±0.2
2.The meander of the tape is assumed with 1mm or less every 100mm between 250mm
3.MATERIAL:CONDUCTIVE POYSTYRENE
4.ALL DIMS IN MM
5.There must not be foreign body adhesion and the state of the surface must be excellent
6.17" PAPER–Reel, 125000 pockets(500m)
7.Surface resistance 1X10E11(max) OHMS/SQ

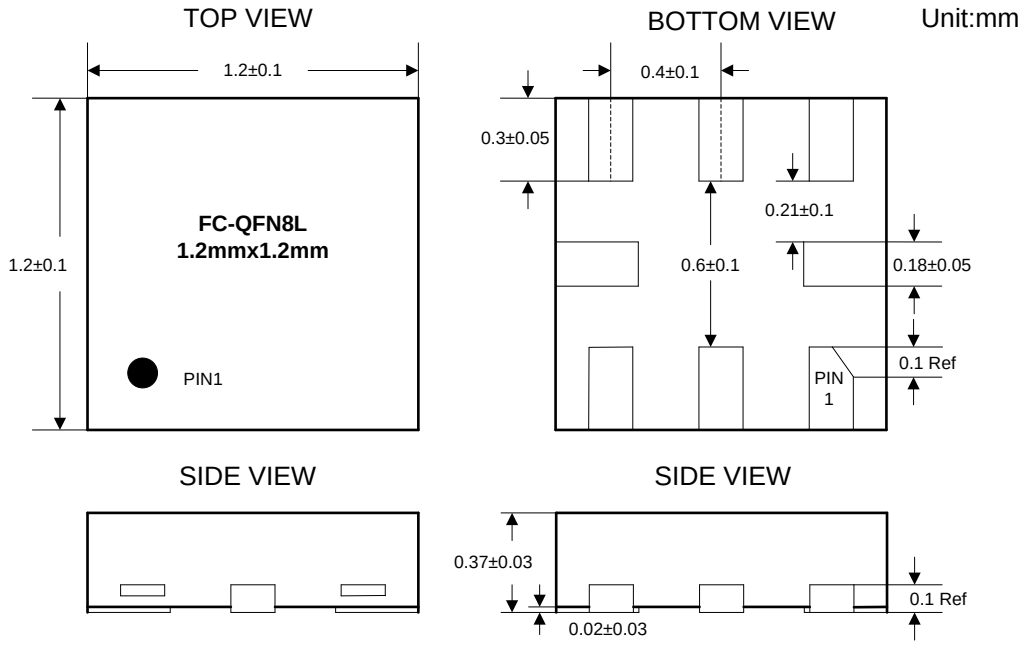
PIN1 Direction



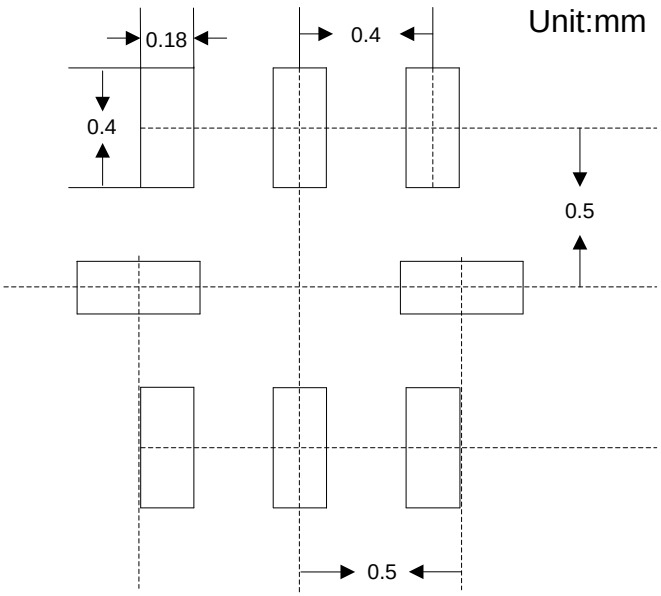
Reel



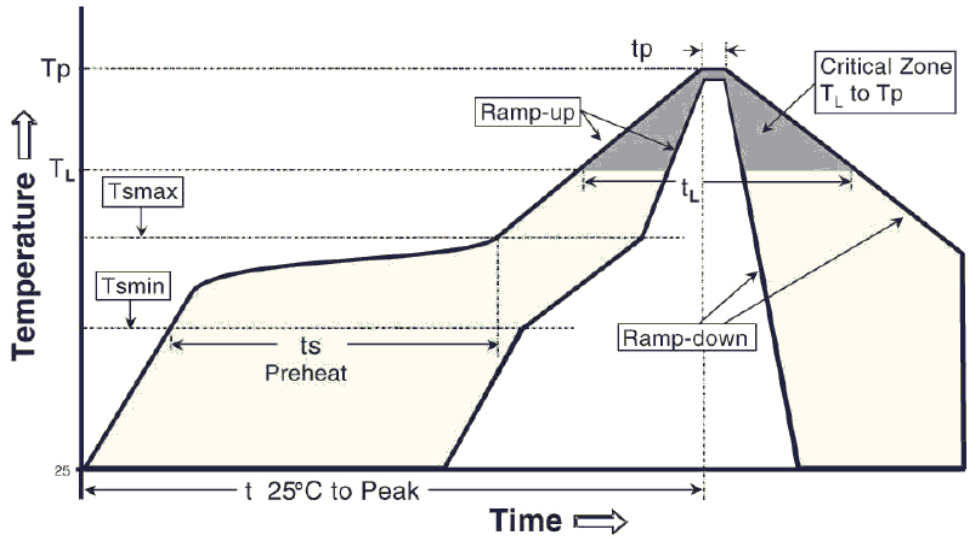
PACKAGE DESCRIPTION



RECOMMENDED LAND PATTERN



REFLOW PROFILE



Reflow profile

Classification Reflow Profile

Reflow condition	Sn-Pb eutectic assembly		Pb-Free assembly	
	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm³	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm³	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm³	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm³
Average ramp-up rate (Liquidus Temperature (T_L) to Peak)	3 °C/second max.		3 °C/second max.	
Preheat - Temperature Min ($T_{s(min)}$) - Temperature Max ($T_{s(max)}$) - Time (min to max) (t_s)	100 °C 150 °C 60-120 seconds		150 °C 200 °C 60-180 seconds	
$T_{s(max)}$ to T_L - Ramp-up Rate			3 °C/second max.	
Time maintained above: - Temperature (T_L) - Time (t_L)	183 °C 60-150 seconds		217 °C 60-150 seconds	
Peak Temperature (T_p)	225 +0/-5 °C	240 +0/-5 °C	245 +0/-5 °C	250 +0/-5 °C
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6 °C/second max.		6 °C/second max.	
Time 25 °C to Peak Temperature	6 minutes max.		8 minutes max.	

Parameters for classification reflow profile

Note: 1. All of the temperature parameters are measured from the top of package;

2、AW2015 is suitable for Pb-Free assembly.

REVISION HISTORY

Vision	Date	Revision Record
V1.0	May 2016	First officially release
V1.1	Apr.. 2017	Update parts of functional description
V1.2	Step. 2017	Update the i2c timing
V1.3	Nov. 2017	Update the ordering information

DISCLAIMER

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.
All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

