# WT6616F
# USB Power Delivery DRP Controller

For NVT power Internal Use Only

## Datasheet (General Version)

## Rev. 0.90

## March 2019

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# Table of Contents



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# 1. General Description

The WT6616F is a highly integrated USB Power Delivery (PD) Dual Role Port (DRP) controller that supports USB PD 3.0 Programmable Power Supply specification. It is designed for power banks.

The WT6616F minimizes external components by integrating USB PD baseband PHY, Type-C detection, shunt regulator, voltage and current monitors, NMOS load switch driver and an 8-bit MCU to allow small form factor and low BOM cost. Wide operation voltage range (3V to 24V) supports PD 3.0 Programmable Power Supply (PPS) specification. A Multi-Time-Programmable (MTP) ROM is provided for program code and user configuration data.

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# 2. Features

- USB Type-C and USB-PD
  - Supports USB PD 3.0 including Programmable Power Supply (PPS)
  - Programmable Type-C pull-up Rp
  - Dual Role Port (DRP)
- Supports USB BC1.2 DCP
- Built-in shunt regulator
  - Programmable constant voltage control
  - Programmable constant current control
  - Integrated low side current sense amplifier
  - Cable drop compensation
- Programmable fault protections
  - Over Voltage Protection (OVP)
  - Under Voltage Protection (UVP)
  - Over Current Protection (OCP)
  - Over Temperature Protection (OTP)
- 10-bit ADC for voltage and current monitoring
- MCU
  - Turbo 8051 compatible MCU
  - 16K bytes Multi-Time-Programmable (MTP) ROM
- Driver for NMOS load switch
- Built-in discharge MOS transistor
- Internal RC oscillator
- Internal VDD regulator
- General purpose I/Os
- Supports power saving mode
- Operating voltage range: 3V to 24V (30V tolerant)
- Operating temperature range: -20°C to +105°C
- Package: 16-Pin QFN

**Applications:**

- USB Type-C with Power Delivery power banks.

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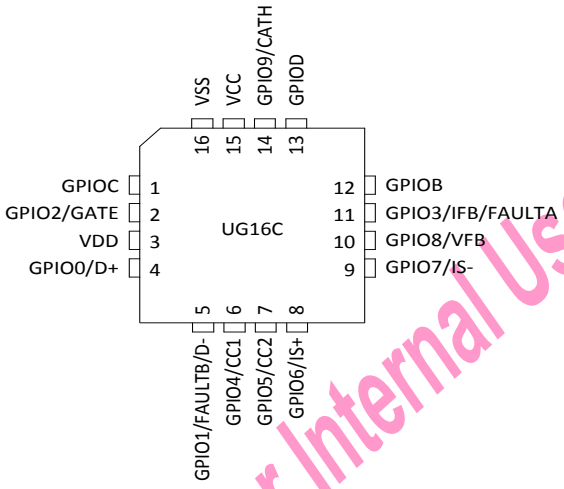
# 3. Pin Assignment

## 3.1. Package Type

16-pin QFN

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## 3.2. Pin Description

| Pin Number QFN 16C | Pin Name | Function | I/O Voltage | Type Input | Type Output | Description |
|---|---|---|---|---|---|---|
| 15 | VCC | VCC | HV | - | - | Positive power supply |
| 15 | GPIOA | GPIOA | HV | TTL | OD | General purpose I/O |
| | | DISC | | - | OD | Discharge |
| 16 | VSS | VSS | - | - | - | Ground |
| 1 | GPIOC | GPIOC | HV | TTL | OD | Serial purpose I/O |
| | | OTPA | | AN | - | Temperature sensing pin |
| | | ADC9 | | AN | - | ADC input |
| | | P07 | | TTL | OD | 8051 port I/O |
| 2 | GPIO2 | GPIO2 | HV | TTL | OD | General purpose I/O |
| | | GATE | | - | PP | Blocking MOS Control |
| | | ADC12 | | AN | - | ADC input |
| 3 | VDD | VDD | LV | - | AN | 4.8V regulator |
| 4 | GPIO0 | GPIO0 | HV | TTL | OD | General purpose I/O |
| | | D+ | | AN | - | D+ for B.C. with USB device side |
| | | ADC6 | | AN | - | ADC input |
| | | TX | | TTL | OD | UART transmitter |
| | | SDAB | | TTL | OD | $I^2C$ SDA B path |
| | | P00 | | TTL | OD | 8051 port I/O |

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| Pin Number QFN 16C | Pin Name | Function | I/O Voltage | Type Input | Type Output | Description |
|---|---|---|---|---|---|---|
| 5 | GPIO1 | GPIO1 | LV | TTL | OD | General purpose I/O |
| | | D- | | AN | - | D- for B.C. with USB device side |
| | | FAULTB | | TTL | OD | Fault indication. Outputs low when OVP/OCP. |
| | | ADC7 | | AN | - | ADC input |
| | | RX | | TTL | - | UART receiver |
| | | SCLB | | TTL | OD | $I^2C$ SCL B path |
| | | P01 | | TTL | OD | 8051 port I/O |
| 6 | GPIO4 | GPIO4 | HV | TTL | - | General purpose Input |
| | | CC1 | | CC | PP | USB Type-C Configuration Channel |
| | | ADC4 | | AN | - | ADC input |
| 7 | GPIO5 | GPIO5 | HV | TTL | - | General purpose Input |
| | | CC2 | | CC | PP | USB Type-C Configuration Channel |
| | | OTPC | | AN | - | Temperature sensing pin |
| | | ADC5 | | AN | - | ADC input |
| 8 | GPIO6 | GPIO6 | LV | TTL | OD | General purpose I/O |
| | | IS+ | | AN | - | Positive input of current sensing amplifier. |
| | | SCLA | | TTL | OD | $I^2C$ SCL A path |
| 9 | GPIO7 | GPIO7 | LV | TTL | OD | General purpose I/O |
| | | IS- | | AN | - | Negative input of current sensing amplifier. |
| | | SDAA | | TTL | OD | $I^2C$ SDA A path |
| 10 | GPIO8 | GPIO8 | LV | TTL | OD | General purpose I/O |
| | | VFB | | AN | - | Feedback of shunt regulator |
| | | P04 | | TTL | OD | 8051 port I/O |
| 11 | GPIO3 | GPIO3 | HV | TTL | OD | General purpose I/O. Open drain output. |
| | | IFB | | AN | - | Feedback of shunt regulator |
| | | FAULTA | | TTL | OD | Fault indication. Output low when OVE/OCP. |
| | | ADC3 | | AN | - | ADC input |
| | | P03 | | TTL | OD | 8051 port I/O |
| 12 | GPIOB | GPIOB | HV | TTL | OD | General purpose I/O. |
| | | OTPB | | AN | - | Temperature sensing pin |
| | | ADC8 | | AN | - | ADC input |
| | | P06 | | TTL | OD | 8051 port I/O |
| 13 | GPIOD | GPIOD | HV | TTL | OD | General purpose I/O |
| | | OTPD | | AN | - | Temperature sensing pin |
| | | P02 | | TTL | OD | 8051 port I/O |
| 14 | GPIO9 | GPIO9 | HV | TTL | OD | General purpose I/O |
| | | CATH | | - | AN | Cathode of shunt regulator |
| | | P05 | | TTL | OD | 8051 port I/O |

Legend: HV = High Voltage (max. 30V), LV = Low voltage (max. 5.5V), OD = Open Drain, PP = Push Pull, AN = analog, TTL = TTL compatible input, CC = USB PD baseband input.

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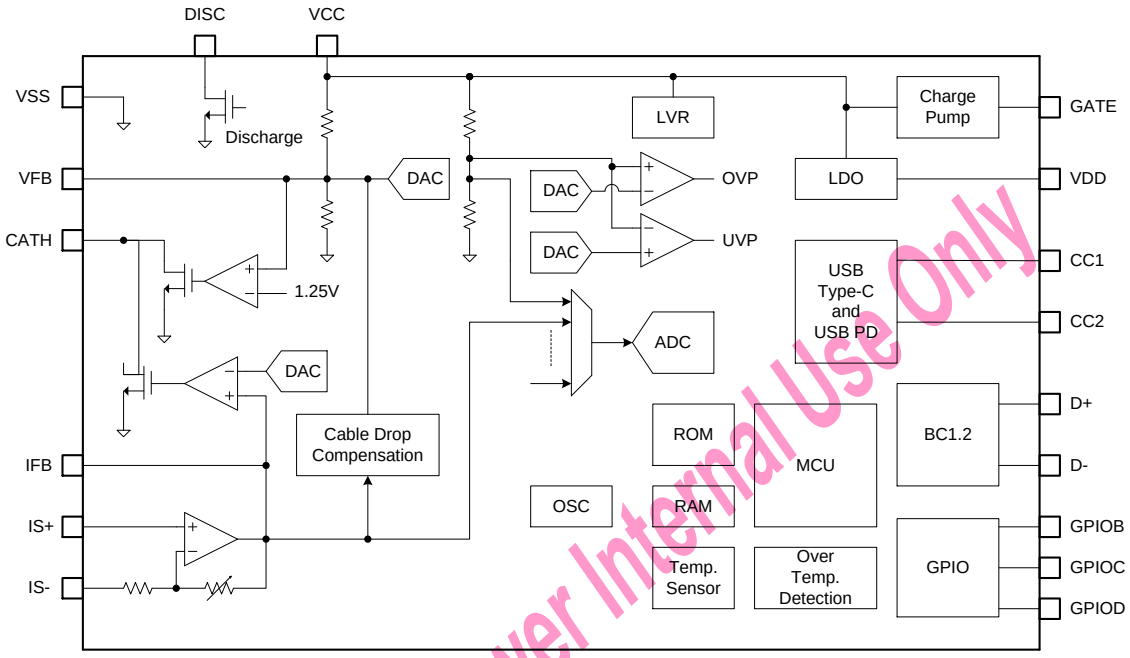
## 4. Block Diagram

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# 5. Functional Description

## 5.1. MCU and Peripherals

### 5.1.1. MCU

The WT6616F embeds an 8-bit 8051 compatible microcontroller with 16-bit addressable space and 8-bit data access functions. RAM size is 768 bytes, including 256 bytes internal RAM and 512 bytes of the external RAM. Program memory is 16k bytes Multiple Time Programmable (MTP) ROM.

### 5.1.2. Timer/Counter

Two general purpose 16-bit timer/counters are provided. Each timer/counter can be configured to operate in a variety of modes as a timer or as an event counter.

### 5.1.3. Serial Port

Standard 8051 serial port with Mode0~3 is supported. Baud rate range is from 2400 to 115200.

### 5.1.4. Interrupt

Five Interrupt sources are provided: two External Interrupts (INT0, INT1), two Timer/Counter Interrupts and one serial port interrupt. The priority of interrupt is programmable for user flexibility.

## 5.2. USB Type-C and Power Delivery

### 5.2.1. USB Type-C termination and detection

WT6616F includes all termination resistors (Rp and Rd). Rp and Rd resistors are required to implement connect detection. Type-C source pull-up resistance (Rp) is implemented by a configurable current source to advertise current capability. Attached/detached detection is done by multiple comparators with different threshold voltage and complied with Type-C specification. The WT6616F will preset Rd on its CC pins for initialization.

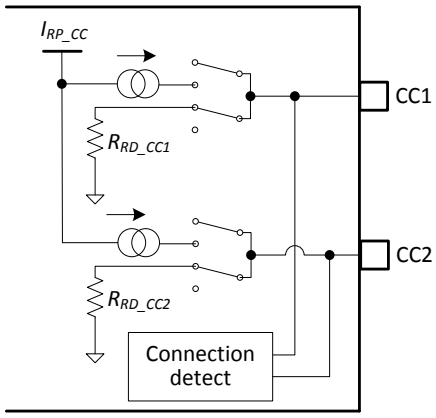


Figure 5-1 Type-C pull-up current and pull low resistors

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### 5.2.2. USB PD PHY

USB PD PHY consists of a pair of transmitter and receiver that communicate across CC wire using Biphase Marking Coding (BMC).

The transmitter performs:

- Receive packet data from the protocol layer
- Calculate and append a CRC
- Encode the packet data including the CRC
- Transmit the Packet (Preamble, SOP, payload, CRC and EOP) across the CC channel using BMC

The receiver performs:

- Recover the clock and lock onto the Packet from the Preamble
- Detect the SOP, SOP' and SOP"
- Decode the received data including the CRC
- Detect the EOP and validate the CRC
- If the CRC is valid, deliver the packet data to the protocol layer
- If the CRC is not valid, flush the received data

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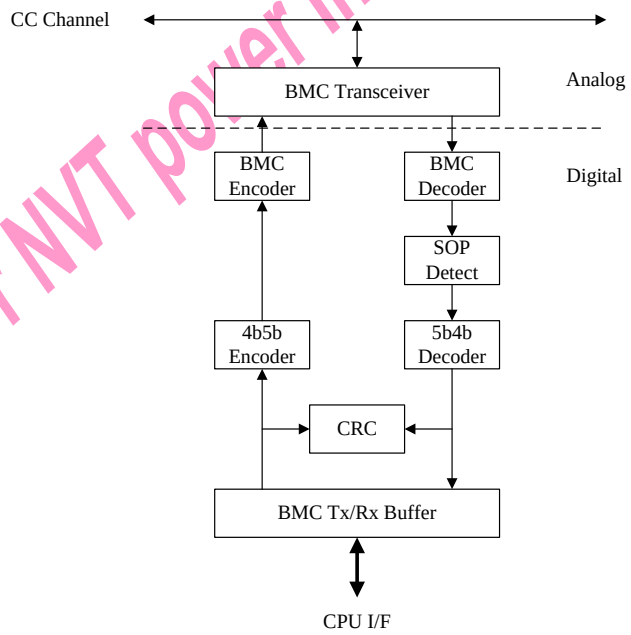


Figure 5-2 USB PD Physical Layer

## 5.3. VBUS Control

Two modes of VBUS control circuit are provided for interfacing with different PWM controllers.

### 5.3.1. Control of optocoupler

The constant voltage regulation is implemented by sensing VCC pin via the resistor divider and comparing with internal reference voltage to generate a compensation signal on the CATH pin. VBUS voltage can be adjusted by DAC from 3.0V to 21V with 20mV granularity.

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The constant current regulation is incorporated with the current sense amplifier. VBUS current is limited when the output of current sense amplifier is larger than the DAC output. A current limit flag will be raised when it is in current limit mode.

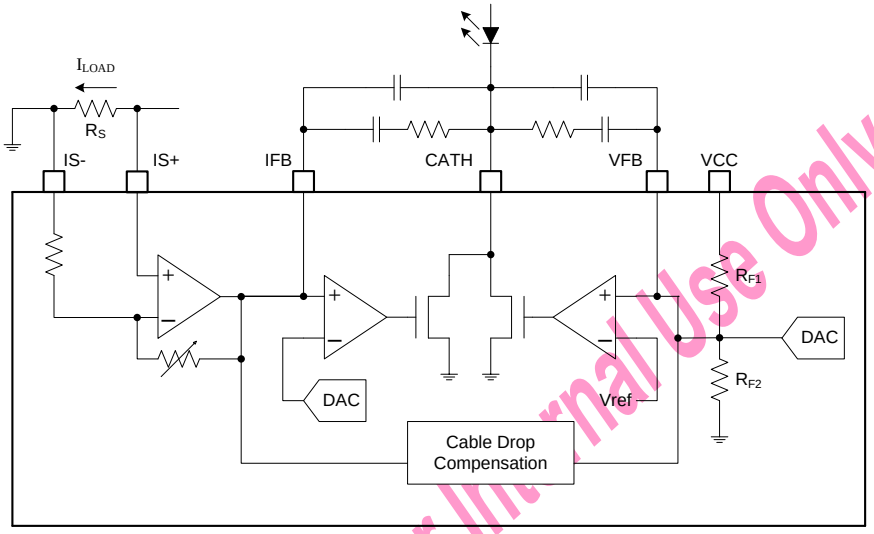


Figure 5-3 Optocoupler control mode

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### 5.3.2. Control of PWM Feedback

In this mode, VFB pin can be connected to the feedback pin of PWM controller such as Power Integrations ™ InnoSwitch3. When the load current exceeds the constant current threshold, a pull-up current is introduced on VFB pin and reduces the VBUS voltage to regulate the current. A compensation capacitor is required on CATH pin for reducing current ripple.

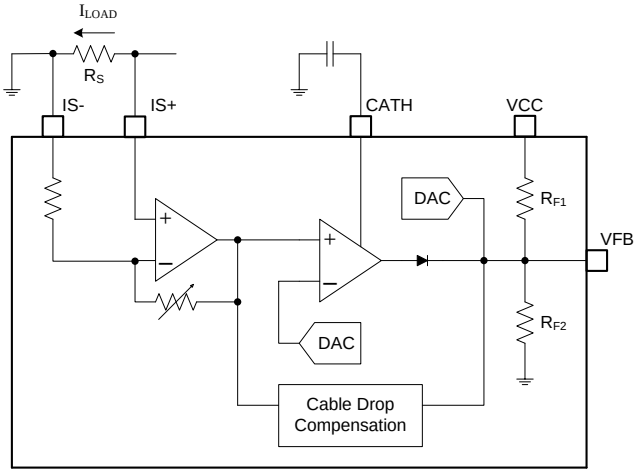


Figure 5-4 Direct feedback control mode

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## 5.4. Cable Drop Compensation

In order to compensate the voltage drop caused by the cable resistance, a compensation current which is proportional to load current is connected to the VFB pin as shown in Figure 5-3.

The compensation voltage is calculated by

$$V_{COMP} = \frac{1}{3} \times K \times (I_{LOAD} \times R_S \times A_V)$$

where K: compensation factor

$A_V$ : gain of current sense amplifier

$R_S$ : current sense resistance

To fully compensate the IR drop, $V_{COMP} = I_{LOAD} \times R_{CABLE}$

So $K = 3 \times \frac{R_{CABLE}}{R_S \times A_V}$

For example, if $R_{CABLE}$=160mΩ, $R_S$=5mΩ, $A_V$=80, then choose K=1.2

## 5.5. Protections

All protections are programmable and can be set to auto-restart or latched. OVP, UVP, OCP and OTP are implemented by hardware and also can be disabled for using FW control.

### 5.5.1. OVP and UVP

Over Voltage Protection and Under Voltage Protection is implemented by comparing VCC with individual DAC (Digital to Analog Converter). When VCC voltage is larger than the OVP trip point or under than the UVP trip point, an interrupt is generated and GATE pin goes to low level to turn off load switch.

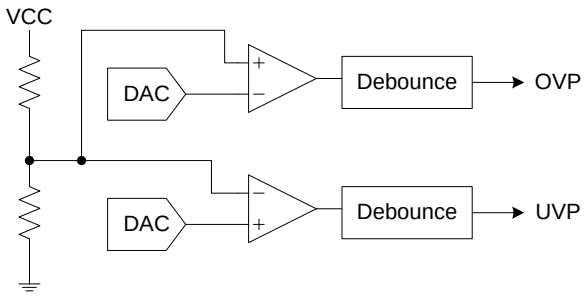


Figure 5-5 OVP and UVP circuit

### 5.5.2. Over Current Protection

Load current is monitored by reading ADC. Over current protection trip point and debounce time are set by firmware. In power saving mode, the ADC can be changed to comparator mode and wake up MCU when load current exceed setting point.

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### 5.5.3. Over Temperature Protection

Over Temperature protection (OTP) is implemented by a comparator and a current source. The current source provides a constant current to the selected pin and sense the voltage on the external NTC thermistor. When temperature is larger than the OTP trip point which is set by MCU setting, GATE pin goes to low level to turn off load switch and generates an interrupt to MCU. Voltage on the thermistor can also be read through ADC.

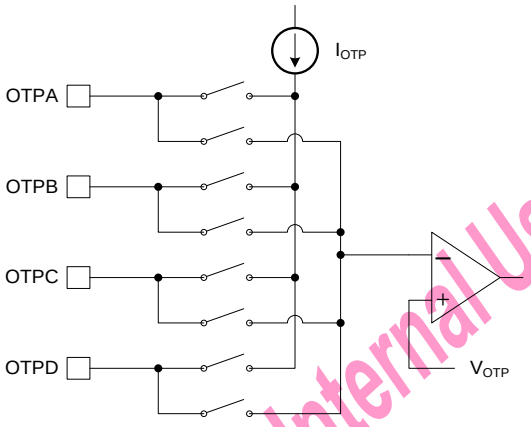


Figure 5-6 Over temperature detection circuit

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## 5.6. On-chip Temperature Sensor

An on-chip temperature sensor is provided. Chip temperature can be read by MCU and generates protection if the temperature is too high.

## 5.7. ADC

The Analog/Digital Converter (ADC) is SAR type with 10-bit resolution and 12 input channels. It provides a single conversion mode with four selectable conversion rate (1MHz, 500kHz, 250Hz and 125kHz) and a comparator mode. The reference voltage of ADC is 2.56V.

**Single Conversion Mode:**

The ADC starts to convert by MCU enabling conversion. When the conversion is completed, a flag and an interrupt are generated to inform MCU reading the data.

**Voltage Compare Mode:**

The input voltage is compared with the DAC and can generate an interrupt either the voltage is higher or lower than the DAC. This function can be used to wakeup MCU when it is stopped during power saving mode.

## 5.8. USB BC1.2

The WT6616F supports USB Battery Charging Rev.1.2 (BC1.2). The HVDCP leverages USB BC1.2 compliant signaling on D+ and D- in order to negotiate voltage requests on VBUS.

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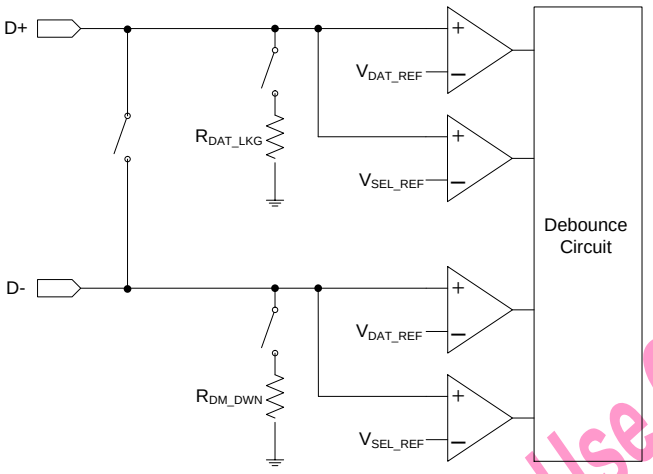


Figure 5-7 BC1.2 block diagram

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## 5.9. Discharge

When VBUS transits from a higher voltage level to a lower voltage level, it requires a discharge current to fulfill the transition time specification of USB-PD. There are four transistors can be enabled independently to control discharge time.

## 5.10. Load Switch Driver

A charge pump is built in to drive the external NMOS load switch. To prevent reverse current from output, it is suggested to use two NMOS switches in series with their sources connected together...

## 5.11. GPIO

All GPIOs can be configured as an input or output except GPI4 and GPI5 are input only. When configured as an output port, it is open drain type.

## 5.12. Watchdog Timer

Watchdog Timer can be used to detect CPU failures, such as the software deadlock circles caused by noises, voltage disturbance, or power off etc. When the internal counter of the Watchdog Timer overflows, a reset signal will be generated then reset the CPU.

## 5.13. Resets

There are several reset sources to generate RESET signal:

(1) Power On Reset (POR)
(2) 1.8V regulator Low Voltage Reset
(3) VCC Under Voltage Lockout (UVLO)
(4) VDD Low Voltage Reset
(5) Watchdog Reset
(6) Program Counter Overflow Reset

All reset sources can be enabled/disabled except Power On Reset.

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# 6. Electrical Characteristics

## 6.1. Absolute Maximum Ratings

| Parameter | | Min. | Max. | Units |
|---|---|---|---|---|
| Supply voltage VCC pin | | –0.3 | 30 | V |
| I/O voltage | GPIO0, GPIO3, GPIO4, GPIO5, GPIO9, GPIOB, GPIOC, GPIOD | –0.3 | VCC + 0.3 (Max. 30V) | V |
| | GPIO2 | –0.3 | 37 | V |
| | GPIO1, GPIO6, GPIO7, GPIO8 | –0.3 | VDD + 0.3 | V |
| Output voltage | VDD | -0.3 | 6 | V |
| Operating temperature | | -40 | 125 | °C |
| Storage temperature | | -55 | 150 | °C |

NOTE: Maximum ratings applied to the device are individual stress limit value. Stresses above those listed may cause permanent damage and reliability may be affected. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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## 6.2. Thermal Characteristics

**16-pin QFN**

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Thermal Resistance (Junction to Air) | | | 44 | | °C /W |
| $\theta_{JC}$ | Thermal Resistance (Junction to Case) | | | 7.3 | | °C /W |
| $T_{JMAX}$ | Maximum Junction Temperature | | | 125 | | °C |

## 6.3. Recommended Operating Conditions

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC\_OPR}$ | Operating voltage | At DFP mode | 3 | | 24 | V |
| | | At UFP mode | 4 | | 24 | V |
| $V_{IO\_HV}$ | GPIO0, GPIO3, GPIO4, GPIO5, GPIO9, GPIOB, GPIOC, GPIOD | | 0 | | $V_{CC\_OPR}$ + 0.3 | V |
| $V_{GATE\_HV}$ | GPIO2 pin | | 0 | | $V_{CC\_OPR}$ + 8.5 | V |
| $V_{IO\_LV}$ | GPIO1, GPIO6, GPIO7, GPIO8 | | 0 | | $V_{O\_LDO}$ + 0.3 | V |
| $V_{DD\_LDO}$ | VDD pin | | 4.6 | 4.85 | 5.1 | V |
| $T_{OPR}$ | Operating Temperature | | -20 | | 105 | °C |

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## 6.4. DC Characteristics (VCC=20V, Ta= -20 ~ +105°C, unless specified)

### 6.4.1. VCC and VDD

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | VCC Operating Voltage | In DFP mode | 3 | | 24 | V |
| | | In UFP mode | 4 | | 24 | V |
| $I_{CC\_OPR1}$ | VCC Current, normal operating | VCC ≧ 4.5V, No load at output, MCU operating @ 10MHz, | | 8 | 10 | mA |
| $I_{CC\_OPR2}$ | VCC Current, normal operating | VCC < 4.5V, No load at output and MCU operating @ 10MHz | | 18 | 22 | mA |
| $I_{CC\_STDBY}$ | VCC Current, standby mode MCU off | CC1 pin floating | | 0.8 | 1.0 | mA |
| | | CC1 pin 5.1KΩ pull low | | | 1.3 | mA |
| $V_{UVLO}$ | VCC Under Voltage Lockout | VCC rising | 3.5 | | 4.35 | V |
| | | VCC falling | 2.6 | | 2.85 | V |
| $V_{DD}$ | VDD regulator output voltage | $I_{DDO}$ = 0 ~ 5mA | 4.6 | 4.85 | 5.1 | V |

### 6.4.2. Shunt Regulator

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output voltage range accuracy (Fig. 6-1) | VPWR=23V, Ta= 25°C , 5V output | | | ±1.5 | % |
| | | VPWR=23V, Ta= 25°C, 3V ~ 21V output | | | ±2.5 | % |
| | | VPWR=23V, Ta= -20°C~ 105°C, 3V ~ 21V output | | | ±3.5 | % |
| $V_{PPS\_STEP}$ | PPS voltage step | | | 20 | | mV |
| $I_{PPS\_STEP}$ | PPS current limit step | $R_{SENSE}$=5mΩ, Av=80 | | 25 | | mA |
| $\Delta I_{PPS\_CL}$ | Current limit accuracy | 1A ≤ current limit ≤3A | | | ±150 | mA |
| | | current limit > 3A | | | ±5 | % |

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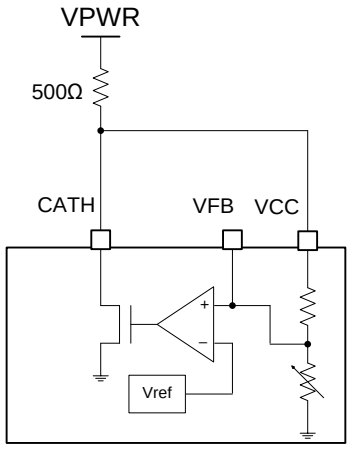


Figure 6-1 Test circuit of shunt regulator

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### 6.4.3. OVP and UVP

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OVP}$ | OVP voltage trip point | | 3 | | 25.5 | V |
| $V_{OVP\_STEP}$ | OVP voltage step | | | 0.1 | | V |
| $\Delta V_{OVP}$ | OVP trip point accuracy | | | | ±5 | % |
| $V_{UVP}$ | UVP voltage trip point | | 3 | | 25.5 | V |
| $V_{UVP\_STEP}$ | UVP voltage step | | | 0.1 | | V |
| $\Delta V_{OVP}$ | UVP trip point accuracy | | | | ±5 | % |

### 6.4.4. Over Current Protection

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{OCP}$ | OCP trip point | Rs=5mΩ, Av=80 | 0.5 | | 6.4 | A |
| $\Delta I_{OCP}$ | OCP accuracy | Rs=5mΩ, Av=80, $I_{OCP}$=3.6A | | | ±200 | mA |

### 6.4.5. ADC

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $N_{ADC}$ | ADC resolution | | | 10 | | Bit |
| $INL_{ADC}$ | ADC INL | Ta= 25°C, $V_{REF\_ADC}$ = 2.56V | | | ±5 | LSB |
| $DNL_{ADC}$ | ADC DNL | Ta= 25°C, $V_{REF\_ADC}$ = 2.56V | | | ±5 | LSB |
| $V_{REF\_ADC}$ | Reference voltage of ADC | Ta= 25°C, VCC=5V | | 2.56 | | V |

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### 6.4.6. CC1 and CC2

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH\_CC}$ | Output high voltage of BMC transmitter | | 1.05 | 1.125 | 1.2 | V |
| $V_{OL\_CC}$ | Output low voltage of BMC transmitter | | 0 | | 0.075 | V |
| $V_{IH\_CC}$ | Input high voltage of BMC receiver | | 0.67 | | 1.45 | V |
| $V_{IL\_CC}$ | Input low voltage of BMC receiver | | -0.25 | | 0.43 | V |
| $Z_{DRIVER\_CC}$ | BMC Transmitter output impedance | | 33 | | 75 | Ω |
| $Z_{BMCRX\_CC}$ | BMC Receiver Input impedance | | 1 | | | MΩ |
| $I_{RP\_CC}$ | CC1 and CC2 pull-up current | Capability 0.5A @5V | 64 | 80 | 96 | μA |
| | | Capability 1.5A @5V | 166 | 180 | 194 | μA |
| | | Capability 3.0A @5V | 304 | 330 | 356 | μA |
| $V_{Rd\_CC}$ | CC1 and CC2 attachment detection threshold | Capability 0.5A @5V | 1.5 | 1.6 | 1.65 | V |
| | | Capability 1.5A @5V | 1.5 | 1.6 | 1.65 | V |
| | | Capability 3.0A @5V | 2.45 | 2.6 | 2.75 | V |
| $R_{Rd\_CC}$ | CC1 and CC2 pull low resistor | | 4.59 | 5.1 | 5.61 | KΩ |

### 6.4.7. D+ and D-

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{DAT\_REF}$ | Data detect voltage | | 0.25 | 0.35 | 0.4 | V |
| $V_{SEL\_REF}$ | Output selection reference | | 1.8 | 2.0 | 2.2 | V |
| $R_{DWN}$ | D- pull down resistance | | 14.25 | 15 | 15.75 | KΩ |
| $R_{DCP\_DAT}$ | D+ to D- resistance during DCP mode | | | 30 | 40 | Ω |
| $R_{DAT\_LKG}$ | D+ leakage resistance | | 300 | 710 | 1500 | KΩ |

### 6.4.8. Temperature Sensor

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{OTP}$ | OTP Current Source | | 19.475 | 20.5 | 21.525 | μA |

### 6.4.9. On-chip Temperature Sensor

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $T_{TS}$ | Internal temperature sensor accuracy | | | | ±10 | °C |

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### 6.4.10. GPIO

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OL\_GPIO4m}$ | Output Low Voltage of GPIO1, GPIO6, GPIO7 and GPIO8 | $I_{OL}$ = 4mA | | | 0.4 | V |
| $V_{OL\_GPIO10m}$ | Output Low Voltage of GPIO0, GPIO3, GPIO9, GPIOB, GPIOC and GPIOD | $I_{OL}$ = 10mA | | | 0.4 | V |
| $V_{OL\_GPIO2}$ | Output Low Voltage of GPIO2 | $I_{OL}$ = 5mA | | | 4 | V |
| $I_{Z\_GPIO}$ | Leakage current of GPIO in Hi-Z | | | | 10 | µA |
| $V_{IH}$ | Input High voltage | GPIO1, GPIO6, GPIO7, GPIO8 | 1.5 | | 4.5 | V |
| | | GPIO0, GPIO2, GPIO3, GPIO4, GPIO5, GPIO9, GPIOB, GPIOC, GPIOD | 1.4 | | VCC | V |
| $V_{IL}$ | Input low voltage | GPIO1 | 0 | | 1.0 | V |
| | | Others GPIOx | 0 | | 0.8 | V |

## 6.5. AC Characteristics (VCC=20V, Ta= -20°C to +105°C, unless specified)

### 6.5.1. Internal Oscillator

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{OSC}$ | Main oscillator frequency | | 9.5 | 10 | 10.5 | MHz |
| $f_{LFOSC}$ | Low frequency oscillator frequency | | 45.5 | 65 | 84.5 | KHz |

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### 6.5.2. USB-PD BMC Transmitter and Receiver

| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{BMC}$ | BMC signal bit rate | | 270 | 300 | 330 | KHz |
| $t_{RISE\_BMC}$ | BMC signal Tx rise time | | 300 | | | ns |
| $t_{FALL\_BMC}$ | BMC signal Tx fall time | | 300 | | | ns |
| $t_{HOLD\_BMC}$ | Time to cease driving the line after the final high-to-low transition | | 1 | | | µs |
| $t_{IFG\_BMC}$ | Time from the end of last bit of a Frame until the start of the first bit of the next Preamble | | 25 | | | µs |
| $t_{END\_BMC}$ | Time to cease driving the line after the end of the last bit of the Frame | | | | 23 | µs |
| $t_{RXFTR\_BMC}$ | BMC receiver bandwidth limiting filter | | 100 | | | ns |
| $t_{NILDLE\_BMC}$ | Time window for detecting non-idle | | 12 | | 20 | µs |
| $N_{NIDLE\_BMC}$ | Number of transitions to be detected to declare bus non-idle | | 3 | | | |

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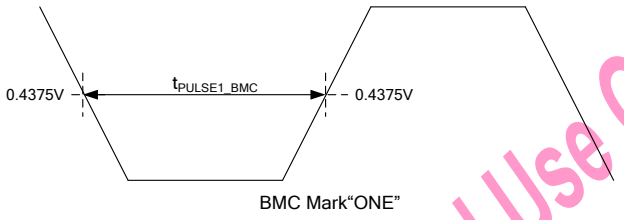
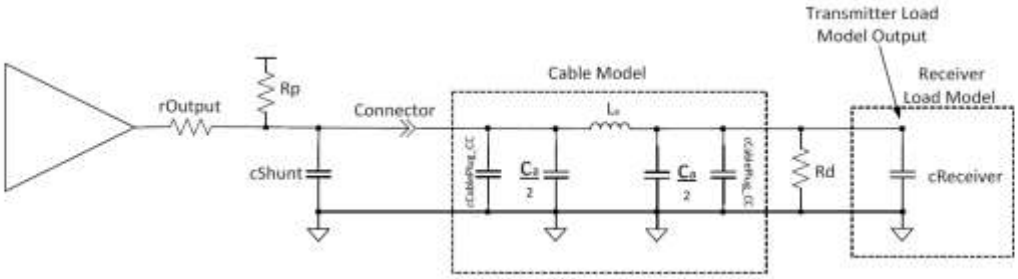
| Parameter | | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PULSE1\_BMC}$ | Pulse width of transmitted BMC "ONE" signal *(1) | Ta = 25°C, CC total Capacitance =1010pF *(2) *(3), CC pin series resistance =47ohm | 1.4 | | 1.8 | µs |

*(1) Pulse width of transmitted BMC "ONE" signal



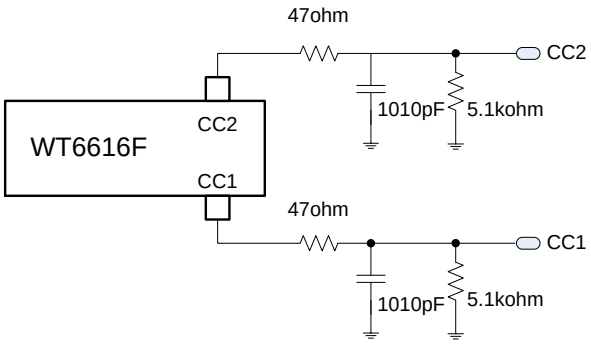
BMC Mark"ONE"

*(2) Reference to USB Power Delivery Specification Revision 3.0. The cShunt=560pF is used and assumes cReceiver is minimum value 200pF, and Cable Model provide 250pF.



Transmitter Load Model for BMC Tx

*(3) Pulse width of transmitted BMC "ONE" signal test circuit

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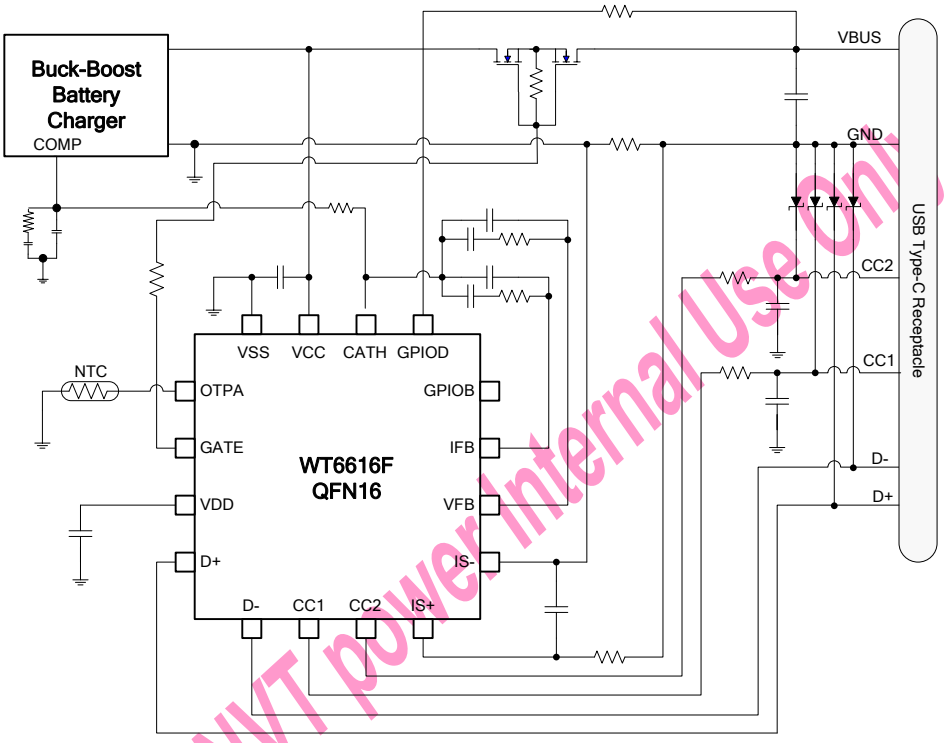
# 7. Examples of Application

## 7.1. USB PD 3.0 Power Banks

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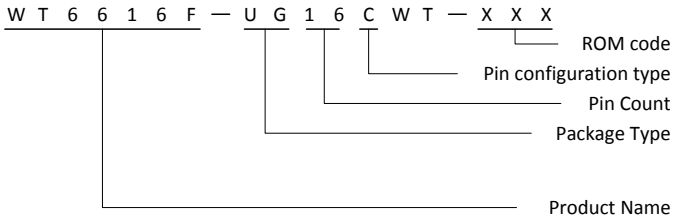
# 8. Ordering Information

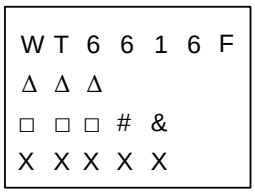
| Package Type | Package Outline | Part Number | Ordering Number | Note |
|---|---|---|---|---|
| 16-pin QFN | 5mm x 5mm | WT6616F | WT6616F-UG16CWT-XXX | - |

Note: suffix number number-XXX for difference Firmware code, please refer to Firmware control list.

**Example:**




**Top Mark**




Δ ROM Code
□ Date Code
# FW Version Code
& Pin configuration type
X Production Tracking code

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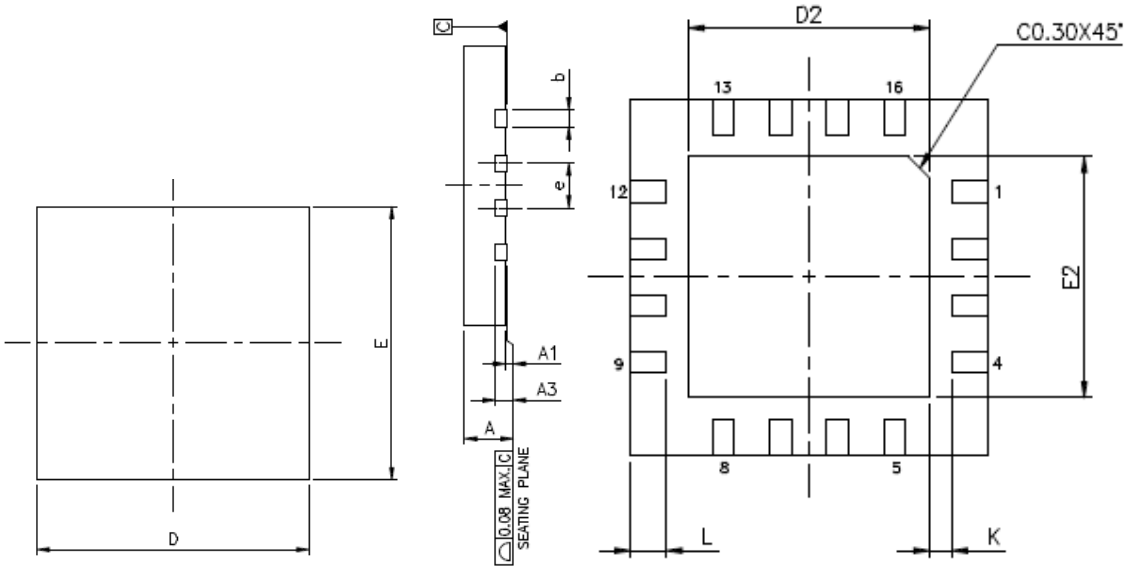
# 9. Package Information

## 9.1. Package Dimension

### 5.1.5. 16-pin QFN




All dimensions shown in mm

| SYMBOL | MIN | NOR | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 | |
| b | 0.25 | 0.30 | 0.35 |
| D | 4.95 | 5.00 | 5.05 |
| E | 4.95 | 5.00 | 5.05 |
| e | | 0.80 | |
| K | 0.20 | - | - |
| L | 0.45 | 0.50 | 0.55 |
| D2 | 3.28 | 3.38 | 3.43 |
| E2 | 3.28 | 3.38 | 3.43 |

**Note:**

1. Dimension “b” applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.

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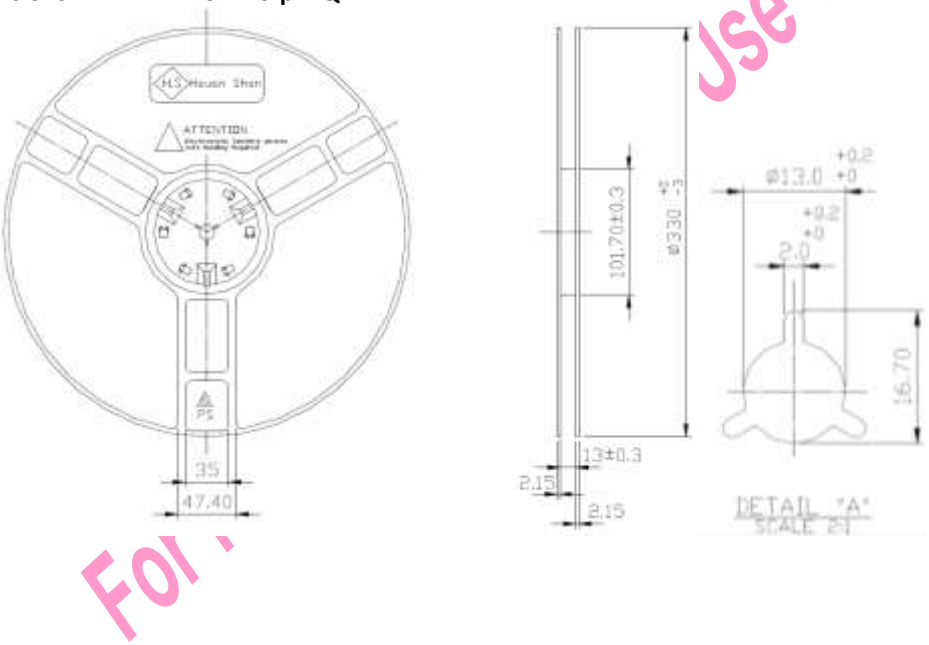
## 9.2. Product Tube and Tapping Specification

| Package Type | EA/TRAY | TRAY/BOX | EA/BOX | Tapping (EA/Reel) |
|---|---|---|---|---|
| 16-pin QFN (5x5mm) | 490 | 10 | 4900 | 5000 |

### 9.2.1 Reel Dimensions

**(1) Reel Dimensions: W=12mm for "16-pin QFN".**

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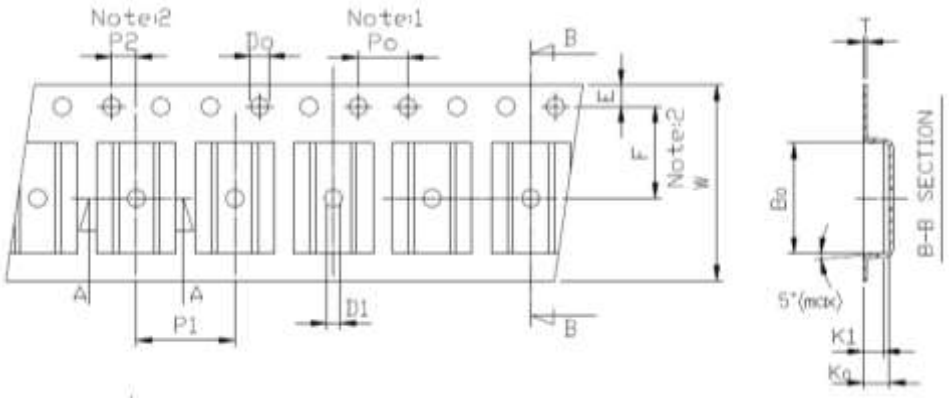
### 9.2.2 Carrier Tape Dimensions

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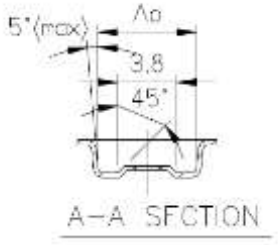


**Notes:**
1. 10 Sprocket hole pitch cumulative tolerance is ±0.1mm
2. Pocket position relative to sprocket hole measured as true position of packet not pocket hole.
3. $A_O$ and $B_O$ measured on a plane 0.3mm above the bottom of the pocket to the top surface of the carrier.
4. $K_O$ measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100 mm through a length of 250 mm.

Unit: mm

| Symbol | 16-pin QFN (5mmx5mm) |
|---|---|
| $A_O$ | 5.25 ± 0.10 |
| $B_O$ | 5.25 ± 0.10 |
| $K_O$ | 1.25 ± 0.10 |
| K1 | - |
| $P_O$ | 4.00 ± 0.10 |
| P1 | 8.00 ± 0.10 |
| P2 | 2.00 ± 0.05 |
| $D_O$ | 1.55 ± 0.05 |
| D1 | 1.50 (MIN) |
| E | 1.75 ± 0.10 |
| F | 5.50 ± 0.05 |
| $10P_O$ | 40.0 ± 0.10 |
| W | 12.0 ± 0.20 |
| T | 0.30 ± 0.05 |

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## 10. Revision History

| Version | Contents of Change | Date |
|---|---|---|
| 0.90 | Initial issue | March 19, 2019 |

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