Table of Contents

1	Title page
2	Notes
3	Block Diagram
4	TOP
5	CPU_Interfaces
6	DDR2 & Flash
7	PERIPHERALS
8	CPU Power
9	ELEVATOR CONNECTORS
10	OSBDM
11	Power from OSBDM

Revisions

Rev	Description	Date	Designer
A	Original Release	8/1/2009	Swann Zhou
B	Modify according to ECR	11/18/2009	Swann Zhou
B1	Revise	5/18/2010	Jun Qiao
B2	Revise	5/20/2010	Jun Qiao
B3	Revise	5/26/2010	Jun Qiao
B4	Revise	6/8/2010	Jun Qiao
B5	Revise	6/9/2010	Jun Qiao
B6	Revise	6/17/2010	Jun Qiao
C	Release	6/21/2010	Jun Qiao
C1	Revise	7/23/2010	Jun Qiao

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Designer: Jim Williams	Drawing Title: **TWR-MCF5441X**	
Drawn by: Jun Qiao	Page Title: **TITLE PAGE**	
Approved:	Size C / Document Number SCH-26131 PDF: SPF-26131	Rev C1
	Date: Friday, July 23, 2010	Sheet 1 of 11

1. Unless Otherwise Specified:

   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:

   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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Drawing Title:

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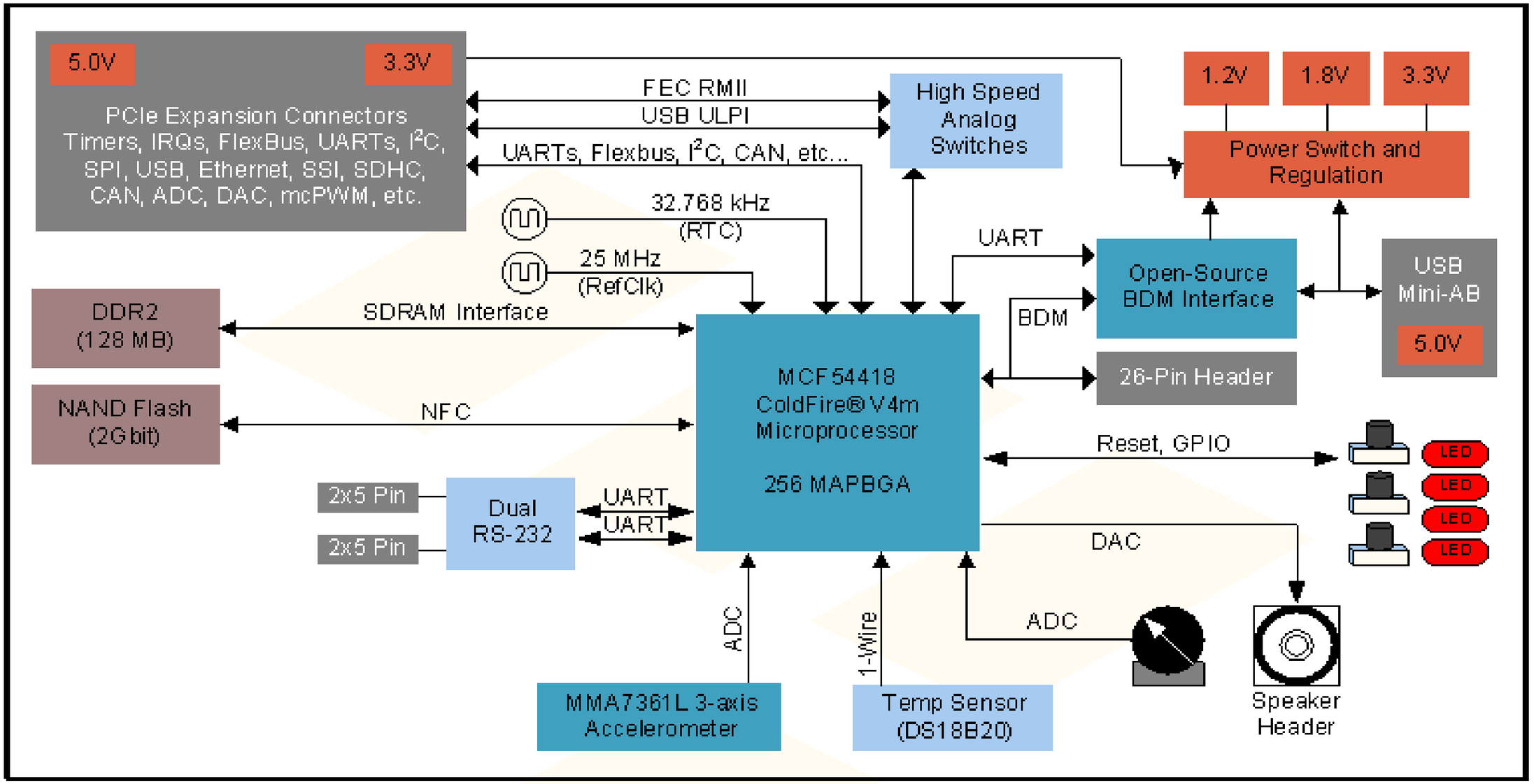
Page Title:

NOTES

Size	Document Number	Rev
C	SCH-26131 PDF: SPF-26131	C

Date: Tuesday, June 22, 2010 Sheet 2 of 11



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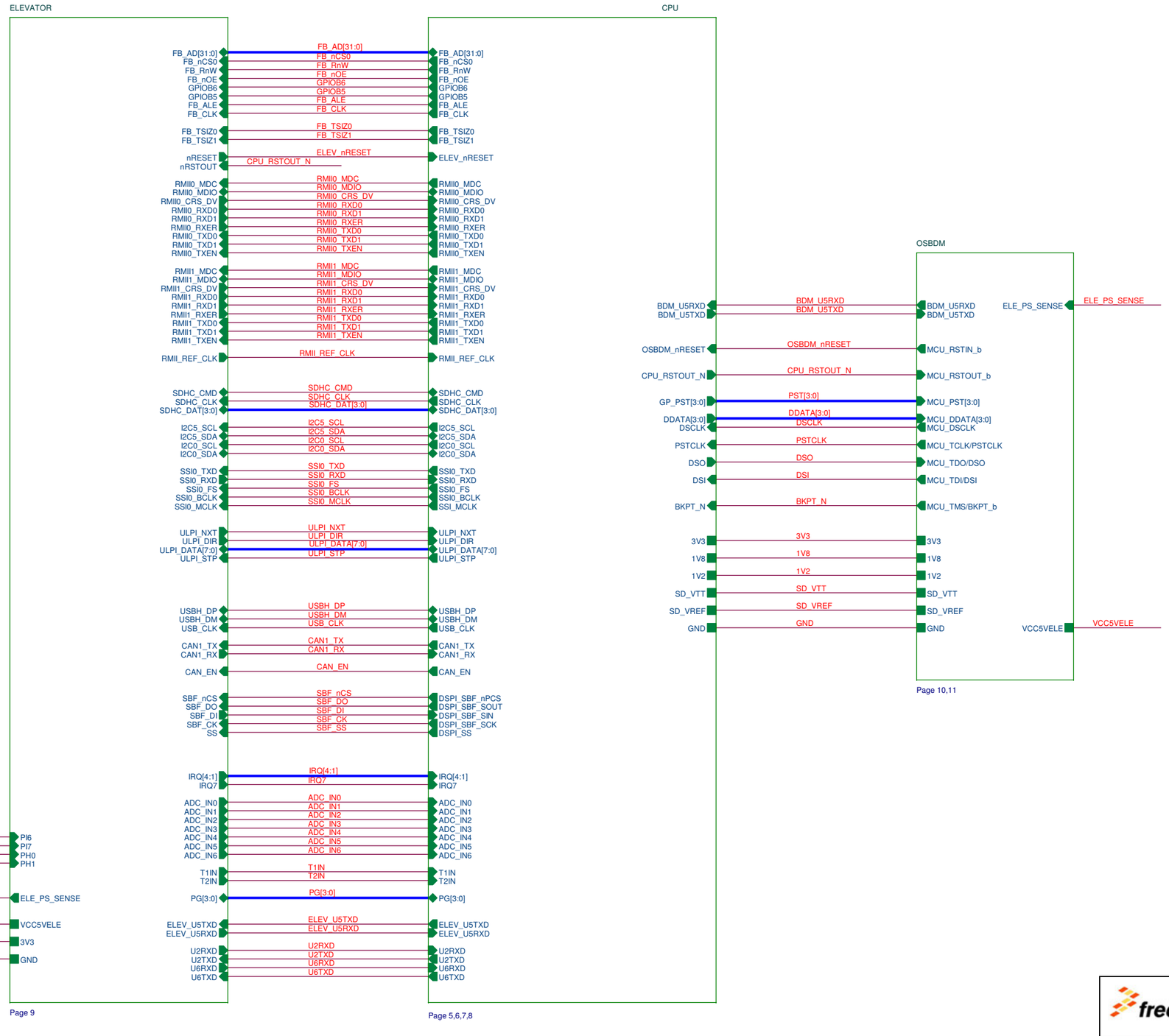
Page Title: **Block Diagram**

Size	Document Number	Rev
C	SCH-26131 PDF: SPF-26131	C

Date: Tuesday, June 22, 2010 Sheet 3 of 11



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Drawing Title:

TWR-MCF5441X

Page Title:

TOP

Size	Document Number	Rev
C	SCH-26131 PDF: SPF-26131	C1

Date: Friday, July 23, 2010 Sheet 4 of 11

U17
QS3VH16233PAG
16:32
(SEL Pin:
0:RMII1;
1:ULPI)
R137 4.7K
R123 22
C138 C128
0.01UF 0.1UF
R141 4.7K
R125 4.7K
R126 22
R140 22
R139 22
ULPI_DATA[7:0]

U4A
MCF54418

C10 3300pF
C18 3300pF
C21 3300pF
C26 3300pF
C23 3300pF
C11 3300pF
C6 3300pF
CT3
CT6
CT9
CT14
CT15
P_ADC_IN0
P_ADC_IN1
P_ADC_IN2
P_ADC_IN4
ADC_IN3
ADC_IN5
ADC_IN6
ACCX
ACCY
ACCZ
POT

R35 4.7K
J6 HDR 1X2 TH
(JTAG_EN: 0: JTAG; 1:BDM)
R30 0
R32 0
R8 R27 R104 R105 R106 4.7K
R1 R2 4.7K
R103 R102 4.7K
U5 DS18B20
R113 4.7K
C22 0.1UF
R145 22
R3 22
R4 22
R5 22
R14 22
R24 1.0M
X1 25MHZ
C17 33PF
C16 33PF
R12 1.0M DNP
Y1 32.768KHz
C4 18PF
C7 18PF
R28 R26 4.7K
R76 R75 22
R55 22
R69 R68 R66 R47 R45 R67 22
R43 R40 R46 22
R52 R51 R73 R50 R49 R53 R72 R74 22
R70 R71 22
R63 R64 22
R61 R38 R36 R57 R48 R37 R60 R59 R62 R58 R56 R41 R39 R42 R65 22
R10 R9 33
J2 HDR TH 1X3
(Default: shunt 2&3)

J5 HDR 2X2
(BOOT MODE Setting)
R33 R54 4.7K
(Default: shunt 3,4)

BOOTMOD[1:0]	Meaning
00	Boot from FlexBus with defaults
01	Override defaults and RCON decides boot source (FlexBus or NAND flash)
1x	Override defaults and boot from serial boot facility with optional load to and boot from RAM. if not booting from RAM, RCON decides the boot source (FlexBus or NAND flash)

CT1
CT2
U5TXD
U5RXD
ELEV_U5TXD
BDM_U5TXD
ELEV_U5RXD
BDM_U5RXD

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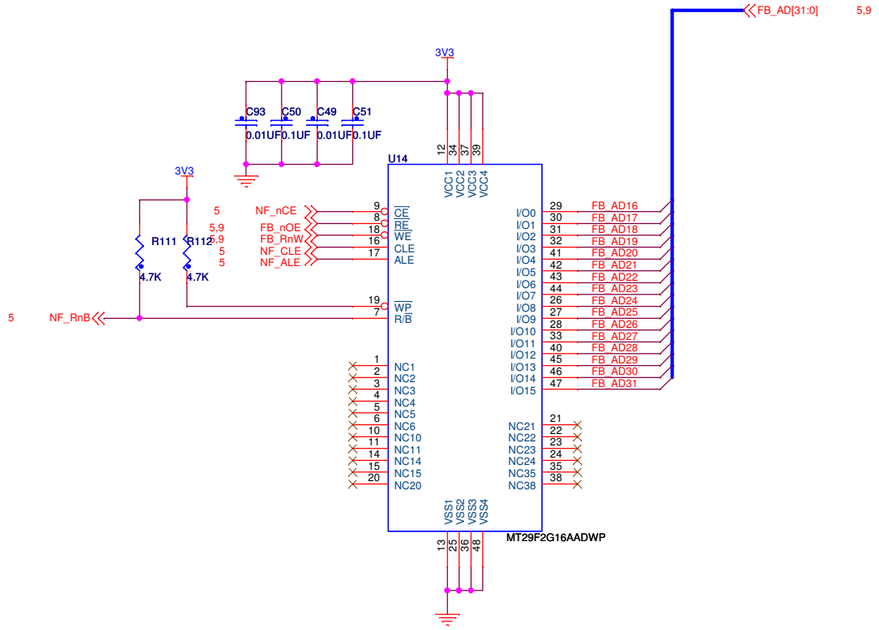
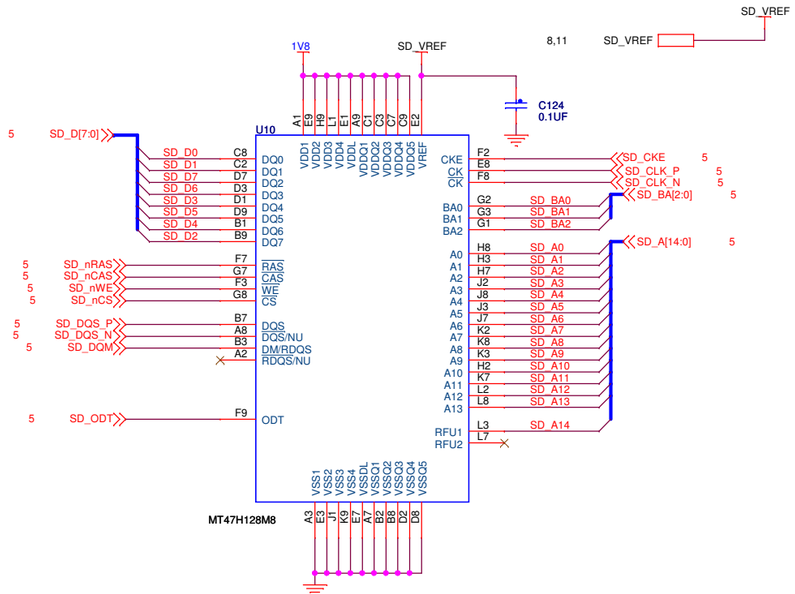
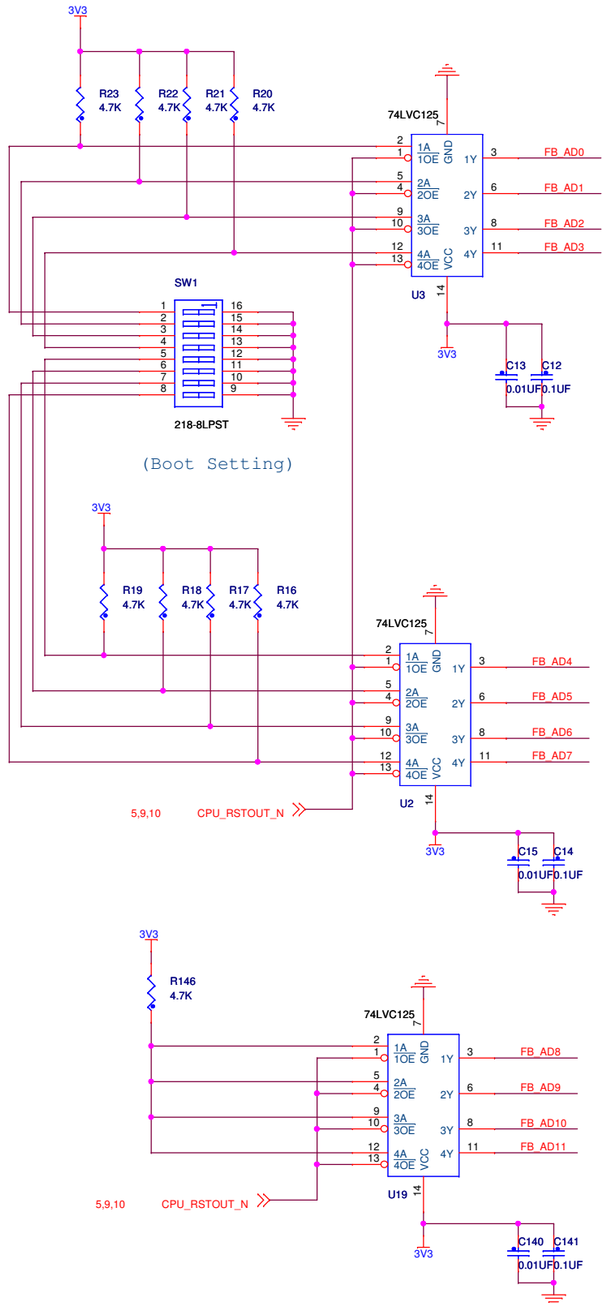
Drawing Title:
TWR-MCF5441X
Page Title:
MCF5441X
Size C | Document Number SCH-26131 PDF: SPF-26131 | Rev C1
Date: Friday, July 23, 2010 | Sheet 5 of 11







Parallel Configuration During Reset when BootMod[1:0]= 01	
Override Pins in Reset	Function
FB_AD0	Boot memory
0	NAND flash
1	FlexBus
FB_AD1	PLL mode
0	Disabled
1	Enabled
FB_AD2	Oscillator mode
0	Crystal oscillator mode
1	Oscillator bypass mode
FB_AD3	FB_ALE select
0	FB_TS_B
1	FB_ALE
FB_AD[5:4]	BOOT Port Size
00	32-bit(32-bit muxed address)
01	8-bit(24-bit non-muxed address)
10	16-bit(16-bit non-muxed address)
11	16-bit(16-bit non-muxed address)
FB_AD[7:6]	PLL Multiplier
00	Fvco = 10 x Fref
01	Fvco = 15 x Fref
10	Fvco = 16 x Fref
11	Fvco = 20 x Fref

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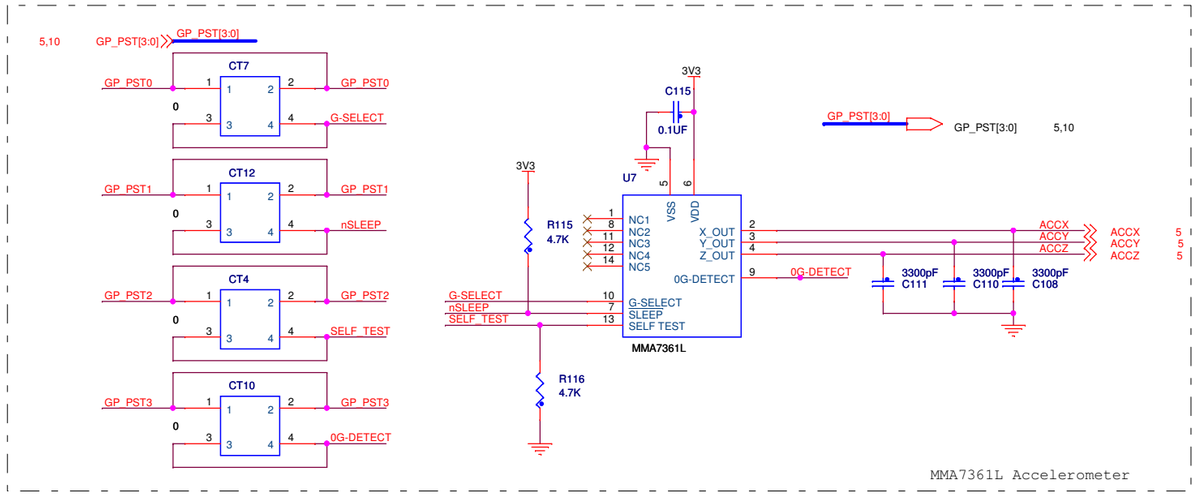
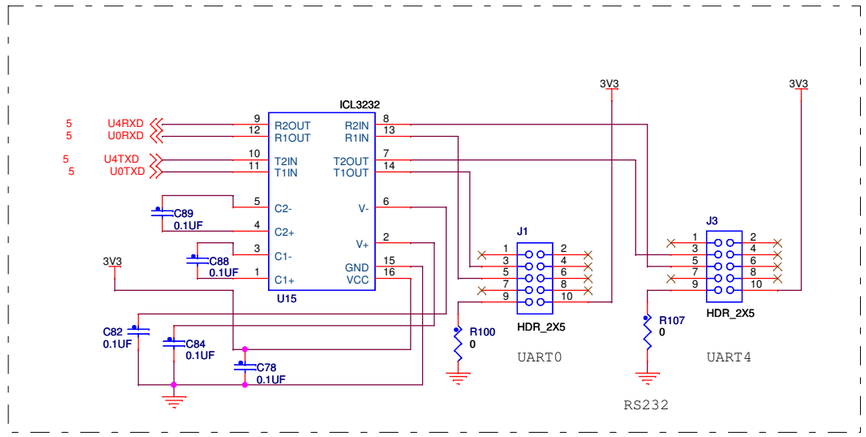
Drawing Title: **TWR-MCF5441X**

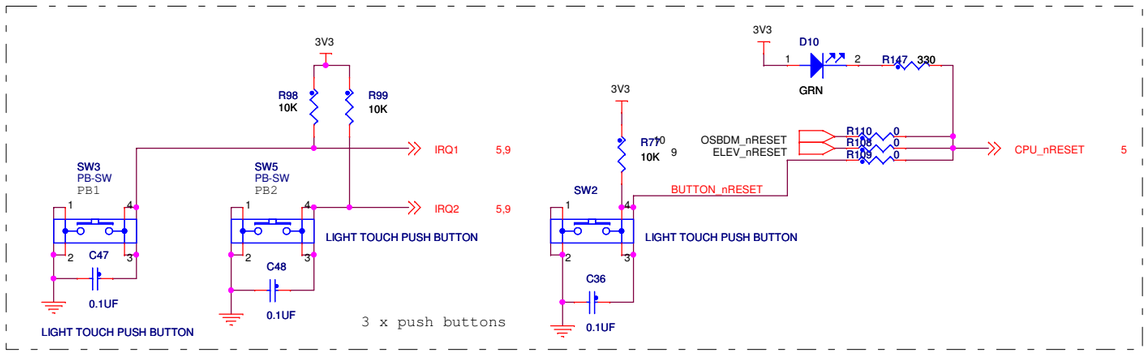
Page Title: **DDR2 & Flash**

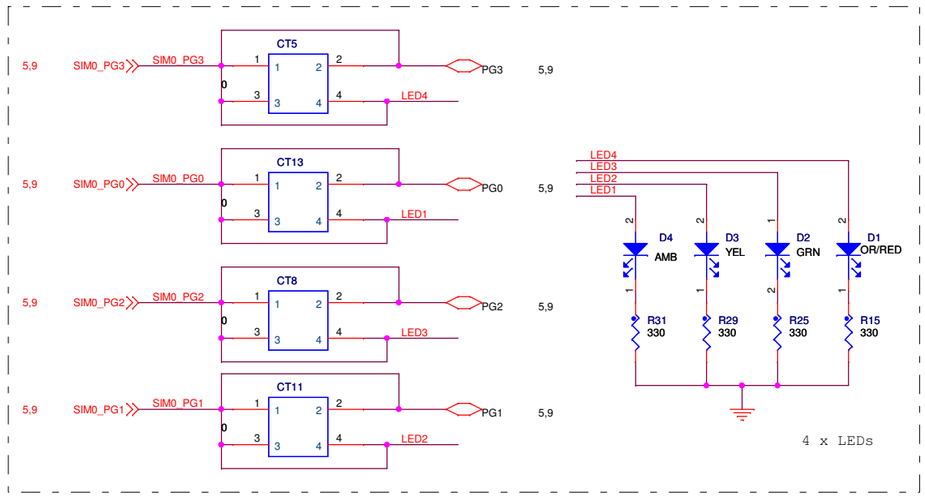
Size	Document Number	Rev
C	SCH-26131 PDF: SPF-26131	C

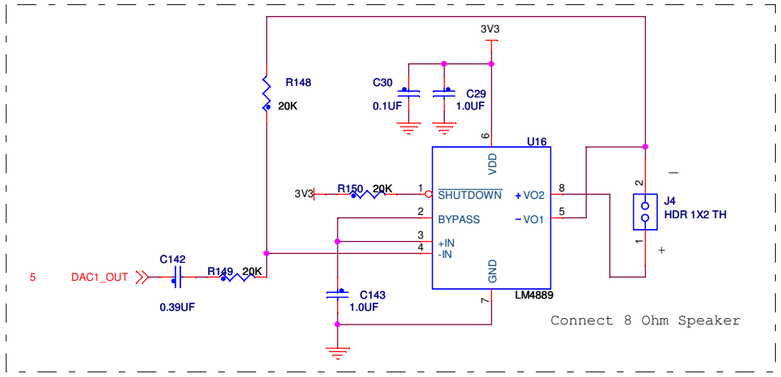
Date: Friday, July 23, 2010 Sheet 6 of 11

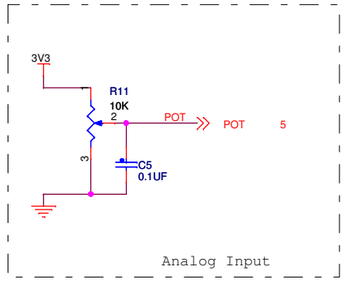












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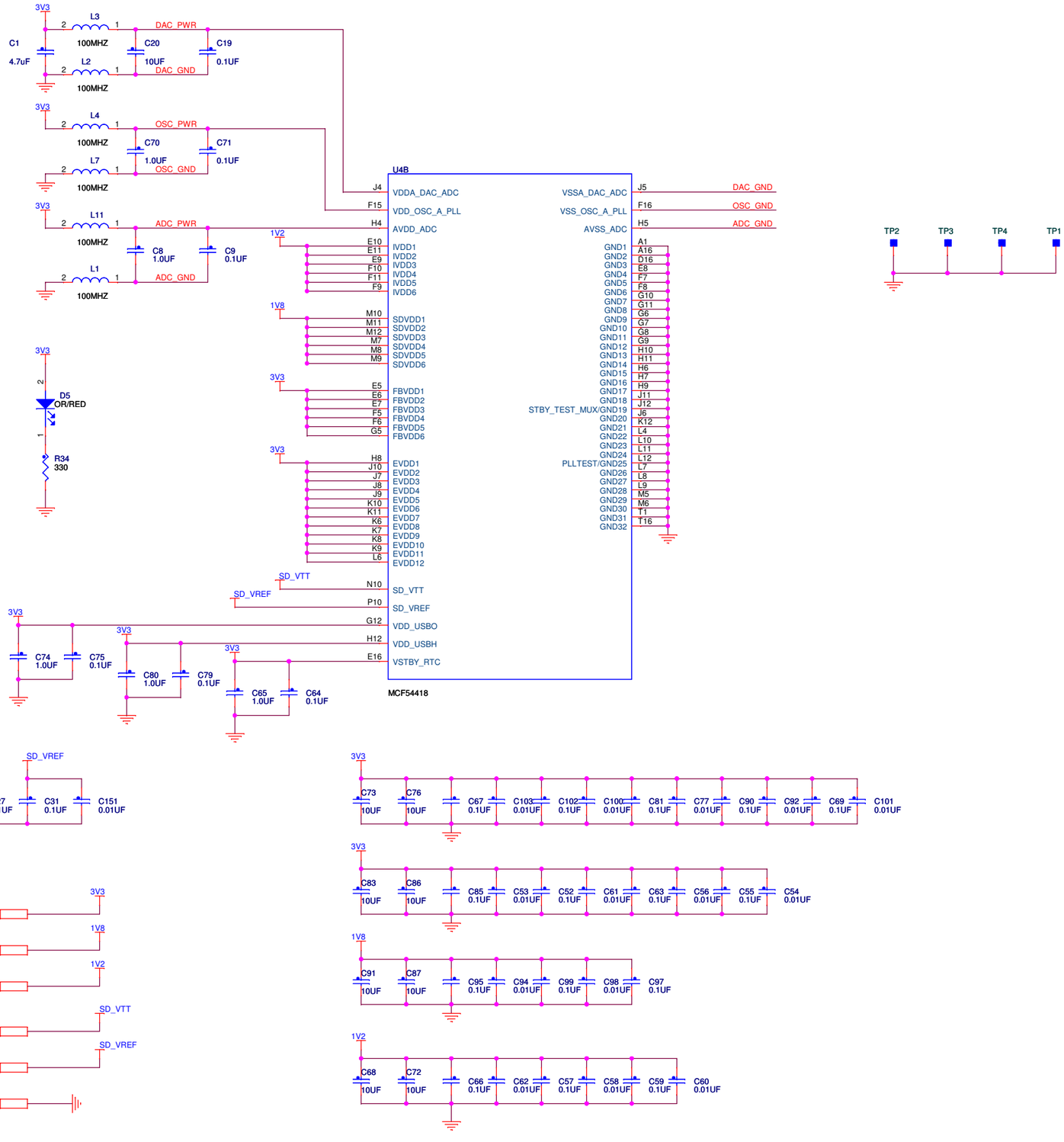
Drawing Title: **TWR-MCF5441X**

Page Title: **PERIPHERALS**

Size	Document Number	Rev
C	SCH-26131 PDF: SPF-26131	C

Date: Friday, July 23, 2010 Sheet 7 of 11



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Drawing Title:

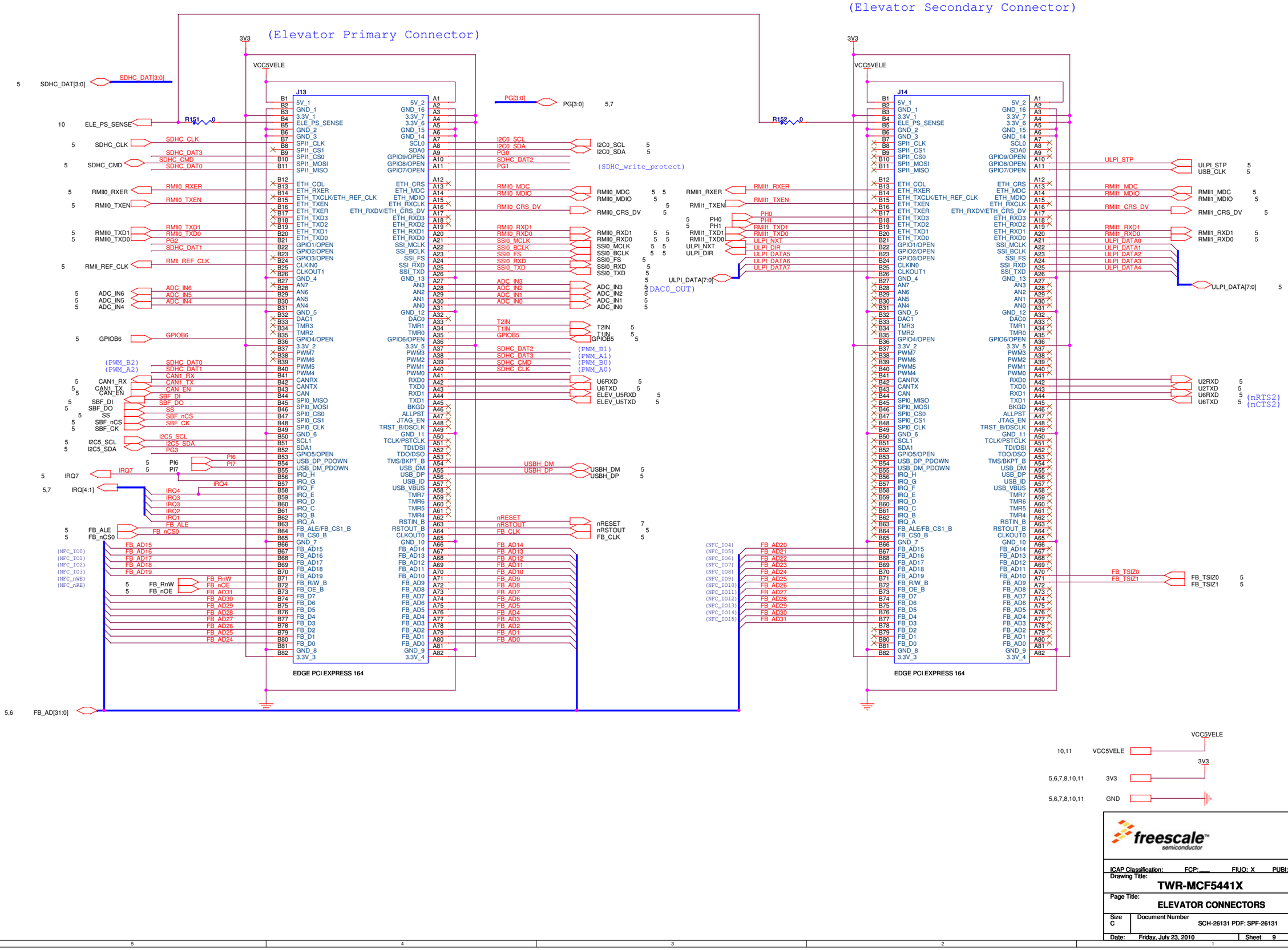
TWR-MCF5441X

Page Title:

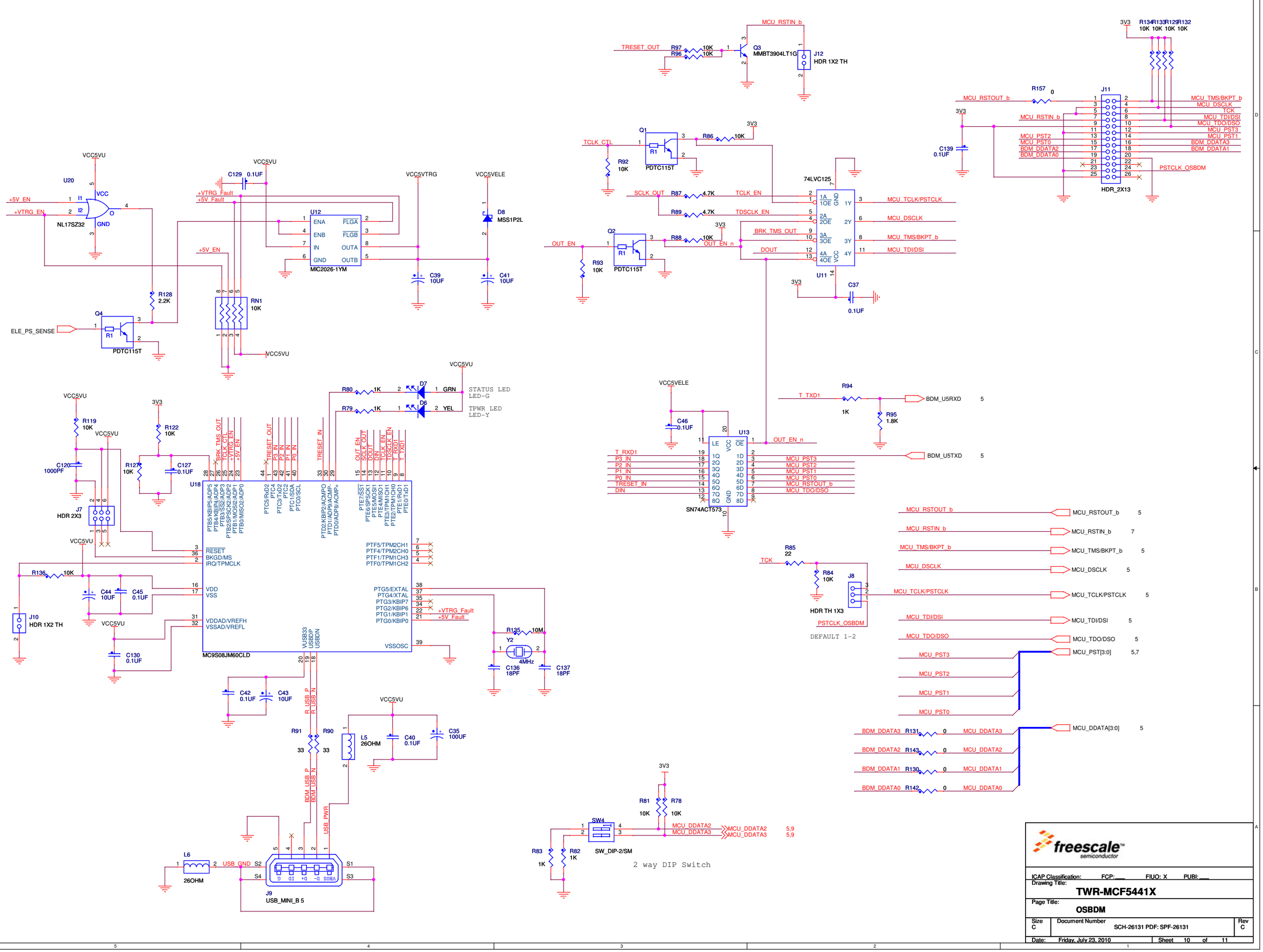
CPU_POWER

Size	Document Number	Rev
C	SCH-26131 PDF: SPF-26131	C

Date: Friday, July 23, 2010 Sheet 8 of 11



ICAP Classification:	FCP:___ FIUO: X PUBI:___
Drawing Title:	TWR-MCF5441X
Page Title:	ELEVATOR CONNECTORS
Size: C	Document Number: SCH-26131 PDF: SPF-26131
Rev: C1	
Date: Friday, July 23, 2010	Sheet 9 of 11


U20
VCC5VU
+5V_EN
+VTRG_EN
NL17SZ32
R128 2.2K
Q4
ELE_PS_SENSE
PDTC115T
C129 0.1UF
+VTRG_Fault
+5V_Fault
U12
MIC2026-1YM
VCC5VTRG
VCC5VELE
D8
MSS1P2L
C39 10UF
C41 10UF
RN1 10K
R119 10K
R122 10K
R127 10K
C120 1000PF
C127 0.1UF
3V3
J7
HDR 2X3
R136 10K
C44 10UF
C45 0.1UF
J10
HDR 1X2 TH
C130 0.1UF
U18
MC9S08JM60CLD
RESET
BKGD/MS
IRQ/TPMCLK
VDD
VSS
VDDAD/VREFH
VSSAD/VREFL
VUSB33
USBDP
USBDN
VSSOSC
PTF5/TPM2CH1
PTF4/TPM2CH0
PTF1/TPM1CH3
PTF0/TPM1CH2
PTG5/EXTAL
PTG4/XTAL
PTG3/KBIP7
PTG2/KBIP6
PTG1/KBIP1
PTG0/KBIP0
R135 10M
Y2
4MHz
C136 18PF
C137 18PF
C42 0.1UF
C43 10UF
R91 33
R90 33
L5 26OHM
C40 0.1UF
C35 100UF
L6
26OHM
J9
USB_MINI_B 5
R80 1K
R79 1K
D7
GRN
D6
YEL
STATUS LED
LED-G
TPWR LED
LED-Y
MCU_RSTIN_b
TRESET_OUT
R97 10K
R96 10K
Q3
MMBT3904LT1G
J12
HDR 1X2 TH
TCLK_CTL
R92 10K
Q1
PDTC115T
R86 10K
SCLK_OUT
R87 4.7K
R89 4.7K
TCLK_EN
TDSCLK_EN
OUT_EN
R93 10K
Q2
R88 10K
OUT_EN_n
BRK_TMS_OUT
DOUT
74LVC125
U11
MCU_TCLK/PSTCLK
MCU_DSCLK
MCU_TMS/BKPT_b
MCU_TDI/DSI
C37 0.1UF
C46 0.1UF
U13
SN74ACT573
T_RXD1
P3_IN
P2_IN
P1_IN
P0_IN
TRESET_IN
DIN
MCU_PST3
MCU_PST2
MCU_PST1
MCU_PST0
MCU_RSTOUT_b
MCU_TDO/DSO
R94
1K
R95 1.8K
T_TXD1
BDM_U5RXD
BDM_U5TXD
SW4
SW_DIP-2/SM
2 way DIP Switch
R81 10K
R78 10K
R83 1K
R82 1K
R134 10K
R133 10K
R129 10K
R132 10K
R157 0
J11
HDR_2X13
C139 0.1UF
MCU_RSTOUT_b
MCU_RSTIN_b
MCU_TMS/BKPT_b
MCU_DSCLK
MCU_TCLK/PSTCLK
MCU_TDI/DSI
MCU_TDO/DSO
MCU_PST[3:0]
MCU_DDATA[3:0]
R85 22
R84 10K
J8
HDR TH 1X3
PSTCLK_OSBDM
DEFAULT 1-2
BDM_DDATA3 R131 0
BDM_DDATA2 R143 0
BDM_DDATA1 R130 0
BDM_DDATA0 R142 0
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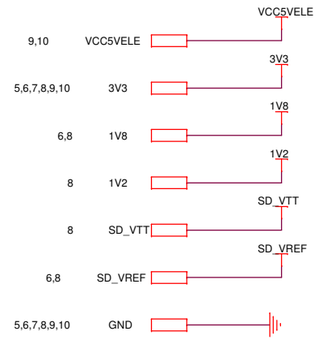
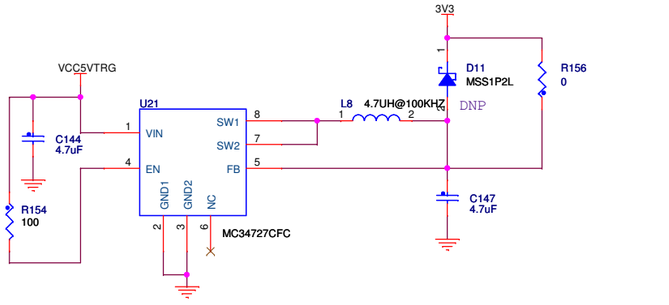
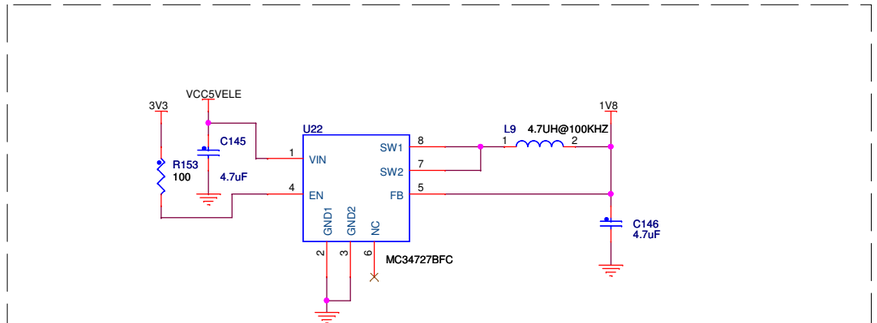
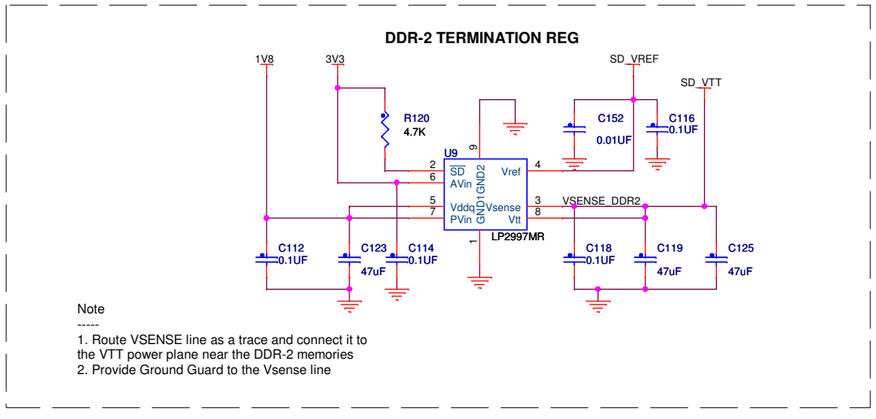
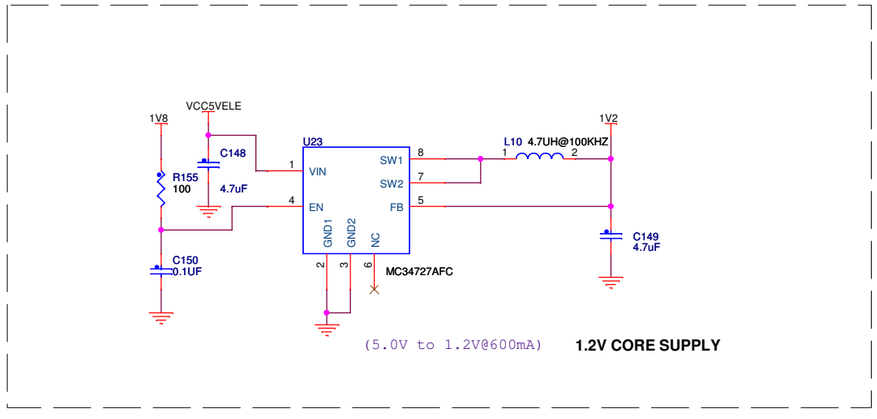
ICAP Classification: FCP: ___ FIUO: X PUBI: ___
Drawing Title: TWR-MCF5441X
Page Title: OSBDM
Size C
Document Number SCH-26131 PDF: SPF-26131
Rev C
Date: Friday, July 23, 2010
Sheet 10 of 11











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Drawing Title:

TWR-MCF5441X

Page Title:

Power from OSBDM

Size	Document Number	Rev
C	SCH-26131 PDF: SPF-26131	C

Date: Friday, July 23, 2010 Sheet 11 of 11