MCF5441*x* ColdFire® Microprocessor Product Brief

Supports MCF54410, MCF54415, MCF54416, MCF54417, & MCF54418

by: Microcontroller Solutions Group

The MCF5441*x* devices are a family of highly-integrated 32-bit microprocessors based on the Version 4m ColdFire microarchitecture, comprising of the V4 integer core, memory management unit (MMU) and enchanced multiply-accumulate unit (EMAC). This product line is well-suited for processing data from and moving data between a variety of common serial interfaces (CAN, I2C, SSI, SPI, UART, and USB) and Ethernet networks, especially for factory automation, process control, and motor control applications. Support for low-cost memory and connectivity options also make this family ideal for a range of consumer digital lifestyle products.

All MCF5441*x* devices operate at up to 250 MHz and include 64 Kbytes of single-cycle SRAM, memory controllers for DDR2 SDRAM and NAND flash, the highly configurable FlexBus for interfacing components like NOR flash, SRAM, and programmable logic devices (FPGAs and CPLDs), a 64-channel DMA controller, and serial memory boot and configuration support.

Communications peripheral interfaces include: USB host and On-the-Go controllers with integrated full-speed/low-speed transceivers and a switchable port

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for an external ULPI high-speed PHY, dual smart card ports, an enhanced controller for MMC, MMCplus, SD, and SDHC memory cards, dual CAN modules, a pair of synchronous serial interfaces, a 1-wire interface for low speed communication to devices (thermostats, batteries, etc.) and a maximum of ten UARTs, six I2C controllers, and four DMA serial peripheral interfaces.

Unique to the MCF5441*x* family is a flexible 10/100 Mbps Ethernet subsystem configurable as: a single media access controller (MAC) with a media independent interface (MII) or reduced MII (RMII), a pair of MACs with dual RMIIs, or, on specific devices, as a 3-port switch with two external ports and the third port internally connected to the processor. The Ethernet MACs incorporate hardware CRC checking/generation and Magic Packet power management. The entire Ethernet subsystem supports the IEEE 1588-2002 standard, a precision clock synchronization protocol for networked measurement and control systems. Certain MCF5441*x* family members also include the cryptographic acceleration unit (CAU), a CPU coprocessor for the DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms implemented in network security protocols like SSL and IPsec.

Additional features include four 32-bit timers that can optionally be linked to the Ethernet subsystem's IEEE 1588 timestamp logic for network-triggered event recognition and generation, a flexible multi-channel pulse width modulation timer suitable for motor control which can also be linked to the IEEE 1588 timestamp logic for synchronizing motors through Ethernet, a fast, 12-bit analog-to-digital converter (ADC) with 8-shared input channels capable of simultaneous parallel conversions, and two 12-bit digital-to-analog converters (DACs). The standard 17 mm × 17 mm 256-ball MAPBGA package has a 1 mm ball pitch and can be escape-routed on 4-layer printed circuit boards.

This document provides an overview of the MCF5441*x* family and focuses on its diverse feature set. It covers the MCF54418 superset device but is applicable to all derivative family members.

1 Application Examples

The MCF5441*x* family is well suited for consumer and industrial applications that require a broad range of peripherals and high performance. As shown in the following examples, this microprocessor is central to the application design and provides the flexibility to add or remove peripheral components as needed.

1.1 Device Server and PLC Application

Figure 1 shows the MCF5441*x* used in a device server and PLC application.

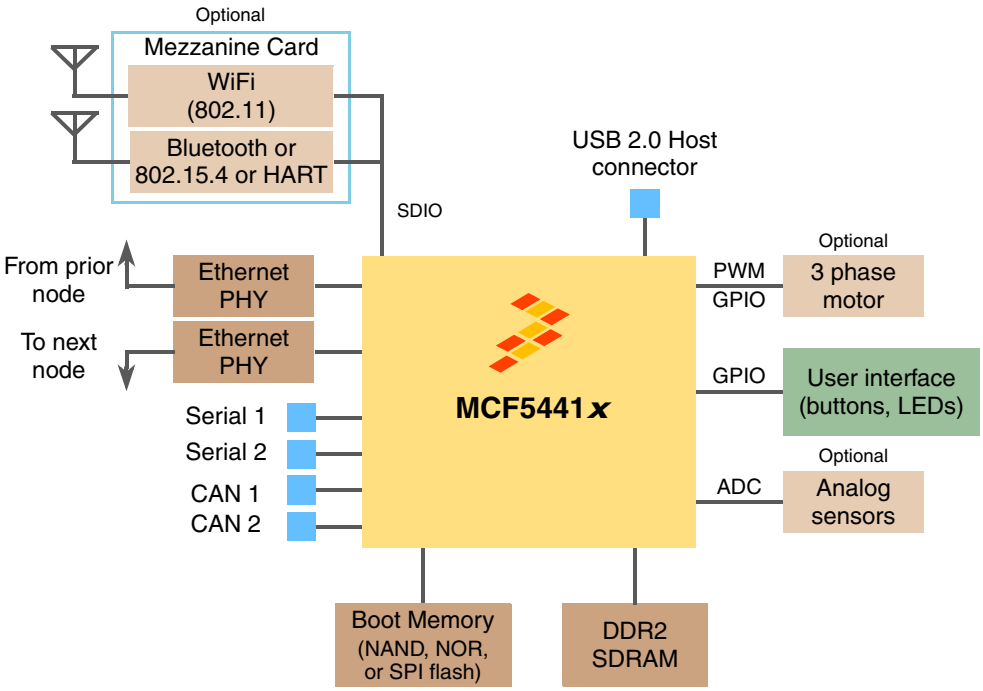


Figure 1. Device Server and PLC Application Example

1.2 Elevator Controller Application

Figure 2 shows the MCF5441*x* in an elevator controller with voice and video capability.

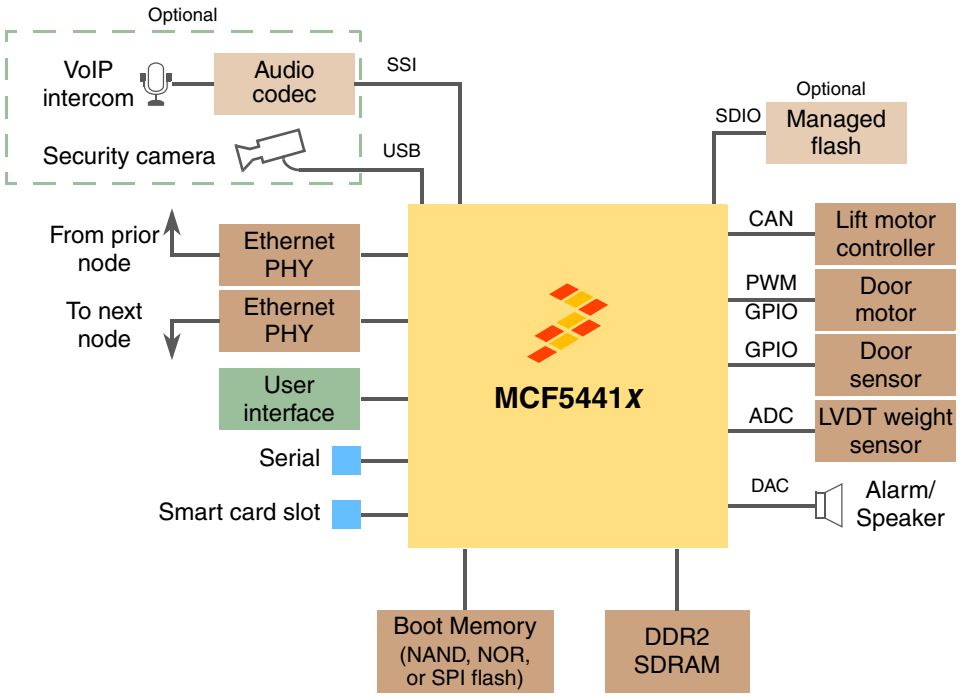


Figure 2. Elevator Controller Application Example

2 Features

2.1 MCF5441*x* Family Comparison

The following table compares the various device derivatives available within the MCF5441*x* family.

Table 1. MCF5441*x* Family Configurations

Module	MCF54410	MCF54415	MCF54416	MCF54417	MCF54418
Version 4 ColdFire core with EMAC (enhanced multiply-accumulate unit) and MMU (memory management unit)	•	•	•	•	•
Cryptography acceleration unit (CAU)	—	—	•	—	•
Core (system) and SDRAM clock	up to 250 MHz				
Peripheral clock (Core clock ÷ 2)	up to 125 MHz				
External bus (FlexBus) clock	up to 100 MHz				
Performance (Dhrystone 2.1 MIPS)	up to 385				
Static RAM (SRAM)	64 Kbytes				

Table 1. MCF5441*x* Family Configurations (continued)

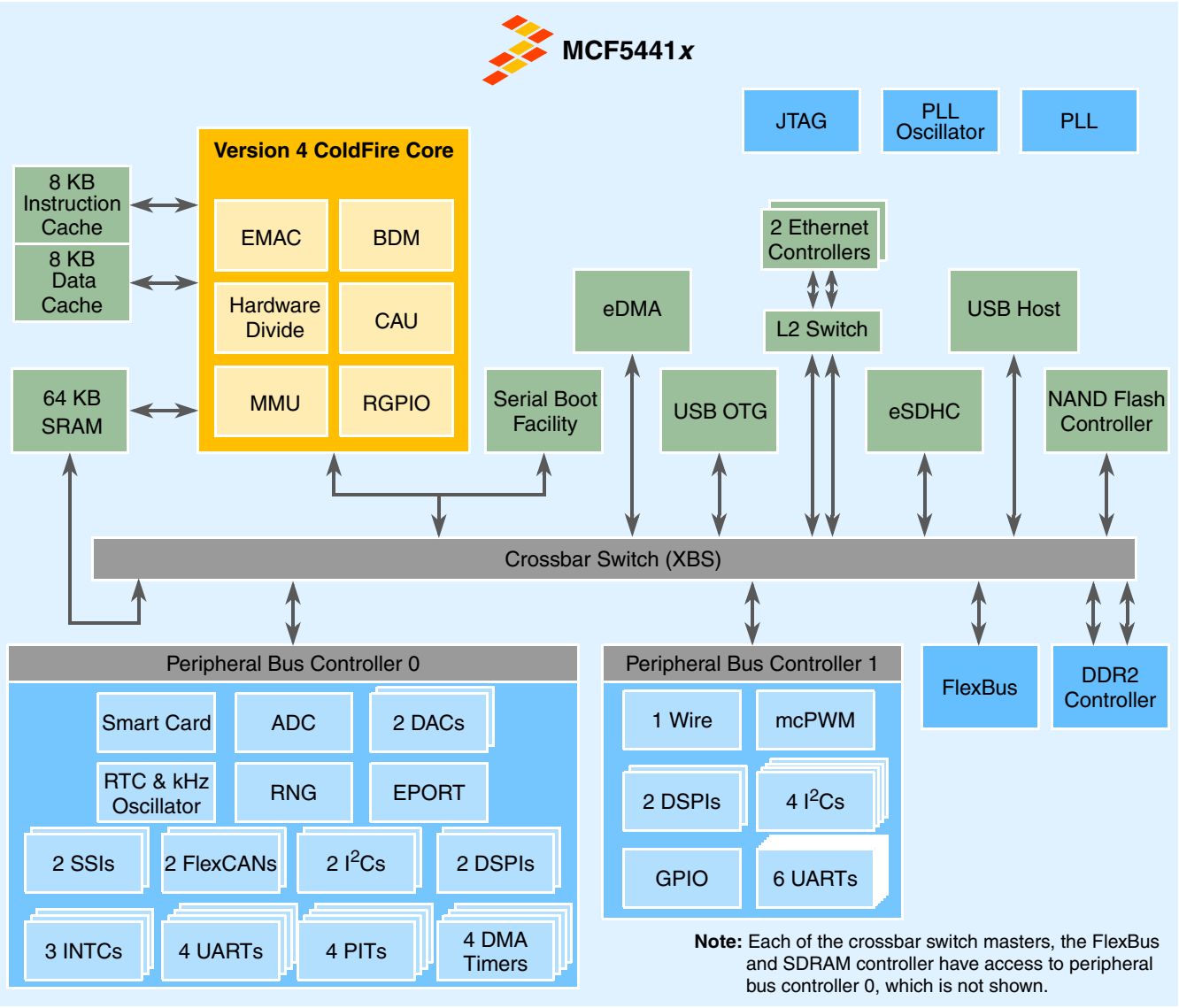
Module	MCF54410	MCF54415	MCF54416	MCF54417	MCF54418
Independent data/instruction cache	8 Kbytes each				
USB 2.0 Host controller	—	•	•	•	•
USB 2.0 Host/Device/On-the-Go controller	•	•	•	•	•
UTMI+ Low Pin Interface (ULPI) for external high-speed USB PHY	—	•	•	•	•
10/100 Mbps Ethernet controller with IEEE 1588 support	1	2	2	2	2
Level 2 IEEE 1588-compliant 3-port Ethernet switch	—	—	—	•	•
Enhanced Secure Digital host controller (eSDHC)	•	•	•	•	•
Smart card/Subscriber Identity Module (SIM)	—	2 ports	2 ports	2 ports	2 ports
UARTs	6	10	10	10	10
DSPI	3	4	4	4	4
CAN 2.0B controllers	1	2	2	2	2
I^2C	4	6	6	6	6
Synchronous serial interface (SSI)	1	2	2	2	2
12-bit ADC	—	•	•	•	•
12-bit DAC	—	2	2	2	2
32-bit DMA timers	4	4	4	4	4
Periodic interrupt timers (PIT)	4	4	4	4	4
Motor control PWM timer (mcPWM)	—	8 channel	8 channel	8 channel	8 channel
64-channel DMA controller	•	•	•	•	•
Real-time clock with 2 KB standby RAM and battery back-up input	•	•	•	•	•
DDR2 SDRAM controller	•	•	•	•	•
FlexBus external memory controller	•	•	•	•	•
NAND flash controller	•	•	•	•	•
1-Wire® interface	•	•	•	•	•
Serial boot facility	•	•	•	•	•
Watchdog timer	•	•	•	•	•
Interrupt controllers (INTC)	3	3	3	3	3
Edge port module (EPORT)	3 IRQs	5 IRQs	5 IRQs	5 IRQs	5 IRQs

Table 1. MCF5441*x* Family Configurations (continued)

Module	MCF54410	MCF54415	MCF54416	MCF54417	MCF54418
Rapid GPIO pins	9	16	16	16	16
General-purpose I/O (GPIO) pins	48	87	87	87	87
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•
Package	196 MAPBGA	256 MAPBGA			

2.2 Block Diagram

Figure 3 shows a top-level block diagram of the MCF5441*x* superset device.



ADC – Analog-to-digital converter
BDM – Background debug module
CAU – Cryptography acceleration unit
DAC – Digital-to-analog
DSPI – DMA serial peripheral interface
eDMA – Enhanced direct memory access module
eSDHC – Enhanced Secure Digital host controller
EMAC – Enchance multiply-accumulate unit
EPORT – Edge port module
GPIO – General purpose input/output module
I²C – Inter-Intergrated Circuit
INTC – Interrupt controller
JTAG – Joint Test Action Group interface
mcPWM – Motor control pulse width modulator
PIT – Programmable interrupt timers
PLL – Phase locked loop module
RGPIO – Rapid GPIO
RNG – Random number generator
RTC – Real time clock
SSI – Synchronous serial interface
USB OTG – Universal Serial Bus On-the-Go controller

Figure 3. MCF5441*x* Block Diagram

2.3 Operating Parameters

- -40ºC to 85ºC junction temperature devices are available
- 1.2V Core, 3.3V I/O, 1.8–3.3V external memory bus

2.4 Packages

Depending on device, the MCF5441*x* family is available in the following packages:

- 196-pin molded array process ball grid array (MAPBGA)
- 256-pin molded array process ball grid array (MAPBGA)

2.5 Chip Level Features

- Version 4 ColdFire® Core with EMAC and MMU
- Up to 385 Dhrystone 2.1 MIPS @ 250 MHz
- 8 Kbytes instruction cache and 8 Kbytes data cache
- 64 Kbytes internal SRAM dual-ported to processor local bus and other crossbar switch masters
- System boot from NOR, NAND, SPI flash, EEPROM, or FRAM
- Crossbar switch technology (XBS) for concurrent access to peripherals or RAM from multiple bus masters
- 64-channel DMA controller
- SDRAM controller supporting full-speed operation from a single x8 DDR2 component up to 250 MHz
- 32-bit FlexBus external memory interface for RAM, ROM, MRAM, and programmable logic
- USB 2.0 host controller
- USB 2.0 host/device/On-the-Go controller
- 8-bit single data rate ULPI port usable by the dedicated USB host module or the USB host/device/OTG module
- Dual 10/100 Ethernet MACs with hardware CRC checking/genration, IEEE 1588-2002 support support, and optional Ethernet switch
- CPU direct-attached hardware accelerator for DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
- Random number generator
- Enhanced Secure Digital host controller for SD, SDHC, SDIO, MMC, and MMCplus cards
- Two ISO7816 smart card interfaces
- Two FlexCAN modules
- Six I^2C bus interfaces with DMA support in master mode
- Two synchronous serial interfaces
- Four 32-bit timers with DMA support

- Four programmable interrupt timers
- 8-channel, 16-bit motor control PWM timer
- Dual 12-bit ADCs with shared input channels and multiple conversion trigger sources
- Dual 12-bit DACs with DMA support
- 1-wire module with DMA support
- NAND flash controller
- Real-time clock with 32-kHz oscillator, 2 KB standby SRAM, and battery backup supply input
- Up to four DMA-supported serial peripheral interfaces (DSPI)
- Up to ten UARTs with single-wire mode support
- Up to five external IRQ interrupts and 2 external DMA request/acknowledge pairs
- Up to 16 processor local bus Rapid GPIO pins
- Up to 87 standard GPIO pins

2.6 Module-by-Module Feature List

The following is a brief summary of the functional blocks in the MCF54418 superset device. For more details refer to the *MCF54418 ColdFire Microprocessor Reference Manual* (MCF54418RM).

2.6.1 Version 4 ColdFire Variable-Length RISC Processor

- Static CMOS operation
- 32-bit address and data path on-chip
- Maximum 250 MHz processor core and 125 MHz bus frequency
- Sixteen total general-purpose 32-bit address and data registers
- Enhanced multiply-accumulate unit (EMAC) for DSP and fast multiply operations
- Hardware divide execution unit supporting various 32-bit operations
- Virtual memory management unit (MMU) providing virtual-to-physical address translation and memory access control
- Implements the ColdFire Instruction Set Architecture, ISA_C

2.6.2 On-chip Memories

- 64 Kbyte dual-ported SRAM on CPU internal bus
  - — Accessible to non-core bus masters (e.g. DMA, USB modules, and Ethernet subsystem) via the crossbar switch
- Non-blocking, independent 8-KB data and instruction caches organized as 4-way set associative with 16 bytes per cache line and 512 cache lines, supporting copy-back and write-through modes

2.6.3 Phase Locked Loop (PLL) and Crystal Oscillator

- 14– MHz input clock
- Programmable frequency multiplication factor settings generating voltage-controlled oscillator (VCO) frequencies from 240– MHz, resulting in a core frequency of 15 MHz ($f_{vco} \div 16$) to MHz (maximum rated frequency).
- Loss-of-lock and loss-of-clock detection and reset
- Direct clocking of system by input clock, bypassing the PLL

2.6.4 Power Management

- Fully static operation with processor sleep and whole chip stop modes
- Limp mode for very low frequency operation while major peripherals are disabled
- Rapid response to interrupts from the low-power sleep mode (wake-up feature)
- Peripheral power management register to enable/disable clocks to most modules
- Software controlled disable of external clock input for low power consumption
- Battery backup supply for RTC and 2 KB standby SRAM for when main processor supply is removed

2.6.5 Chip Configuration Module (CCM)

- System configuration during reset
- Bus monitor, abort monitor
- Part identification number and part revision number
- Serial boot and configuration capability
  - — Supports SPI-compatible EEPROM, flash, and FRAM
  - — Pre-boot control of multiple chip configuration options

2.6.6 Reset Controller

- Separate reset in and reset out signals
- Seven sources of reset: power-on reset (POR), external, software, watchdog timer, loss of lock, loss of clock, JTAG instruction
- Status flag indication of source of last reset

2.6.7 System Control Module

- Access control registers
- Watchdog timer with 2^n (where n = 8–31) clock cycle selectable timeout period
- Dedicated clock source (32-kHz on-chip oscillator) for watchdog timer
- Core fault reporting

2.6.8 Crossbar Switch

- Concurrent access from different masters to different slaves
- Slave arbitration attributes configured on a per basis
- Fixed or round-robin arbitration

2.6.9 Universal Serial Bus (USB) Host Controller

- Fully compliant with the *Universal Serial Bus Specification, Revision 2.0*
- Support for full speed (FS = 12 Mbps) and low speed (LS = 1.5 Mbps) with on-chip FS/LS transceiver
- Compatible with the *Enhanced Host Controller Interface (EHCI) Specification for Universal Serial Bus, Revision 1.0*
- Connects to external 5V power control chip for downstream power
- Optional UTMI+ Low Pin Interface (ULPI) to support high speed (HS = 480 Mbps) transfers with external PHY, shared with USB OTG module
- Uses 60 MHz reference clock based off of the system clock or from an external pin

2.6.10 Universal Serial Bus (USB) 2.0 On-The-Go (OTG) Controller

- Fully compliant with the *Universal Serial Bus Specification, Revision 2.0* and *On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a*
- Support for full speed (FS) and low speed (LS) via on-chip FS/LS transceiver in host mode
- Compatible with the *Enhanced Host Controller Interface (EHCI) Specification for Universal Serial Bus, Revision 1.0* (host mode)
- Connects to external 5V power control chip for downstream power (host mode)
- Support for full speed with on-chip transceiver in device mode
- Optional UTMI+ Low Pin Interface (ULPI) to support high speed (HS = 480 Mbps) transfers with external PHY, shared with USB host module
- Connects to external OTG charge pump and resistor chip via I^2C bus
- Uses 60 MHz reference clock based off of the system clock or from an external pin

2.6.11 DDR SDRAM Controller

- Supports glueless interface to DDR2 SDRAM devices
- 8-bit wide memory port runs at the CPU clock frequency to deliver up to 500 MBps of memory bandwith at 250 MHz
- Unique interface design reduces memory subsystem cost to the cost of a single x8 commodity DDR2 component while delivering performance equivalent to a 32-bit wide single data rate SDRAM subsystem running at up to 125 MHz and requiring two x16 or four x8 components

- Innovative controller uses two crossbar switch slave ports, multiple read/write queues, and intelligent transfer ordering to maximize memory channel utilization and reduce multi-master access latency
- 16 bytes critical word first burst transfer
- Up to 15 lines of row address, up to 12 column address lines, 8 banks (3-bits), and one chip select
- Supports 16, 32, 64, 128, or 256 MB of memory using a single 16M × 8 (128 Mb), 32M × 8 (256 Mb), 64M × 8 (512 Mb), 128M × 8 (1 Gb), or 256M × 8 (2 Gb) component
- Supports page mode to maximize the data rate
- Supports sleep mode and self-refresh mode

2.6.12 FlexBus (External Interface)

- 32-bit external bidirectional multiplexed address/data bus
- Glueless connections to 8-, 16-, and 32-bit external memory devices (SRAM, flash, ROM, etc.)
- Support for independent primary and secondary wait states per chip select
- Programmable address setup and hold time with respect to chip-select assertion, per transfer direction
- Glueless interface to SRAM devices with or without byte strobe inputs
- Supports asynchronous and synchronous memories with a dedicated address latch signal available
- Programmable wait state generator
- Up to six chip selects available
- Byte/write enables (byte strobes)
- Ability to boot from external memories that are 8, 16, or 32 bits wide

2.6.13 Ethernet Assembly

- On-chip layer 2 (L2) Ethernet switch
  - 3-port switch (one port internal to the switch core)
  - IEEE 1588 support
  - Fast cut-through mode
  - QoS with 8 queues per port
  - Port mirroring
  - Level 3 IP snooping
  - Link aggregation
- Two Ethernet controllers with 10/100 BaseT/TX capability; half duplex or full duplex
  - Hardware support for *IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*, IEEE 1588
  - Media independent interface (MII) and reduced media independent interface (RMII) support

- Built-in unified DMA
  - On-chip transmit and receive FIFOs
  - Supports legacy buffer descriptor programming models and functionality
  - Enchanced buffer descriptor programming model for new Ethernet functionality
- Supports wake-up from low power mode through magic packets
- During chip reset, ability to route traffic from one port to another
- Multiple clock source options for time-stamping clock

2.6.14 Cryptography Acceleration Unit (CAU)

- Instruction-level coprocessor
- Supports DES, 3DES, AES, MD5, SHA-1, and SHA-256

2.6.15 Random Number Generator

- National Institute of Standards and Technology (NIST)-approved pseudo-random number generator
- Supports the key generation algorithm defined in the Digital Signature Standard
- Integrated entropy sources capable of providing the PRNG with entropy for its seed.

2.6.16 Secure Digital Host Controller (SDHC)

- Compatible with the following specifications:
  - SD Host Controller Standard Specification, Version 2.0 (www.sdcard.org)
  - MultiMediaCard System Specification, Version 4.2 (www.mmca.org)
  - SD Memory Card Specification, Version 2.0 (www.sdcard.org)
  - SDIO Card Specification, Version 2.0 (www.sdcard.org)
  - CE-ATA Card Specification, Version 1.0 (www.sdcard.org)
- Designed to work with CE-ATA, SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, MMC 4x, and MMC RS cards
- SD bus clock up to 52 MHz
- Supports 1- and 4-bit SD and SDIO modes, 1-, 4-, and 8-bit MMC modes, and 1-, 4-, and 8-bit CE-ATA devices
- Contains a fully configurable 128 x 32-bit FIFO for read/write data

2.6.17 Subscriber Identity Module (SIM)

- Two ISO7816 smart card interfaces
- Three interfaces supported (two-wire, external one-wire, and internal one-wire)
- Programmable clock divisor

- Fourteen total interrupt sources (six transmit, six receive, two control functions)

2.6.18 Synchronous Serial Interfaces (SSI)

- Two SSIs each support shared (synchronous) transmit and receive sections
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as 32 time slots
- Gated clock mode operation requiring no frame sync
- Programmable data interface modes such as I^2S, LSB aligned, and MSB aligned
- Programmable word length up to 24 bits
- AC97 support

2.6.19 FlexCAN Modules

- Two FlexCAN modules support the full implementation of the *CAN Specification Version 2.0, Part B*
  - Standard data and remote frames (up to 109 bits long)
  - Extended data and remote frames (up to 127 bits long)
  - 0–8 bytes data length
  - Programmable bit rate up to 1 Mbit/sec
- Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 bytes data length each, configurable as Rx or Tx, all supporting standard and extended messages
- Unused MB space can be used as general purpose RAM space
- Listen-only mode capability
- Content-related addressing
- Three programmable mask registers: global (MBs 0–13), special for MB14 and special for MB15
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message

2.6.20 Analog-Digital Converters (ADC)

- Two 4-channel, 12-bit ADCs with sequential and parallel sampling
- Software, external, and on-chip (such as mcPWM and DMA timers) triggered conversions
- DMA interface to the on-chip 64 channel DMA controller
- Supports multiple low power modes, including auto-power down

2.6.21 Digital-Analog Converters (DAC)

- Dual 12-bit DACs

- DMA interface to the on-chip 64 channel DMA controller
- High-/low-speed programmable operation
- Software, external, and on-chip (such as mcPWM and DMA timers) triggered conversions
- Automatic waveform generation, including square, triangle, and sawtooth
- DAC output connected to the on-chip ADC for digital to digital comparision for debug

2.6.22 NAND Flash Controller

- 8- or 16-bit NAND flash interface
- Internal 9-KByte RAM buffer configurable as boot RAM
- Supports all NAND flash products regardless of density/organization
- Automatic write protection during power-up
- Handshaking to indicate ready/busy status
- Supports time division multiplexing external memory interface (FlexBus) cycles with long access times of NAND flash devices
- Integrated DMA engine to support self-initiated data transfer from NAND flash to system memory or any slave devices on crossbar switch

2.6.23 1-Wire Interface

- Communicates with an external 1-Wire device as defined by Maxim
- Clock divider to generate the bus reference clock from the peripheral bus clock
- DMA interface to the on-chip 64 channel DMA controller

2.6.24 Robust Real Time Clock

- Full clock: hours, minutes, and seconds with storing option
- Calendar: day, month, year, and day of the week with storing option
- Automatic adjustment for daylight savings with user-defined parameters
- Automatic month and leap year adjustment
- Programmable alarm with interrupt
- Seven periodic interrupts
- Minute stopwatch
- Once-per-day, once-per-hour, once-per-minute, and once-per-second interrupts
- Operation determined by reference input oscillator clock frequency and value programmed into user-accessible registers
- Ability to wake the processor from low-power modes (wait, doze, and stop) via the RTC interrupts
  - The RTC is enabled during stop mode

- Battery operation (standby mode) ensures seamless operation when processor power is removed
- Protection against tampering and spurious memory/register updates
- Supports hardware compensation to improve accuracy against crystal frequency variations
- Dedicated 2 KB RAM for storing the system contents during standby operation when processor power is removed

2.6.25 Programmable Interrupt Timers (PIT)

- Four programmable interrupt timers each with a 16-bit counter
- Configurable as a down counter or free-running counter

2.6.26 DMA Timers

- Four 32-bit timers with DMA and interrupt request trigger capability
- Input capture and reference compare modes
- Support for the Ethernet assembly's IEEE 1588 timebase and count values
- Programmable delay support

2.6.27 DMA Serial Peripheral Interfaces (DSPI)

- Four DSPIs with up to four chip selects available per DSPI module
- Full-duplex, three-wire synchronous transfer
- Master and slave modes with programmable master bit-rates
- Up to 16 pre-programmed transfers

2.6.28 Motor Control Pulse Width Modulation (mcPWM) Module

- 16-bit resolution for center-aligned, edge-aligned, and asymmetrical PWMs
- Four PWM output pairs (8 total outputs) that can operate as complementary pairs or independent channels
- Synchronization to external hardware, other PWM channels, or the IEEE 1588 timestamp via the on-chip DMA timer
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Multiple output trigger events can be generated per PWM cycle via hardware
- Support for double-switching PWM outputs
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion

- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a force-out event
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual-edge capture functionality
- Enhanced triggering capability
  - Multiple ADC trigger events can be generated per PWM cycle

2.6.29 Universal Asynchronous Receiver Transmitters (UARTs)

- Ten UARTs each with a 16-bit divider for clock generation
- DMA support with separate transmit and receive requests
- Support for single wire and wired-OR mode
- Programmable clock-rate generator
- Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
- Up to 2 stop bits in 1/16 increments
- Error-detection capabilities

2.6.30 I^2C Modules

- Six interchip bus interfaces for EEPROMs, LCD controllers, A/D converters, and keypads
- DMA support in master mode
- Fully compatible with industry-standard I^2C bus
- Master or slave modes support multiple masters
- Automatic interrupt generation with programmable level

2.6.31 Interrupt Controllers

- Three interrupt controllers, supporting up to 64 interrupt sources each, organized as seven programmable levels
- Unique vector number for each interrupt source
- Ability to mask any individual interrupt source plus a global mask-all capability
- Support for service routine software interrupt acknowledge (IACK) cycles
- Combinational path to provide wake-up from low power modes

2.6.32 Edge Port Module

- Each pin can be individually configured as low level sensistive interrupt pin or edge-detecting interrupt pin (rising, falling, or both)

- Exit stop mode via level-detect function

2.6.33 DMA Controller

- 64 fully programmable channels with 32-byte transfer control descriptors
- Data movement via dual-address transfers for 8-, 16-, 32- and 128-bit data values
- Programmable source, destination addresses, transfer size, support for enhanced address modes
- Support for major and minor nested counters with one request and one interrupt per channel
- Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration
- External request/acknowledge pins

2.6.34 Rapid GPIO Interface

- 16 bits of high-speed GPIO functionality connected to the processor's local bus
- Pin toggle rates typically 1.5–3.5x faster than traditional GPIO pin connected to the peripheral bus
- Unused Rapid GPIO pins can be used as traditional GPIO

2.6.35 General Purpose I/O Interface

- Up to 48 bits of GPIO for the 196 MAPBGA device
- Up to 71 bits of GPIO for the 256 MAPBGA device
- Bit manipulation supported via set/clear functions
- Various unused peripheral pins may be used as GPIO
- Drive strength and slew rate control

2.6.36 System Debug Support

- Background debug mode (BDM) Revision D+
- Real time debug support, with four PC breakpoint registers and a pair of address breakpoint registers with optional data
- Compressed processor status and debug data captured into on-chip trace buffer

2.6.37 JTAG Support

- JTAG part identification and part revision numbers

3 Developer Environment

The MCF5441*x* family of MPUs supports similar tools and third party developers as other Freescale ColdFire products, offering a widespread, established network of tools and software vendors.

The following development support will be available:

- Evaluation boards (EVBs)
- Compilers and debuggers
- Debug interfaces
- Initialization tool

The following software support will be available:

- Code examples
- Various module drivers (e.g., Ethernet, USB, SPI, I^2C)
- Third party real-time operating systems (RTOS)

4 Revision History

Table 2 provides a revision history for this document.

Table 2. MCF54418PB Document Revision History

Rev. No.	Date	Substantive Change(s)
0	08/2008	Initial NDA revision
1	2/2009	Major updates to introduction section Figure 1 and Figure 2: Combined “NAND or NOR flash” and “Serial boot flash” blocks In Table 1: • Split “Peripheral and external bus clock” row • Removed ULPI from MCF54410 • Split “L2 Ethernet switch with two Ethernet controllers” row. Two controllers are available on MCF54415–8, L2 switch available on MCF54417–8 • Changed “10-bit DAC” to “12-bit DAC” • Removed mcPWM from MCF54410 In Section 2.5, “Chip Level Features” • Removed mobile DDR support • Expanded description of Ethernet features • Expanded description of SDHC • In Real-time clock bullet, added 2 KB standby RAM feature • Added number of RGPIO and GPIO pins In Section 2.6.1, “Version 4 ColdFire Variable-Length RISC Processor”, added MMU bullet In Section 2.6.3, “Phase Locked Loop (PLL) and Crystal Oscillator”, changed “14–50MHz reference crystal” to “14–40MHz reference crystal” and added third bullet In Section 2.6.4, “Power Management”, added limp mode bullet In Section 2.6.5, “Chip Configuration Module (CCM)”, removed “Configurable output pad drive strength control” and “Configurable boot clock frequency” and added “Pre-boot control of multiple chip configuration options” In Section 2.6.9, “Universal Serial Bus (USB) Host Controller”, added ULPI bullet In Section 2.6.10, “Universal Serial Bus (USB) 2.0 On-The-Go (OTG) Controller”, added compliance to USB2.0 and EHCI specs. In Section 2.6.11, “DDR SDRAM Controller”, removed mobile DDR support, expanded description of “8-bit memory port” bullet, added two bullets, expanded description of memory size support In Section 2.6.35, “General Purpose I/O Interface”, added “Drive strength and slew rate control”

Table 2. MCF54418PB Document Revision History (continued)

Rev. No.	Date	Substantive Change(s)
2	2/2009	Updates to introduction and features list to match Overview chapter of *MCF5441x Reference Manual*, Rev 0 Changed 144 MAPBGA package to 169 MAPBGA
3	07/2010	Entered changes based on shared review comments

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