Commercial and Industrial DDR2 512Mb SDRAM

Features

- **JEDEC DDR2 Compliant**
  - Double-data rate on DQs, DQS, DM bus
  - 4n Prefetch Architecture
- **Throughput of valid Commands**
  - Posted CAS and Additive Latency (AL)
- **Signal Integrity**
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
- **Data Integrity**
  - Auto Refresh and Self Refresh Modes
- **Power Saving Modes**
  - Power Down Mode
- **SSTL_18 compliance and Power Supply**
  - VDD/VDDQ = 1.70 to 1.90V

Options

■ **Speed Grade (DataRate/CL-tRCD-tRP)** [1]
- 1066 Mbps / 7-7-7
- 800 Mbps / 5-5-5

■ **Temperature Range (*Tc*)** [2]
- Commercial Grade = 0℃ to + 95℃
- Industrial Grade = - 40℃ to + 95℃

Programmable functions

■ **Output Drive Impedance (Full, Reduced)**
■ **Burst Length (4, 8)**
■ **Burst Type (Sequential, Interleaved)**
■ **Rtt (50, 75, 150)**
■ **CAS Latency (3, 4, 5, 6, 7)**
■ **Additive Latency (0, 1, 2, 3, 4, 5, 6)**
■ **WR (2, 3, 4, 5, 6, 7, 8)**

Density / Packages information

Lead-free RoHS compliance and Halogen-free

512Mb (Org. / Package)		Width x Length (mm)	Ball pitch (mm)
64 Mb x 8	60 VFBGA	8.00 x 10.00	0.80
32 Mb x 16	84 VFBGA	8.00 x 12.50	0.80

Density and Addressing

Configuration	64 Mb x 8	32 Mb x 16
Number of Banks	4	4
Bank Address	BA0 – BA1	BA0 – BA1
Auto Precharge	A10/AP	A10/AP
Row Address	A0 - A13	A0 - A12
Column Address	A0 - A9	A0 – A9
Page Size	1 KB	2 KB

Notes:
1. The timing specification of high speed bin is backward compatible with low speed bin.
2. If TC exceeds 85°C, the DRAM must be refreshed externally at 2x refresh. It is required to set tREFI=3.9μs in auto refresh mode and to set '1' for EMRS (2) bit A7 in self refresh mode.

Major Timing Specifications for Corresponding Bins

DDR2-1066, DDR2-800 and DDR2-667

Speed Bin	DDR2-1066[1]		DDR2-800[1]				DDR2-667[1]		Units
CL-tRCD-tRP	7-7-7		5-5-5		6-6-6		5-5-5		
Parameter	min	max	min	max	min	max	min	max	
tRCD	13.125	-	12.5	-	15	-	15	-	ns
tRP	13.125	-	12.5	-	15	-	15	-	ns
tRC	58.125	-	57.5	-	60	-	60	-	ns
tRAS	45	70K	45	70K	45	70K	45	70K	ns
tCK(avg), CL=3	Option[2]		Option[2]				Option[2]		ns
tCK(avg), CL=4	3.75	7.5	3.75	8	3.75	8	3.75	8	ns
tCK(avg), CL=5	3	7.5	2.5	8	3	8	3	8	ns
tCK(avg), CL=6	2.5	7.5	Option[2]		2.5	8	Option[2]		ns
tCK(avg), CL=7	1.875	7.5	Option[2]				Option[2]		ns

Notes

1. The timing specification of high speed bin is backward compatible with low speed bin
   - DDR2-1066 7-7-7 is compatible with DDR2-800 5-5-5/6-6-6 and DDR2-667 5-5-5.
   - DDR2-800 5-5-5 is compatible with DDR2-800 6-6-6 and DDR2-667 5-5-5.
   - DDR2-800 6-6-6 is compatible with DDR2-667 5-5-5.
2. Please confirm with NTC for its availability.

Ordering Information

Lead-free RoHS compliance and Halogen-free

Commercial Grade				
Organization	**Part Number**	**Package**	**Speed [1]**	
			Data Rate(Mbps)	**CL-TRCD-TRP**
64 Mb x 8	NT5TU64M8EE-AC	60-Ball BGA	800	5-5-5
32 Mb x 16	NT5TU32M16EG-BE	84-Ball BGA	1066	7-7-7
	NT5TU32M16EG-AC		800	5-5-5

Industrial Grade				
Organization	**Part Number**	**Package**	**Speed [1]**	
			Data Rate(Mbps)	**CL-TRCD-TRP**
64 Mb x 8	NT5TU64M8EE-ACI	60-Ball BGA	800	5-5-5
32 Mb x 16	NT5TU32M16EG-ACI	84-Ball BGA	800	5-5-5

Notes

1. The timing specification of high speed bin is backward compatible with low speed bin
2. Please confirm with NTC for the available schedule.

NANYA Component Part Numbering Guide

NANYA Technology

Special Type Option
- **I** = Industrial Grade
- **B** = Reduced Standby
- **H** = Automotive Grade 2
- **A** = Automotive Grade 3

Speed

Product Family
- **5S** = SDRAM
- **5D** = DDR SDRAM
- **5T** = DDR2 SDRAM
- **5C** = DDR3 SDRAM

SDRAM

75B	= PC-133	3-3-3
6K	= PC-166	3-3-3

DDR SDRAM

6K	= DDR - 333	2.5-3-3
5T	= DDR - 400	3-3-3

Interface & Power(VDD & VDDQ)

V	= LVTTL	(**3.3**V , **3.3**V)
E	= LVTTL	(**2.5**V , **2.5**V)
S	= SSTL_2	(**2.5**V , **2.5**V)
M	= LVTTL	(**1.8**V , **1.8**V)
U	= SSTL_18	(**1.8**V , **1.8**V)
B	= SSTL_15	(**1.5**V , **1.5**V)
A	= SSTL_18	(**2.0**V , **2.0**V)
C	= SSTL_135	(**1.35**V , **1.35**V)
F	= SSTL_125	(**1.25V , 1.25V**)

DDR2 SDRAM

5A	= DDR2 - 400	3-3-3
37B	= DDR2 - 533	4-4-4
3C	= DDR2 - 667	5-5-5
25C/AC	= DDR2 - 800	5-5-5
25D/AD	= DDR2 - 800	6-6-6
BE	= DDR2-1066	7-7-7
BD	= DDR2-1066	6-6-6

Organization(Depth , Width)

4M 16	**= 8M8**		**=** 64 Mb
8M 16	**= 16M8**		**=** 128Mb
16M 16	**= 32M 8**	**= 64M 4**	**=** 256Mb
32M 16	**= 64M 8**	**= 128M 4**	**=** 512Mb
64M 16	**= 128M 8**	**= 256M 4**	**=** 1Gb
128M 16	**= 256M 8**	**= 512M 4**	**=** 2Gb
256M 16	**= 512M 8**	**= 1024M4**	**=** 4Gb

Note: M= Mono

DDR3 SDRAM

AC	= DDR3 - 800	5-5-5
AD	= DDR3 - 800	6-6-6
BE	= DDR3 - 1066	7-7-7
BF	= DDR3 - 1066	8-8-8
CF	= DDR3 - 1333	8-8-8
CG	= DDR3 - 1333	9-9-9
DG	= DDR3- 1600	9-9-9
DH	= DDR3 - 1600	10-10-10
DI	= DDR3 - 1600	11-11-11
EJ	= DDR3 - 1866	12-12-12
EK	= DDR3 - 1866	13-13-13
FK	= DDR3 - 2133	13-13-13
FL	= DDR3- 2133	14-14-14

Device Version

A = 1st	Version	**B** = 2nd	Version
C = 3rd	Version	**D** = 4th	Version
E = 5th	Version	**F** = 6th	Version
G = 7th	Version	**H** = 8th	Version

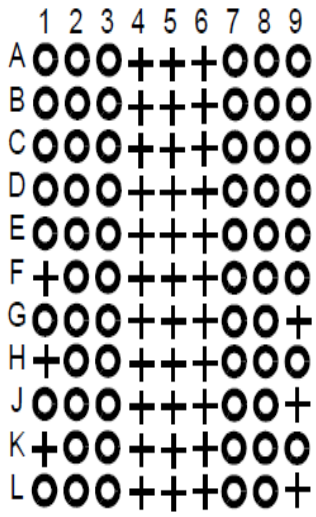
Package Code

RoHS + Halogen Free
- **S**= TSOP(II)
- **N**=78 -Ball BGA
- **P**=96 -Ball BGA
- **E**=60 -Ball BGA
- **J**=68 -Ball BGA
- **M**=92 -Ball BGA
- **U**=71 -Ball BGA
- **Y**=63 -Ball BGA
- **8**=136-Ball BGA
- **G**= DDR1 BGA / DDR2 84- Ball BGA

60-ball BGA Ballout and Package Outline Drawing (x8)

< TOP View>

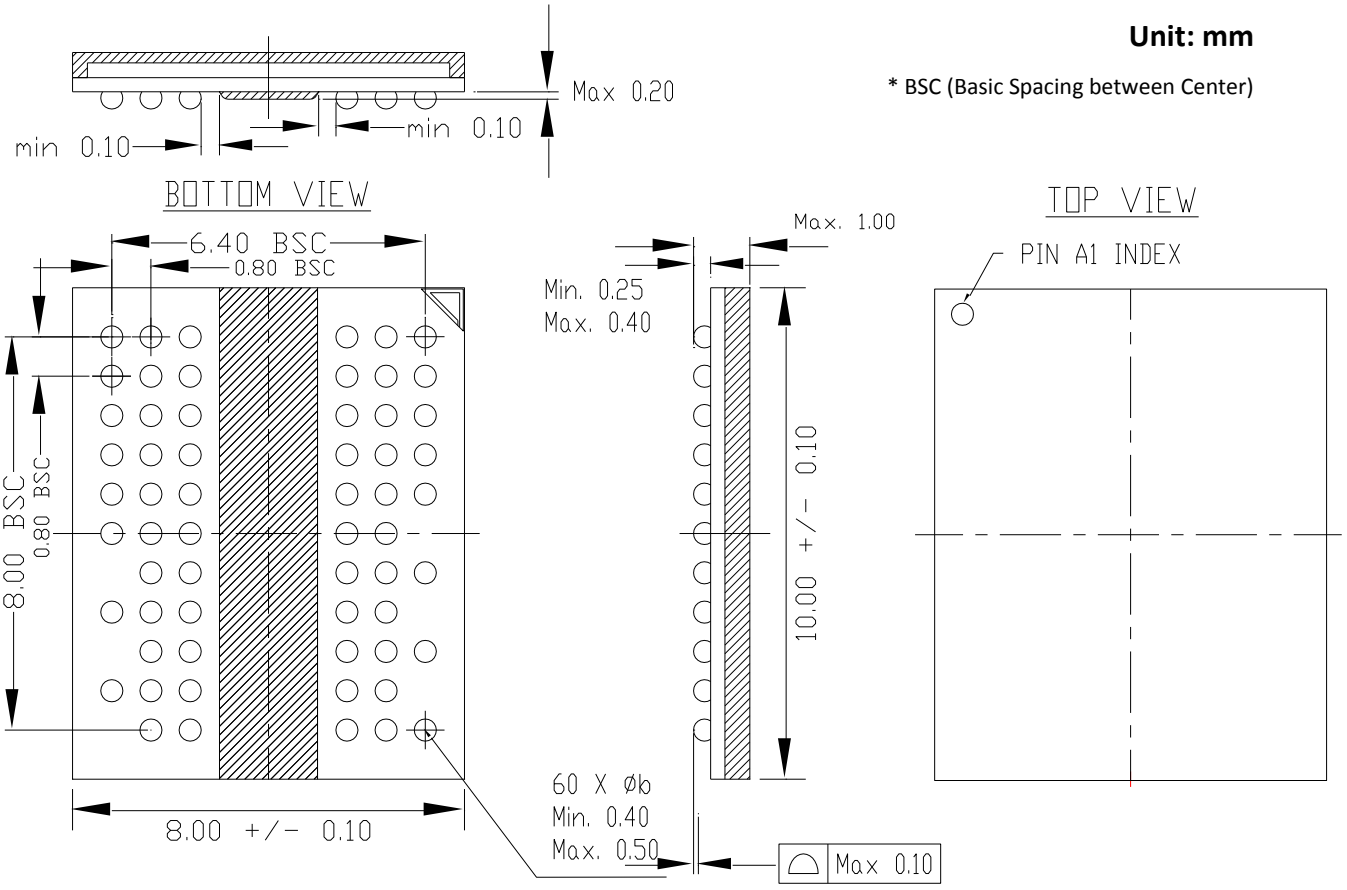
See the balls through the package



	1	2	3	4 5 6	7	8	9	
A	VDD	NU, $\overline{RDQS}$	VSS		VSSQ	$\overline{DQS}$	VDDQ	A
B	DQ6	VSSQ	DM,RDQS		DQS	VSSQ	DQ7	B
C	VDDQ	DQ1	VDDQ		VDDQ	DQ0	VDDQ	C
D	DQ4	VSSQ	DQ3		DQ2	VSSQ	DQ5	D
E	VDDL	VREF	VSS		VSSDL	CK	VDD	E
F		CKE	$\overline{WE}$		$\overline{RAS}$	$\overline{CK}$	ODT	F
G	NC	BA0	BA1		$\overline{CAS}$	$\overline{CS}$		G
H		A10/AP	A1		A2	A0	VDD	H
J	VSS	A3	A5		A6	A4		J
K		A7	A9		A11	A8	VSS	K
L	VDD	A12	NC		NC	A13		L
	1	2	3	4 5 6	7	8	9	

Unit: mm

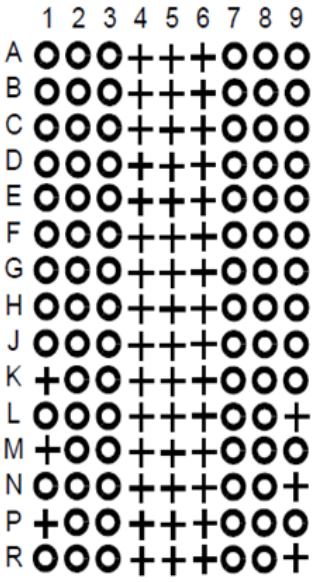
* BSC (Basic Spacing between Center)



84-ball BGA Ballout and Package Outline Drawing (x16)

< TOP View>

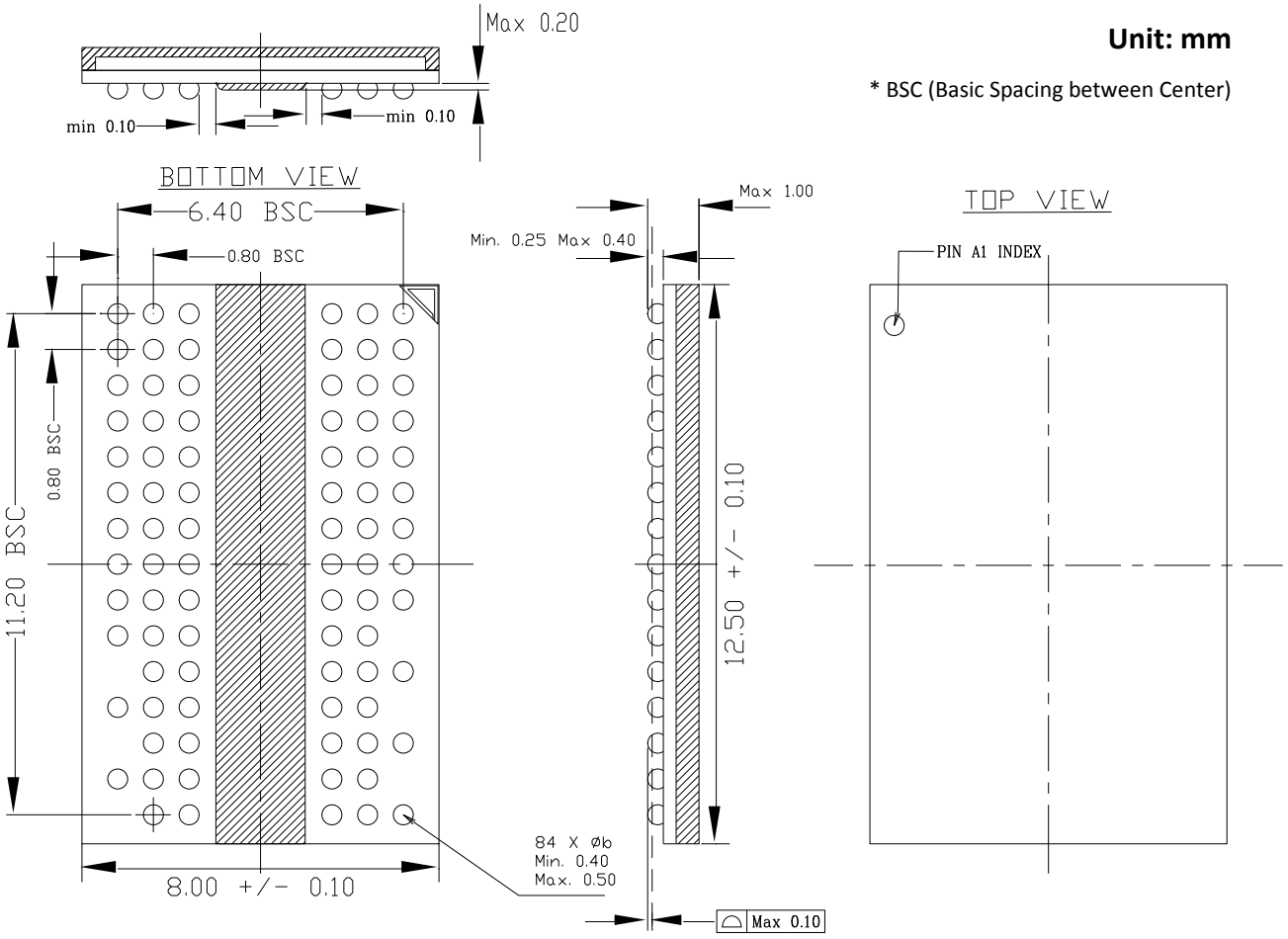
See the balls through the package



	1	2	3	4	5	6	7	8	9	
A	VDD	NC	VSS				VSSQ	$\overline{UDQS}$	VDDQ	A
B	DQ14	VSSQ	UDM				UDQS	VSSQ	DQ15	B
C	VDDQ	DQ9	VDDQ				VDDQ	DQ8	VDDQ	C
D	DQ12	VSSQ	DQ11				DQ10	VSSQ	DQ13	D
E	VDD	NC	VSS				VSSQ	$\overline{LDQS}$	VDDQ	E
F	DQ6	VSSQ	LDM				LDQS	VSSQ	DQ7	F
G	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
H	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
J	VDDL	VREF	VSS				VSSDL	CK	VDD	J
K		CKE	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT	K
L	NC	BA0	BA1				$\overline{CAS}$	$\overline{CS}$		L
M		A10/AP	A1				A2	A0	VDD	M
N	VSS	A3	A5				A6	A4		N
P		A7	A9				A11	A8	VSS	P
R	VDD	A12	NC				NC	NC		R
	1	2	3	4	5	6	7	8	9	

Unit: mm

* BSC (Basic Spacing between Center)



Ball Descriptions

Symbol	Type	Function
CK,$\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$,$\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (LDM, UDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0 – BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 – A13	Input	**Address Inputs:** Provides the row address for Activate commands and the column address and Auto Precharge or Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the precharge applies to one bank (A10=low) or all banks (A10=high). If only one bank is to be precharged, the bank is selected by BA0-BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/output	**Data Inputs/Output:** Bi-directional data bus.

Symbol	Type	Function
DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$)	Input/output	**Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. For the x16, LDQS corresponds to the data on DQ0 - DQ7; UDQS corresponds to the data on DQ8-DQ15. The data strobes DQS, LDQS and UDQS may be used in single ended mode or paired with the optional complementary signals $\overline{DQS}$, $\overline{LDQS}$ and $\overline{UDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables the complementary data strobe signals.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. For x16 configuration ODT is applied to each DQ, UDQS, $\overline{UDQS}$, LDQS, $\overline{LDQS}$, UDM and LDM signal. The ODT pin will be ignored if the EMRS (1) is programmed to disable ODT.
NC	-	**No Connect:** No internal electrical connection is present.
VDDQ	Supply	**DQ Power Supply:** 1.8V ± 0.1V
VSSQ	Supply	**DQ Ground**
VDDL	Supply	**DLL Power Supply:** 1.8V ± 0.1V
VSSDL	Supply	**DLL Ground**
VDD	Supply	**Power Supply:** 1.8V ± 0.1V
VSS	Supply	**Ground**
VREF	Supply	**SSTL_1.8 reference voltage**

Note 1: The signal may show up in a different symbol but it indicates the same thing. e.g., /CK = CK# = $\overline{CK}$ = CKb, /DQS = DQS# = $\overline{DQS}$ = DQSb, /CS= CS# = $\overline{CS}$ = CSb.

Functional Descriptions

The 512Mb DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits.

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for the burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Activate command, which is followed by a Read or Write command. The address bits registered coincident with the activate command are used to select the bank and row to be accesses (BA0-BA1 select the bank, A0-A13 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the Auto-Precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

Power-up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The following sequence is required for POWER UP and Initialization.

1. Either one of the following sequence is required for Power-up.

(1)

While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT at a Low state (all other inputs may be undefined) The VDD voltage ramp time must be no greater than 200ms from when VDD ramps from 300mV to VDD min; and during the VDD voltage ramp up, IVDD-VDDQI≦0.3 volts. Once the ramping of the supply voltages is complete (when VDDQ crosses VDDQ min), the supply voltage specifications in Re-commanded DC operating conditions table.

- VDD, VDDL, and VDDQ are driven from a signal power converter output, AND
- VTT is limited to 0.95V max, AND
- Vref tracks VDDQ/2; Vref must be within ±300mV with respect to VDDQ/2 during supply ramp time.
- VDDQ>=VREF must be met at all times.

(2)

While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT at a Low state, all other inputs may be undefined, voltage levels at I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, VDD≧VDDL≧VDDQ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete, which is when VDDQ crosses VDDQ min. Once the ramping of the supply voltages is complete, the supply voltage specifications provided in Re-commanded DC operating conditions table.

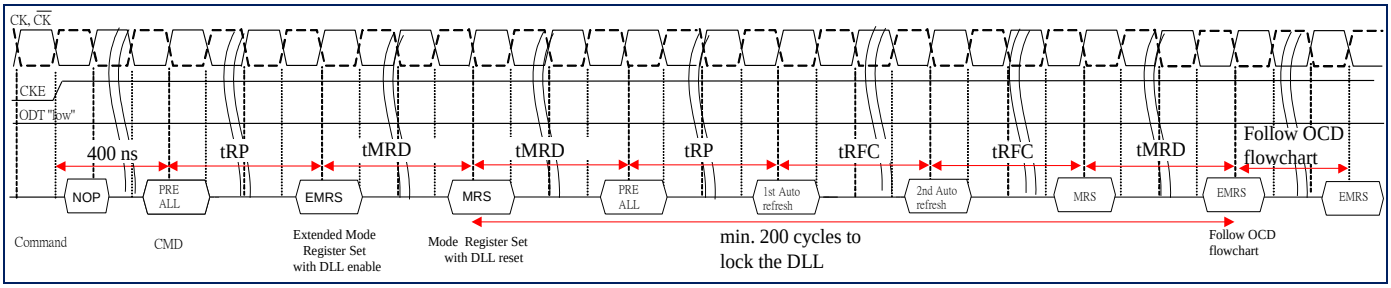
- Apply VDD/VDDL before or at the same time as VDDQ.
- VDD/VDDL voltage ramp time must be no greater than 200ms from when VDD ramps from 300mV to VDDmin.
- Apply VDDQ before or at the same time as VTT.
- The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500ms. (Note: While VDD is ramping, current may be supplied from VDD through the DRAM to VDDQ.)
- Vref must track VDDQ/2; Vref must be within ±300mV with respect to VDDQ/2 during supply ramp time.
- VDDQ ≧ VREF must be met at all time.
- Apply VTT.

2. Start clock (CK, $\overline{CK}$) and maintain stable condition.

3. For the minimum of 200us after stable power (VDD, VDDL, VDDQ, VREF, and VTT are between their minimum and maximum values as stated in Re-commanded DC operating conditions table, and stable clock, then apply NOP or Deselect & take CKE HIGH.
4. Wait minimum of 400 ns then issue precharge all command. NOP or Deselect applied during 400 ns period.
5. Issue an EMRS command to EMR(2). (To issue EMRS command to EMR(2), provide LOW to BA0 and BA1,HIGH to BA1.)
6. Issue an EMRS command to EMR(3). (To issue EMRS command to EMR(3), provide LOW to BA1, HIGH to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue DLL Enable command, provide LOW to A0, HIGH to BA0 and LOW to BA1-BA1 and A12-A13. And A9=A8=A7=LOW must be used when issuing this command.)
8. Issue a Mode Register Set command for DLL reset.(To issue DLL Reset command, provide HIGH to A8 and LOW to BA0-BA1.)
9. Issue a precharge all command.
10. Issue 2 more auto-refresh commands.
11. Issue a MRS command with LOW to A8 to initialize device operation (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 7, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRs to EMR (1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR (1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).
13. The DDR2 DRAM is now ready for normal operation.

* To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

Example:



Register Definition

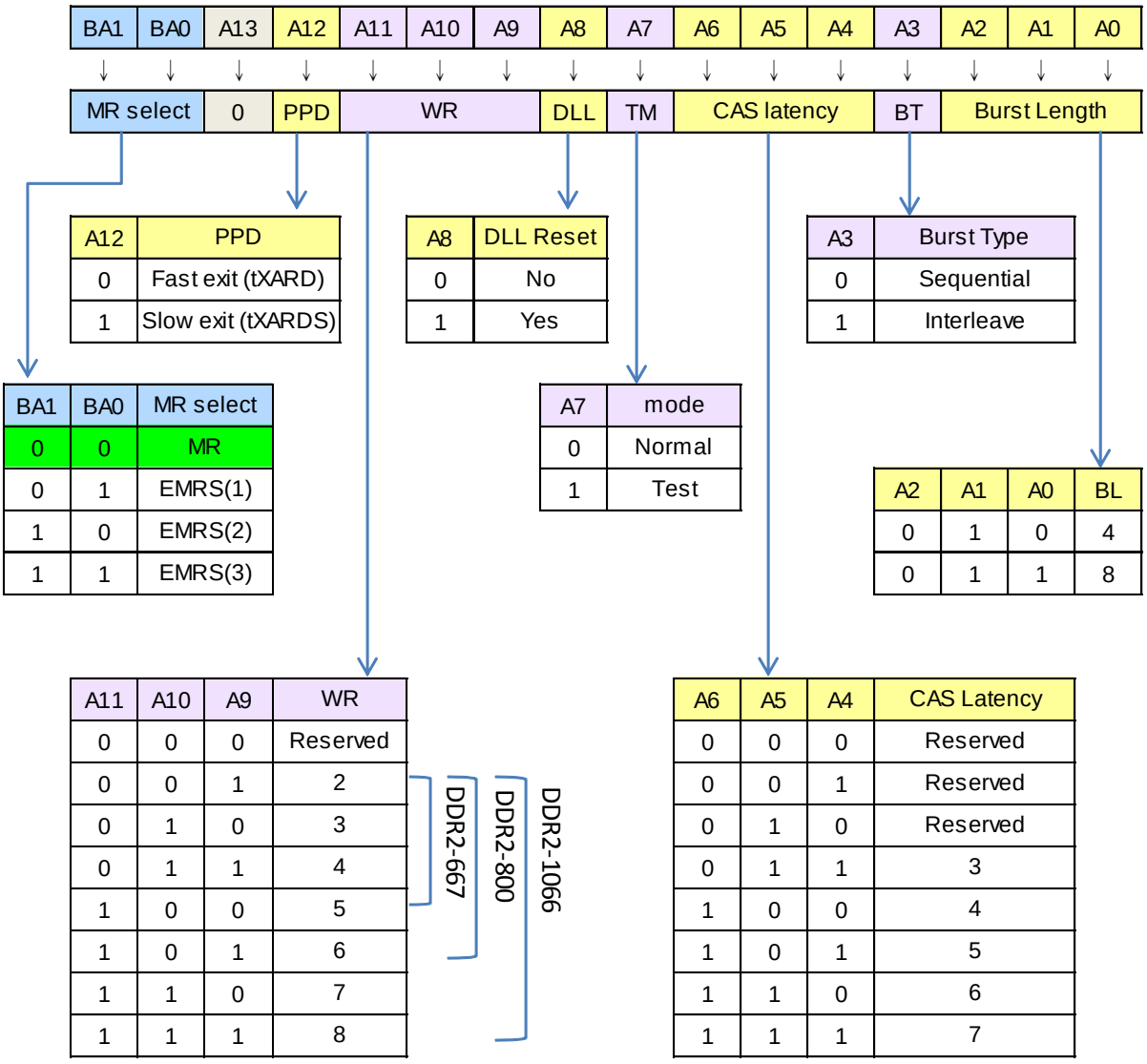
Programming the Mode Registration and Extended Mode Registers

For application flexibility, burst length, burst type, CAS latency, DLL reset function, write recovery time (tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, additive CAS latency, driver impedance, ODT (On Die Termination), single-ended strobe and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) and Extended Mode Registers (EMR (#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued. MRS, EMRS and DLL Reset do not affect array contents, which mean re-initialization including those can be executed any time after power-up without affecting array contents.

Mode Registration Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1 and BA1, while controlling the state of address pins A0 ~ A13. The DDR2 SDRAM should be in all banks precharged (idle) mode with CKE already high prior to writing into the mode register. The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharged state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst length. Burst address sequence type is defined by A3 and CAS latency is defined by A4 ~ A6. A7 is used for test mode and must be set to low for normal MRS operation. A8 is used for DLL reset. A9 ~ A11 are used for write recovery time (WR) definition for Auto-Precharge mode.

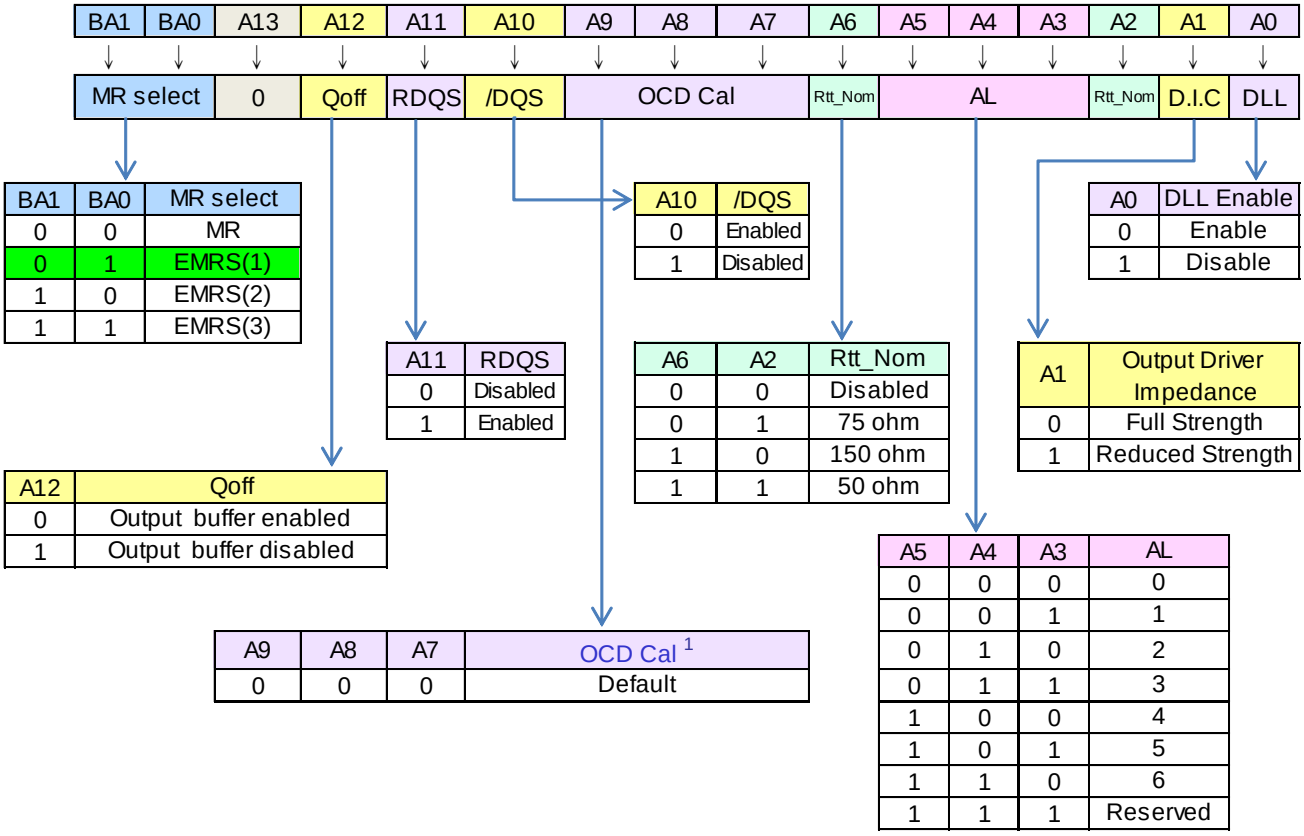
Mode Register – MR Programming



NOTE 1 Bits of Reserved for future use must be set to 0 when programming the MR.

NOTE 2 For DDR2-400/533, WR (write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = RU{ tWR[ns] / tCK[ns] }, where RU stands for round up). For DDR2-667/800/1066, WR min is determined by tCK(avg) max and WR max is determined by tCK(avg) min. WR[cycles] = RU{ tWR[ns] / tCK(avg)[ns] }, where RU stands for round up. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Extended Mode Register Set -EMRS (1) Programming



BA1	BA0	MR select
0	0	MR
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3)

A10	/DQS
0	Enabled
1	Disabled

A0	DLL Enable
0	Enable
1	Disable

A11	RDQS
0	Disabled
1	Enabled

A6	A2	Rtt_Nom
0	0	Disabled
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm

A1	Output Driver Impedance
0	Full Strength
1	Reduced Strength

A12	Qoff
0	Output buffer enabled
1	Output buffer disabled

A5	A4	A3	AL
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

A9	A8	A7	OCD Cal [1]
0	0	0	Default

Single-ended and Differential Data Strobe Signals

A11	A10	Strobe Function Matrix			
RDQS	$\overline{DQS}$	RDQS/DM	$\overline{RDQS}$	DQS	$\overline{DQS}$
0(Disable)	0(Enable)	DM	Hi-z	DQS	$\overline{DQS}$
0(Disable)	1(Disable)	DM	Hi-z	DQS	Hi-z
1(Enable)	0(Enable)	RDQS	$\overline{RDQS}$	DQS	$\overline{DQS}$
1(Enable)	1(Disable)	RDQS	Hi-z	DQS	Hi-z

NOTE 1 Default must be set to 0. OCD Calibration is unsupported.

NOTE 2 Bits of Reserved for future use must be set to 0 when programming the EMR(1).

NOTE 3 Output disabled - DQs, DQSs, $\overline{DQSs}$, RDQS, $\overline{RDQS}$. This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included.

NOTE 4 If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

Extended Mode Register Set –EMRS (1)

The extended mode register EMRS(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, $\overline{DQS}$ disable, OCD program, RQDS enable. The default value of the extended mode register EMRS(1) is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1, and high on BA0, while controlling the state of the address pins. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the EMRS (1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength output driver. A3-A5 determines the additive latency, A7-A9 are used for OCD control, A10 is used for $\overline{DQS}$ disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.

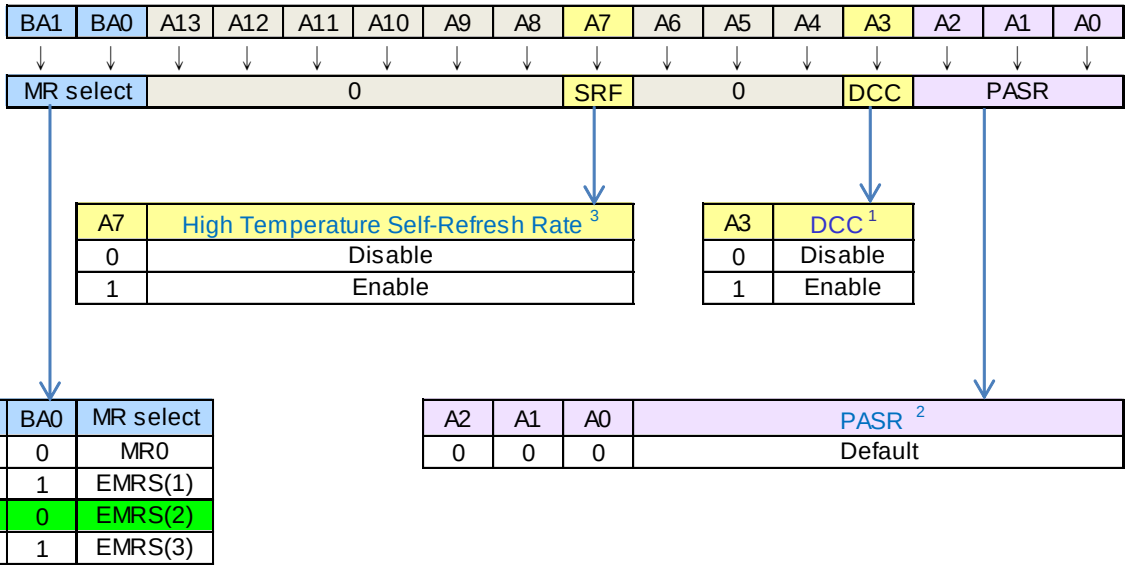
DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is reset, 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Less clock cycles may result in a violation of the t_{AC} or t_{DQSCK} parameters.

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Q_{off} bit in the EMRS (1) is set to 0). When the Q_{off} bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure I_{DD} currents during Read operations, without including the output buffer current and external load currents.

Extended Mode Register Set -EMRS (2) Programming



A7	High Temperature Self-Refresh Rate [3]
0	Disable
1	Enable

A3	DCC [1]
0	Disable
1	Enable

BA1	BA0	MR select
0	0	MR0
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3)

A2	A1	A0	PASR [2]
0	0	0	Default

NOTE 1 User can set the EMR(2) [A3] bit to enable DCC.

NOTE 2 Default must be set to 0. PASR is unsupported.

NOTE 3 Controller has to set the EMR(2)[A7] bit to enable the self-refresh rate in case of higher than 85 ℃ temperature self-refresh operation.

NOTE 4 Bits of Reserved for future use must be set to 0 when programming the EMR(2).

Extended Mode Register Set EMRS (2)

The Extended Mode Registers (2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, high on BA1, while controlling the states of address pin A0-A13. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register (2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

Extended Mode Register Set -EMRS (3) Programming

All bits in EMRS(3) expect BA0 and BA1 are reserved for future use and must be programmed to 0 when setting the mode register during initialization.

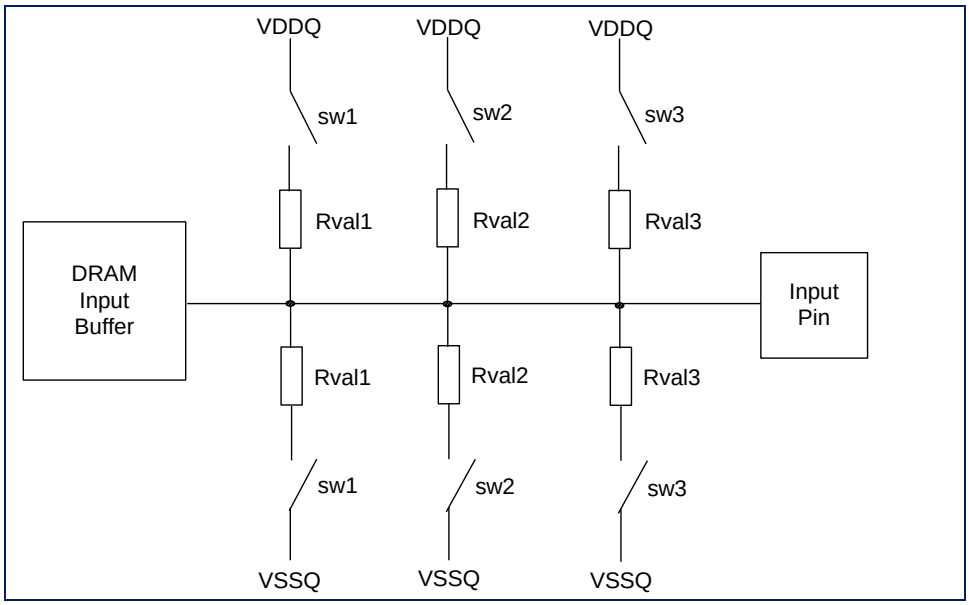
BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
1	1	0													

On-Die Termination (ODT)

ODT (On-Die Termination) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQ, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$, and DM signal for x16 configuration ODT is applied to each DQ, UDQS, $\overline{\text{UDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDM and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self-Refresh mode.

Functional Representation of ODT

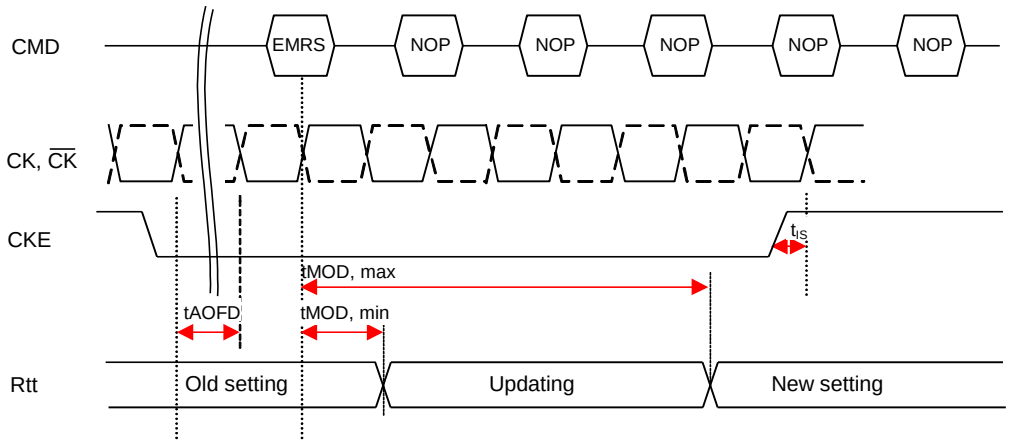


Switch sw1, sw2, or sw3 is enabled by the ODT pin. Selection between sw1, sw2, or sw3 is determined by “Rtt (nominal)” in EMRS. Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.

ODT related timings

MRS command to ODT update delay

During normal operation the value of the effective termination resistance can be changed with an EMRS command. The update of the Rtt setting is done between tMOD, min and tMOD, max, and CKE must remain HIGH for the entire duration of tMOD window for proper operation. The timings are shown in the following timing diagram.



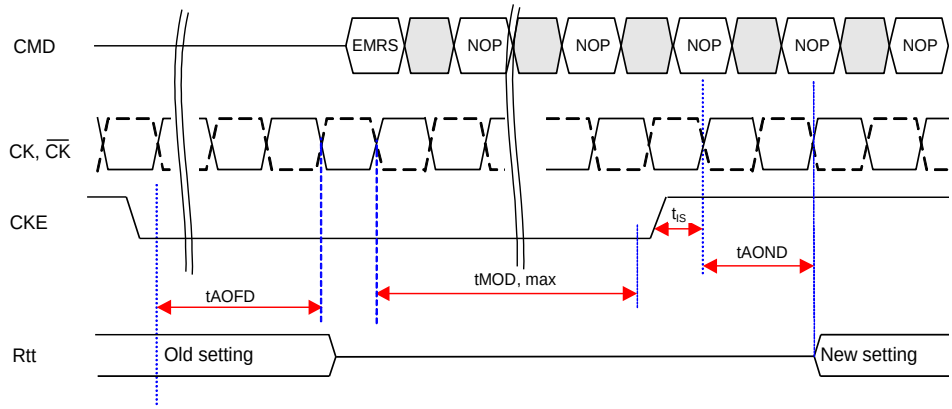
EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt(Nominal)
Setting in this diagram is the Register and I/O setting, not what is measured from outside.

However, to prevent any impedance glitch on the channel, the following conditions must be met.

- tAOFD must be met before issuing the EMRS command.
- ODT must remain LOW for the entire duration of tMOD window, until tMOD, max is met.

Now the ODT is ready for normal operation with the new setting, and the ODT may be raised again to turn on the ODT.

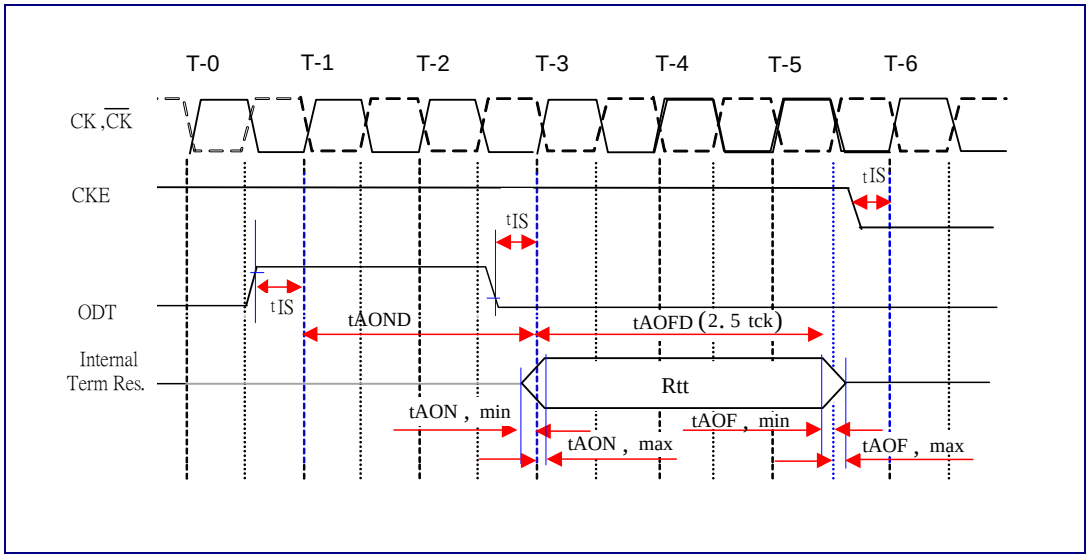
Following timing diagram shows the proper Rtt update procedure.



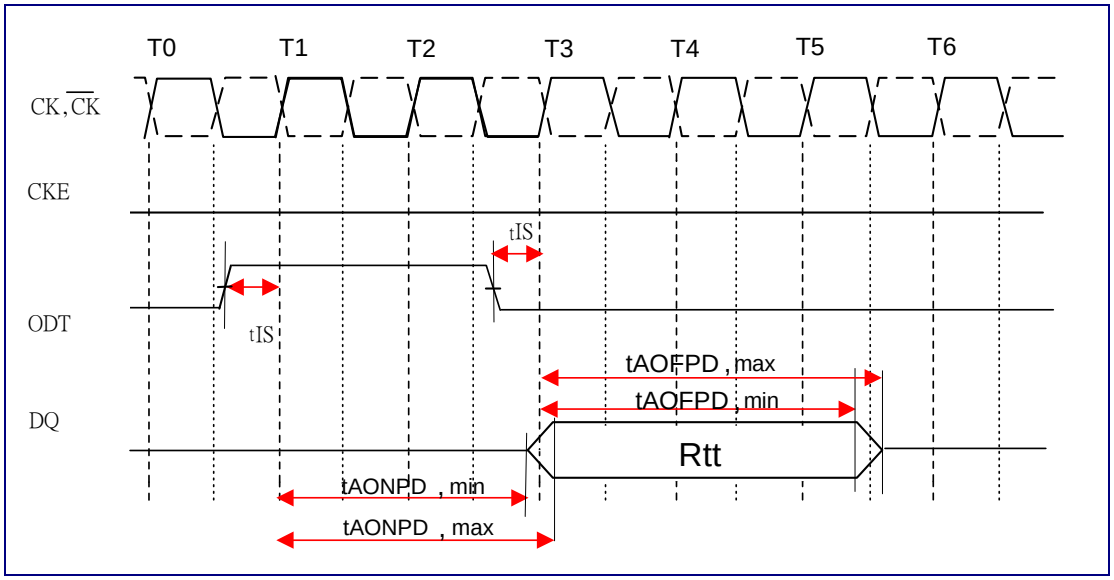
EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt(Nominal)
Setting in this diagram is the Register and I/O setting, not what is measured from outside.

ODT On/Off timings

ODT timing for active/standby mode



ODT Timing for Power-down mode



Bank Activate Command

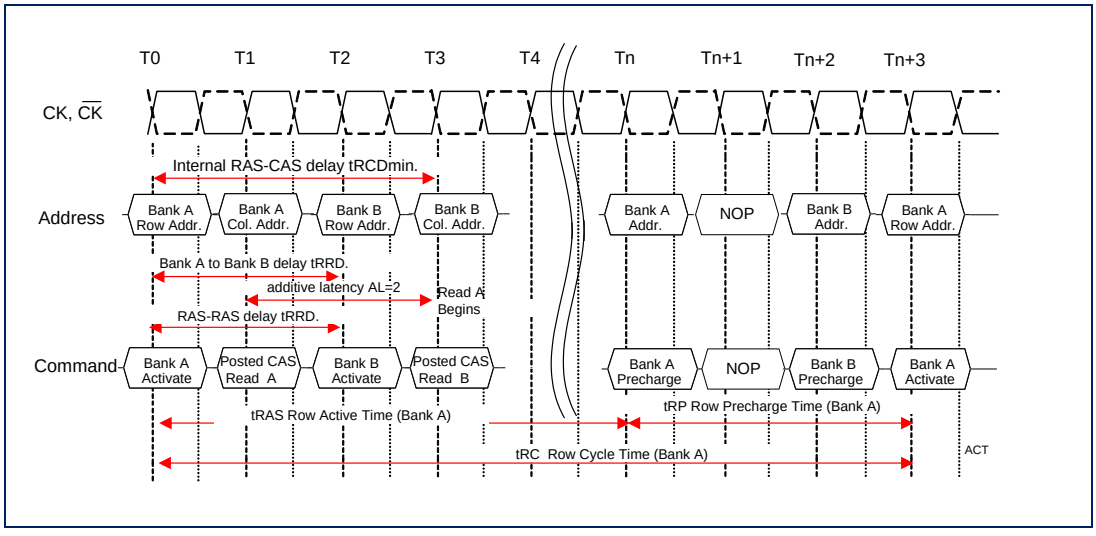
The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high plus $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 ~ BA1 are used to select the desired bank. Row addresses A0 through A13 have to be applied. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If an R/W command is issued to a bank that has not satisfied the t_{RCDmin} specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure t_{RCDmin} is satisfied. Additive latencies of 0, 1, 2, 3, 4, 5, and 6 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined (t_{RC}). The minimum time interval between Bank Active commands, to other bank, is the Bank A to Bank B delay time (t_{RRD}).

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules. One for restricting the number of sequential ACT commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are list as follow:

* 8 bank device sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW by tCK and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

*8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device will equal to tRP+tCK, where tRP is the value for a single bank pre-charge.

Bank Activate Command Cycle: t_{RCD} = 3, AL = 2, t_{RP} = 3, t_{RRD} = 2, t_{CCD} = 2



Read and Write Commands and Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low). The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is restricted to specific segments of the page length.

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL=8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively, and the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (t_{CCD}) is minimum 2 clocks for read or write cycles.

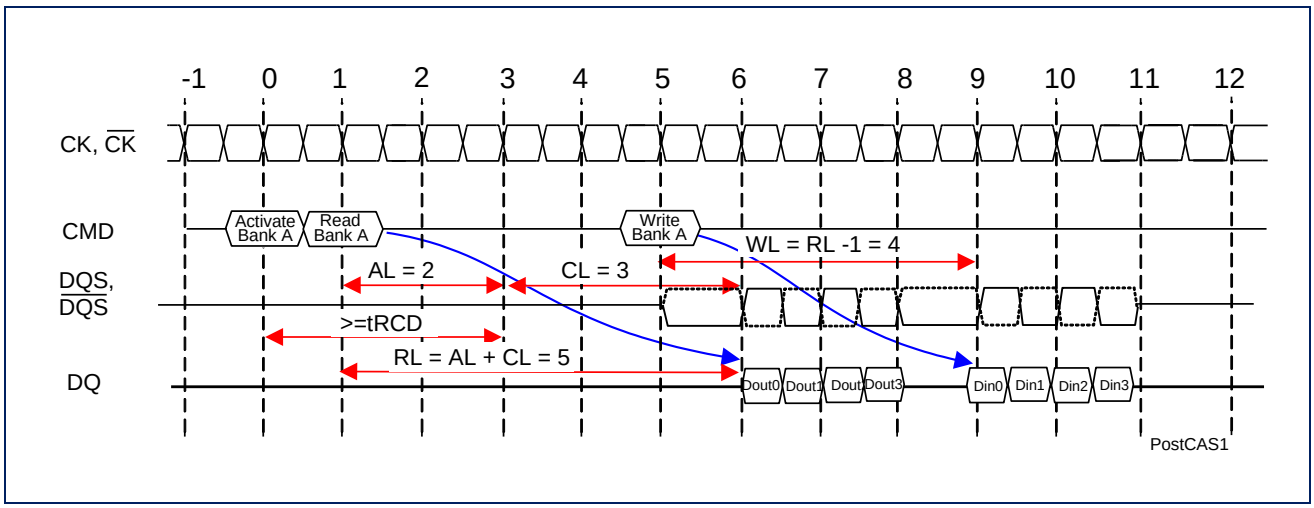
Posted $\overline{CAS}$

Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the $\overline{RAS}$ to $\overline{CAS}$ delay time, t_{RCD}, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the $\overline{CAS}$ latency (CL). Therefore if a user chooses to issue a Read/Write command before the tRCDmin, then AL greater than 0 must be written into the EMRS (1). The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus $\overline{CAS}$ latency (RL=AL+CL). If a user chooses to issue a Read command after the t_{RCDmin} period, the Read Latency is also defined as RL = AL + CL.

Example of posted $\overline{CAS}$ operation:

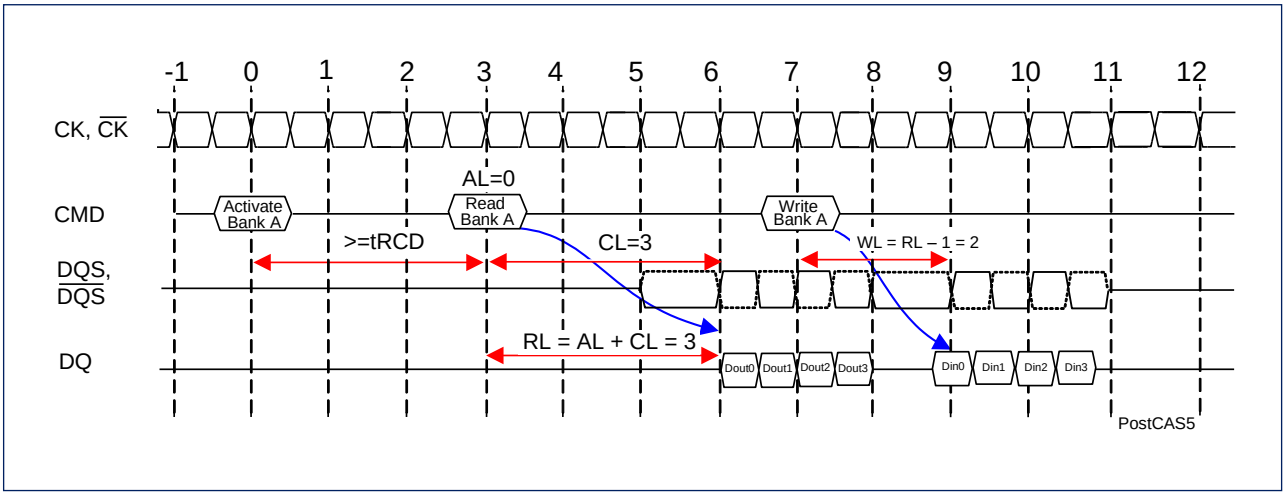
Read followed by a write to the same bank:

AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 4



Read followed by a write to the same bank:

AL = 0, CL = 3, RL = (AL + CL) = 3, WL = (RL -1) = 2, BL = 4



Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the “Burst Interruption “section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

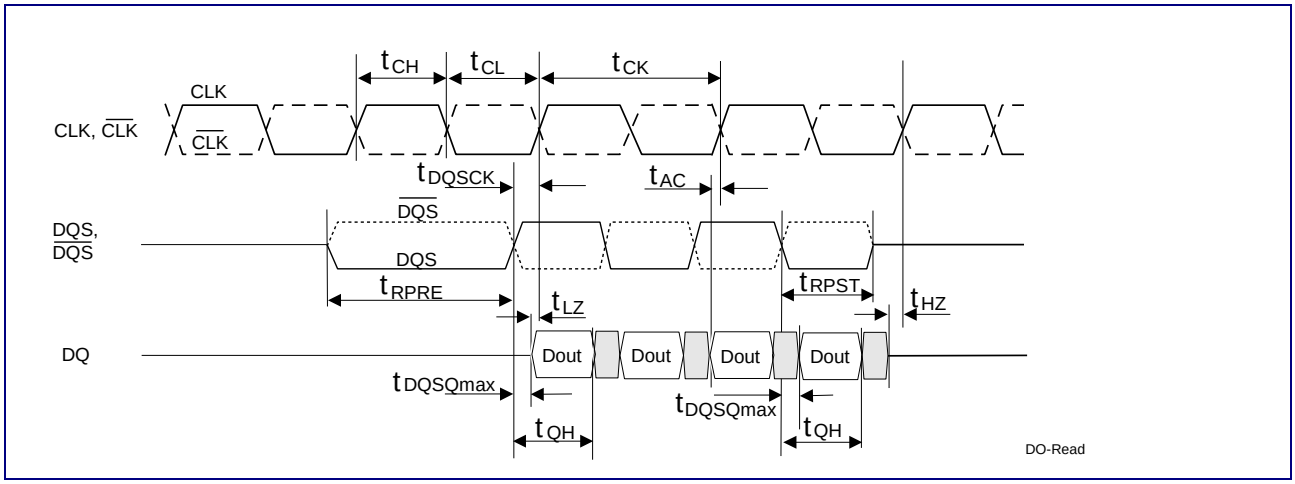
Burst Length and Sequence

Burst Length	Starting Address			Sequential Addressing (decimal)	Interleave Addressing (decimal)
	A2	A1	A0		
4	-	0	0	0, 1, 2, 3	0, 1, 2, 3
	-	0	1	1, 2, 3, 0	1, 0, 3, 2
	-	1	0	2, 3, 0, 1	2, 3, 0, 1
	-	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Burst Read Command

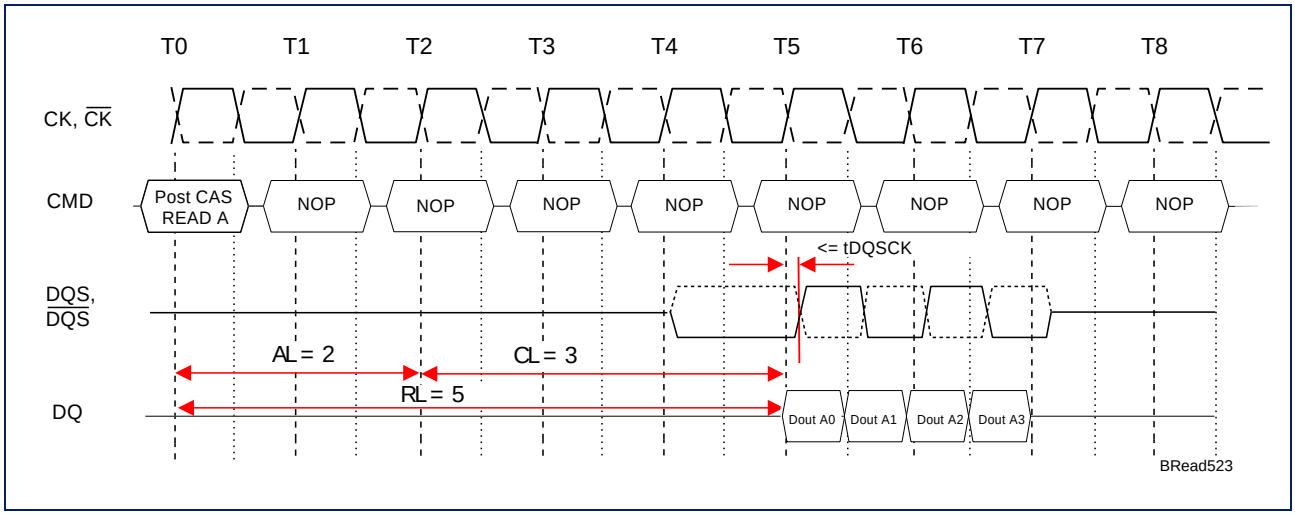
The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS (1))

Basic Burst Read Timing

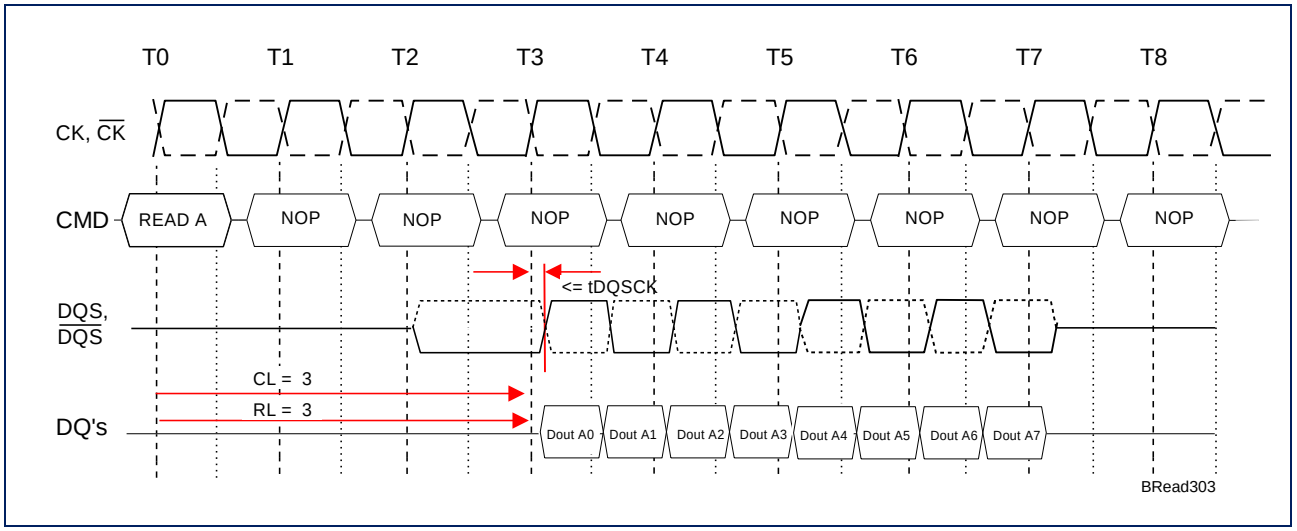


Examples:

Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)



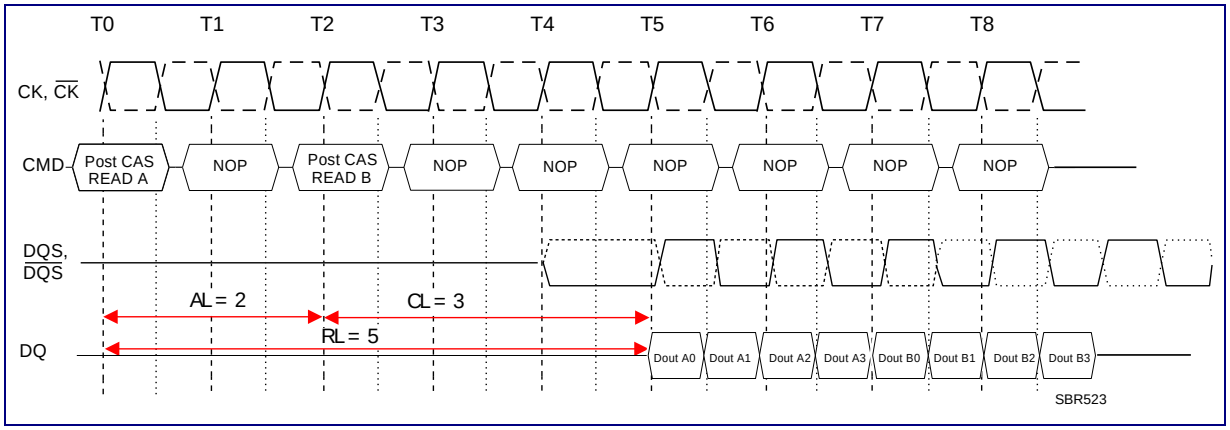
Burst Read Operation: RL = 3 (AL = 0, CL = 3, BL = 8)



Burst Read followed by Burst Write : RL = 5, WL = (RL-1) = 4, BL = 4

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around time(tRTW), which is 4 clocks in case of BL=4 operation, 6 clocks in case of BL=8 operation.

Seamless Burst Read Operation: RL = 5, AL = 2, CL = 3, BL = 4



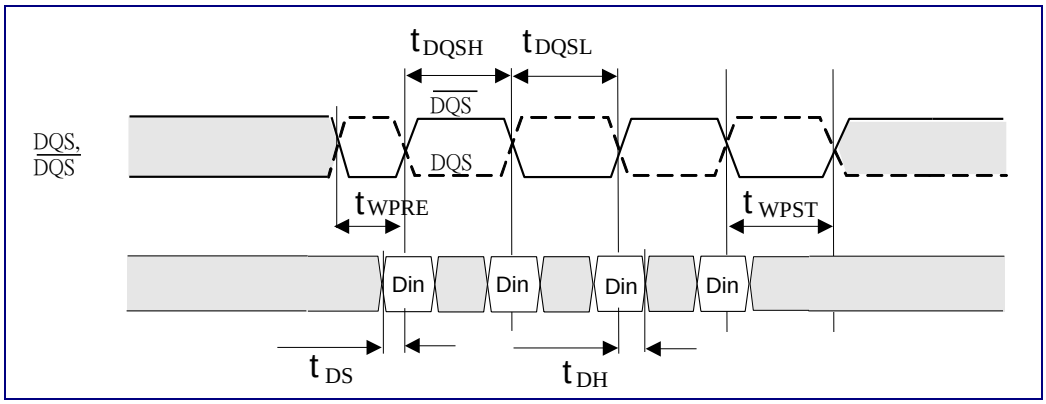
The seamless burst read operation's supported by enabling a read command at every clock for BL=4 operation, and every 4 clock for BL=8 operation. This operation allows regardless of same or different banks as long as the banks activated.

Burst Write Command

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) has to be driven low (preamble) a time tWPRE prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named "write recovery time" (WR).

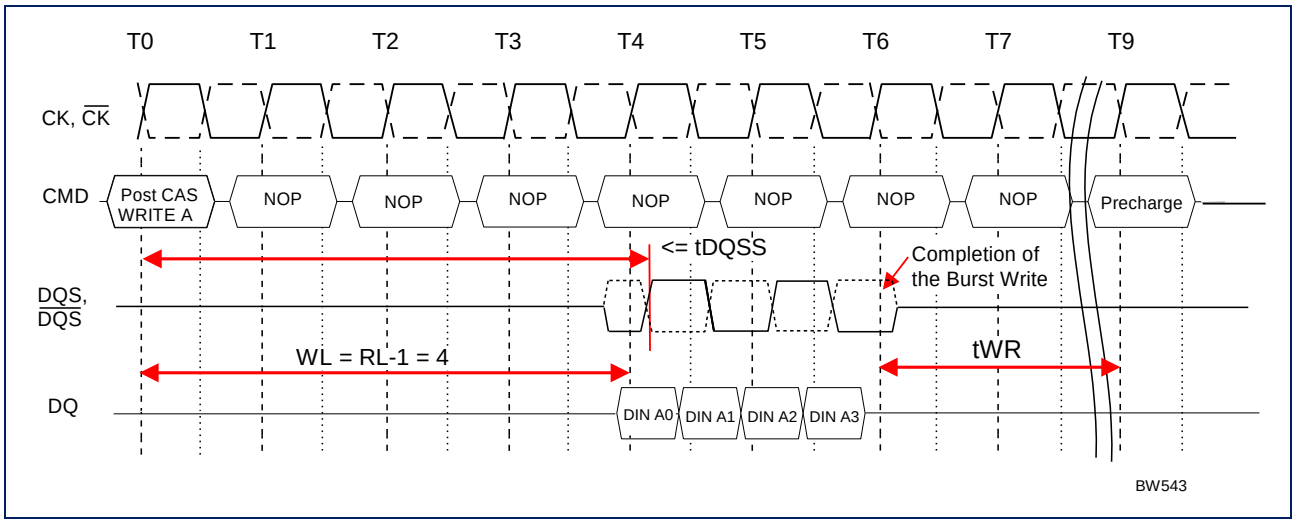
DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing measured is mode dependent.

Basic Burst Write Timing



Example:

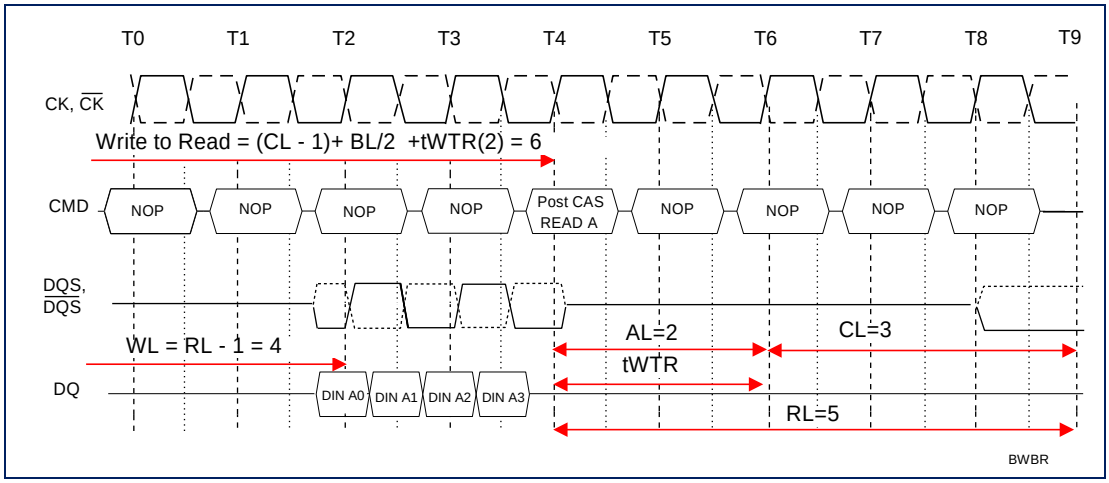
Burst Write Operation: RL = 5 (AL = 2, CL = 3), WL = 4, BL = 4



Burst Read followed by Burst Write : RL = 5, WL = (RL-1) = 4, BL = 4

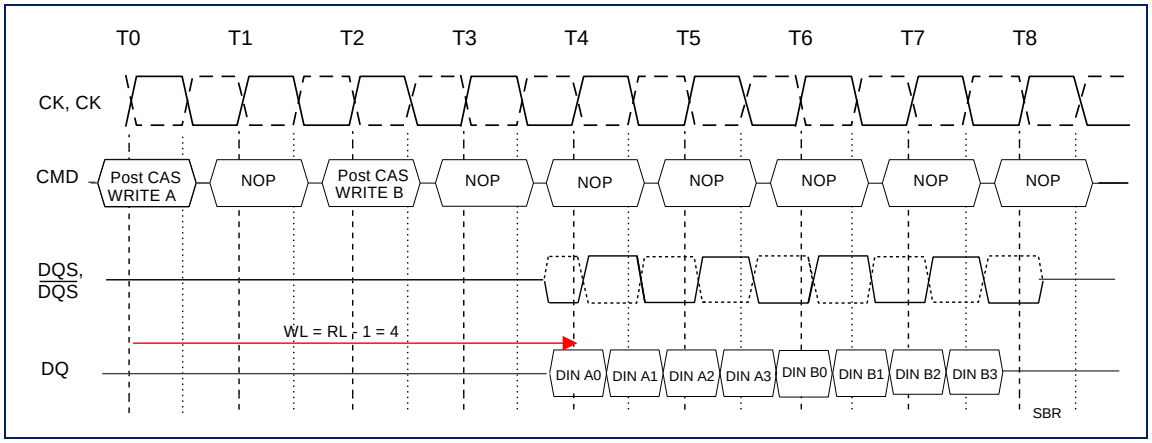
The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around time(tRTW), which is 4 clocks in case of BL=4 operation, 6 clocks in case of BL=8 operation.

Burst Write followed by Burst Read: RL = 5 (AL = 2, CL = 3), WL = 4, tWTR = 2, BL = 4



The minimum number of clocks from the burst write command to the burst read command is (CL - 1) +BL/2 + t_{WTR} where t_{WTR} is the write-to-read turn-around time t_{WTR} expressed in clock cycles. The t_{WTR} is not a write recovery time (t_{WR}) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.

Seamless Burst Write Operation: RL = 5, WL = 4, BL = 4

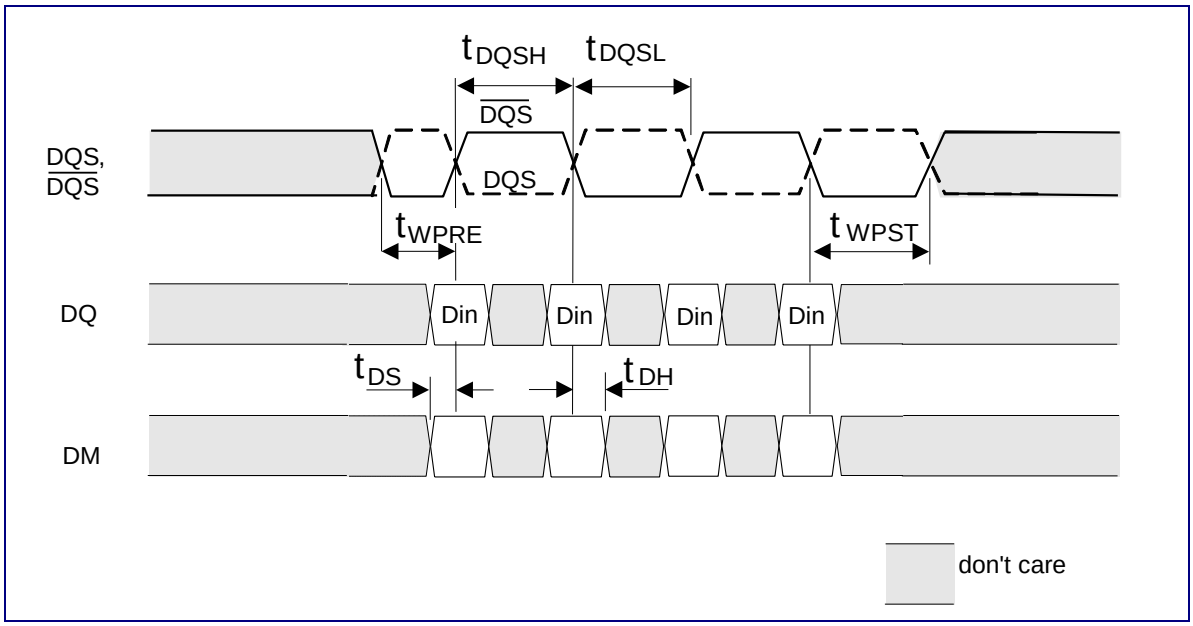


The seamless burst write operation is supported by enabling a write command every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

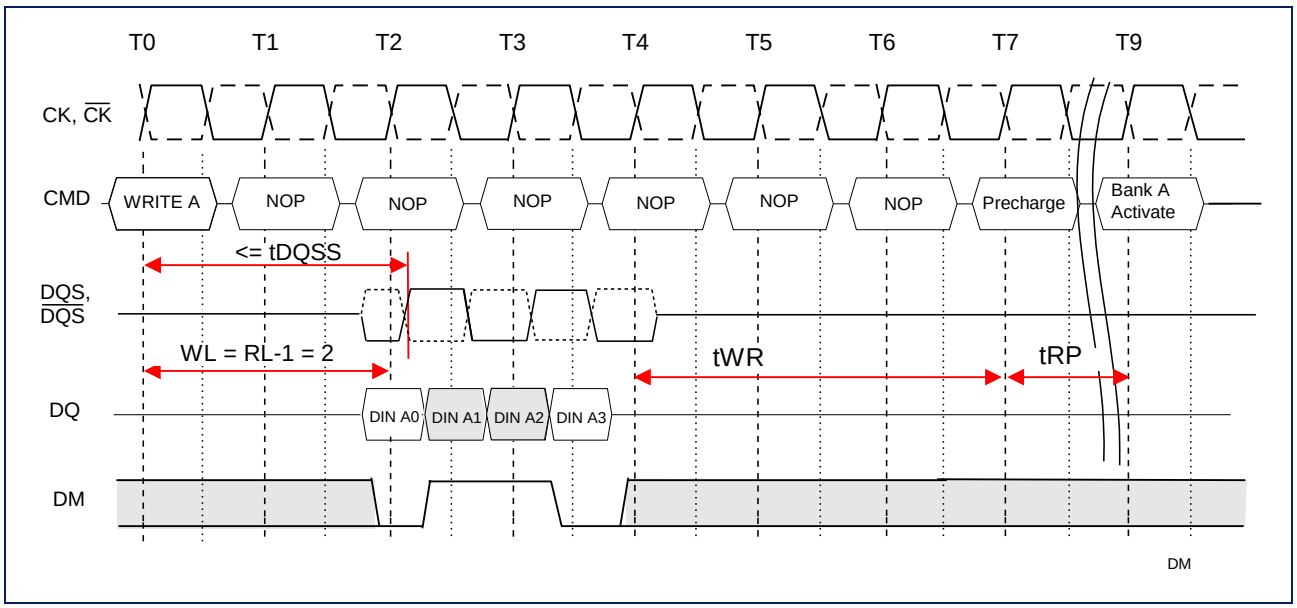
Write Data Mask

One write data mask input (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM of x16 bit organization is not used during read cycles.

Write Data Mask Timing



Burst Write Operation with Data Mask: RL = 3 (AL = 0, CL = 3), WL = 2, t_{WR} = 3, BL = 4



Burst Interruption

Interruption of a read or write burst is only allowed on burst of 8. Burst interrupt of 4 is prohibited.

Below are the constraints of burst interruption:

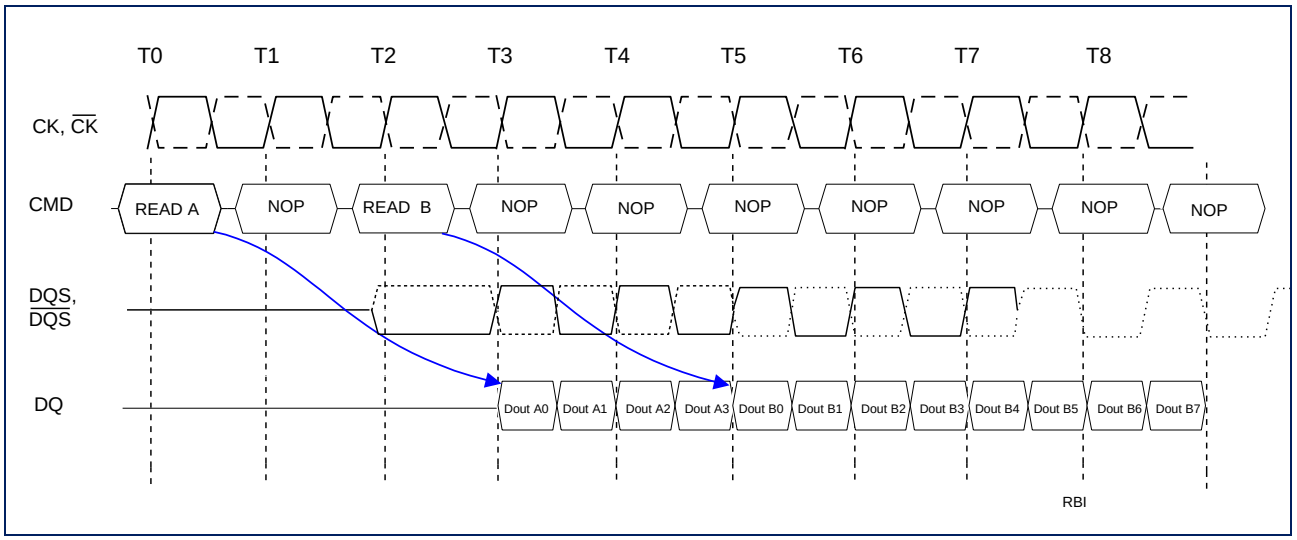
1. A Read Burst of 8 can only be interrupted by another Read command. Read burst interruption by a Write or Precharge Command is prohibited.
2. A Write Burst of 8 can only be interrupted by another Write command. Write burst interruption by a Read or Precharge Command is prohibited.
3. Read burst interrupt occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.
4. Write burst interrupt occur exactly two clocks after the previous Write command. Any other Read burst interrupt timings are prohibited.
3. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.
4. Read or Write burst with Auto-Precharge enabled is not allowed to be interrupted.
5. Read burst interruption is allowed by a Read with Auto-Precharge command.
6. Write burst interruption is allowed by a Write with Auto-Precharge command.

Notes:

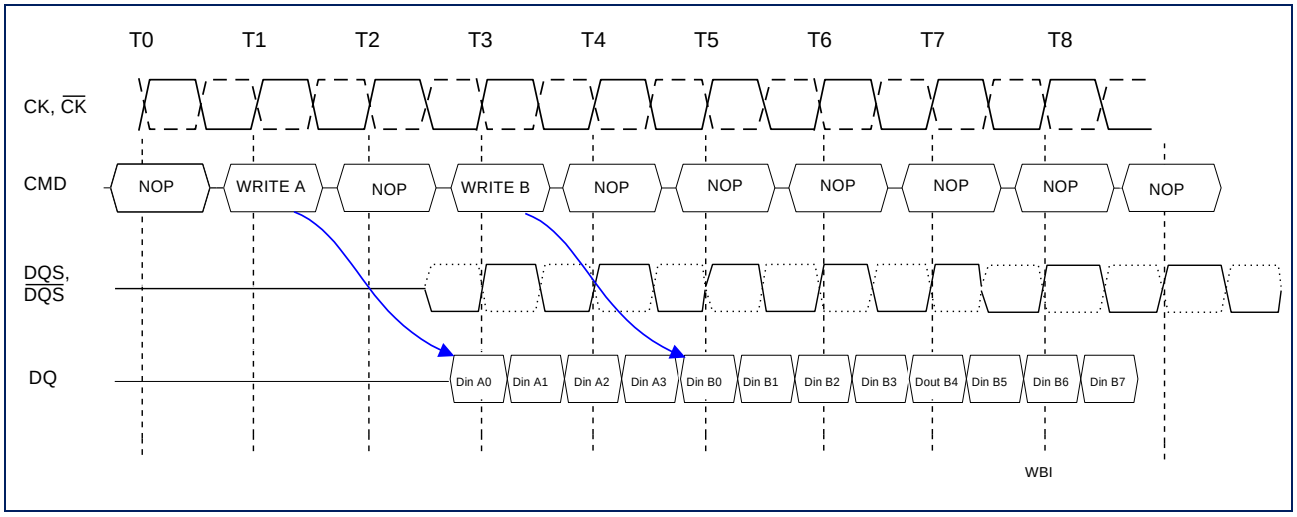
1. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt). Minimum Write to Precharge timing is WL + BL/ 2 + tWR, where tWR starts with the rising clock after the un-interrupted burst end and not form the end of the actual burst end.

Examples:

Read Burst Interrupt Timing Example: (CL = 3, AL = 0, RL = 3, BL = 8)



Write Burst Interrupt Timing Example: (CL = 3, AL = 0, WL = 2, BL = 8)



Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Pre-charge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0, and BA1 are used to define which bank to precharge when the command is issued.

Bank Selection for Precharge by Address Bit

A10	BA1	BA0	Precharge Bank(s)
LOW	LOW	LOW	Bank 0 only
LOW	LOW	HIGH	Bank 1 only
LOW	HIGH	LOW	Bank 2 only
LOW	HIGH	HIGH	Bank 3 only
HIGH	Don't Care	Don't Care	All banks

Burst Read Operation Followed by a Precharge

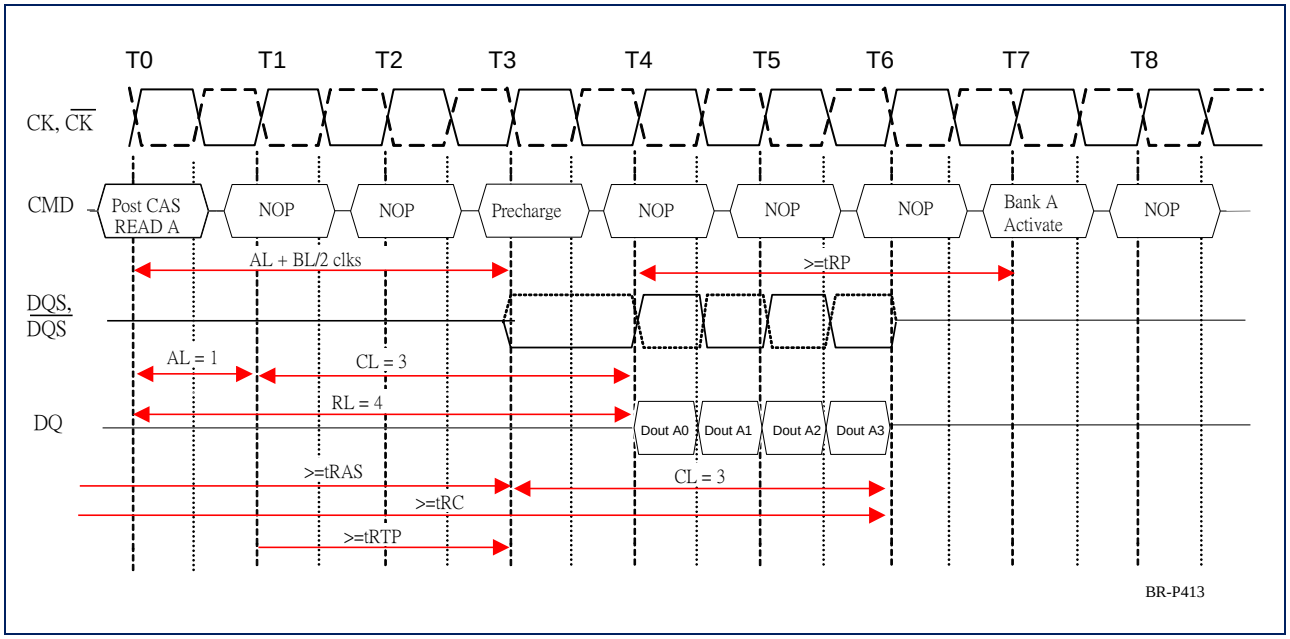
Minimum Read to Precharge command spacing to the same bank = AL + BL/2 + max (RTP, 2) - 2 clocks.

For the earliest possible precharge, the Precharge command may be issued on the rising edge which is “Additive Latency (AL) + BL/2 clocks” after a Read Command, as long as the minimum tRAS timing is satisfied.

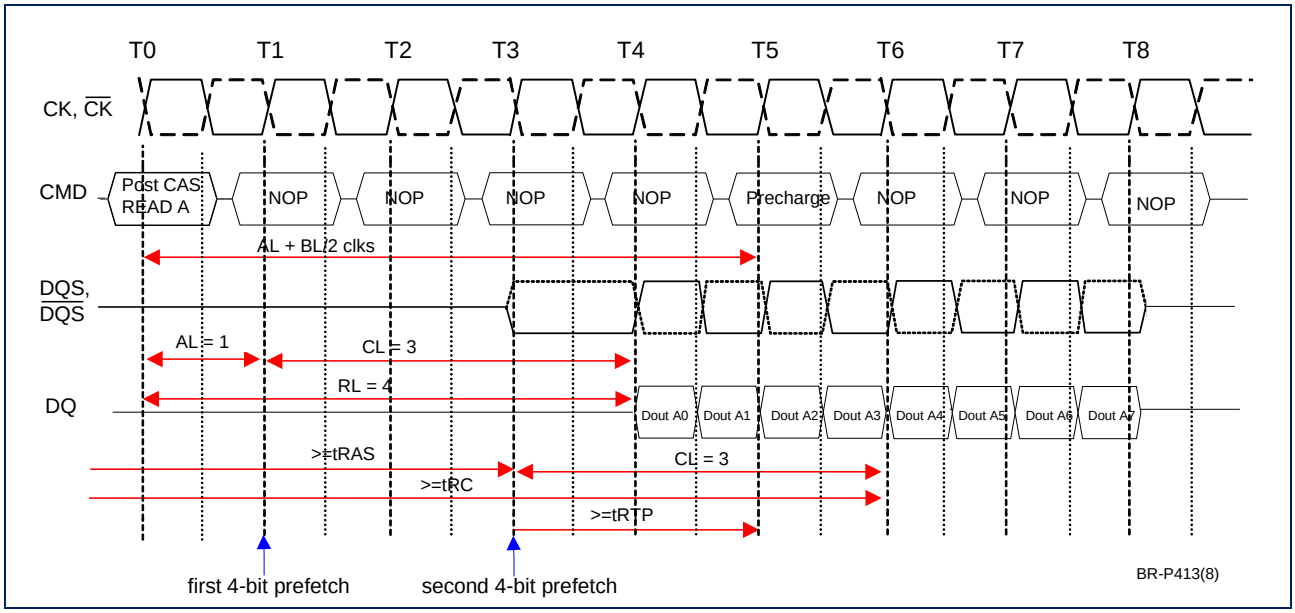
The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is call tRTP (Read to Precharge). For BL=4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL=8 this is the time from AL + 2 clocks after the Read to the Precharge command.

Examples:

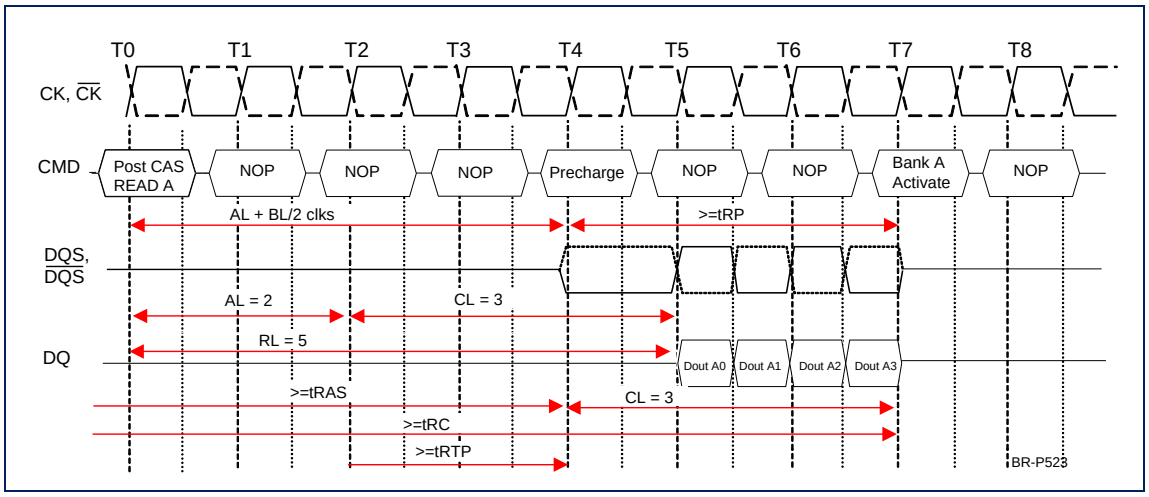
Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 4, t_{RTP} ≦ 2 clocks



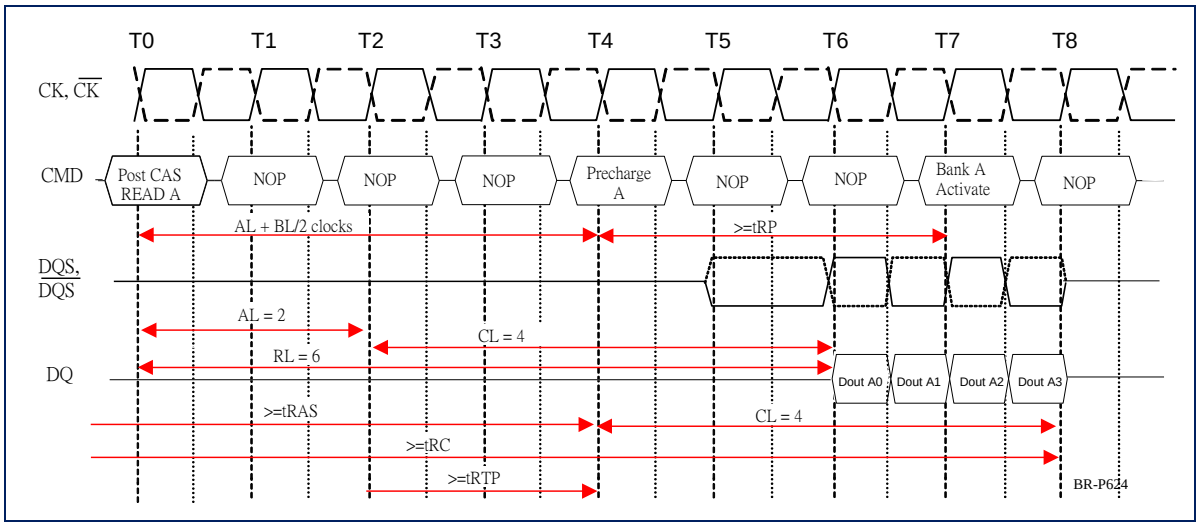
Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 8, t_{RTP} ≦ 2 clocks



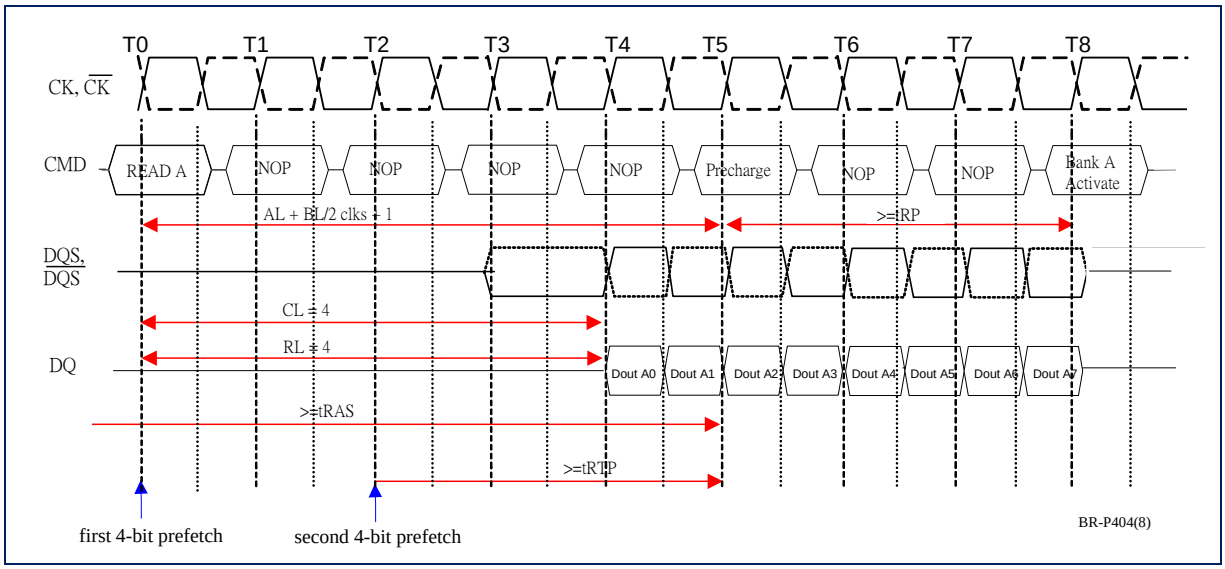
Burst Read Operation Followed by Precharge: RL = 5 (AL = 2, CL = 3), BL = 4, t_{RTP} ≦ 2 clocks



Burst Read Operation Followed by Precharge: RL = 6, (AL = 2, CL = 4), BL = 4, t_{RTP} ≦ 2 clocks



Burst Read Operation Followed by Precharge: RL = 4, (AL = 0, CL = 4), BL = 8, t_{RTP} > 2 clocks

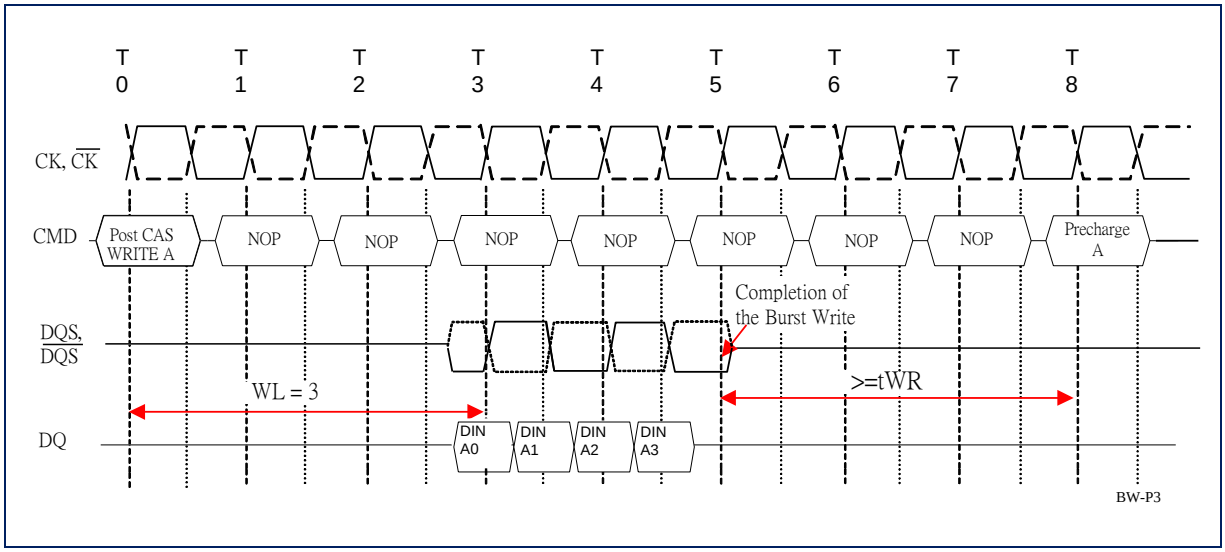


Burst Write followed by Precharge

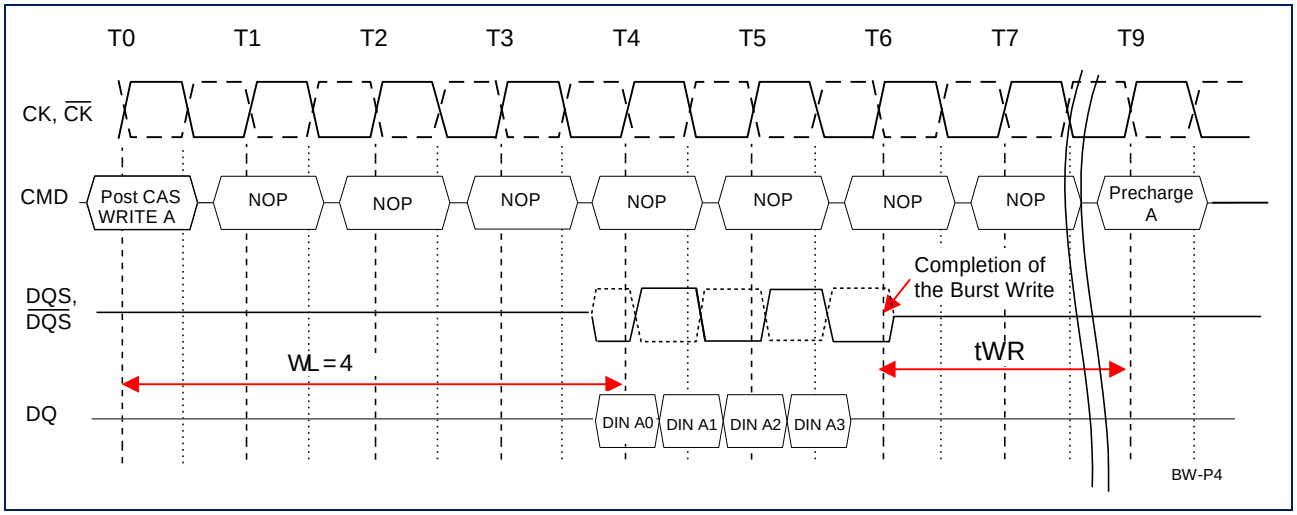
Minimum Write to Precharge command spacing to the same bank = **WL + BL/2 + t_{WR}**. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the burst write to the Precharge command. No Precharge command should be issued prior to the t_{WR} delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. t_{WR} is an analog timing parameter (see the AC table in this datasheet) and is not the programmed value for t_{WR} in the MRS.

Examples:

Burst Write followed by Precharge : WL = (RL - 1) = 3, BL = 4, t_{WR} = 3



Burst Write followed by Precharge : WL = (RL - 1) = 4, BL = 4, t_{WR} = 3



Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Pre-charge Command or the Auto-Precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the Auto-Precharge function is enabled. During Auto-Precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge internally on the rising edge which is $\overline{CAS}$ Latency (CL) clock cycles before the end of the read burst. Auto-Precharge is also implemented for Write Commands. The precharge operation engaged by the Auto-Precharge command will not begin until the last data of the write burst sequence is properly stored in the memory array. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{CAS}$ Latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed so that the Auto-Precharge command may be issued with any read or write command.

Burst Read with Auto-Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if t_{RAS}(min) and t_{RTP} are satisfied. If t_{RAS}(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until t_{RAS}(min) is satisfied. If t_{RTP}(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until t_{RTP}(min) is satisfied.

In case the internal precharge is pushed out by t_{RTP}, t_{RP} starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + t_{RTP} + t_{RP}. For BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + t_{RTP} + t_{RP}. Note that both parameters t_{RTP} and t_{RP} have to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:

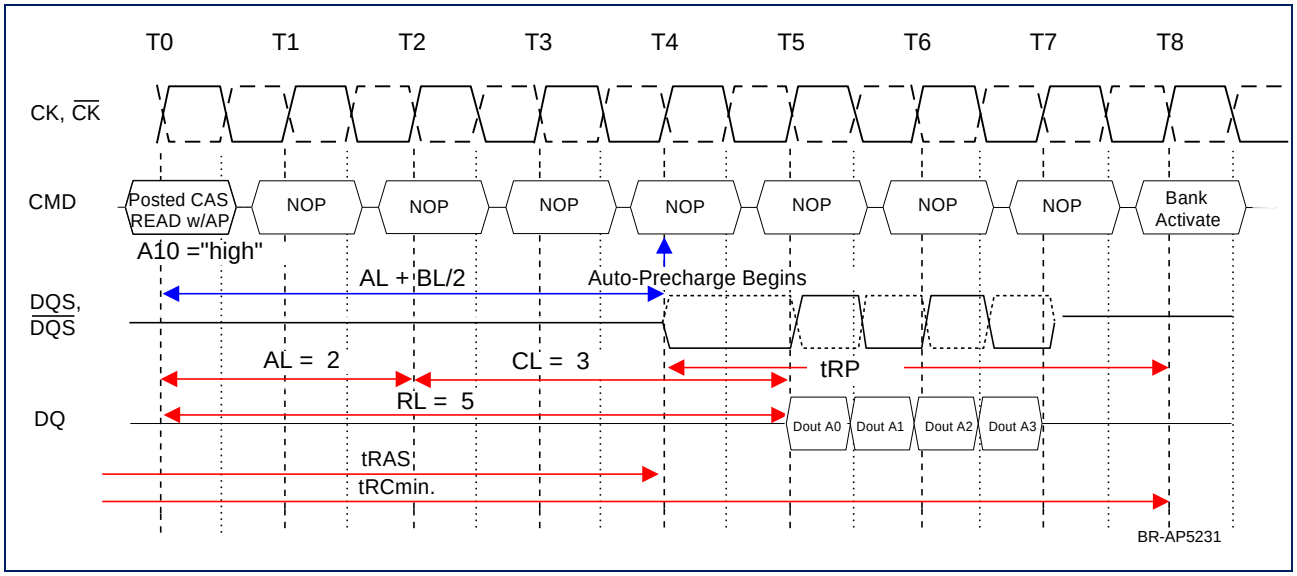
(1) The $\overline{RAS}$ precharge time (t_{RP}) has been satisfied from the clock at which the Auto-Precharge begins.

(2) The $\overline{RAS}$ cycle time (t_{RC}) from the previous bank activation has been satisfied.

Examples:

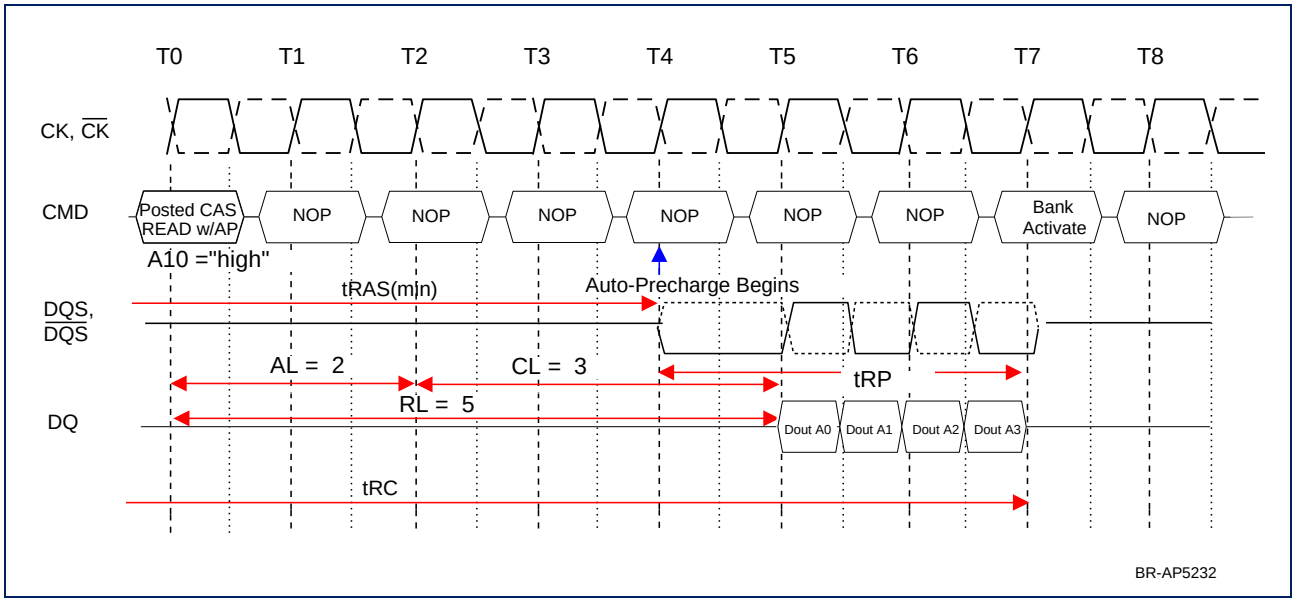
Burst Read with Auto-Precharge followed by an activation to the Same Bank (t_{RC} Limit)

RL = 5 (AL = 2, CL = 3), BL = 4, t_{RTP} ≦ 2 clocks



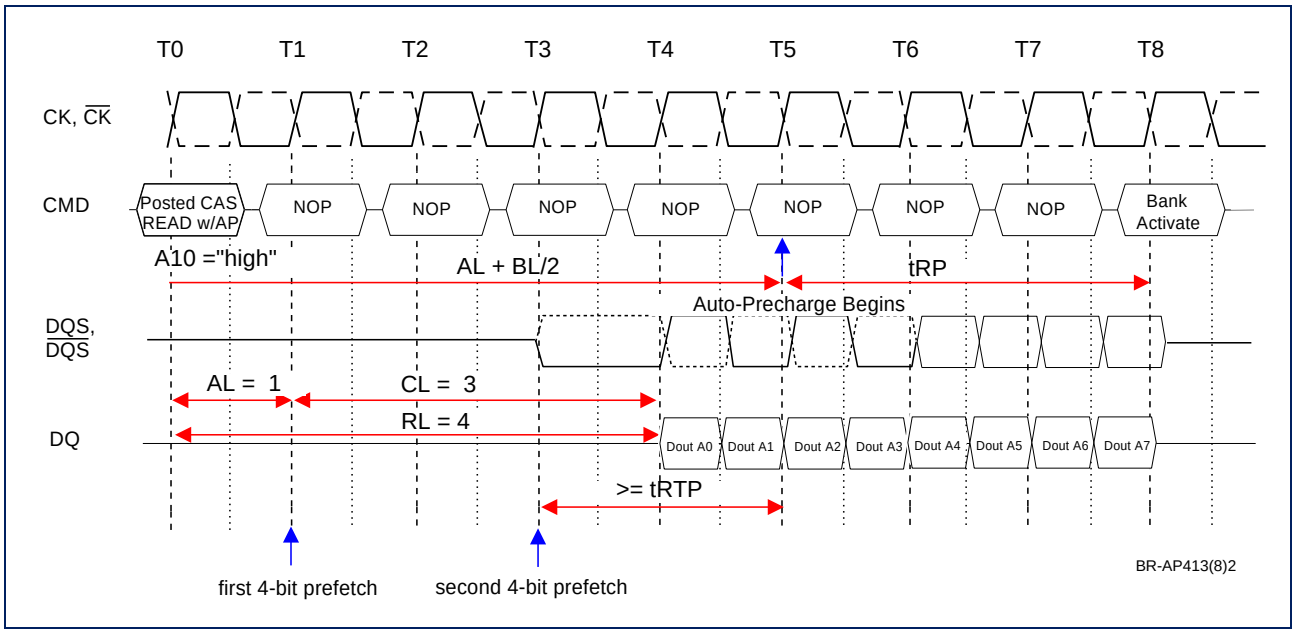
Burst Read with Auto-Precharge followed by an Activation to the Same Bank (tRAS Limit):

RL = 5 (AL = 2, CL = 3), BL = 4, tRTP ≦ 2 clocks



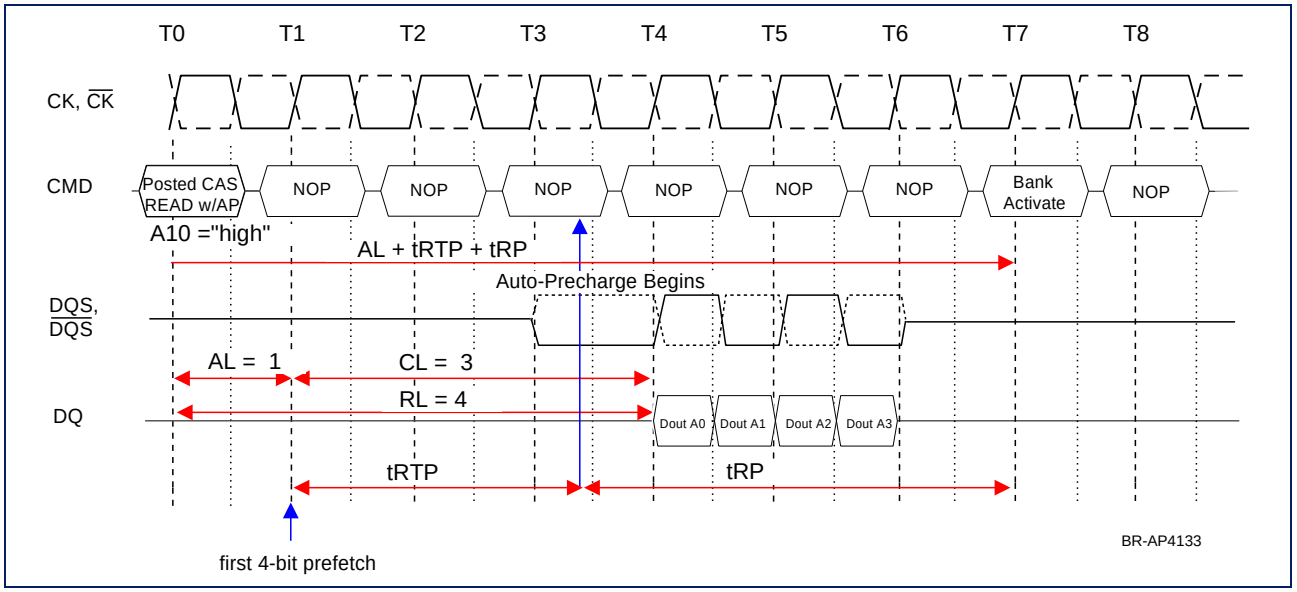
Burst Read with Auto-Precharge followed by an Activation to the Same Bank:

RL = 4 (AL = 1, CL = 3), BL = 8, t_{RTP} ≦ 2 clocks



Burst Read with Auto-Precharge followed by an Activation to the Same Bank:

RL = 4 (AL = 1, CL = 3), BL = 4, t_{RTP} > 2 clocks



Burst Write with Auto-Precharge

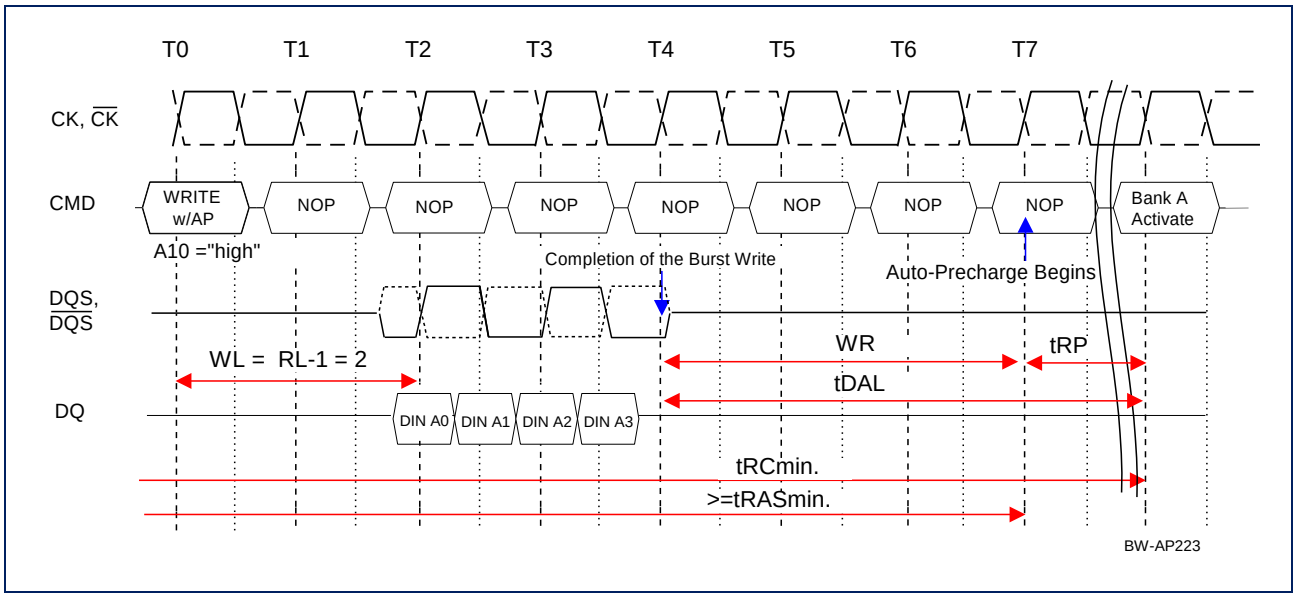
If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the write burst plus the write recovery time delay (WR), programmed in the MRS register, as long as t_{RAS} is satisfied. The bank undergoing Auto-Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

(1) The last data-in to bank activate delay time (t_{DAL} = WR + t_{RP}) has been satisfied.

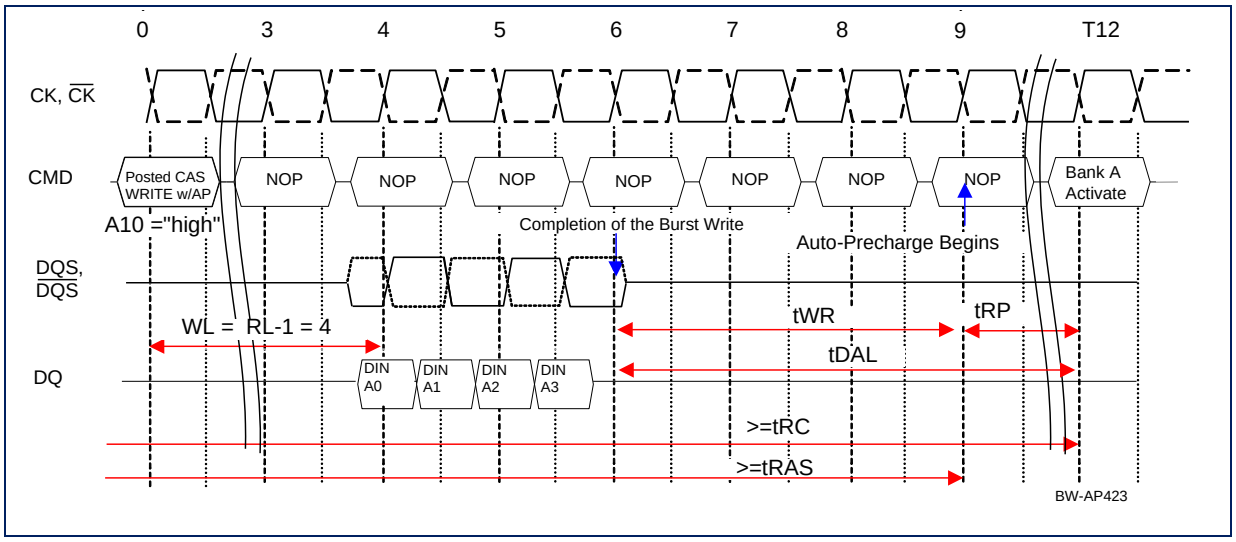
(2) The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Examples:

Burst Write with Auto-Precharge (t_{RC} Limit): WL = 2, t_{DAL} = 6 (WR = 3, t_{RP} = 3), BL = 4



Burst Write with Auto-Precharge (t_{WR} + t_{RP} Limit) : WL = 4, t_{DAL} = 6 (t_{WR} = 3, t_{RP} = 3), BL = 4



Precharge & Auto Precharge Clarification

From Command	To Command	Minimum Delay between "From command" to "to command"	Units	Note
Read	Precharge (to same Bank as Read)	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
	Precharge All	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
Read w/AP	Precharge (to same Bank as Read w/AP)	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
	Precharge All	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
Write	Precharge (to same Bank as Write)	WL + BL/2 + tWR	tCK	2
	Precharge All	WL + BL/2 + tWR	tCK	2
Write w/AP	Precharge (to same bank as Write w/AP)	WL + BL/2 + WR	tCK	2
	Precharge All	WL + BL/2 + WR	tCK	2
Precharge	Precharge (to same bank as Precharge)	1	tCK	2
	Precharge All	1	tCK	2
Precharge All	Precharge	1	tCK	2
	Precharge All	1	tCK	2

Note:

1) RTP [cycles] = RU {tRTP(ns)/tCK(ns)}, where RI stands for round up.

2) For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP or tRPa depending on the latest precharge command issued to that bank.

Refresh

SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit Auto-Refresh command, or by an internally timed event in Self-Refresh mode. Dividing the number of device rows into the rolling 64 ms interval defined the average refresh interval t_{REFI}, which is a guideline to control for distributed refresh timing.

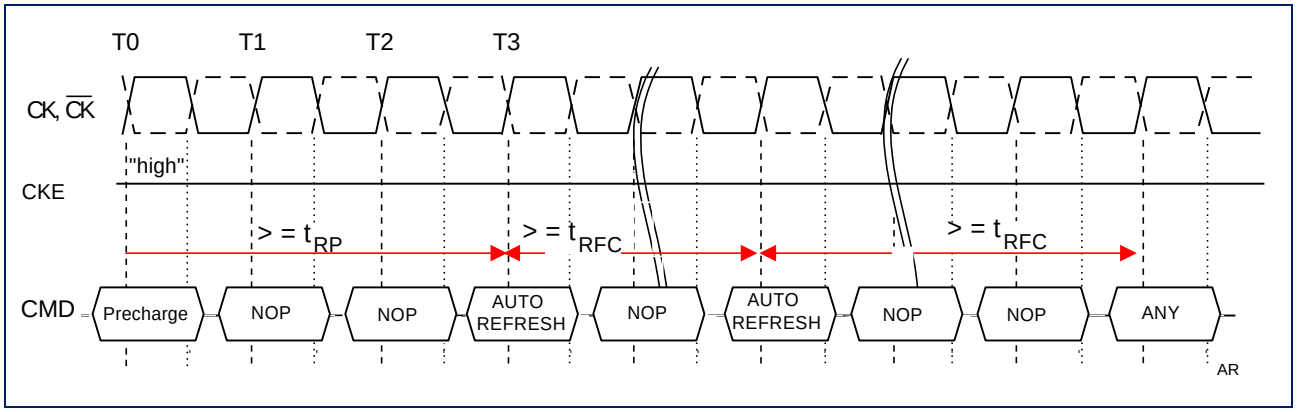
Auto-Refresh Command

Auto-Refresh is used during normal operation of the DDR2 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits ”Don’t Care” during an Auto-Refresh command. The DDR2 SDRAM requires Auto-Refresh cycles at an average periodic interval of t_{REFI} (maximum).

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Auto-Refresh mode. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time (t_{RP}) before the Auto-Refresh Command can be applied. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto-Refresh Command and the next Activate Command or subsequent Auto-Refresh Command must be greater than or equal to the Auto-Refresh cycle time (t_{RFC}).

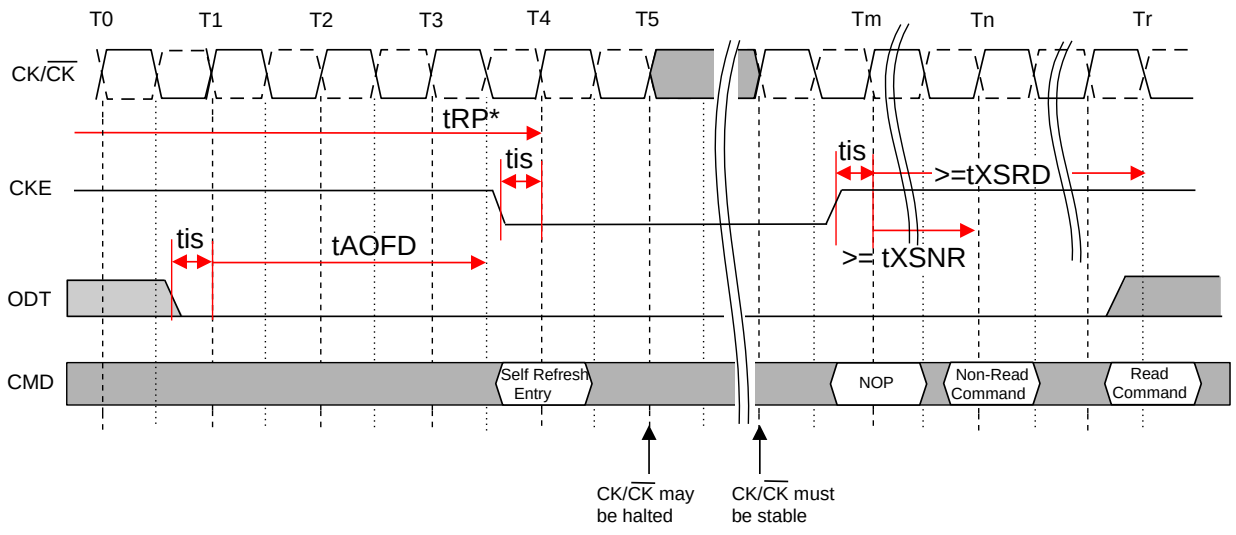
To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Auto-Refresh command and the next Auto-Refresh command is 9 * t_{REFI}.



Self-Refresh Command

The Self-Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR2 SDRAM retains data without external clocking.

The DDR2 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{CKE}$ held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS (1) command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the DDR2 SDRAM has entered Self-Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self-Refresh operation. Once Self-Refresh Exit command is registered, a delay equal or longer than the t_{XSNR} or t_{XSRD} must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self-Refresh exit period (t_{XSNR} or t_{XSRD}) for proper operation. NOP or DESELECT commands must be registered on each positive clock edge during the Self-Refresh exit interval. Since the ODT function is not supported during Self-Refresh operation, ODT has to be turned off t_{AOFD} before entering Self-Refresh Mode and can be turned on again when the t_{XSRD} timing is satisfied.



* Device must be in theing "All banks idle" state to enter Self Refresh mode.
* ODT must be turned off prior to entering Self Refresh mode.
* tXSRD (>=200 tCK) has to be satisfied for a Read or as Read with Auto-Precharge commend.
* tXSNR has to be satisfied for any command execept Read or a Read with Auto-Precharge command, where tXSNR is defined as tRFC + 10ns.
* The minium CKE low time is defined by the $t_{CKEmin.}$ timming parameter.
* Since CKE is an SSTL input, V_{REF} must maintained during Self-Refresh.

Power-Down

Power-down is synchronously entered when CKE is registered low, along with NOP or Deselect command. CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any other operation such as row activation, Precharge, Auto-Precharge or Auto-Refresh is in progress, but power-down IDD specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are precharged, this mode is referred to as *Precharge Power-down*; if power-down occurs when there is a row active in any bank, this mode is referred to as *Active Power-down*. For Active *Power-down* two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to "low" this mode is referred as "standard active power-down mode" and a fast power-down exit timing defined by the t_{XARD} timing parameter can be used. When A12 is set to "high" this mode is referred as a power saving "low power active power-down mode". This mode takes longer to exit from the power-down mode and the t_{XARDS} timing parameter has to be satisfied.

Entering power-down deactivates the input and output buffers, excluding CK, CK, ODT and CKE. Also the DLL is disabled upon entering Precharge Power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are "Don't Care". Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, t_{XP}, t_{XARD} or t_{XARDS}, after CKE goes high. Power-down exit latencies are defined in the AC spec table of this data sheet.

Power-Down Entry

Active Power-down mode can be entered after an activate command. *Precharge Power-down* mode can be entered after a precharge, Precharge-All or internal precharge command. It is also allowed to enter power-mode after an Auto-Refresh command or MRS / EMRS(1) command when t_{MRD} is satisfied.

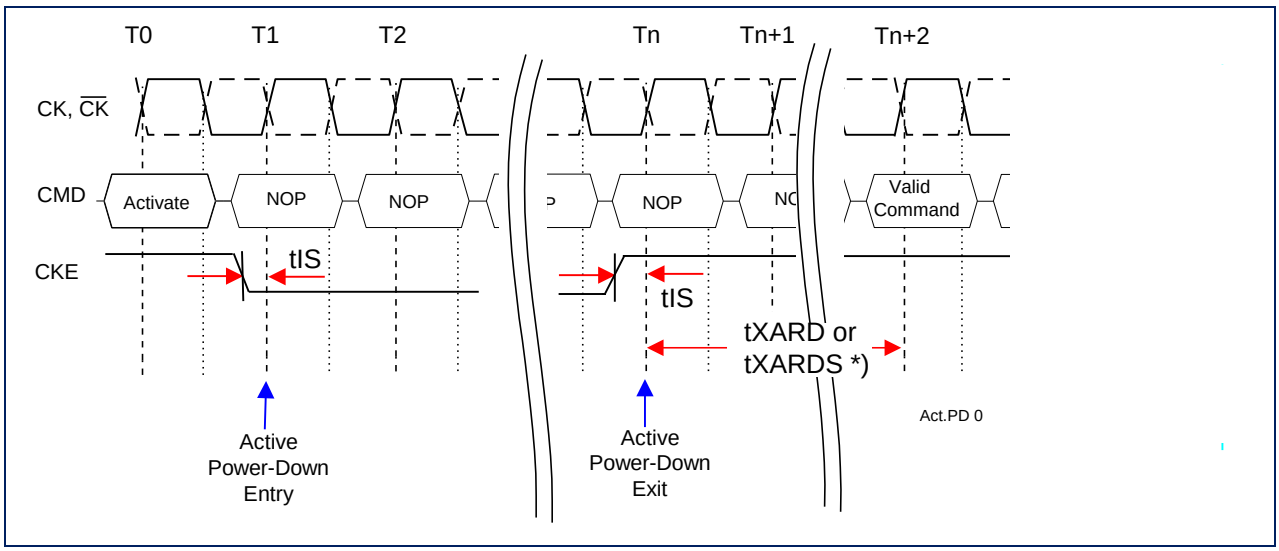
Active Power-down mode entry is prohibited as long as a Read Burst is in progress, meaning CKE should be kept high until the burst operation is finished. Therefore Active Power-Down mode entry after a Read or Read with Auto-Precharge command is allowed after RL + BL/2 is satisfied.

Active Power-down mode entry is prohibited as long as a Write Burst and the internal write recovery is in progress. In case of a write command, active power-down mode entry is allowed then WL + BL/2 + tWTR is satisfied.

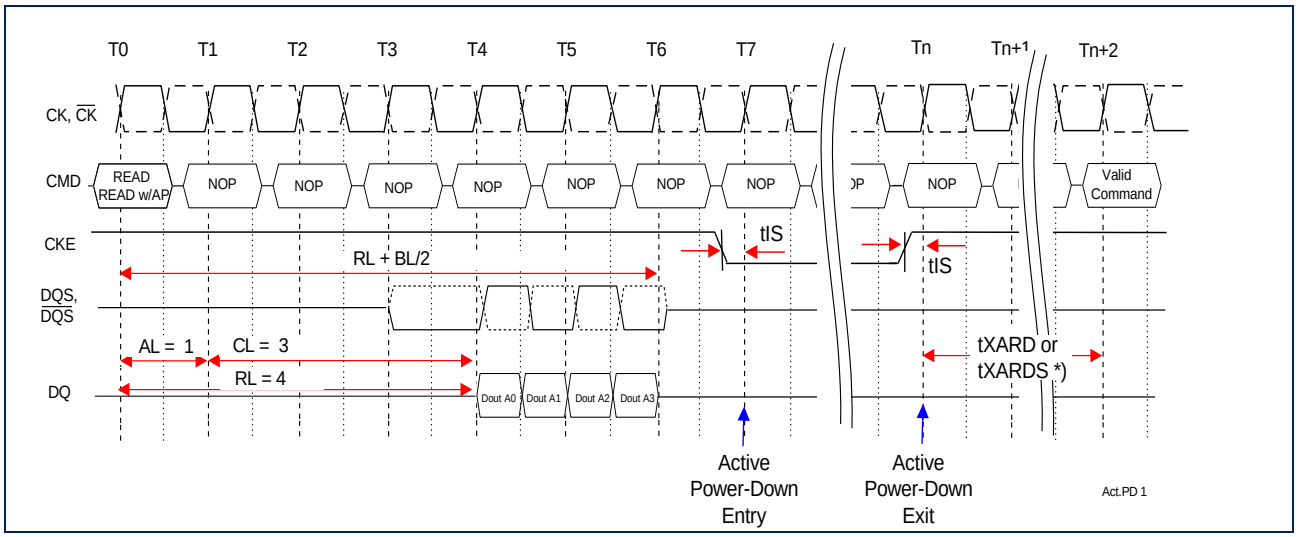
In case of a write command with Auto-Precharge, Power-down mode entry is allowed after the internal precharge command has been executed, which WL + BL/2 + WR is starting from the write with Auto-Precharge command. In case the DDR2 SDRAM enters the *Precharge Power-down* mode.

Examples:

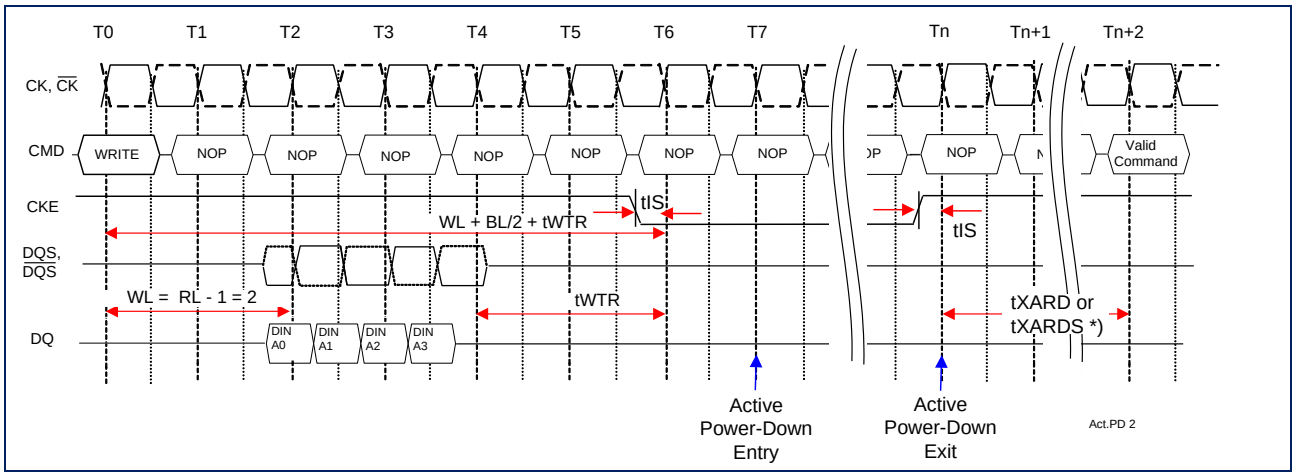
Active Power-Down Mode Entry and Exit after an Activate Command



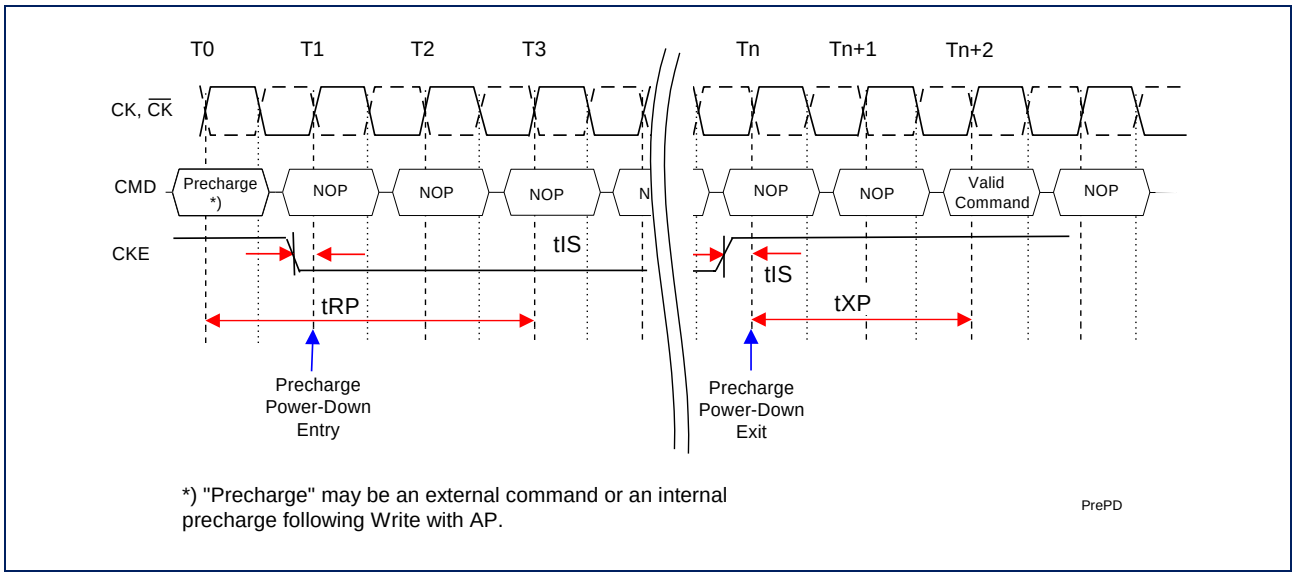
Active Power-Down Mode Entry and Exit after a Read Burst: RL = 4 (AL = 1, CL =3), BL = 4



Active Power-Down Mode Entry and Exit after a Write Burst: WL = 2, tWTR = 2, BL = 4



Precharge Power Down Mode Entry and Exit



No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't care.

Input Clock Frequency Change

During operation the DRAM input clock frequency can be changed under the following conditions:

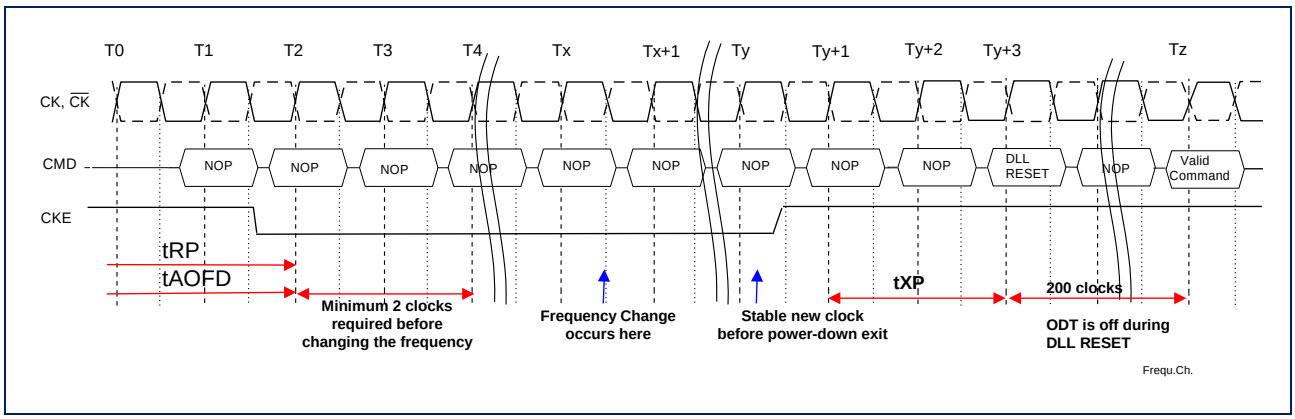
a) During Self-Refresh operation

b) DRAM is in Precharge Power-down mode and ODT is completely turned off.

The DDR2-SDRAM has to be in Precharged Power-down mode and idle. ODT must be already turned off and CKE must be at a logic "low" state. After a minimum of two clock cycles after tRP and tAOFD have been satisfied the input clock frequency can be changed. A stable new clock frequency has to be provided, before CKE can be changed to a "high" logic level again. After t_{XP} has been satisfied a DLL RESET command via EMRS(1) has to be issued. During the following DLL re-lock period of 200 clock cycles, ODT must remain off. After the DLL-re-lock period the DRAM is ready to operate with the new clock frequency.

Example:

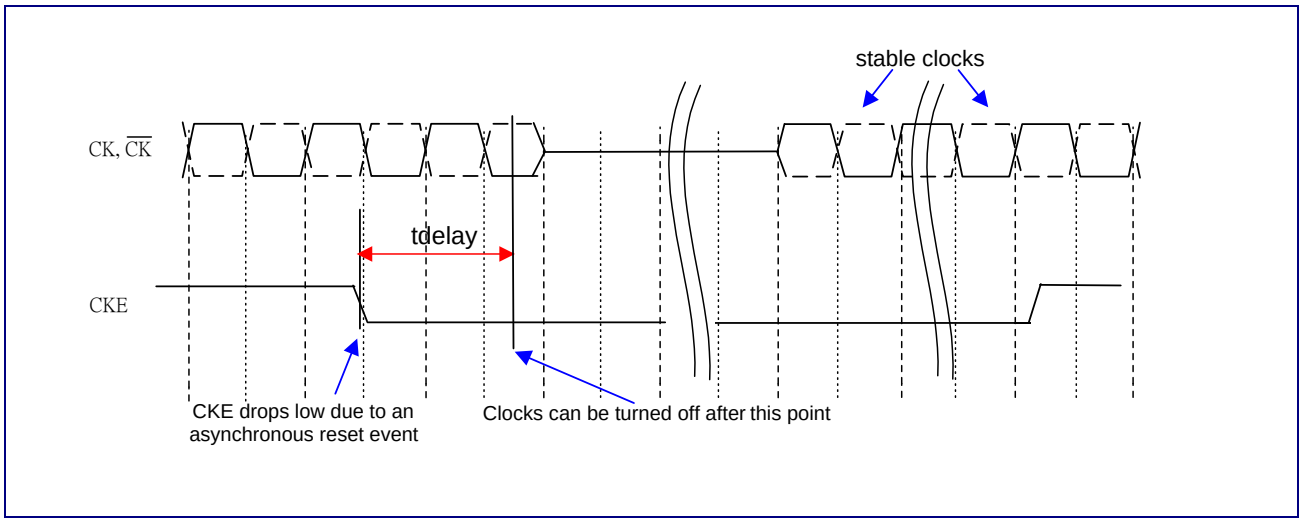
Input frequency change during Precharge Power-Down mode



Asynchronous CKE Low Event

DRAM requires CKE to be maintained “high” for all valid operations as defined in this data sheet. If CKE asynchronously drops “low” during any valid operation DRAM is not guaranteed to preserve the contents of the memory array. If this event occurs, the memory controller must satisfy a time delay (t_{delay}) before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised “high” again. The DRAM must be fully re-initialized as described the the initialization sequence. DRAM is ready for normal operation after the initialization sequence. See AC timing parametric table for t_{delay} specification.

Asynchronous CKE Low Event



Command Truth Table

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-BA1	A11-A13	A10	A0-A9	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1, 2
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	1
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	1,8
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7,8
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

Notes:

1. All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and CKE at the rising edge of the clock.
2. Bank addresses (BAx) determine which bank is to be operated upon. For (E) MRS BAx selects an (Extended) Mode Register.
3. Burst reads or writes at BL = 4 cannot be terminated.
4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. X means "H or L (but a defined logic level)".
7. Self refresh exit is asynchronous.
8. Vref must be maintained during Self Refresh operation.

Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State	CKE		Command (N) $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$	Action (N)	Notes
	Previous Cycle	Current Cycle			
Power-Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	DESELECT or NOP	Power-Down Exit	4, 8, 11, 13
Self Refresh	L	L	X	Maintain Self Refresh	11, 15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5, 9, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	4,8,10,11,13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	4,8,10,11,13
	H	L	AUTOREFRESH	Self Refresh Entry	6, 9, 11,13
Any State other than listed above	H	H	Refer to the Command Truth Table		7

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
3. Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELCT only.
10. Power-Down and Self Refresh cannot be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress. See section 2.8 "Power Down" and section 2.7.2 "Self Refresh Command" for a detailed list of restrictions.
11. Minimum CKE high time is 3 clocks, minimum CKE low time is 3 clocks.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
13. The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefore limited by the refresh requirements.
14. CKE must be maintained high while the device is in OCD calibration mode.
15. "X" means "don't care (including floating around VREF)" in Self Refresh and Power Down. However DT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in MRS(1)).
16. Vref must be maintained during Self Refresh operation

Operating Conditions

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on VDD pin relative to VSS	-1.0 to + 2.3	V	1,3
V_{DDQ}	Voltage on VDDQ pin relative to VSS	-0.5 to + 2.3	V	1,3
V_{DDL}	Voltage on VDDL pin relative to VSS	-0.5 to + 2.3	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to VSS	-0.5 to + 2.3	V	1,4
T_{STG}	Storage Temperature	-55 to + 100	℃	1,2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ. When VDD and VDDQ and VDDL are less than 500 mV, Vref may be equal to or less than 300 mV.
4. Voltage on any input or I/O may not exceed voltage on VDDQ.

DRAM Component Operating Temperature Range

Symbol	Parameter	Grade	Rating	Units	Notes
T_{OPER}	Operating Temperature	Standard	0 to 95	℃	1,2
		Industrial	- 40 to 95		1,2

Notes:

1. Operating temperature is the case surface temperature (TCASE) on the center/top side of the DRAM.
2. If TC exceeds 85℃, the DRAM must be refreshed externally at 2x refresh. It is required to set tREFI=3.9μs in auto refresh mode and to set '1' for EMRS (2) bit A7 in self refresh mode.

AC & DC Operating Conditions

DC Operating Conditions

Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min	Typ	Max		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1
V_{DDDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	5
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1,5
V_{REF}	Input Reference Voltage	0.49 * VDDQ	0.5 * VDDQ	0.51 * VDDQ	V	2, 3
V_{TT}	Termination Voltage	VREF - 0.04	VREF	VREF + 0.04	V	4

Notes:

1. There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must be less than or equal to VDD.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak ac noise on VREF may not exceed +/- 2% VREF (dc).
4. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors is expected to be set equal to VREF and must track variations in die dc level of VREF.
5. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ, and VDDL tied together.

ODT DC Electrical Characteristic

Parameter / Condition	Symbol	Min	Nom	Max	Units	Notes
Rtt eff. impedance value for EMRS(1)(A6,A2)=0,1; 75Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt eff. impedance value for EMRS(1)(A6,A2)=1,0; 150Ω	Rtt2(eff)	120	150	180	Ω	1
Rtt eff. impedance value for EMRS(1)(A6,A2)=1,1; 50Ω	Rtt3(eff)	40	50	60	Ω	1
Deviation of VM with respect to VDDQ / 2	delta VM	- 6		+ 6	%	2

Notes:

1. Measurement Definition for Rtt(eff):

$$Rtt(eff) = \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

2. Measurement Definition for VM:

$$\Delta VM = \left(\frac{2 \times Vm}{VDDQ} - 1 \right) \times 100\%$$

DC & AC Logic Input Levels

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the cross point of DQS and its complement, DQS. This distinction in timing methods is guaranteed by design and characterization. In single ended mode, the DQS (and RDQS) signals are internally disabled and don't care.

Input DC logic level

Symbol	Parameter	Min	Max	Units
V_{IH}(dc)	DC input logic high	VREF + 0.125	VDDQ + 0.3	V
V_{IL}(dc)	DC input logic low	-0.3	VREF - 0.125	V

Input AC logic level

Symbol	Parameter	DDR2-1066		DDR2-667, DDR2-800		Units
		Min	Max	Min	Max	
V_{IH}(ac)	AC input logic high	VREF + 0.200	-	VREF + 0.200	VDDQ+Vpeak	V
V_{IL}(ac)	AC input logic low	-	VREF - 0.200	VSSQ-Vpeak	VREF - 0.200	V
NOTE 1 Refer to Overshoot/undershoot specifications for Vpeak value: maximum peak amplitude allowed for overshoot and undershoot.						

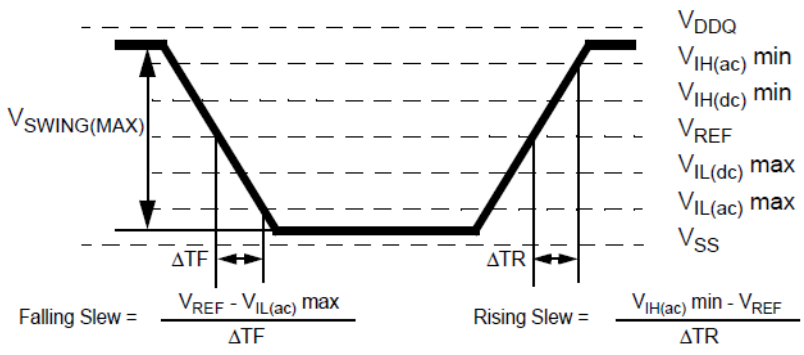
AC input test conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 x V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2,3

NOTE 1 Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL(AC)}$ level applied to the device under test.

NOTE 2 The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)}$ min for rising edges and the range from V_{REF} to $V_{IL(ac)}$ max for falling edges as shown in the below figure.

NOTE 3 AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



Differential input AC logic level

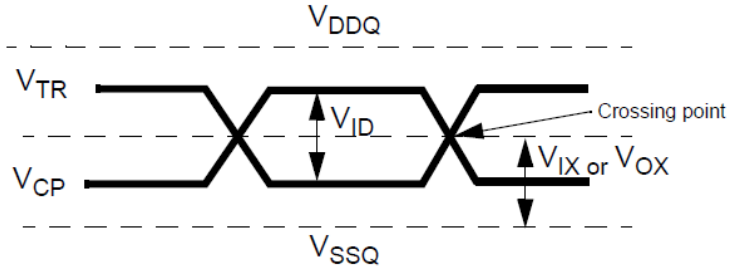
Symbol	Parameter		Min	Max	Units	Notes
V_{ID} (ac)	ac differential input voltage	DDR2-667/800	0.5	VDDQ	V	1,3
		DDR2-1066	0.5	VDDQ + 0.6 [1]		
V_{IX} (ac)	ac differential crosspoint voltage		0.5 x VDDQ - 0.175	0.5 x VDDQ + 0.175	V	2

NOTE 1 Follow JEDEC 1066 specification (JESD208)

NOTE 2 V_{ID}(AC) specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to VIH(AC) - VIL(AC).

NOTE 3 The typical value of V_{IX}(AC) is expected to be about 0.5 x VDDQ of the transmitting device and V_{IX}(AC) is expected to track variations in VDDQ. V_{IX}(AC) indicates the voltage at which differential input signals must cross.

NOTE 4 Refer to Overshoot/undershoot specifications for Vpeak value: maximum peak amplitude allowed for overshoot and undershoot.



Differential AC output parameters

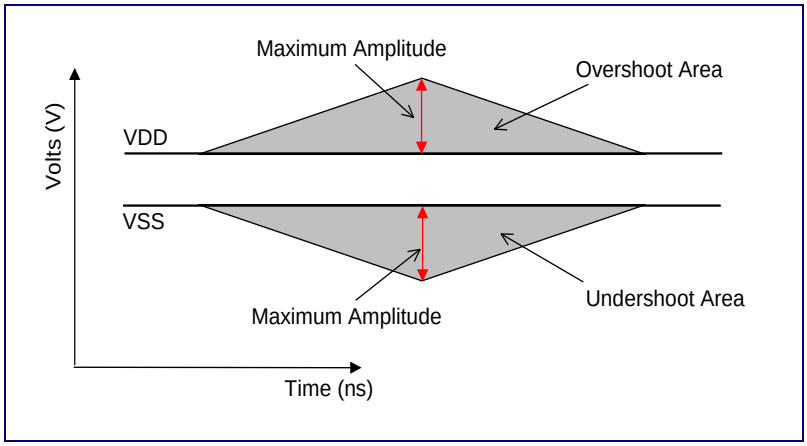
Symbol	Parameter	Min	Max	Units	Notes
V_{OX} (ac)	ac differential crosspoint voltage	0.5 x VDDQ - 0.125	0.5 x VDDQ + 0.125	V	1

NOTE 1 The typical value of VOX(AC) is expected to be about 0.5 x VDDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ . VOX(AC) indicates the voltage at which differential output signals must cross.

Overshoot and Undershoot Specification

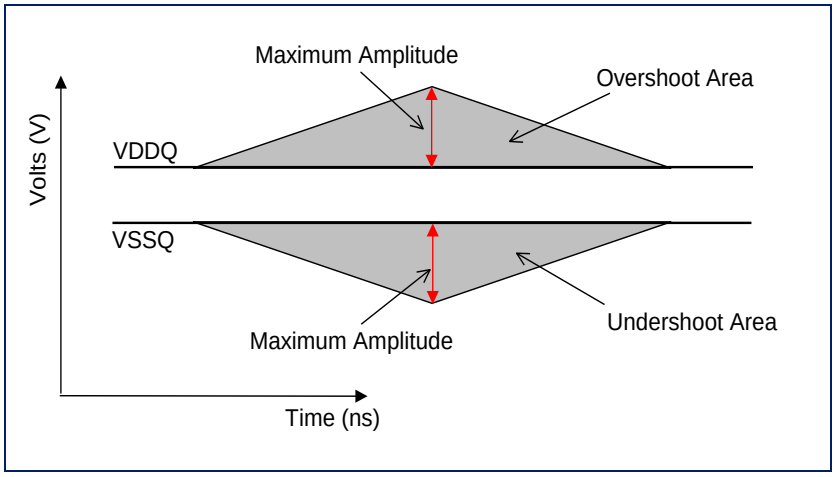
AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	DDR2-1066	DDR2-800	DDR2-667	Units
Maximum peak amplitude allowed for overshoot area	0.5(0.9) [1]	0.5(0.9) [1]	0.5(0.9) [1]	V
Maximum peak amplitude allowed for undershoot area	0.5(0.9) [1]	0.5(0.9) [1]	0.5(0.9) [1]	V
Maximum overshoot area above VDD	0.5	0.66	0.8	V/ns
Maximum undershoot area below VSS	0.5	0.66	0.8	V/ns
NOTE 1 The maximum requirements for peak amplitude were reduced from 0.9V to 0.5V.				



AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	DDR2-1066	DDR2-800	DDR2-667	Units
Maximum peak amplitude allowed for overshoot area	0.5	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	0.5	V
Maximum overshoot area above VDD	0.19	0.23	0.23	V/ns
Maximum undershoot area below VSS	0.19	0.23	0.23	V/ns



Power & Ground Clamp V-I Characteristics

Power and Ground clamps are provided on address, $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, $\overline{WE}$, CKE, and ODT pins.

V-I characteristics for input-only pins with clamps

Voltage across clamp (V)	Minimum Power Clamp Current	Minimum Ground Clamp Current	Units
0.0	0.0	0.0	mA
0.1	0.0	0.0	mA
0.2	0.0	0.0	mA
0.3	0.0	0.0	mA
0.4	0.0	0.0	mA
0.5	0.0	0.0	mA
0.6	0.0	0.0	mA
0.7	0.0	0.0	mA
0.8	0.1	0.1	mA
0.9	1.0	1.0	mA
1.0	2.5	2.5	mA
1.1	4.7	4.7	mA
1.2	6.8	6.8	mA
1.3	9.1	9.1	mA
1.4	11.0	11.0	mA
1.5	13.5	13.5	mA
1.6	16.0	16.0	mA
1.7	18.2	18.2	mA
1.8	21.0	21.0	mA

Output Buffer Levels

Output AC test conditions

Symbol	Parameter	SSTL_18	Units	Notes
V_{OTR}	Output Timing Measurement Reference Level	0.5 x V_{DDQ}	V	1

NOTE 1 The VDDQ of the device under test is referenced.

OCD default characteristics

Description	Parameter	Min	Nom	Max	Units	Notes
Output slew rate	Sout	1.5	-	5	V/ns	1-6

NOTE 1 Absolute Specifications (TOPER; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V). DRAM I/O specifications for timing, voltage, and slew rate are no longer applicable if OCD is changed from default settings.

NOTE 2 Slew rate measured from vil(ac) to vih(ac).

NOTE 3 The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

NOTE 4 DRAM output slew rate specification applies to 400 MT/s, 533 MT/s & 667 MT/s speed bins.

NOTE 5 Timing skew due to DRAM output slew rate mis-match between DQS / DQS and associated DQ's is included in tDQSQ and tQHS specification.

NOTE 5 DDR2 SDRAM output slew rate test load is defined in the AC Timing specification Table.

IDD Measurement Conditions

IDD values are for full operating range of Voltage and Temperature

Symbol	Parameter/Condition
IDD0	**Operating one bank active-precharge current**; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W
IDD2P	**Precharge power-down current**; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
IDD2N	**Precharge standby current**; All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD2Q	**Precharge quiet standby current**; All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING

IDD3P(0)	**Active power-down current**; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING MRS A12 bit is set to "0"(Fast Power-down Exit);
IDD3P(1)	**Active power-down current**; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING MRS A12 bit is set to "1"(Slow Power-down Exit);
IDD3N	**Active standby current**; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD5B	**Burst refresh current**; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;

	Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0 V; CKE ≤ 0.2 V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = 1 x tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following pages for detailed timing conditions

Notes:

1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS, RDQS, RDQS, LDQS, LDQS, UDQS, and UDQS. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. For DDR2-667/800/1066 testing, tCK in the Conditions should be interpreted as tCK(avg)
6. Definitions for IDD
   - LOW = Vin ≤ VILAC(max)
   - HIGH = Vin ≥ VIHAC(min)
   - STABLE = inputs stable at a HIGH or LOW level
   - FLOATING = inputs at VREF = VDDQ/2
   - SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between

IDD testing parameters

Speed	DDR2-1066	DDR2-1066	DDR2-800	DDR2-667	Units
CL-tRCD-tRP	6-6-6	7-7-7	5-5-5	5-5-5	
CL(IDD)	6	7	5	5	tCK
tRCD(IDD)	11.25	13.125	12.5	15	ns
tRC(IDD)	56.25	58.125	57.5	60	ns
tRRD(IDD) – X8	7.5	7.5	7.5	7.5	ns
tRRD(IDD) – X16	10	10	10	10	ns
tFAW(IDD) – X8	35	35	35	37.5	ns
tFAW(IDD) – X16	45	45	45	50	ns
tCK(IDD)	1.875	1.875	2.5	3	ns
tRASmin(IDD)	45	45	45	45	ns
tRASmax(IDD)	70K	70K	70K	70K	ns
tRP(IDD)	11.25	13.125	12.5	15	ns
tRFC(IDD)	105	105	105	105	ns

Detailed IDD7

Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation

All banks are being interleaved at minimum tRC(IDD) without violating tRRD(IDD) and tFAW(IDD) using a burst length of 4.

Control and address bus inputs are STABLE during DESELECTs. IOUT = 0 mA

Timing Patterns for 4 bank devices with 1 KB or 2 KB page size

-DDR2-667 5-5-5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D

-DDR2-667 4-4-4: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D

-DDR2-800 6-6-6: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D D

-DDR2-800 5-5-5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D

-DDR2-800 4-4-4: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D

-DDR2-1066 7-7-7: A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D

-DDR2-1066 6-6-6: A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D

IDD Specifications

Symbol	X8				X16				Unit
	DDR2-800		DDR2-1066		DDR2-800		DDR2-1066		
	Typical	Max	Typical	Max	Typical	Max	Typical	Max	
IDD0	61	75	76	85	74	85	93	100	mA
IDD1	64	85	80	90	76	95	95	110	mA
IDD2P	5	8	5	8	5	8	5	8	mA
IDD2Q	30	40	36	45	30	40	36	45	mA
IDD2N	37	45	45	50	37	45	45	50	mA
IDD3P0	26	40	30	45	35	50	40	55	mA
IDD3P1	12	25	12	25	21	40	21	40	mA
IDD3N	53	70	63	80	61	80	71	90	mA
IDD4W	122	150	152	180	150	170	187	220	mA
IDD4R	120	140	150	175	143	165	177	195	mA
IDD5B (tRC = tRFC)	96	110	124	130	95	120	123	130	mA
IDD5D (tRC = tREFI)	38	45	46	50	38	45	46	50	mA
IDD6	5	7	5	7	4.5	7	5	7	mA
IDD7	120	150	150	170	170	185	218	240	mA

Input/output capacitance

Parameter	Symbol	DDR2-1066		DDR2-800		DDR2-667		Units
		Min	Max	Min	Max	Min	Max	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	1.0	2.0	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	x	0.25	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	1.75	1.0	1.75	1.0	2.0	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	x	0.25	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	3.5	2.5	3.5	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	x	0.5	x	0.5	pF

Refresh parameters

Parameter	Symbol			512Mb	Unit	Notes
Refresh to **active/Refresh** command time	**tRFC**			**105**	ns	1
Average periodic Refresh interval	**tREFI**	Commercial	0℃ ≦ Tcase ≦ 85℃	**7.8**	μs	1
			85℃ ≦ Tcase ≦ 95℃	**3.9**		1,2,3
		Industrial	- 40℃ ≦ Tcase ≦ 85℃	**7.8**		1
			85℃ ≦ Tcase ≦ 95℃	**3.9**		1,2,3
		Automotive 2	- 40℃ ≦ Tcase ≦ 85℃	**7.8**		1
			85℃ ≦ Tcase ≦ 105℃	**3.9**		1,2,3
		Automotive 3	- 40℃ ≦ Tcase ≦ 85℃	**7.8**		1
			85℃ ≦ Tcase ≦ 95℃	**3.9**		1,2,3

NOTE 1 If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

NOTE 2 This is an additional feature. For detailed information, please refer to “operating temperature condition” chapter in this spec

NOTE 3 When TC exceeds 85℃, the DRAM must be refreshed externally at 2x refresh. It is required to set tREFI=3.9μs in auto refresh mode and to set ‘1’ for EMRS (2) bit A7 in self refresh mode.

AC & DC operating conditions

Timing parameters (DDR2-1066 and DDR2-800)

Parameter	Symbol	DDR2-1066		DDR2-800		Units[34]	Notes
		Min	Max	Min	Max		
Clock cycle time	tCK	1875	7500	2500	8000	ps	35,36
CK HIGH pulse width	tCH	0.48	0.52	0.48	0.52	tCK(avg)	35,36
CK LOW pulse width	tCL	0.48	0.52	0.48	0.52	tCK(avg)	35,36
Write command to DQS associated clock edge	WL	RL - 1		RL - 1			
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	- 0.25	0.25	tCK(avg)	30
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK(avg)	30
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK(avg)	30
DQS input HIGH pulse width	tDQSH	0.35	-	0.35	-	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	-	0.35	-	tCK(avg)	
Write preamble	tWPRE	0.35	-	0.35	-	tCK(avg)	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10
Address and control input setup time	tIS(base)	125	-	175	-	ps	5,7,9,22 ,29
Address and control input hold time	tIH(base)	200	-	250	-	ps	5,7,9,23 ,29
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK(avg)	
DQ and DM input setup time (differential strobe)	tDS(base)	0	-	50	-	ps	6,7,8,20 ,28,31
DQ and DM input hold time (differential strobe)	tDH(base)	75	-	125	-	ps	6,7,8,21 ,28,31
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK(avg)	
DQ output access time from CK,$\overline{CK}$	tAC	- 350	350	- 400	400	ps	40
DQS output access time from CK,$\overline{CK}$	tDQSCK	-325	325	- 350	350	ps	40
Data-out high-impedance time from CK,$\overline{CK}$	tHZ	-	tAC,max	-	tAC,max	ps	18,40
DQS(/DQS) low-impedance time from CK,$\overline{CK}$	tLZ(DQS)	tAC,min	tAC,max	tAC,min	tAC,max	ps	18,40
DQ low-impedance time from CK,$\overline{CK}$	tLZ(DQ)	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	175	-	200	ps	13
CK half pulse width	tHP	Min(tCH(abs),tCL(abs))	-	Min(tCH(abs),tCL(abs))	-	ps	37
DQ hold skew factor	tQHS	-	250	-	300	ps	38
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	-	tHP-tQHS	-	ps	39
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19,41

Parameter	Symbol	DDR2-1066		DDR2-800		Units[34]	Notes
		Min	Max	Min	Max		
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19,42
Active to active command period for 1KB page size	tRRD	7.5	-	7.5		ns	4,32
Active to active command period for 2KB page size	tRRD	10	-	10	-	ns	4,32
Four Activate Window for 1KB page size	tFAW	35	-	35	-	ns	32
Four Activate Window for 2KB page size	tFAW	45	-	45	-	ns	32
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2	-	2	-	nCK	
Write recovery time	tWR	15	-	15	-	ns	32
Auto precharge write recovery + precharge time	tDAL	WR+tnRP	-	WR+tnRP	-	nCK	33
Internal write to read command delay	tWTR	7.5	-	7.5	-	ns	24,32
Internal read to precharge command delay	tRTP	7.5	-	7.5	-	ns	3,32
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3	-	3	-	nCK	27
Exit self refresh to a non-read command	tXSNR	tRFC + 10	-	tRFC + 10	-	ns	32
Exit self refresh to a read command	tXSRD	200	-	200	-	nCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	nCK	
Exit active power down to read command	tXARD	2	-	2	-	nCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	10 - AL	-	8 - AL	-	nCK	1,2
ODT turn-on delay	tAOND	2	2	2	2	nCK	16
ODT turn-on	tAON	tAC,min	tAC,max + 2.575	tAC,min	tACmax + 0.7	ns	6,16,40
ODT turn-on (Power-Down mode)	tAONPD	tAC,min + 2	3 x tCK(avg) +tAC,max + 1	tAC,min + 2	2 x tCK(avg) +tAC,max + 1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	nCK	17,45
ODT turn-off	tAOF	tAC,min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	ns	17,43,45
ODT turn-off (Power-Down mode)	tAOFPD	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	ns	
ODT to power down entry latency	tANPD	4	-	3	-	nCK	
ODT power down exit latency	tAXPD	11	-	8	-	nCK	
Mode register set command cycle time	tMRD	2	-	2	-	nCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	32
OCD drive mode output delay	tOIT	0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS +tCK(avg) +tIH	-	tIS +tCK(avg) +tIH	-	ns	15

AC & DC operating conditions

Timing parameters (DDR2-667)

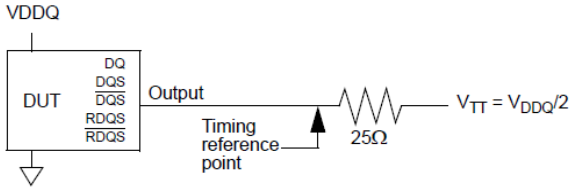
Parameter	Symbol	DDR2-667		Units[34]	Notes
		Min	Max		
Clock cycle time	tCK	3000	8000	ps	35,36
CK HIGH pulse width	tCH	0.48	0.52	tCK(avg)	35,36
CK LOW pulse width	tCL	0.48	0.52	tCK(avg)	35,36
Write command to DQS associated clock edge	WL	RL - 1		nCK	
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	tCK(avg)	30
DQS falling edge to CK setup time	tDSS	0.2	-	tCK(avg)	30
DQS falling edge hold time from CK	tDSH	0.2	-	tCK(avg)	30
DQS input HIGH pulse width	tDQSH	0.35	-	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	-	tCK(avg)	
Write preamble	tWPRE	0.35	-	tCK(avg)	
Write postamble	tWPST	0.4	0.6	tCK(avg)	10
Address and control input setup time	tIS(base)	200	-	ps	5,7,9,22,29
Address and control input hold time	tIH(base)	275	-	ps	5,7,9,23,29
Control & Address input pulse width for each input	tIPW	0.6	-	tCK(avg)	
DQ and DM input setup time (differential strobe)	tDS(base)	100	-	ps	6,7,8,20,28,31
DQ and DM input hold time (differential strobe)	tDH(base)	175	-	ps	6,7,8,21,28,31
DQ and DM input pulse width for each input	tDIPW	0.35	-	tCK(avg)	
DQ output access time from CK,$\overline{CK}$	tAC	- 450	450	ps	40
DQS output access time from CK,$\overline{CK}$	tDQSCK	- 400	400	ps	40
Data-out high-impedance time from CK,$\overline{CK}$	tHZ	-	tAC,max	ps	18,40
DQS($\overline{DQS}$) low-impedance time from CK,$\overline{CK}$	tLZ(DQS)	tAC,min	tAC,max	ps	18,40
DQ low-impedance time from CK,$\overline{CK}$	tLZ(DQ)	2 x tAC,min	tAC,max	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	240	ps	13
CK half pulse width	tHP	Min(tCH(abs),tCL(abs))	-	ps	37
DQ hold skew factor	tQHS	-	340	ps	38
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	ps	39
Read preamble	tRPRE	0.9	1.1	tCK(avg)	19,41
Read postamble	tRPST	0.4	0.6	tCK(avg)	19,42
Active to active command period for 1KB page size	tRRD	7.5	-	ns	4,32
Active to active command period for 2KB page size	tRRD	10	-	ns	4,32
Four Activate Window for 1KB page size	tFAW	37.5	-	ns	32
Four Activate Window for 2KB page size	tFAW	50	-	ns	32

Parameter	Symbol	DDR2-667		Units[34]	Notes
		Min	Max		
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2	-	nCK	
Write recovery time	tWR	15	-	ns	32
Auto precharge write recovery + precharge time	tDAL	WR + tnRP	-	nCK	33
Internal write to read command delay	tWTR	7.5	-	ns	24,32
Internal read to precharge command delay	tRTP	7.5	-	ns	3,32
CKE minimum pulse width(HIGH and LOW pulse width)	tCKE	3	-	nCK	27
Exit self refresh to a non-read command	tXSNR	tRFC + 10	-	ns	32
Exit self refresh to a read command	tXSRD	200	-	nCK	
Exit precharge power down to any non-read command	tXP	2	-	nCK	
Exit active power down to read command	tXARD	2	-	nCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	7 - AL	-	nCK	1,2
ODT turn-on delay	tAOND	2	2	nCK	16
ODT turn-on	tAON	tAC,min	tACmax + 0.7	ns	6,16,40
ODT turn-on (Power-Down mode)	tAONPD	tAC,min + 2	2 x tCK(avg) +tAC,max + 1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	nCK	17,45
ODT turn-off	tAOF	tAC,min	tAC,max + 0.6	ns	17,43,45
ODT turn-off (Power-Down mode)	tAOFPD	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	ns	
ODT to power down entry latency	tANPD	3	-	nCK	
ODT power down exit latency	tAXPD	8	-	nCK	
Mode register set command cycle time	tMRD	2	-	nCK	
MRS command to ODT update delay	tMOD	0	12	ns	32
OCD drive mode output delay	tOIT	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS +tCK(avg) +tIH	-	ns	15

General notes, which may apply for all AC parameters

General Note 1 DDR2 SDRAM AC timing reference load

The figure represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally a coaxial transmission line terminated at the tester electronics. This reference load is also used for output slew rate characterization.



AC timing reference load

The output timing reference voltage level for single ended signals is the cross point with VTT.
The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. $\overline{\text{DQS}}$) signal.

General Note 2 Slew Rate Measurement Levels

a) Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS - $\overline{\text{DQS}}$) output slew rate is measured between DQS - $\overline{\text{DQS}}$ = - 500mV and DQS - $\overline{\text{DQS}}$ = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

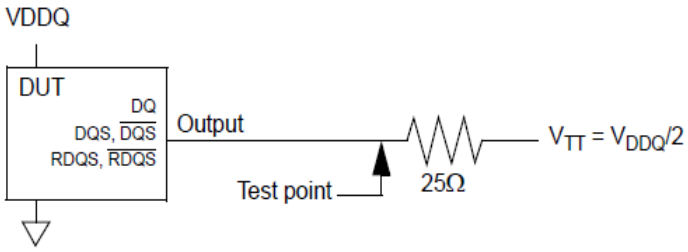
b) Input slew rate for single ended signals is measured from Vref(dc) to VIH(ac),min for rising edges and from Vref(dc) to VIL(ac),max for falling edges.

For differential signals (e.g. CK - $\overline{\text{CK}}$) slew rate for rising edges is measured from CK - $\overline{\text{CK}}$ = - 250 mV to CK - $\overline{\text{CK}}$ = + 500 mV (+ 250 mV to - 500 mV for falling edges).

c) VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{\text{CK}}$, or between DQS and $\overline{\text{DQS}}$ for differential strobe.

General Note 3 DDR2 SDRAM output slew rate test load

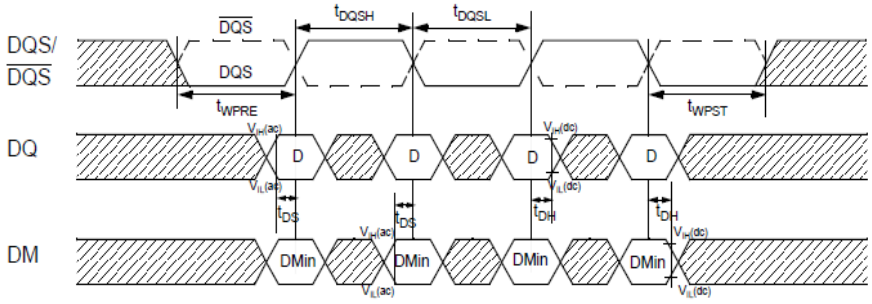
Output slew rate is characterized under the test conditions as following



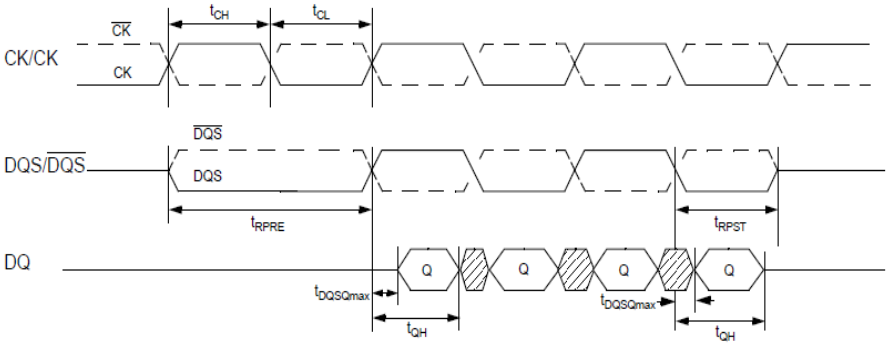
Slew rate test load

General Note 4 Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the cross point of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10 kΩ resistor to insure proper operation.



Data Input (Write) Timing



Data output (read) timing

General Note 5 AC timings are for linear signal transitions. See Specific Notes on derating for other signal transitions.

General Note 6 All voltages are referenced to VSS.

General Note 7 These parameters guarantee device behavior, but they are not necessarily tested on each device..

General Note 8 Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific notes for dedicated AC parameters

Specific Note 1 User can choose which active power down exit timing to use via MRS (bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.

Specific Note 2 AL = Additive Latency.

Specific Note 3 This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min) have been satisfied.

Specific Note 4 A minimum of two clocks (2 x tCK or 2 x nCK) is required irrespective of operating frequency.

Specific Note 5 Timings are specified with command/address input slew rate of 1.0 V/ns. See Specific Notes on derating for other slew rate values.

Specific Note 6 Timings are specified with DQs, DM, and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns. See Specific Notes on derating for other slew rate values.

Specific Note 7 Timings are specified with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1 V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

Specific Note 8 Data setup and hold time derating.

tDS/tDH derating with differential data strobe (DDR2-1066, DDR2-800, DDR2-667)

Δ tDS, Δ tDH Derating Values																			
(Units: ps)		DQS, $\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew rate (V/ns)	2	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the Δ tDS and Δ tDH derating value respectively. Example: tDS (total setup time) = tDS(base) + Δ tDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vih(ac)min.

Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max.

If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value.

If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$.

Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$.

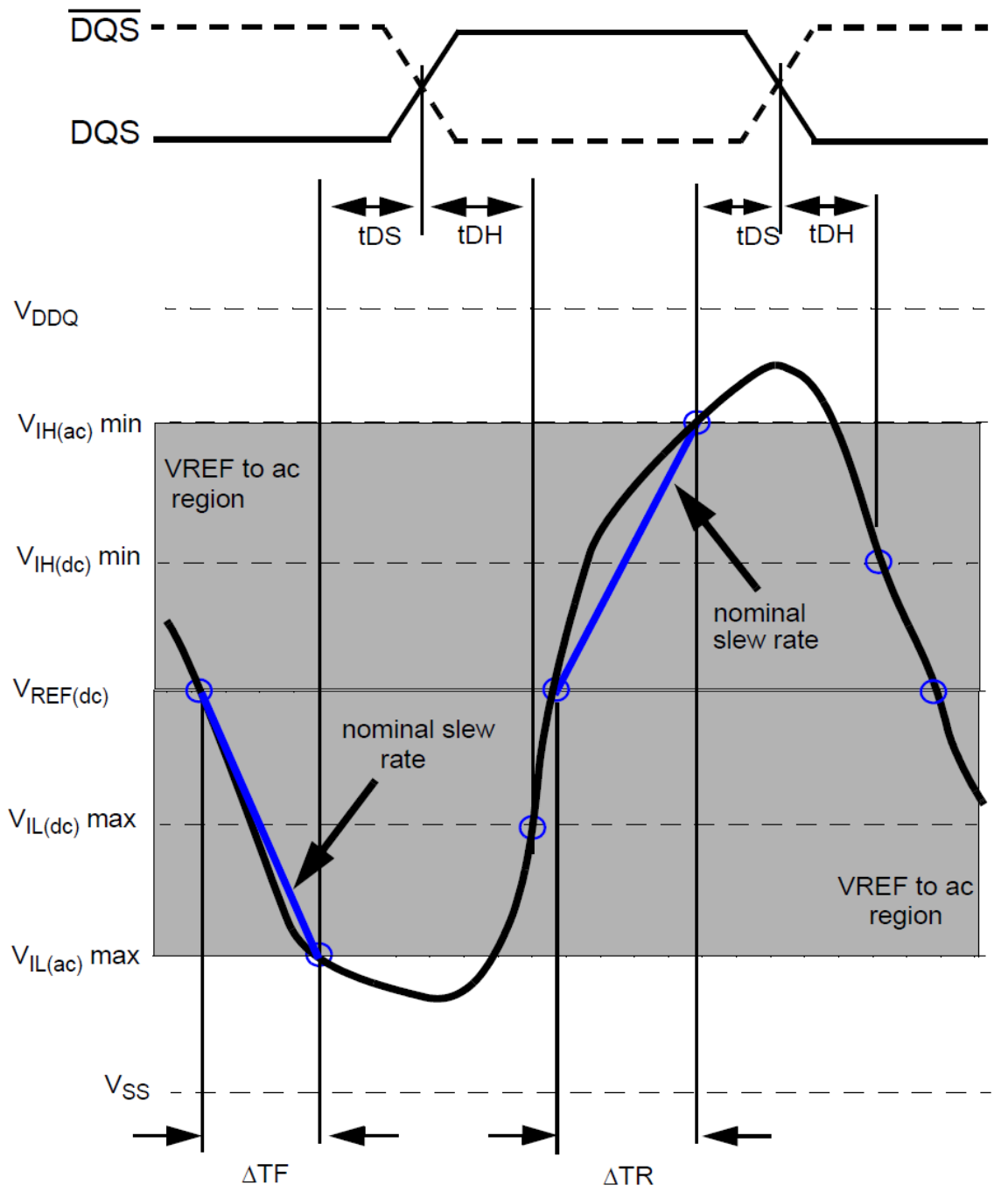
If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 79 for differential data strobe.) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).

The derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Illustration of nominal slew rate for tDS (differential DQS, $\overline{DQS}$)

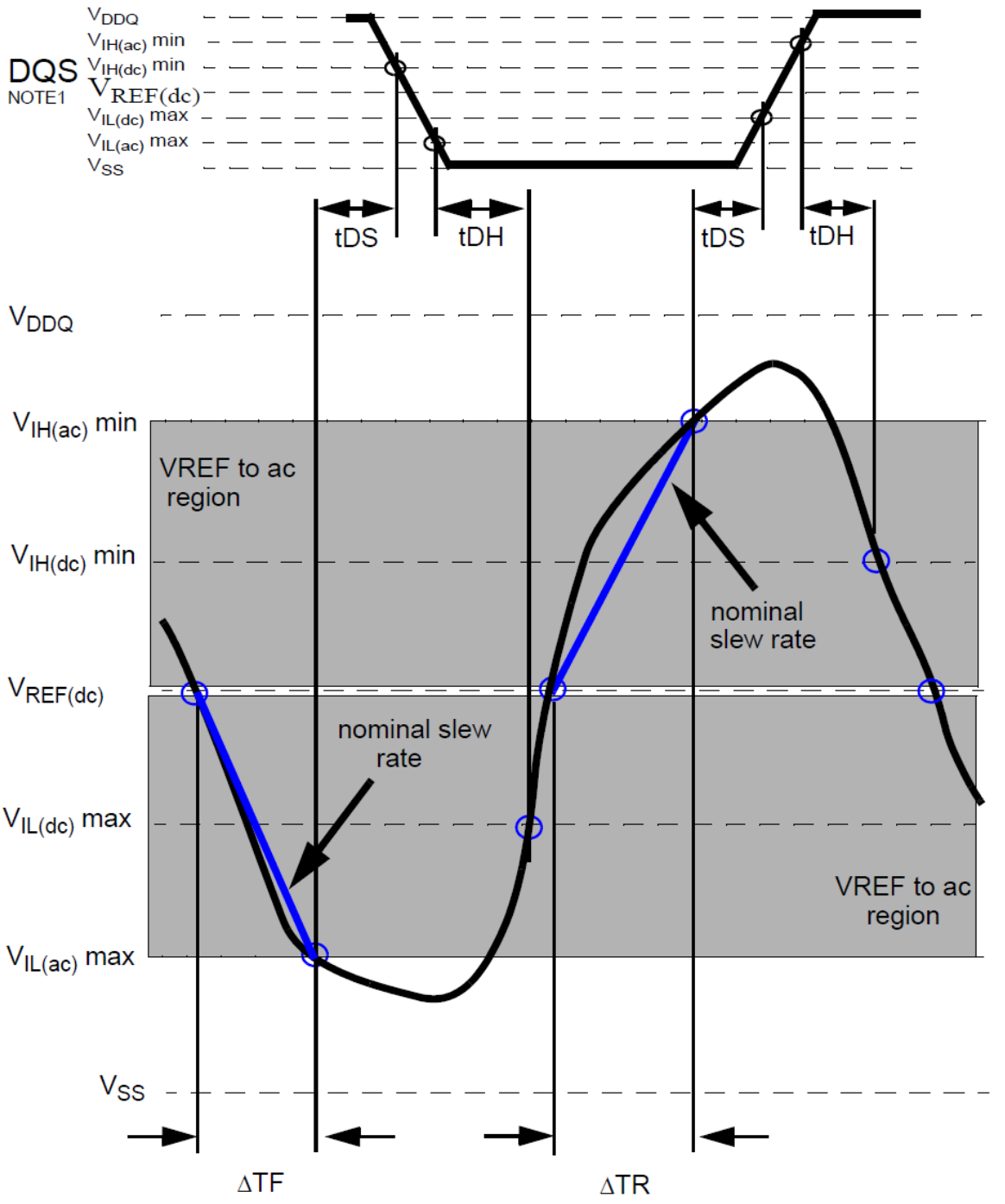


$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - Vil(ac)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{Vih(ac)min - V_{REF(dc)}}{\Delta TR}$$

Illustration of nominal slew rate for tDS (single-ended DQS)

NOTE 1 DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - Vil(ac)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{Vih(ac)min - V_{REF(dc)}}{\Delta TR}$$

Illustration of tangent line for tDS (differential DQS, $\overline{DQS}$)

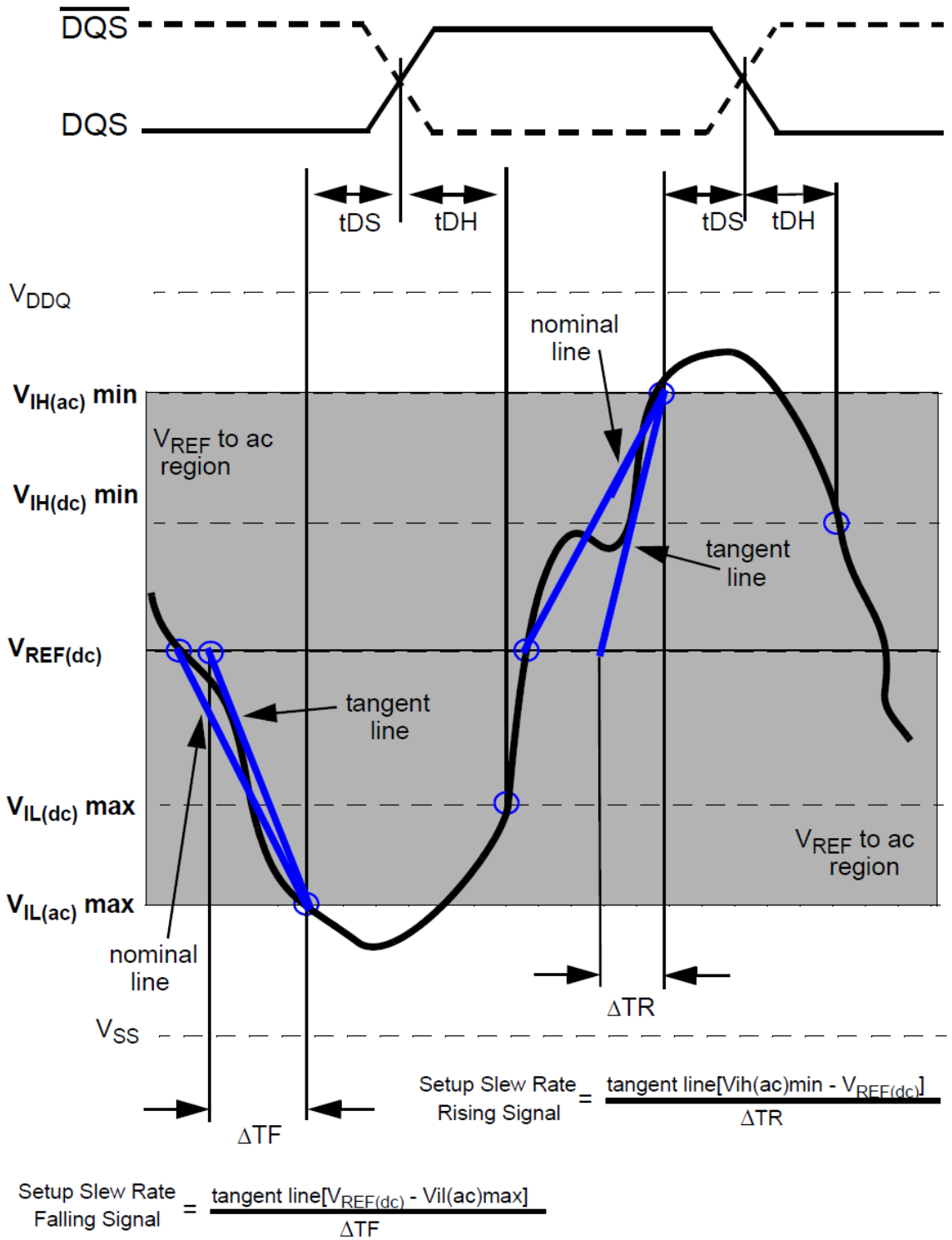


Illustration of tangent line for tDS (single-ended DQS)

NOTE DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

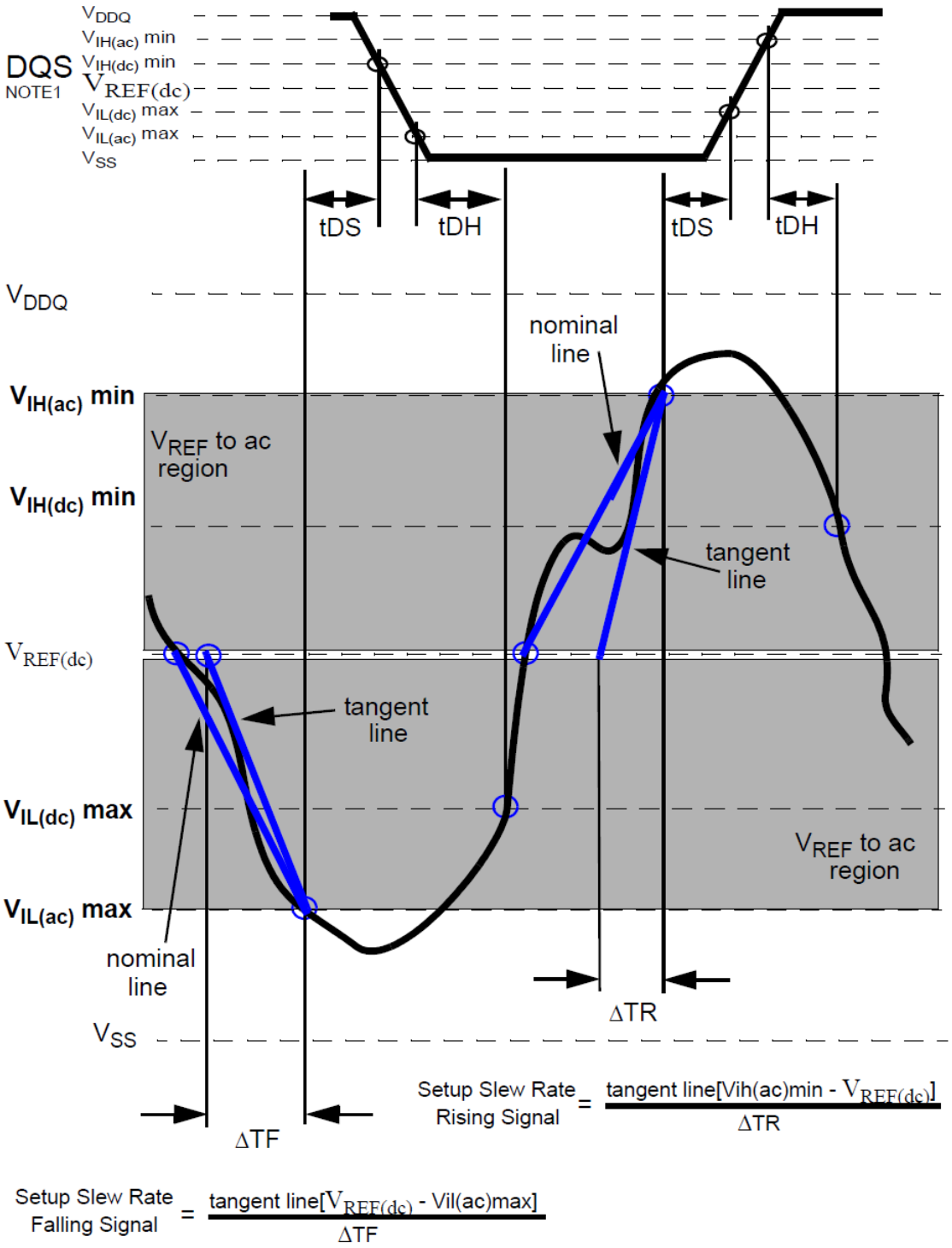
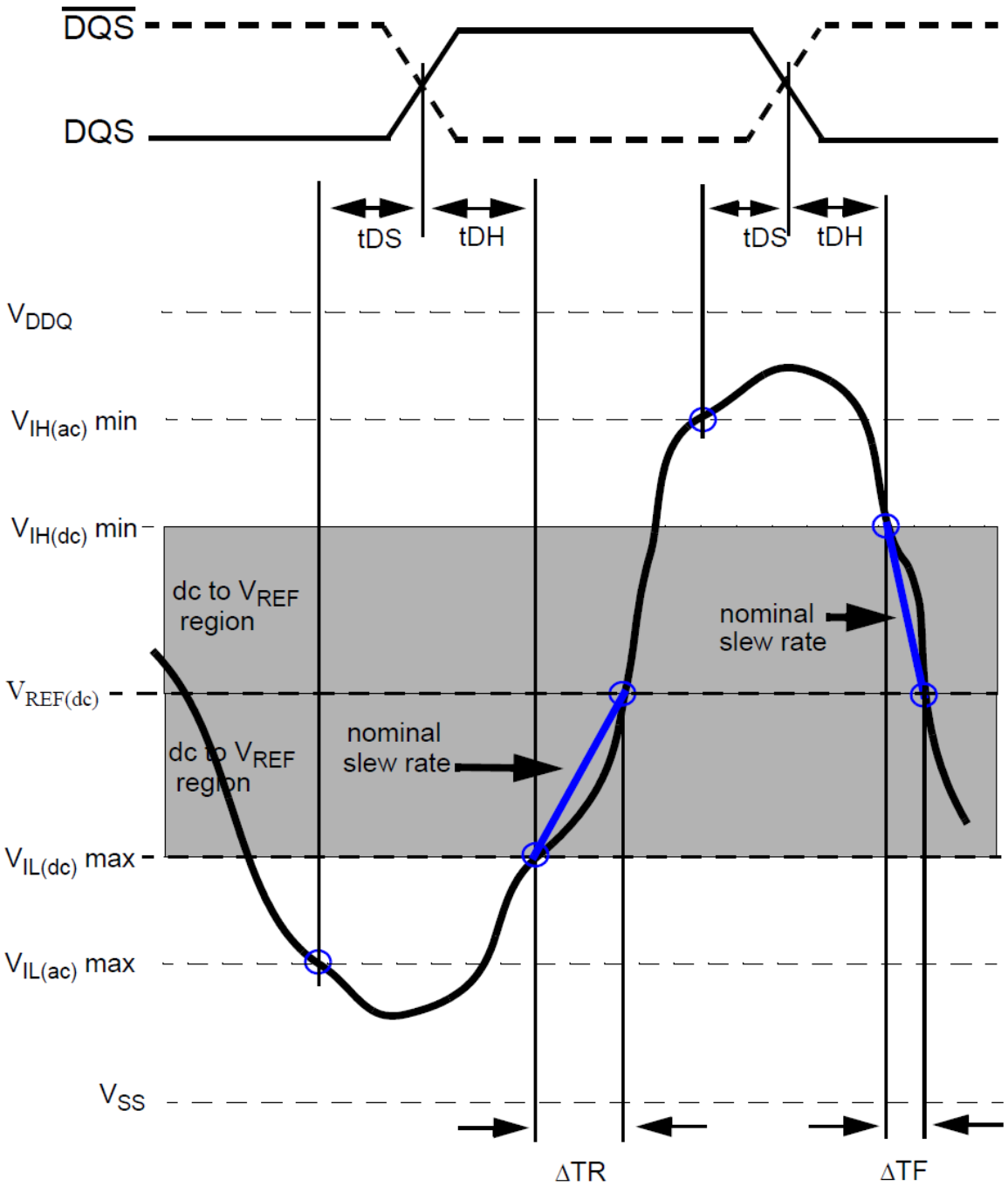


Illustration of nominal slew rate for tDH (differential DQS, $\overline{DQS}$)

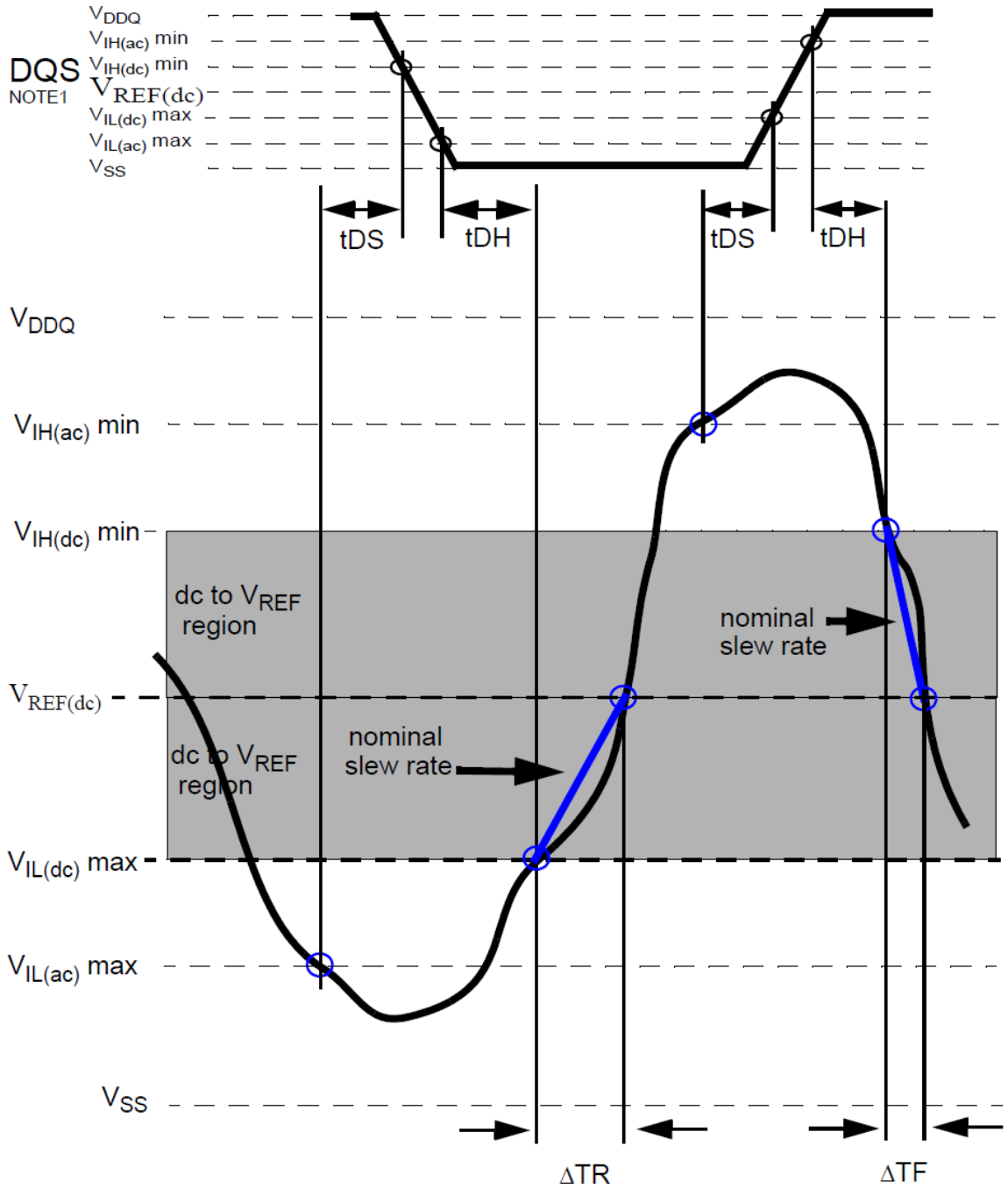


$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - Vil(dc)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{Vih(dc)min - V_{REF(dc)}}{\Delta TF}$$

Illustration of nominal slew rate for tDH (single-ended DQS)

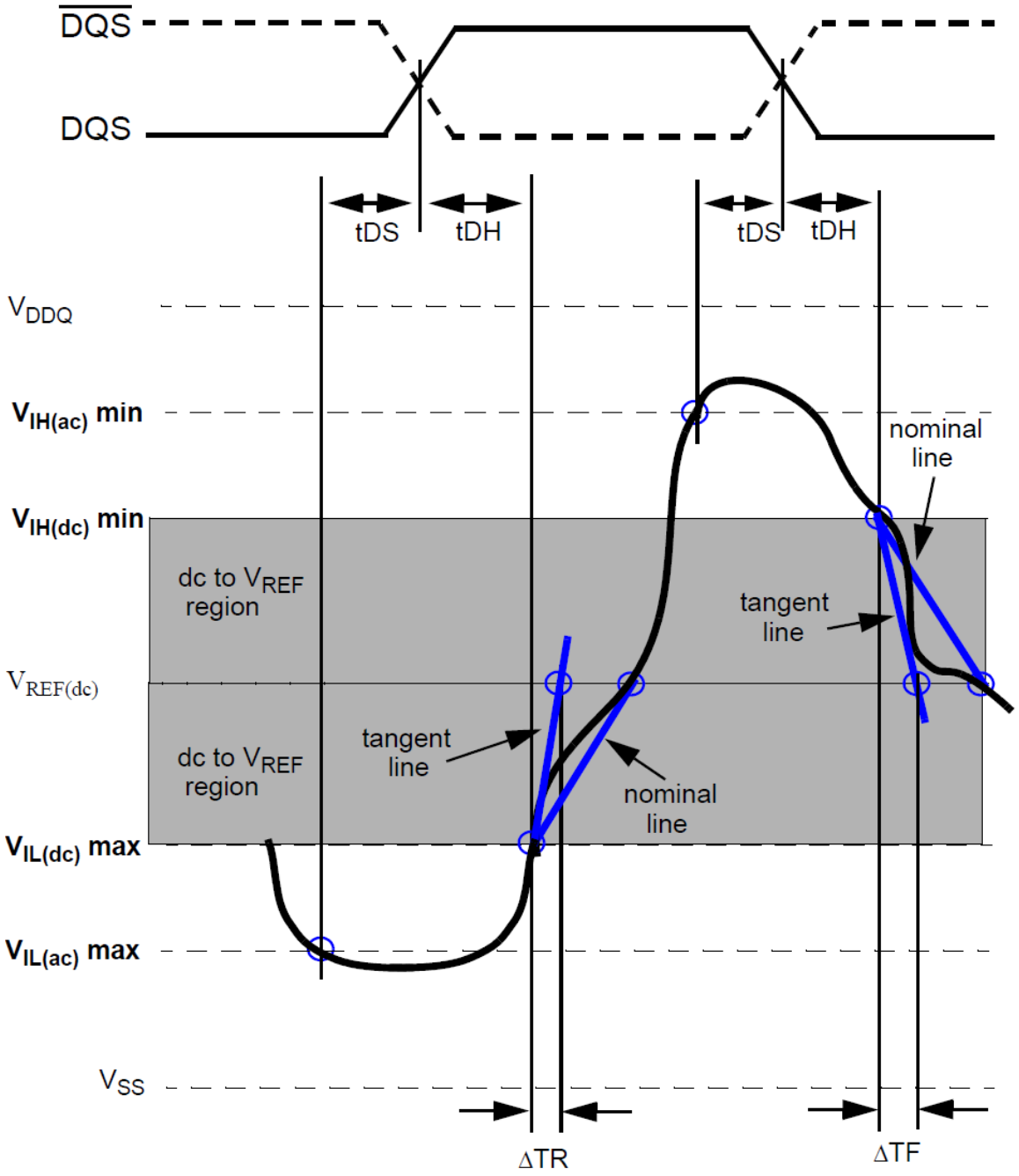
NOTE DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - Vil(dc)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{Vih(dc)min - V_{REF(dc)}}{\Delta TF}$$

Illustration tangent line for tDH (differential DQS, $\overline{DQS}$)

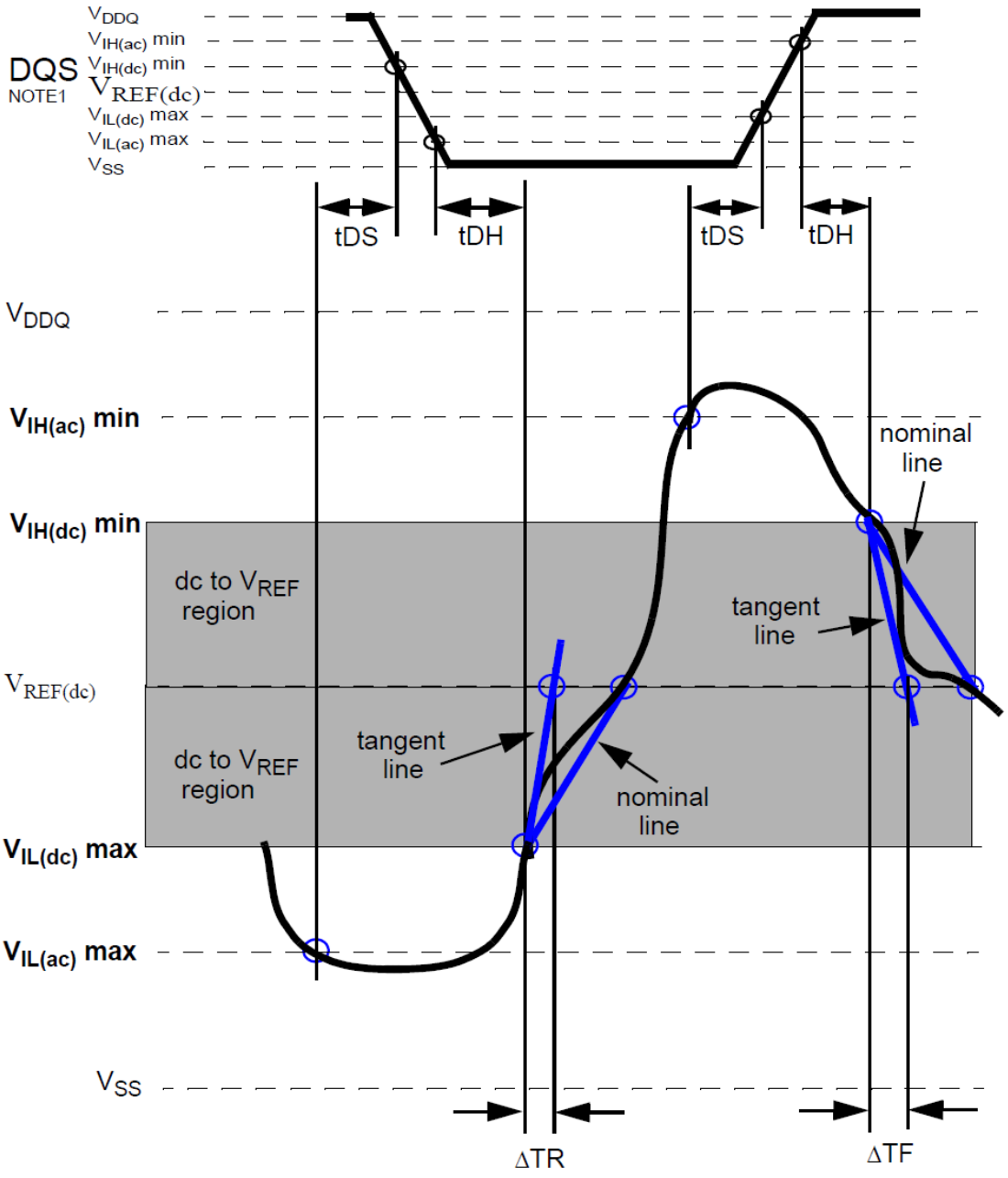


$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{REF(dc)} \text{ - Vil(dc)max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [Vih(dc)min - } V_{REF(dc)} \text{]}}{\Delta TF}$$

Illustration tangent line for tDH (single-ended DQS)

NOTE DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{REF(dc)} \text{ - Vil(dc)max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [Vih(dc)min - } V_{REF(dc)} \text{]}}{\Delta TF}$$

Specific Note 9 tIS and tIH (input setup and hold) derating

tIS/tIH derating with differential data strobe (DDR2-1066, DDR2-800, DDR2-667)

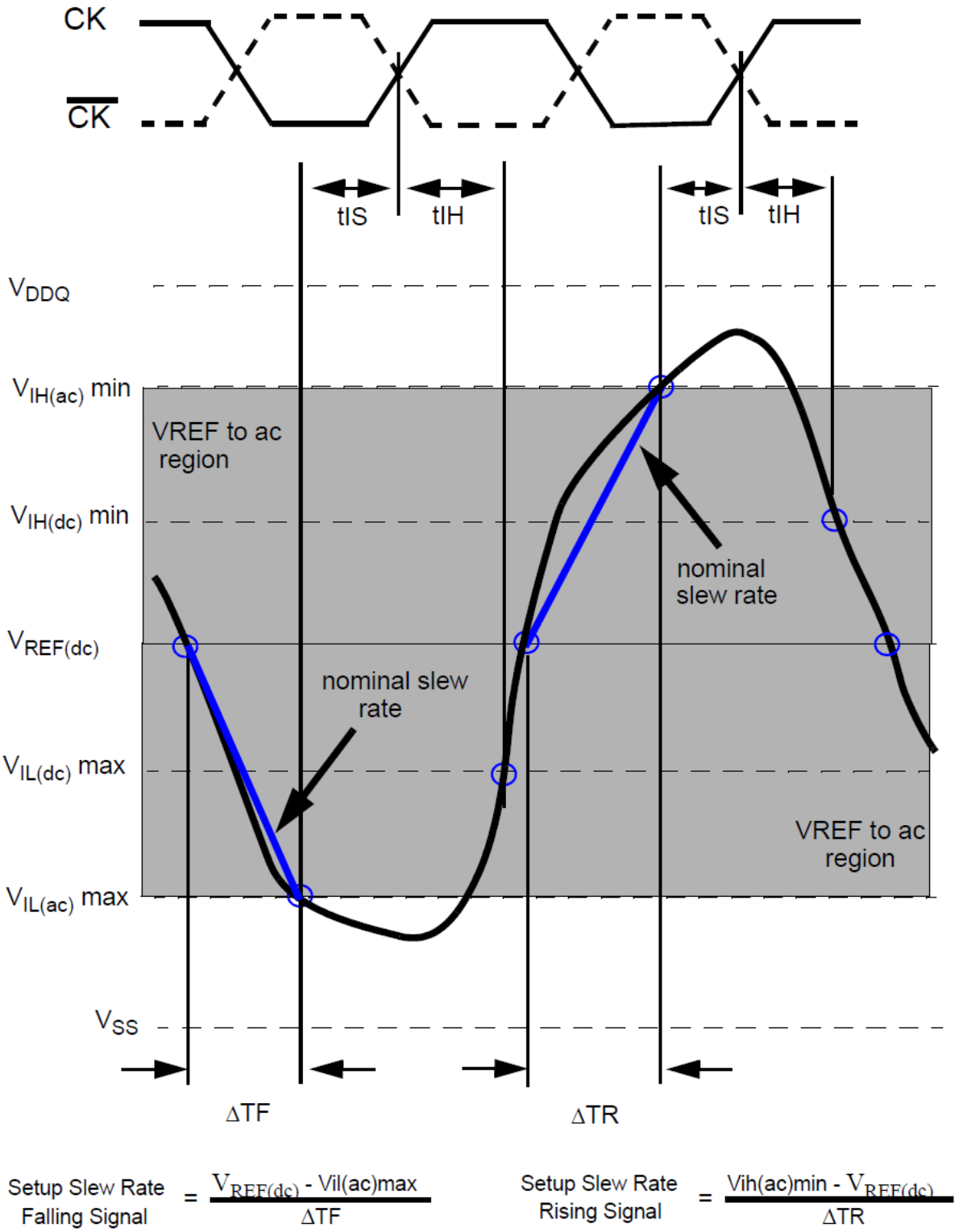
Δ tIS, Δ tIH Derating Values								
		CK, $\overline{CK}$ Differential Slew Rate						Units
		2.0 V/ns		1.5 V/ns		1.0 V/ns		
		Δ tIS	Δ tIH	Δ tIS	Δ tIH	Δ tIS	Δ tIH	
Command Address Slew rate (V/ns)	4.00	150	94	180	124	210	154	ps
	3.50	143	89	173	119	203	149	ps
	3.00	133	83	163	113	193	143	ps
	2.50	120	75	150	105	180	135	ps
	2.00	100	45	130	75	160	105	ps
	1.50	67	21	97	51	127	81	ps
	1.00	0	0	30	30	60	60	ps
	0.90	-5	-14	25	16	55	46	ps
	0.80	-13	-31	17	-1	47	29	ps
	0.70	-22	-54	8	-24	38	6	ps
	0.60	-34	-83	-4	-53	26	-23	ps
	0.50	-60	-125	-30	-95	0	-65	ps
	0.40	-100	-188	-70	-158	-40	-128	ps
	0.30	-168	-292	-138	-262	-108	-232	ps
	0.25	-200	-375	-170	-345	-140	-315	ps
	0.20	-325	-500	-295	-470	-265	-440	ps
	0.15	-517	-708	-487	-678	-457	-648	ps
	0.10	-1000	-1125	-970	-1095	-940	-1065	ps

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the Δ tIS and Δ tIH derating value respectively. Example: tIS (total setup time) = tIS(base) + Δ tIS Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vih(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value (see Figure 81). If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc) or the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac). For slew rates in between the values listed, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Illustration of nominal slew rate for tIS



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - Vil(ac)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{Vih(ac)min - V_{REF(dc)}}{\Delta TR}$$

Illustration of tangent line for tIS

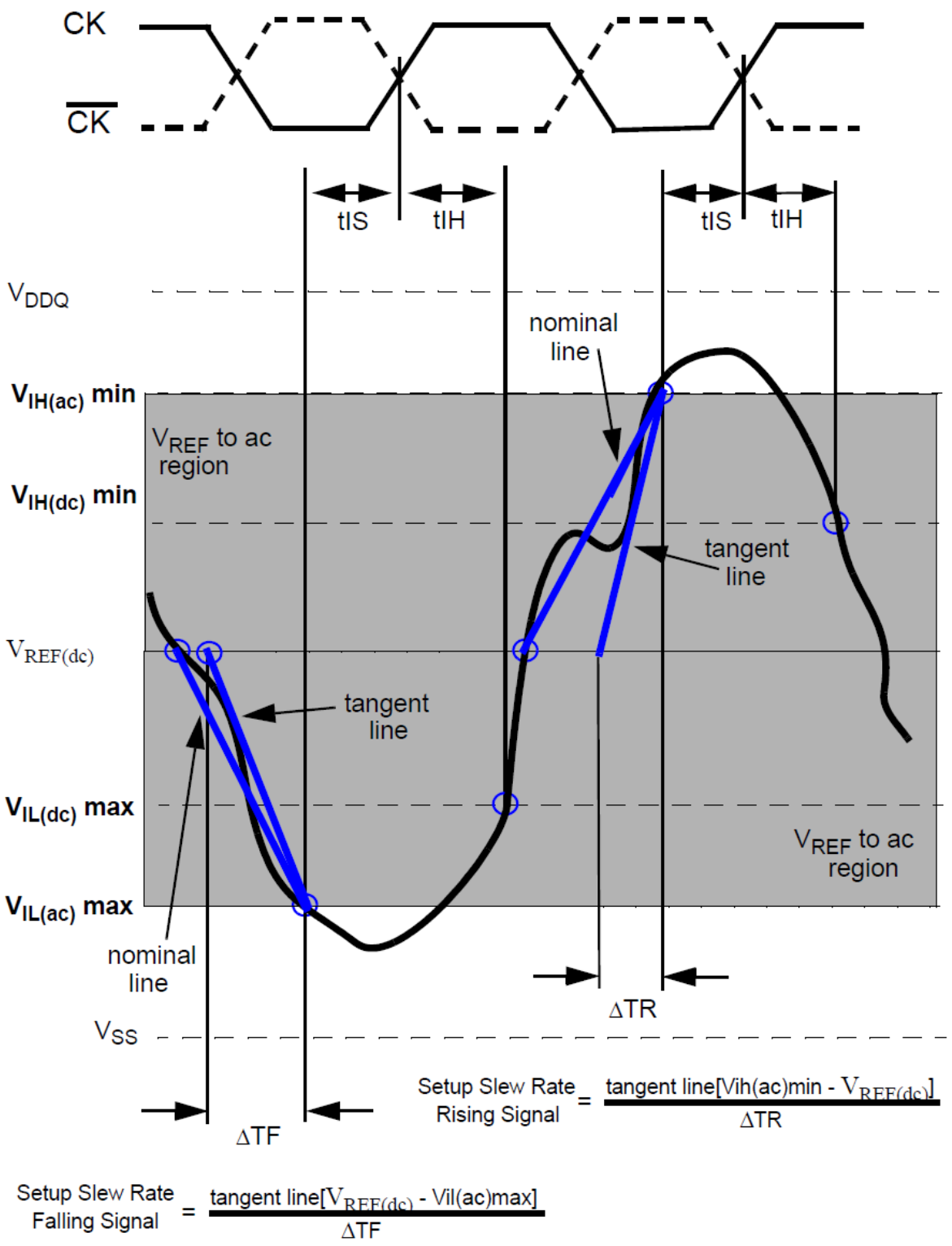
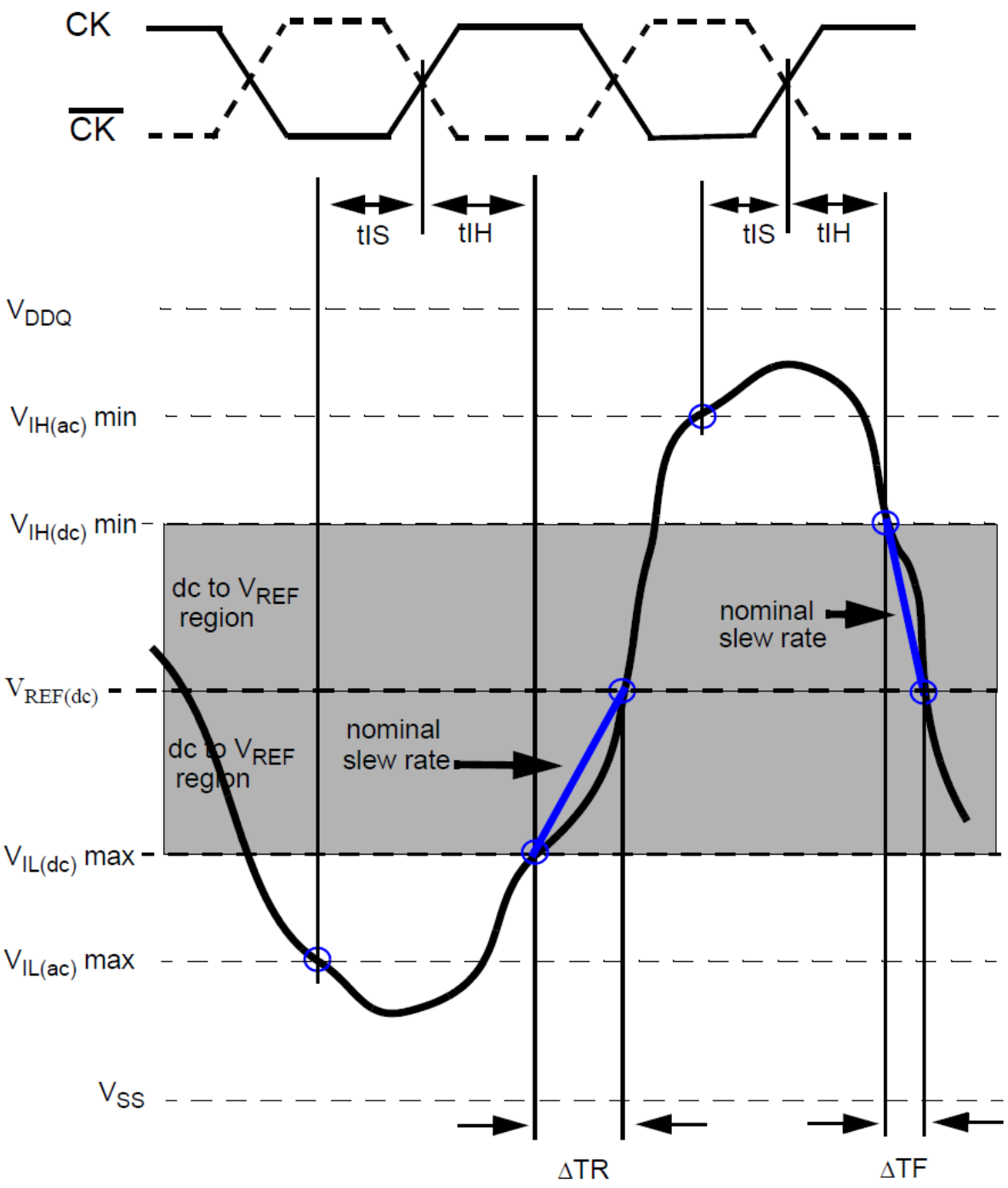


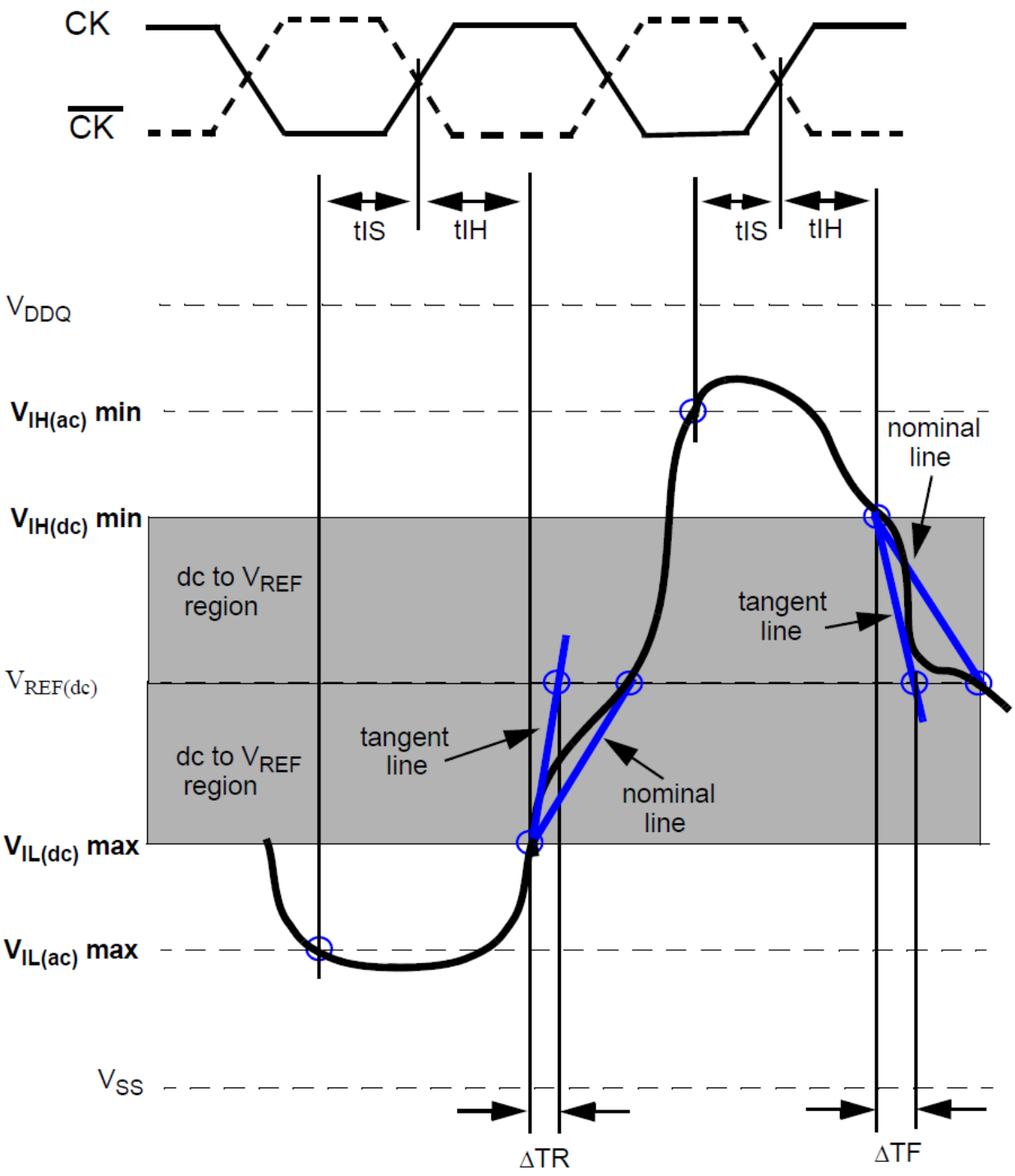
Illustration of nominal slew rate for tIH



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - Vil(dc)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{Vih(dc)min - V_{REF(dc)}}{\Delta TF}$$

Illustration tangent line for tIH



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{REF(dc)} \text{ - Vil(dc)max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [Vih(dc)min - } V_{REF(dc)} \text{]}}{\Delta TF}$$

Specific Note 10 The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

Specific Note 11 MIN (tCL, tCH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

Specific Note 12 tQH = tHP – tQHS, where:

tHP = minimum half clock period for any given cycle and is defined by clock HIGH or clock LOW (tCH, tCL).

tQHS accounts for:

1) The pulse duration distortion of on-chip clock circuits; and

2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

Specific Note 13 tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.

Specific Note 14 tDAL = WR + RU{ tRP[ns] / tCK[ns] }, where RU stands for round up.

WR refers to the tWR parameter stored in the MRS. For tRP, if the result of the division is not already an integer,round up to the next highest integer. tCK refers to the application clock period.

Example: For DDR533 at tCK = 3.75ns with WR programmed to 4 clocks.

tDAL = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.

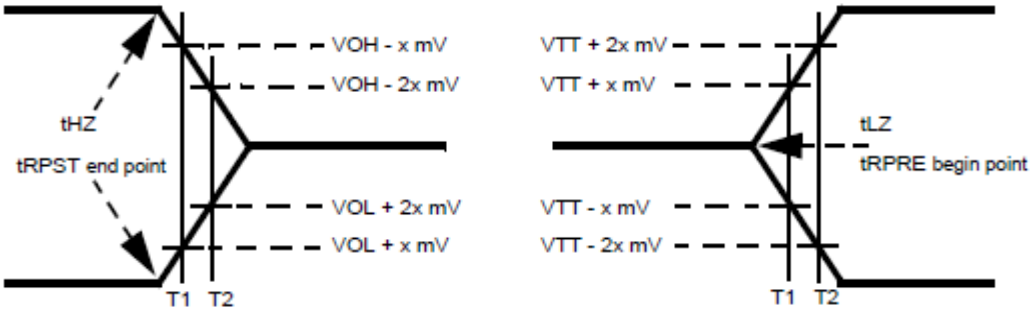
Specific Note 15 The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required.

Specific Note 16 ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND, which is interpreted differently per speed bin. For DDR2-667/800, tAOND is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

Specific Note 17 ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD, which is interpreted differently per speed bin. For DDR2-667/800, if tCK(avg) = 3 ns is assumed, tAOFD is 1.5 ns (= 0.5 x 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

Specific Note 18 tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ) .The following figure shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQ's and tLZ(DQS) refers to tLZ of the (U/L/R)DQS and $\overline{\text{(U/L/R)DQS}}$ each treated as single-ended signal.

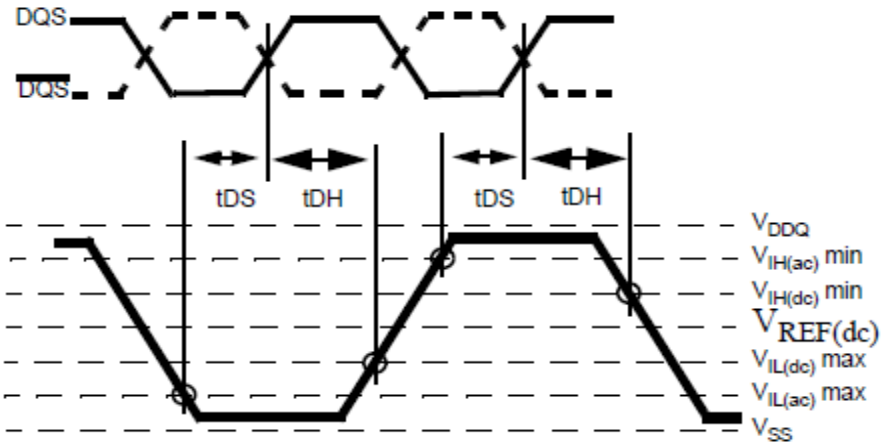
Specific Note 19 tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). The following figure shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.



Method for calculating transitions and endpoints

Specific Note 20 Input waveform timing tDS with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the VIH(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the VIL(ac) level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, $\overline{DQS}$ signals must be monotonic between Vil(dc)max and Vih(dc)min.

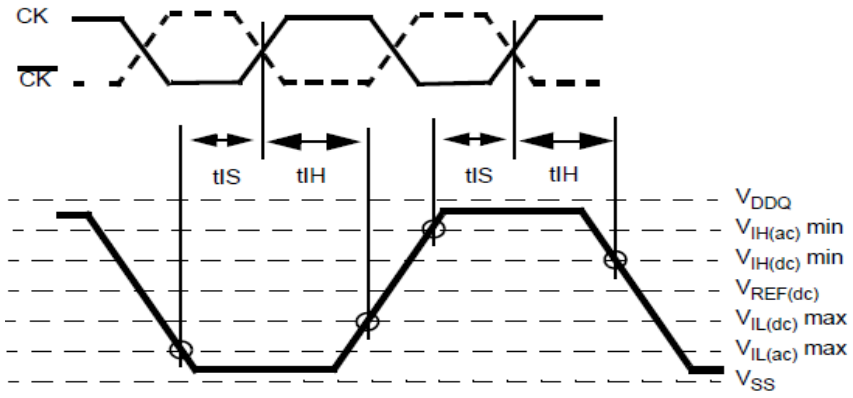
Specific Note 21 Input waveform timing tDH with differential data strobe enabled MR[bit10]=0, is referenced from the differential data strobe crosspoint to the input signal crossing at the VIH(dc) level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the VIL(dc) level for a rising signal applied to the device under test. DQS, $\overline{DQS}$ signals must be monotonic between Vil(dc)max and Vih(dc)min.



Differential input waveform timing – tDS and tDH

Specific Note 22 Input waveform timing is referenced from the input signal crossing at the VIH(ac) level for a rising signal and VIL(ac) for a falling signal applied to the device under test.

Specific Note 23 Input waveform timing is referenced from the input signal crossing at the VIL(dc) level for a rising signal and VIH(dc) for a falling signal applied to the device under test.



Differential input waveform timing – tIS and tIH

Specific Note 24 tWTR is at lease two clocks (2 x tCK or 2 x nCK) independent of operation frequency.

Specific Note 25 Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the VIH(ac) level to the single-ended data strobe crossing VIH/L(dc) at the start of its transition for a rising signal, and from the input signal crossing at the VIL(ac) level to the single-ended data strobe crossing VIH/L(dc) at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

Specific Note 26 Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the VIH(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a rising signal, and from the input signal crossing at the VIL(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

Specific Note 27 tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges.CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.

Specific Note 28 If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

Specific Note 29 These parameters are measured from a command/address signal ($\overline{CKE}$, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note 30 These parameters are measured from a data strobe signal ((L/U/R)DQS/$\overline{DQS}$) crossing to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note 31 These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS/$\overline{DQS}$) crossing.

Specific Note 32 For these parameters, the DDR2 SDRAM device is characterized and verified to support

tnPARAM = RU{tPARAM / tCK(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.

For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which tRP = 15ns, the device will support tnRP =RU{tRP / tCK(avg)} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and active command at Tm+5 is valid even if (Tm+5 - Tm) is less than 15ns due to input clock jitter.

Specific Note 33 tDAL [nCK] = WR [nCK] + tnRP [nCK] = WR + RU {tRP [ps] / tCK(avg) [ps] }, where WR is the value programmed in the mode register set.

ex) For DDR2-1066 7-7-7 at tCK(avg) = 1.875 ns with WR programmed to 8 nCK,

tDAL = 8 + RU{13.125 ns / 1.875 ns} [nCK] = 8 + 7 [nCK] = 15 [nCK]

Specific Note 34 New units, 'tCK(avg)' and 'nCK', are introduced in DDR2-667, DDR2-800 and DDR2-1066

Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation.

Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

ex) tXP = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+2,even if (Tm+2 - Tm) is 2 x tCK(avg) + tERR(2per),min.

ex) tXP = 3 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+3, even if (Tm+3 - Tm) is 3 x tCK(avg) + tERR(3per),min.

Specific Note 35 Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters' and these parameters apply. The jitter specified is a random jitter meeting a Gaussian distribution.

Input clock jitter spec parameter apply

Parameter	Symbol	DDR2-1066		DDR2-800		DDR2-667		Units
		min	max	min	max	min	max	
Clock period jitter	tJIT(per)	-90	90	-100	100	-125	125	ps
Clock period jitter during DLL locking period	tJIT(per,lck)	-80	80	-80	80	-100	100	ps
Cycle to cycle clock period jitter	tJIT(cc)	-180	180	-200	200	-250	250	ps
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-160	160	-160	160	-200	200	ps
Cumulative error across 2 cycles	tERR(2per)	-132	132	-150	150	-175	175	ps
Cumulative error across 3 cycles	tERR(3per)	-157	157	-175	175	-225	225	ps
Cumulative error across 4 cycles	tERR(4per)	-175	175	-200	200	-250	250	ps
Cumulative error across 5 cycles	tERR(5per)	-188	188	-200	200	-250	250	ps
Cumulative error across n cycles,n = 6 ... 10, inclusive	tERR(6-10per)	-250	250	-300	300	-350	350	ps
Cumulative error across n cycles,n = 11 ... 50, inclusive	tERR(11-50per)	-425	425	-450	450	-450	450	ps
Duty cycle jitter	tJIT(duty)	-75	75	-100	100	-125	125	ps

Definitions:

- tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$
$$where \qquad N = 200$$

- tCH(avg) and tCL(avg)

tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

- tJIT(duty)

tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).

tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)}

where,

tJIT(CH) = {tCHi- tCH(avg) where i=1 to 200}

tJIT(CL) = {tCLi- tCL(avg) where i=1 to 200}

- tJIT(per), tJIT(per,lck)

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).

tJIT(per) = Min/max of {tCKi- tCK(avg) where i=1 to 200}

tJIT(per) defines the single period jitter when the DLL is already locked.

tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

tJIT(per) and tJIT(per,lck) are not guaranteed through final production testing.

- tJIT(cc), tJIT(cc,lck)

tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles:

tJIT(cc) = Max of |tCKi+1 – tCKi|

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT(cc,lck) are not guaranteed through final production testing.

- tERR(2per), tERR (3per), tERR (4per), tERR (5per), tERR (6-10per) and tERR (11-50per)

tERR is defined as the cumulative error across multiple consecutive cycles from tCK(avg).

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

$$where \begin{cases} n = 2 & for \quad tERR(2per) \\ n = 3 & for \quad tERR(3per) \\ n = 4 & for \quad tERR(4per) \\ n = 5 & for \quad tERR(5per) \\ 6 \le n \le 10 & for \quad tERR(6-10per) \\ 11 \le n \le 50 & for \quad tERR(11-50per) \end{cases}$$

Specific Note 36 These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (min and max of SPEC values are to be used for calculations in the table below.)

Parameter	Symbol	min	max	Units
Absolute clock period	tCK(abs)	tCK(avg),min + tJIT(per),min	tCK(avg),max + tJIT(per),max	ps
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min x tCK(avg),min +tJIT(duty),min	tCH(avg),max x tCK(avg),max + tJIT(duty),max	ps
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min x tCK(avg),min + tJIT(duty),min	tCL(avg),max x tCK(avg),max + tJIT(duty),max	ps

Example: For DDR2-667, tCH(abs),min = (0.48 x 3000 ps) - 125 ps = 1315 ps

Specific Note 37 tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH. The value to be used for tQH calculation is determined by the following equation;

tHP = Min (tCH(abs), tCL(abs)),

where,

tCH(abs) is the minimum of the actual instantaneous clock HIGH time;

tCL(abs) is the minimum of the actual instantaneous clock LOW time;

Specific Note 38 tQHS accounts for:

1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and

2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers

Specific Note 39 tQH = tHP – tQHS, where:

tHP is the minimum of the absolute half period of the actual input clock; and tQHS is the specification value under the max column.

{The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}

Examples:

1) If the system provides tHP of 1315 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 975 ps minimum.

2) If the system provides tHP of 1420 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 1080 ps minimum.

3) If the system provides tHP of 825 ps into a DDR2-1066 SDRAM, the DRAM provides tQH of 575 ps minimum.

4) If the system provides tHP of 900 ps into a DDR2-1066 SDRAM, the DRAM provides tQH of 650 ps minimum.

Specific Note 40 When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps and tERR(6-10per),max = + 293 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 400 ps - 293 ps = - 693 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 400 ps + 272 ps = + 672 ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ),min(derated) = - 900 ps - 293 ps = - 1193 ps and tLZ(DQ),max(derated)= 450 ps + 272 ps = + 722 ps. (Caution on the min/max usage!)

Specific Note 41 When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(per),min = - 72 ps and tJIT(per),max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 ps = + 2178 ps and tRPRE,max(derated) = tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 93 ps = + 2843 ps. (Caution on the min/max usage!)

Specific Note 42 When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(duty),min = - 72 ps and tJIT(duty),max = + 93ps, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 ps = + 928 ps and tRPST,max(derated) = tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 93 ps = + 1592 ps. (Caution on the min/max usage!)

Specific Note 43 When the device is operated with input clock jitter, this parameter needs to be derated by { -tJIT(duty),max - tERR(6-10per),max } and { - tJIT(duty),min - tERR(6-10per),min } of the actual input clock.(output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps, tERR(6-10per),max = + 293 ps, tJIT(duty),min = - 106 ps and tJIT(duty),max = + 94 ps, then tAOF,min(derated) = tAOF,min+ { - tJIT(duty),max - tERR(6-10per),max } = - 450 ps + { - 94 ps - 293 ps} = - 837 ps and tAOF,max(derated) =tAOF,max + { - tJIT(duty),min - tERR(6-10per),min } = 1050 ps + { 106 ps + 272 ps } = + 1428 ps. (Caution on the min/max usage!)

Specific Note 44 For tAOFD of DDR2-667/800, the 1/2 clock of nCK in the 2.5 x nCK assumes a tCH(avg),average input clock HIGH pulse width of 0.5 relative to tCK(avg). tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH(avg) of 0.48, the tAOF,min should be derated by subtracting 0.02 x tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.52, the tAOF,max should be derated by adding 0.02 x tCK(avg) to it. Therefore, we have;

tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH(avg),min)] x tCK(avg)

tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH(avg),max) - 0.5] x tCK(avg)

or

tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH(avg),min] x tCK(avg))

tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH(avg),max - 0.5] x tCK(avg))

where tCH(avg),min and tCH(avg),max are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls.

Note that these deratings are in addition to the tAOF derating per input clock jitter, i.e. tJIT(duty) and tERR(6-10per).

However tAC values used in the equations shown above are from the timing parameter table and are not derated.

Thus the final derated values for tAOF are;

tAOF,min(derated_final) = tAOF,min(derated) + { - tJIT(duty),max - tERR(6-10per),max }

tAOF,max(derated_final) = tAOF,max(derated) + { - tJIT(duty),min - tERR(6-10per),min }

Revision History

Version	Page	Modified	Description	Released
1.0	All	-	Preliminary Release.	08/2013
1.1	All	-	Official Release.	01/2014
1.2	P1,2,13	CL2	Remove CL2 function.	03/2014

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