L50 Hardware Design

GPS Module Series

Rev. L50_Hardware_Design_V2.1

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About the Document

History

Revision	Date	Author	Description
1.0	2011-08-17	Baly BAO/ Harry LIU	Initial
1.1	2012-03-28	Baly BAO	1. Emphasized only hardware-base I2C communication is supported. 2. Peak supply current is changed to 60mA. 3. Deleted the content related to 18 × 18 antenna. 4. The recommended battery is changed to MS920SE. 5. Added reference designs for ON_OFF and RESET. 6. Optimized the reference design for UART interface and I2C interface. 7. Modified the timing chart. 8. Modified the current consumption.
2.0	2013-4-10	Ray XU	1. Modified Figure 19，Figure 26 and added Table 18. 2. Added chapter 7.5: Ordering information. 3. Removed pulled up resistor in Figure 11 4. Added new features based on SiRFROM2.2 version. ● Added Chapter 3.11: Fast Time-sync. ● Added Chapter 3.10: Hardware Baud Rate Configuration. ● Modified the current consumption in tracking, acquisition, hibernate mode as well as ATP, PTF mode. ● Modified max update rate. ● Modified Figure 17: Reference Design for CGEE Function. 5. Added notes in chapter 3.9.
2.1	2014-06-11	Ray XU	Updated packaging information.

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1 Introduction

This document defines and specifies L50 GPS module. It describes L50 hardware interface and its external application reference circuits, mechanical size and air interface.

This document can help you quickly understand L50's interface specifications, electrical and mechanical characteristics. Associated with application notes, you can use L50 module to design and set up application easily.

2 Product Concept

2.1. General Description

L50 is a GPS ROM-based module with embedded GPS patch antenna and features fast acquisition and tracking with the latest SiRF Star IV ROM2.2 technology. This module provides outstanding GPS performance in a slim package. Based on an external optional EEPROM which provides capability of storing ephemeris and downloading patch codes through UART, L50 can support Standalone and A-GPS (CGEE function). Advanced jamming suppression mechanism and innovative RF architecture, L50 provides a higher level of anti-jamming and ensures maximum GPS performance. The module supports location, navigation and industrial applications including autonomous GPS C/A, SBAS (WAAS, EGNOS and QZSS) and A-GPS. Furthermore, a patch antenna has been designed into the L50 module. This will reduce your design complexity greatly.

- L50, in SMD type, can be embedded in your applications via the 24-pin pads with the slim 28×16×3mm package. It provides all hardware interfaces between the module and host board.
- The multiplexed communication interface: UART/I2C interface.
- The Dead Reckoning I2C interface up to 400Kbps can be used to connect with an external EEPROM to save ephemeris data for CGEE function and to store patch codes.

The module is RoHS compliant to EU regulation.

2.2. Key Features

The following table describes the detailed features of L50 module.

Table 1: Module Key Features

Feature	Implementation
Power Supply	Supply voltage: 1.71V - 1.89V typical: 1.8V
Power Consumption	● Acquisition 33 mA @ -130dBm ● Tracking 31 mA @ -130dBm ● Hibernate 14uA
Receiver Type	● GPS L1 1575.42MHz C/A Code ● 48 search channels
Sensitivity(NOTE2)	● Reacquisition -160dBm ● Tracking -163dBm ● Acquisition -148dBm
Time-To-First-Fix(NOTE1)	● Cold Start (Autonomous) <33s ● Warm Start (Autonomous) <33s ● Warm Start (With CGEE) 10s typ. ● Hot Start (Autonomous) <1s
Horizontal Position Accuracy	● <2.5 m CEP
Max Update Rate	● 5Hz 1Hz by default
Accuracy of 1PPS Signal	● Typical accuracy 500 ns ● Time pulse 200ms
Velocity Accuracy	● Without aid 0.01m/s
Acceleration Accuracy	● Without aid 0.1m/s²
Dynamic Performance	● Maximum altitude 18288m ● Maximum velocity 514m/s ● Acceleration 4 G
Dead Reckoning I2C Interface	● CGEE ● Hardware baud rate configuration ● MEMS support (TBD devices) ● Standard I2C bus maximum data rate 400kbps ● Minimum data rate 100kbps
Communication Interface	● Support multiplexed UART/I2C interface ● The output is CMOS 1.8V compatible and the input is 3.6V tolerant

Temperature Range	● Normal operation: -40°C ~ +85°C ● Storage temperature: -45°C ~ +125°C
Physical Characteristics	Size: 28±0.15 mm×16±0.15 mm×3±0.2mm Weight: Approx. 4 g

NOTES

1. TTFF listed in above table is measured in conducted method by 8-star GPS simulator.
2. The sensitivity is measured in conducted method.

2.3. Functional Diagram

The block diagram of L50 is shown in the following figure.

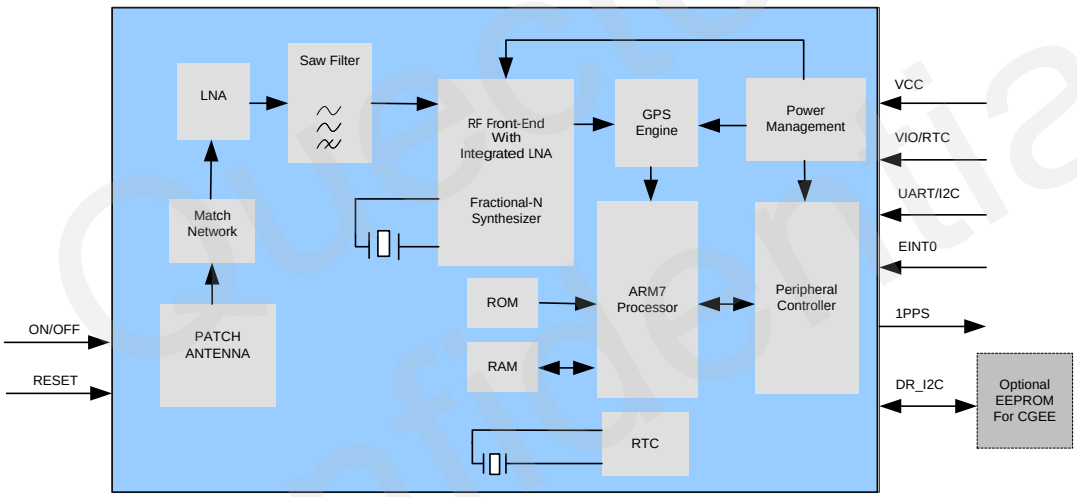


Figure 1: Module Functional Diagram

2.4. Evaluation Board

In order to help you to develop applications with L50, Quectel offers an Evaluation Board (EVB) with appropriate power supply, RS-232 serial port and EEPROM.

NOTE

For more details, please refer to the ***document [1]***.

2.5. Protocol

L50 supports standard NMEA-0183 protocol and the One Socket Protocol (OSP), which is the binary protocol interface that enables your host device to access all SiRF GPS chip products of the SiRF Star IV family and beyond. The module is capable of supporting the following NMEA formats: ***GGA, GSA, GLL, GSV, RMC, and VTG.***

Table 2: The Module Supports Protocols

Protocol	Type
NMEA	Input/output, ASCII, 0183, 3.01
OSP	Input/output, OSP protocol

NOTE

Please refer to ***document [2]*** about NMEA standard protocol and SiRF private protocol.

3 Application Interface

3.1. General Description

L50 is a 24-pin surface mounted device (SMD) which could be embedded into your application conveniently. Sub-interfaces included in these pins are described in details in the following chapters:

3.2. Pin Assignment of the Module（Bottom view）

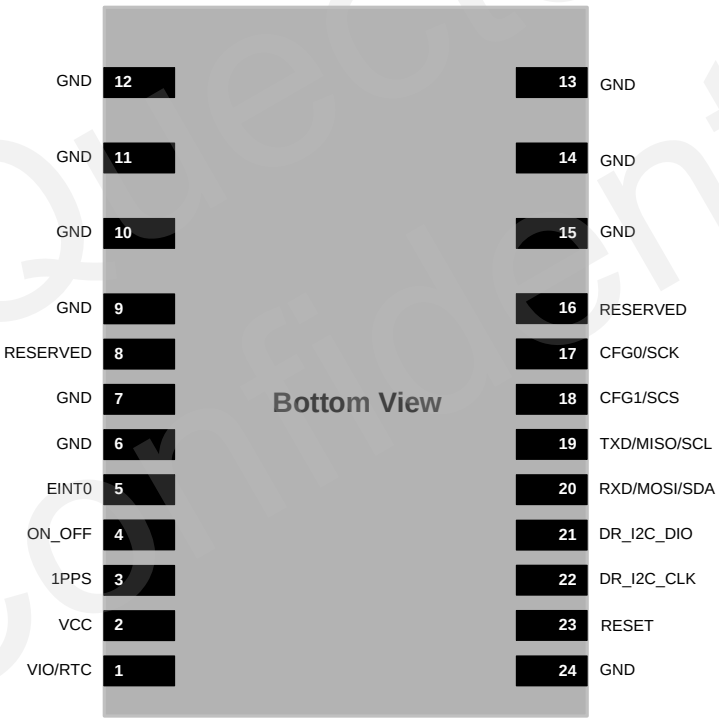


Figure 2: Bottom View of the Module

3.3. Pin Description

Table 3: Pin Description

Power Supply					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
VCC	2	I	Supply voltage	Vmax=1.89V Vmin=1.71V Vnom=1.8V	Supply current should be no less than 100mA.
VIO/RTC	1	I	RTC and CMOS I/O voltage supply	Vmax=1.89V Vmin=1.71V Vnom=1.8V $I_{VIO/RTC}$=14uA@ Hibernate mode(VCC=1.8V)	Power supply for RTC and CMOS I/O. In FULL_ON mode, make sure both VIO/RTC and VCC are simultaneously powered on. In Hibernate mode, make sure VIO/RTC is powered on to keep the data lossless.
General Purpose Input/output					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
RESET	23	I	External reset input, active low	VILmin=0V VILmax=0.45V VIHmin= 0.7* VIO/RTC VIHmax=3.6V	The system reset is provided by the RTC monitor circuit and it is active low. If unused, leave this pin unconnected.
EINT0	5	I	External interrupt input pin	VILmin=0V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	Pull this pin down to ground directly.
ON_OFF	4	I	Power control pin	VILmin=0V VILmax=0.45V VIHmin= 0.7* VIO/RTC VIHmax=3.6	If the pin is pulled down for at least 1ms and then released, the module will switch its working mode between Hibernate and FULL_ON.
1PPS	3	O	One pulse per second	VOLmin=0V VOLmax=0.4V VOHmin=0.75*VCC	1PPS output provides a pulse signal for time purpose. If unused, leave this pin unconnected.
Serial Interface					

PIN NAME	PIN NO.	I/O	DESCRIPTION	DC CHARACTERISTICS	COMMENT
DR_I2C_DIO	21	I/O	● Dead Reckoning I2C data (SDA) ● Baud rate configuration	VOLmax=0.4V VOHmin=0.75*VCC VILmin=0V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	If unused, leave this pin unconnected.
DR_I2C_CLK	22	O	● Dead Reckoning I2C clock(SCL) ● Baud rate configuration	VOLmax=0.4V VOHmin=0.75*VCC	If unused, leave this pin unconnected.
CFG0/ SCK	17	I	Configure Pin 0	VILmin=0V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	When serial port is configured as UART, pull up to VCC via a 10k resistor.
CFG1/ SCS	18	I	Configure Pin 1	VILmin=0V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	When serial port is configured as I2C, pull down to GND via a 10k resistor.
RXD/ MOSI/ SDA	20	I/O	Function overlay: ● UART_RX UART data receive (RXD) ● I2C_DIO I2C data (SDA)	VOLmax=0.4V VOHmin=0.75*VCC VILmin=0V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	
TXD/ MISO/ SCL	19	I/O	Function overlay: ● UART_TX UART data transmit (TXD) ● I2C_CLK I2C clock (SCL)	VOLmax=0.4V VOHmin=0.75*VCC VILmin=0V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	

Others					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
GND	6,7,9, 10,11, 12, 13,14, 15, 24		Ground		
Reserved	8,16		Reserved		Leave them unconnected.

3.4. Operating Modes

The table below briefly summarizes the various operating modes in the following chapters.

Table 4: Overview of Operating Modes

Mode		Function
Full on mode	Acquisition mode	The module starts to search satellite, determine visible satellites and coarse carrier frequency and code phase of satellite signals. When the acquisition is done, it switches to tracking mode automatically.
	Tracking mode	The module refines acquisition's message, as well as keeps tracking and demodulating the navigation data from the specific satellites.
Hibernate mode		Hibernate mode means a low power state where only the internal I/O keeps alive, non-volatile RTC, patch RAM and backup RAM block is powered on. Other internal blocks like digital baseband and RF are internally powered off

3.5. Power Management

There are two power supply pins in L50, VCC and VIO/RTC.

3.5.1. VCC Power

VCC pin supplies power for GPS BB domain and GPS RF domain. The power supply VCC's current varies according to the processor load and satellite acquisition. Typical VCC max current is 60 mA. So it is

important that the power is clean and stable. Generally, ensure that the VCC supply ripple voltage meets the requirement: 54 mV (RMS) max @ f=0~3MHz and 15 mV (RMS) max @ f >3 MHz.

Table 5: Pin Definition of the VCC pin

Name	Pin	Function
VCC	2	Power supply for GPS BB and RF part

3.5.2. VIO/RTC Power

The VIO/RTC pin supplies power for all RTC domain and CMOS I/O domain, so VIO/RTC should be powered all the time when the module is running. It ranges from 1.71V to 1.89V. In order to achieve a better Time To First Fix (TTFF) after VCC powers down, VIO/RTC should be valid all the time. It can supply power for SRAM memory which contains all the necessary GPS information for quick start-up and a small amount of user configuration variables.

Table 6: Pin Definition of the VIO/RTC Pin

Name	Pin	Function
VIO/RTC	1	Power supply for RTC and CMOS /IO

3.5.3. Energy Saving Mode

3.5.3.1. ATP Mode

Adaptive trickle power (ATP): In this mode, L50 cycles three modes internally to optimize power consumption. These three modes consist of FULL_ON mode, CPU only mode and standby mode. The FULL_ON mode lasts typically 300ms to require new ephemeris to get a valid position, and the other two modes are partially powered off or completely powered off to decrease power consumption. The timing sequence is shown in following figure. This mode is configurable with SiRF binary protocol message ID151. The following diagram is a default configuration and it is tested in the strong signal environment. When the signal becomes weak, it will not comply with the following rule. The weaker the signal is, the longer time the module lasts in FULL_ON mode. In the extreme condition, when there is no signal input, the mode cycles only two modes, which are FULL_ON and standby mode.

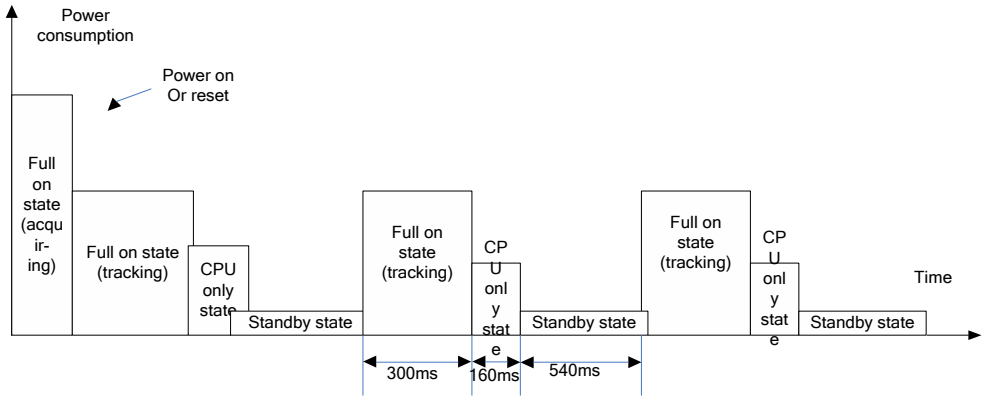


Figure 3: ATP Timing Sequence

Example:
GPS signal generator provides-130dBm GPS signal.
Send command "A0A2000997000000C8000000C80227B0B3" to set the following parameters for the module and make L50 enter into Adaptive Trickle Power mode:
Update frequency: 1 Hz
On-time: 200 ms
The average current in Adaptive Trickle Power mode is about 11 mA.

3.5.3.2. PTF Mode

Push to fix (PTF): In this mode, L50 is configured to be waked up periodically, typically every 1800 seconds (configurable range 10~7200 seconds) for updating position and collecting new ephemeris data from valid satellites. For the rest of the time, the module stays in Hibernate mode. A position request acts as a wakeup of the module, which is then able to supply a position within the hot-start time specification.This mode is configurable with SiRF binary protocol message ID167 and the following figure is the default configuration. Additionally, when the signal becomes weak, pushing to fix function is not valid.

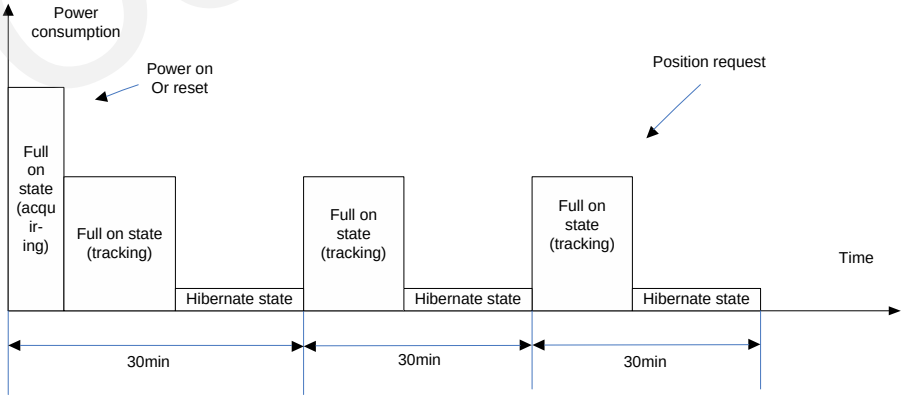


Figure 4: PTF Timing Sequence

Example：
GPS signal generator provides-130dBm GPS signal.
Send command “A0A2000FA7000075300001D4C00000003C0000031DB0B3” to set the following parameters for L50 module:

- Maximum time for sleep mode: 30 seconds
- Max. Satellite search time: 120 seconds
- Cycle time: 60 seconds

Send command “A0A2000997000100C8000000C80227B0B3” to make L50 enter into Push-to-Fix mode. The average current in Push-to-Fix mode is about 2.5 mA.

3.5.3.3. Hibernate Mode

Hibernate mode means low power consumption. Some power domains are powered off such as ARM, DSP and RF part, but the RTC domain includes all non-volatile logic, and the RAM, and GPS BB logic I/O are still active. The module is woken up from Hibernate mode on the next ON_OFF (at rising edge) using all internal aided information like GPS time, Ephemeris, Last Position and so on, to carry out a fast TTFF in either Cold or Warm start mode.

NOTE

L50 should be switched to Hibernate mode firstly by controlling ON_OFF pin, if you need to cut off VCC of L50.

3.6. Power Supply

3.6.1. Power Reference Design

The following diagram is one solution of power supply for L50 module. You can follow this reference design to get a short TTFF in either warm start or cold start. One concern of this design is that the battery will take the place of VCC_3.3 to supply power for RTC and CMOS I/O of the module when VCC_3.3 is absent. Furthermore, VCC_3.3 will charge the battery when it is active.

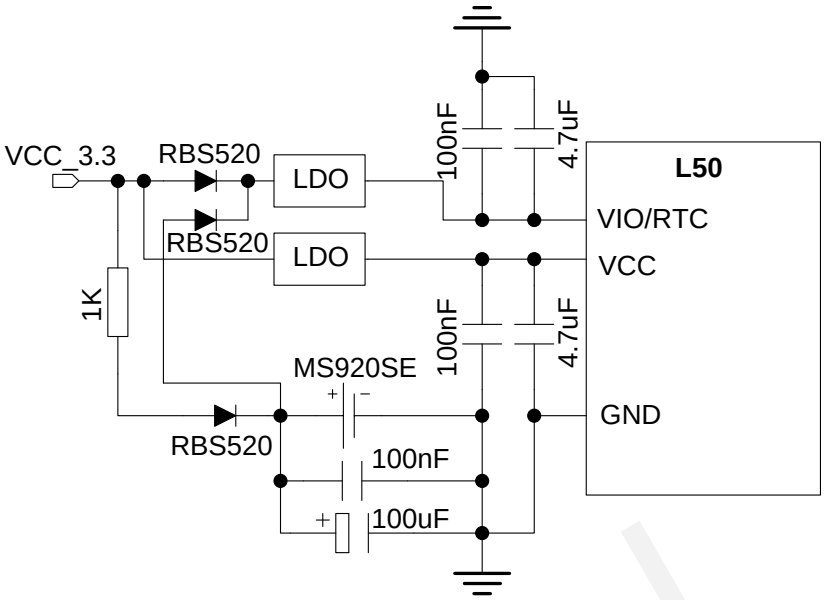


Figure 5: Power Design Reference for L50 Module

3.6.2. Battery

In this part, the charging circuit of battery is introduced and MS920SE is chosen as an example, the following circuit is the reference design.

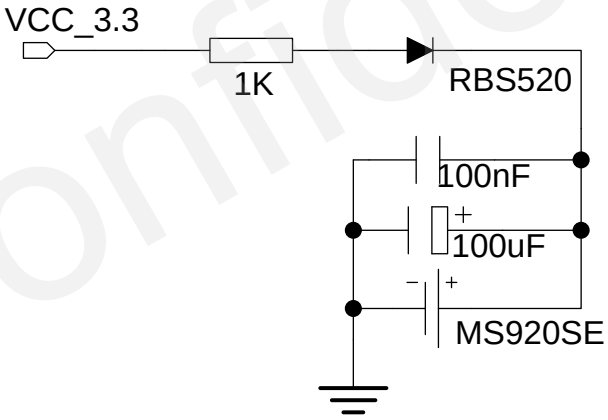


Figure 6: Reference Charging Circuit for Chargeable Battery

Coin-type rechargeable battery such as MS920SE from Seiko can be used and the schottky diode such as RB520S30T1G from ON Semiconductor is recommended to be used here for its low voltage drop. The discharging characteristic of MS920SE is shown in the following figure.

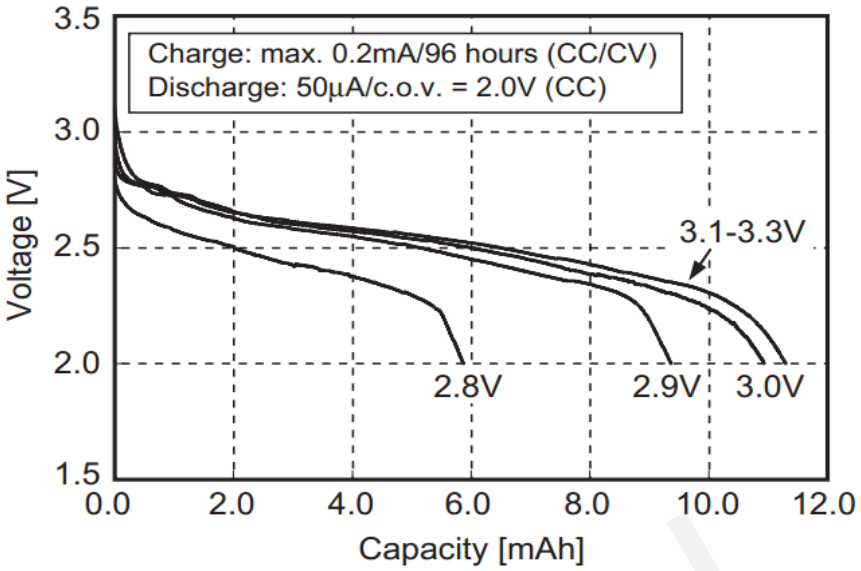


Figure 7: Discharging Characteristics of MS920SE

3.7. Timing Sequence

The ON_OFF pin is used to switch the module between FULL_ON mode and Hibernate mode.

L50 integrates internal power on reset circuit with external RESET signal which belongs to VIO/RTC domain. When VCC and VIO/RTC are supplied simultaneously, the internal power on reset circuit executes. Normally, external control of RESET is not necessary.

The following diagram is the reference timing sequence. Firstly, VCC and VIO/RTC power on, then a pulse of wakeup will be generated, after that when ON_OFF is toggled, the module will go into the FULL_ON mode and the WAKEUP will turn to high level. Next toggling of the ON_OFF will make the module return to the Hibernate mode. The state conversion is shown in the following figure.

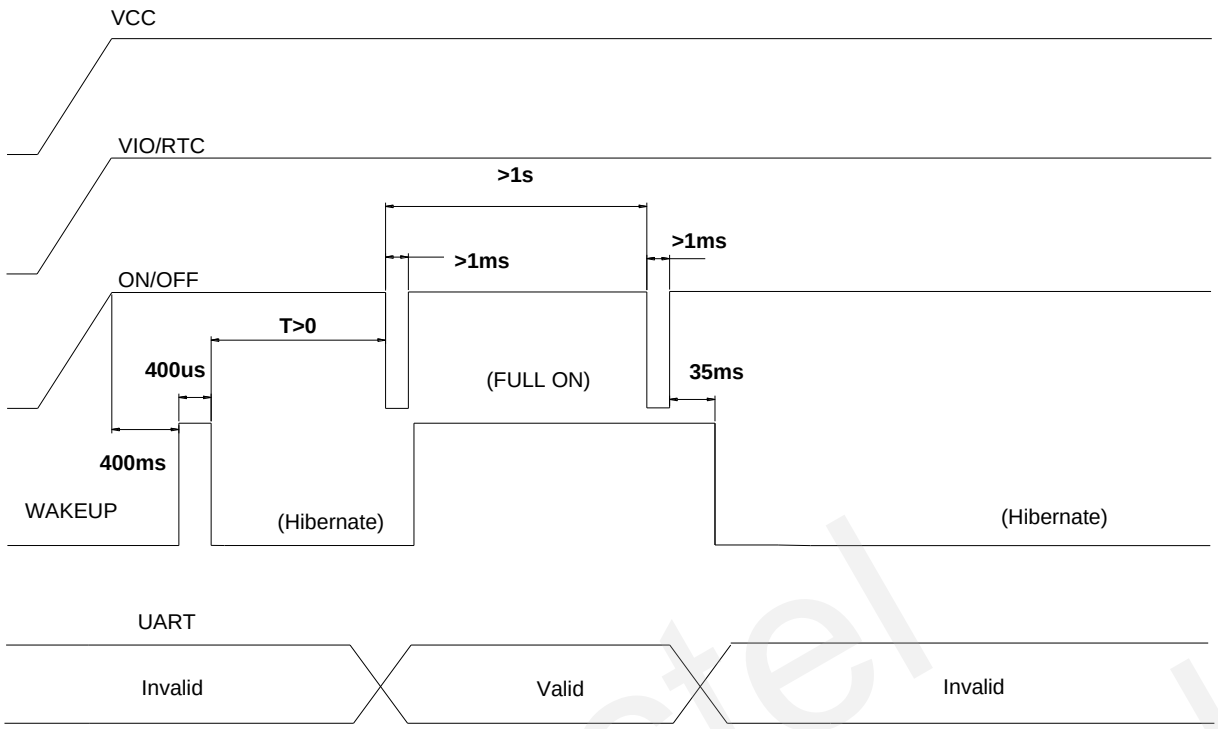


Figure 8: Turn on Timing Sequence of Module

NOTES

1. If the “ON_OFF” pin is controlled by host controller, a 1KΩ resistor should be inserted between the GPIO of the controller and “ON_OFF” pin.
2. WAKEUP is an internal signal of L50.

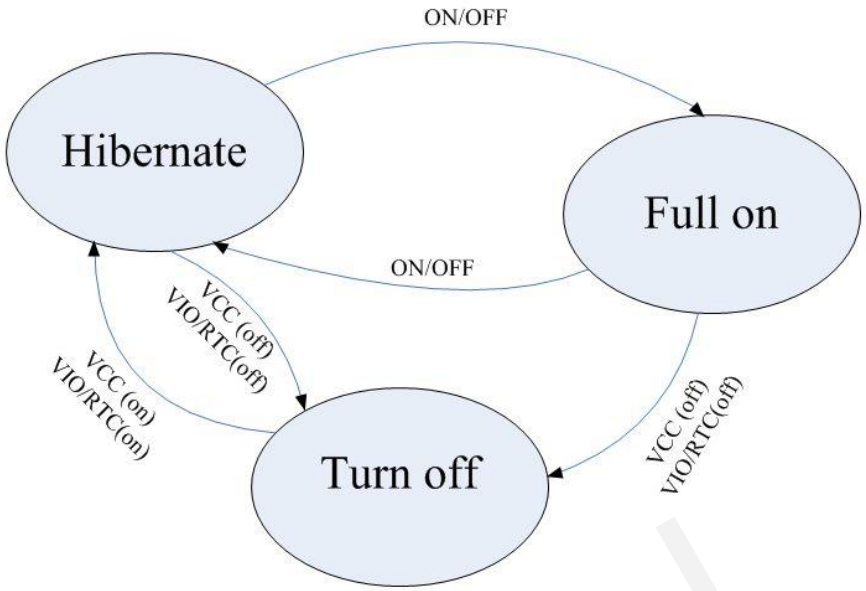


Figure 9: State Conversion of Module

As to the 3V or 3.3V system, the reference design for ON_OFF pin is shown as below.

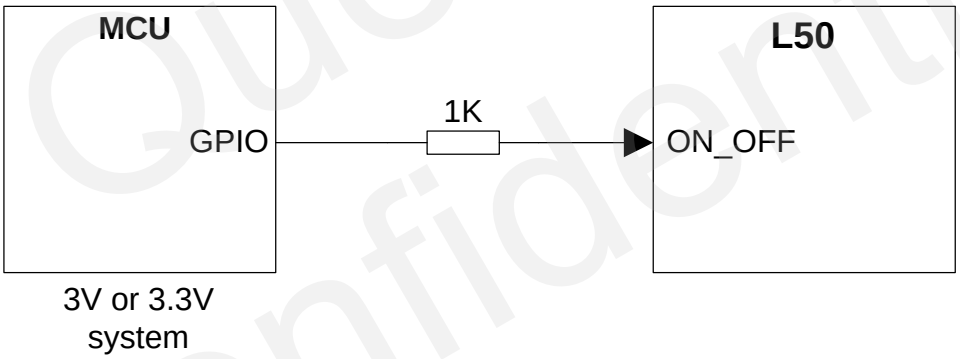


Figure 10: ON_OFF Design for 3V or 3.3V System

For 5V system, the reference design for ON_OFF pin is shown in the following figure.

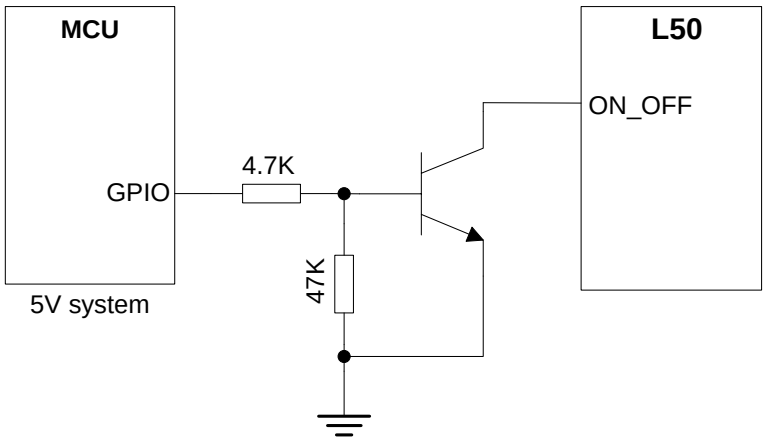


Figure 11: ON_OFF Design for 5V System

If RESET pin is used, please refer to the following design.

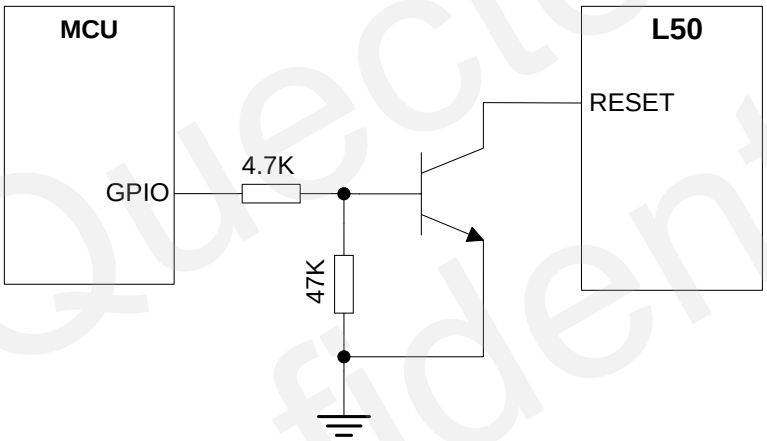


Figure 12: Reference Design for RESET

3.8. Communication Interface

Communication interface which includes UART interface/I2C interface is used to output NMEA messages or to communicate with your device via the OSP protocol. All these interfaces are multiplexed on a share set of pins. The interface selection is not intended to be changed dynamically but only at boot time.

Table 7: Multiplexed Functional Pins for Communication Interface

Pin Name	Pin NO.	Communicate Interface	
		UART	I2C
CFG0/SCK	17	Pull up	Open
CFG1/SCS	18	Open	Pull down
RXD/MOSI/SDA	20	Data receive	I2C data (SDA)
TXD/MISO/SCL	19	Data transmit	I2C clock (SCL)

3.8.1. UART Interface

L50 offers multiplexed pins which can be configured as one UART interface and CFG0/SCK should be pulled up to VCC via a 10K resistor. The module is designed as a DCE (Data Communication Equipment). Serial port TXD/MISO/SCL is connected to UART RX of your device, while serial port RXD/MOSI/SDA is connected to UART TX of your device. It supports data baud rate from 4800bps to 115200bps, meanwhile you can change the baud rate by SIRF binary protocol message ID 134.

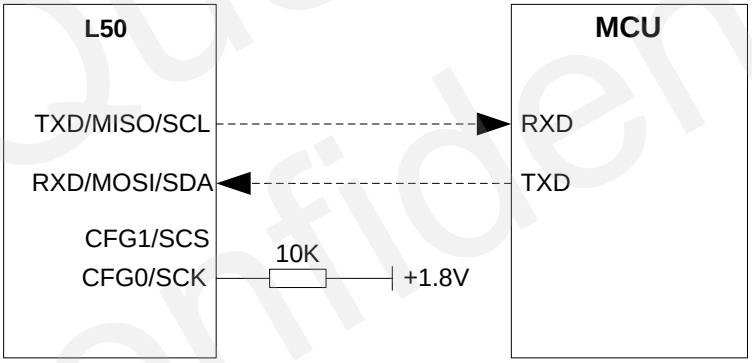


Figure 13: Reference Design for UART Interface

This UART interface has the following features:

- The UART interface can be used to output NMEA and input & output OSP messages.
  The default types of NMEA output are **RMC, GGA, GSA, and GSV (after successful positioning).**
- The UART interface supports the following data rates:
  4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200.
  The default setting is 4800bps, 8 bits, no parity bit, 1 stop bit, no hardware flow control.
- The output is CMOS 1.8V compatible and the input is 3.6V tolerant.

NOTE

It is strongly recommended that the UART interface is used to output NMEA message to serial port of host processor.

The UART interface does not support the RS-232 level. It supports the TTL/CMOS level. If the module's UART interface is connected to the UART interface of a computer, it is necessary to insert a level shift circuit between the module and the computer. Please refer to the following figure.

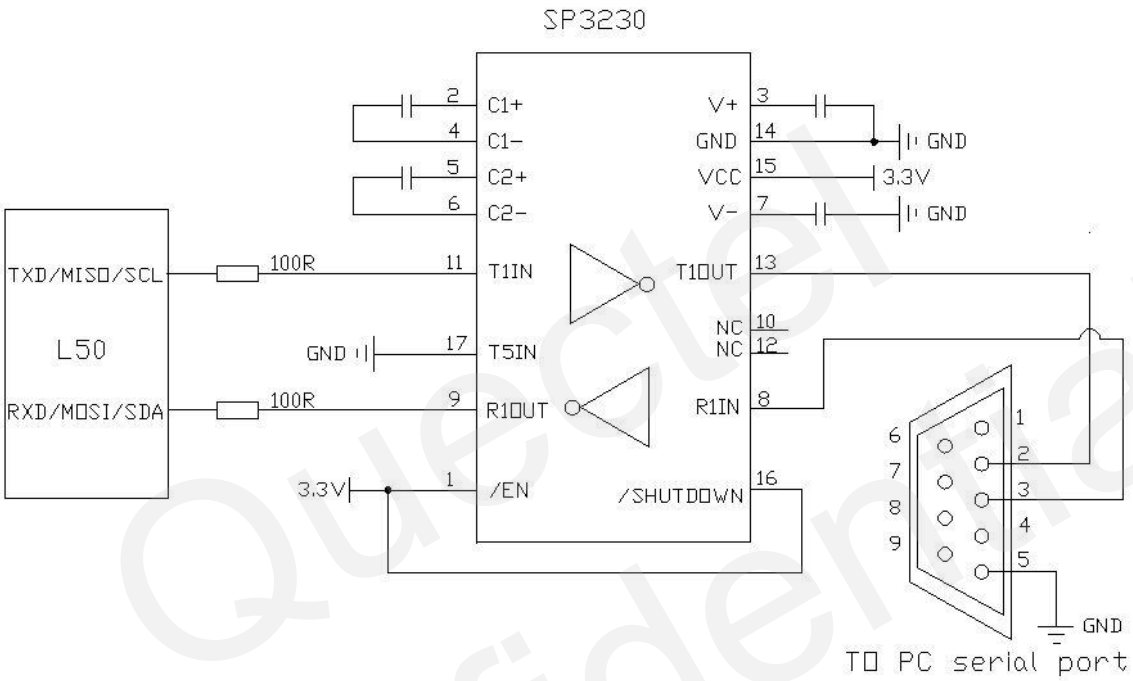


Figure 14: RS-232 Level Shift Circuit

3.8.2. I2C Interface

L50 provides multiplex function via TXD/MISO/SCL, RXD/MOSI/SDA and CFG1/SCS to construct I2C interface. Communication interface is configured as I2C by pulling down CFG1/SCS. The default mode is master mode. It is important that you must pull up these two pins via 2.2K resistor for the OC/OD interface. Otherwise, there is no signal output. In addition, only hardware-based I2C communication is supported. This interface acts as a master when it outputs NMEA data, while it is a slave when it receives commands.

This I2C interface has the following features:

- Operate up to 400kbps.
- Support Multi-master I2C mode by default.
- Default I2C address values are RX: 0x60, TX: 0x62.

The following figure is the I2C timing sequence.

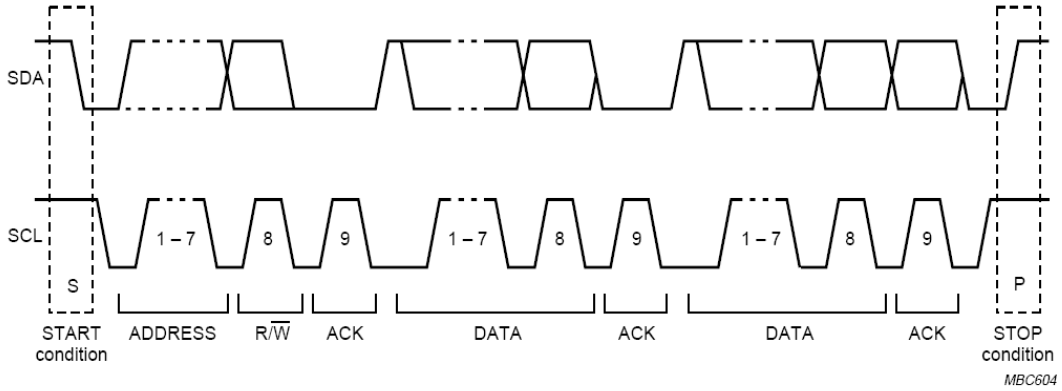


Figure 15: I2C Timing Sequence

The following circuit is an example of connection.

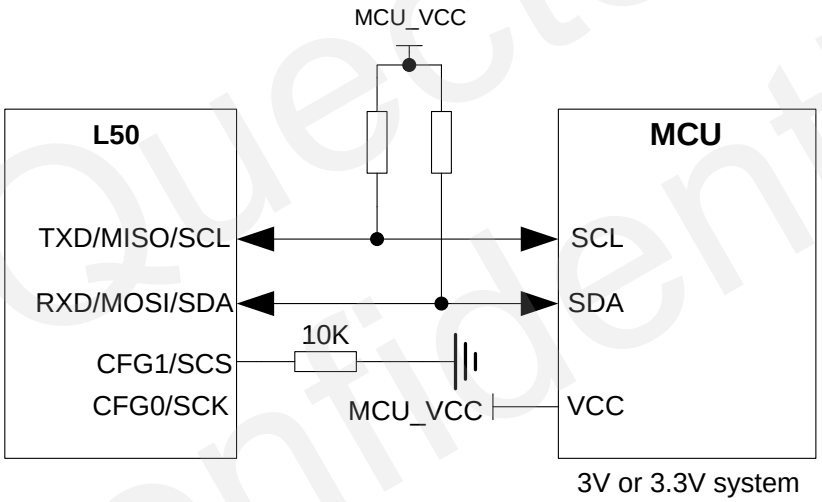


Figure 16: Reference Design for I2C Interface

NOTE

The above figure only shows the reference design of I2C interface for the 3V or 3.3V system. For 5V system, a level shifter should be used.

3.8.3. SPI Interface

The Serial Peripheral Interface (SPI) provides access to a flexible, full-duplex synchronous serial bus. However, L50 does not support SPI at present.

3.9. Assisted GPS

By supplying aided information like ephemeris, almanac, rough last position, time and satellite status, A-GPS can help improve TTFF and the acquisition sensitivity of the GPS receiver.

L50 supports one kind of A-GPS called Client Generated Extended Ephemeris (CGEE) which ensures fast TTFF up to 3 days. The CGEE data is generated internally from satellite ephemeris as a background task, and then L50 collects ephemeris from as many satellites as possible before entering Hibernate mode.

The CGEE functionality requires that VIO/RTC power supply is kept active all the time and an external 1Mbit EEPROM connected to DR_I2C bus for CGEE data storage. The recommended EEPROMs are in the following table and they are verified.

Table 8: Recommended EEPROM

Manufacturer	Part Number
ST	M24M01
Seiko Instruments Inc.	S-24CM01C
Atmel	AT24C1024B

NOTES

1. The part number which we recommend is a series part number, please get more details from the datasheet such as operation voltage and package.
2. L50@ROM2.2 only supports 1.8V EEPROM.
3. DR_I2C_DIO and DR_I2C_CLK pins have been pulled up to VCC internally.

Table 9: Pin Definition of the DR_I2C Interfaces

Interface	Name	Pin	Function
Dead Reckoning I2C Interface	DR_I2C_DIO	21	I2C data (SDA)
	DR_I2C_CLK	22	I2C clock (SCL)

The DR_I2C_DIO and DR_I2C_CLK pins have been pulled up to VCC. The following circuit is the reference design for L50 and EEPROM.

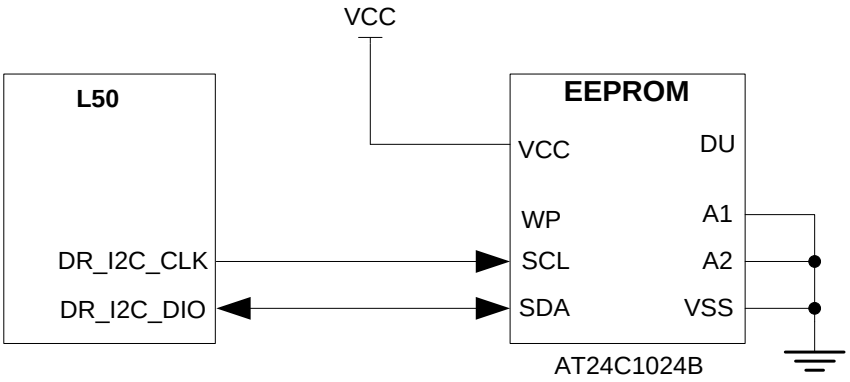


Figure 17: Reference Design for CGEE Function

3.10. Hardware Baud Rate Configuration

Excluding Dead Reckoning I2C interface, DR_I2C_DIO, DR_I2C_CLK pins can also be used as the baud rate configuration pins of UART, but these two functions cannot be used simultaneously. Note that these two pins have been pulled high internally to VCC in the module. So you can just pull 200ohm resistor to ground to have a pull low action and let the pin floating to have a pull high action. Pay attention that hardware baud rate configuration should be done before starting the module, or it is not available.

This baud rate configuration is not available if any EEPROM is attached to these two pins. The default baud rate is NMEA 4800 when an EEPROM device is attached, but can be changed via OSP message, for more details, please refer to the ***document [2].***

The following table has shown the baud rate configuration list. As DR_I2C_DIO, DR_I2C_CLK pins have been pulled high internally to VCC, the default setting of UART is NMEA in 4800bps if these two pins are floating. Note that the function described in this chapter is based on SiRF ROM2.2 version.

Table 10: Baud Rate Configuration

DR_I2C_DIO	DR_I2C_CLK	Protocol	Baud Rate
Floating	Floating	NMEA	4800
Floating	Pull low	NMEA	9600
Pull low	Floating	NMEA	38400

3.11. Fast Time-sync

L50 provides Fast time-sync function for special application to reduce power consumption. These special applications include watches and clocks for UTC time. It uses technique that limits how many message the satellite navigation must be observed before it declares the correct time. Due to this technique, the module will find the time very quickly compared to normal operation. It is about 6 seconds to get the UTC time in the condition of one visible satellite with C/N value bigger than 23 in static states. You can turn off the module immediately once the UTC time is got to save power consumption. This function is disabled by default and it can be enabled by OSP Message ID 136, for more details, please refer to the ***document [2].***

4 Radio Frequency

L50 receives L1 band signal from GPS satellites at a nominal frequency of 1575.42MHz. It is an ultra slim module with embedded 15.0×15.0×2.0 mm patch antenna. Alongside highest reliability and quality of patch antenna, L50 also offers 48 PRN channels, which allows the module to acquire and track satellites in the shortest time, even at a very low signal level.

4.1. Antenna

The quality of the embedded GPS antenna is crucial to the overall sensitivity of the GPS system. L50 offers an on-module patch antenna. A 15.0×15.0×2.0mm patch antenna is chosen for reducing product size. This antenna is specially designed for satellite reception applications. And it has excellent stability and sensitivity to consistently provide high signal reception efficiency. The specification of the antenna used by L50 is described in following table.

Table 11: Antenna Specification for L50 Module

Antenna type	Parameter	Specification	Notes
Patch Antenna	Size	15.0×15.0×2.0mm	
	Range of receiving Frequency	1575.42MHz±1.023MHz	
	Impendence	50 Ohm	
	Band Width	10MHz minimum	Return Loss≦-10dB
	Frequency Temperature Coefficient (TF)	0±20ppm/°C	-40°C-150°C
	Polarization	RHCP	Right Hand Circular Polarization
	Gain at Zenith	1.0dBi typ.	Centre frequency
	VSWR	1.5 max	
	Axial ratio	3 dB max	

The test result of the antenna used by L50 is shown in following figure. This embedded GPS antenna provides good radiation efficiency, right hand circular polarization and optimized radiation pattern. The antenna is insensitive to surroundings and has high tolerance against frequency shifts.

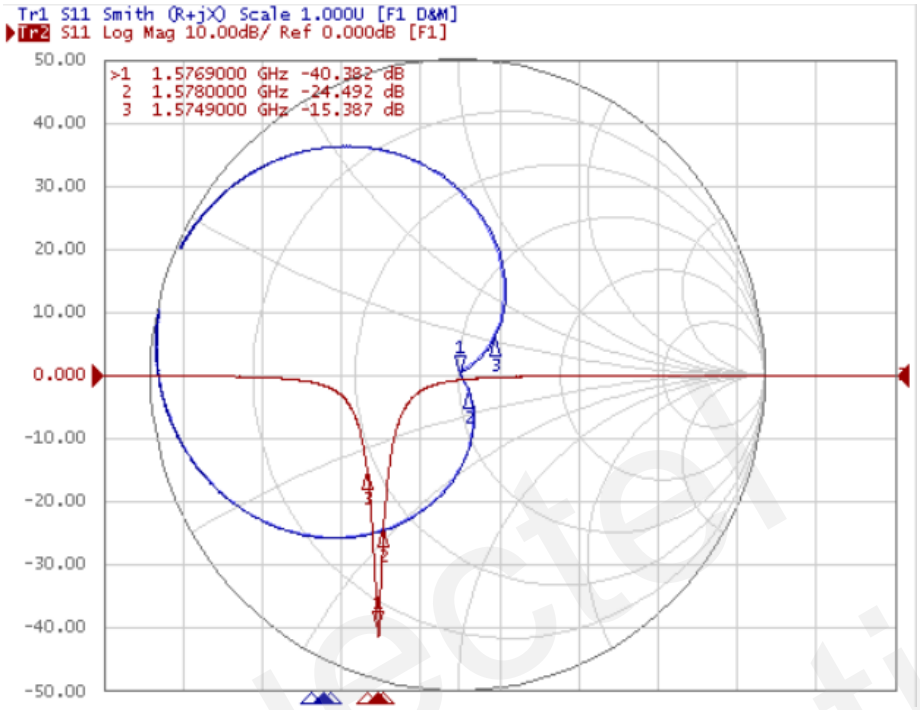


Figure 18: Patch Antenna Test Result with Ground Plane 29.5mm×28.5mm

4.2. PCB Design Guide

Radiation characteristics of antenna depend on various factors, such as the size and shape of the PCB, the dielectric constant of components nearby. For the best performance, it is recommended to follow these rules listed as below.

- Keep at least 10mm distance to the nearest edge of the mother board. It will be better for L50 to be placed in the center of the mother board.
- Keep enough distance between L50 antenna and tall components (h>3mm) and the minimum d is 10mm.
- Put L50 on the top of the device, which can guarantee antenna to face to open sky and achieve good receiving performance during operation.
- Device enclosure should be made of non-mental materials especially around antenna area. The minimum distance between antenna and enclosure is 1mm.

- It is recommended that the mother board is bigger than 80mm×40mm for the better performance. And pour ground copper on the whole mother board

- Other antennas such as BT\WIFI\GSM should be kept minimum 10mm distance far away from the embedded patch antenna in L50.

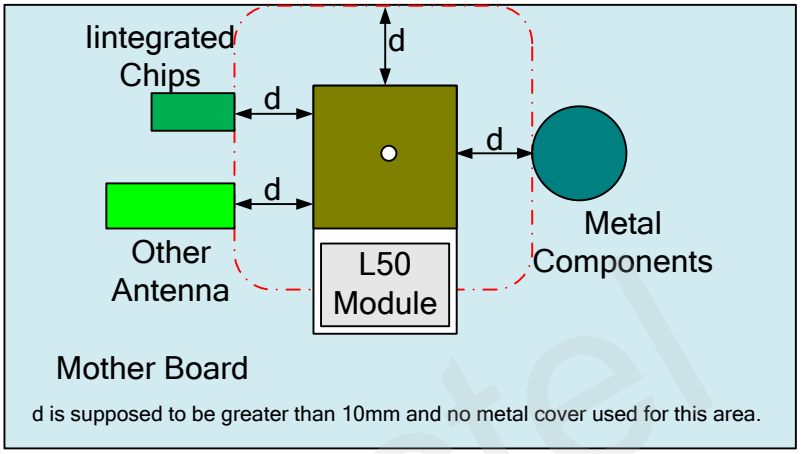


Figure 19: L50 Module Placement Guide

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum rating for power supply and voltage on digital pins of the module are listed in the following table

Table 12: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Power Supply Voltage （VCC）	-0.3	2	V
Backup Battery Voltage (VIO/RTC)	-0.3	2	V
Input Voltage at Digital Pins	-0.5	3.6	V
Storage Temperature Range	-45	125	°C

NOTE

Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. The product is not protected against over voltage or reversed voltage. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes

5.2. Operating Conditions

Table 13: Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VCC	Supply voltage	Voltage must stay within	1.71	1.8	1.89	V

		the min/max values, including voltage drop, ripple, and spikes.				
I_{VCC}	Peak supply current	VCC=1.8V@-148dBm	—	—	60	mA
VIO/RTC	Backup voltage supply		1.71	1.8	1.89	V
$I_{VIO/RTC}$	Backup battery current	VIO/RTC=1.8V in Hibernate mode	—	14	—	uA
T_{OPR}	Normal Operating temperature		-40	25	85	°C

NOTE

Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

5.3. Current Consumption

Table 14: The Module Current Consumption

Parameter	Condition	Min.	Typ.	Max.	Unit
I_{total} Acquisition	Open sky @-130dBm	-	33	-	mA
I_{total} Tracking	Open sky@-130dBm	-	31	-	mA
I_{total} Hibernate	VIO/RTC=VCC=1.8V	-	14	-	uA

NOTE

$I_{total}=I_{VCC}+I_{VIO/RTC}$

5.4. Current Consumption for VIO/RTC Domain

Table 15: Current Consumption for VIO/RTC Domain

Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{VIO/RTC}$	In FULL_ON mode, VCC = 1.8V.		980		uA
	Enter into FULL_ON mode firstly and then turn off VCC.		800		uA
	In Hibernate mode, VCC = 1.8V.		14		uA
	Enter into Hibernate mode firstly and then turn off VCC.		14		uA

5.5. Electro-Static Discharge

L50 module has excellent ESD performance, because every pin is protected by a transient voltage suppressor (TVS). However, ESD protection precautions should still be emphasized. Proper ESD handing and packaging procedures must be applied throughout the processing, handing and operation of any application.

The ESD bearing capability of the module is listed in the following table.

Table 16: The ESD Endurance Table (Temperature: 25°C, Humidity: 45 %)

Pin	Contact discharge	Air discharge
VCC, GND, Patch Antenna	±5KV	±10KV
Others	±4KV	±8KV

5.6. Reliability Test

Table 17: Reliability Test

Test Item	Condition	Standard
Thermal Shock	-30°C...+80°C, 144 cycles	GB/T 2423.22-2002 Test Na IEC 68-2-14 Na
Damp Heat, Cyclic	+55°C; >90% Rh 6 cycles for 144 hours	IEC 68-2-30 Db Test
Vibration Shock	5~20Hz,0.96m^2/s^3;20~500Hz,0.96m^2/s^3-3 dB/oct, 1hour/axis; no function	2423.13-1997 Test Fdb IEC 68-2-36 Fdb Test
Heat Test	85°C, 2 hours, Operational	GB/T 2423.1-2001 Ab IEC 68-2-1 Test
Cold Test	-40°C, 2 hours, Operational	GB/T 2423.1-2001 Ab IEC 68-2-1 Test
Heat Soak	90°C, 72 hours, Non-Operational	GB/T 2423.2-2001 Bb IEC 68-2-2 Test B
Cold Soak	-45°C, 72 hours, Non-Operational	GB/T 2423.1-2001 A IEC 68-2-1 Test

6 Mechanics

This chapter describes the mechanical dimensions of the module.

6.1. Mechanical Dimensions of the Module

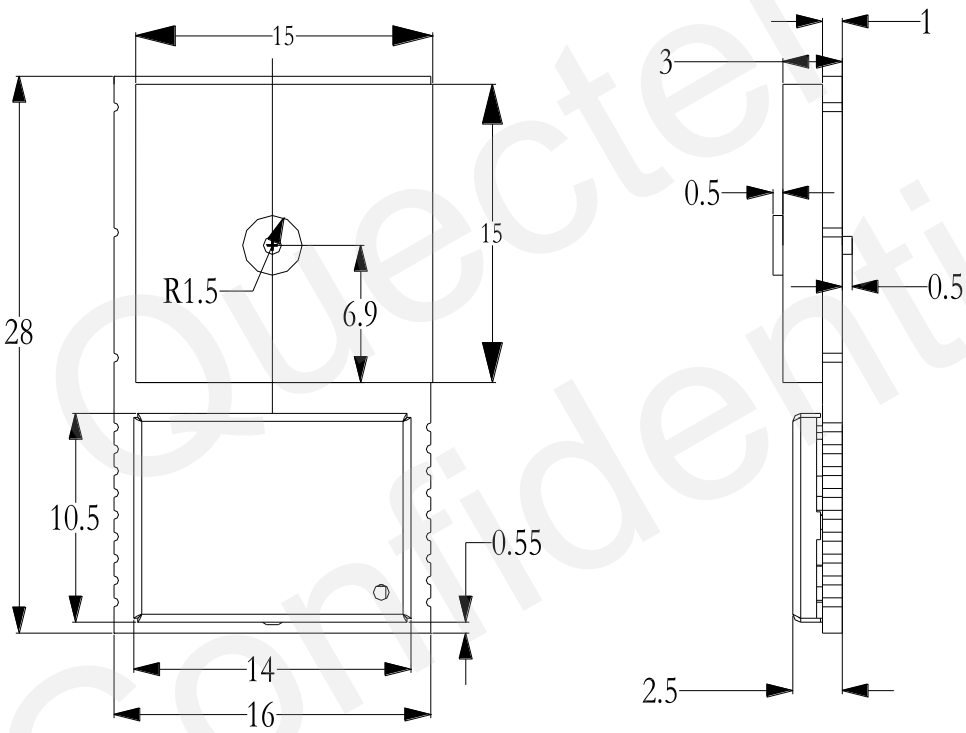


Figure 20: L50 Top View and Side View (Unit: mm)

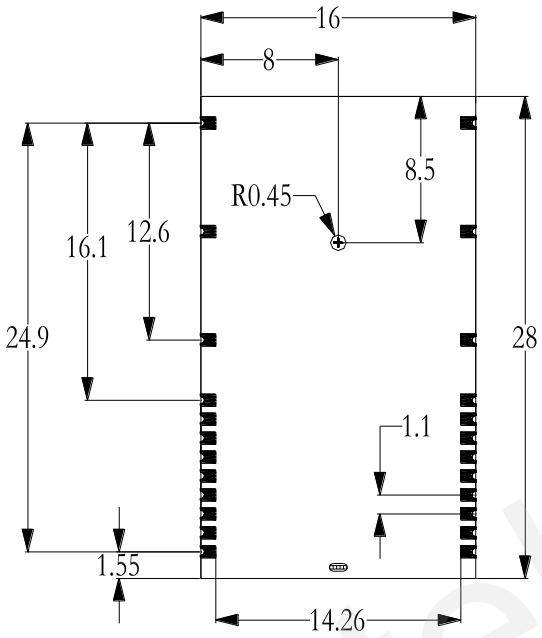


Figure 21: L50 Bottom View (Unit: mm)

6.2. Footprint of Recommendation

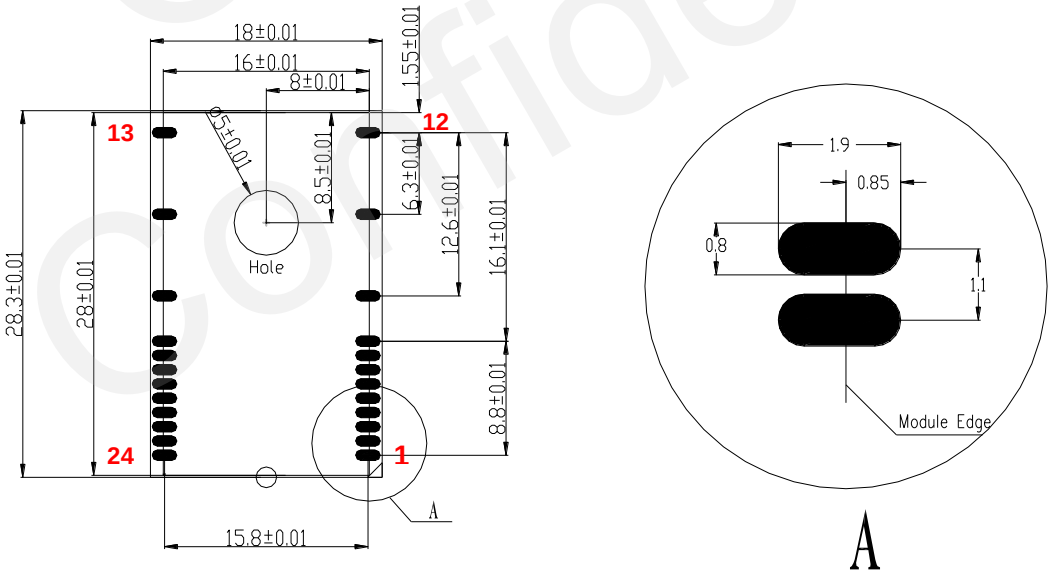


Figure 22: Footprint of Recommendation (Unit: mm)

6.3. Top View of the Module

Figure 23: Top View of Module

6.4. Bottom View of the Module

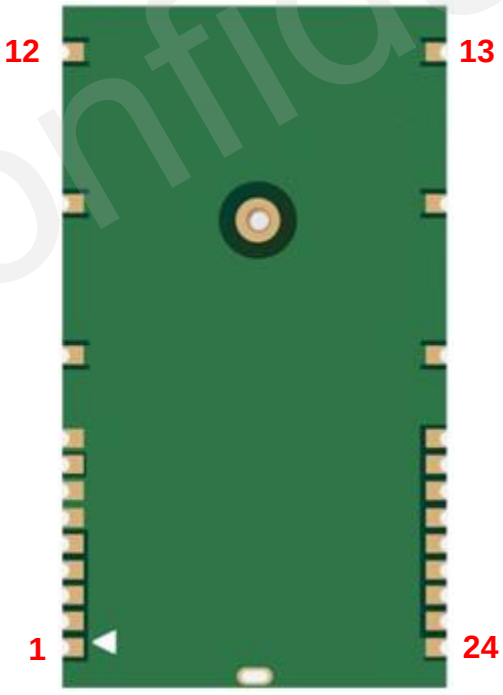


Figure 24: Bottom View of Module

7 Manufacture

7.1. Assembly and Soldering

L50 is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. It is suggested that the minimum height of solder paste stencil is 130um to ensure sufficient solder volume. Pad openings of paste mask can be increased to ensure proper soldering and solder wetting over pads. It is suggested that peak reflow temperature is 235~245ºC (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260ºC. To avoid damage to the module when it is repeatedly heated, it is suggested that the module should be mounted after the first panel has been reflowed. The following picture is the actual diagram which we have operated.

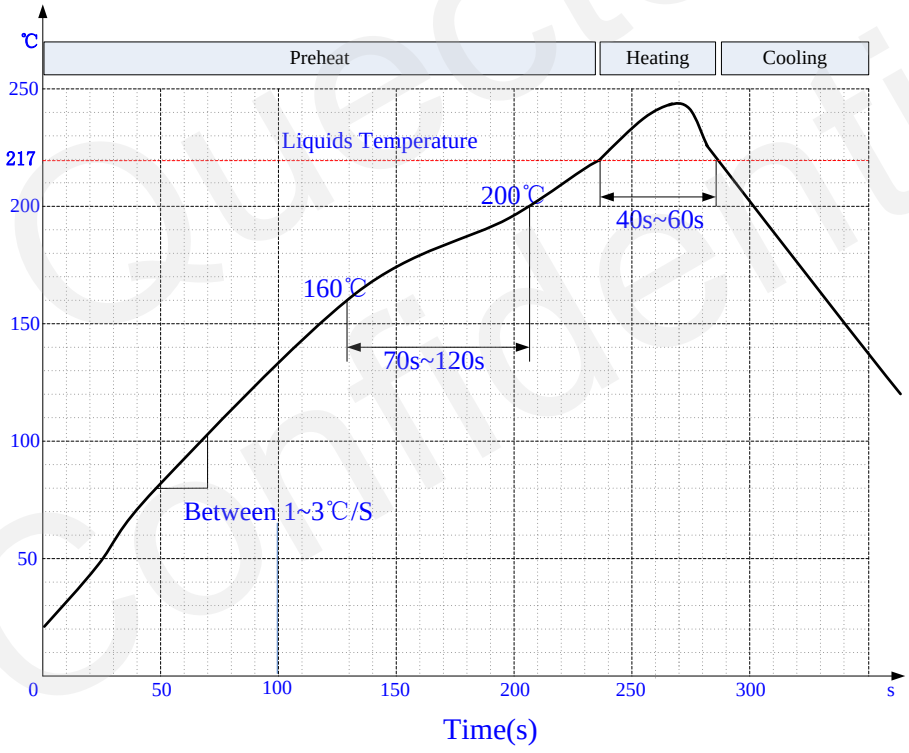


Figure 25: Ramp-soak-spike-reflow of Furnace Temperature

7.2. Moisture Sensitivity

L50 is sensitive to moisture absorption. To prevent L50 from permanent damage during reflow soldering, baking before reflow is required in following cases:

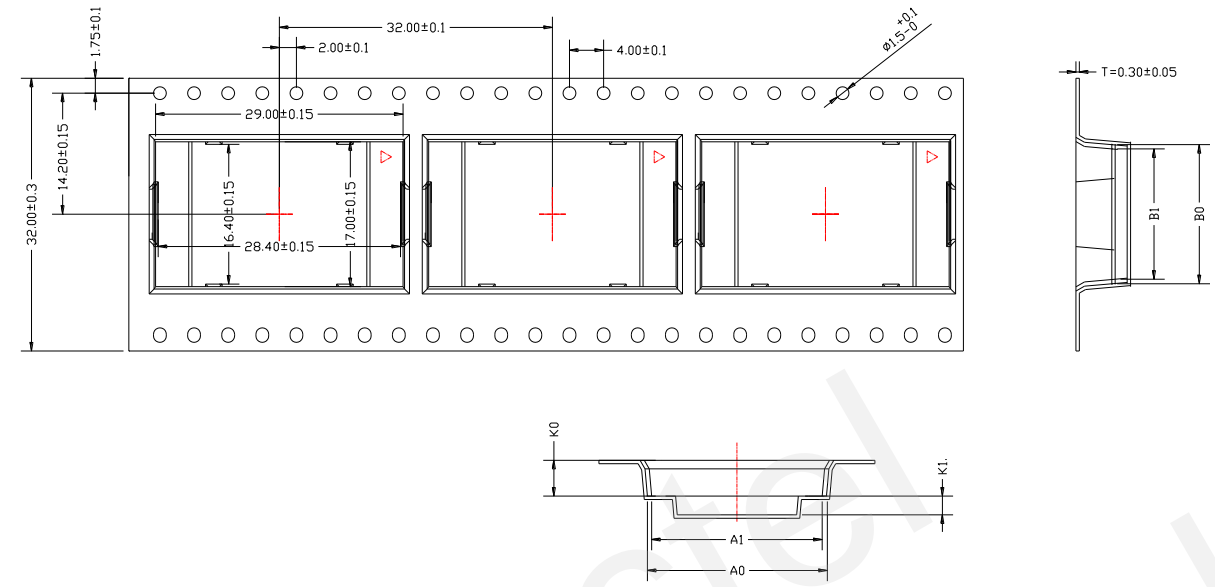
- Humidity indicator card: At least one circular indicator is no longer blue.
- The seal is opened and the module is exposed to excessive humidity.

L50 should be baked for 192 hours at temperature 40℃±5℃/-0℃ and <5% RH in low-temperature containers, or 24 hours at temperature 125℃±5℃ in high-temperature containers. Care should be taken that plastic tape is not heat resistant. L50 should be taken out before pre-heating, otherwise, the tape may be damaged by high temperature heating.

7.3. ESD Safe

L50 module is an ESD sensitive device and should be careful to handle.

7.4. Tape and Reel



ITEM	W	T	A0	A1	B0	B1	B2	K0	K1	P	F	E	D	P0	P2
DIM	32.0	0.30	29.0	28.4	17.0	16.4		4.2	2.0	32.0	14.2	1.75	1.5	4.0	2.0
TOLE	± 0.3	± 0.05	± 0.15	± 0.15	± 0.15	± 0.15	± 0.1	± 0.15	± 0.15	± 0.1	± 0.15	± 0.1	+0.10 −0.00	± 0.1	± 0.1

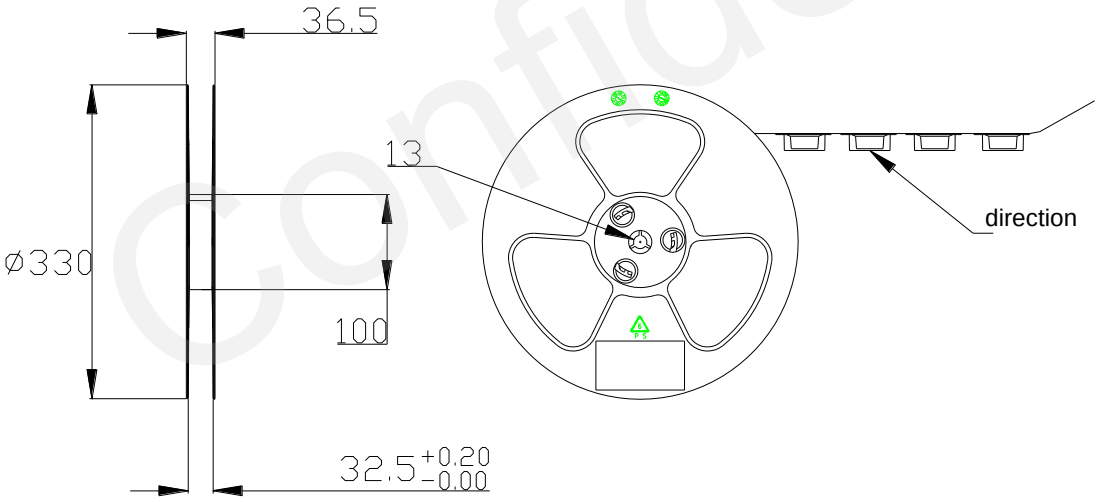


Figure 26: Tape and Reel Specification (Unit: mm)

Table 18: Reel Packing

Model Name	MOQ for MP	Minimum Package: 250pcs	Minimum Package × 4=1000pcs
L50	250pcs	Size: 370×350×56mm N.W: 1.000kg G.W: 1.723kg	Size: 380×250×365mm N.W: 4.000kg G.W: 7.370kg

7.5. Ordering Information

Table 19: Ordering Information

Model Name	Ordering Code
L50 @ROM2.2	L50B-S44

8 Appendix Reference

Table 20: Related Documents

SN	Document Name	Remark
[1]	L50_EVB_User_Guide	L50 EVB User Guide
[2]	L50_GPS_Protocol	L50 GPS Protocol Specification
[3]	SIRF_AGPS_Application_Note	SIRF Platform A-GPS Application Note

Table 21: Terms and Abbreviations

Abbreviation	Description
CGEE	Client Generated Extended Ephemeris
CPU	Center processing unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
EGNOS	European Geostationary Navigation Overlay Service
GPS	Global Positioning System
GNSS	Global Navigation Satellite System
GGA	GPS Fix Data
GLL	Geographic Position – Latitude/Longitude
GSA	GNSS DOP and Active Satellites
GSV	GNSS Satellites in View
HDOP	Horizontal Dilution of Precision
IC	Integrated Circuit

I/O	Input/Output
Kbps	Kilo Bits Per Second
LNA	Low Noise Amplifier
MSAS	Multi-Functional Satellite Augmentation System
NMEA	National Marine Electronics Association
OSP	One Socket Protocol
PDOP	Position Dilution of Precision
RMC	Recommended Minimum Specific GNSS Data
SBAS	Satellite-based Augmentation System
SUPL	Secure User Plane Location
SAW	Surface Acoustic Wave
TBD	To Be Determined
TTFF	Time-To-First-Fix
UART	Universal Asynchronous Receiver & Transmitter
VDOP	Vertical Dilution of Precision
VTG	Course over Ground and Ground Speed, Horizontal Course and Horizontal Velocity
WAAS	Wide Area Augmentation System
ZDA	Time & Date
Inorm	Normal Current
Imax	Maximum Load Current
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value

VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value