L20 Hardware Design

GPS Module Series

Rev. L20_Hardware_Design_V2.2

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About the Document

History

Revision	Date	Author	Description
1.0	2010-12-03	Crystal HE/ David WEI	Initial
1.1	2012-04-15	Crystal HE	1. Modified Figure 6, 9, 10, 11, 16. 2. Added description of hibernate mode in Chapter 3.3.3. 3. Added description of AGPS in chapter 3.5. 4. Modified data I_{VCC} and I_{BCKP} in Table 13. 5. Modified data, I_{VCC} tracking, I_{VCC} acquisition and I_{VCC} hibernate in Table 14. 6. Added Chapter 7 Manufacturing. 7. Modified recommended battery for V_BCKP. 8. Modified the accuracy of 1PPS signal. 9. Added the current consumption of V_BCKP
1.2	2012-10-26	King HAO	1. Modified time sequence of switching between full on and hibernate mode. 2. Modified RS-232 level shift circuit. 3. Modified reference design for L20 module. 4. Modified the Reel and Tapes of L20 module.
2.1	2013-01-22	Ray XU	1. Restructure the contents of Chapter 3.3. ● Added Chapter 3.3.3: Power Saving Mode. ● Added Chapter 3.3.3.2: ATP Mode. ● Added Chapter 3.3.3.3: PTF Mode. 2. Modified Figure 1: Module Functional Diagram. 3. Modified the description of Chapter 7.3 and added Table 18. 4. Added chapter 7.4：Ordering information. 5. Added new features based on ROM2.2 firmware. ● Added Chapter 3.6: Hardware Baud Rate Configuration. ● Added Chapter 3.7: Fast Time-sync.

			● Modified the current consumption in tracking, acquisition and backup mode. ● Modified max update rate. ● Modified Figure 10: L20 Reference Design.
2.2	2014-06-11	Tony GAO	1. Modified the input power at RFIN. 2. Updated packaging information.

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1 Introduction

This document defines and specifies the L20 GPS module. It describes L20 hardware interface and its external application reference circuits, mechanical size and air interface.

This document can help you quickly understand module interface specifications, electrical and mechanical details. We also offer you other documents such as L20 software application notes and user guider. These documents can ensure you use L20 module to design and set up mobile applications quickly.

2 Product Concept

2.1. General Description

L20 GPS ROM-based module features fast acquisition and tracking with the latest SiRF Star IV ROM 2.2 technology. This module provides outstanding GPS performance in a compact form factor. Equipped with an external optional EEPROM which provides capability for storing ephemeris and patch codes downloaded through UART, L20 can support either Standalone or A-GPS (CGEE function). Advanced jamming suppression mechanism and innovative RF architecture ensures a high level of immunity for jamming and maximum GPS performance. The module supports location, navigation and industrial applications including autonomous GPS C/A, SBAS (WAAS, EGNOS and QZSS), and A-GPS.

L20 is an SMD type module with the compact form factor 16mm × 12.2mm × 2.4 mm, which can be embedded in your applications through the 24-pin pads. It provides all hardware interfaces between the module and host board.

The module is fully ROHS compliant to EU regulation.

2.2. Key Features

Table 1: Module key Features

Feature	Implementation
Power Supply	● Single supply voltage: 2.0V~3.6V typical: 3.0V
Power Consumption	● Acquisition: 39mA ● Tracking: 36mA
Receiver Type	● GPS L1 1575.42MHz C/A Code ● 48 search channels
Sensitivity	● Cold start (Autonomous): -148dBm ● Reacquisition: -160dBm ● Tracking: -163dBm
Time-To-First-Fix	● Cold start (Autonomous): <35s ● Warm start (Autonomous): <35s ● Hot start (Autonomous): <1s

Horizontal Position Accuracy	●	<2.5 m CEP
Max Update Rate	●	5Hz
Accuracy of 1PPS Signal	●	Typical accuracy: 500ns
	●	Time pulse width: 200ms
Velocity Accuracy	●	Without aid: 0.01m/s
Acceleration Accuracy	●	Without aid: 0.1m/s²
Dynamic Performance	●	Maximum altitude: <18288m
	●	Maximum velocity: 514m/s Maximum
	●	Acceleration: 4G
I2C Interface	●	Open drain output
	●	Operate up to 400Kbps
UART Port	●	UART Port: two lines TXD1 and RXD1
	●	Baud rate configured by Hardware.
	●	Used for NMEA or OSP messages output/input
Temperature Range	●	Normal operation: -40°C ~ +85°C
	●	Storage temperature: -45°C ~ +125°C
Physical Characteristics	●	Size: 16±0.15 × 12.2±0.15 × 2.4±0.1mm
	●	Weight: about 1.0 g

2.3. Function Diagram

The following is the block diagram of L20 module. It consists of single chip GPS IC which includes RF part and Base-band part, LNA and SAW filter.

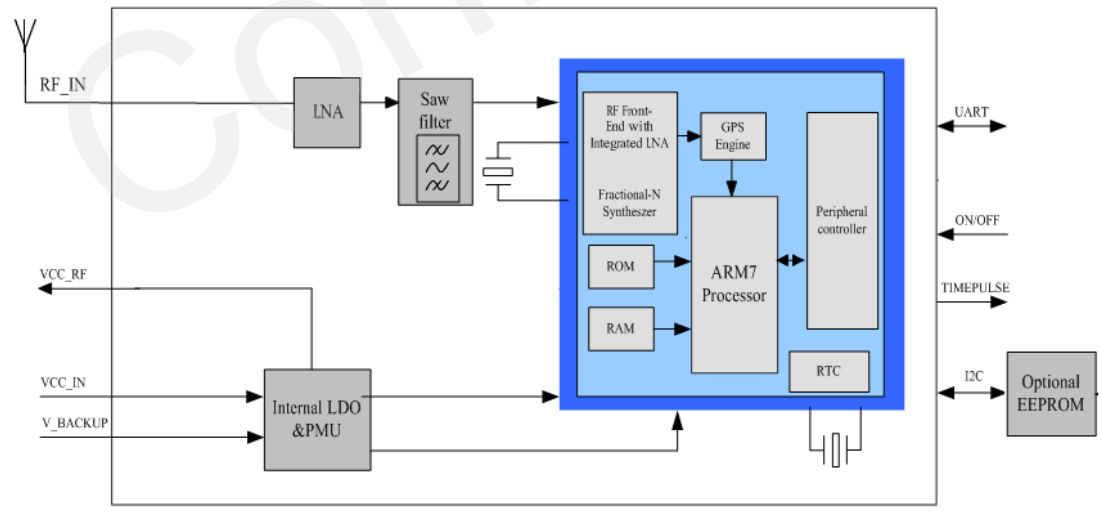

Figure 1: Module Functional Diagram

2.4. Evaluation Board

In order to help you to develop applications with L20 module, Quectel supplies an Evaluation Board (EVB) with appropriate power supply, RS-232 serial cable and active antenna.

For more details, please refer to ***the document [1]***.

2.5. Protocol

The module supports standard NMEA-0183 protocol and the One Socket Protocol, OSP, which is the binary protocol interface that enables the host processor of your device to access all SiRF GPS chip products of the SiRF Star IV family and beyond. The module is capable of supporting the following NMEA formats: ***GGA, GSA, GLL, GSV, RMC, and VTG***.

Table 2: The Module Supported Protocols

Protocol	Type
NMEA	Output, ASCII, 0183, 3.01
OSP	Input/output, OSP protocol

NOTE

Please refer to ***document [2]*** about ***NMEA*** standard protocol and ***SiRF*** private protocol.

3 Application

The module is equipped with a 24-pin 1.1mm pitch SMT pad that connects to host application platform. Sub-interfaces included in these pads are described in details in the following chapters.

- Power management *(refer to Section 3.3)*
- UART interface *(refer to Section 3.4.1)*
- I2C interface (*refer to Section 3.4.2*)

Electrical and mechanical characteristics of the SMT pad are specified in ***chapter 5 & chapter 6***.

3.1. Pin Description

Table 3: Pin Description

Power Supply				
Pin Name	I/O	Description	DC Characteristics	Comment
VCC	I	Supply voltage	Vmax=3.6V Vmin=2.0V Vnom=3.0V	Supply current of no less than 100mA.
V_BCKP	I	Backup power supply	Vmax=3.6V Vmin=2.0V Vnom=3.0V I_{BCKP}=33uA @Hibernate mode, VCC=3.0V	Power supply for RTC when VCC is not applied for the system.
VCC_RF	O	Output voltage RF section	Vmax=3.6V Vmin=2.0V Vnom=3.0V Imax=50mA	Usually supply power for external active antenna, if the supply voltage is suitable for that active antenna. VCC_RF=VCC. If unused, keep this pin open.
General Purpose Input/Output				
Pin Name	I/O	Description	DC Characteristics	Comment
ON_OFF	I	Power control pin	VILmin=-0.4V VILmax=0.45V	Applying a pulse which consists of a low level that persists for at least

			VIHmin=0.7×VCC VIHmax=3.6V	1ms and a rising edge onto the ON_OFF pin can switch operating mode between hibernate and full-on. If unused, keep this pin open.
TIMEPULSE	O	Time pulse	VOLmin=-0.3V VOLmax=0.4V VOHmin=0.75×VCC	1 pulse per second (1PPS). Synchronized at rising edge, pulse width 200ms. If unused, keep this pin open.
Serial Interface				
Pin Name	I/O	Description	DC Characteristics	Comment
SDA2	I/O	● Serial data Input/output ● Baud rate configuration pin	VOLmax=0.4V VOHmin=0.75×VCC VILmin=-0.4V VILmax=0.45V VIHmin=0.7×VCC VIHmax=3.6V	
SCL2	O	● Serial clock output ● Baud rate configuration pin	VOLmax=0.4V VOHmin=0.75×VCC	
RXD1	I	Receive data	VILmin=-0.4V VILmax=0.45V VIHmin=0.7×VCC VIHmax=3.6V	
TXD1	O	Transmit data	VOLmax=0.4V VOHmin=0.75×VCC	
RF Interface				
Pin Name	I/O	Description	DC Characteristics	Comment
RFIN	I	GPS signal input	Impedance of 50Ω	Refer to ***chapter 4***

3.2. Operating Modes

The table below briefly summarizes the various operating modes in the following chapters.

Table 4: Overview of Operating Modes

Mode		Function
Full on Mode	Acquisition mode	The module starts to search satellite, determine visible satellites and coarse carrier frequency and code phase of satellite signals. When the acquisition is done, it switches to tracking mode automatically.
	Tracking mode	The module refines acquisition's message, as well as keeps tracking and demodulating the navigation data from the specific satellites.
Hibernate Mode		Hibernate mode means a low power state where only the internal I/O keeps Alive, non-volatile RTC, patch RAM and backup RAM block is powered on. Other internal blocks like digital baseband and RF are internally powered off

3.3. Power Management

There are two power supply pins, VCC and V_BCKP.

3.3.1. VCC - Main Power

The main power supply is fed through the VCC pin. During operation, the current drawn by L20 GPS module can vary by some orders of magnitude. It is important that the power supply is able to support the peak current. For this reason, the power supply must be able to provide sufficient current up to 100mA.

An LDO (Low Dropout Regulator) device is recommended for VCC.

3.3.2. V_BCKP - Backup Battery

The RTC (Real Time Clock) power supply of module can be directly provided by an external capacitor or battery (rechargeable or non-chargeable) through the V_BCKP pin, in order to achieve a better Time to First Fix (TTFF) after a power down. It can supply power for backed-up memory which contains all the necessary GPS information for quick start-up and a small amount of user configuration variables.

NOTE

The V_BCKP pin should be connected to a battery or a capacitor for GPS module hot start.

Table 5: Pin Definition of the V_BCKP Pin

Name	Pin	Function
V_BCKP	22	Backup voltage supply

Please refer to the following figure for RTC backup:

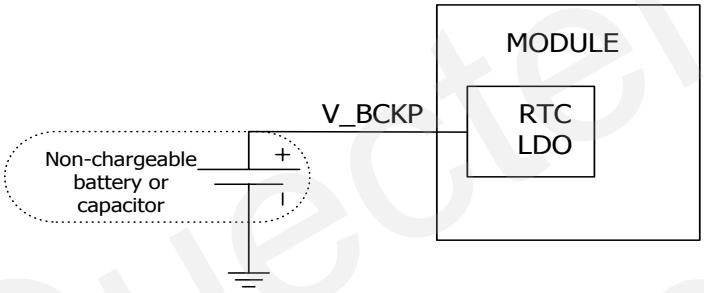

Figure 2: RTC Supply from Non-chargeable Battery or Capacitor

The V_BCKP pin does not implement charging for rechargeable battery. It is necessary to add a charging circuitry for rechargeable battery. It is shown as the following figure:

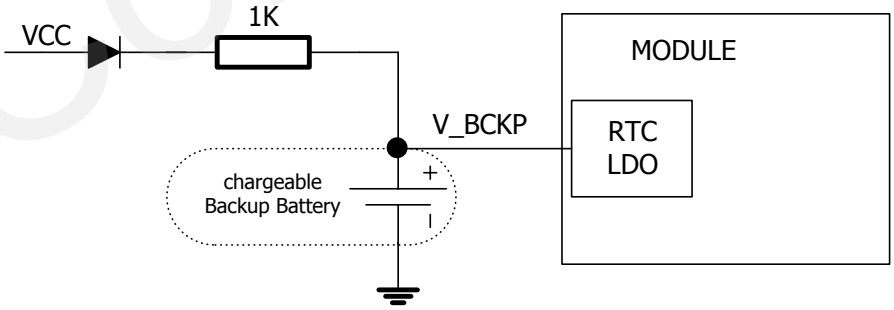

Figure 3: Reference Charging Circuit for Chargeable Battery

Coin-type Rechargeable Capacitor such as MS920SE from Seiko can be used and Schottky diode such as RB520S30T1G from ON Semiconductor is recommended to be used here for its low voltage drop.

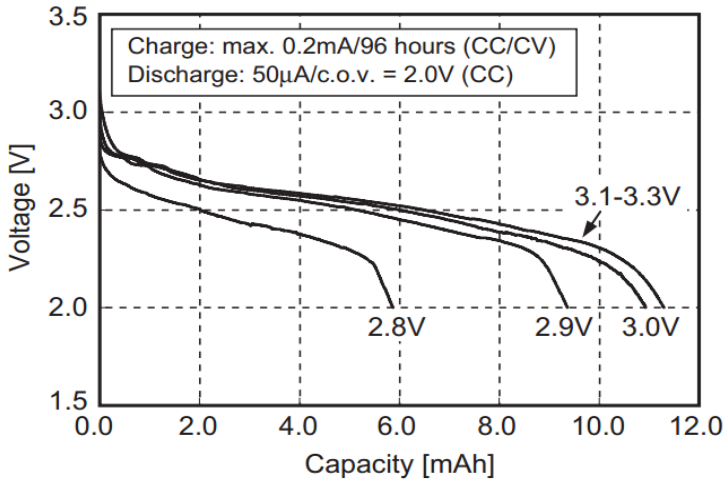

Figure 4: Seiko MS920SE Charge and Discharge Characteristics

3.3.3. Power Saving Mode

3.3.3.1. Hibernate Mode

Hibernate mode means low consumption in this mode. Some power internal domains are powered off such as ARM, DSP and RF part, but the RTC domain including all non-volatile logic, the RAM, and GPS BB logic I/O is still active. The module is waked up from Hibernate mode on the next ON_OFF (at rising edge) using all internal aided information like GPS time, Ephemeris, Last Position and so on, to carry out a fast TTFF in either Cold or Warm start mode.

The following picture is the reference time sequence. Here two low pulses on ON/OFF pin come from the external button or your device. L20 module can enter full on mode automatically when power on due to there is an ON/OFF control circuit in it.

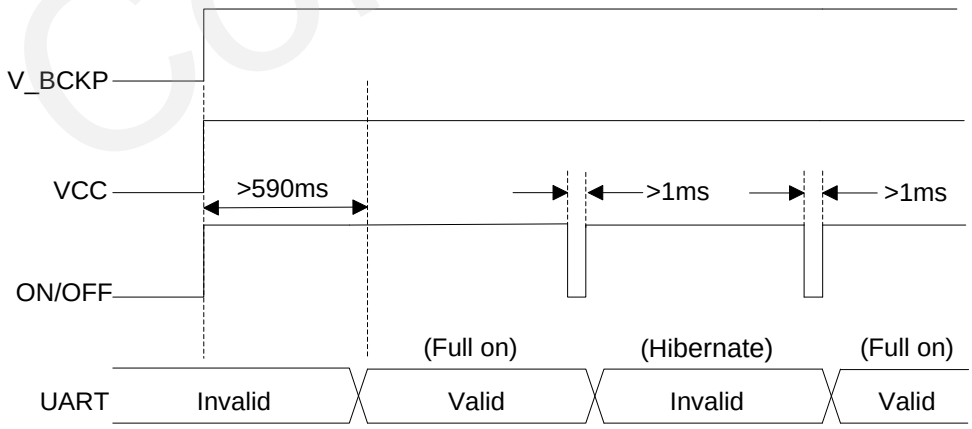

Figure 5: Time Sequence of Switching between Full on &Hibernate

3.3.3.2. ATP Mode

Adaptive trickle power (ATP): In this mode, L20 cycles three modes internally to optimize power consumption. This three modes consist of full on mode, CPU only mode and standby mode. The full on mode lasts about 200~900ms to require new ephemeris to get a valid position, and the other two modes mean that DSP and RF are partially power off or completely power off to decrease consumption. The timing sequence is shown in following figure. This mode is configurable with SiRF binary protocol message ID151. The following diagram is a default configuration and it is tested in the strong signal environment. When the signal becomes weak, it will not comply with the following rule. The weaker the signal is, the longer time the module lasts in full on mode. In the extreme condition, when there is no signal input, the mode cycles only two modes including full on and standby mode.

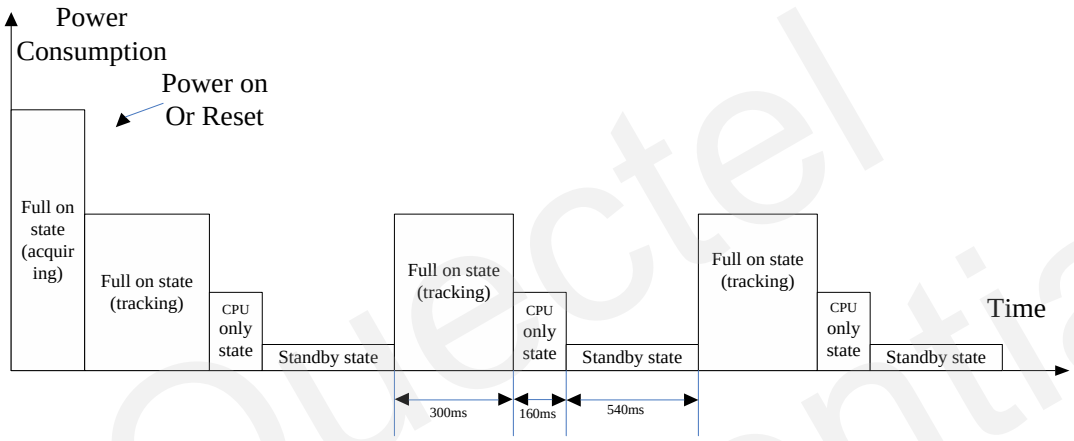

Figure 6: ATP Timing

Example:
GPS signal generator provides-130dBm GPS signal.
Send command “A0A20009 97000000C8000000C8 0227B0B3” to set module the following parameters and enter into Adaptive Trickle Power mode:

- Update frequency: 1 Hz
- On-time: 200 ms

The average current in Adaptive Trickle Power mode is about 16 mA.

3.3.3.3. PTF Mode

Push to fix (PTF): In this mode, L20 is configured to be waked up periodically, typically every 1800 sec (configurable range 10… 7200 sec) for updating position and collecting new ephemeris data from valid satellites. For the rest of the time, the module stays in Hibernate mode. A position request acts as a wakeup of the module, which is then able to supply a position within the hot-start time specification.This mode is configurable with SiRF binary protocol message ID167 and ID151. The following figure is the default configuration. Additionally, when the signal becomes weak, push to fix function is not valid.

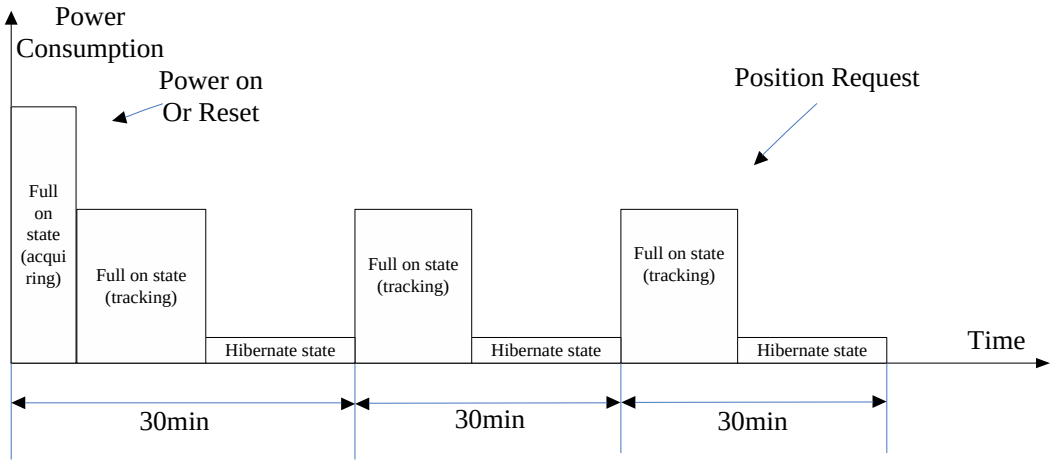

Figure 7: PTF Timing

Example:
GPS signal generator provides-130dBm GPS signal.
Send command "A0A2000FA7000075300001D4C00000003C0000 031DB0B3" to set L20 module the following parameters:

- Maximum time for sleep mode: 30 seconds
- Max. Satellite search time: 120 seconds
- Cycle time: 60 seconds

Send command "A0A20009 97000100C8000000C8 0227B0B3" to enter Push-to-Fix mode
The average current in Push-to-Fix mode is about 9 mA.

3.4. Communication Interface

L20 module uses UART interface to output NMEA messages or to communicate with the host processor via the OSP protocol.

3.4.1. UART Interface

The module provides one universal asynchronous receiver & transmitter serial port. The module is designed as a DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection. The module and the client (DTE) are connected through the following signal (shown as following figure). It supports data baud-rate from 4800bps to 115200bps.

UART interface:

- TXD1: Send data to the RXD signal line of DTE
- RXD1: Receive data from the TXD signal line of DTE

Table 6: Pin Definition of the UART Interfaces

Interface	Name	Pin	Function
UART Interface	TXD1	20	Transmit data
	RXD1	21	Receive data

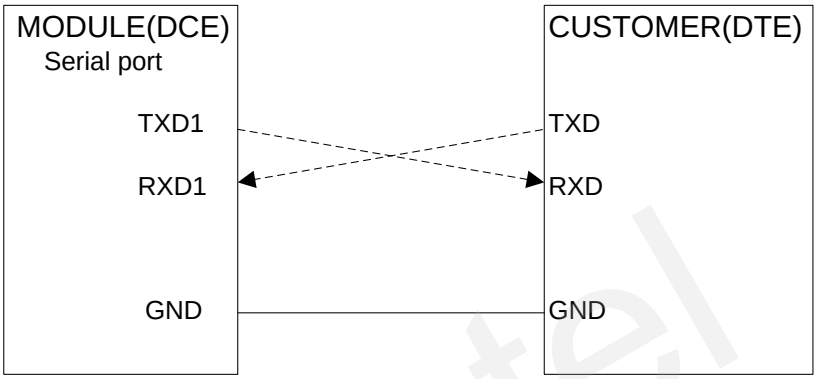

Figure 8: Connection of UART Interface

This UART interface has the following features:

- The UART interface can be used to output NMEA and input & output OSP messages.
  The default output NMEA type setting is **RMC, GGA, GSA, and GSV** (after successful positioning).
- The UART interface supports the following data rates:
  4800, 9600, 19200, 38400, 57600, 115200.
  The default setting is 4800bps, 8 bits, no parity bit, 1 stop bit, no hardware flow control.
- Hardware flow control and synchronous operation are not supported.

The UART interface does not support the RS-232 level. It supports only the CMOS level. If the module UART interface is connected to the UART port of a computer, it is necessary to insert a level shift circuit between the module and the computer. Please refer to the following figure.

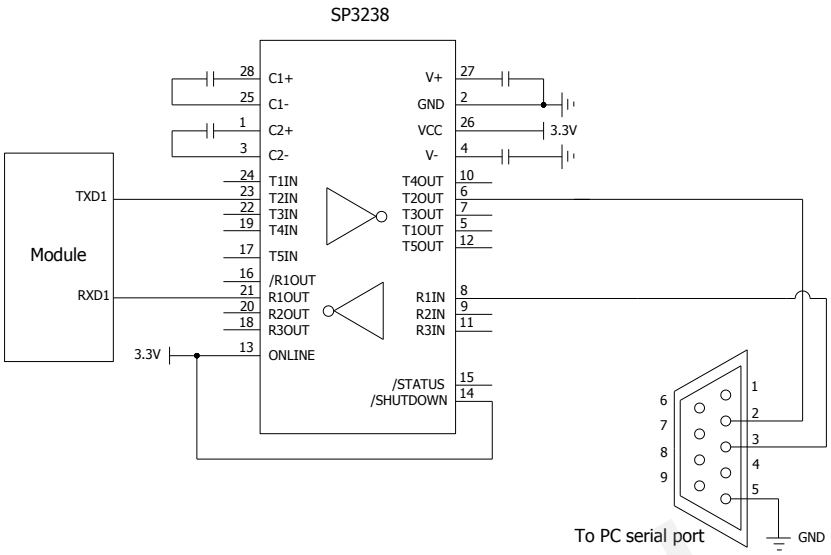

Figure 9: RS-232 Level Shift Circuit

3.4.2. I2C Interface

L20 provides an I2C interface which can operate up to 400kbps to access an EEPROM where EE (extended ephemeris) data and updated patch code are stored. These two pins are pulled up to VCC internally.

Table 7: Pin Definition of the I2C Interfaces

Interface	Name	Pin	Function
I2C Interface	SDA2	18	Serial data output/input
	SCL2	19	Serial clock output

3.5. Assisted GPS

By supplying aided information like ephemeris, almanac, rough last position, time and satellite status, A-GPS can help improving TTFF of the GPS receiver.

L20 supports one kind of A-GPS called Client Generated Extended Ephemeris (CGEE) which ensures fast TTFF for 3 days.

The CGEE data is generated internally from satellite ephemeris.The CGEE feature requires that V_BCKP power supply is kept active all the time and an external 1Mbit EEPROM connected to I2C bus for CGEE

data storage. The recommended EEPROM is in the following table and it is verified.

Table 8: Recommended EEPROM

Manufacturer	Part Number
ST	M24M01
Seiko Instruments Inc.	S-24CM01C
Atmel	AT24C1024B

NOTE

The part number recommended is part number series. Please get more details from the datasheet such as operation voltage and package.

For more details, please refer to ***document [3].***

3.6. Hardware Baud Rate Configuration

Excluding I2C interface, SDA2, SCL2 pins can also be used as the baud rate configuration pins of UART, but these two functions cannot be used simultaneously. Note that these two pins have been pulled high internally to VCC in the module. So you can just pull 200ohm resistor to ground to have a pull low action and let the pin floating to have a pull high action. Pay attention that: hardware baud rate configuration should be done before starting the module, or it is not available.

This baud rate configuration is not available if any EEPROM is attached to these two pins. The default baud rate is NMEA 4800 when an EEPROM device is attached, but can be changed via OSP message, for more details, please refer to ***the document [2].***

The following table shows the baud rate configuration list. As SDA2, SCL2 pins have been pulled high internally to VCC. The default setting of UART1 is NMEA in 4800bps if these two pins are floating. Note that the function described in this chapter is based on ROM2.2 firmware.

Table 9: Baud Rate Configuration

SDA2	SCL2	Protocol	Baud rate
Floating	Floating	NMEA	4800

Floating	Pull low	NMEA	9600
Pull Low	Floating	NMEA	38400

3.7. Fast Time-sync

L20 provides Fast time-sync function for special application to reduce power consumption. These special applications include watches and clocks for UTC time. It uses technique that limits how many message the satellite navigation must be observed before it declares the correct time. Due to this technique, the module will find the time very quickly compared to normal operation. It is about 6 seconds to get the UTC time in the condition of one visible satellite with C/N value bigger than 23 in static states. You can turn off the module immediately once the UTC time is got to save power consumption. This function is disabled by default and it can be enabled by OSP Message ID 136, for more details, please refer to ***the document [2].***

3.8. Reference Design

The following figure is a reference design with L20 module.

The module will directly start when VCC is applied and it will automatically output NMEA messages.

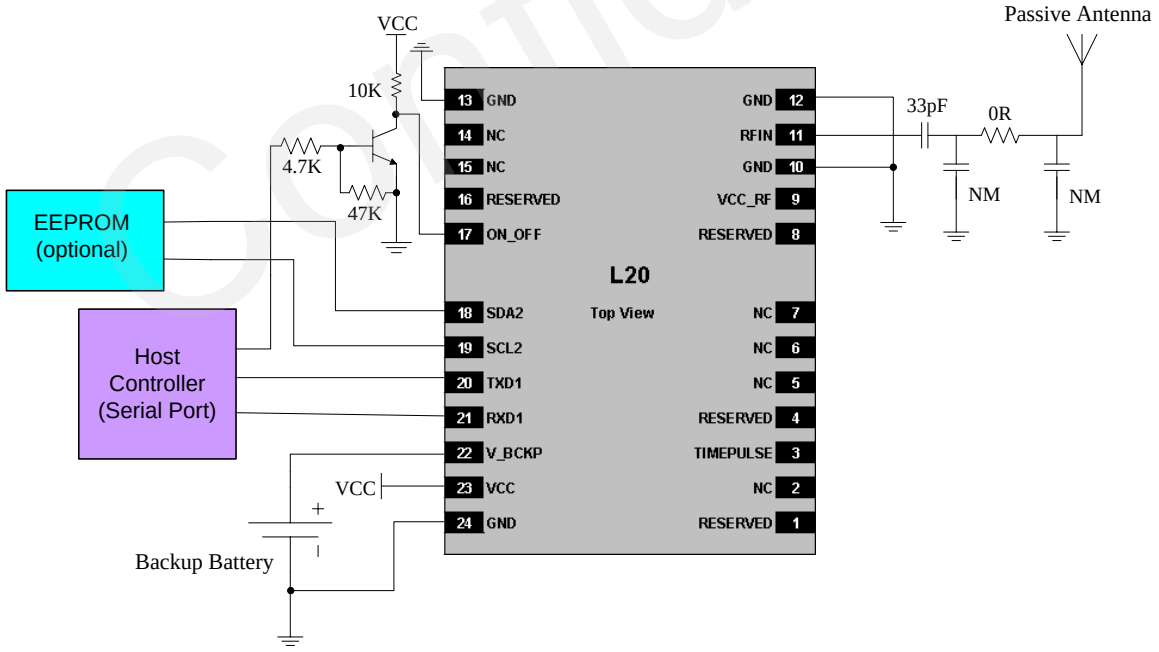

Figure 10: Reference Design for L20 Module

4 Antenna Interface

L20 module receives L1 band signal from GPS satellites at a nominal frequency of 1575.42MHz. The RF signal is connected to the RFIN pin. The input impedance of RFIN is 50Ω.

4.1. Antenna

L20 module can be connected to passive or active antenna.

Table 10: Recommended Antenna Specification

Antenna Type	Specification
Passive Antenna	Center frequency: 1575.42MHz Band width: >20MHz Gain: >0dBi Polarization: RHCP or Linear
Active Antenna	Center frequency: 1575.42MHz Band width: >5MHz Minimum gain: 15-20dBi (compensate signal loss in RF cable) Maximum noise figure: 1.5dB Maximum gain: 50dBi Polarization: RHCP or Linear

4.2. Antenna Supply

4.2.1. Passive Antenna

Passive antenna which does not require a DC bias voltage can be connected to RFIN pin directly. VCC_RF can be left open. It is always beneficial to reserve a passive matching network between the antenna and the RFIN port of the module. The following figure is the reference design.

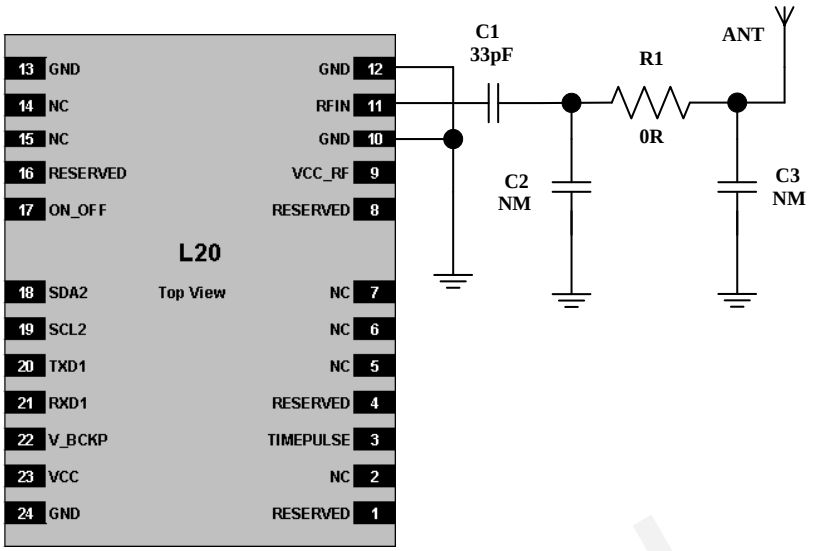

Figure 11: Reference design for passive antenna

4.2.2. Active Antenna

Active antenna, carrying an integrated low-noise amplifier, could be connected to RFIN directly. If an active antenna is connected to RFIN, the integrated low-noise amplifier of the antenna must be powered by a correct supply voltage. Usually, the supply voltage is fed to the antenna through the coaxial RF cable. An active antenna consumes current at 5~20mA. The inductor outside the module prevents the RF signal from leaking into the VCC_RF pin and routes the bias supply to the active antenna.

The reference design of the supply part for active antenna is shown in the figure below.

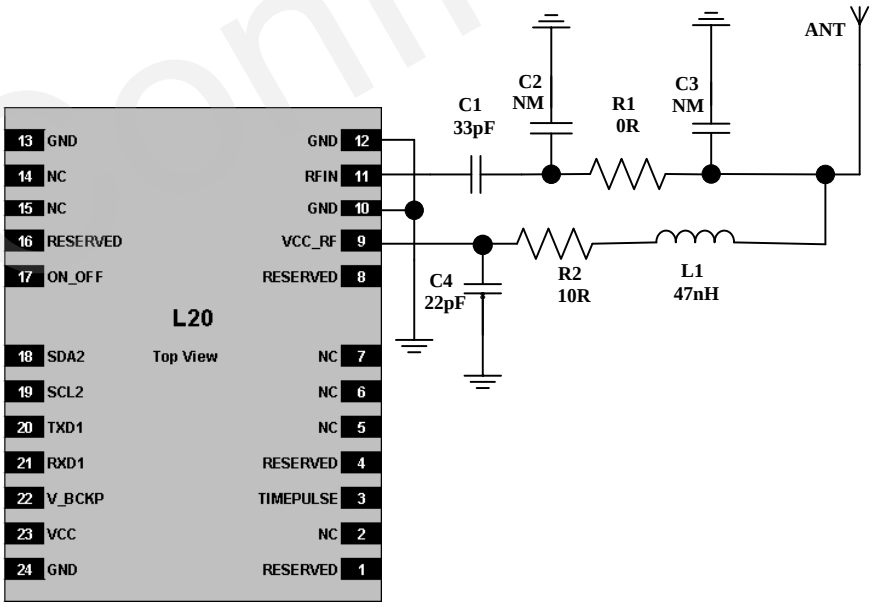

Figure 12: Reference Design for Active Antenna with VCC_RF

The voltage of VCC_RF, which is the same as VCC, might not be suitable for the external active antenna. In this case, an external power supply should be applied. Please refer to the reference circuit shown in the following figure.

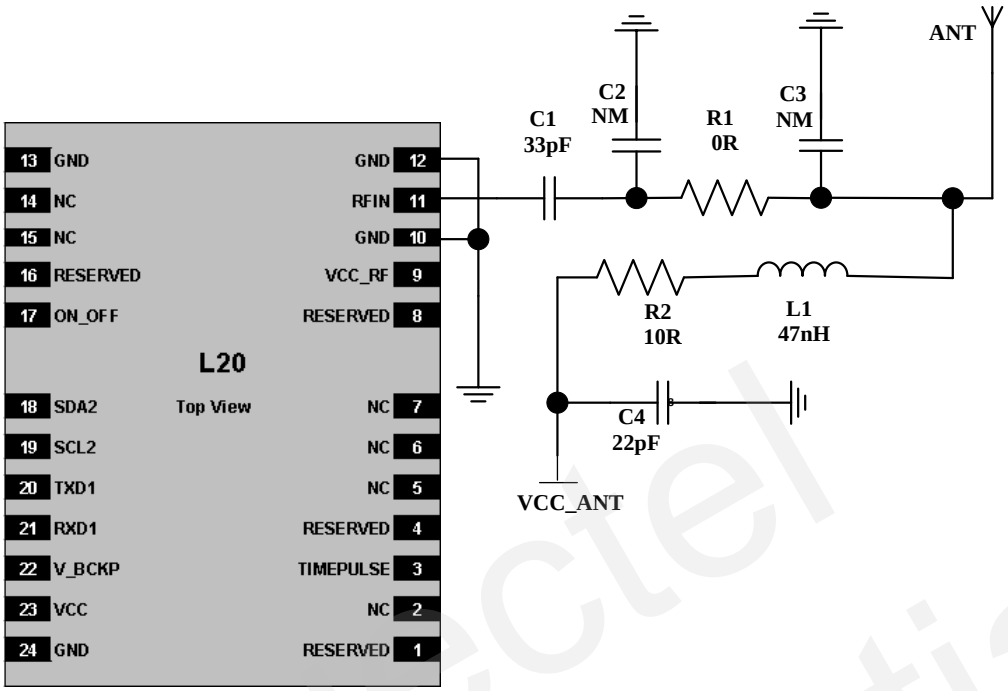

Figure 13: Reference Design for Active Antenna with External Power

NOTE

The rated power of resistor R2 should be chosen no less than 1 watt in case active antenna is shorted unexpectedly.

5 Electrical, Reliability and Radio Characteristics

5.1. Pin Assignment of the Module

Figure 14: Pin Assignment

Table 11: L20 Pin Assignment

PIN No.	PIN Name	I/O	PIN No.	PIN Name	I/O
1	RESERVED		24	GND	
2	NC		23	VCC	I
3	TIMEPULSE	O	22	V_BCKP	I
4	RESERVED		21	RXD1	I
5	NC		20	TXD1	O
6	NC		19	SCL2	O

7	NC		18	SDA2	I/O
8	RESERVED		17	ON_OFF	I
9	VCC_RF	O	16	RESERVED	
10	GND		15	NC	
11	RFIN	I	14	NC	
12	GND		13	GND	

5.2. Absolute Maximum Ratings

Absolute maximum rating for power supply and voltage on digital pins of the module are listed in the following table.

Table 12: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Power Supply Voltage（VCC）	-0.3	6	V
Backup Battery Voltage (V_BCKP)	-0.3	6	V
Input Voltage at Digital Pins	-0.5	3.6	V
	-0.5	3.6	
VCC_RF Output Current (Ivccrf)	—	100	mA
Input Power at RFIN (Prfin)	—	15	dBm
Storage Temperature	-45	125	°C

NOTE

Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. The product is not protected against over voltage or reversed voltage. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

5.3. Operating Conditions

Table 13: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VCC	Supply voltage	Voltage must stay within the min/max values, including voltage drop, ripple, and spikes.	2.0	3.0	3.6	V
I_{VCC}	Peak supply current	VCC=3.3V @-148dBm			65	mA
V_BCKP	Backup voltage supply		2.0	3.0	3.6	V
I_{BCKP}	Backup battery current	V_BCKP=3.0V, VCC=3.0V, in Hibernate mode		33		uA
VCC_RF	Output voltage RF section				VCC	V
I_{VCC_RF}	VCC_RF output				50	mA
TOPR	Normal Operating temperature		-40	25	85	℃

NOTES

1. This figure can be used to determine the maximum current capability of power supply.
2. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

5.4. Current Consumption

The values for current consumption are shown in following table.

Table 14: The Module Current Consumption

Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{VCC} @Acquisition	@-130dBm		39		mA

I_{VCC} @Tracking	@-130dBm (For Cold start, 10 minutes after First Fix. For Hot Start, 15 seconds after First Fix.)	36	mA
I_{VCC} @ Hibernate	VCC=3.0V,V_BCKP=3.0V	7	mA

5.5. Current Consumption for V_BCKP

Table 15: Current Consumption for V_BCKP

Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{BCKP}	In FULL_ON mode, VCC=3.0V.		550		uA
	Enter into FULL_ON mode first and then turn off VCC.		770		uA
	In Hibernate mode, VCC=3.0V.		33		uA
	Enter into Hibernate mode first and then turn off VCC.		165		uA

5.6. Electro-static Discharge

Although the module is fully protected against ESD strike, ESD protection precautions should still be emphasized. Proper ESD handing and packaging procedures must be applied throughout the processing, handing and operation of any application.

The ESD bearing capability of the module is listed in following table.

Table 16: The ESD Endurance Table (Temperature: 25℃, Humidity: 45%)

Pin	Contact Discharge	Air Discharge
Antenna Port	±5KV	±10KV
VCC, GND, RFIN	±4KV	±8KV
Others	±3KV	±6KV

5.7. Reliability Test

Table 17: Reliability Test

Test item	Conditions	Standard
Thermal Shock	-30°C...+80°C, 144 cycles	GB/T 2423.22-2002 Test Na IEC 68-2-14 Na
Damp Heat, Cyclic	+55°C; >90% Rh 6 cycles for 144 hours	IEC 68-2-30 Db Test
Vibration Shock	5~20Hz, 0.96m2/s3; 20~500Hz, 0.96m2/s3-3dB/oct, 1hour/axis; no function	2423.13-1997 Test Fdb IEC 68-2-36 Fdb Test
Heat Test	85°C, 2 hours, operational	GB/T 2423.1-2001 Ab IEC 68-2-1 Test
Cold Test	-40°C, 2 hours, operational	GB/T 2423.1-2001 Ab IEC 68-2-1 Test
Heat Soak	90°C, 72 hours, non-operational	GB/T 2423.2-2001 Bb IEC 68-2-2 Test B
Cold Soak	-45°C, 72 hours, non-operational	GB/T 2423.1-2001 A IEC 68-2-1 Test

6 Mechanics

This chapter describes the mechanical dimensions of the module.

6.1. Mechanical View of the Module

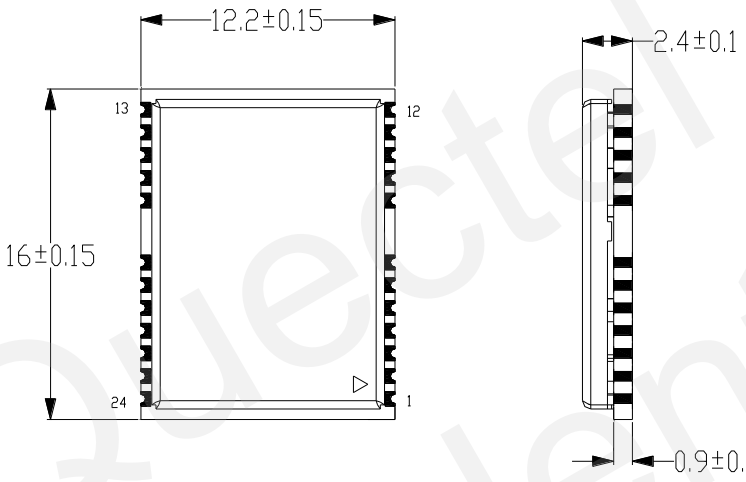

Figure 15: L20 Top View and Side Dimensions (Unit: mm)

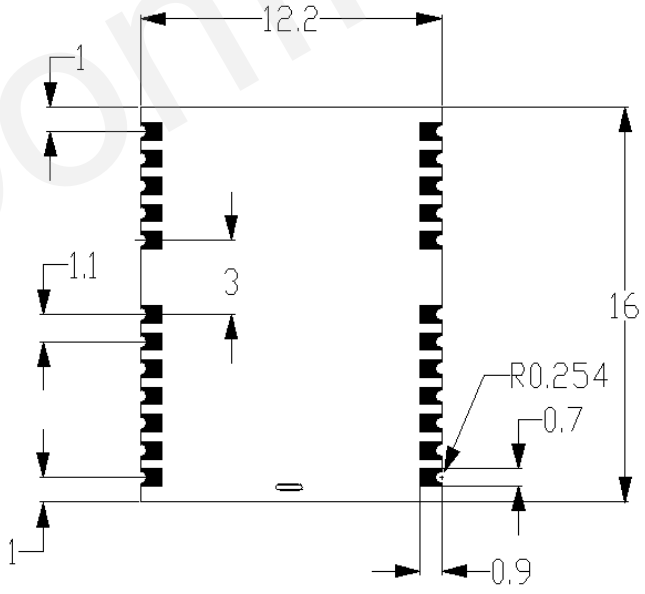

Figure 16: L20 Bottom Dimensions (Unit: mm)

6.2. Footprint of Recommendation

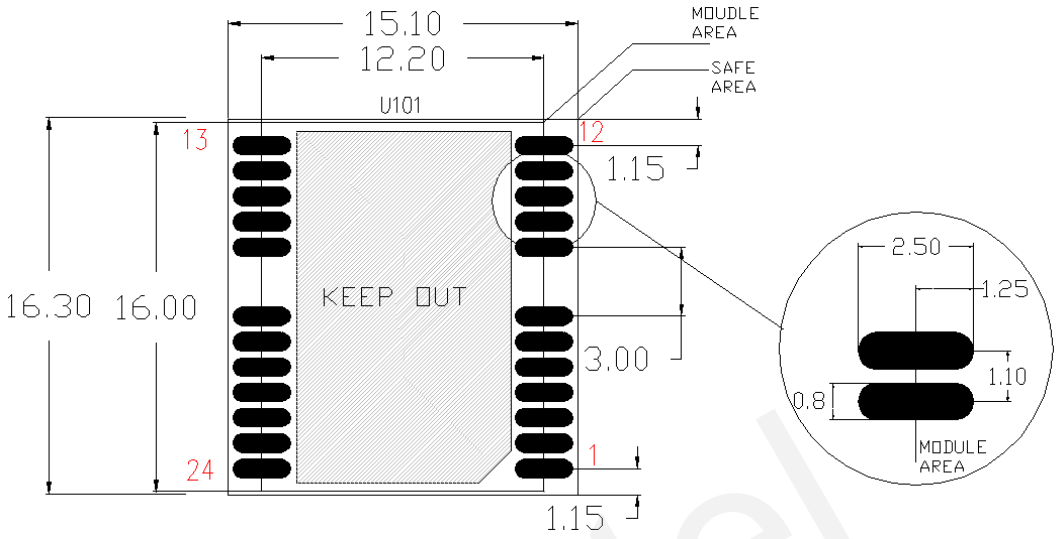

Figure 17: Footprint of Recommendation (Unit: mm)

NOTES

The keep-out area should be covered by solder mask and top silk layer for isolation between the top layer of host board and the bottom layer of the module.

6.3. Top View of the Module

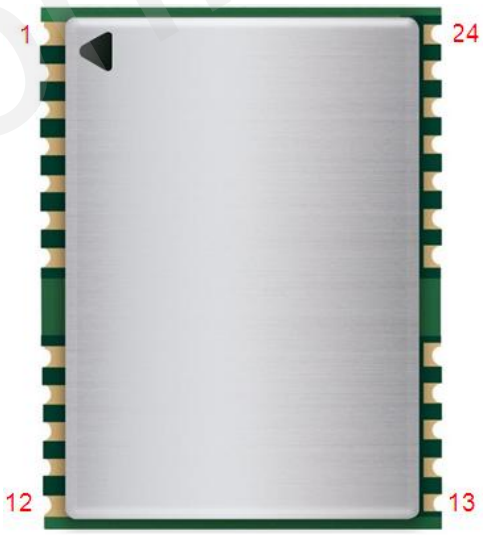

Figure 18: Top View of the Module

6.4. Bottom View of the Module

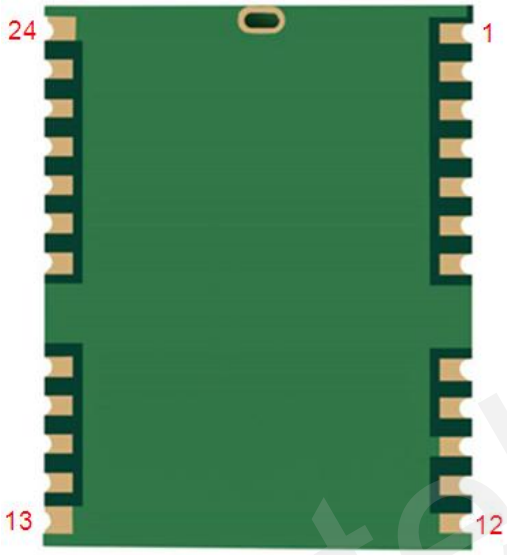

Figure 19: Bottom view of the Module

7 Manufacturing

7.1. Assembly and Soldering

L20 is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. It is suggested that the minimum height of solder paste stencil is 130um to ensure sufficient solder volume. Pad openings of paste mask can be increased to ensure proper soldering and solder wetting over pads. It is suggested that peak reflow temperature is 235~245ºC (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260ºC. To avoid damage to the module when it is repeatedly heated, it is suggested that the module should be mounted after the first panel has been reflowed. The following picture is the actual diagram which we have operated.

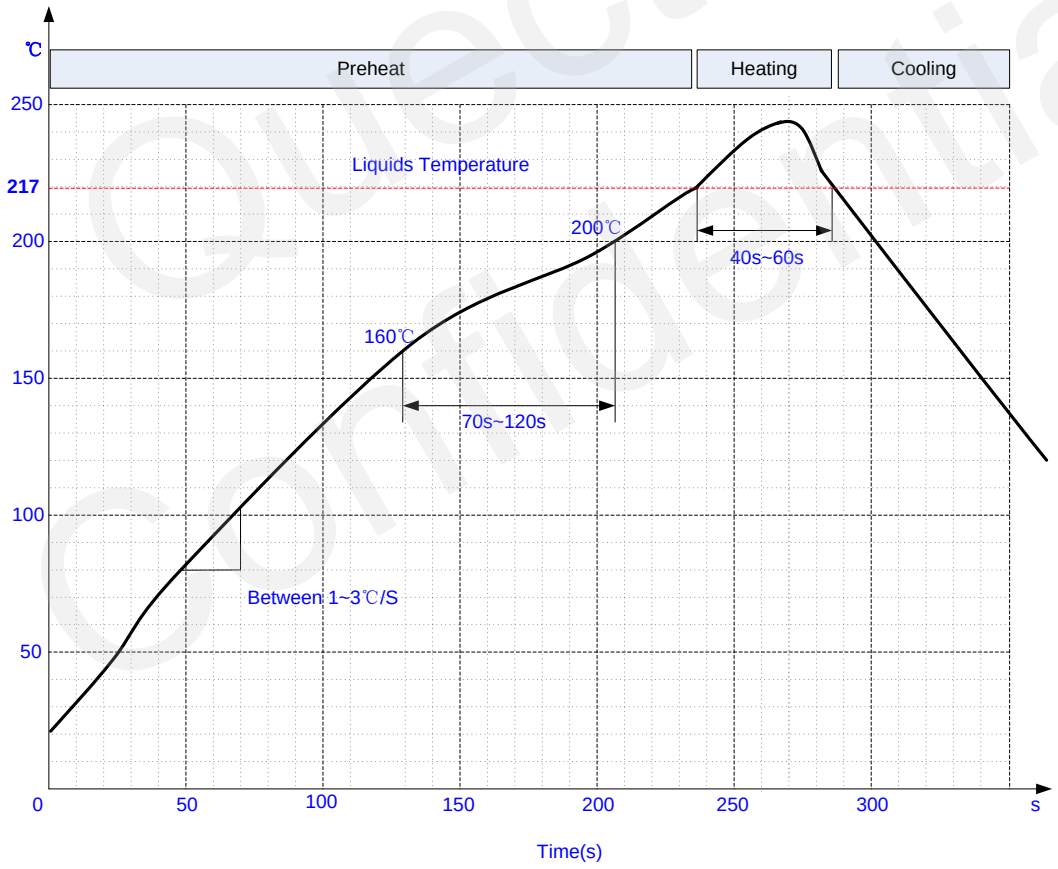

Figure 20: Ramp-soak-spike-reflow of Furnace Temperature

7.2. Moisture Sensitivity

L20 is sensitivity to moisture absorption. To prevent L20 from permanent damage during reflow soldering, baking before reflow is required in following cases:

- Humidity indicator card: At least one circular indicator is no longer blue
- The seal is opened and the module is exposed to excessive humidity.

L20 should be baked for 192 hours at temperature 40ºC+5ºC/-0ºC and <5% RH in low-temperature containers, or 24 hours at temperature 125ºC±5ºC in high-temperature containers. Care should be taken that plastic tape is not heat resistant. L20 should be taken out before preheating, otherwise, the tape maybe damaged by high-temperature heating.

7.3. Packaging

The modules are stored inside a vacuum-sealed bag which is ESD protected. It should not be opened until the devices are ready to be soldered onto the application.

L20 is shipped in tape and reel form. The reel is 330mm in diameter and each reel contains 250pcs modules.

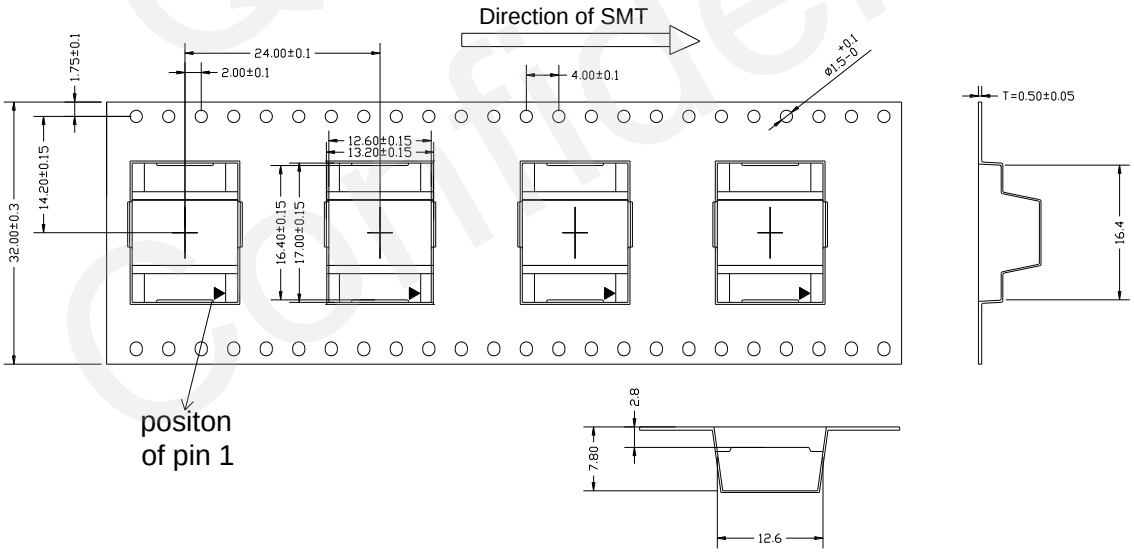

Figure 21: Dimensions and Orientations for L20 on Tape (Unit: mm)

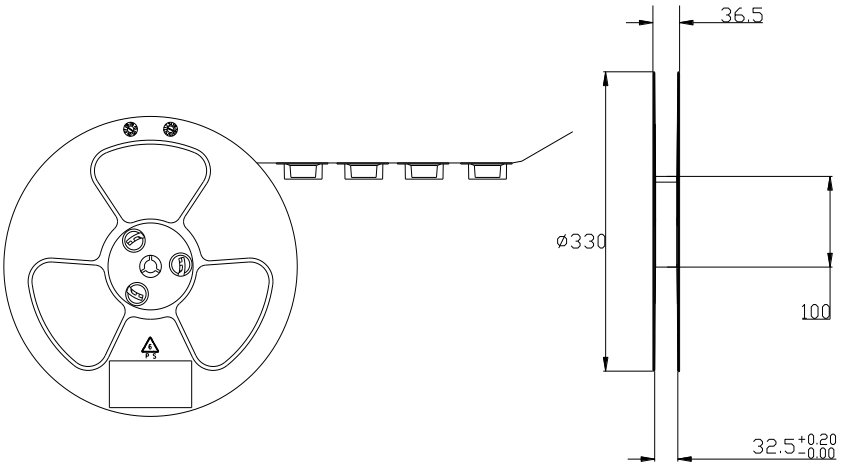

Figure 22: Dimensions of reel for 250pcs (Unit: mm)

Table 18: Reel Packing

Model Name	MOQ for MP	Minimum Package: 250pcs	Minimum Package x4=1000pcs
L20	250pcs	Size: 370mm × 350mm × 56mm N.W: 0.26kg G.W: 1.00kg	Size: 380mm × 250mm × 365mm N.W: 1.1kg G.W: 4.6kg

7.4. Ordering Information

Table 19: Ordering Information

Model Name	Ordering Code
L20 @ROM2.2	L20B-S44

8 Appendix Reference

Table 20: Related Documents

SN	Document Name	Remark
[1]	Quectel_L20_EVB_User_Guide	L20 EVB user guide
[2]	Quectel_L20_GPS_Protocol_Specification	L20 GPS protocol specification
[3]	Quectel_SIRF_AGPS_Application_Note	SIRF Platform A-GPS application note

Table 21: Terms and Abbreviations

Abbreviation	Description
CGEE	Client Generated Extended Ephemeris
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
EGNOS	European Geostationary Navigation Overlay Service
GPS	Global Positioning System
GNSS	Global Navigation Satellite System
GGA	GPS Fix Data
GLL	Geographic Position – Latitude/Longitude
GSA	GNSS DOP and Active Satellites
GSV	GNSS Satellites in View
HDOP	Horizontal Dilution of Precision
IC	Integrated Circuit
I/O	Input/Output

Kbps	Kilo Bits Per Second
LNA	Low Noise Amplifier
MSAS	Multi-Functional Satellite Augmentation System
NMEA	National Marine Electronics Association
OSP	One Socket Protocol
PDOP	Position Dilution of Precision
QZSS	Quasi-Zenith Satellite System
RMC	Recommended Minimum Specific GNSS Data
SBAS	Satellite-based Augmentation System
SUPL	Secure User Plane Location
SAW	Surface Acoustic Wave
TBD	To Be Determined
TTFF	Time-To-First-Fix
UART	Universal Asynchronous Receiver & Transmitter
VDOP	Vertical Dilution of Precision
VTG	Course over Ground and Ground Speed, Horizontal Course and Horizontal Velocity
WAAS	Wide Area Augmentation System
ZDA	Time& Date
Inorm	Normal Current
Imax	Maximum Load Current
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value

VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value