Lab 2 Practice

Prerequisites

Concept	Video Lectures	in this lab
Data flow modeling	CT Verilog series 04	Wire, reg, signed, etc
Behavioral modeling	CT Verilog series 05 ~ 06	Always block
Sequential blocks	CT Verilog series 07	Synchronous output with clock

It is strongly recommended that you complete these practice exercises to prepare for the basic lab.

1. Summation with 1-Cycle Delay (40%)

Design a simple circuit that outputs the sum of two signed 8-bit inputs (A, B).

1. To prevent potential timing issues, the sum must be stored in a **flip-flop (FF)** before being sent to the output, introducing a **1-cycle delay**.
2. The output is updated at the **positive edge of the clock**.
3. The reset is **synchronous, active-high**. When reset is asserted, the output should be **0**.
4. Complete the Verilog template lab2_1_practice.v with the provided testbench and pattern file (lab2_1_practice_t.v, pattern_A_practice.dat). Refer to the Appendix for instructions on adding the pattern files to simulation sources.
5. Your design must pass simulation, which will display the following PASS message:

```
scores =  40 / 40
PASS!
```

IO List and Specification:

Signal	I/O	Bit Width	Description
clk	input	1	Clock (positive-edge triggered)
rst	input	1	Synchronous active-high reset
A	input	8	Signed operand
B	input	8	Signed operand
out	output	12	Signed result: A+B (delayed by 1 cycle)

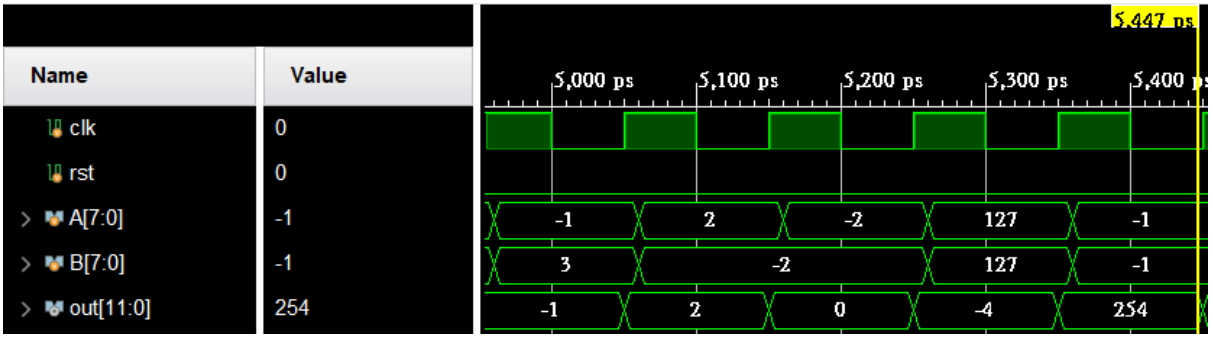
The sum must appear **1 cycle after inputs are given**.

Example

Cycle	A	B	out (after 1 cycle)
1	-8’d1	8’d3	x
2	8’d2	-8’d2	12’d2
3	-8’d2	-8’d2	12’d0
4	8’d127	8’d127	-12’d4
5	-8’d1	-8’d1	12’d254

x indicates “don’t care”.

Refer to the following waveform for a correct output example:



The radix of **A** , **B** and **out** is signed decimal on the waveform.

Notes

- **Do not modify** the testbench or patterns.
- The TA will use the same testbench with additional hidden patterns to test your design for the basic lab. The grading is based on correctness. Pass/Fail messages of the testbench are only to assist the debugging.
- Ensure your design correctly handles **signed arithmetic**.

2. Subtraction with 2-Cycle Delay (60%)

Design a circuit that computes the subtraction of two signed 8-bit inputs (A, B).

1. The result must appear at the output **2 clock cycles** after the inputs are given.
2. The output is updated at the positive edge of the clock.
3. The reset is synchronous, active-high. When reset is asserted, the output should be 0.
4. Complete the Verilog template lab2_2_practice.v with the provided testbench and pattern files (lab2_2_practice_t.v, pattern_B_practice.dat). Refer to the Appendix for instructions on adding the pattern files to simulation sources.
5. Your design must pass simulation, which will display the following PASS message:

```
scores =  60 / 60
PASS!
```

IO List and Specification:

Signal	I/O	Bit Width	Description
clk	input	1	Clock (positive-edge triggered)
rst	input	1	Synchronous active-high reset
A	input	8	Signed operand
B	input	8	Signed operand
out	output	12	Signed result: A-B (delayed by 2 cycles)

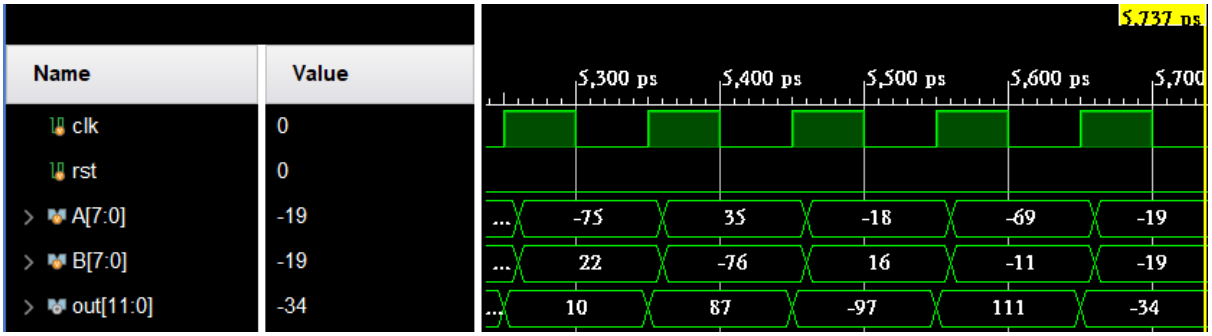
The subtraction must appear **2 cycles after inputs are given**.

Example

Cycle	A	B	out(after 2 cycle)
1	-8’d75	8’d22	x
2	8’d35	-8’d76	x
3	-8’d18	8’d16	-12’d97
4	-8’d69	-8’d11	12’d111
5	-8’d19	-8’d19	-12’d34

x indicates “don’t care”.

Refer to the following waveform for a correct output example:

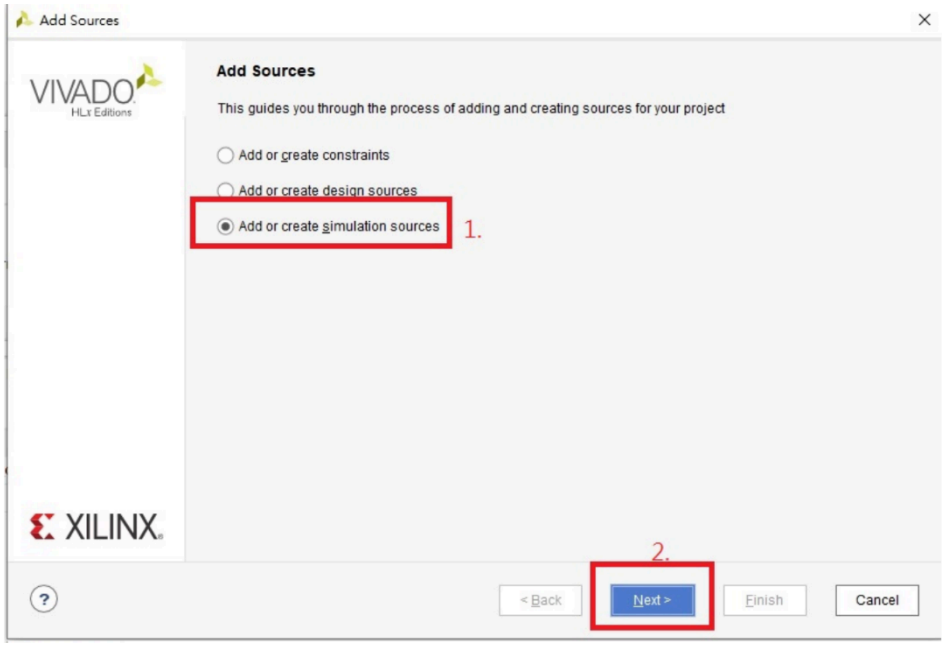


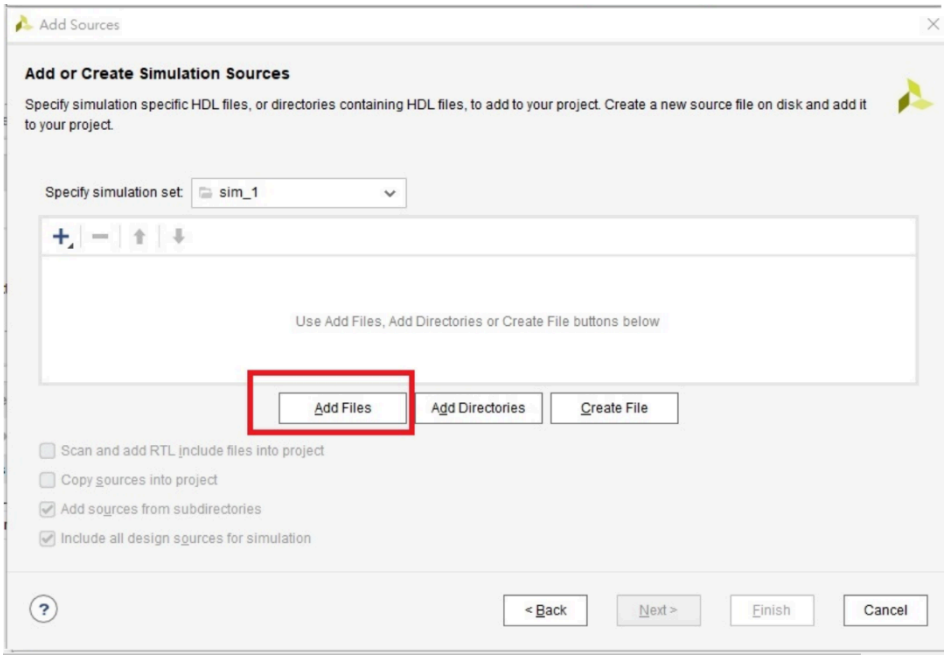
The radix of **A** , **B** and **out** is signed decimal on the waveform.

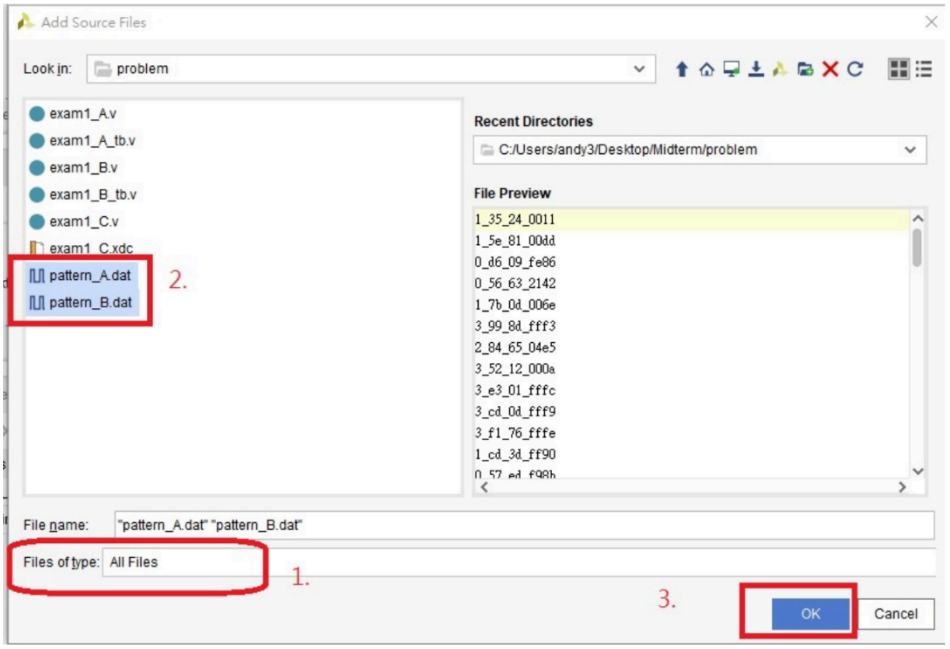
Notes

- **Do not modify** the testbench or patterns.
- The TA will use the same testbench with additional hidden patterns to test your design for the basic lab. The grading is based on correctness. Pass/Fail messages of the testbench are only to assist the debugging.
- Ensure your design correctly handles **signed arithmetic**.

Appendix: Adding Pattern Files to Vivado Simulation






Add Source Files
Look in: problem
exam1_A.v
exam1_A_tb.v
exam1_B.v
exam1_B_tb.v
exam1_C.v
exam1_C.xdc
pattern_A.dat
pattern_B.dat
2.
Recent Directories
C:/Users/andy3/Desktop/Midterm/problem
File Preview
1_35_24_0011
1_5e_81_00dd
0_d6_09_fe86
0_56_63_2142
1_7b_0d_006e
3_99_8d_fff3
2_84_65_04e5
3_52_12_000a
3_e3_01_fffc
3_cd_0d_fff9
3_f1_76_fffe
1_cd_3d_ff90
File name: "pattern_A.dat" "pattern_B.dat"
Files of type: All Files
1.
3.
OK
Cancel