Lab 3 Practice: LEDs Controller

Objective

1 This exercise will help you gain hands-on experience with FPGA LEDs, clock division, and finite-state machine (FSM) design in Verilog.

Action Items

1. lab3_practice.v

In this lab, you must design an LED controller based on a finite-state machine (FSM). Then you can control the LED sequence using switches, as described below.

a. I/O list

I/O	Connected to	Definition
clk	W5	Clock signal with the frequency of 100MHz
rst	SW15	Asynchronous active-high reset signal, resetting FSM to **INITIAL** state
slow	SW0	Enables the slow LED flashing
fast	SW1	Enables the fast LED flashing
end_light	SW2	Ends the light sequence and transitions FSM to **FINAL** state
led[15:0]	LD15~LD0	Lighting up the LEDs in the sequence based on the control of the switches

b. **FSM Specification**

The FSM should consist of three states: **INITIAL**, **PLAY**, and **FINAL**.

- You may design a variant, but it must respect the reset switch behavior described.
- At any state, **rst == 1** forces the FSM to enter the **INITIAL**. When **rst** becomes 0, the FSM resumes normal operation.

✓ **INITIAL** state

- Entered when **rst == 1**.
- All LEDs (**LD15~LD0)** are **on**.

LD15 ●●●●●●●●●●●●●●●● LD0

(● : LED on, ○ : LED off)

- When **rst == 0**, the FSM transitions to the **PLAY** state on the next clock cycle.

✓ **PLAY** state
- If **end_light** is set to **1**, the FSM transitions to the **FINAL** state on the next cycle.
- If **end_light** is set to **0**, the FSM stays in the **PLAY** state.
- In this state, the LED behavior depends on switch settings:
  - **Slow Mode** (**slow==1**):
    Even-numbered LEDs flash at the rate of **100MHz/2^{28}**.
    LD15○●○●○●○●○●○●○●○● LD0
    (● : LED on, ○ : LED off)
    LD15○○○○○○○○○○○○○○○○ LD0
    (● : LED on, ○ : LED off)
  - **Fast Mode** (**fast==1**):
    Odd-numbered LEDs flash at the rate of **100MHz/2^{27}**.
    LD15 ●○●○●○●○●○●○●○●○ LD0
    (● : LED on, ○ : LED off)
    LD15○○○○○○○○○○○○○○○○ LD0
    (● : LED on, ○ : LED off)
  - If **slow** and **fast** are both set to **1**:
    - Even LEDs follow slow flashing.
    - Odd LEDs follow fast flashing.

✓ **FINAL** state
- All 16 LEDs flash on and off once per second.
- After five seconds (three on-off cycles, i.e., on → off → on → off → on), the FSM returns to the **INITIAL** state.

LD15 ●●●●●●●●●●●●●●●● LD0 (1 second ON)
(● : LED on, ○ : LED off)
LD15 ○○○○○○○○○○○○○○○○ LD0 (1 second OFF)
(● : LED on, ○ : LED off)

You must use the following template for your design:

```
module lab3_practice (
    input wire clk,
    input wire rst,
    input wire slow,
    input wire fast,
```

```
        input wire end_light,

        output reg[15:0] led

    );

    // add your design here
endmodule
```

Attention

- ✓ If you create several modules, merge them into a single Verilog file.
- ✓ This practice prepares you for the next lab. Make sure you fully understand your design.
- ✓ Feel free to ask questions about the specification on the EECLASS forum.
- ✓ DO NOT copy-and-paste code segments from PDFs (hidden characters may cause hard-to-debug syntax errors).