A 40Gb/s CTLE of a PAM-4 Wireline Receiver

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***Abstract*— An analog frontend for a 40Gb/s four-level pulse-amplitude modulation (PAM-4) wireline receiver is presented. The proposed frontend is based on the structure of the active continuous time linear equalizer (CTLE) and provides the peaking gain of 4.8 dB at Nyquist frequency, which can significantly reduce the inter-symbol interference (ISI). The paper focus on the balance between high peaking gain and DC gain as well as low power consumption.**

***Index Terms*— CTLE, PAM-4, ISI, SerDes, wireline, receiver, CMOS**

I. Introduction

With the exponential growth demand for high speed data transmission, new standards for electrical interconnections are proposed. Four-level pulse-amplitude modulation (PAM-4) has the better spectral efficiency than the conventional non-return-to-zero (NRZ) but is more sensitive to inter-symbol interference (ISI), noise and other nonlinearities [1], which requires a better performing interface for the signal transmission.

Serializer & Deserializer (SerDes) are widely used to recover the distorted signal caused by the channel with the low-pass frequency domain characteristics. Continuous time linear equalizer (CTLE) is an important part in the receiver and plays significant role in preliminary improving the signal quality [2]. One of the most important issues in the CTLE design is to raise the peaking gain at the Nyquist frequency and fully compensate the channel loss. The frequency response of the channel with the CTLE within the Nyquist frequency should be approximately a constant.

In this paper, a CTLE working on a 40Gb/s SerDes receiver is presented and this CTLE provides 4.8dB peaking gain at 10-GHz Nyquist frequency. Section II analyses the structure of CTLE and proposes comprehensive improvements on raising the peaking. Section III provides the simulation results of the presented CTLE and section IV makes the conclusion.

II. Circuit Design

The negative CTLE based on the RC network is shown in Fig. 1, which has the following transfer function

$$\mathrm{H(s)} = \frac{R_2 C_1}{C_1 + C_2} * \frac{S + \frac{1}{R_1 C_1}}{S + \frac{R_1 + R_2}{R_1 (C_1 + C_2)}} \qquad (1)$$

It has only a zero and a pole, and can be regarded as a high-pass filter. However, due to its drawbacks on the gain less than 1 and the complex input/output impedance match probl-

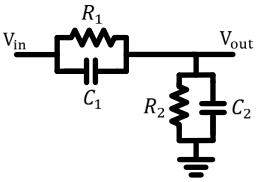

Fig.1. Schematic of the negative CTLE based on RC network.

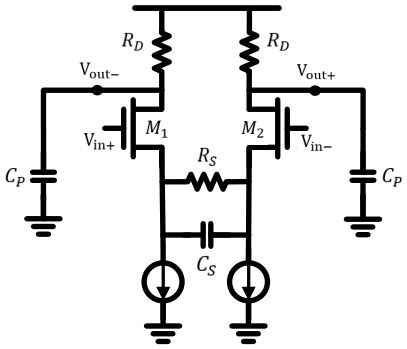

Fig. 2. Schematic of the active CTLE circuit.

lems, the positive CTLE is more popular in the receiver design. The active CTLE in Fig. 2 is a differential pair with degeneration resistor and capacitor.

The main issue in the CTLE design is to raise the peaking gain at the Nyquist frequency and fully compensate the channel loss. The fundamental design method is to establish the math expression of the circuits, get the formula of circuits performance indexes and alter the parameters to reach the design requirements. The analysis is focus on the frequency domain so the s-domain model of the circuits is widely used.

Its transfer function is written below

$$\mathrm{H(s)} = \frac{g_m}{C_P} * \frac{S + \frac{1}{R_S C_S}}{(S + \frac{1 + g_m R_s/2}{R_S C_S})(S + \frac{1}{R_D C_P})} \qquad (2)$$

And one zero and two poles can be derived

$$W_z = \frac{1}{R_S C_S} \quad W_{p1} = \frac{1+g_m R_S/2}{R_S C_S} \quad W_{p2} = \frac{1}{R_D C_P} \qquad (3)$$

The poles frequency should be around the Nyquist frequency and be higher than the zero frequency to achieve high-frequency peaking gain at the Nyquist frequency. The ideal peaking that represents the ability of CTLE to compensate high-frequency is defined as follow

$$\text{ideal peaking} = \frac{W_{p1}}{W_z} = 1 + g_m R_S/2 \qquad (4)$$

To achieve the goal of raising the ideal peaking, from the

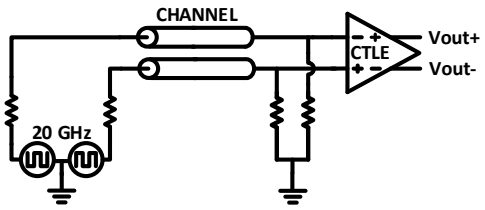

Fig. 3. Schematic of the test circuit for the proposed CTLE.

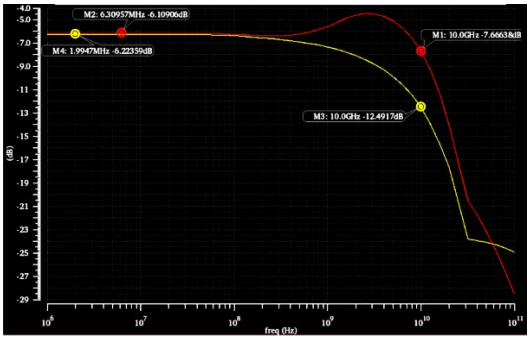

Fig. 4. The AC simulation results.

perspective of the frequency response, the raising range of the response should be extended. And from the perspective of the ideal peaking definition, the difference between the zero and the dominant pole should be larger. These two perspectives both require a lower zero frequency W_z and a higher dominant pole frequency W_{p1}. Increasing the second pole is an extra option because this method will also extend the raising range of the frequency response and the peaking gain will be lifted.

Therefore, increasing the transconductance g_m and the degenerate resistor R_S is a regular method. Augmenting the C_S and reducing R_D can also improve the peaking. The value of C_P is a constant and depends on the input impedance of the next stage. However, these parameters also affect other performance indexes besides peaking gain.

For example, when the *S* in the transfer function is equal to 0, the frequency response is the DC gain

$$A_{DC} = \frac{g_m R_D}{1 + g_m R_S/2} \qquad (5)$$

If the value of R_D is reduced to increase the peaking gain, the DC gain will decrease and from the schematic of the CTLE in Fig. 2, it can be deduced that the V_{DS} of the transistor will be raised so the static power dissipation of the transistor will also increase.

To make the system to achieve the best performance, the design should keep the balance among peaking gain, DC gain, power consumption, silicon area, etc. In this paper, the main method to raise the peaking gain is to increase the value of the degenerate resistor R_S and the degenerate capcitor C_S.

III. Simulation Results

The proposed CTLE is designed in TSMC 65-nm CMOS technology with 1.0 V supply. A channel with 6.39 dB loss at 10-GHz Nyquist frequency is used in the simulation. The schematic of the test circuits is shown in Fig. 3. Resistors at the both side of the channel are used to reduce the reflections.

As shown in Fig. 4, the red curve is the frequency response

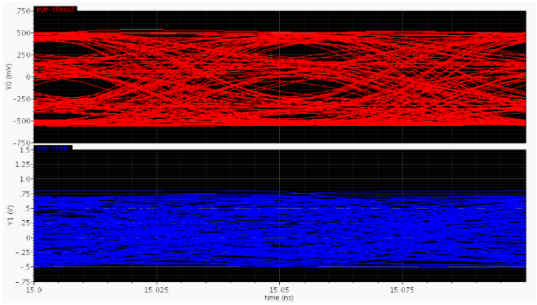

Fig. 5. The input and output eye diagram of the CTLE.

of the channel, the DC gain of which is around -6.2dB because of the voltage division by the series resistors and the loss in channel. The yellow curve is the frequency response of the channel with the proposed CTLE. The CTLE provides 4.8 dB gain at Nyquist frequency and the DC gain is greater than 1.

The input PAM-4 signal is 1.2Vpp differential running at 20 GBaud. As shown in Fig. 5, the eye is closed with 6.39 dB channel loss. After the equalization, the ISI can be greatly reduced and eye opening is 210 mV height and 20 ps width.

IV. Conclusion

This paper presents a 40Gb/s PAM-4 active CTLE designed in 65-nm CMOS process. The proposed CTLE can compensate 4.8dB gain at Nyquist frequency and simulation shows that the proposed CTLE can reduce the ISI and reopen the eye of the input signal.

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