

PENGYU ZENG

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EDUCATION

University of Washington

Doctor of Philosophy in Electrical and Computer Engineering

Seattle, WA

Sept. 2023 - June 2028(Expected)

- **Advisor:** Prof. [Sajjad Moazeni](#)
- **Research Interests:**
 - High-speed Serial Links, Photonic Interconnects, Mixed-signal Circuits

Wuhan University

Bachelor of Engineering in Electronic Information Engineering

Wuhan, China

Sept. 2019 - June 2023

- **GPA:** 3.85/4.0 (91/100)
- **Major Courseworks:**
 - **Circuits:** Analog Circuits (4.0/4.0), Digital Circuits (4.0/4.0), Communication Electronic Circuits (4.0/4.0), Electrical and Electronic Engineering Training (4.0/4.0)
 - **Embedded Systems:** Embedded System Design (4.0/4.0), Principle and Interface Technology of Microcomputer (4.0/4.0), Microprocessor and Its System Design (4.0/4.0)
 - **Programming:** Programming Fundamentals (4.0/4.0), Algorithms and Data Structures (4.0/4.0), Programming Practice (4.0/4.0), Embedded Software Design (4.0/4.0)
 - **Mathematics & Physics:** Methods of Mathematical Physics (4.0/4.0), Signals and Systems (4.0/4.0), Probability and Statistics & Stochastic Progress (4.0/4.0), Electromagnetic Theory (4.0/4.0)

University of Notre Dame

Visiting Student in Electrical Engineering

South Bend, IN

June 2022 - Aug. 2022

TECHNICAL SKILLS

- **EDA Tools:** Cadence Virtuoso, HSPICE, LTSPICE, Altium Designer
- **Programming Languages:** MATLAB, Verilog, Python, C, C++, C#, Java
- **FPGA & Embedded Development IDE:** CCS, Keil, Quartus, Vivado
- **MCU Platforms:** MSP430, MSP432, STM32, C51

RESEARCH & INTERNSHIPS

University of Washington, ECE Department

Analog IC Design: Coherent Co-packaged Optical Transceiver

Seattle, WA

Sept. 2023 - May 2024

- Designed the 40Gbps serializer and deserializer for the transceiver
 - Proposed a novel True Single-Phase Clock(TSPC) **latch**, which is **2.4x** faster than the standard cell
 - Proposed a novel **Tri-state MUX**, which has **0.3x** jitter compared to the conventional design
 - Designed the clock distribution for the serializer and deserializer
- Designed the analog frontend(AFE) for the receiver
 - Used MATLAB to make a comparison among different architectures of AFE to find a optimal design with better SNR

- Built the AFE with Transimpedance Amplifier(TIA) and Continues Time Linear Equalizer(CTLE) based on the simulation results of MATLAB

Shineview Co. Ltd., Analog Design Department

Shanghai, China

*Analog IC Design: **Bandwidth Extension based AFE for High-speed Display Driver** March 2023 - June 2023*

- Used Cross-coupled Pair(XCP) to introduce a pair of conjugate poles to implement tunable-peaking CTLE, and to increase the peaking and bandwidth of CTLE
- Designed multi-stage amplifiers with bandwidth extension for the AFE

Tsinghua University, School of Integrated Circuits

Beijing, China

*Analog IC Design: **A 40Gbps CTLE for a PAM4 Wireline Receiver***

June 2021 - July 2021

- Finished the design, drew the schematic and layout of a 40Gbps CTLE in TSMC 65nm CMOS process, finished DRC/LVS/PEX and post-simulation on Cadence Virtuoso

University of Notre Dame, EE Department

South Bend, IN

*Analog IC Design: **8T SRAM-based Unified Analog Compute-In-Memory and PUF** June 2022 - Aug. 2022*

- Designed an 8T SRAM-based Unified Compute-In-Memory and Physical Unclonable Function with automated generator on Python and verified the circuits on the HSPICE with 16nm PTM

Fudan University, State Key Lab of ASIC and System

Shanghai, China

*Analog IC Design: **Error Analysis and Agile Design in Pipelined ADC***

Sept. 2021 - Jan. 2022

- Designed a behavioral model of the Pipelined ADC on MATLAB to verify the digital error correction and calibration algorithm
- Made systematic and quantitative analysis in digital error correction algorithm, which is crucial in pipelined ADC, making clear explanation of the principle of correction, the reason of outputs' overlap-addition, etc.

Wuhan University, Electronic Information School

Wuhan, China

*Digital IC Design: **A SoC for Dehaze Acceleration Based on ARM Cortex-M3***

Mar. 2021 - Sept. 2021

- Designed a SoC on Xilinx FPGA for real time image dehazing, which used ARM Cortex-M3 as CPU and encapsulated Dark Channel Prior algorithm into an IP core.

Wuhan University, Electronic Information School

Wuhan, China

*Board Level System Design: **Intelligent Transport Robot Based on Raspberry Pi***

Dec. 2020 - Feb. 2021

- Designed the board-level peripheral circuits for Raspberry Pi which is running object detection and color recognition algorithm to autonomously carry the cargo

SELECTED AWARDS

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- **Mitacs Globalink Research Award** (Awarded to top students worldwide to do research in Canada)
 - **Excellent Overseas Visiting Students Fellowship** 1%
 - **Beacon Fire Scholarship** 2%
 - **Merit Student of Wuhan University** 5%
 - **First-class Scholarship of Wuhan University** 5%

PUBLICATIONS & MANUSCRIPTS

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- J. Liu, B. Cheng, **P. Zeng**, S. Davis, M. Chang and N. Cao, "Privacy-by-Sensing with Time-domain Differentially-Private Compressed Sensing", in submission to Design, Automation, and Test in Europe (DATE), Apr. 2023.
 - **P. Zeng**, and Z. Tang, "A Comprehensive Analysis of Error Correction in Pipelined ADC" [PDF]
 - F. Shao and **P. Zeng**, "Urban Waterlogging Monitoring System Based on LoRa Technology," to appear at International Conference on Computer, Communication, Control, Automation and Robotics (CCCAR), Mar. 2022.