Pengyu Zeng

https://pengyuzeng03.github.io | pengyuzeng03@gmail.com | (+86) 159-8606-6878

EDUCATION

Wuhan University **Wuhan, China**

Bachelor of Science in Electronic Information Engineering *Sept. 2019 – June 2023*

- **GPA & Scores:** 3.85/4.00 (91/100); TOEFL:106/120
- **Selected Awards:** Mitacs Globalink Research Award (Awarded to top students worldwide to do research in Canada), Excellent Overseas Visiting Students Award (1%), Beacon-fire Scholarship (2%), Merit Student of Wuhan University (5%)
- **Relevant Courses:** Analog Circuits (4.0/4.0), Digital Circuits (4.0/4.0), Methods of Mathematical Physics (4.0/4.0), Signals and Systems (4.0/4.0), Probability and Statistics & Stochastic Progress (4.0/4.0), Algorithms and Data Structures (4.0/4.0)

RESEARCH INTERESTS

- Mixed-signal Circuits/Computing System, Compute-in-Memory, Hardware Security, Agile Design

RESEARCH EXPERIENCE

University of Notre Dame, Advisor: Prof. Ningyuan Cao **South Bend, IN**

Summer Research Intern (In-person), **Unified Mixed-signal Compute-In-Memory and PUF** *June 2022 – Aug. 2022*

- Designed the model of 8T SRAM based CIM with automated generator. Derived and summarized the impact of nonidealities (process variation, noise, Early Effect, etc.) from physical level to architecture level.
  - Abstracted the process variation. Proposed universal equations to quantify the static noise caused by the variation in various CIM arrays and verified with 16nm PTM in HSPICE. Equations show SNR is independent of circuits parameters.
  - Used Parseval's Theorem to figure out that V_{rms} of thermal noise is a constant when the dimension of MAC array changes.
  - Wrote Python scripts to achieved an automated flow from circuits and testbench generation to simulation results analysis.
- Designed an energy/area efficient privacy-preserved mixed-signal computing system on unified CIM and PUF.
  - Directly mapped random projection algorithm on the computing array to encrypt and compress the input feature
  - Reused CIM array as the PUF, which works to generate the key for the random projection, to achieve area efficiency.
  - Lowered V_{WL} to increase the random variation and used differential structure to eliminate the systematic variation to improve the randomness and robustness of PUF.

Fudan University, Advisor: Prof. Zhangwen Tang **Shanghai, China**

Research Assistant, **The Error Correction Analysis and Agile Design in the Pipelined ADC** *Sept. 2021 – Jan. 2022*

- Made systematic and quantitative analysis in digital error correction algorithm, which is crucial in pipelined ADC.
  - Established the transfer function to connect the analog signal and digital output, accurately and clearly analyzing the digital output error caused by comparators threshold mismatch or aperture error.
  - Proposed that the correction principal is the weights ratio of two adjacent stage's output is inherently opposite to the ratio of output errors. Used Recursive Thinking to verify the validation of the digital error correction on the architecture level.
  - Explained the reason of non-integer precision and the overlap-addition of the digital outputs by establishing the function of the input analog signal, quantized signal and digital output.
  - Quantified the noise tolerance ability, error correction range and output encoding among three kinds of ADC structures.
- Built a behavioral model of the pipelined ADC with MATLAB to accelerate the design process.
  - Designed a model with variable parameters in Op-amp and MDAC to verify the error correction and calibration algorithm. Proposed Monte Carlo Simulation to get comprehensive simulation results of ENOB, SNR, SFDR, etc.
  - Added changeable noise (reference voltage noise, amplifier output noise, etc.) and mismatch (capacitor mismatch, comparator offset, etc.) to analyze the impact of nonidealities on the performance of the ADC.

Tsinghua University, Advisor: Prof. Ziqiang Wang **Beijing, China**

Summer Research Intern (In-person), **A 40Gb/s CTLE for a PAM4 Wireline Receiver** *June 2021 – July 2021*

- Drew the schematic and layout in a 65nm CMOS process, finished DRC/LVS/PEX and post-simulation on Cadence Virtuoso.
- Adopted variable-controlling method to improve the performance of the CTLE and found the tradeoff among peaking gain, DC gain and power dissipation. Small model of MOSFET and frequency domain analysis is used.
- Used MATLAB to verify the nonideal characteristic of the bode diagram with different zeros and poles.

PUBLICATIONS & MANUSCRIPTS

- J. Liu, B. Cheng, **P. Zeng**, S. Davis, M. Chang and N. Cao, "Privacy-by-Sensing with Time-domain Differentially-Private Compressed Sensing", in submission to *Design, Automation, and Test in Europe (DATE)*, Apr. 2023.
- **P. Zeng**, Y. Chen and Z. Tang, "A Comprehensive Analysis of Error Correction in Pipelined ADC".
- F. Shao and **P. Zeng**, "Urban Waterlogging Monitoring System Based on LoRa Technology," to appear at *International Conference on Computer, Communication, Control, Automation and Robotics (CCCAR)*, Mar. 2022.

TECHNICAL SKILLS

- **EDA Tools:** Cadence Virtuoso, HSPICE, LTSPICE, Quartus, Vivado, Altium Designer
- **Programming Languages:** Verilog, SPICE, Assembly Language(ARM, Intel), C, C++, C#, Python, MATLAB, Latex