Detailed Analysis of the Digital Error Correction in the Pipelined ADC

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Introduction

- Digital error correction is one of the most crucial algorithms in the pipelined ADC. The structure of the ADC depends on this algorithm which can correct the aperture error and the digital output error caused by the mismatch of comparators.

- There are many different methods to analysis this algorithm presented in previous works. Meanwhile, there are many details need to be interpreted.

- This report tries to integrate different methods and proposes the detailed analysis on the basic thinking of the pipelined ADC, the principal of the digital error correction algorithm and the significant points in the valid algorithm.

Outline

- The physical model of the pipelined ADC
- The basic pipelined ADC
- Redundancy and digital error correction
- Comparator offset and digital output

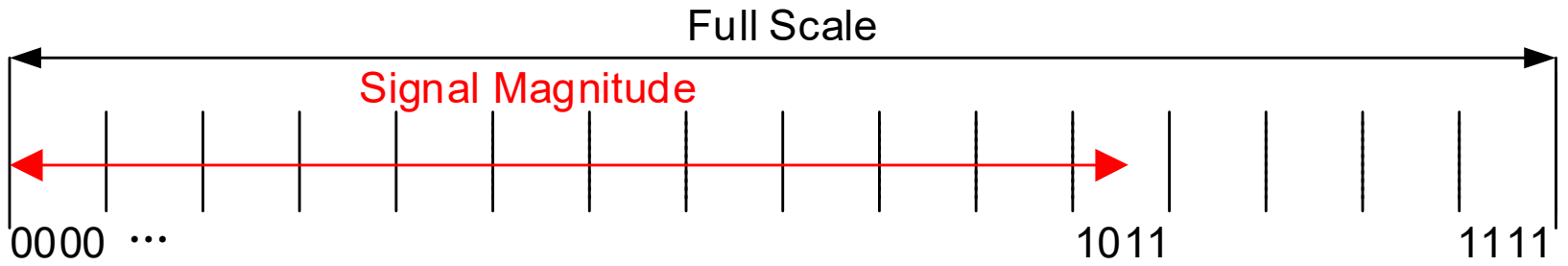
Outline

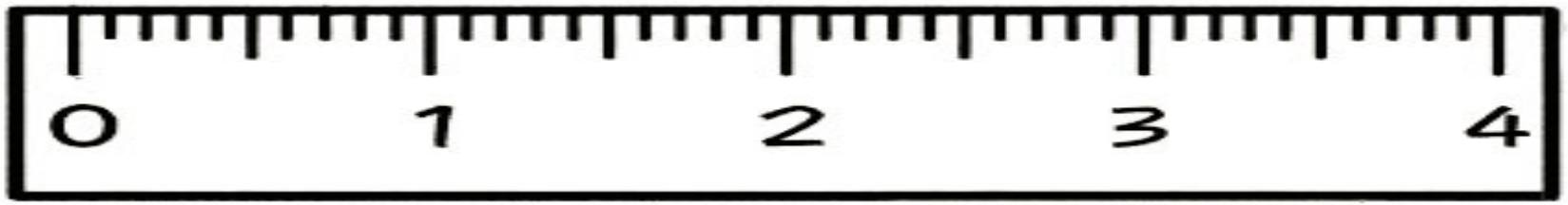
- Key points
  - The physical model of the pipelined ADC
  - The basic pipelined ADC
  - Redundancy and digital error correction
  - Comparator offset and digital output

- To build:
  - Physical model
  - Circuits
  - Math expression
- Analysis the al-gorithm with the math expression

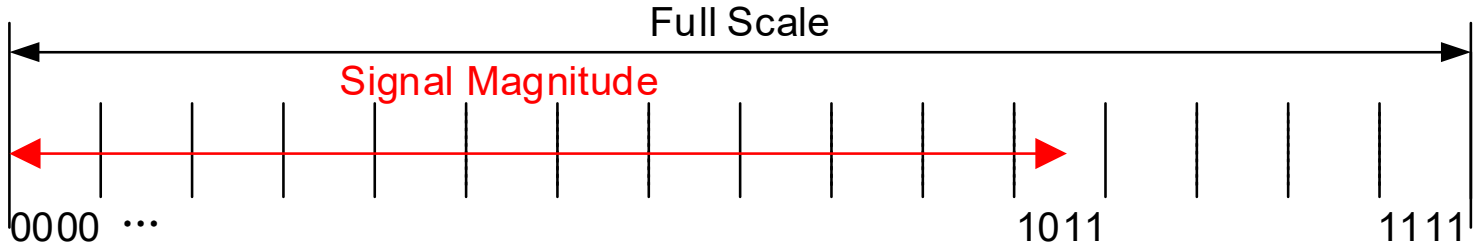
Physical Model

- Basic ADC (Flash)
- *k* bit Need 2^k-1 comparators

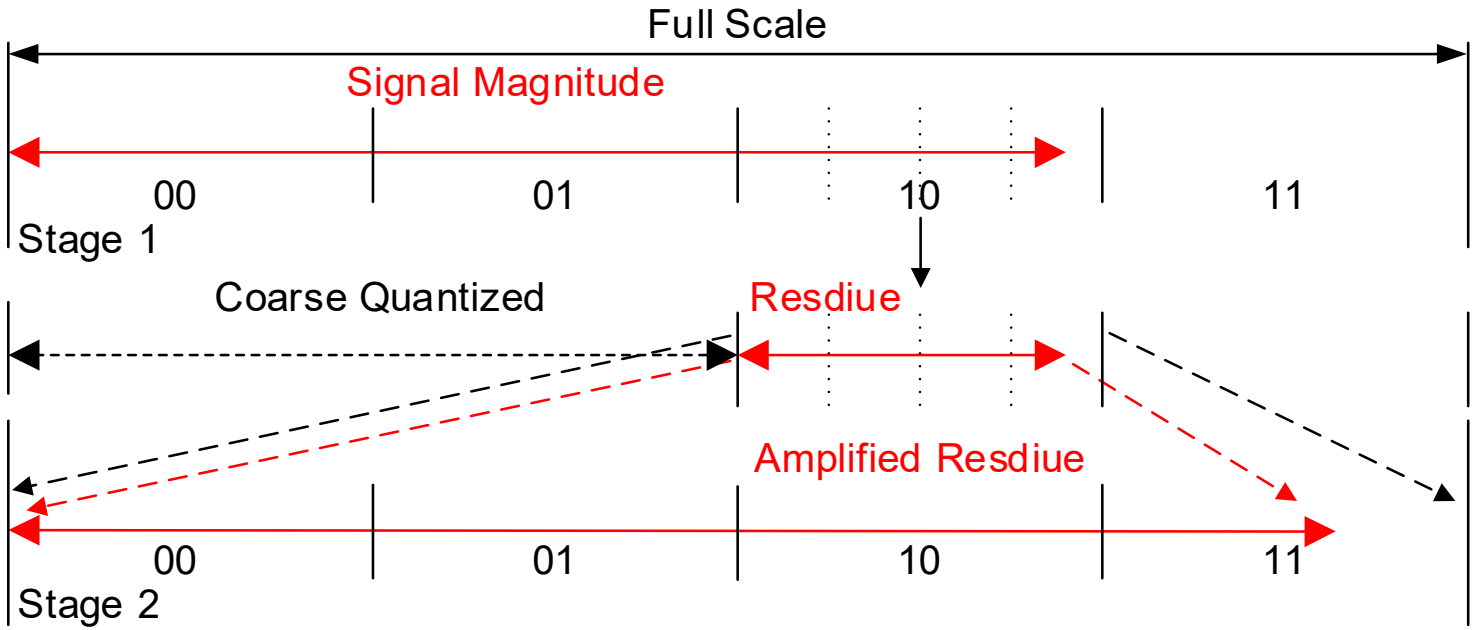




Physical Model



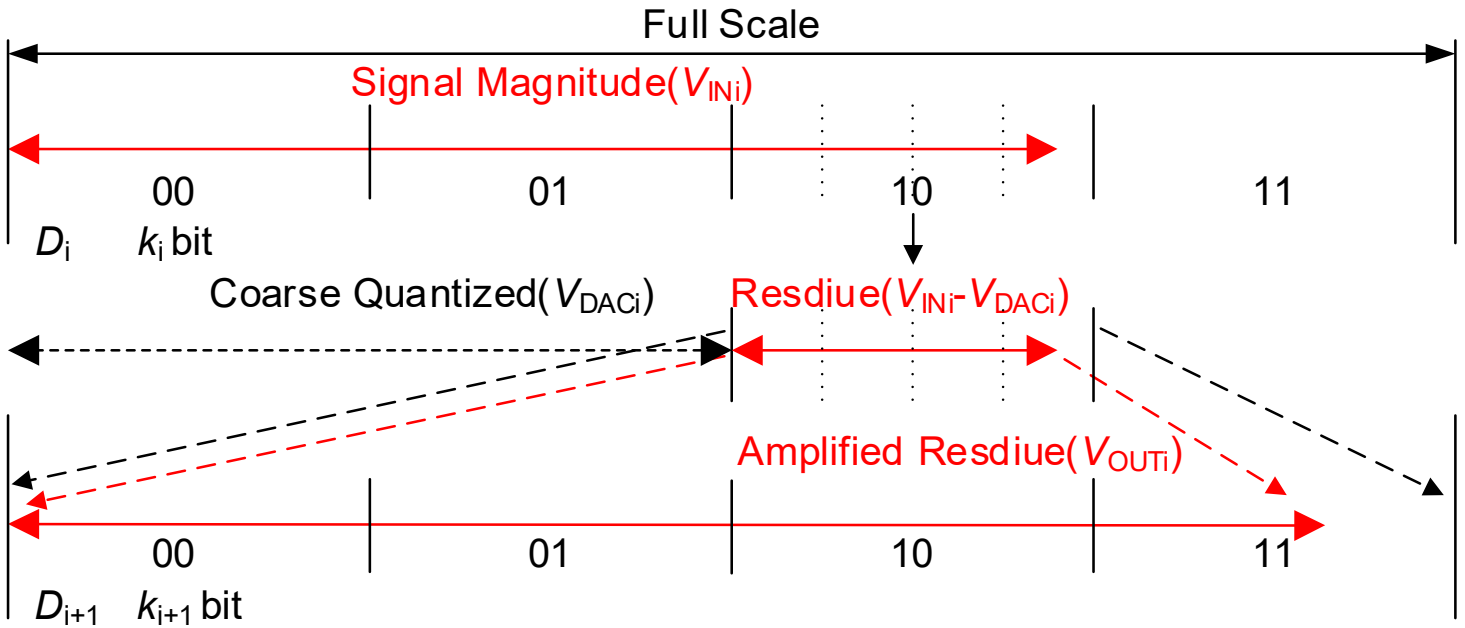
- 15 Comparators



- Step by step
  - Coarse quantize
  - Get the **residue**
  - Amplify and quantize
- 2*3=6 Comparators

Physical Model

- The Thinking of the Pipelined ADC



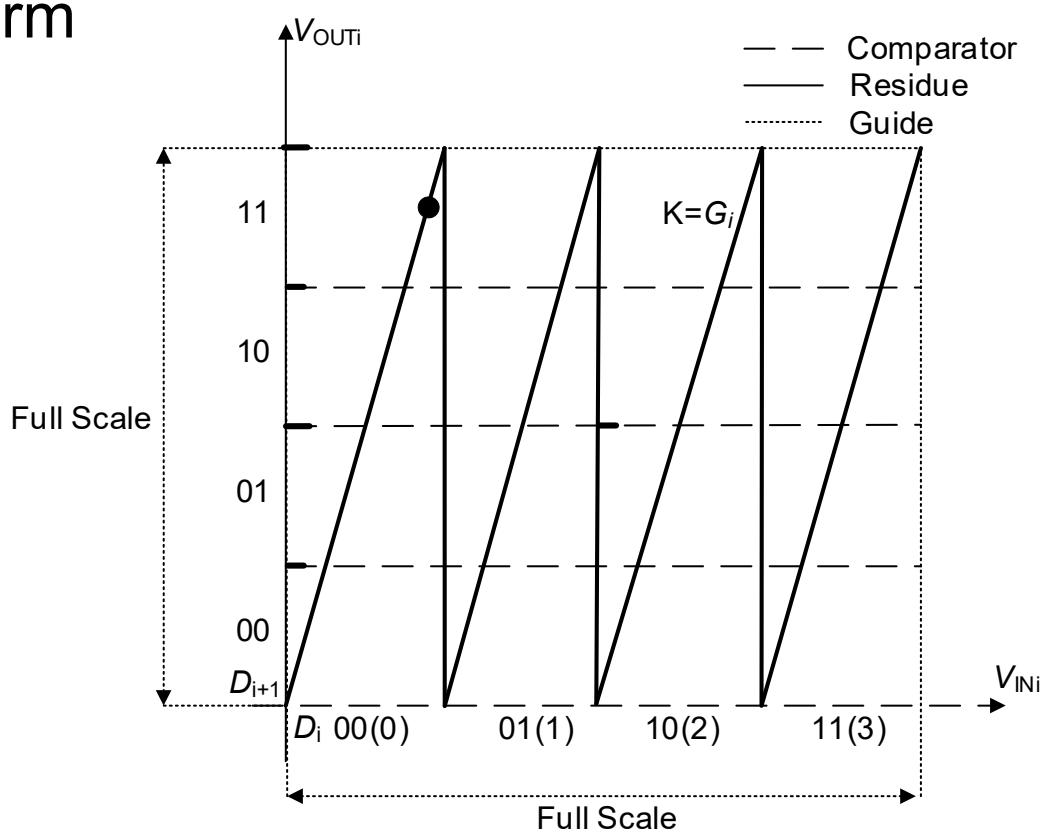
- Step by step
  - Coarse quantize
  - Get the **residue**
  - Amplify and quantize

$$V_{OUTi}=G_i(V_{RESi})=G_i(V_{INi}-D_iLSB_i) \qquad LSB_i=\frac{FS}{2^{k_i}}$$

$$V_{RESi}<LSB_i \qquad G_i=2^{k_i}$$

Physical Model

- The Transfer Waveform



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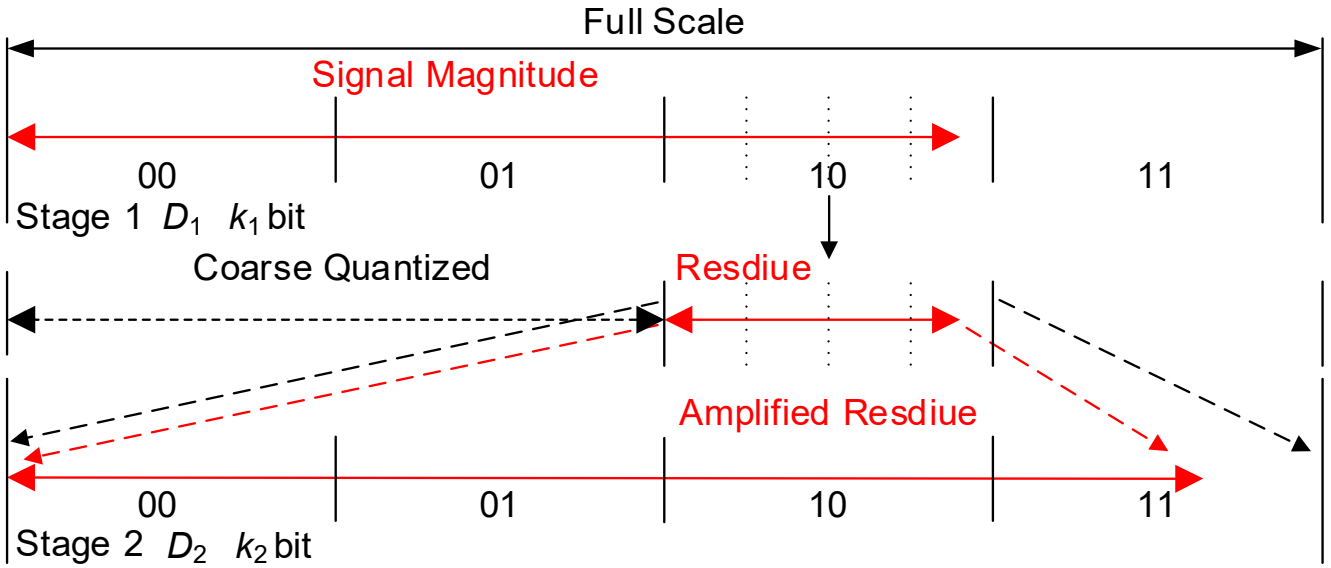
$$V_{RESi}<LSB_i \qquad G_i=2^{k_i}$$

Physical Model

- Digital Output of the Pipelined ADC



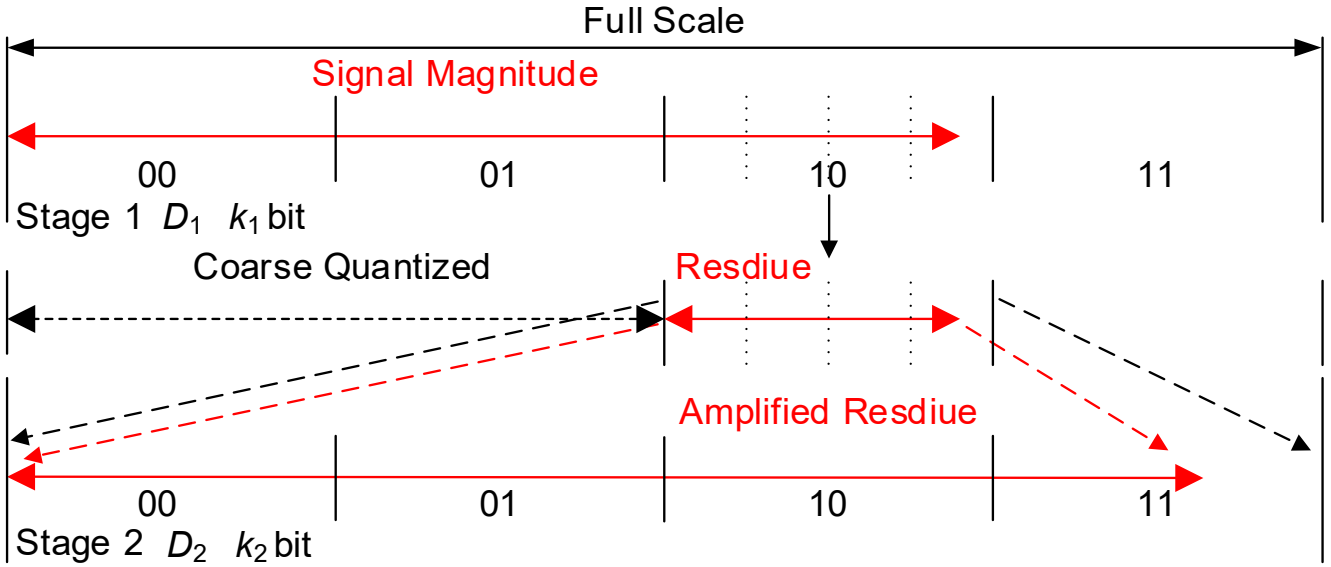
Stage 1: 10

Stage 2: 11

Why? System output : 1011

Physical Model

- Digital Output

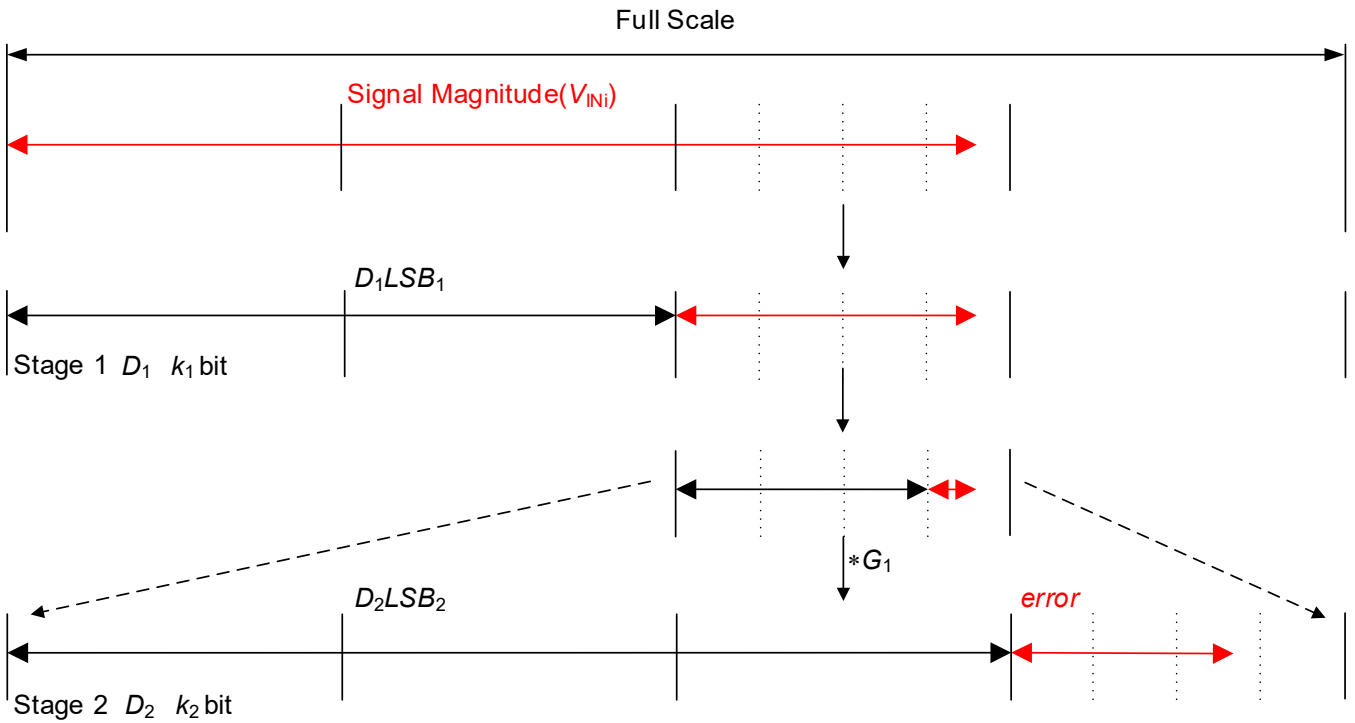


- A_{OUT} is the analog output of the ADC, *error* is the system quantization error

$$V_{IN} = A_{OUT} + error \qquad A_{OUT} = D_{OUT}LSB = \sum \frac{A_{OUTi}}{\prod_{n=1}^{i-1} G_n} = \sum \frac{D_i LSB_i}{\prod_{n=1}^{i-1} G_n} = \frac{D_1 LSB_1}{1} + \frac{D_2 LSB_2}{G_1}$$

Physical Model

- Digital Output



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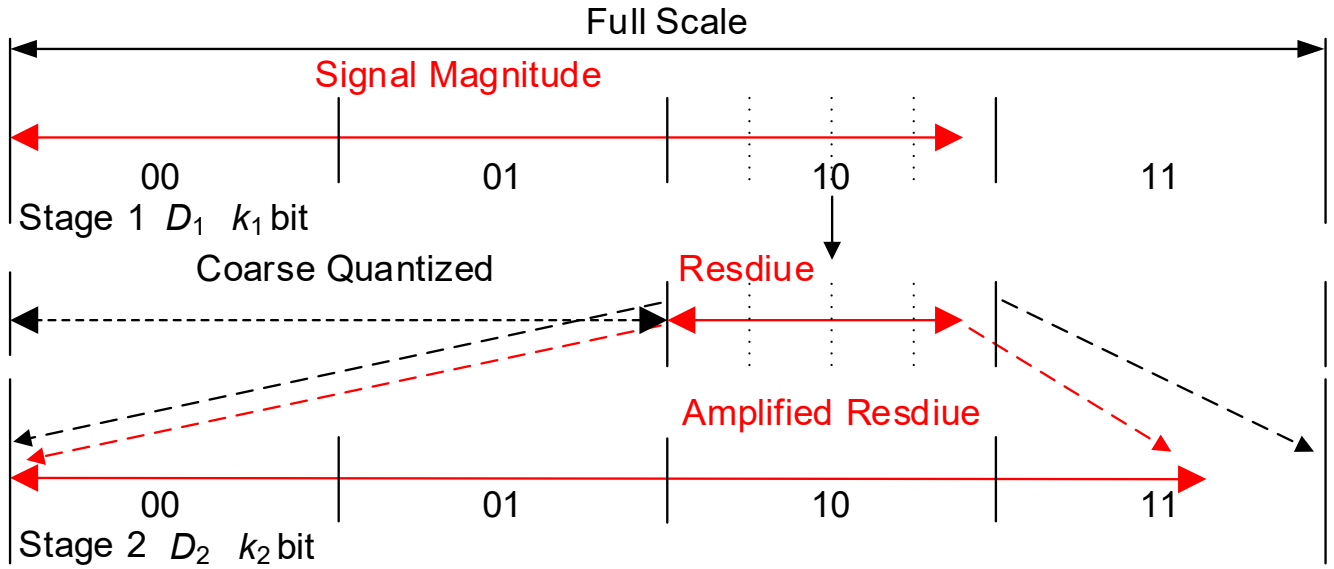
- Actually, A_{OUTi} is equal to V_{DACi}

Physical Model

- Digital Output

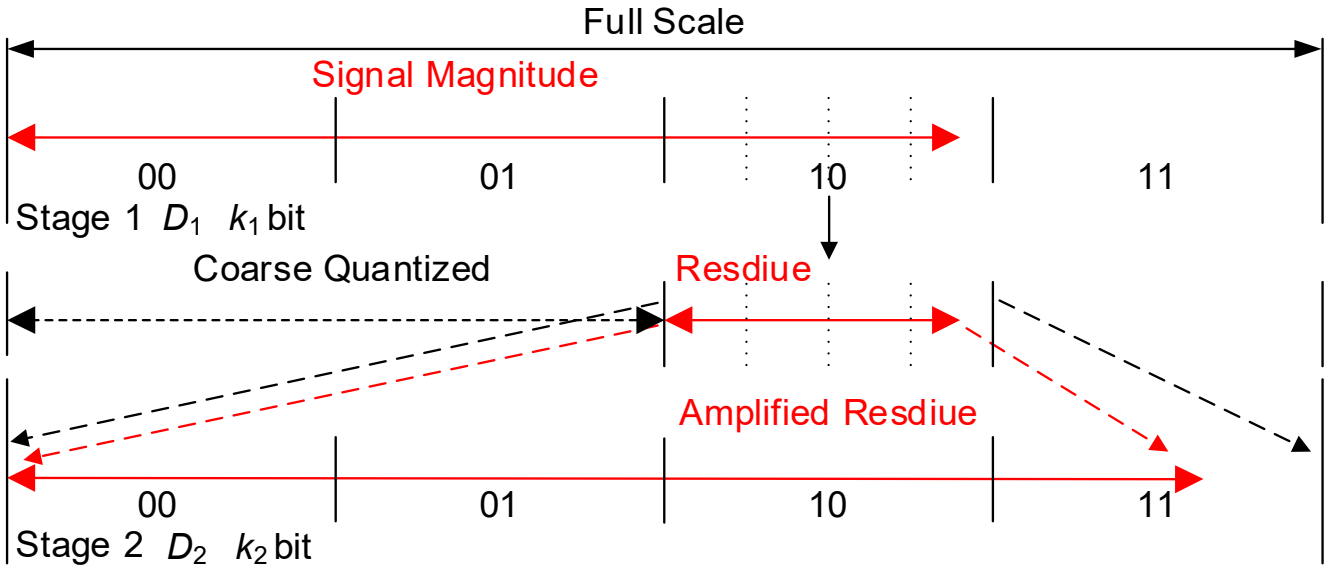


$$A_{OUT} = D_{OUT}LSB = \frac{D_1 LSB_1}{1} + \frac{D_2 LSB_2}{G_1} \qquad LSB_i = \frac{FS}{2^{k_i}}$$

$$A_{OUT} = D_1 \frac{FS}{2^{k_1}} + D_2 \underbrace{\frac{FS}{G_1 2^{k_2}}}_{LSB} = D_1 G_1 2^{k_2-k_1} LSB + D_2 LSB = (D_1 G_1 2^{k_2-k_1} + D_2) LSB$$

Physical Model

- Digital Output



$$A_{OUT} = D_{OUT}LSB = \frac{D_1 LSB_1}{1} + \frac{D_2 LSB_2}{G_1}$$

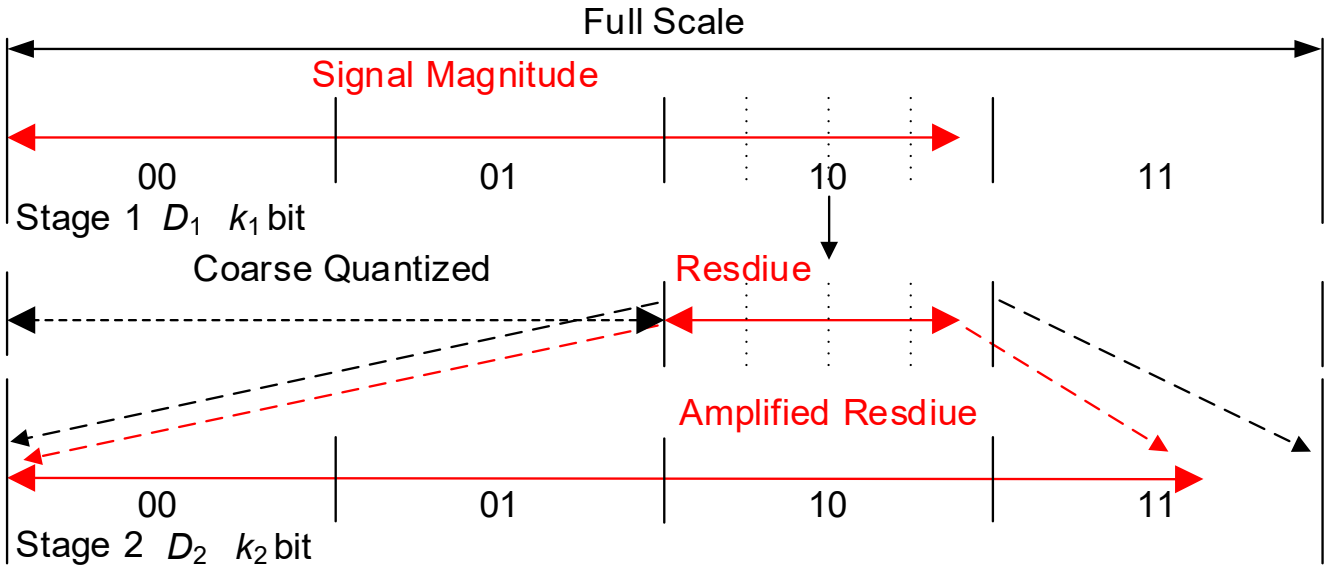
$$A_{OUT} = D_1 \frac{FS}{2^{k_1}} + D_2 \frac{FS}{G_1 2^{k_2}} = D_1 G_1 2^{k_2-k_1} LSB + D_2 LSB = (D_1 G_1 2^{k_2-k_1} + D_2)LSB$$

$$A_{OUT} = D_{OUT}LSB = (G_1 2^{k_2-k_1} D_1 + D_2)LSB$$

$$D_{OUT} = G_1 2^{k_2-k_1} D_1 + D_2$$

Physical Model

- Digital Output



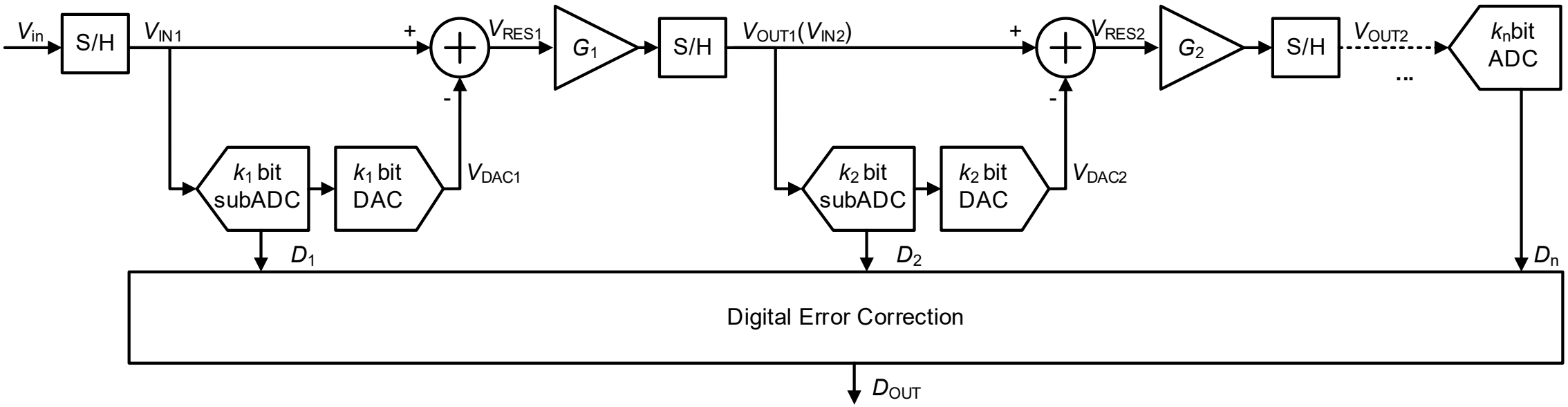
$$D_{OUT} = G_1 2^{k_2 - k_1} D_1 + D_2$$

$$G_1 = 2^{k_1} \quad D_{OUT} = 2^{k_2} D_1 + D_2$$

$$D_{OUT} = D_1 << k_2 + D_2$$

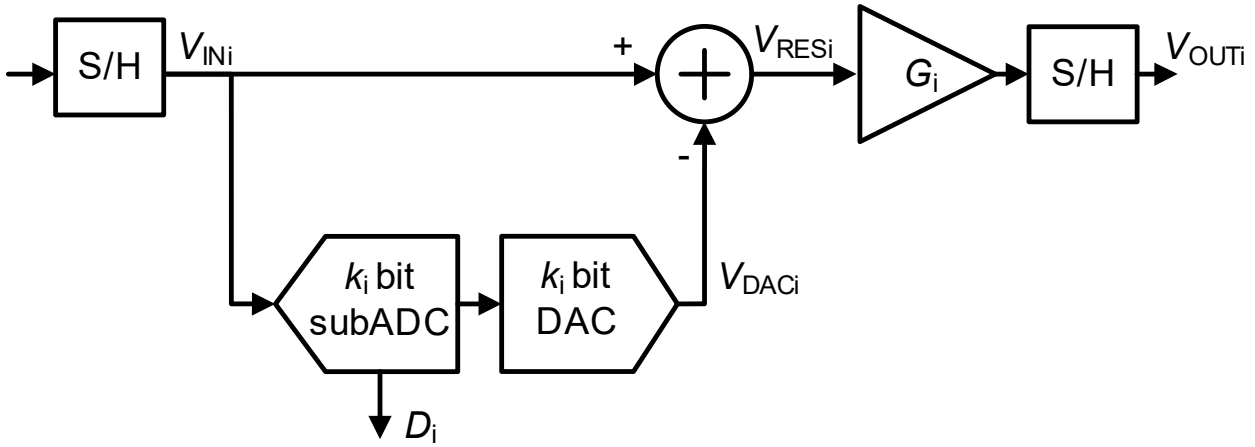
Stage 1: 10
Stage 2: 11
Output : 1011

Basic Pipelined ADC



Basic Pipelined ADC

- Differences between the Physical Model and the Actual Circuits



$$V_{OUTi} = G_i(V_{RESi}) = G_i(V_{INi} - V_{DACi}) = G_i(V_{INi} - D_i LSB_i) = G_i(V_{INi} - D_i \frac{V_{REF}}{2^{k_i - 1}})$$

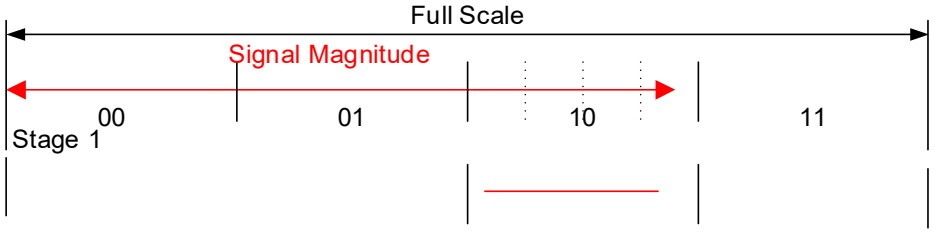
- In the circuits, the D_i in the formula is not equal to the digital output of the stage

Basic Pipelined ADC

- Differences between the Physical Model and the Actual Circuits

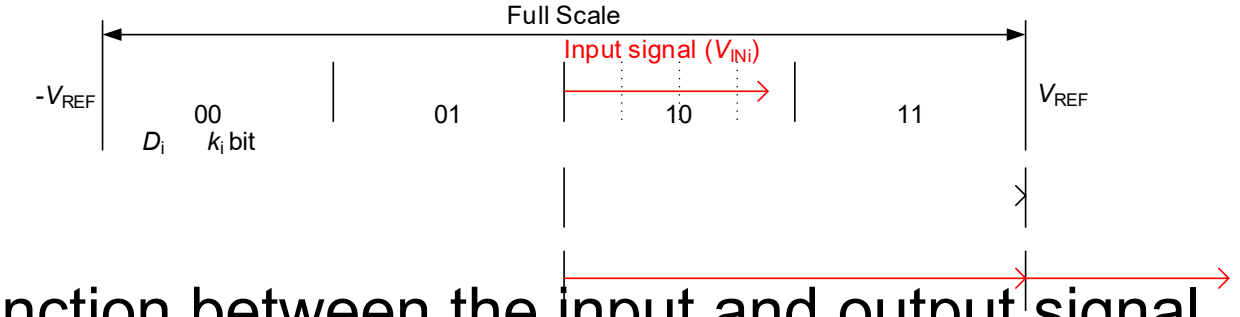
Physical Model:

- Magnitude from the lower border



Actual Circuits:

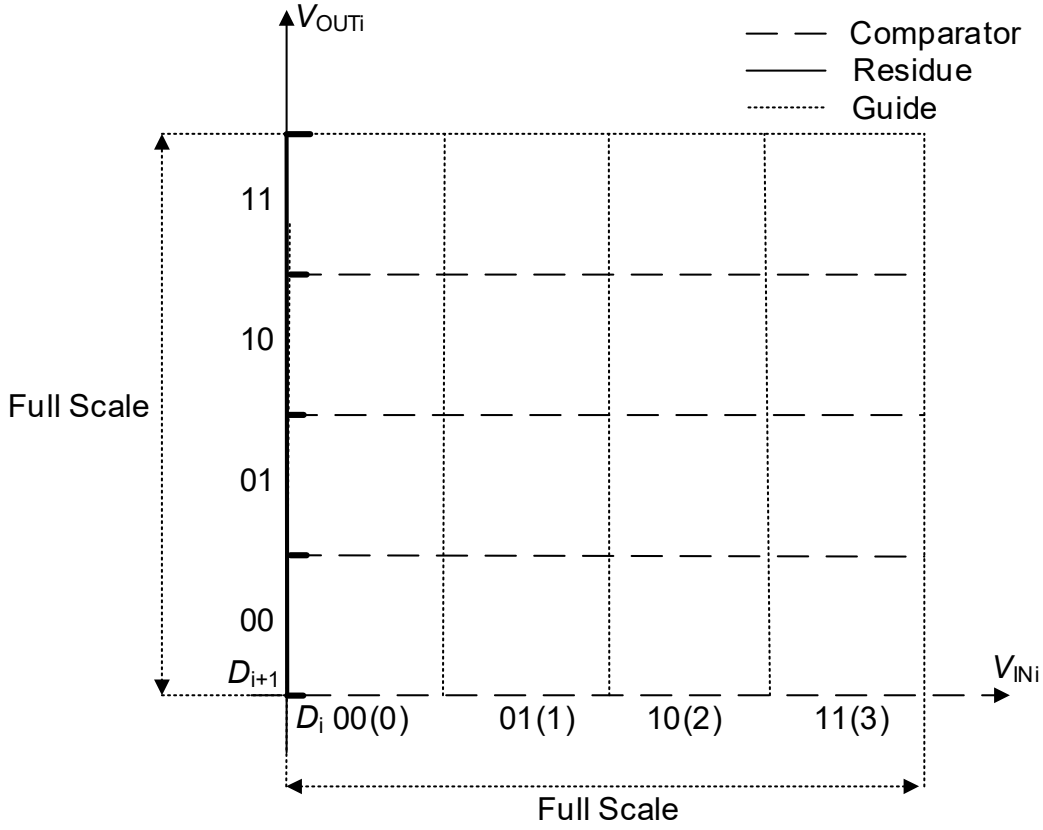
- Vector starting from the origin(zero)



- The key point is to build a bijection function between the input and output signal

Basic Pipelined ADC

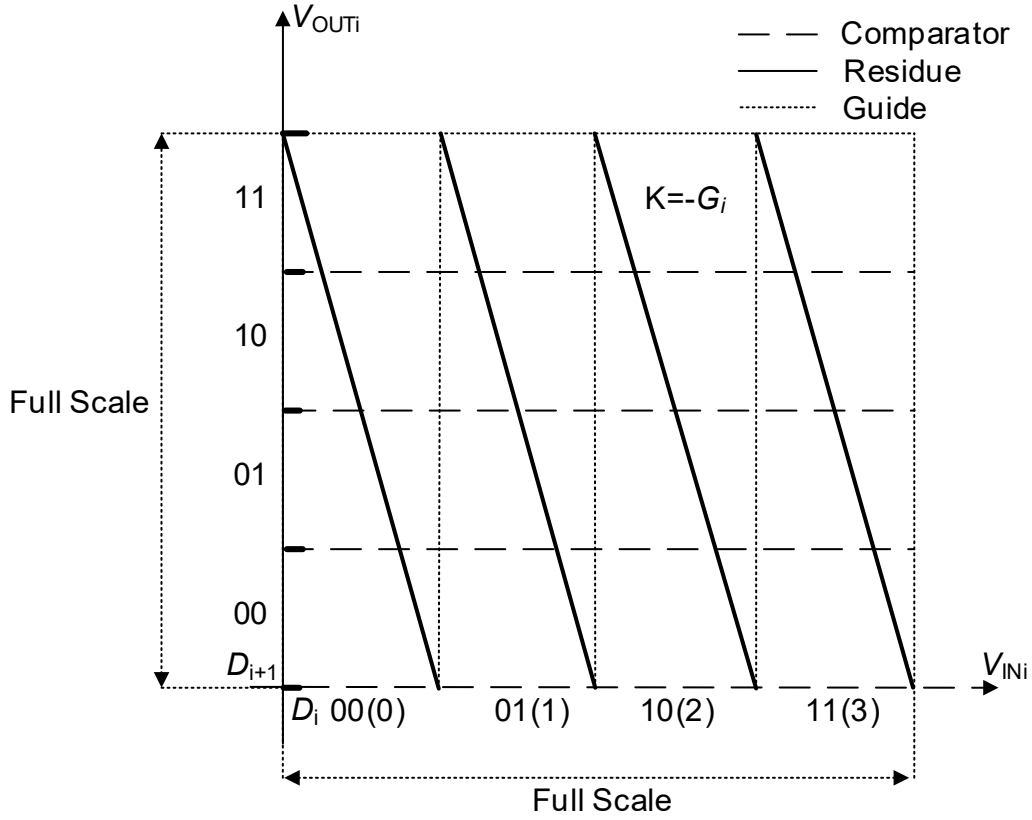
- The Requirements of the Transfer Waveform



- Sectional linear bijection function
- Output range is equal to input range

Basic Pipelined ADC

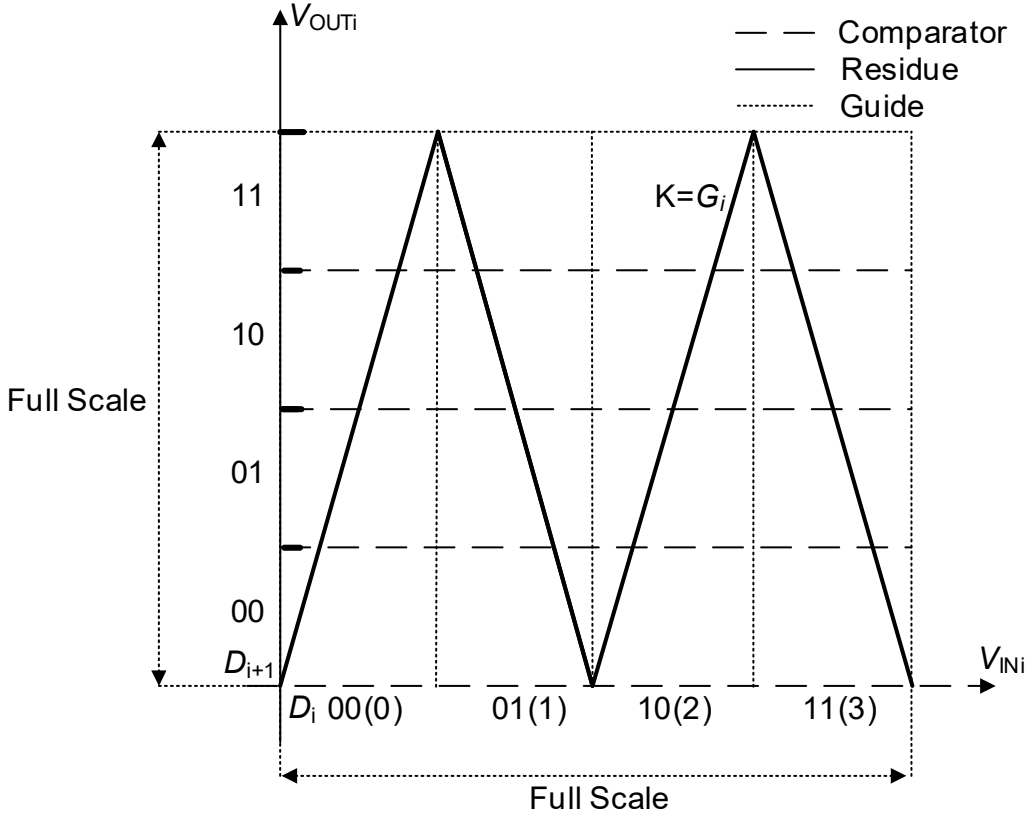
- Example 1



- The decoding is complex
- Voltage level changes more frequently

Basic Pipelined ADC

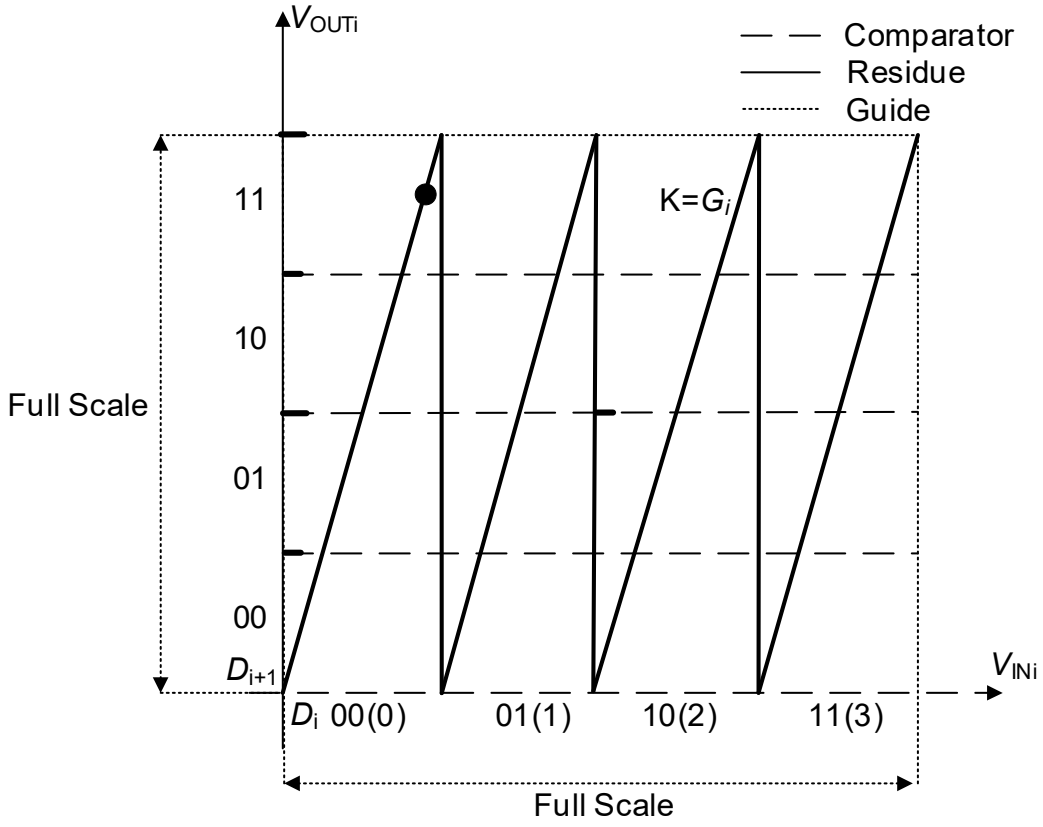
- Example 2



- Used in the folding ADC
- Unable to introduce the redundancy

Basic Pipelined ADC

- Example 3

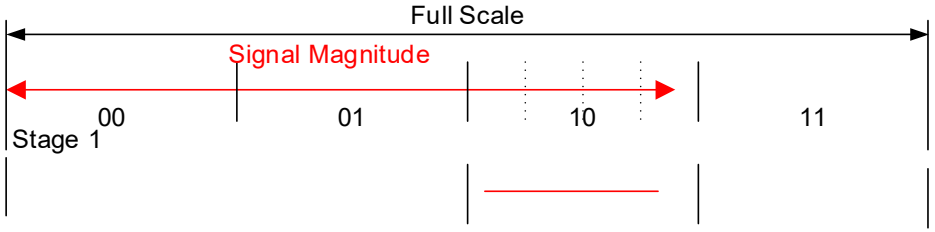


Basic Pipelined ADC

- Differences between the Physical Model and the Actual Circuits

Physical Model:

- Magnitude from the lower border



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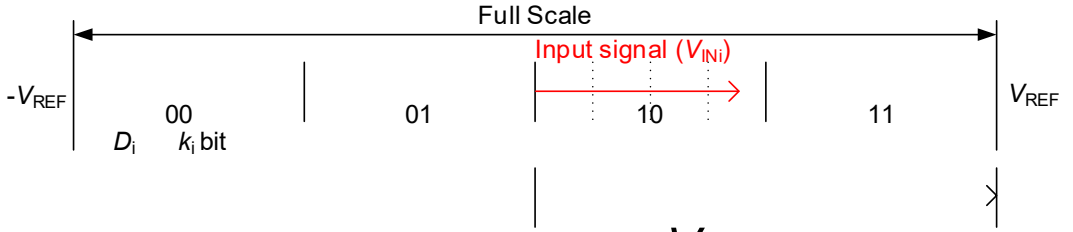
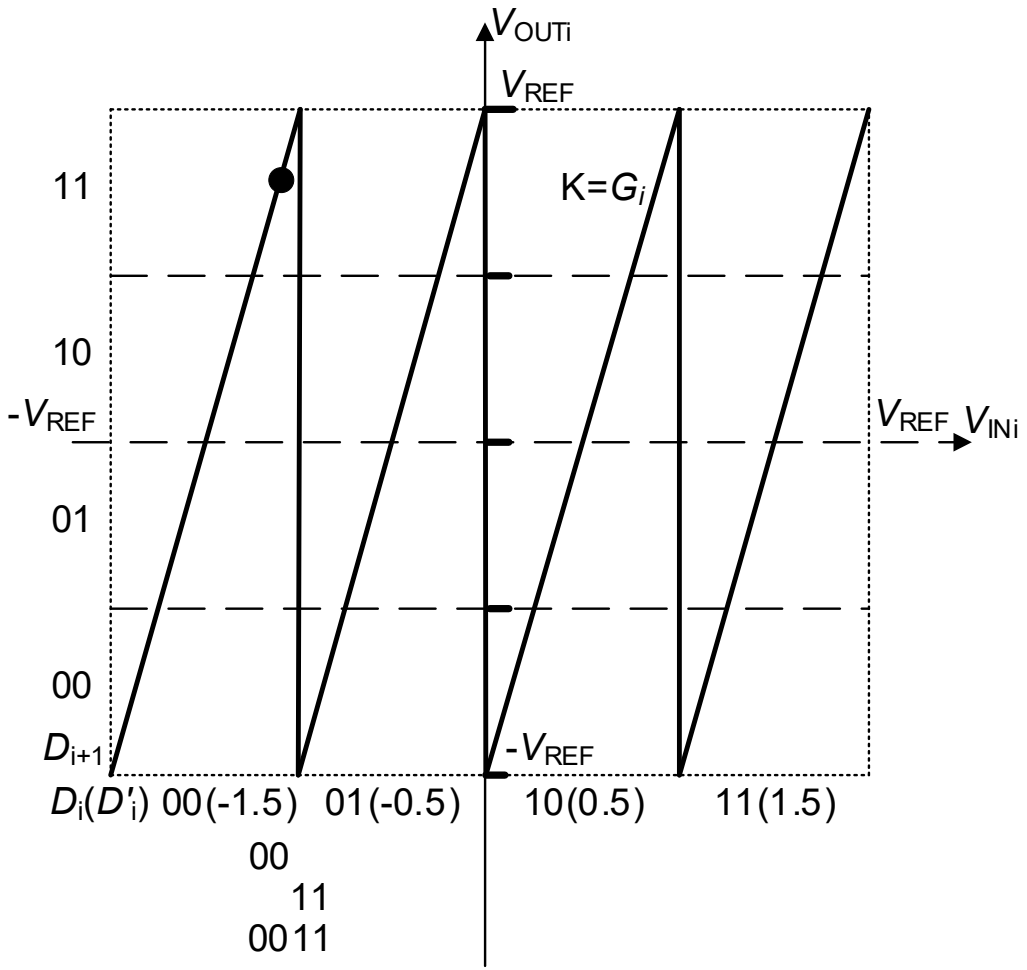


$$V_{OUTi} = G_i(V_{INi} - V_{DACi}) = G_i(V_{INi} - D'_i \frac{V_{REF}}{2^{k_i-1}}) = G_i(V_{INi} - D'_i LSB_i)$$

- In the formula, the D_i should be written as D'_i
- D'_i is used to calculate the residue, D_i is the digital output of the stage
- D'_i may not be equal to D_i , but should be one-to-one corresponding to D_i

Basic Pipelined ADC

- Math Expressions
  - According to two requirements of transfer waveform, we can get the new curve:

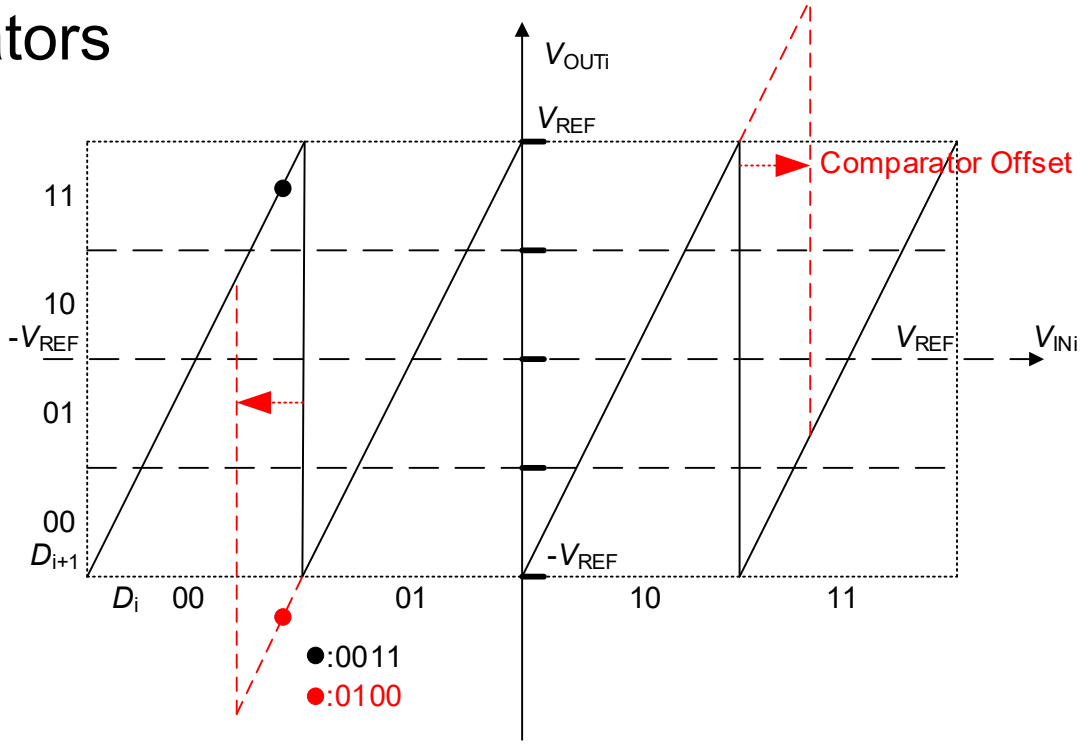


  - The formula:

$$V_{OUTi} = G_i(V_{INi} - V_{DACi}) = G_i(V_{INi} - D'_i \frac{V_{REF}}{2^{k_i-1}}) = G_i(V_{INi} - D'_i LSB_i)$$

Redundancy and Digital Error Correction

- Mismatch of Comparators

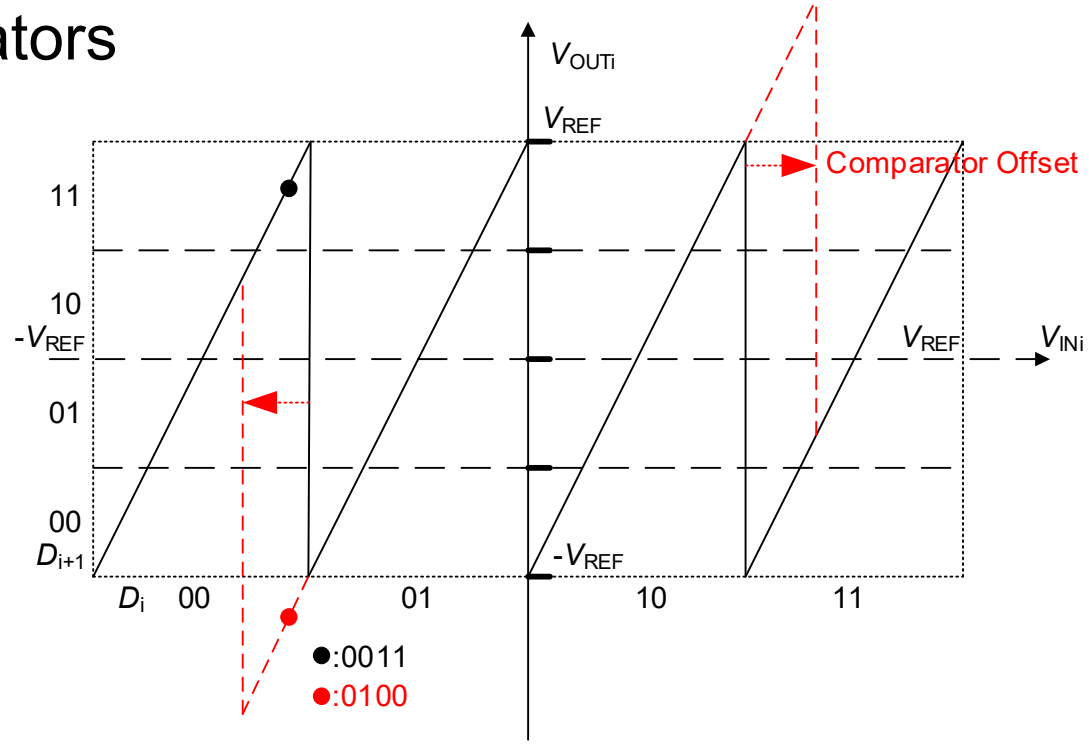


$$V_{OUT1} = 4(V_{IN1} - D'_1 LSB_1)$$

$$V_{OUT2} = 4(V_{OUT1} - D'_2 LSB_2)$$

Redundancy and Digital Error Correction

- Mismatch of Comparators



●: $V_{OUT2} = 16V_{IN1} - 16D'_1 LSB_1 - 4D'_2 LSB_2$

●: $V^*_{OUT2} = 16V_{IN1} - 16(D'_1+1)LSB_1 - 4(D'_2 - 3)LSB_2 = V_{OUT2} - 4LSB_2$

●: $D_{OUT} = 4D_1 + D_2$

●: $D^*_{OUT} = 4(D_1 + 1) + (D_2 - 3) = D_{OUT} + 1$

Redundancy and Digital Error Correction

- Problems Caused by the Mismatch
  - Amplified residue is out of the input range
  - Mismatch causes the error in the digital output and the next stage input

Redundancy and Digital Error Correction

- Solutions
  - Reduce the inter-stage gain and bring the redundancy
  - Correct the error in the digital output so the present output is right
  - Correct the next stage input so the later output is right

Redundancy and Digital Error Correction

- Solutions
  - Reduce the inter-stage gain and bring the redundancy
  - Correct the error in the digital output so the present output is right
  - Correct the next stage input so the later output is right
    - It can be proved that the next stage input is right when the digital output is right

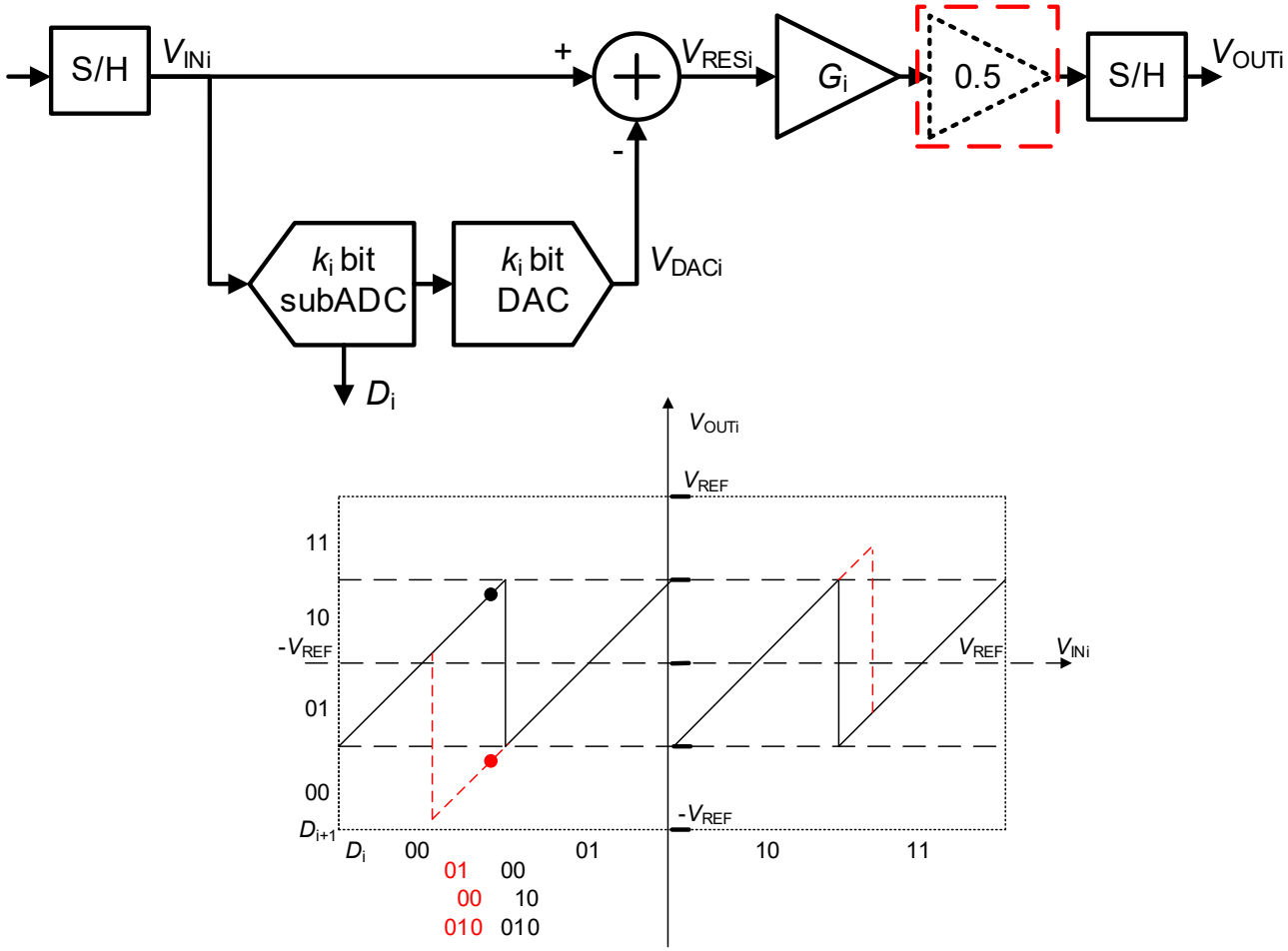
$$
\begin{aligned}
V_{OUT2} &= G_2(V_{IN2} - D'_2 LSB_2) \\
&= G_2(G_1 V_{IN1} - G_1 D'_1 LSB_1 - D'_2 LSB_2) \\
&= G_2\left[G_1 V_{IN1} - (G_1 2^{k_2 - k_1} D'_1 - D'_2) LSB_2\right] \\
&= G_2(G_1 V_{IN1} - D'_{OUT} LSB_2)
\end{aligned}
$$

Redundancy and Digital Error Correction

- Solutions
  - Reduce the inter-stage gain and bring the redundancy into residue
  - Correct the error in the digital output so the present output is right
  - Correct the next stage input so the later output is right
    - It can be proved that the next stage input is right when the digital output is right
    - In the following chapter, the analysis will only discuss about the digital error correction algorithm's effect on the digital output

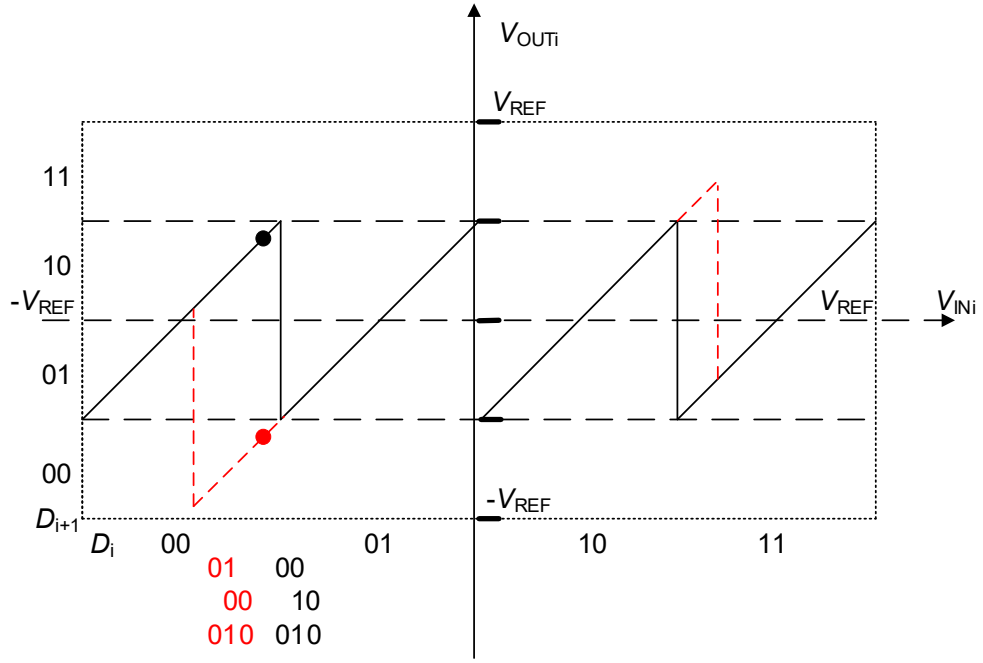
Redundancy and Digital Error Correction

- Reduce the Inter-stage Gain



Redundancy and Digital Error Correction

- Digital Output of the Pipelined ADC with Redundancy



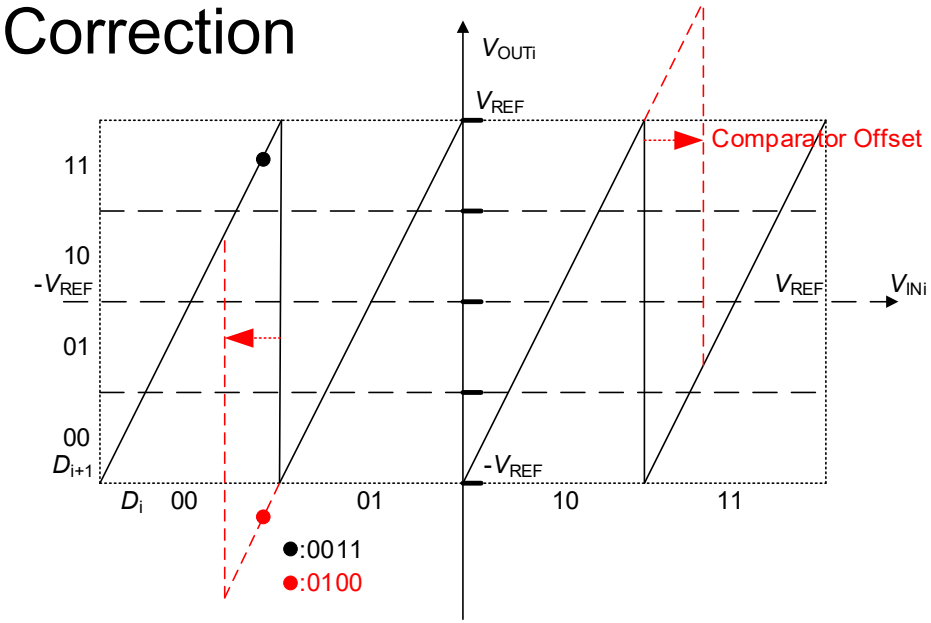
$$V_{OUTi} = G_i(V_{INi} - V_{DACi}) \qquad G_1 = 2^{k_i - 1}$$

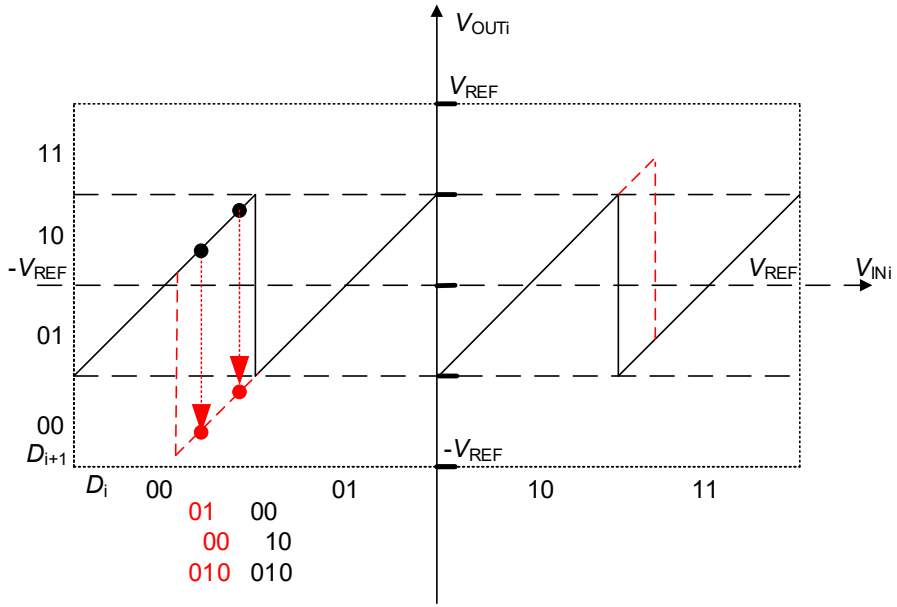
$$D_{OUT} = G_1 2^{k_2 - k_1} D_1 + D_2 = 2^{k_2 - 1} D_1 + D_2 = D_1 << (k_2 - 1) + D_2$$

1 bit overlap

Redundancy and Digital Error Correction

- Error Correction





$$V_{IN2} = V_{OUT1} = 4(V_{IN1} - D'_1 LSB_1)$$

$$D^*_1 = D_1 + 1 \rightarrow V^*_{IN2} = V_{IN2} - 4LSB_1 \rightarrow D^*_2 = D_2 - 3$$

$$D_{OUT} = 4D_1 + D_2$$

$$D^*_{OUT} = 4(D_1 + 1) + (D_2 - 3) = D_{OUT} + 1$$

$$V_{IN2} = V_{OUT1} = 2(V_{IN1} - D'_1 LSB_1)$$

$$D^*_1 = D_1 + 1 \rightarrow V^*_{IN2} = V_{IN2} - 2LSB_1 \rightarrow D^*_2 = D_2 - 2$$

$$D_{OUT} = 2D_1 + D_2$$

$$D^*_{OUT} = 2(D_1 + 1) + (D_2 - 2) = D_{OUT}$$

Redundancy and Digital Error Correction

- Key Points in the Correction
    - Digital output change can be fully detected
    - The weights ratio of digital output and its variation are intrinsically opposite

Redundancy and Digital Error Correction

- Key Points in the Correction
  - Digital output change can be fully detected
  - The weights ratio of digital output and its variation are intrinsically opposite

$$V_{INi+1} = V_{OUTi} = G_i(V_{INi} - D'_i LSB_i)$$

$$\Delta D_1 \rightarrow \Delta V_{IN2} = -G_1 LSB_1 \Delta D_1 \rightarrow \Delta D_2 = \frac{\Delta V_{IN2}}{LSB_2}$$

$$\Delta D_2 = \frac{\Delta V_{IN2}}{LSB_2} = -\frac{G_1 LSB_1}{LSB_2}\Delta D_1 = -G_1 2^{k_2 - k_1}\Delta D_1 = -W_{12}\Delta D_1$$

Redundancy and Digital Error Correction

- Key Points in the Correction
  - Digital output change can be fully detected
  - The weights ratio of digital output and its variation are intrinsically opposite

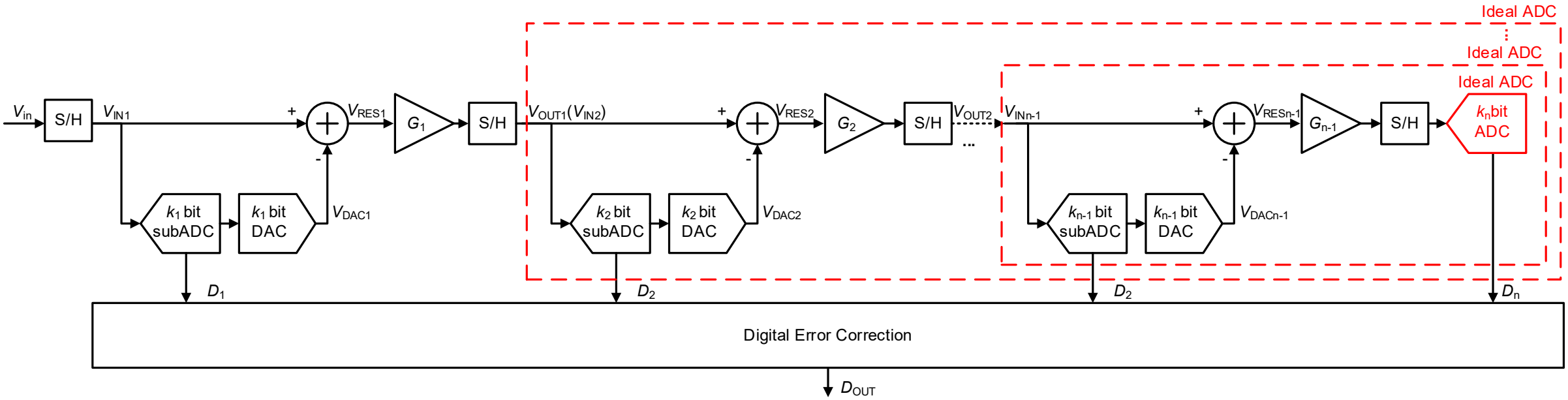
$$\Delta D_2 = -W_{12}\Delta D_1$$

$$D_{OUT} = G_1 2^{k_2-k_1} D_1 + D_2 = W_{12} D_1 + D_2$$

$$\begin{aligned} D^*_{OUT} &= W_{12}(D_1 + \Delta D_1) + (D_2 + \Delta D_2) \\ &= W_{12} D_1 + D_2 + (W_{12}\Delta D_1 + \Delta D_2) \\ &= W_{12} D_1 + D_2 + (W_{12}\Delta D_1 - W_{12}\Delta D_1) \\ &= D_{OUT} \end{aligned}$$

Redundancy and Digital Error Correction

- Key Points: Recursive Thought



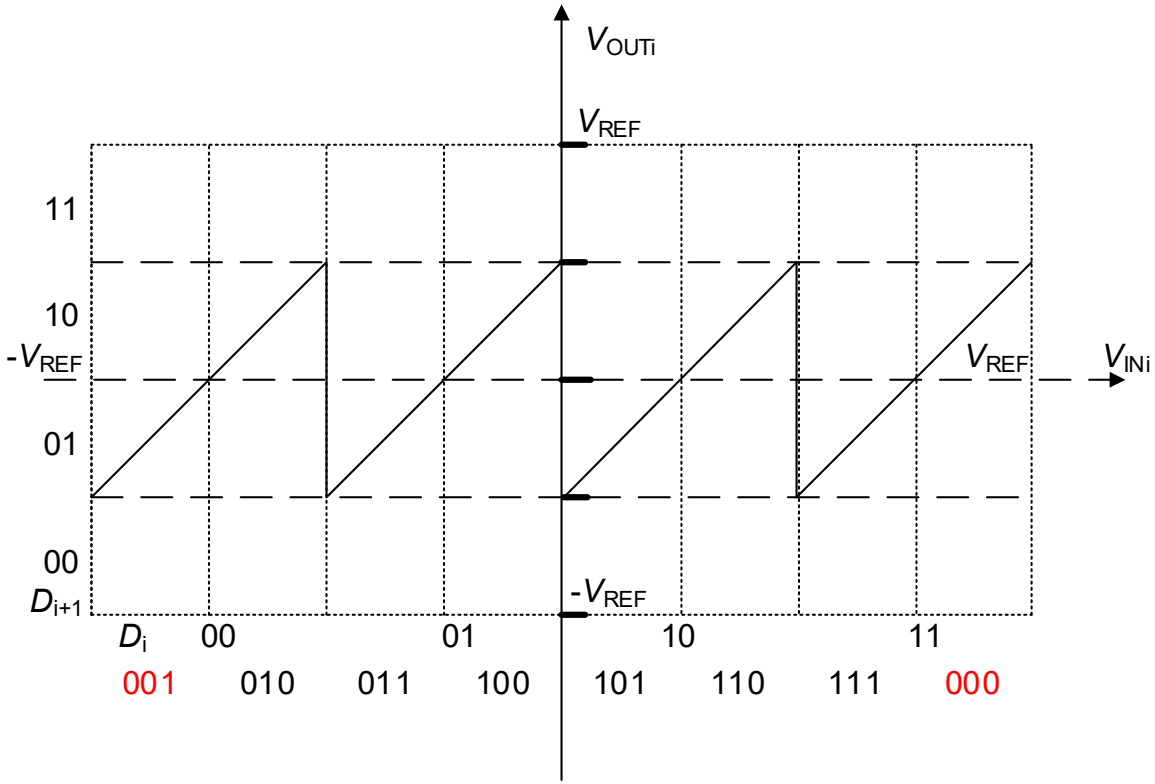
- Though the algorithm is discussed under the circumstance that there is no offset in the next stage's comparators, the algorithm remains feasible when the final stage is without or with little mismatch.

Comparator Offset and Digital Output

- Problems
  - Zero-cross comparator are sensitive to the noise (chatter)
  - The digital output has offset

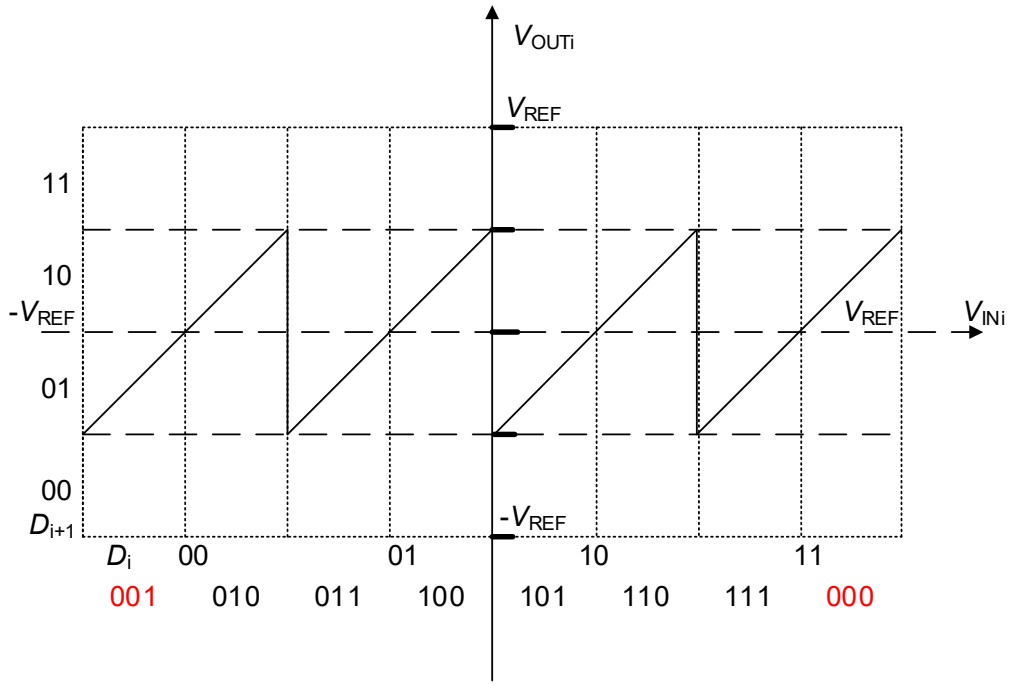
Comparator Offset and Digital Output

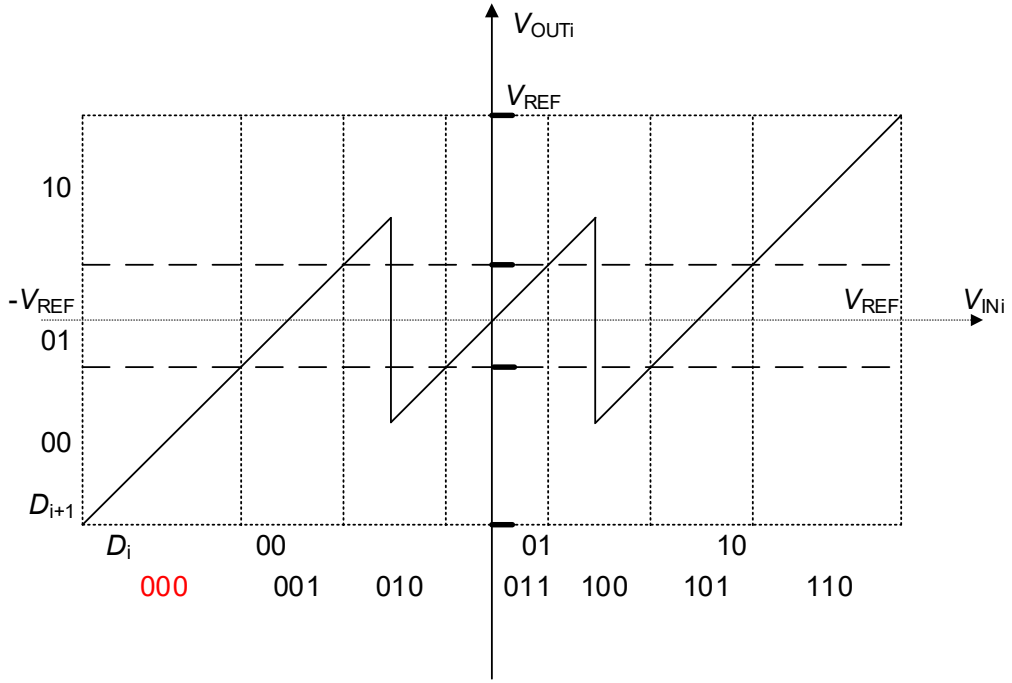
- Digital Output Offset



Comparator Offset and Digital Output

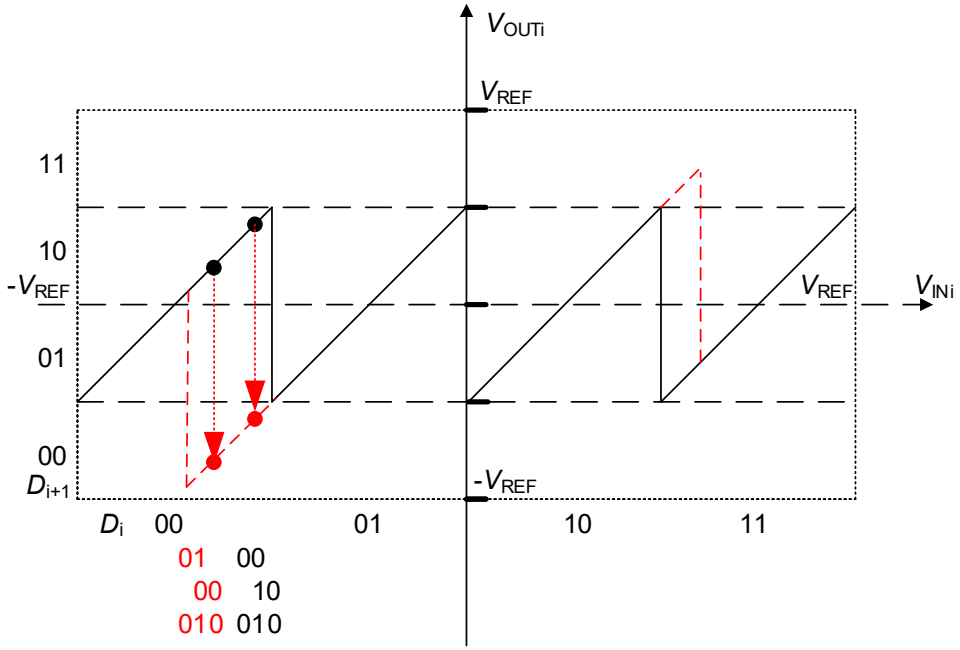
- Offset Introduced to All Comparators

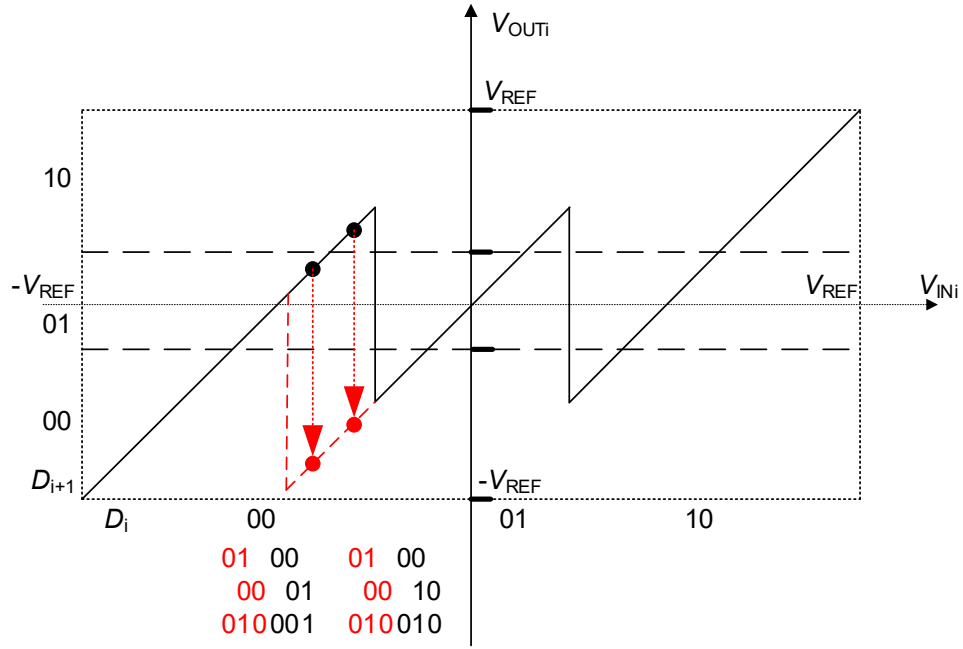




Comparator Offset and Digital Output

- Error Correction





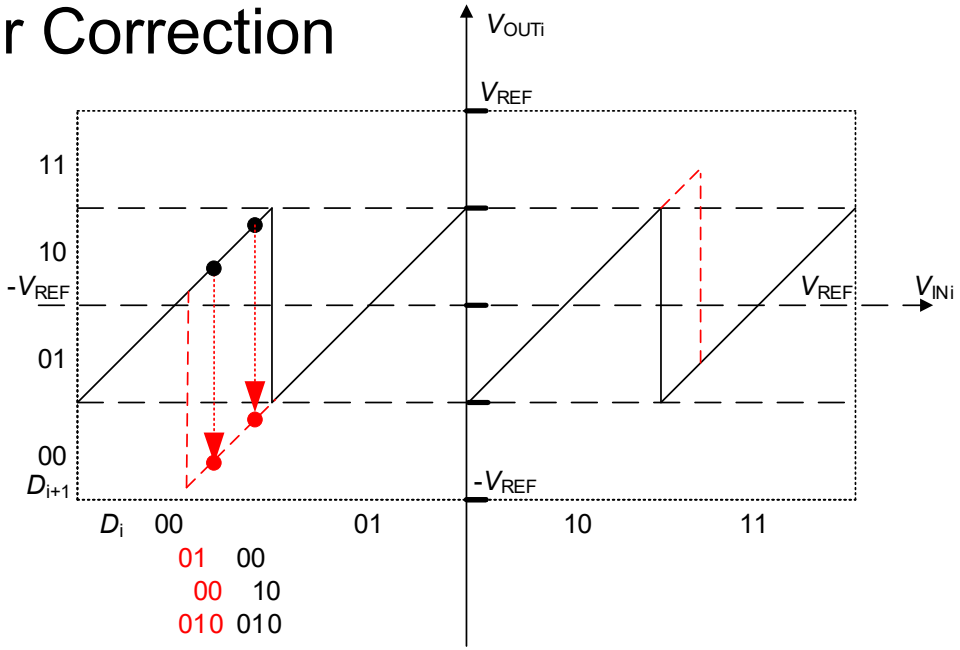
- The correction algorithm remains valid but some of the error are not fully detected (the arrow on the left only cross 1 comparators line instead of 2)

Comparator Offset and Digital Output

- Key Points in the Correction
    - Digital output change can be fully detected
    - The weights ratio of digital output and its variation are intrinsically opposite

Comparator Offset and Digital Output

- Error Correction

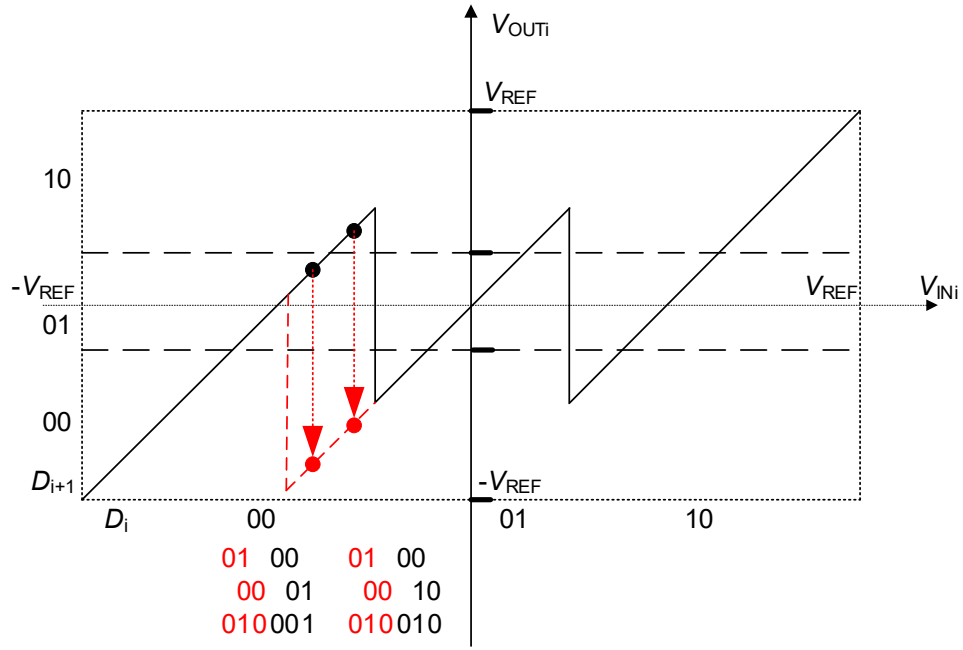


$$V_{IN2} = V_{OUT1} = 2(V_{IN1} - D'_1 LSB_1)$$

$$D^*_1 = D_1 + 1 \rightarrow V^*_{IN2} = V_{IN2} - 2LSB_1 \rightarrow D^*_2 = D_2 - 2$$

$$D_{OUT} = 2D_1 + D_2$$

$$D^*_{OUT} = 2(D_1 + 1) + (D_2 - 2) = D_{OUT}$$



$$V_{IN2} = V_{OUT1} = 2(V_{IN1} - D'_1 LSB_1)$$

$$D^*_1 = D_1 + 1 \rightarrow V^*_{IN2} = V_{IN2} - 2LSB_1 \rightarrow D^*_2 = D_2 - 1$$

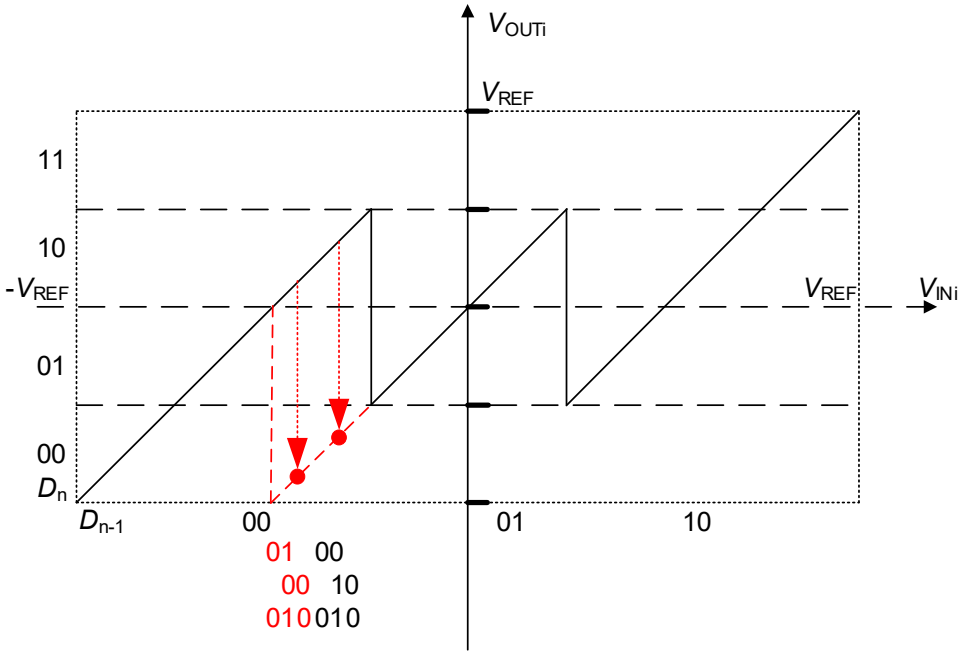
$$D_{OUT} = 2D_1 + D_2$$

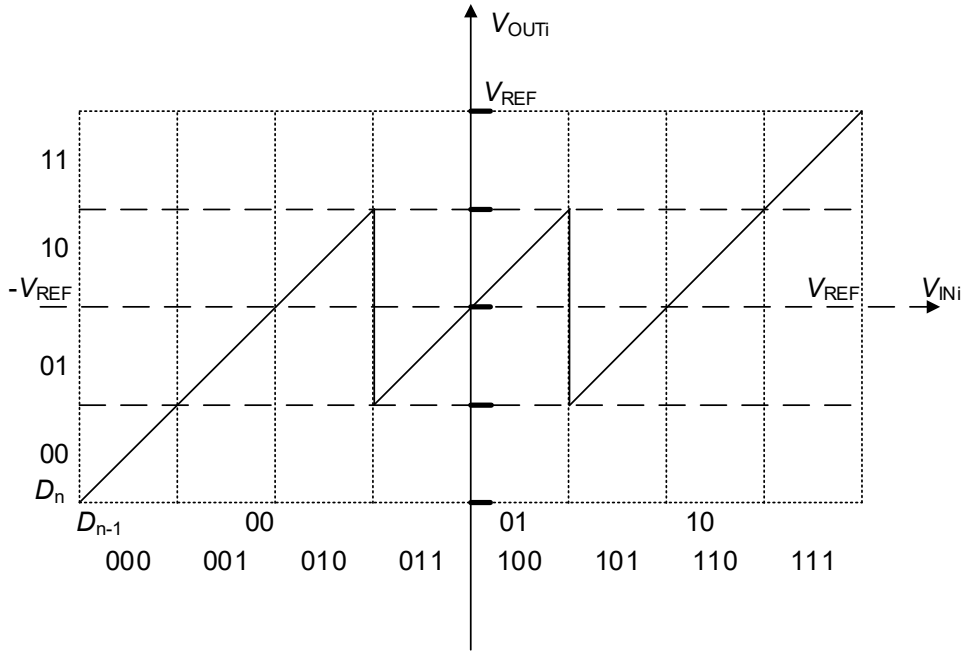
$$D^*_{OUT} = 2(D_1 + 1) + (D_2 - 1) = D_{OUT} - 1$$

- Error can't be corrected immediately

Comparator Offset and Digital Output

- Error Correction

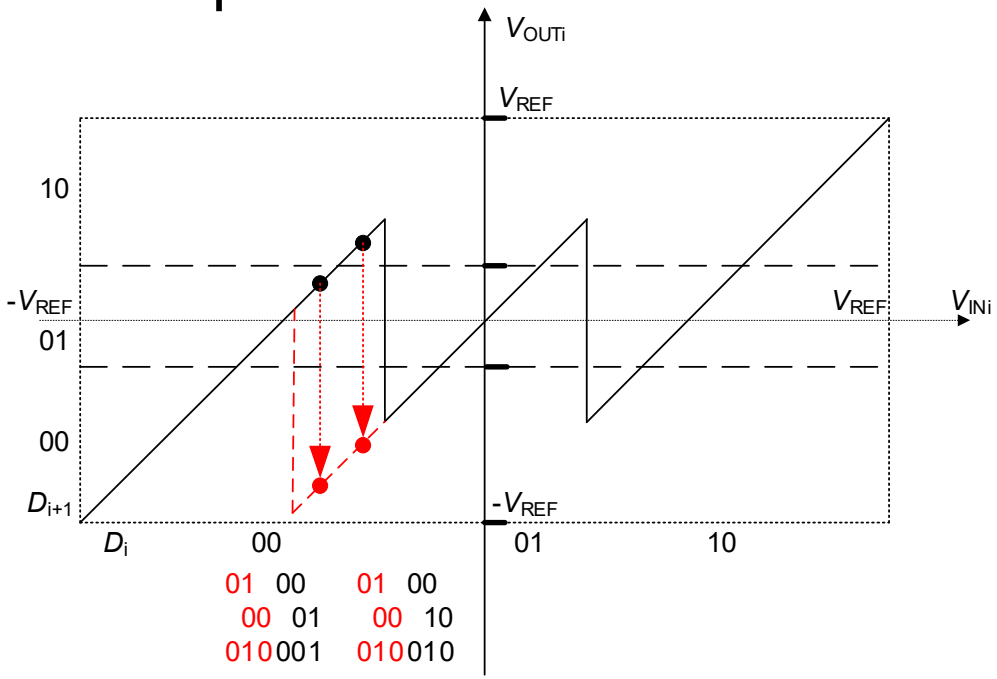


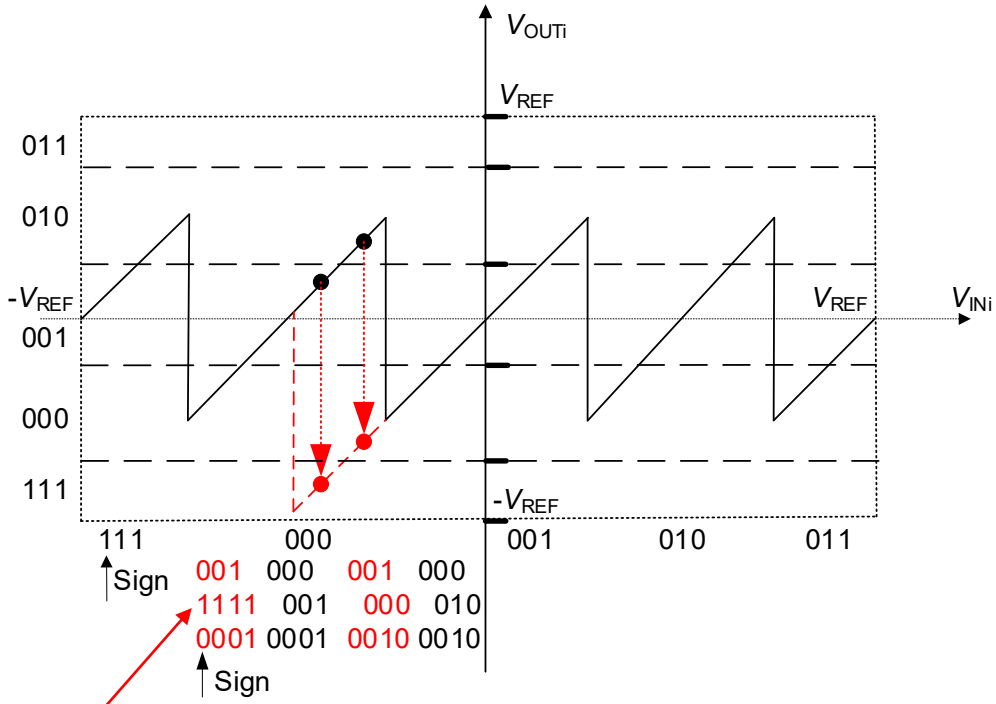


- Generally, the final stage(stage n) is a zero-cross flash comparator and the error of the previous stage (stage n-1) can be fully corrected. The stage n-1 and stage n can be regard as an ideal zero-cross flash together so all the previous error can be corrected (recursive thought) .

Comparator Offset and Digital Output

- Add a Comparator



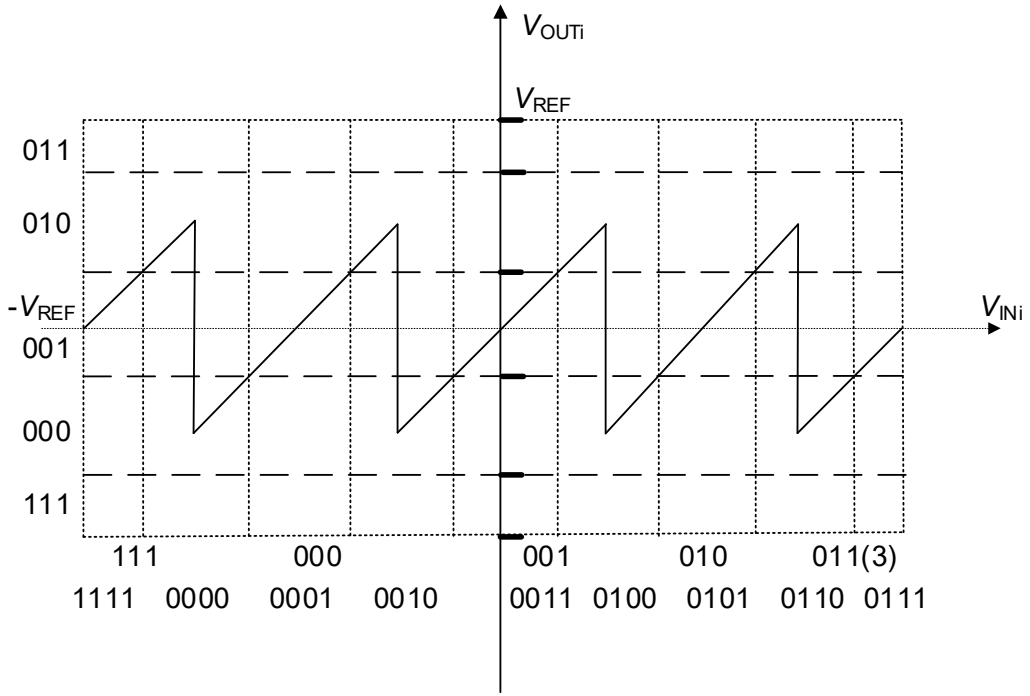


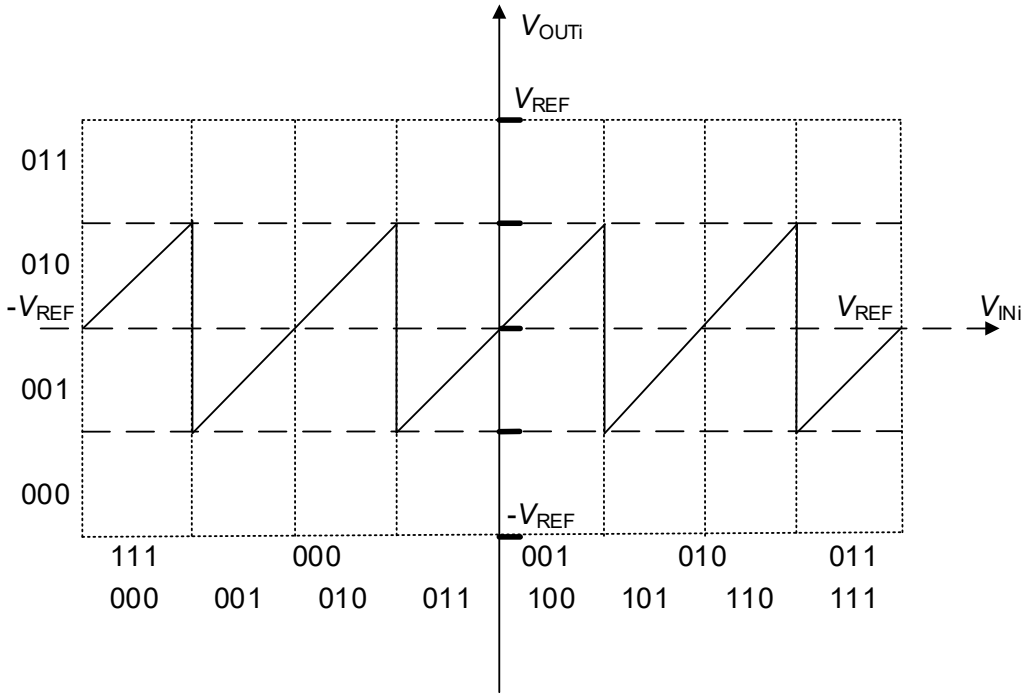
- Should be 1111(-1) instead of 0111(7)

- Error can't be corrected immediately
- Error can be corrected immediately

Comparator Offset and Digital Output

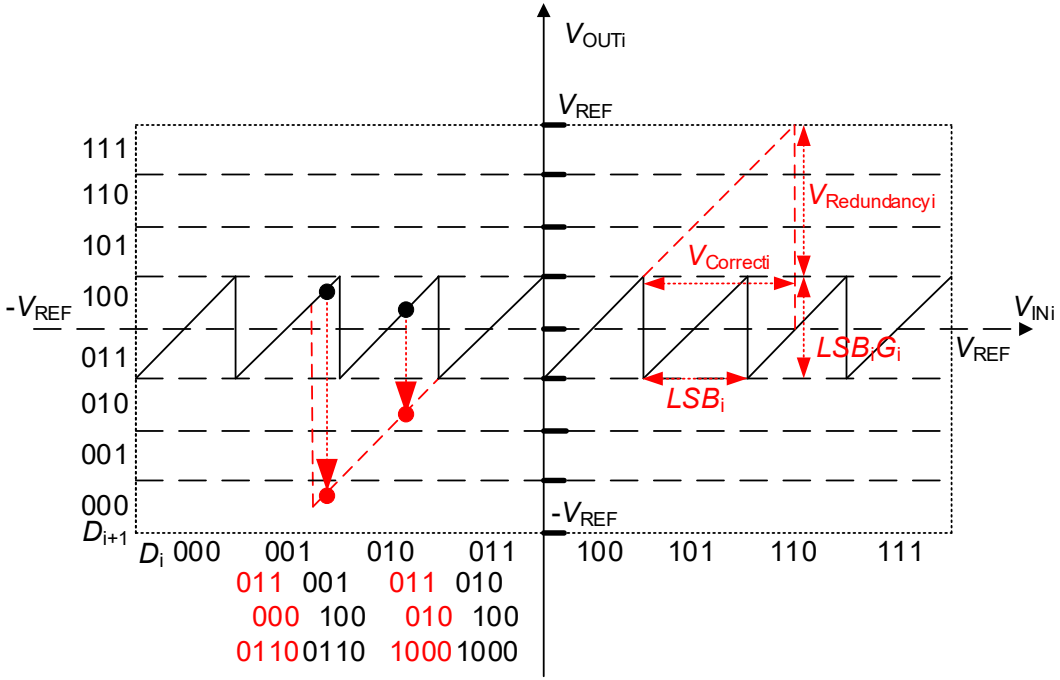
- No Digital Output Offset

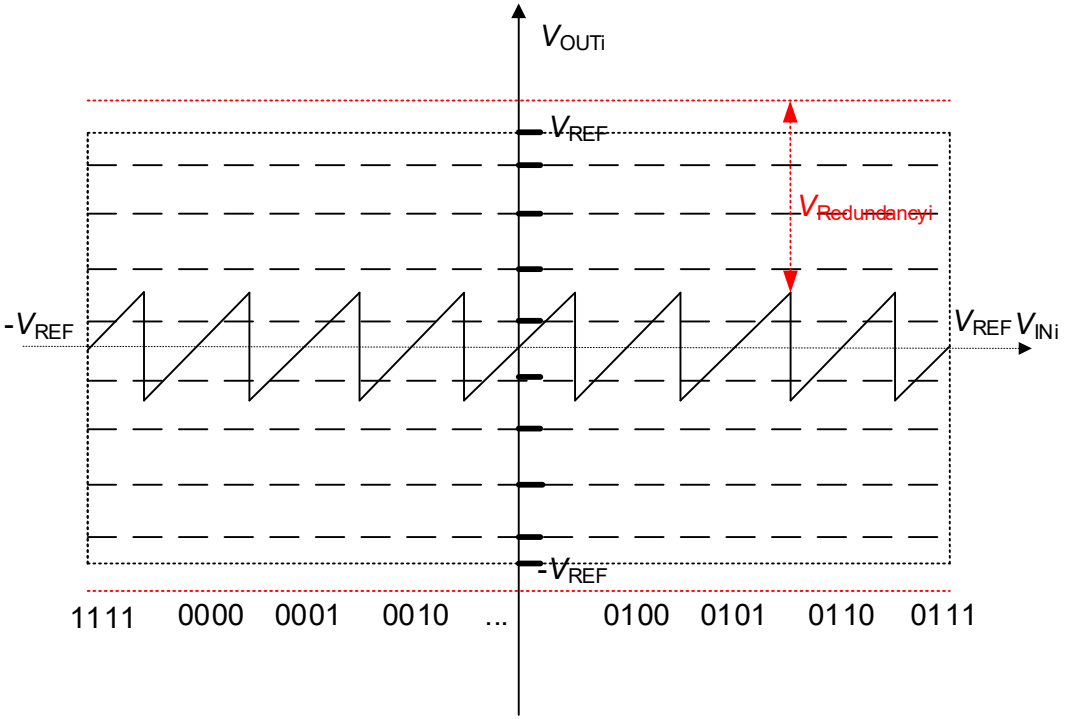




Redundancy and Digital Error Correction

- The Correction Range (Tolerable Mismatch)
  - Example of a 3 bit stage with 2 bit overlap $k_i = 3 \quad G_1 = 2^{k_i - 2}$

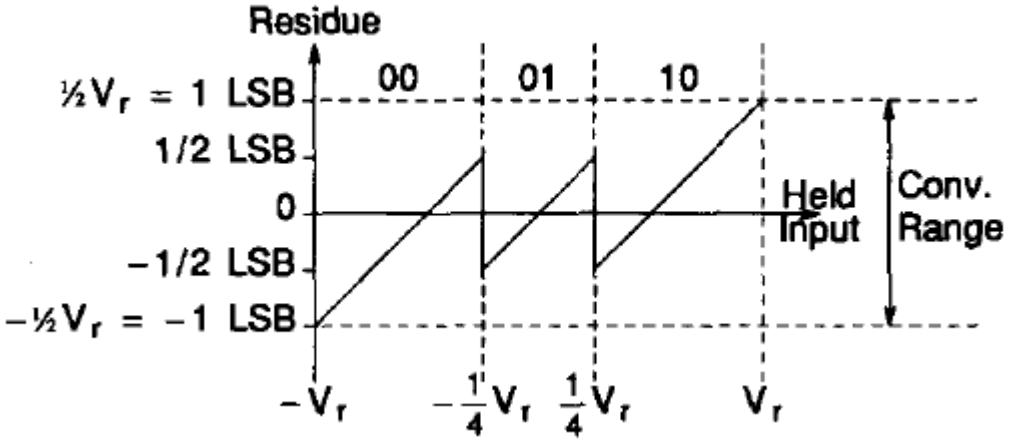




$$V_{Correcti} = V_{Redundancyi} / G_i$$

Redundancy and Digital Error Correction

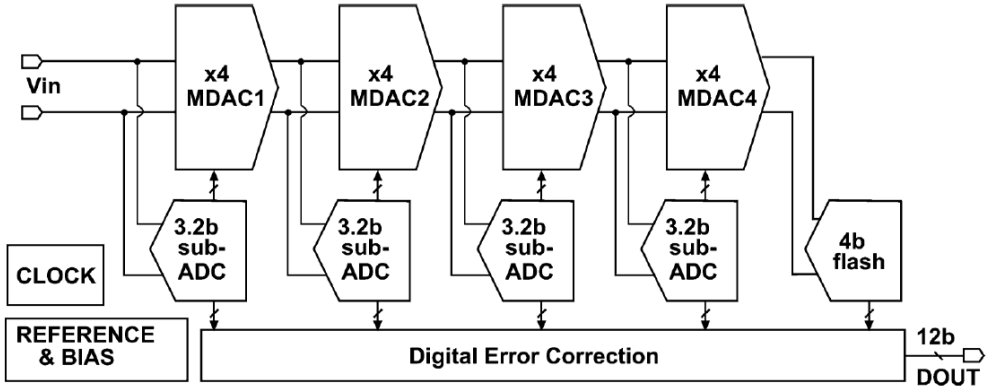
- 1.5 bit ?



$2^n - 2$ comparators. As a result, the resolution of each stage except the last is $\log_2(2^n - 1)$ bits. If $n = 2$ b, as in this example, the resolution per stage is about 1.5 b,

$\log_2(2^2-1)=1.58$ (bit)

[1] S. H. Lewis, H. S. Fetterman, G. F. Gross, R. Ramachandran and T. R. Viswanathan, "A 10-b 20-Msample/s analog-to-digital converter," in IEEE Journal of Solid-State Circuits, vol. 27, no. 3, pp. 351-358, March 1992.



The first stage is composed of a 3.2 bit sub-ADC (eight comparators) and an MDAC with gain of 4. Each of the subsequent stages is scaled down by a factor of 2 relative to the preceding

$\log_2(2^3+1)=3.16$ (bit)

[2] S. Shin et al., "A 12 bit 200 MS/s Zero-Crossing-Based Pipelined ADC With Early Sub-ADC Decision and Output Residue Background Calibration," in IEEE Journal of Solid-State Circuits, vol. 49, no. 6, pp. 1366-1382, June 2014.

Thanks for Your Attention