Pengyu Zeng

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EDUCATION

Wuhan University **Wuhan, China**

Bachelor of Science in Electronic Information Engineering *Sept. 2019 – June 2023*

- **GPA & Scores:** 3.85/4.00 (91/100); TOEFL:106
- **Selected Awards:** Mitacs Globalink Research Award (Awarded to top students worldwide to do research in Canada), Beacon-fire Scholarship (2%), First-class Scholarship of Wuhan University (5%), Merit Student of Wuhan University (5%)
- **Relevant Coursework:** Analog Circuits, Digital Circuits, Communication Electronic Circuits, Methods of Mathematical Physics, Signals and Systems, Probability and Statistics, Stochastic Progress, Electromagnetic Field Theory

RESEARCH INTERESTS

- Compute In-memory (Architecture, circuits and software co-design), Analog and Mixed-signal Circuits, Hardware Security

RESEARCH EXPERIENCE

University of Notre Dame, Advisor: Prof. Ningyuan Cao **South Bend, IN**

Summer Research Intern (In-person), **Unified Compute-In-Memory and PUF Based on 8T SRAM** *June 2022 – Aug. 2022*

- Build the model of 2T array based CIM, and analyzed the impact of the nonidealities (including Early Effect, process variation and noise) on the performance (linearity, variation, resolution) of CIM:
  - Established the relationship between the internal parameters (discharge current, output range, etc.) and external designed parameters (V_{WL}, V_{DD}, etc.).
  - Early Effect causes same mismatch for all columns while the process variation leads to the different mismatch from column to column. Calibration can be used to reduce the mismatch.
  - Process variation also results in the variation in the output, which can be defined as static noise. The average power of the thermal noise (dynamic noise) is unchanged in arrays with different rows. SNR is used to estimate the precision of CIM. Trade-off is found between the precision and area.
- Calculated the entropy and Bit Error Rate (BER) to evaluate the randomness and robustness of PUF
  - Voltage droop and discharge time can be used as the output of PUF.
  - Systematic process variation and noise will degrade the performance of PUF. Changing the parameters of PUF (discharge current, voltage droop, etc.) can increase the performance.
- Modeled the process variation and temperature variation in a die with MATLAB

Fudan University, Advisor: Prof. Zhangwen Tang **Shanghai, China**

Research Assistant, **The Error Correction Analysis and Agile Design in the Pipelined ADC** *Sept. 2021 – Jan. 2022*

- Made systematic analysis in the digital error correction algorithm of the pipelined ADC, which is fundamental but is not explained clearly in the related publications. My work answers following questions: why this algorithm can correct error caused by the offset and aperture error? why the output resolutions are .5 bits and added up with overlap? why all the threshold voltages are designed with 1/2 LSB offset
  - Established the function and the transfer waveform of the input signal and residue signal
  - Used the function to analyze the digital output error and prove that the error correction algorithm is valid because the ratio of two adjacent stage's output is inherently opposite to the ratio of output errors caused by comparators mismatch
  - Explained the non-integer bits and the operation of overlap-add between two adjacent outputs by establishing the function of the input signal and quantized signal
  - Made a comparison among three kinds of structures with different transfer characteristics in the ability of noise tolerance, error correction range and output offset
- Built a behavioral model of the pipelined ADC with MATLAB to accelerate the design process
  - Designed a model with variable parameters in Op-amp and MDAC to verify the error correction and calibration algorithm
  - Added changeable noise (reference voltage noise, amplifier noise, etc.) and mismatch (capacitor mismatch, comparator offset, etc.) to analyze the impact of nonidealities on the performance of the ADC
  - Proposed Monte Carlo Simulation to get more comprehensive simulation results of ENOB, SNR, SFDR, etc.

Tsinghua University, School of Integrated Circuits, Advisor: Prof. Ziqiang Wang **Beijing, China**

Summer Research Intern (In-person), **A 40Gb/s CTLE for a PAM4 Wireline Receiver** *June 2021 – July 2021*

- Drew the schematic and layout in a 65nm CMOS process, finished DRC/LVS/PEX and post-simulation on Cadence Virtuoso
- Adopted variable-controlling method to improve the performance of the CTLE and find the tradeoff among peaking gain, DC gain and power dissipation. Small model of MOSFET and frequency domain analysis is used.
- Used MATLAB to verify the nonideal characteristic of the bode diagram with different zeros and poles

PUBLICATIONS

- J. Liu, B. Cheng, **P. Zeng**, S. Davis, M. Chang and N. Cao, "Privacy-by-Sensing with Time-domain Differentially-Private Compressed Sensing", in submission to *Design, Automation, and Test in Europe (DATE)*, Apr. 2023.
- F. Shao and **P. Zeng**, "Urban Waterlogging Monitoring System Based on LoRa Technology," to appear at *International Conference on Computer, Communication, Control, Automation and Robotics (CCCAR)*, Mar. 2022.