Soumya Ranjan Dash

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EDUCATION

University of Pennsylvania, *School of Engineering and Applied Science* **May '24**

Master of Science in Engineering: Electrical Engineering, GPA: 3.13/4 (Till 2nd sem)

NIST Berhampur, *Department of Electronics & Communication Engineering* **June '22**

Bachelor of Technology: Electronics & Communication Engineering, GPA: 8.76/10.00

SKILLS

Language: C/C++, Verilog, SystemVerilog, UVM, HLS, Python, VHDL, Spark, Perl, Matlab, HTML, CSS, SQL
Software/Tools: Synopsys VCS & Verdi, QuestaSim, Xilinx Vitis, Vivado, Cadence Virtuoso, Vim, VSCode, Unix, Windows
Industry Standards: AMBA4 (AXI, AHB, APB), Ethernet, SPI, I2C, UART

COURSEWORK

Completed: Digital VLSI Design, Networks & Protocols, Computer Architecture, Datacenter Architecture, Big Data Analytics, SystemVerilog for UVM, Verification with UVM, Embedded Systems, Ongoing: SystemC Basics, TLM, & Synthesis, SoC Design & Verification

WORK EXPERIENCE {For More}

Mack Institute - The Wharton School, *Autoware Research Assistant (Part-time), Philadelphia, PA* **Sept '23 – present**

- Utilized Python with REST/GraphQL APIs to collect from GitHub and prepare or organize data using SQL, etc. after extraction, applied visualizations using Matplotlib, Seaborn etc. to highlight current trends to enable data-driven insights in innovation management.

Seagate Technology, *VLSI Digital Read Channel Design & Verification Intern (Full-time), Longmont, CO* **May '23 – Aug '23**

- Collaborated with Seagate's Read Channel IP Development team and led the development process of a VIP for AXI Master module from the ground up capable of concurrent-asynchronous Read/Write and Brust Transfer to multiple DRAM Clients
- Architected and developed all the UVCs keeping scalable, reusable with SystemVerilog & UVM methodology in a UNIX environment using Synopsys VCS verdi tool, meanwhile implemented a coverage model, and learned the Digital Read Channel SoC architecture.

VLSI Lab – NIST, *Undergraduate Research Assistant (Part-time), Berhampur, India* **Mar '21 – Aug '22**

- Worked on the FPGA implementation of Brain-inspired Deep Neural Networks followed by Functional verification, & Physical Design.

SELECTED PROJECTS {For more}

Ethernet MAC and 10BASE-T PHY RTL Design and Verification **Sept '23 – Ongoing**

- Developing a custom Ethernet MAC and 10BASE-T PHY in Verilog for an FPGA, implementing IEEE 802.3 standards with CRC error Checks.
- Using Vivado for Synthesis, QuestaSim for functional verification and crafting complex UVCs using SystemVerilog and UVM methodology.

Boot Security and Real-Time Communication Optimization for an Electronic Trading System SoC **Sept '23 – Ongoing**

- Boot image validation, enhanced system security with performance analysis, and identification of bottlenecks using HLS C in Xilinx Vitis.
- Optimizing IPC communication between Cortex-A9 and MicroBlaze PP on Zynq-7000 SoC, reducing latency in RTOS-based data transfer.

HLS-based RV32I Multi-Core RISC-V FPGA Processor Modelling and Validation **Aug '23 – Ongoing**

- Validation of RV32I instruction cores in multi-core RISC-V with multihart pipelines & Cores using HLS in C/C++, with FPGA implementation.
- Proficient utilization of Xilinx Vitis, Vivado, RISC-V Spike Tools, and AXI interconnections for high performance and optimization.

Scalable AXI4 Master VIP with SystemVerilog in QuestaSim **July '23 – Sept '23**

- Built a VIP for AXI3 using the Mentor Questa tool that's scalable for AXI4 and interfaces to multiple Slaves RTL designed by Verilog.
- Created UVCs to verify all types of Brust Transfers & Cache support, Out of Order, Overlapping transactions and SV Assertions & Coverage.

Building a Robust UVM-based Verification IP for Router's RTL Design **May '23 – June '23**

- Led Cadence Xcelium-based verification IP development with UVM with automation features,multichannel Sequencers etc.
- Orchestrated integration of UVCs, employing scoreboard with TLM imp connectors for verification and functional coverage analysis.

Design Verification of a 16-bit Pipelined Superscalar LC4 Processor **Jan '23 – May '23**

- Designed and verified a processor in Verilog, optimizing pipelines to meet a 66 MHz timing, addressing hazards and bottlenecks.
- Tested design on Xilinx Zynq 7000 SoC using Vivado after 5-stage pipeline verification at the block/subsystem/System level.

Design and verification of CLBs of a 16x1 MUX for FPGA with energy-delay optimization **Nov '22 – Dec '22**

- Created a CLB block having LUTs containing 16X1 MUX, DRAM, DFF, FIFO etc. with AMI 0.60u C5N technology in Cadence virtuoso.
- Achieved a frequency of 64.935MHz,load energy of 3.006nj,active energy of 3.28nJ, CLB area of 230nm^2, and 'FOM' of 1.15*10^-23 m^2sJ.

Accelerator - Digital Systems for Spiking Neural Network emulation using Verilog **Feb '22 – June '22**

- Constructed an SNN accelerator with an Izikevich Neuron, STDP training and AER communication, along with RAM-based weight storage.
- Tested pattern recognition workload followed by optimization through model adaptations in Vivado for deployment on an Artix-7 FPGA.