Soumya Ranjan Dash

dsoumya@seas.upenn.edu • (267) 249-4750 • www.linkedin.com/in/srd00

EDUCATION

University of Pennsylvania, *School of Engineering and Applied Science* **Aug '22 - May '24 [Expected]**
- MS in Electrical Engineering (ASIC/SoC Design Verification, Distributed Computing), GPA - Ongoing

NIST Berhampur, *Department of Electronics & Communication Engineering* **Aug '18 - June '22**
- Bachelors of Technology in Electronics & Communication Engineering, GPA - 3.5/4.0

SKILLS

Distributed Computing: Data Centers, Spark, Big Data, AWS, Networks & Protocols (HTTP, DNS, TCP/IP, Ethernet, Routing, Security),ASICs
Big Data Analytics: Data Mining, EDA, ETL, Data Visualization, REST APIs, Machine Learning, Deep Learning, Spark, Statistics
Operating Systems: Windows, Linux, Unix, Ubuntu
Language: Verilog, SystemVerilog, UVM, C/C++, Python, Matlab, HTML & CSS, Bootstrap, Python, SQL
Software/Tools: AWS, Oracle VM VirtualBox, Synopsys VCS & Verdi, QuestaSim, Xilinx Vitis & Vivado, Cadence Virtuoso
Industry Standards: AMBA4 (AXI, AHB, APB), Ethernet, SPI, I2C, UART

COURSEWORK

Big Data Analytics, Data Center, Networks & Protocols, Digital VLSI, Computer Architecture, Embedded Systems, MEMS & NEMS Devices

WORK EXPERIENCE { *For More* }

Mack Institute - The Wharton School, *Data Research Assistant (Part-time), Philadelphia, PA* **Sept '23 – present**
- Utilized APIs to extract data from GitHub, Managed Databases using Python, SQL & worked with other firms for more data insights.

Seagate Technology, *VLSI Digital Read Channel(SoC) Design & Verification Intern (Full-time), Longmont, CO* **May '23 – Aug '23**
- Collaborated with RTL designers of the Read Channel IP team, led the development of a VIP(Unit Level) that located >5 RTL Bugs for AXI Master module from scratch capable of concurrent Read/Write & Incrementing Burst Transfer to multiple DRAM Clients.
- Architected and developed all the UVCs keeping scalable, reusable with SystemVerilog & UVM in UNIX platform using Synopsys VCS verdi after reading design specification, implemented a coverage model, learned about DRC SoC Architecture & regression tests.
- Documented project architecture & development, given monthly code review presentation with annotated code, Slides, & report.

VLSI Lab – NIST, *Undergraduate Research Assistant (Part-time), Berhampur, India* **Mar '21 – Aug '22**
- Worked on the RTL Synthesis, Functional verification, & Physical Design of Brain-inspired Deep Neural Networks(BbNN, SNN etc.).

SELECTED PROJECTS { *For More* }

HLS-based RV32I Multi-Core RISC-V Processor Modelling & Validation **Aug '23 – Oct '23**
- Validated RV32I instruction cores in multi-core RISC-V with multihart pipelines & Cores using HLS in C/C++, with FPGA implementation.
- Utilized by Xilinx Vitis, Vivado, RISC-V Spike Tools, & AXI interconnect supporting Cache coherency for high performance & optimization.

Scalable AXI4 Master VIP with SystemVerilog(SV)-UVM in QuestaSim **July '23 – Sept '23**
- Built a SV UVM Based VIP for AXI3 using the QuestaSim that's scalable for AXI4 and interfaces to Slave RTL designed by Verilog.
- Created UVCs to verify Brust Transfers & Cache support, Out of Order, Overlapping transactions and SV Assertions with 40% Coverage.

Building a Robust UVM-based Verification IP for Router's RTL Design **May '23 – June '23**
- Led Cadence Xcelium-based verification IP development with UVM with automation features,multichannel Sequencers etc.
- Orchestrated integration of UVCs, employing scoreboard with TLM imp connectors for verification and achieved functional coverage 30%.

Design Verification of a 16-bit Pipelined Superscalar LC4 RISC Processor **Jan '23 – May '23**
- Designed and verified a processor in Verilog, Optimizing pipelines to meet a 66 MHz timing, addressing hazards and bottlenecks.
- Synthesized the design on Xilinx Zynq 7000 SoC in Vivado after 5-stage pipelined superscalar verification at Unit/subsystem/System level.

Design and verification of CLBs of a 16x1 MUX for FPGA with energy-delay optimization **Nov '22 – Dec '22**
- Created a CLB block having LUTs containing 16X1 MUX, DRAM, DFF, FIFO etc. with AMI 0.60u C5N technology in Cadence virtuoso.
- Achieved a frequency of 64.935MHz,load energy of 3.006nj,active energy of 3.28nJ, CLB area of 230nm^2, and 'FOM' of 1.15*10^-23 m^2sJ.

Interactive Customer Experience System - DinoPlay **Oct '22 – Dec '22**
- Crafted & integrated systems: DinoPlay for gaming, MoveDetect for human motion recognition, and ChatBot for interactive engagement
- Included VGA display with Pico's PIO, OpenCV for motion detection, ST7735 LCD & mono enclosed speaker to enrich user experience.

Accelerator - Digital Systems for Spiking Neural Network emulation using Verilog **Feb '22 – June '22**
- Constructed an SNN accelerator with an Izikevich Neuron, STDP training and AER communication, along with RAM-based weight storage.
- Tested pattern recognition workload followed by optimization through model adaptations in Vivado for deployment on an Artix-7 FPGA.