Soumya Ranjan Dash

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EDUCATION

University of Pennsylvania, *School of Engineering and Applied Science* **Aug '22 - May '24 [Expected]**
Master of Science in Engineering: **Electrical Engineering**, GPA - Ongoing
NIST Berhampur, *Department of Electronics & Communication Engineering* **Aug '18 - June '22**
Bachelor of Technology: **Electronics & Communication Engineering**, GPA - 3.5/4.0

SKILLS

Data Analytics: Data Mining, EDA, ETL, Data Visualization, REST APIs, Machine Learning, Deep Learning, Spark, Statistics
VLSI & Computer Architecture: RTL Design, Functional Verification, Digital VLSI Design, High Level Synthesis, **Test Planning**
Languages: **Python, C/C++,** Verilog, SystemVerilog, UVM, Matlab, **Web development(HTML & CSS, Bootstrap, Javascript, PHP, SQL)**
Industry Standards: AMBA4 (AXI, AHB, APB), Ethernet, SPI, I2C, UART
UPenn Courses: **Big Data Analytics, Digital VLSI, Computer Architecture, Embedded Systems,** Network Protocols, Data Center Architecture
Cadence courses(Extra): **SystemVerilog** for UVM, **Accelerated Verification** with UVM, SystemC Modeling, TLM & Synthesis (Ongoing)

WORK EXPERIENCE

Mack Institute - The Wharton School, *Data Research Assistant (Part-time), Philadelphia, PA* **Sept '23 – present**
- Utilized **REST/GraphQL APIs** to extract data from GitHub, prepare, organized data, and created **databases(.csv, .json etc.)** using **Python, SQL, and Spark** to accelerate **Big Data Processing** contributed to "Autoware Health & Performance" **Research project**.
- **Collaborated** with Autoware Foundation and other organizations to get user **data insights**, applied **statistical methods** followed by **visualizations** in **Matplotlib, Seaborn** etc. to highlight current trends to enable data-driven insights in Autoware innovations.

Seagate Technology, *VLSI Digital Read Channel(SoC) Design & Verification Intern (Full-time), Longmont, CO* **May '23 – Aug '23**
- Worked with Seagate's Read Channel IP team and **led the development** of a VIP for AXI Master module verifying concurrent Read/Write, Incrementing Burst Transfer to multiple DRAM Clients, & done **timing diagram analysis** showing **logical reasoning** skills.
- **Designed** and **built** all scalable, reusable UVCs in SystemVerilog & UVM in **UNIX**, **debugged** interactively using verdi debugger tool, implemented a **coverage model**, learnt the DRC **architecture & Regression test** process, and performed coverage **data analysis**.

Internshala Trainings, **Teaching Assistant – Python**, Gurgaon, India **Dec '21 – May '22**
- Worked in a **Python** based **app development** course, enhanced **debugging skills** by resolving **code queries** & **evaluating projects**.

SELECTED PROJECTS {Work Samples}

Flight Delay Prediction and Efficient Journey Recommendation using Machine Learning Models*[Software, Algorithms]* **Mar '23 – April '23**
- Built a flight delay prediction system with **Logistic Regression, Random Forest, XGBoost, and Catboost** models, did EDA in **Python & SQL**, feature selection, **hyperparameter tuning, and evaluation metrics** (recall, precision, F1 score, accuracy).
- Employed **Linear Regression** for flight time prediction, **XGBoost** for route optimization, & run **deep learning algorithms** on GPU.

HLS-based RV32I Multi-Core RISC-V FPGA Processor Modelling and Validation[*Computer Architecture*] **Aug '23 – Oct '23**
- Validation of RV32I instruction cores in **multi-core** RISC-V with **multihart pipelines & Cores** using HLS in **C/C++** & FPGA implementation.
- Utilization of Xilinx Vitis, Vivado, RISC-V Spike Tools, and **AXI interconnects** with Cache coherency for high performance and optimization.

Building a Robust UVM-based Verification IP for Router's RTL Design[*Digital Design, Debugging*] **May '23 – June '23**
- Led Cadence Xcelium-based verification IP development with UVM with **automation** features,multichannel Sequencers etc.
- Orchestrated integration of UVCs, employing scoreboard with TLM imp connectors for verification and **functional coverage analysis**.

Design Verification of a 16-bit Pipelined Superscalar LC4 Processor[*Computer Architecture*] **Jan '23 – May '23**
- Designed and verified a **processor** in Verilog, optimizing pipelines to meet a **66 MHz timing**, **addressing** hazards and bottlenecks.
- Tested design on **Xilinx Zynq 7000 SoC** using Vivado after 5-stage pipeline **verification** at the block/subsystem/System level.

Design & Layout of CLBs block for FPGA with energy-delay & area optimization[*Digital Design, Circuit Analysis*] **Nov '22 – Dec '22**
- Created a CLB LUTs having 6T-SRAM array, D-FF, SIPO etc. with AMI 0.60u C5N technology in Cadence virtuoso, followed by Layout Design.
- Achieved a **frequency** of 64.935MHz,**load energy** of 3.006nj,**active energy** of 3.28nJ, CLB area 230nm^2, & 'FOM' of 1.15*10^-23 m^2sJ.

Interactive Customer Experience System - DinoPlay, MoveDetect, ChatBot[*Software, Circuit Analysis, Lab tools***]** **Oct '22 – Dec '22**
- Constructed and **integrated** an Interactive Customer Experience System featuring DinoPlay on VGA display, MoveDetect, and ChatBot.
- Prepared a **custom circuit** containing Raspberry Pico, a Raspberry Pi camera for motion detection, ST7735 LCD Display, and Mono Enclosed Speaker etc. utilized **oscilloscopes** & **logic analyzer** for electrical **signal analysis**, **locating faults**, and **debugging** the circuits.
- **Showcased** the project creating a simple **website** using **HTML, CSS, Bootstrap,** & **JavaScript**, demonstrating **web development skills**.