8.3.3 FIFO manager

This block is designed to manage a RAM as a FIFO in order to optimize the data exchange between the CPU and the HOST.

8.3.3.1 FIFO manager functional description

The RAM used for the FIFO is shared between the SPI and HSU interfaces. Indeed, these interfaces cannot be used simultaneously. The selection of the interface used is done by firmware. The FIFO manager block is the common part between the SPI and the HSU interfaces. It consists of a Data register, a Status register and also some registers to define the characteristics of the FIFO. These registers are addressed by the CPU as SFRs.

The RAM used as a FIFO is divided into two part: a receive part and a transmit part.

This block also manages the possible conflicts existing around the FIFO between the CPU and the interfaces. Indeed, a request coming from the interface (TR_req or RCV_req) can be simultaneous with a request to access to the data register coming from the CPU.

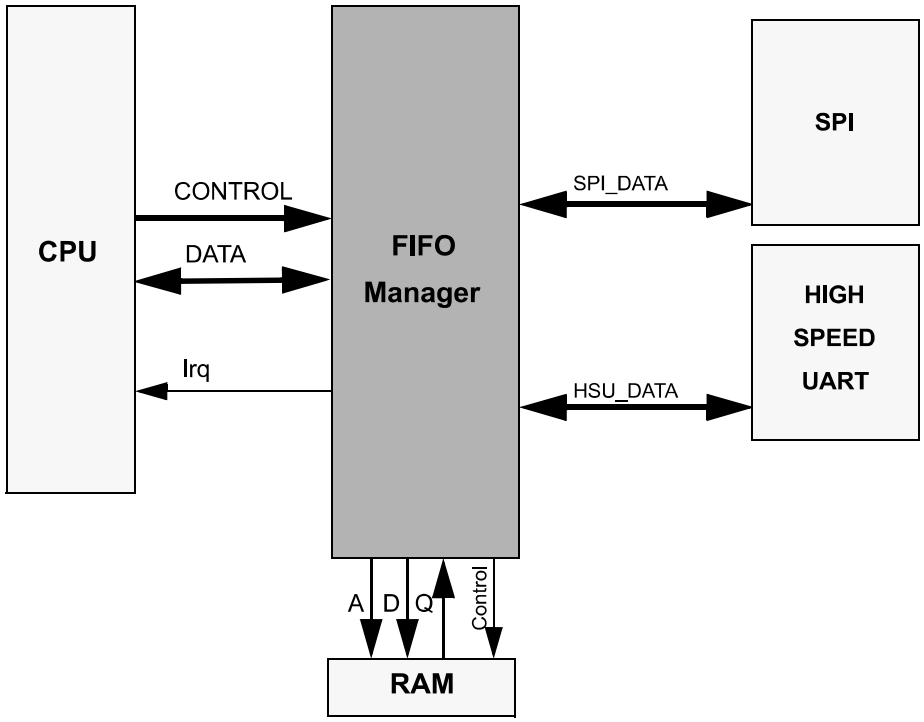

Fig 12. FIFO manager block diagram

9 SFR registers are needed to manage the FIFO manager.

Table 91. Fifo manager SFR register list

Name	Size [bytes]	SFR Address	Description	Access
RWL	1	9Ah	FIFO Receive Waterlevel: Controls the threshold of the FIFO in reception	R/W
TWL	1	9Bh	FIFO Transmit Waterlevel: Controls the threshold of the FIFO in transmission	R/W
FIFOFS	1	9Ch	FIFO Transmit FreeSpace: Status of the number of characters which can still be loaded in the FIFO	R/W
FIFOFF	1	9Dh	FIFO Receive Fullness: Status of the number of received characters in the FIFO	R/W
SFF	1	9Eh	Global Status/Error messages	R
FIT	1	9Fh	Interrupt Source	R/W
FITEN	1	A1h	Interrupt Enable and Reset FIFO	R
FDATA	1	A2h	Data reception/transmission buffer	R/W
FSIZE	1	A3h	Control the size of the FIFO in Reception	R/W

8.3.3.2 RWL register

This register defines the warning level of the Receive FIFO for the CPU. It implies a FIFO buffer overflow.

Table 92. RWL register (SFR: address 9Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RWaterlevel[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 93. Description of RWL bits

Bit	Symbol	Description
7 to 0	RWaterlevel[7:0]	Overflow threshold of the Receive FIFO to set a warning

8.3.3.3 TWL register

This register defines the warning level of the Transmit FIFO for the CPU. It implies a FIFO buffer underflow.

Table 94. TWL register (SFR: address 9Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TWaterlevel[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 95. Description of TWL bits

Bit	Symbol	Description
7 to 0	TWaterlevel[7:0]	Underflow threshold of the Transmit FIFO to set a warning

8.3.3.4 FIFOFS register

This register indicates the number of bytes that the CPU can still load into the FIFO until the Transmit FIFO is full.

Table 96. FIFOFS register (SFR: address 9Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TransmitFreespace[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 97. Description of FIFOFS register bits

Bit	Symbol	Description
7 to 0	TransmitFreespace[7:0]	Freespace into the FIFO

8.3.3.5 FIFOFF register

This register indicates the number of bytes already received and loaded into the Receive FIFO.

Table 98. FIFOFF register (SFR: address 9Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ReceiveFullness[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 99. Description of FIFOFF bits

Bit	Symbol	Description
7 to 0	ReceiveFullness[7:0]	Number of bytes received in the FIFO

8.3.3.6 SFF register

The register bits are used to allow the CPU to monitor the status of the FIFO. The primary purpose is to detect completion of data transfers.

Table 100. SFF register (SFR: address 9Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FIFO_EN	-	TWLL	TFF	TFE	RWLH	RFF	RFE
Reset	0	0	1	0	1	0	0	1
Access	R/W	R	R	R	R	R	R	R

Table 101. Description of SFF bits

Bit	Symbol	Description
7	FIFO_EN	**Fifo Enable:** Set to logic 1 this bit enables the FIFO manager clock (CPU_CLK). Set to logic 0 the clock remains low.
6	-	Reserved.
5	TWLL	**Transmit WaterlLevelLow:** This bit is set to logic 1 when the number of bytes stored into the Transmit FIFO is equal or smaller than the threshold TWaterlevel.
4	TFF	**Transmit FIFO Full:** This is set to logic 1 if the transmit part of the FIFO is full. It is set to logic 0 when a transfer is completed.
3	TFE	**Transmit FIFO Empty:** This bit indicates when the transmit part of the FIFO is empty. It is set to logic 0 when the CPU writes a character in the data register.
2	RWLH	**Receive WaterLevel High**: This bit is set to logic 1 when the number of bytes stored into the Receive FIFO is greater or equal to the threshold RWaterlevel.
1	RFF	**Receive FIFO Full:** This bit is set to logic 1 if the receive part of the FIFO is full. It is set to logic 0 by reading the FDATA register.
0	RFE	**Receive FIFO Empty:** This bit indicates when the receive part of the FIFO is empty. Set to logic 1, when the Receive FIFO is empty. Set to logic 0, when the Receive FIFO contains at least 1 byte.

8.3.3.7 FIT register

The FIT register contains 6 read-write bits which are logically OR-ed to generate an interrupt going to the CPU.

Table 102. FIT register (SFR: address 9Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Reset	-	WCOL_ IRQ	TWLL_ IRQ	TFF_ IRQ	RWLH_ IRQ	ROVR_ IRQ	RFF_ IRQ
Reset	0	0	0	0	0	0	0	0
Access	W	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 103. Description of FIT bits

Bit	Symbol	Description
7	Reset	**Reset:** Set to logic 1, Reset defines that the bits set to logic 1 in the write command are set to logic 0 in the register.
6	-	Reserved
5	WCOL_IRQ	**Write COLlision IRQ:** This bit is set to logic 1 when the transmitted part of the FIFO is already full (TFF is set to logic 1) and a new character is written by the CPU in the data register.
4	TWLL_IRQ	**Transmit WaterlLevelLow IRQ:** This bit is set to logic 1 when the number of bytes stored into the Transmit FIFO is equal or smaller than the threshold TWaterlevel.
3	TFF_IRQ	**Transmit FIFO Full IRQ:** This is set to logic 1 if the transmitted part of the FIFO is full.
2	RWLH_IRQ	**Receive WaterLevel High IRQ:** This bit is set to logic 1 when the number of bytes stored into the Receive FIFO is greater or equal to the threshold RWaterlevel.
1	ROVR_IRQ	**Read OVeRrun IRQ:** This bit indicates that a read overrun has occured.It occurs when the receiver part of the FIFO is full and a new data transfer is completed. Then the new received data is lost and ROVR_IRQ is set.
0	RFF_IRQ	**Receive FIFO Full IRQ:** This bit is set to logic 1 if the received part of the FIFO is full.

8.3.3.8 FITEN register

The FITEN register enables or disables the interrupt requests to the CPU. It is also used to reset the content of the Receive and Transmit FIFO.

Table 104. FITEN register (SFR: address A1h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TFLUSH	RFLUSH	EN_WCOL_IRQ	EN_TWLL_IRQ	EN_TFF_IRQ	EN_RWLH_IRQ	EN_ROVR_IRQ	EN_RFF_IRQ
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 105. Description of FITEN bits

Bit	Symbol	Description
7	TFLUSH	When set to logic level 1, the pointer of the Transmit FIFO is reset. This bit and RFLUSH must not be set at the same time.
6	RFLUSH	When set to logic level 1, the pointer of the Receive FIFO is reset. This bit and TFLUSH must not be set at the same time but one after the other.
5	EN_WCOL_IRQ	**ENable Write COLlision IRQ:** When set to logic 1, the WCOL_IRQ is enabled. The bit IE1_5 of register IE1 (see Table 13 on page 18) has also to be set to logic 1 to enable the corresponding CPU interrupt.
4	EN_TWLL_IRQ	**ENable Transmit WaterlLevelLow IRQ:** When set to logic 1, the TWLL_IRQ is enabled. The bit IE1_5 of register IE1 (see Table 13 on page 18) has also to be set to logic 1 to enable the corresponding CPU interrupt.
3	EN_TFF_IRQ	**ENable Transmit FIFO Full IRQ:** When set to logic level 1, the TFF_IRQ is enabled. The bit IE1_5 of register IE1 (see Table 13 on page 18) has also to be set to logic 1 to enable the corresponding CPU interrupt.
2	EN_RWLH_IRQ	**ENable Receive WaterLevel High IRQ:** When set to logic 1, the RWLH_IRQ is enabled. The bit IE1_5 of register IE1 (see Table 13 on page 18) has also to be set to logic 1 to enable the corresponding CPU interrupt.
1	EN_ROVR_IRQ	**ENable Read OVeRrun IRQ:** When set to logic 1, the ROVR_IRQ is enabled. The bit IE1_5 of register IE1 (see Table 13 on page 18) has also to be set to logic 1 to enable the corresponding CPU interrupt.
0	EN_RFF_IRQ	**ENable Receive FIFO Full IRQ:** When set to logic 1, the RFF_IRQ is enabled. The bit IE1_5 of register IE1 (see Table 13 on page 18) has also to be set to logic 1 to enable the corresponding CPU interrupt.

8.3.3.9 FDATA register

The FDATA register is used to provide the transmitted and received data bytes. Each data written in the data register is pushed into the Transmit FIFO. Each data read from the data register is popped from the Receive FIFO.

Table 106. FDATA register (SFR: address A2h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FDATA[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 107. Description of FDATA bits

Bit	Symbol	Description
7 to 0	FDATA[7:0]	Writing to FDATA writes to the transmit buffer. Reading from FDATA reads from the receive buffer.

8.3.3.10 FSIZE register

This register defines the size of the Receive FIFO. The maximum size is 182 bytes. The free space not used by the Receive FIFO in the RAM will be allocated to Transmit FIFO.

Table 108. FSIZE register (SFR: address A3h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ReceiveSize[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 109. Description of FSIZE bits

Bit	Symbol	Description
7 to 0	ReceiveSize[7:0]	Size of the Receive FIFO

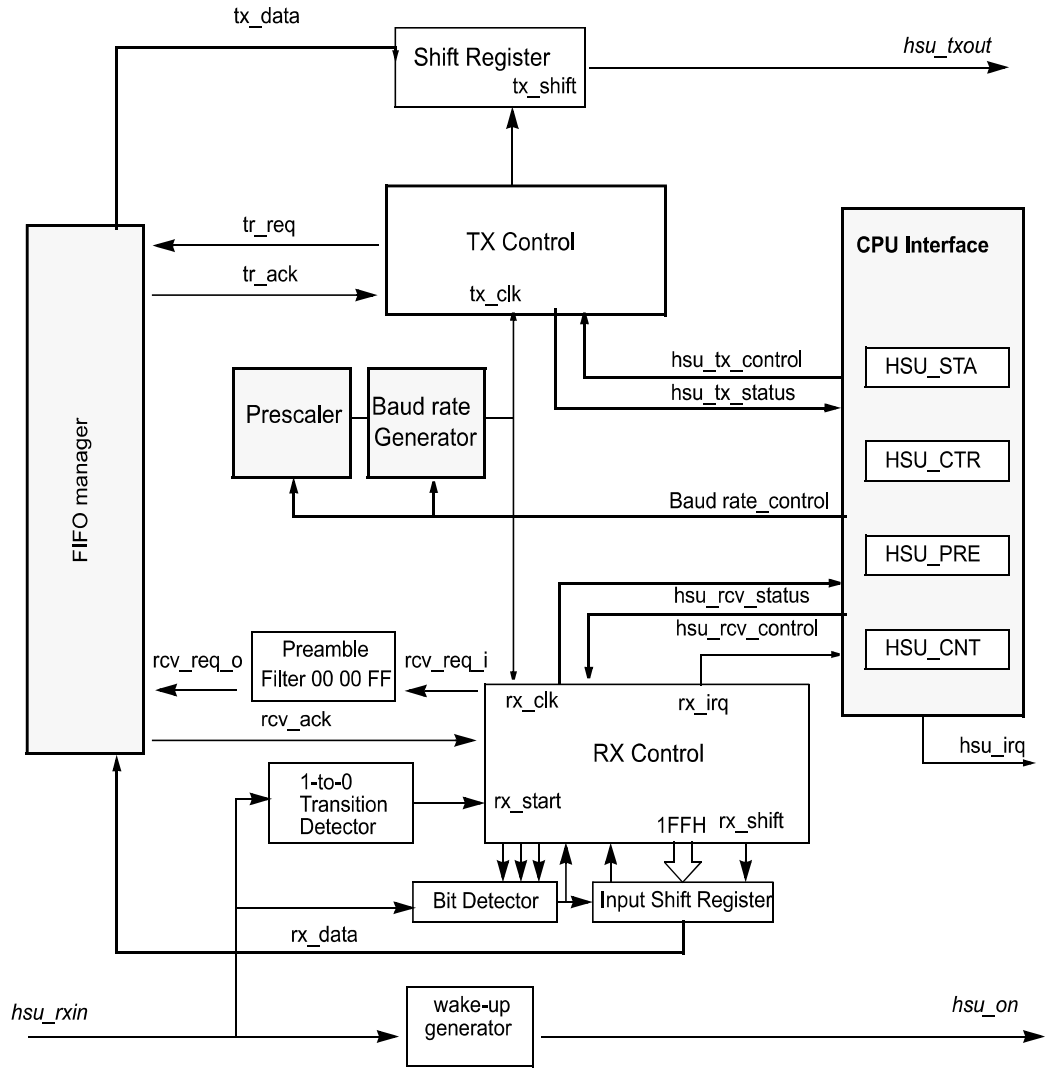

Fig 13. HSU block diagram

The HSU contains 4 SFRs:

Table 110. HSU SFR register list

Name	Size [bytes]	SFR Address	Description	Access
HSU_STA	1	ABh	HSU STAtus register	R/W
HSU_CTR	1	ACh	HSU ConTRol register	R/W
HSU_PRE	1	ADh	HSU PREscaler for baud rate generator	R/W
HSU_CNT	1	AEh	HSU CouNTer for baud rate generator	R/W

8.3.5 Serial Parallel Interface (SPI)

The SPI has the following features:

- Compliant with Motorola de-facto Serial Peripheral Interface (SPI) standard
- Synchronous, Serial, Half-Duplex communication, 5 MHz max
- Slave configuration
- 8 bits bus interface

Through the SPI interface, the host can either access the FIFO manager (acting as data buffer) or the SPI status register. This selection is made through the hereafter described protocol.

The SPI interface is managed by 2 SFRs.

Table 120. SPI SFR register list

Name	Size [bytes]	SFR address	Description	R/W
SPIcontrol	1	A9h	SPI control bits	R/W
SPIstatus	1	AAh	SPI Status/Error bits	R

8.3.5.1 Shift register pointer

A shift register is used to address the SPI interface. The value loaded in this register is either the first byte of the FIFO manager or the SPI status register.

The first byte received from the host will contain the address of the register to access (SPI status or FIFO manager FDATA) and also whether it is a SPI write or read. This character is managed by hardware.

The bits used to define these operations are the 2 LSBs of the first byte.

Table 121. SPI operation

Bit 1	Bit 0	Operation
0	0	No effect
0	1	FIFO manager write access
1	0	SPI Status register read access
1	1	FIFO manager read access

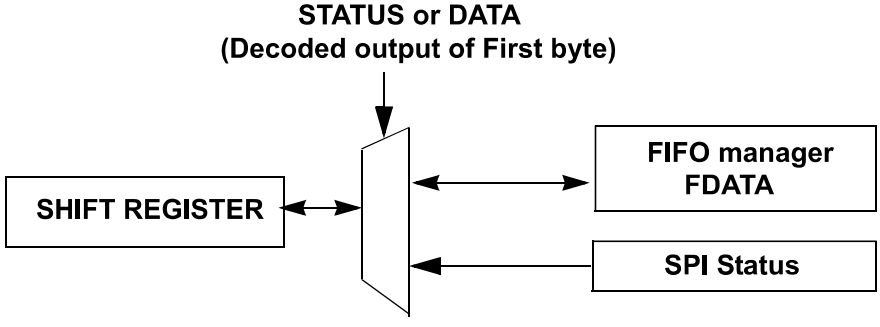

Fig 14. Memory manager shift register management

8.3.5.2 Protocol

Once the FIFO is full enough (see FIFO manager thresholds in Table 91 on page 67), the CPU sets bit READY in the SPI Status register to logic 1. Polling the SPI Status register, the host is informed of the READY flag and can start the data transfer.

The protocol used is based on:

- ADDRESS / DATA protocol for status data exchanges
- ADDRESS / DATA / DATA / DATA... for data transfers

An exchange starts on the falling edge of NSS and follows the diagram described below.

8.3.5.3 SPI status register read

There is in that case no read request going to the FIFO manager.
The content of the status register is loaded in the SPI shift register.

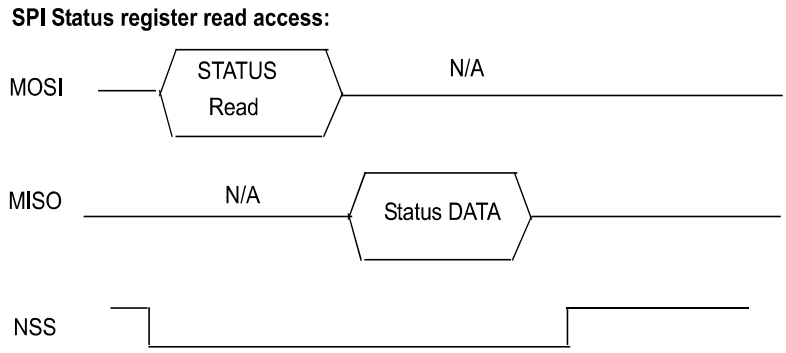

Fig 15. SPI Status register read access

8.3.5.4 FIFO manager read access

Bytes are loaded from the FIFO manager into the SPI shift register and sent back to the host.
Remark: for proper operation, the firmware should write an additional byte in the FIFO manager (FDATA). This byte will not be transmitted.

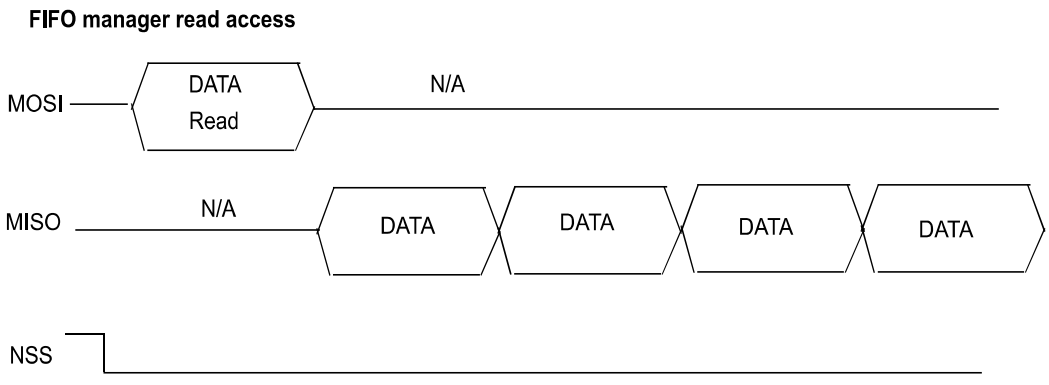

Fig 16. SPI FIFO manager read access

8.3.5.5 FIFO manager write access

MISO is maintained at logic 0. Once a byte is received, a write request is sent to the FIFO manager and the byte is loaded from SPI shift register into Receive FIFO of the FIFO manager.

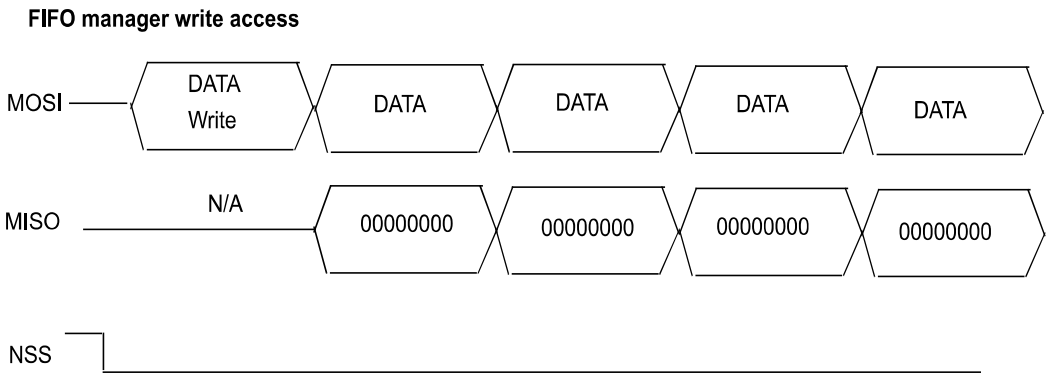

Fig 17. SPI FIFO manager write access

8.3.5.6 SPIcontrol register

SPIcontrol register contains programmable bits used to control the function of the SPI block. This register has to be set prior to any data transfer.

Table 122. SPIcontrol register (SFR: address A9h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	Enable	-	CPHA	CPOL	IE1	IE0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R	R/W	R/W	R/W	R/W

Table 123. Description of SPIcontrol bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5	Enable	**SPI enable:** When set to logic 1, enables the SPI interface assuming that selif[1:0] are set to 01b.
4	-	Reserved.
3	CPHA	**Clock PHAse:** This bit controls the relationship between the data and the clock on SPI transfers. When set to logic 0: Data is always sampled on the first clock edge of SCK. When set to logic 1: Data is always sampled on the second clock edge of SCK.
2	CPOL	**Clock POLarity:** This bit controls the polarity of SCK clock. When set to logic 1, SCK starts from logic 0 else starts from logic 1.
1	IE1	**Interrupt Enable 1:** When set to logic 1, the hardware interrupt generated by TR_FE in SPIstatus register is enabled. The bit IE1_5 of register IE1 (see Table 13 on page 18) has also to be set to logic 1 to enable the corresponding CPU interrupt.
0	IE0	**Interrupt Enable 0:** When set to logic 1, the hardware interrupt generated by RCV_OVR in SPIstatus register is enabled. The bit IE1_5 of register IE1 (see Table 13 on page 18) has also to be set to logic 1 to enable the corresponding CPU interrupt.

Remark: The following figure explains how bits CPOL and CPHA can be used.

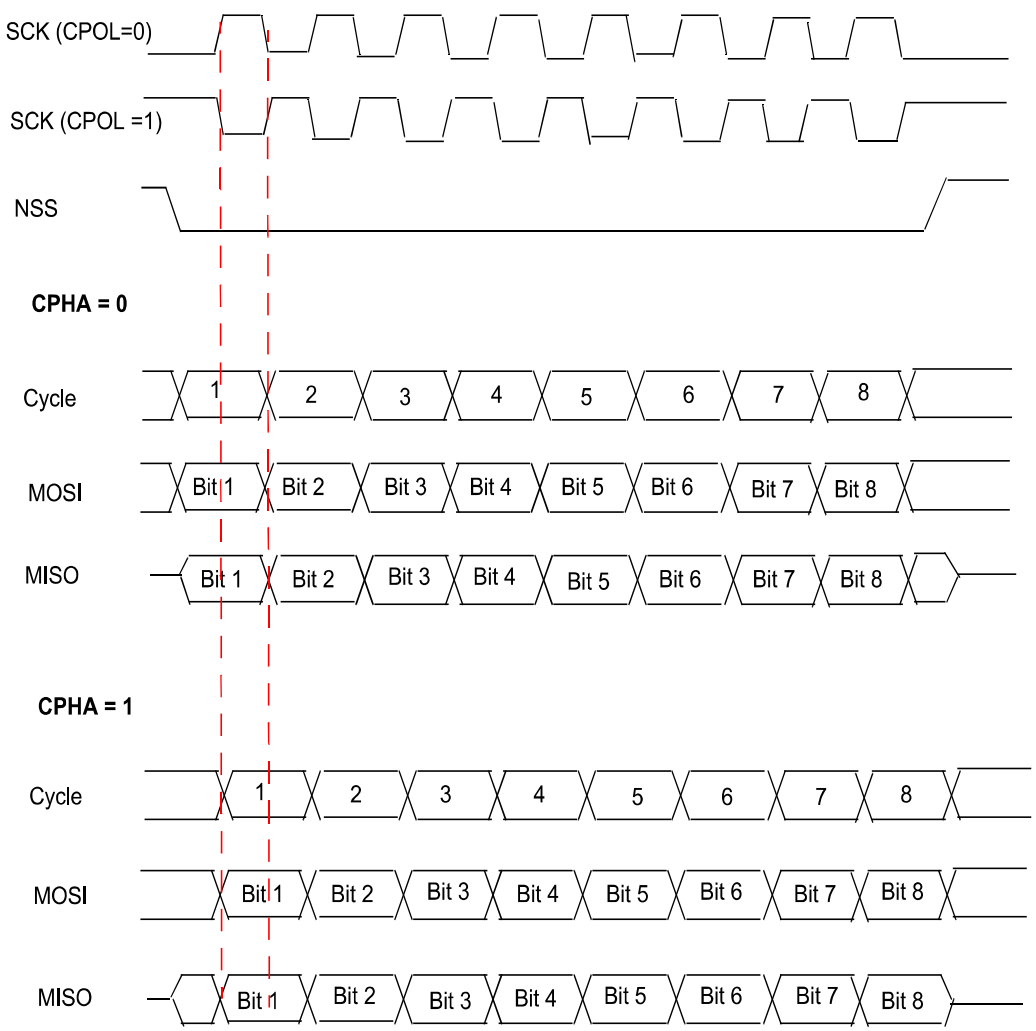

Fig 18. SPI Data transfer format

8.3.5.7 SPIstatus register

The SPIstatus register is byte addressable. It contains bits which are used to monitor the status of the SPI interface, including normal functions, and exception conditions. The primary purpose of this register is to detect completion of a data transfer. The remaining bits in this register are exception condition indicators.

Table 124. SPIstatus register (SFR: address AAh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	TR_FE	RCV_OVR	-	READY
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W

Table 125. Description of SPIstatus bits

Bit	Symbol	Description
7 to 4	-	Reserved.
3	TR_FE	**Transmit FIFO Empty:** Set to logic 1 when the host attempts to read a new byte and FIFO manager is empty. An interrupt can be generated if enabled (see IE1 bit in register SPIcontrol). It is set to logic 0 by firmware.
2	RCV_OVR	**Receive Overrun:** Set to logic 1 when the host attempts to write a new byte and FIFO manager is full, or has not yet processed the previous byte. An interrupt can be generated if enabled (see IE0 bit in register SPIcontrol) It is set to logic 0 by firmware.
1	-	**Reserved. This bit must be set to logic 0.**
0	READY	**Ready flag. The firmware set READY to logic 1 to inform the host when PN532 is ready to send data.**

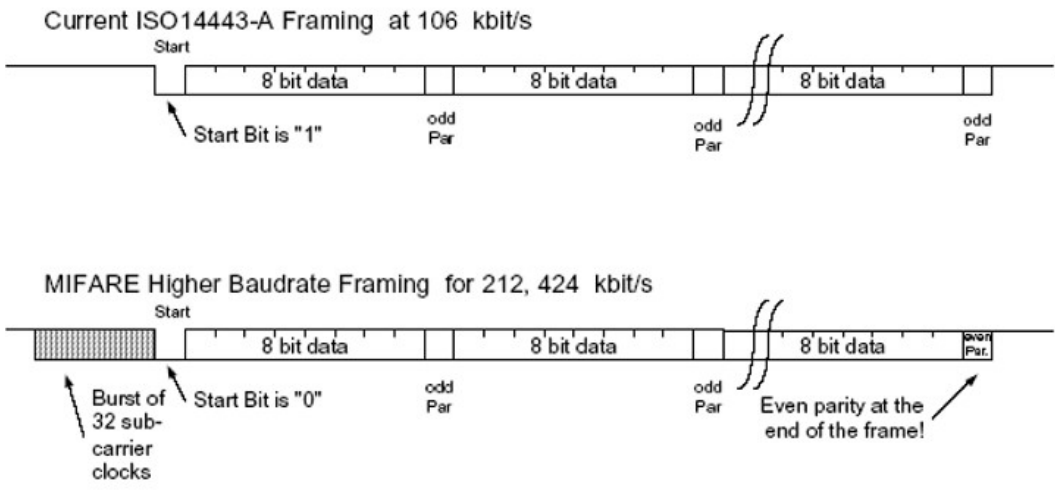

Fig 28. Data coding and framing according to ISO/IEC 14443A