Bill Davis
605.411 Problem Set 5

1. (a) Yes, this eliminates 1 bubble, since an instruction can, in the same clock cycle read a register in stage 2 that is being written too by another instruction in stage 5.
   (b) The branch history table (BHT) is consulted during the instruction fetch stage.
   (c) The decode history table (DHT) is consulted during the instruction decode, and only when the instruction is a branch instruction.
   (d) The BHT is consulted for every instruction.
   (e) The DHT is only consulted for branch instructions.

2. (a) This takes 20 clock cycles to complete
   (b) See the attached spreadsheet
   (c) Since this would eliminate the bubbles it was take 12 clock cycles to complete

3. lui $4, 0x00EB
   addi $5, $0, 8
   NOP
   ori $4, $4, 64
   NOP
   NOP
   sw $5, 0($4)
   sll $5,$5, 3
   lw $6, 0($4)
   NOP
   NOP
   slt $7, $6, $5
   NOP
   sw $7 , 4($5)

4. (a) Without data forwarding there would be 2 bubbles
   (b) With data forwarding there are 0 bubbles

5. There are no data dependencies in this sequence. Even though the first and second instruction both use register $5, sw merely reads the value and does not alter it.

6. (a) 24 Clock Cycles
   (b) 11 Clock Cycles
   (c) 34 Clock Cycles (Since this operates like a pipeline with 15 stages)
   (d) 21 Clock Cycles