Example Files

Seven example circuits are included in this folder:

mealy_ex.ckt is the example given in Figure 6 in the SimUaid User's Manual.

mul.ckt is based on the binary multiplier of Figure 18-7 in Fundamentals of Logic Design, 6th ed., using SimUaid parts. To test this multiplier, reset the simulation, show I/O values, and then proceed as follows:

1. Set the input switches for the multiplicand and multiplier.
2. Set LdM = 1 and toggle CLK to clear the accumulator and load the multiplier. Then return LdM to 0.
3. Observe M, and use the appropriate sequence of Add, Sh, and CLK signals to complete the multiplication. (Add causes the adder output to be loaded into the accumulator.)
4. Read the product.

mulSM.ckt is the same as mul.ckt with a state machine controller and counter added. The state machine implements the add-shift control of Figure 18-9. Since you will have to change St to 1 and then return it to 0 after one clock cycle, you won't be able to use the Simulate->Go menu item (or the "GO" button). Instead, use Simulate->Step (or ctrl-T or the button to the right of "STOP") for each clock cycle. Note that the first time you use it after a reset, there will be no rising edge, so the flip-flops won't change.

busdivider.ckt is based on the divider of Figure 18-13 with the subtracter replaced by an adder and a complementer. To change the value of the dividend and divisor, select Edit->Label from the menu (or just click on the button labeled "ABC"), and then right-click on the box labeled "dividend" or "divisor."

busdivSM.ckt is the same as busdivider.ckt with a state machine controller and counter added.

dicegameSM.ckt is based on the DiceGame module of Figure 19-11, with the state machine controller of Figure 19-14. Note that to change the value of the sum of the dice without resetting, as is necessary to test some cases, you cannot access the Edit->Label menu item (or the button labeled "ABC"). Instead, just right-click on the box that says "Sum."

Asynch.ckt is an asynchronous circuit example taken from Fundamentals of Logic Design, 4th edition, Figure 27-9. A reset switch has been added to reset the latches. The input signal generators generate waveforms that correspond to the last example in Figure 27-4, part 4. NOTE: If you have troubles with the SimUAid reset button (or "Reset" from the "Simulate" menu, or Ctrl+R) giving crazy waveforms, then set the circuit reset switch to zero, and then reset SimUAid.