Synthesis Reports

1.Synthesis Reports

| Tool Version : Vivado v.2024.1 (win64) Build 5076996 Wed May 22 18:37:14 MDT 2024

| Date : Sun Nov 16 08:18:54 2025

| Host : LAVANYA running 64-bit major release (build 9200)

| Command : report_utilization -file vending_machine_top_utilization_synth.rpt -pb vending_machine_top_utilization_synth.pb

| Design : vending_machine_top

| Device : xc7k70tfbv676-1

| Speed File : -1

| Design State : Synthesized

Utilization Design Information

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8. Black Boxes

9. Instantiated Netlists

1. Slice Logic

+-------------------------+-------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+-------------------------+-------+-------+------------+-----------+-------+

| Slice LUTs* | 35359 | 0 | 0 | 41000 | 86.24 |

| LUT as Logic | 35359 | 0 | 0 | 41000 | 86.24 |

| LUT as Memory | 0 | 0 | 0 | 13400 | 0.00 |

| Slice Registers | 33484 | 0 | 0 | 82000 | 40.83 |

| Register as Flip Flop | 33484 | 0 | 0 | 82000 | 40.83 |

| Register as Latch | 0 | 0 | 0 | 82000 | 0.00 |

| F7 Muxes | 7616 | 0 | 0 | 20500 | 37.15 |

| F8 Muxes | 3792 | 0 | 0 | 10250 | 37.00 |

+-------------------------+-------+-------+------------+-----------+-------+

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

Warning! LUT value is adjusted to account for LUT combining.

Warning! For any ECO changes, please run place_design if there are unplaced instances

1.1 Summary of Registers by Type

+-------+--------------+-------------+--------------+

| Total | Clock Enable | Synchronous | Asynchronous |

+-------+--------------+-------------+--------------+

| 0 | _ | - | - |

| 0 | _ | - | Set |

| 0 | _ | - | Reset |

| 0 | _ | Set | - |

| 0 | _ | Reset | - |

| 0 | Yes | - | - |

| 0 | Yes | - | Set |

| 33484 | Yes | - | Reset |

| 0 | Yes | Set | - |

| 0 | Yes | Reset | - |

+-------+--------------+-------------+--------------+

2. Memory

+----------------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+----------------+------+-------+------------+-----------+-------+

| Block RAM Tile | 0 | 0 | 0 | 135 | 0.00 |

| RAMB36/FIFO* | 0 | 0 | 0 | 135 | 0.00 |

| RAMB18 | 0 | 0 | 0 | 270 | 0.00 |

+----------------+------+-------+------------+-----------+-------+

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

+-----------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+-----------+------+-------+------------+-----------+-------+

| DSPs | 0 | 0 | 0 | 240 | 0.00 |

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4. IO and GT Specific

+----------------------------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+----------------------------+------+-------+------------+-----------+-------+

| Bonded IOB | 143 | 0 | 0 | 300 | 47.67 |

| Bonded IPADs | 0 | 0 | 0 | 26 | 0.00 |

| Bonded OPADs | 0 | 0 | 0 | 16 | 0.00 |

| PHY_CONTROL | 0 | 0 | 0 | 6 | 0.00 |

| PHASER_REF | 0 | 0 | 0 | 6 | 0.00 |

| OUT_FIFO | 0 | 0 | 0 | 24 | 0.00 |

| IN_FIFO | 0 | 0 | 0 | 24 | 0.00 |

| IDELAYCTRL | 0 | 0 | 0 | 6 | 0.00 |

| IBUFDS | 0 | 0 | 0 | 288 | 0.00 |

| GTXE2_COMMON | 0 | 0 | 0 | 2 | 0.00 |

| GTXE2_CHANNEL | 0 | 0 | 0 | 8 | 0.00 |

| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 0 | 24 | 0.00 |

| PHASER_IN/PHASER_IN_PHY | 0 | 0 | 0 | 24 | 0.00 |

| IDELAYE2/IDELAYE2_FINEDELAY | 0 | 0 | 0 | 300 | 0.00 |

| ODELAYE2/ODELAYE2_FINEDELAY | 0 | 0 | 0 | 100 | 0.00 |

| IBUFDS_GTE2 | 0 | 0 | 0 | 4 | 0.00 |

| ILOGIC | 0 | 0 | 0 | 300 | 0.00 |

| OLOGIC | 0 | 0 | 0 | 300 | 0.00 |

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5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	2	0	0	32	6.25
BUFIO	0	0	0	24	0.00
MMCME2_ADV	0	0	0	6	0.00
PLLE2_ADV	0	0	0	6	0.00
BUFMRCE	0	0	0	12	0.00
BUFHCE	0	0	0	96	0.00
BUFR	0	0	0	24	0.00

6. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
PCIE_2_1	0	0	0	1	0.00
STARTUPE2	0	0	0	1	0.00

| XADC | 0 | 0 | 0 | 1 | 0.00 |

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7. Primitives

+----------+-------+---------------------+

| Ref Name | Used | Functional Category |

+----------+-------+---------------------+

| FDCE | 33484 | Flop & Latch |

| LUT6 | 30301 | LUT |

| MUXF7 | 7616 | MuxFx |

| MUXF8 | 3792 | MuxFx |

| LUT4 | 3724 | LUT |

| LUT5 | 1655 | LUT |

| LUT2 | 1076 | LUT |

| LUT3 | 759 | LUT |

| IBUF | 76 | IO |

| OBUF | 67 | IO |

| CARRY4 | 27 | CarryLogic |

| LUT1 | 12 | LUT |

| BUFG | 2 | Clock |

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8. Black Boxes

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| Ref Name | Used |

+----------+------+

9. Instantiated Netlists

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| Ref Name | Used |

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2.Utilization- synth Design

| Tool Version : Vivado v.2024.1 (win64) Build 5076996 Wed May 22 18:37:14 MDT 2024

| Date : Sun Nov 16 08:18:54 2025

| Host : LAVANYA running 64-bit major release (build 9200)

| Command : report_utilization -file vending_machine_top_utilization_synth.rpt -pb vending_machine_top_utilization_synth.pb

| Design : vending_machine_top

| Device : xc7k70tfbv676-1

| Speed File : -1

| Design State : Synthesized

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8. Black Boxes

9. Instantiated Netlists

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	35359	0	0	41000	86.24
LUT as Logic	35359	0	0	41000	86.24
LUT as Memory	0	0	0	13400	0.00
Slice Registers	33484	0	0	82000	40.83
Register as Flip Flop	33484	0	0	82000	40.83
Register as Latch	0	0	0	82000	0.00
F7 Muxes	7616	0	0	20500	37.15
F8 Muxes	3792	0	0	10250	37.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

Warning! LUT value is adjusted to account for LUT combining.

Warning! For any ECO changes, please run place_design if there are unplaced instances

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
33484	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	135	0.00
RAMB36/FIFO*	0	0	0	135	0.00
RAMB18	0	0	0	270	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

+-----------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+-----------+------+-------+------------+-----------+-------+

| DSPs | 0 | 0 | 0 | 240 | 0.00 |

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4. IO and GT Specific

+-----------------------------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+-----------------------------+------+-------+------------+-----------+-------+

| Bonded IOB | 143 | 0 | 0 | 300 | 47.67 |

| Bonded IPADs | 0 | 0 | 0 | 26 | 0.00 |

| Bonded OPADs | 0 | 0 | 0 | 16 | 0.00 |

| PHY_CONTROL | 0 | 0 | 0 | 6 | 0.00 |

| PHASER_REF | 0 | 0 | 0 | 6 | 0.00 |

| OUT_FIFO | 0 | 0 | 0 | 24 | 0.00 |

| IN_FIFO | 0 | 0 | 0 | 24 | 0.00 |

| IDELAYCTRL | 0 | 0 | 0 | 6 | 0.00 |

| IBUFDS | 0 | 0 | 0 | 288 | 0.00 |

| GTXE2_COMMON | 0 | 0 | 0 | 2 | 0.00 |

| GTXE2_CHANNEL | 0 | 0 | 0 | 8 | 0.00 |

| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 0 | 24 | 0.00 |

| PHASER_IN/PHASER_IN_PHY | 0 | 0 | 0 | 24 | 0.00 |

| IDELAYE2/IDELAYE2_FINEDELAY | 0 | 0 | 0 | 300 | 0.00 |

| ODELAYE2/ODELAYE2_FINEDELAY | 0 | 0 | 0 | 100 | 0.00 |

| IBUFDS_GTE2 | 0 | 0 | 0 | 4 | 0.00 |

| ILOGIC | 0 | 0 | 0 | 300 | 0.00 |

| OLOGIC | 0 | 0 | 0 | 300 | 0.00 |

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5. Clocking

+----------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+----------+------+-------+------------+-----------+-------+

| BUFGCTRL | 2 | 0 | 0 | 32 | 6.25 |

| BUFIO | 0 | 0 | 0 | 24 | 0.00 |

| MMCME2_ADV | 0 | 0 | 0 | 6 | 0.00 |

| PLLE2_ADV | 0 | 0 | 0 | 6 | 0.00 |

| BUFMRCE | 0 | 0 | 0 | 12 | 0.00 |

| BUFHCE | 0 | 0 | 0 | 96 | 0.00 |

| BUFR | 0 | 0 | 0 | 24 | 0.00 |

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6. Specific Feature

+----------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

| BSCANE2 | 0 | 0 | 0 | 4 | 0.00 |

| CAPTUREE2 | 0 | 0 | 0 | 1 | 0.00 |

| DNA_PORT | 0 | 0 | 0 | 1 | 0.00 |

| EFUSE_USR | 0 | 0 | 0 | 1 | 0.00 |

| FRAME_ECCE2 | 0 | 0 | 0 | 1 | 0.00 |

| ICAPE2 | 0 | 0 | 0 | 2 | 0.00 |

| PCIE_2_1 | 0 | 0 | 0 | 1 | 0.00 |

| STARTUPE2 | 0 | 0 | 0 | 1 | 0.00 |

| XADC | 0 | 0 | 0 | 1 | 0.00 |

7. Primitives

| Ref Name | Used | Functional Category |

| FDCE | 33484 | Flop & Latch |

| LUT6 | 30301 | LUT |

| MUXF7 | 7616 | MuxFx |

| MUXF8 | 3792 | MuxFx |

| LUT4 | 3724 | LUT |

| LUT5 | 1655 | LUT |

| LUT2 | 1076 | LUT |

| LUT3 | 759 | LUT |

| IBUF | 76 | IO |

| OBUF | 67 | IO |

| CARRY4 | 27 | CarryLogic |

| LUT1 | 12 | LUT |

| BUFG | 2 | Clock |

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8. Black Boxes

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| Ref Name | Used |

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9. Instantiated Netlists

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| Ref Name | Used |

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