2022 Digital IC Design
Final Project

NAME	魏本憲
Student ID	NE6104113

Functional Simulation Result of LZ77 Encoder

Testing Pattern 0	Pass	Testing Pattern 1	Pass	Testing Pattern 2	Pass

```
# cycle 206f5, expect(01,03,6) , get(01,03,6) >> Pass
# cycle 2071b, expect(1b,02,9) , get(1b,02,9) >> Pass
# cycle 2073e, expect(00,00,1) , get(00,00,1) >> Pass
# cycle 2075f, expect(00,00,$) , get(00,00,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
```

```
# cycle 1a11f, expect(00,00,2) , get(00,00,2) >> Pass
# cycle 1a140, expect(00,00,7) , get(00,00,7) >> Pass
# cycle 1a162, expect(01,01,e) , get(01,01,e) >> Pass
# cycle 1a186, expect(15,02,$) , get(15,02,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
```

```
# cycle 1c837, expect(17,01,4) , get(17,01,4) >> Pass
# cycle 1c85b, expect(19,02,7) , get(19,02,7) >> Pass
# cycle 1c880, expect(0b,02,0) , get(0b,02,0) >> Pass
# cycle 1c8a3, expect(00,00,$) , get(00,00,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
```

Functional Simulation Result of LZ77 Decoder

Testing Pattern 0	Pass	Testing Pattern 1	Pass	Testing Pattern 2	Pass

```
# cycle 02004, expect 1, get 1 >> Pass
# ------------------------------------------------------------
# -------------- Decoding finished, ALL PASS --------------
# ------------------------------------------------------------
# ------------------------------------------------------------
# ----- Interpolation finished, result is written out -----
# ------------------------------------------------------------
```

```
# cycle 02004, expect f, get f >> Pass
# ------------------------------------------------------------
# -------------- Decoding finished, ALL PASS --------------
# ------------------------------------------------------------
# ------------------------------------------------------------
# ----- Interpolation finished, result is written out -----
# ------------------------------------------------------------
```

```
# cycle 02004, expect 0, get 0 >> Pass
# ------------------------------------------------------------
# -------------- Decoding finished, ALL PASS --------------
# ------------------------------------------------------------
# ------------------------------------------------------------
# ----- Interpolation finished, result is written out -----
# ------------------------------------------------------------
```

Quality of Interpolated Results					
Testing Pattern 0	23.7970028	Testing Pattern 1	24.5099628	Testing Pattern 2	27.8758807

Description of your design

LZ77encoder 電路是針對同一個字串去做壓縮為目標
LZ77 decoder 電路是 testbench 給定開頭和相同的字串去做設計
ELA 電路則是根據此行的上下兩排去做插值去做設計

Scoring = Pattern 0 PSNR + Pattern 1 PSNR + Pattern 2 PSNR
The higher, the better.