Intel FPGA VIP webinar series

Building Video Processing Pipelines

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Video processing on FPGAs made easy

Objectives

- What resources are available to develop Video Processing solutions?
- From the basics: step through an incremental series of example designs
- End2End flow demonstration: hardware architecture design, software development & debug
- Sessions will be recorded. Exercise manuals and project files will be available for on-demand consumption

Resources for Video Processing Applications

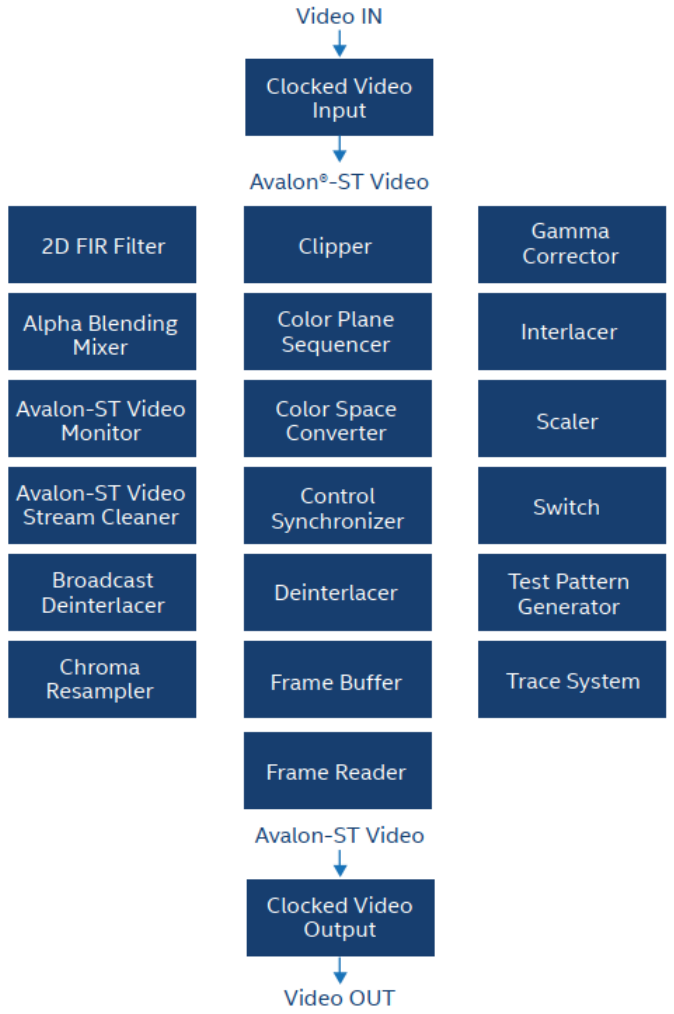
Plug & Play blocks for rapid design creation

- Video Processing building blocks (VIP Suite)
- Connectivity IPs (DisplayPort, HDMI, SDI, …)
- Development kits and video I/O daughter cards
- Collection of reference designs and application notes

- This webinar series ;)

8K-Ready Video and Image Processing Suite

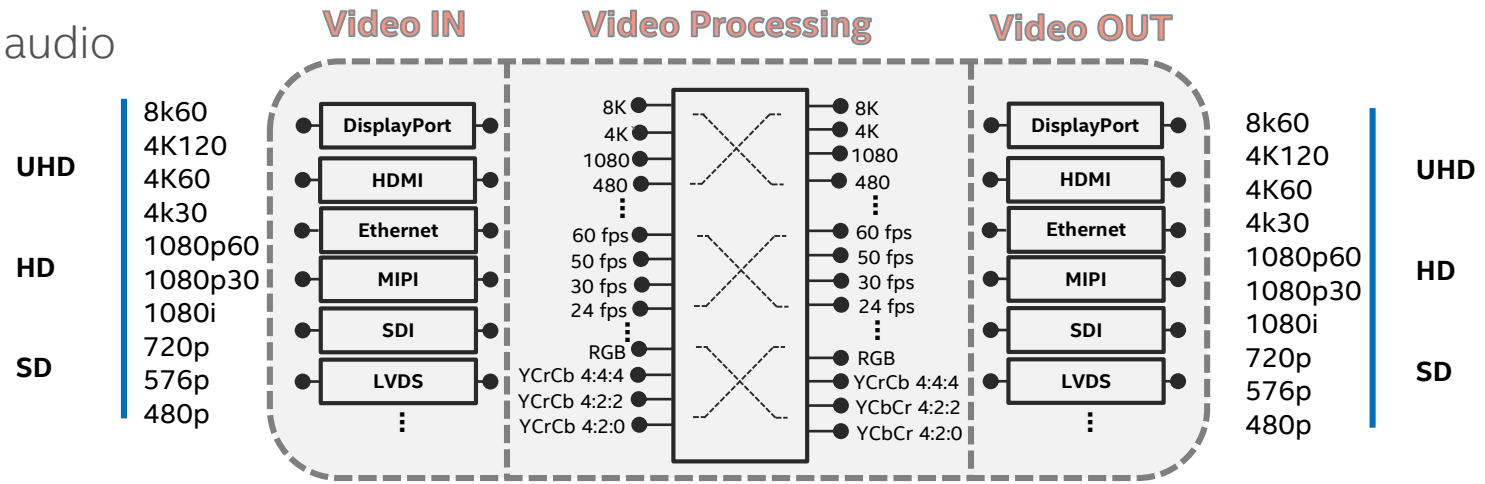
- Collection of 20+ IP functions with support for all Intel FPGAs
- VIP Suite II provides a design philosophy for rapid new design creation and easy integration of custom value-add features
- Easy integration with video connectivity IP cores, such as: HDMI, DisplayPort, 12G-SDI, SMPTE 2110 and MIPI
- Supports a wide range of resolutions, fps, bits per color
  - 1080p/4K/8K, HDR ready, 120+ fps, 16 bpc
- Visually exceeds most of the ASSPs



https://www.intel.com/content/www/us/en/programmable/products/intellectual-property/ip/dsp/m-alt-vipsuite.html

Video Connectivity IPs

- DisplayPort
  - Compliant with 1.4 -> 2.0 in dev
  - Up to 4-ch MST Support, up to 8-ch audio
  - Link Training quality analysis
- HDMI
  - Compliant with 2.0 and prev
  - Supporting new 2.1 FRL
  - Deep color mode, up to 8-ch audio
- HDCP
  - Certified 1.4/2.3 with HDMI and DP
- SDI
  - Multistandard up to 12G-SDI

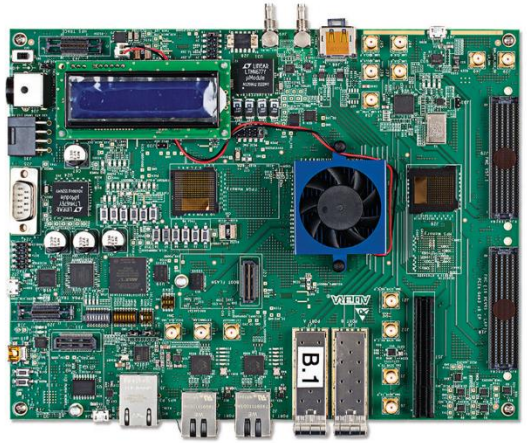


https://www.intel.com/content/www/us/en/broadcast/products/programmable/applications/connectivity-solutions.html

Development kits and I/O cards

Build your PoC matching FPGA fabric and interfaces

Stratix10



Arria10

ARROW
Cyclone10 GX SoM
+ carrier

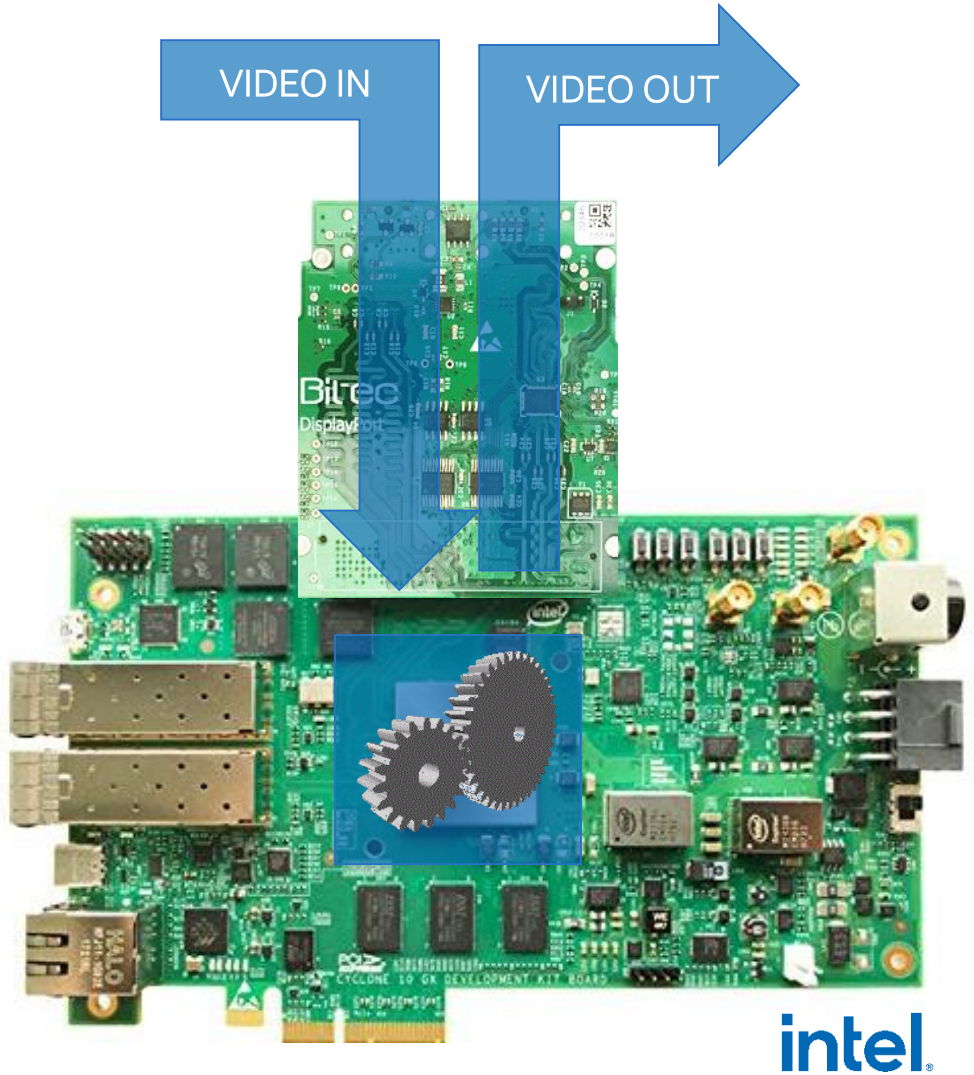
HDMI

DisplayPort

12G-SDI

Hardware used in these webinars

- Cyclone10 GX devkit
  - https://www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/cyclone-10-gx-development-kit.html
- Bitec displayport daughter card rev.11
  - https://bitec-dsp.com/product/fmc-displayport-daughter-card-revision-11/



Reference Designs and App Notes

Full-featured examples up to 8K

		SDI	DisplayPort	HDMI	VIP
A10/C10 GX/SX	Reference Design/ Examples	1. A10 / C10 SDI Design Example VCXO/VCXOless 2. 12G SDI + CVI/CVO ref design (2SI only)	1. A10 / C10 DP 1.4 Design Example 2. DP 1.4 RX/TX 3. A10 / C10 DP 1.2 UDX Lite 4. A10 DP UDX 1.4 8k30 in/out	1. A10 UDX10 (HDMI 2.0) Ref Design, C10 UDX10 Lite 2. A10 / C10 HDMI 2.0 Design Example (retransmit) 3. EA HDMI 2.1 Design Example (retransmit)	1. A10 UHD (4k60) HDMI 2.0 Ref Design 2. A10 / C10 DP 1.2, C10 HDMI 2.0 UDX Lite 3. A10 DP 1.4 8k30 in/out
	Target Hardware	1.2. A10/C10 FPGA Devkit + Nextera FMC/Terasic 3. A10/C10 FPGA Devkit + Terasic	1 - 4. A10/C10 FPGA Devkit + Bitec DP FMC daughter card rev8/11	1-2: A10/C10 FPGA Devkit + Bitec HDMI FMC daughter Card rev11 3. Bitec FMC HDMI 2.1 rev4	1. A10/C10 GX Devkit + Bitec HDMI FMC daughter Card rev11 2/3. A10 GX Devkit + Bitec DP FMC daughter card rev8/11
S10 GX/SX/MX	Reference Design/ Examples	1. SDI Design Example VCXO/VCXOless 2. 12G multi-rate Audio Embed, De-embed (upon request)	1. DP 1.4 design example	1.HDMI Design Example	
	Target Hardware	1. S10 FPGA H-tile / SoC kit (upon request) DevKit+ Nextera FMC/Terasic	1. S10 FPGA Devkit + Bitec DP FMC daughter card rev 8/11	1. S10 GX Dev Kit + Bitec HDMI 2.0 FMC daughter card rev11	

References

- Displayport IP User Guide
  - https://www.intel.com/content/www/us/en/programmable/products/intellectual-property/ip/interface-protocols/m-alt-displayport-megacore.html
- Cyclone 10 GX Displayport Design Example User Guide
  - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug-dex-dp-c10gx.pdf
- AN745: Design Guidelines for Displayport Interface
  - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an_745.pdf
- Quartus Prime Pro Installation Guide – 20.3
  - https://www.intel.com/content/dam/altera-www/global/en_US/pdfs/literature/manual/quartus_install.pdf
- NiosII EDS installation – 20.3
  - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/nios2/n2sw_nii5v2gen2.pdf
- Embedded Design Handbook
  - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/nios2/edh_ed_handbook.pdf

Webinar Series

Soft start -> Increasing Complexity

1. Building a video processing pipeline (Oct, 14th and 21st)
   - Getting video processed through the devkit, incremental flow
   - Detailed step flow on hardware implementation
   - Software application development using C++ API for a Nios II CPU
2. Strategies to debug a VIP pipeline (Nov, 4th)
   - Overview of system level considerations and key video concepts
   - Introduce the methods to build up and debug video systems
   - Overview of Avalon-ST Video protocol
3. Integrate a simple custom component (Nov, 19th)
   - How to add your “secret sauce” to the application
   - Step flow on how to develop a custom component compliant with VIP
4. Adding On Screen Display overlay (Dec, 16th)
   - Use a lightweight graphic library with Nios
   - Add text and graphic content overlay on top of your live video

All sessions – 10:00am to 12:00pm CET