

Intel FPGA VIP webinar series

Session 4

Adding OSD overlay

Francisco Perez

Intel FPGA Field Applications Engineer

v.1 – December 2020



Video processing on FPGAs made easy

Content available in the GitHub repo:

https://github.com/perezfra/VIP_webinars_Intel_FPGA

Objectives

- What resources are available to develop Video Processing solutions?
- From the basics: step through an incremental series of example designs
- End2End flow demonstration: hardware architecture design, software development & debug
- Sessions will be recorded. Exercise manuals and project files will be available for on-demand consumption

Webinar Series

Soft start -> Increasing Complexity

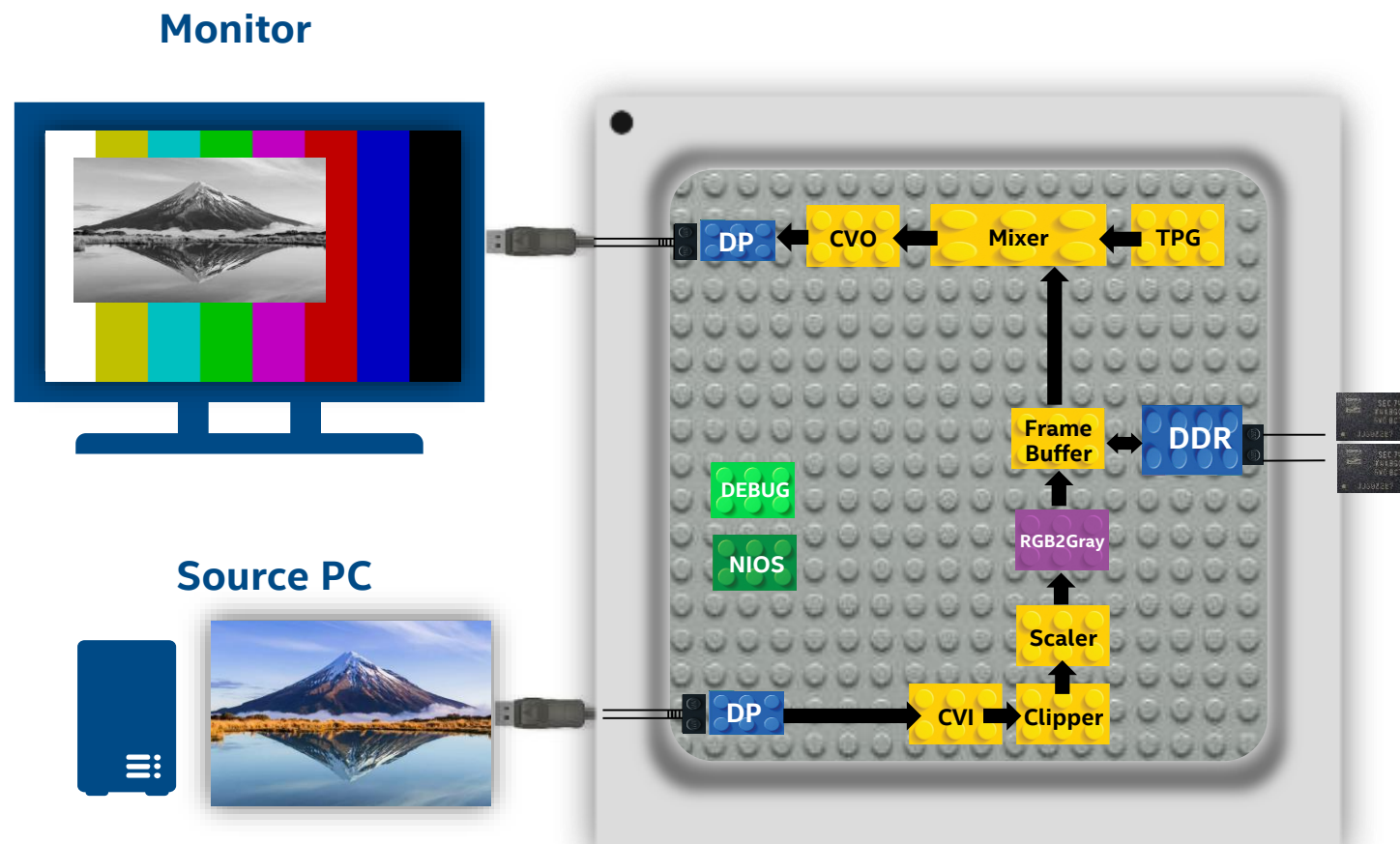
1. Building a video processing pipeline (Oct, 14th and 21st)
 - 1.1- DisplayPort loopback example design implementation
 - 1.2- Building our first video pipeline using VIP suite cores
 - 1.3- Complete End2End VIP pipeline
2. Strategies to debug a VIP pipeline (Nov, 4th)
 - Overview of system level considerations and key video concepts
 - Overview of Avalon-ST Video protocol
 - Bring up your pipeline using System Console
3. Integrate a simple custom component (Nov, 19th)
 - How to add your “secret sauce” to the application
 - Step flow on how to develop a custom component compliant with VIP
4. Adding On Screen Display overlay (Dec, 16th)
 - Use a lightweight graphic library with Nios
 - Add text and graphic content overlay on top of your live video

https://github.com/perezfra/VIP_webinars_Intel_FPGA

Building a Video Processing Pipeline

Previous Session 3 – Nov, 19th

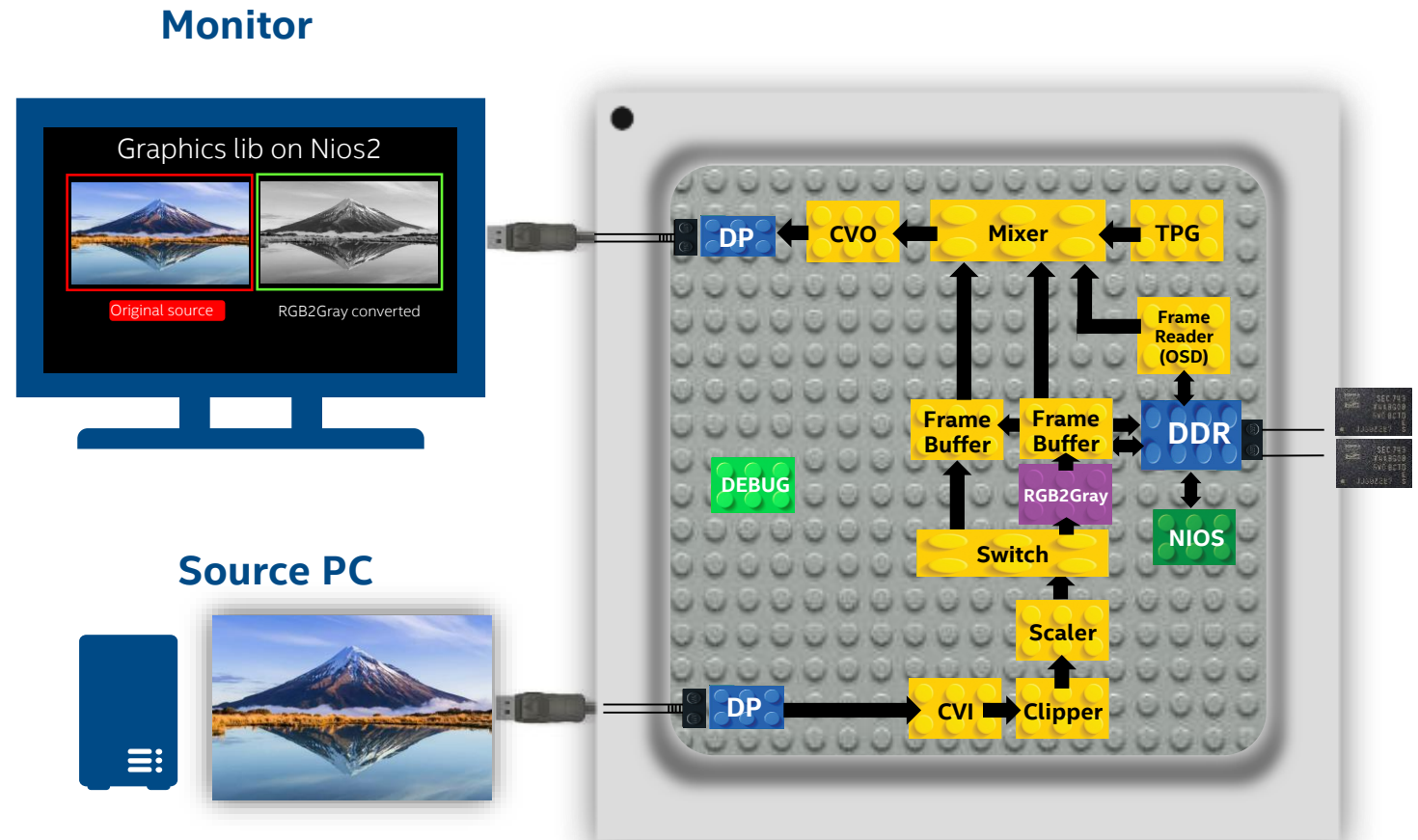
1. Build a video pipeline using VIP cores (cropping, scaling and mixing with a background) and debug
2. Develop and integrate a custom module to perform RGB to Grayscale conversion



Adding OSD overlay

Session 4 – Dec, 16th

1. Build a video pipeline using VIP cores (cropping, scaling and mixing with a background) and debug
2. Develop and integrate a custom module to perform RGB to Grayscale conversion
3. Duplicate video stream with switch and create PiP
4. Add a Frame reader to retrieve graphic frame from DDR3
5. Add new layers to mixer
6. Use a graphic lib on Nios2 to generate shapes and text



Adding OSD overlay

Motivations

- The VIP suite contains +20 different IP cores installed by default. The collection provides modules for basic and required manipulations: crop, scale, color space conversion, gamma correction, deinterlace, mix, ... But...
- How can you add graphics elements to the screen?
- How to add an operation menu, insert some text string to show information or display values?
- What if you need some alignment markers, or bounding boxes, ...?

Adding OSD overlay

Flow

- Insert a Frame Reader component to continuously read data from a specific memory space in the DDR3 bank.
- A Nios2 processor writes, on that same memory space, text and graphical content using a lightweight library
- The Frame Reader is configured to retrieve pixel information from the specific memory address and generates AvalonST-Video packets that are routed to a layer in the mixer.
- This layer has been configured to support alpha blending, so we can play with different transparency levels on the graphic content.

Adding OSD overlay

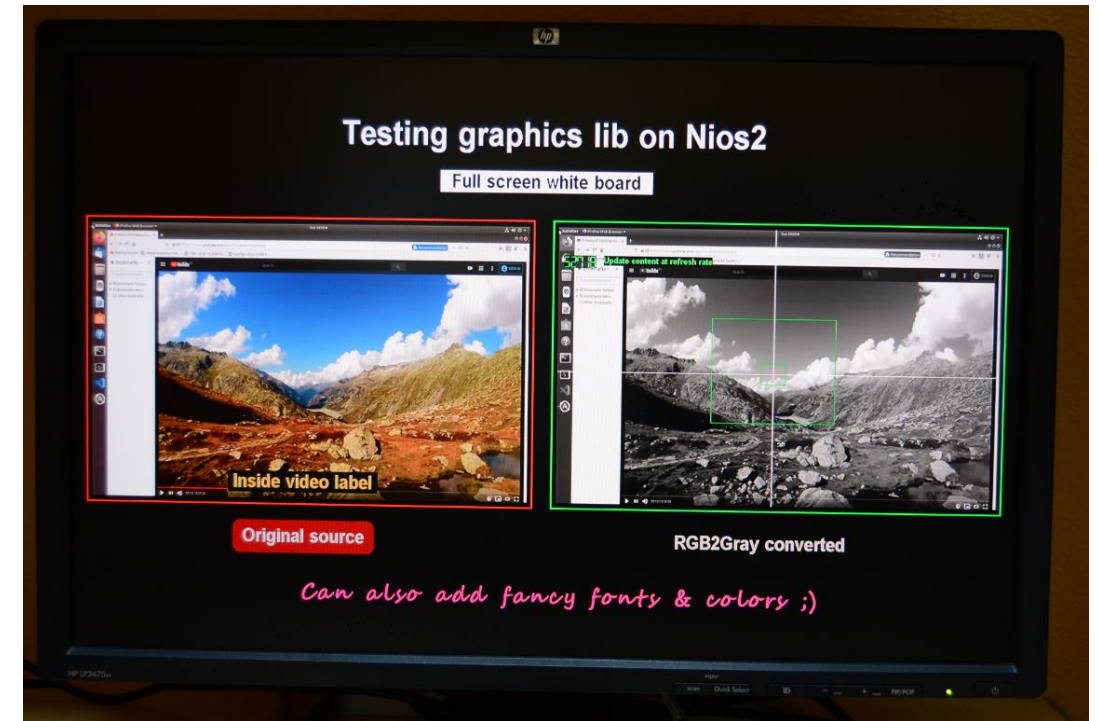
FPGA partitioning

- With FPGAs you can decouple your control and data planes and partition your application into blocks to be implemented in software programs or hardware logic in the FPGA fabric.
- We have implemented a frame reader component able to read back from memory at the required refresh of 1080p60 for the application to overlay graphic content on top of full screen video.
- Once configured, this Frame Reader acts autonomously, without any CPU intervention.
- The CPU is then in charge of updating the graphic content at its own pace, rendering information in the memory space allocated as graphic frame.

Adding OSD overlay

Final result

- In this session, we modify the VIP pipeline to include and configure the different hardware modules, as well as, add and use the graphic library in the software flow.
- We have duplicated the video data path to allow simultaneous visualization of the video source in 2 independent picture-in-picture windows: original source and gray scale converted version for comparison.
- We have created some basic text strings and rectangular boxes added on top of video.



Session 4 – Adding OSD overlay

HW implementation

Adding OSD overlay – HW flow

Setting up the Quartus project

- Extract the files in the **4_OSD_Overlay_v1.tar.gz** package and open the Quartus project located at
<extracted_folder>/quartus/c10_dp_demo.qpf



custom_ip



quartus



rtl



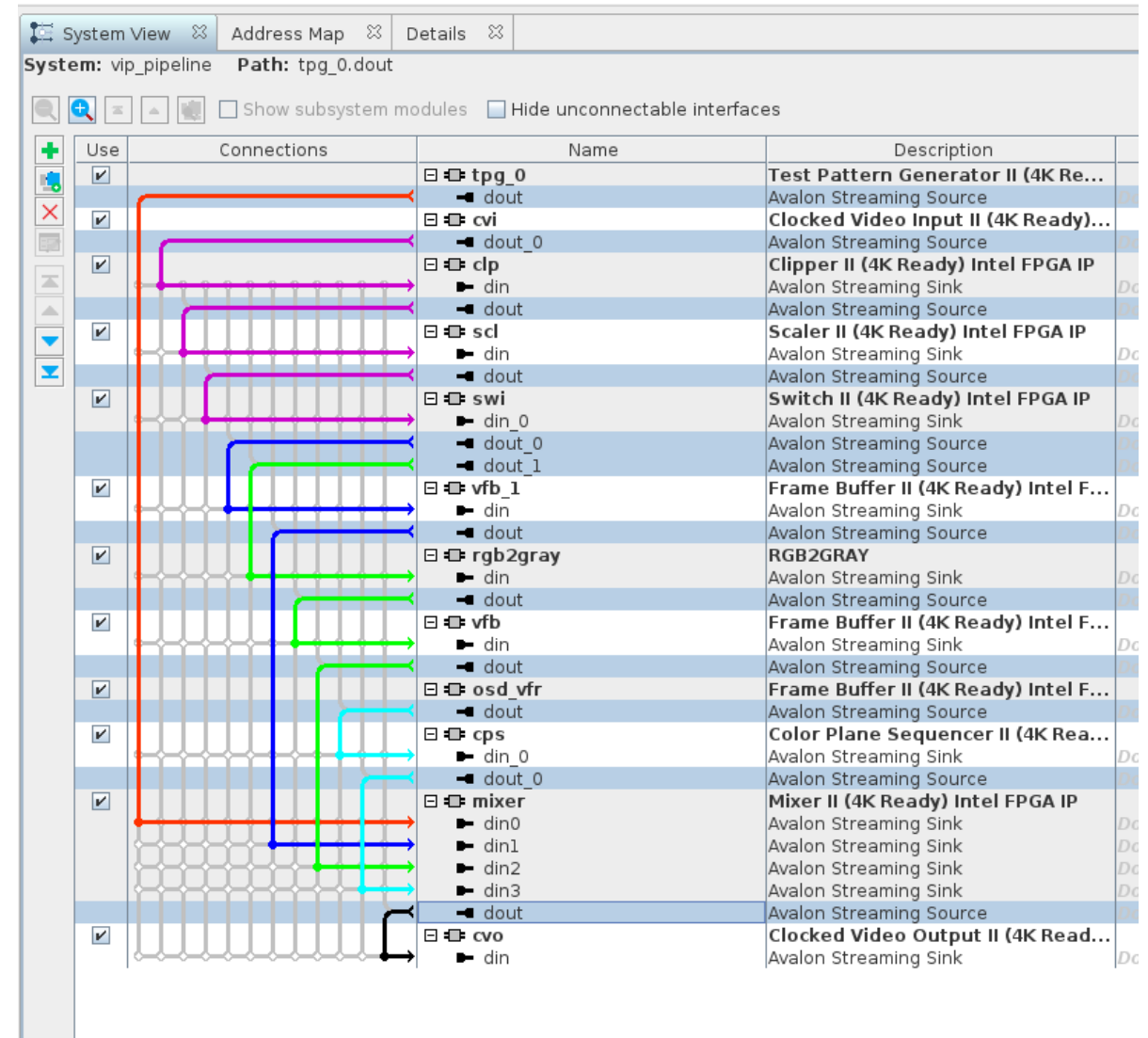
software

- Download the file from the github repo
 - https://github.com/perezfra/VIP_webinars_Intel_FPGA

Adding OSD overlay – HW flow

Understanding the pipeline 1/3

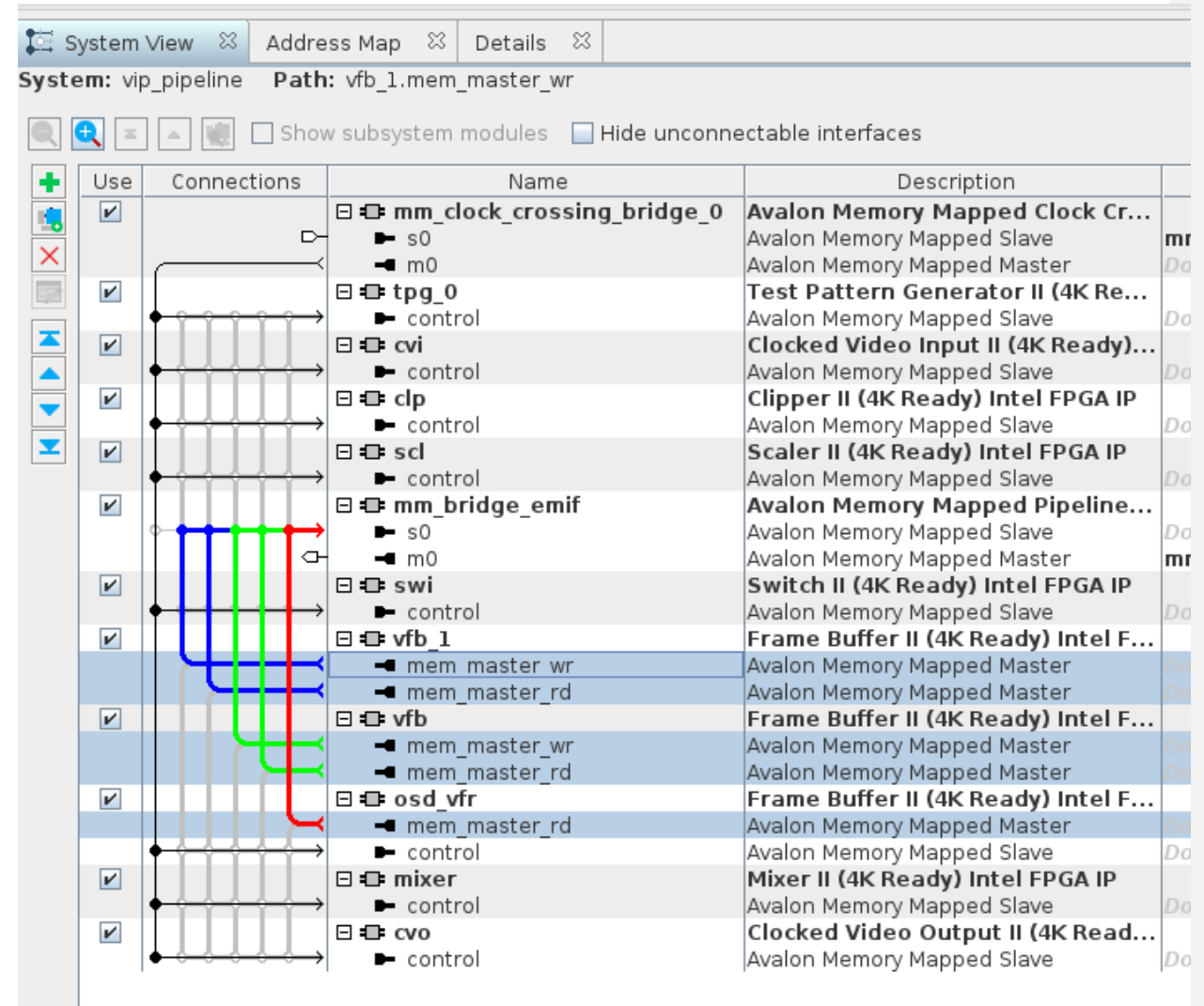
- Launch Platform Designer and select
<extracted_folder>/rtl/core/vip_pipeline.qsys to open
- Filter by **Avalon-ST Interfaces** to get a cleaner view on the video data path.



Adding OSD overlay – HW flow

Understanding the pipeline 2/3

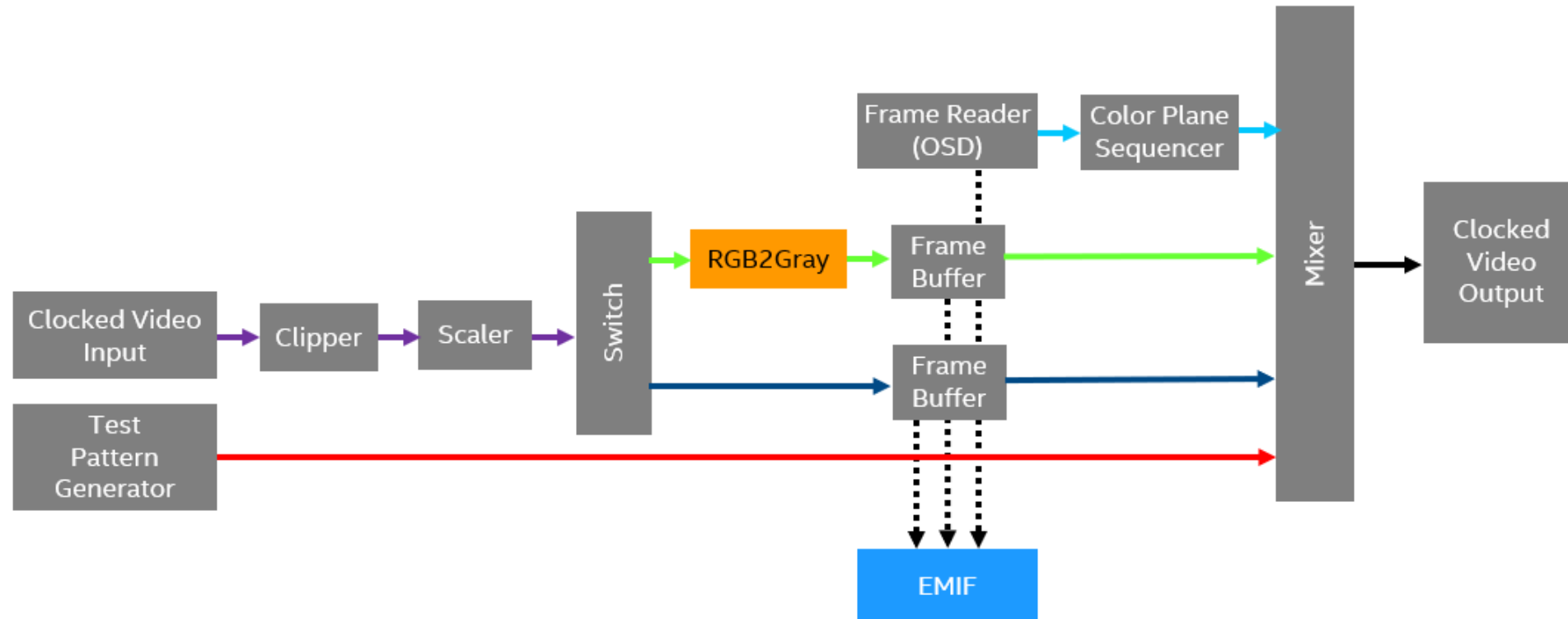
- Filter by **Avalon-MM Interfaces**
- Different Frame Buffer components share the same DDR3 bank
- Platform Designer automatically generates arbitration logic



Adding OSD overlay – HW flow

Understanding the pipeline 3/3

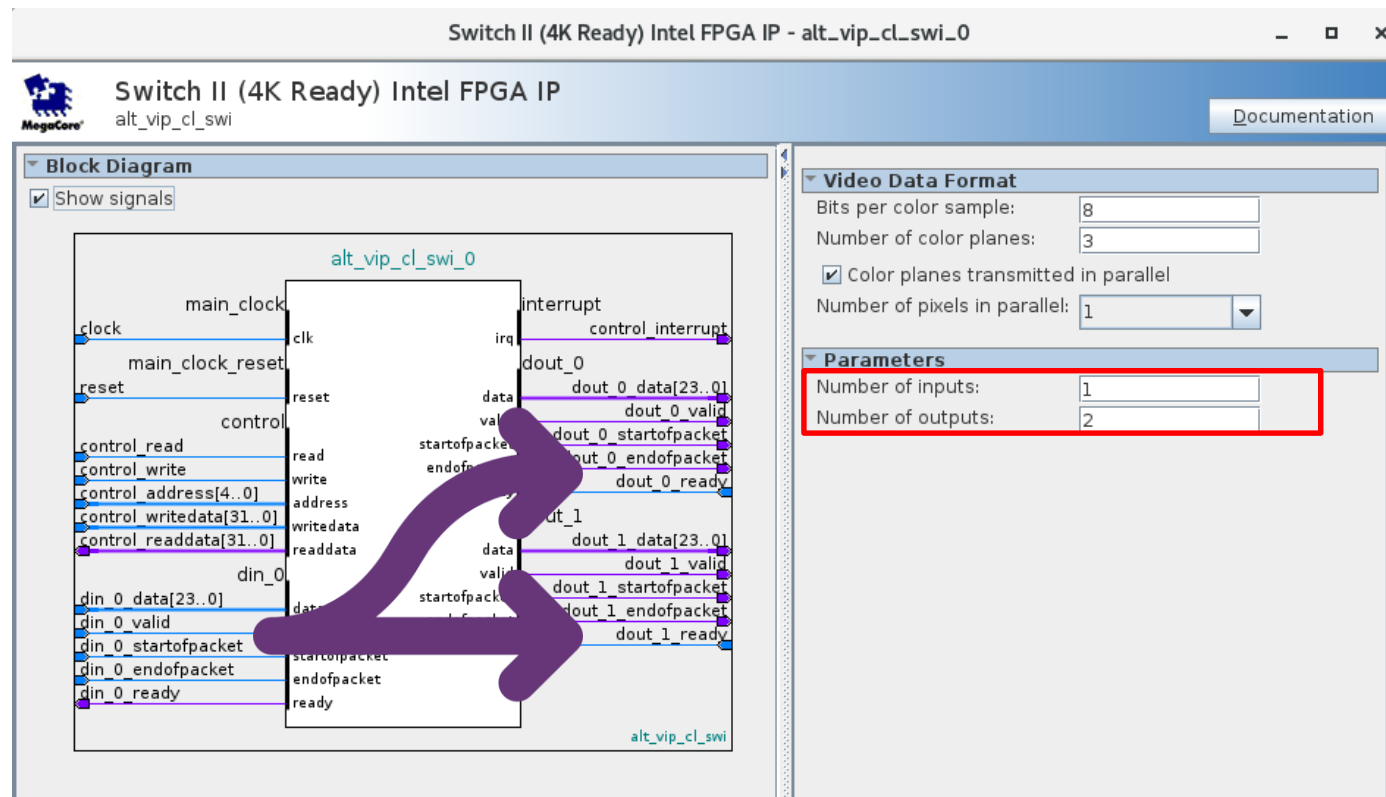
- Final diagram representation of the `vip_pipeline.qsys` subsystem



Adding OSD overlay – HW flow

Switch

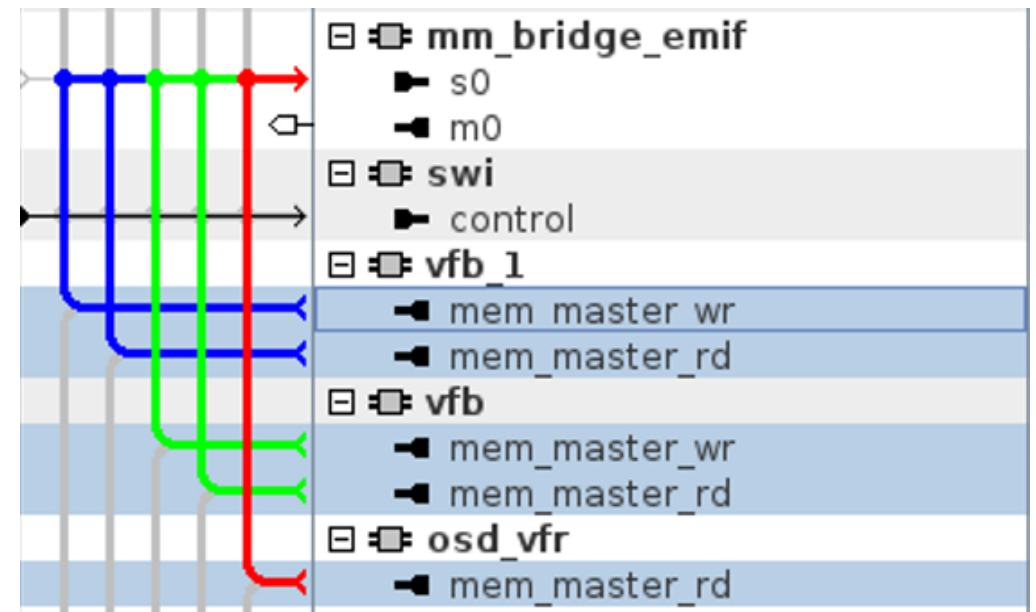
- Duplicate a video stream



Adding OSD overlay – HW flow

Memory Map – 1/7

- In the Cyclone10 GX devkit we have 1GB or DDR3: 0x0 <> 0x3fff_ffff
- In **`vip_pipeline.qsys`** we have 3 components connected to the pipeline bridge, that will be finally connected to the DDR3 emif in the **`dp_core.qsys`** subsystem
- Let's see how to configure each Frame Buffer



Adding OSD overlay – HW flow

Memory Map – 2/7

- If you need a refresh consider go back to the session
1.3_Building_Complete_Pipelines
where we explain all the details about Frame Buffer configuration
- We need to set the Frame buffer memory base address to be exclusive
- Enabling fixed inter-buffer offset has advantages in software development
- This is **vfb_1** used for original video source: 0x04000000

Frame Buffer II (4K Ready) Intel FPGA IP
alt_vip_cl_vfb

Video Data Format

Maximum frame width: 1920
Maximum frame height: 1080
Bits per color sample: 8
Number of color planes: 3
☒ Color planes transmitted in parallel
Number of pixels in parallel: 1
☐ Interlace support

Memory

☒ Use separate clock for the Avalon-MM master interface(s)
Avalon-MM master(s) local ports width: 256
FIFO depth Write: 64
Av-MM burst target Write: 32
FIFO depth Read: 64
Av-MM burst target Read: 32
☒ Align read/write bursts on read boundaries
Maximum ancillary packets per frame: 0
Maximum length ancillary packet in symbols: 10
Frame buffer memory base address: 0x04000000
☒ Enable use of fixed inter-buffer offset
Inter-buffer offset: 0x01000000

Adding OSD overlay – HW flow

Memory Map – 3/7

- Enable Frame Dropping and Repeating
- We have now 3 video frames allocated to fixed addresses
 - 0x04000000
 - 0x05000000
 - 0x06000000
- Let's do the same with the other video Frame Buffer

Optimization

- ☐ Prioritize Fmax over memory bandwidth

Frame Configuration

- ☐ Module is Frame Reader only
- ☐ Module is Frame Writer only
- ☒ Frame dropping
- ☒ Frame repeating
- Delay length (frames):
- ☐ Locked rate support
- ☒ Drop invalid frames
- ☐ Drop/repeat user packets

Control

- ☐ Run-time writer control
- ☐ Run-time reader control

Parameterization Messages

Type	Message
?	
i	Buffer 3 frames, storage required is 49152 kB (0x04000000 to 0x07000000)

Adding OSD overlay – HW flow

Memory Map – 4/7

- We use **vfb** component for our **rgb2gray** stream flow
- We set base address to 0x0
- Also enable fixed offset
- We have now 3 video frames allocated to fixed addresses
 - 0x00000000
 - 0x01000000
 - 0x02000000

The screenshot displays a configuration window for a video processing component. A red rectangle highlights the 'Frame buffer memory base address' set to 0x00000000 and 'Enable use of fixed inter-buffer offset' checked, with an 'Inter-buffer offset' of 0x01000000. Below this, the 'Optimization' section has 'Prioritize Fmax over memory bandwidth' unchecked. The 'Frame Configuration' section has 'Module is Frame Reader only' and 'Module is Frame Writer only' unchecked, 'Frame dropping' and 'Frame repeating' checked, 'Delay length (frames)' set to 1, 'Locked rate support' unchecked, 'Drop invalid frames' checked, and 'Drop/repeat user packets' unchecked. The 'Control' section has 'Run-time writer control' and 'Run-time reader control' unchecked. At the bottom, the 'Parameterization Messages' table shows a message: 'Buffer 3 frames, storage required is 49152 kB (0x00000000 to 0x03000000)', which is also highlighted by a red rectangle.

Type	Message
?	Buffer 3 frames, storage required is 49152 kB (0x00000000 to 0x03000000)

Adding OSD overlay – HW flow

Memory Map – 5/7

- `osd_vfr` has a special configuration as Frame Reader only
- 4 color planes to enable **ARGB**
- Base address to 0x08000000

Frame Buffer II (4K Ready) Intel FPGA IP
alt_vip_cl_vfb

Video Data Format

Maximum frame width: 1920
Maximum frame height: 1080
Bits per color sample: 8
Number of color planes: 4
☒ Color planes transmitted in parallel
Number of pixels in parallel: 1
☐ Interlace support

Memory

☒ Use separate clock for the Avalon-MM master interface(s)
Avalon-MM master(s) local ports width: 256
FIFO depth Write: 64
Av-MM burst target Write: 32
FIFO depth Read: 64
Av-MM burst target Read: 32
☒ Align read/write bursts on read boundaries
Maximum ancillary packets per frame: 0
Maximum length ancillary packet in symbols: 10
Frame buffer memory base address: 0x08000000
☒ Enable use of fixed inter-buffer offset
Inter-buffer offset: 0x01000000

Adding OSD overlay – HW flow

Memory Map – 6/7

- Frame Reader only
- Frame repeating
- Run-time reader control
- We have now 3 video frames allocated to fixed addresses
 - 0x08000000
 - 0x09000000
 - 0x0a000000

Optimization

- ☐ Prioritize Fmax over memory bandwidth

Frame Configuration

- ☒ Module is Frame Reader only
- ☐ Module is Frame Writer only
- ☐ Frame dropping
- ☒ Frame repeating
- Delay length (frames):
- ☐ Locked rate support
- ☐ Drop invalid frames
- ☐ Drop/repeat user packets

Control

- ☐ Run-time writer control
- ☒ Run-time reader control

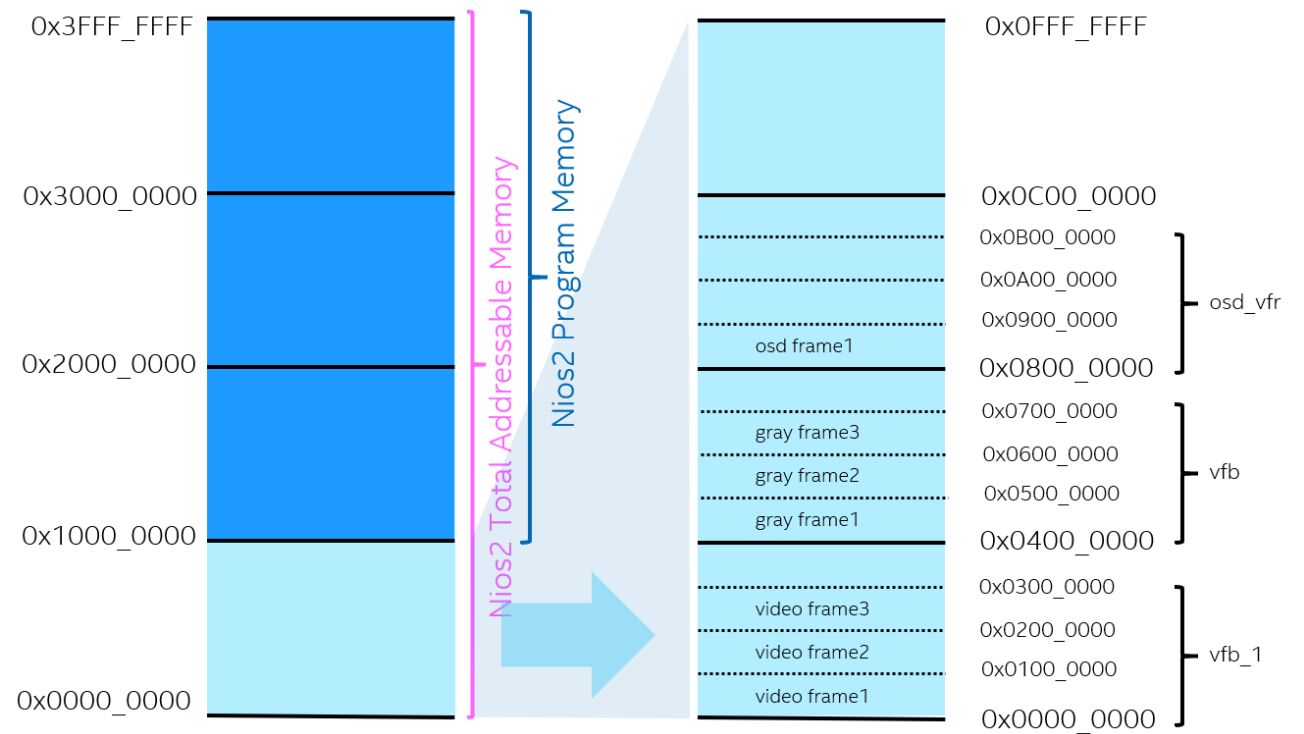
Parameterization Messages

Type	Message
?	
i	Buffer 3 frames, storage required is 49152 kB (0x08000000 to 0x0b000000)

Adding OSD overlay – HW flow

Memory Map – 7/7

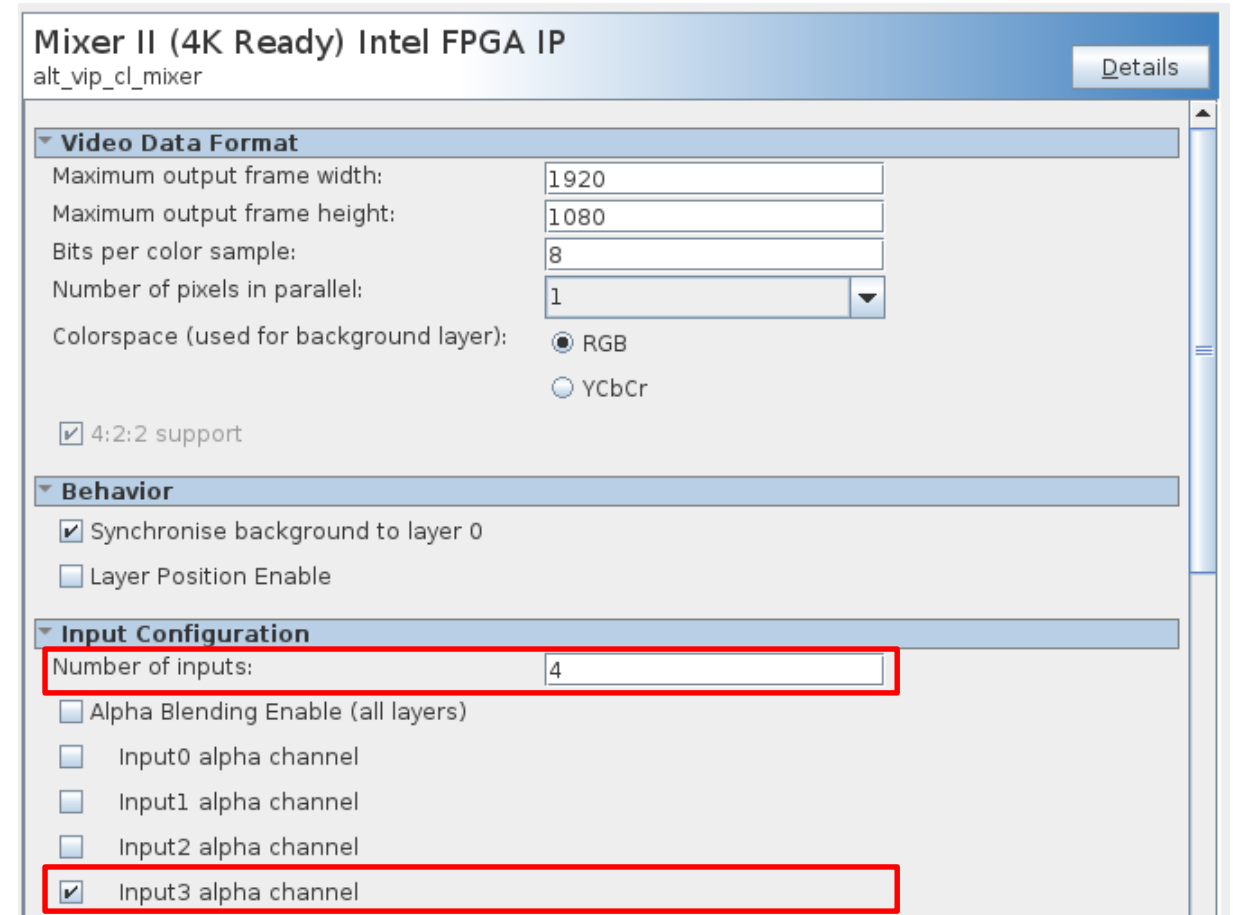
- DDR3 memory space sliced into different masters
 - Non-overlapping regions
- We allocate up to 0x1000_0000 for video memory
- Nios2 can address the total space, however program memory is set above 0x1000_0000



Adding OSD overlay – HW flow

Mixer – 1/3

- We enable 4 layers
 - Tpg, original, rgb2gray, osd
- We activate osd Alpha channel
- 3 Alpha modes
 - No blending, opaque
 - Static, run-time prog value
 - Per-pixel streaming
- More details in VIP User Guide
 - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_vip.pdf



Mixer II (4K Ready) Intel FPGA IP
alt_vip_cl_mixer Details

Video Data Format

Maximum output frame width: 1920
Maximum output frame height: 1080
Bits per color sample: 8
Number of pixels in parallel: 1
Colorspace (used for background layer): ☒ RGB ☐ YCbCr

☒ 4:2:2 support

Behavior

☒ Synchronise background to layer 0
☐ Layer Position Enable

Input Configuration

Number of inputs: 4

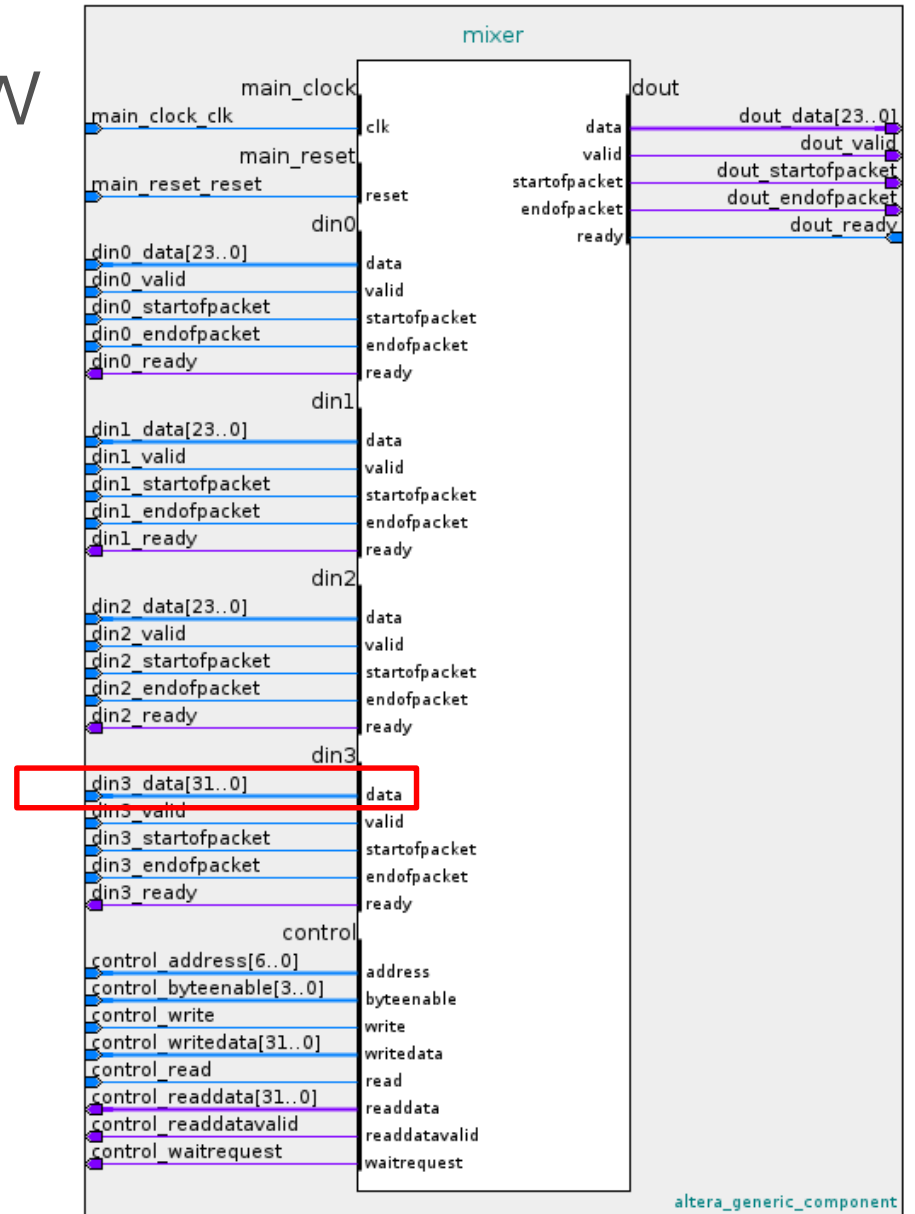
☐ Alpha Blending Enable (all layers)

☐ Input0 alpha channel
☐ Input1 alpha channel
☐ Input2 alpha channel
☒ Input3 alpha channel

Adding OSD overlay – HW flow

Mixer – 2/3

- When you turn the InputN alpha channel parameter, the IP core adds an extra symbol per-pixel for that input.
 - The least significant symbol is the alpha value.
- The valid range of alpha coefficients is 0 to 1, where 1 represents full translucence, and 0 represents fully opaque.
- The Mixer II IP core determines the alpha value width based on the bits per pixel per color parameter.
- For 8-bit alpha values
 - 255 full transparency
 - 0 fully opaque



Adding OSD overlay – HW flow

Mixer – 3/3

- When you turn the InputN alpha channel parameter, the IP core adds an extra symbol per-pixel for that input.

- The least significant symbol is the alpha value.

- For din3[31:0] the color plane mapping is the following:

$\text{Din3}[31:0] = \text{Red}[31:24], \text{Green}[23:16], \text{Blue}[15:8], \text{Alpha}[7:0]$

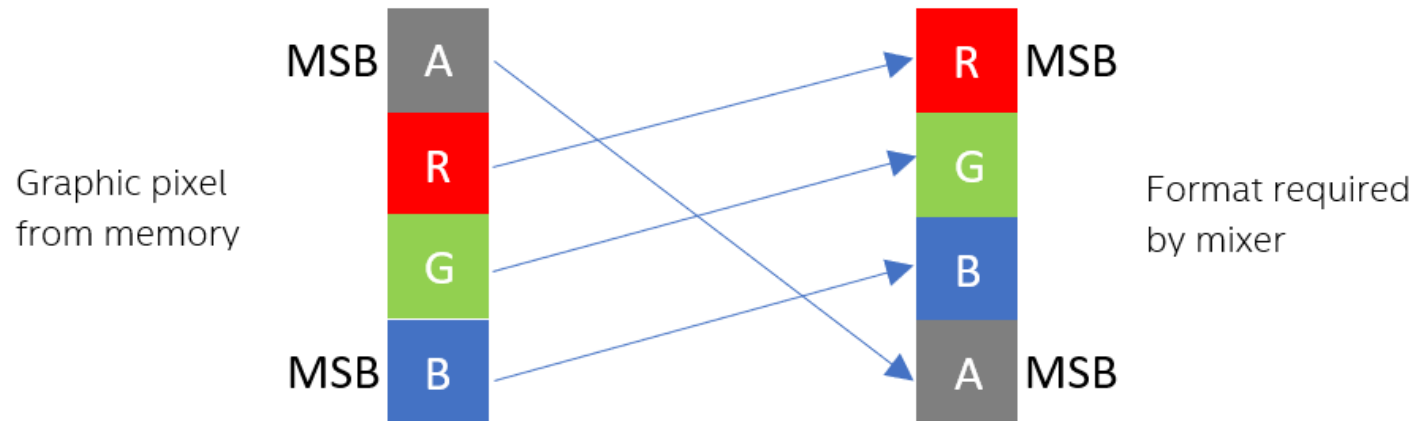
- But the graphic lib running on Nios writes pixels in the format:

$\text{Pixel_into_mem}[31:0] = \text{Alpha}[31:24], \text{Red}[23:16], \text{Green}[15:8], \text{Blue}[7:0]$

Adding OSD overlay – HW flow

Color Plane Sequencer – 1/2

- We need to make some color arrangements
- Use Color Plane Sequencer



Adding OSD overlay – HW flow

Color Plane Sequencer – 2/2

- 1 IN -> 1 OUT, 4 color planes >> Reassing components

Color Plane Sequencer II (4K Ready) Intel FPGA IP
alt_vip_cl_cps Details

General

How user packets are handled: ☐ No user packets allowed
☐ Discard all user packets received
☒ Pass all user packets through to the output

☐ Add extra pipelining registers

Interfaces

Bits per color sample: 8

Number of inputs: 1

Number of outputs: 1

din_0

☒ Add input fifo
Input fifo size: 8

Number of color planes: 4

☒ Color planes transmitted in parallel

Number of pixels in parallel: 1

☐ Specify an input pattern over two pixels

	Bits (31..24)	Bits (23..16)	Bits (15..8)	Bits (7..0)
Pixel 0	A	R	G	B
Pixel 1	inactive	inactive	inactive	inactive

dout_0

☒ Add output fifo
Output fifo size: 8

Number of color planes: 4

☒ Color planes transmitted in parallel

Number of pixels in parallel: 1

☒ Propagate user packets from input 0
☐ Propagate user packets from input 1
☐ Specify an output pattern over two pixels

	Bits (31..24)	Bits (23..16)	Bits (15..8)	Bits (7..0)
Pixel 0	R	G	B	A
Pixel 1	inactive	inactive	inactive	inactive

Adding OSD overlay – HW flow

Connecting the Nios2 CPU – 1/4

- Open **dp_core.qsys**
- Filter by Avalon-MM
- The **cpu** data and instruction masters are connected to **EMIF**
 - To execute the program
 - To write into graphic memory block (addressed by **osd_vfr**)

The screenshot shows the 'Address Map' window in Qsys for the system 'dp_core' at the path 'emif_c10_ddr3.ctrl_amm_0'. The window displays a table of components and their connections. The 'Use' column has checkboxes for each component, and the 'Connectio...' column shows the connection lines. The 'Name' and 'Description' columns provide details for each component.

Use	Connectio...	Name	Description
<input checked="" type="checkbox"/>		cpu	Nios II Processor
		data_master	Avalon Memory Mapped Master
		instruction_master	Avalon Memory Mapped Master
		debug_mem_slave	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		onchip_mem	On-Chip Memory (RAM or ROM) In...
		s1	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		jtag_uart	JTAG UART Intel FPGA IP
		avalon_jtag_slave	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		sys_clock_timer	Interval Timer Intel FPGA IP
		s1	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		sysid	System ID Peripheral Intel FPGA IP
		control_slave	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		i2c_master	Avalon I2C (Master) Intel FPGA IP
		csr	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		dp_rx	dp_rx
		dp_rx_mgmt_bridge_s0	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		dp_tx	dp_tx
		dp_tx_mgmt_bridge_s0	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		vip_pipeline	vip_pipeline
		mm_bridge_emif_m0	Avalon Memory Mapped Master
		mm_clock_crossing_bridge_0_s0	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		emif_c10_ddr3	External Memory Interfaces Intel...
		ctrl_amm_0	Avalon Memory Mapped Slave
<input checked="" type="checkbox"/>		jtag_avmm_master	JTAG to Avalon Master Bridge Int...
		master	Avalon Memory Mapped Master

Adding OSD overlay – HW flow

Connecting the Nios2 CPU – 2/4

- CPU can address the complete 1GB DDR3 space
- We need to map the program memory out of the video space
 - Configure cpu vectors

The screenshot shows the 'Address Map' window with a table of memory mappings. The table has three columns: 'Slave', 'cpu.data_master', and 'cpu.instruction_master'. The 'emif_c10_ddr3.ctrl_amm_0' entry is highlighted with a red box, indicating its mapping to the full address space (0x0000_0000 - 0x3fff_ffff) for both masters.

Slave	cpu.data_master	cpu.instruction_master
cpu.debug_mem_slave	0x4010_3800 - 0x4010_3fff	0x4010_3800 - 0x4010_3fff
emif_c10_ddr3.ctrl_amm_0	0x0000_0000 - 0x3fff_ffff	0x0000_0000 - 0x3fff_ffff
i2c_master.csr	0x4010_4000 - 0x4010_403f	
jtag_uart.avalon_jtag_slave	0x4010_4068 - 0x4010_406f	
onchip_mem.s1	0x4008_0000 - 0x400c_5bff	0x4008_0000 - 0x400c_5bff
sys_clock_timer.s1	0x4010_4040 - 0x4010_405f	
sysid.control_slave	0x4010_4060 - 0x4010_4067	
dp_rx.dp_rx_mgmt_bridge_s0	0x4010_2000 - 0x4010_2fff	
dp_tx.dp_tx_mgmt_bridge_s0	0x4010_1000 - 0x4010_1fff	
vip_pipeline.mm_clock_crossing_bridge_0_s0	0x4010_0000 - 0x4010_0fff	

Adding OSD overlay – HW flow

Connecting the Nios2 CPU – 3/4

- Add offset to Reset and Exception vectors
- Linker will map program symbols (code & data) starting at 0x1000_0000

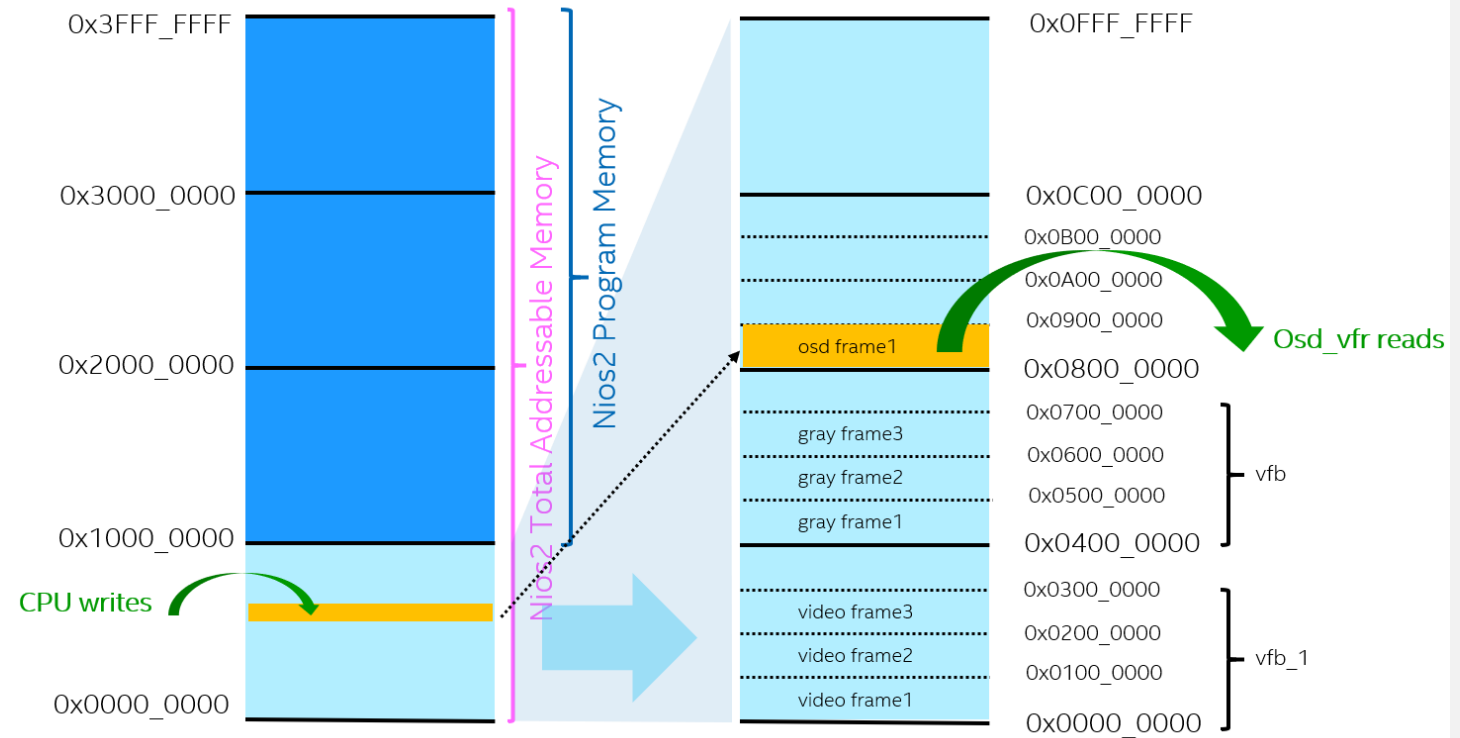
The screenshot shows the 'Nios II Processor' configuration window for 'altera_nios2_gen2'. The 'Vectors' tab is selected. It contains three sections: 'Reset Vector', 'Exception Vector', and 'Fast TLB Miss Exception Vector'. In the 'Reset Vector' section, the 'Reset vector memory' dropdown is set to 'emif_c10_ddr3.ctrl_amm_0', the 'Reset vector offset' is '0x10000000', and the 'Reset vector' is '0x10000000'. In the 'Exception Vector' section, the 'Exception vector memory' dropdown is also set to 'emif_c10_ddr3.ctrl_amm_0', the 'Exception vector offset' is '0x10000020', and the 'Exception vector' is '0x10000020'. The 'Fast TLB Miss Exception Vector' section has 'Fast TLB Miss Exception vector memory' set to 'None', 'Fast TLB Miss Exception vector offset' set to '0x00000000', and 'Fast TLB Miss Exception vector' set to '0x00000000'. Red boxes highlight the memory and offset fields for the Reset and Exception vectors.

Section	Field	Value
Reset Vector	Reset vector memory:	emif_c10_ddr3.ctrl_amm_0
	Reset vector offset:	0x10000000
	Reset vector:	0x10000000
Exception Vector	Exception vector memory:	emif_c10_ddr3.ctrl_amm_0
	Exception vector offset:	0x10000020
	Exception vector:	0x10000020
Fast TLB Miss Exception Vector	Fast TLB Miss Exception vector memory:	None
	Fast TLB Miss Exception vector offset:	0x00000000
	Fast TLB Miss Exception vector:	0x00000000

Adding OSD overlay – HW flow

Connecting the Nios2 CPU – 4/4

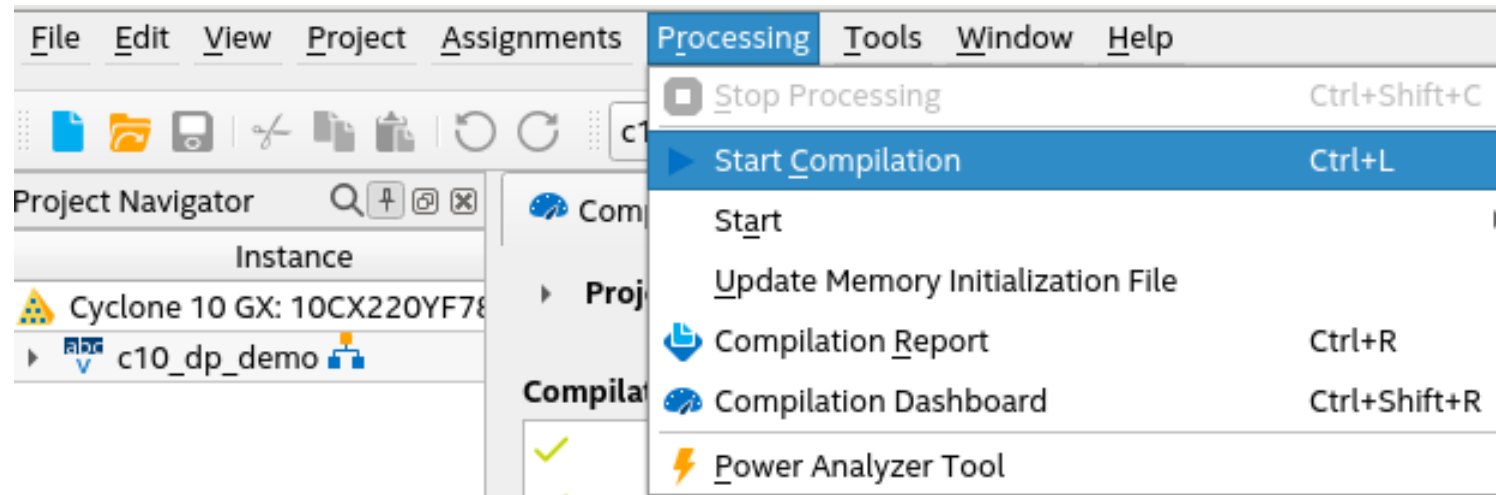
- Program memory is low bounded to 0x1000_0000
- But **cpu:data.master** still can access to full space
- We will create a pointer to 0x0800_0000 to write graphic information
- Then will be consumed by **osd_vfr** and sent to the mixer



Adding OSD overlay – HW flow

Generate bitstream

- Save **dp_core.qsys** and generate HDL files
- No need to modify top level file
- Processing->Start_Compilation



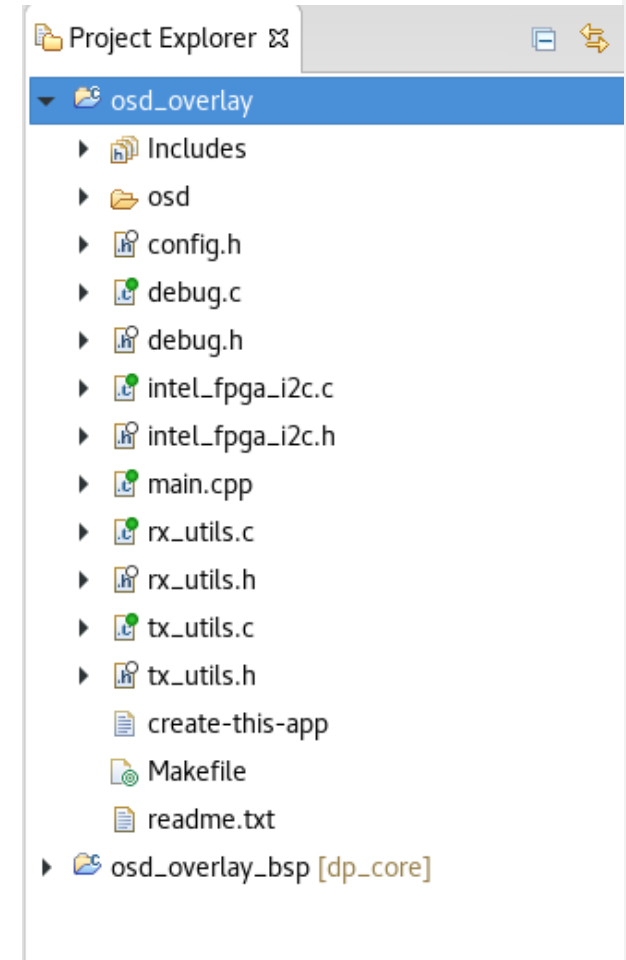
Session 4 – Adding OSD overlay

SW Development

Adding OSD overlay – SW flow

Create application and bsp

- As we did in previous sessions, generate the software application for Nios II processor using the supplied source code files.
 - Create a workspace folder under <project_dir>/software
 - In Eclipse, create a new application and bsp from template (**osd_overlay**)
 - Configure the bsp
 - Add DisplayPort libraries to the application
 - Copy files from **source** folder to **osd_overlay**
- For a comprehensive step guide checkout the `Session4_OSD_Overlay_lab_v1.pdf` manual in the repo
 - https://github.com/perezfra/VIP_webinars_Intel_FPGA



Adding OSD overlay – SW flow

Examine the code

- **source** folder content
- We have already familiar files
- **osd** folder contains the graphic lib implementation

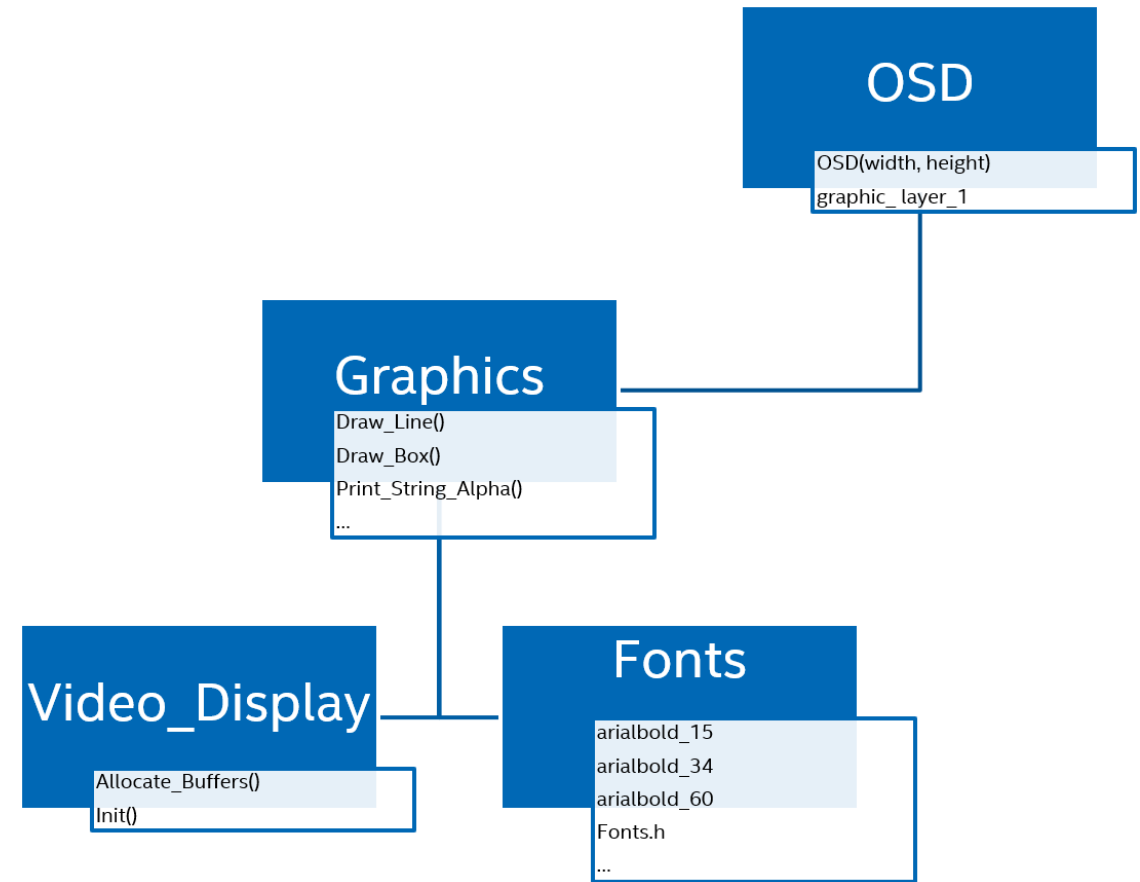


Adding OSD overlay – SW flow

Exploring the graphic library

■ osd folder content

- OSD class
- Graphics class
- Video_Display class
- fonts



Adding OSD overlay – SW flow

Configuring components in main.cpp – 1/3

- Include new components
 - `#include "Frame_Reader.hpp"`
 - `#include "Switch.hpp"`
- Create a Frame_Reader object
 - `Frame_Reader osd_vfr(VIP_PIPELINE_OSD_VFR_BASE, -1);` // From system.h, no interrupt
- Configure object parameters
 - `osd_vfr.set_frame_information(1920,1080,0);` // This is the resolution of our output image
 - `osd_vfr.set_frame_address(0x80000000);` // Frame Buffer Memory Base Address
 - `osd_vfr.start();` // Set the GO bit to start the component

Adding OSD overlay – SW flow

Configuring components in main.cpp – 2/3

■ Create a Switch object

- Switch `swi(VIP_PIPELINE_SWI_BASE);`

■ Configure object parameters

```
IOWR(VIP_PIPELINE_SWI_BASE,4,1); //Dout0 control, route din_0
IOWR(VIP_PIPELINE_SWI_BASE,5,1); //Dout1 control, route din_0
IOWR(VIP_PIPELINE_SWI_BASE,3,1); //Output Switch register, enable new values at the SWI output
swi.start();
```

■ From VIP User Guide

3	Output Switch	Writing a 1 to bit 0 indicates that the video output streams must be synchronized; and the new values in the output control registers must be loaded.
4	Dout0 Output Control	A one-hot value that selects which video input stream must propagate to this output. For example, for a 3-input switch: <ul style="list-style-type: none">• 3'b000 = no output• 3'b001 = din_0• 3'b010 = din_1• 3'b100 = din_2
5	Dout1 Output Control	As Dout0 Output Control but for output dout1.

Adding OSD overlay – SW flow

Configuring components in main.cpp – 3/3

- Create a Mixer object with 4 layers

- Mixer mixer(VIP_PIPELINE_MIXER_BASE, 4); // 4 layers mixer: background, original video, rgb2gray, osd

- Configuring the Mixer

```
173 mixer[0].set_offset(0, 0);           // Background layer offset 0,0
174 mixer[0].enable_layer();
175 mixer[1].set_offset(40, 300);        // PiP position of original (scaled) video
176 mixer[1].disable_layer();
177 mixer[2].set_offset(990, 300);       // PiP position of rgb2gray video
178 mixer[2].disable_layer();
179 mixer[3].set_offset(0,0);            // OSD layer offset to 0,0 for full screen coverage
180 mixer[3].disable_layer();
181 mixer[3].set_alpha_blending_mode(MixerLayer::IN_STREAM_ALPHA); // set the ALPHA mode for the layer
182
183 mixer.start();
```

Adding OSD overlay – SW flow

Initialize graphics library – 1/5

- Create a OSD object with full screen resolution
 - OSD osd(1920, 1080);
- OSD class declaration

```
20 class OSD {
21     /******
22      * Properties *
23      *****/
24     private:
25         int width;
26         int height;
27         long screen_pixel_count;
28     public:
29         Graphics graphic_layer_1;
30
31     /******
32      * Methods *
33      *****/
34     public:
35         OSD(int osd_width, int osd_height); // Constructor
36         ~OSD(void); // Destructor
37
38 };
39
```

Adding OSD overlay – SW flow

Initialize graphics library – 2/5

■ OSD constructor

```
20 /*
21  * Constructor
22  */
23 OSD::OSD(int osd_width, int osd_height){
24
25     width = osd_width;
26     height = osd_height;
27
28     if(graphic_layer_1.Init(width, height, VIDEO_DISPLAY_COLOR_DEPTH, 0x08000000, 1)){
29         printf("Memory allocation error (graphic_layer_1)");
30         while(1);
31     }
32
33     screen_pixel_count = width * height;
34
35     // Clear the frame buffer to initial content
36     // We set black color and full transparency
37     graphic_layer_1.Draw_Box(0,0,width,height,0x000000,1,0xFF);
38 }
```

VIDEO_DISPLAY_COLOR_DEPTH is declared as 32 (8 bits per ARGB color planes)

0x08000000 is the Frame Reader Memory Base Address we set at hardware configuration time.

Note that we set the same value in the software for consistency:

```
osd_vfr.set_frame_address(0x8000000);
```

Adding OSD overlay – SW flow

Initialize graphics library – 3/5

■ Graphics initialization

```
38 int Video_Display::Init(int width, int height, int color_depth, int buffer_location, int num_buffers){
39     int i, error;
40
41     // We'll need these values more than once, so let's pre-calculate them.
42     vd_bytes_per_pixel = color_depth >> 3; // same as /8
43     vd_bytes_per_frame = ((width * height) * vd_bytes_per_pixel);
44
45     // Fill out the display structure
46     vd_width = width;
47     vd_height = height;
48     vd_color_depth = color_depth;
49     vd_num_buffers = num_buffers;
50     vd_buffer_location = buffer_location;
51     vd_buffer_being_displayed = 0;
52     vd_buffer_being_written = 0;
53
54     // Allocate our frame and descriptor buffers
55     error = Allocate_Buffers();
56
57     vd_screen_base_address = ((int)(vd_buffer_ptrs[vd_buffer_being_written]->buffer));
58
59     return(error);
60 }
```

Allocate_Buffers() uses the internal property `vd_buffer_location` to remap the pointer.

Adding OSD overlay – SW flow

Initialize graphics library – 4/5

■ Buffers allocation

```
98 int Video_Display::Allocate_Buffers(void){
99     int i, ret_code = 0;
100
101     /* Allocate our frame buffers and descriptor buffers */
102     for(i=0; i<vd_num_buffers; i++){
103         vd_buffer_ptrs[i] = (video_frame*) malloc(sizeof(video_frame));
104
105         if(vd_buffer_ptrs[i] == NULL){
106             ret_code = -1;
107         }
108
109         if(vd_buffer_location == VIDEO_DISPLAY_USE_HEAP ) {
110             vd_buffer_ptrs[i]->buffer = (void*) alt_uncached_malloc((vd_bytes_per_frame));
111
112             if(vd_buffer_ptrs[i]->buffer == NULL)
113                 ret_code = -1;
114         }
115         else{
116             vd_buffer_ptrs[i]->buffer = (void*)(vd_buffer_location + (i * vd_bytes_per_frame));
117         }
118
119         vd_buffer_ptrs[i]->desc_base = ((void*) 0);
120     }
121
122     return ret_code;
123 }
```

creates a dynamic memory buffer of a video frame's size

uses the internal property `vd_buffer_location` to remap the pointer

Adding OSD overlay – SW flow

Initialize graphics library – 5/5

■ Clear the buffer

```
20 /*
21  * Constructor
22  */
23 OSD::OSD(int osd_width, int osd_height){
24
25     width = osd_width;
26     height = osd_height;
27
28     if(graphic_layer_1.Init(width, height, VIDEO_DISPLAY_COLOR_DEPTH, 0x08000000, 1)){
29         printf("Memory allocation error (graphic_layer_1)");
30         while(1);
31     }
32
33     screen_pixel_count = width * height;
34
35     // Clear the frame buffer to initial content
36     // We set black color and full transparency
37     graphic_layer_1.Draw_Box(0,0,width,height,0x000000,1,0xFF);
38 }
```

We draw a whole frame filled box to initialize random content to a black “transparent” color.

Adding OSD overlay – SW flow

Using the graphics library – 1/5

```
/* *****  
 * CLASS DEFINITION  
 * ***** */  
class Graphics : public Video_Display {  
    /* *****  
     * Properties *  
     * ***** */  
  
    /* *****  
     * Methods *  
     * ***** */  
public:  
    Graphics(); // Constructor  
    ~Graphics(); // Destructor  
  
    void* get_Graphic_Base_Address(void);  
  
    /* Graphical */  
private:  
    void Set_Pixel(int horiz, int vert, unsigned int color);  
    void Set_Round_Corner_Points(int cx, int cy, int x, int y, int straight_width, int straight_height, int color, char fill);  
    void Paint_Block(int horiz_start, int vert_start, int horiz_end, int vert_end, int color, char transparency);  
    void Draw_Horiz_Line(short horiz_start, short horiz_end, int vert, int color);  
    void Draw_Sloped_Line(unsigned short horiz_start, unsigned short vert_start, unsigned short horiz_end, unsigned short vert_end, int color);  
    void CopyImageToBuffer(char* dest, char* src, int src_width, int src_height);  
  
public:  
    void Draw_Line(int horiz_start, int vert_start, int horiz_end, int vert_end, int width, int color);  
    void Draw_Box(int horiz_start, int vert_start, int horiz_end, int vert_end, int color, int fill, char transparency);  
    void Draw_Rounded_Box(int horiz_start, int vert_start, int horiz_end, int vert_end, int radius, int color, int fill, char transparency);  
  
    /* Text */  
private:  
    inline void Seperate_Color_Channels(unsigned char * color, unsigned char * red, unsigned char * green, unsigned char * blue);  
    inline void Read_From_Frame(int horiz, int vert, unsigned char *red, unsigned char *green, unsigned char *blue);  
    inline void Alpha_Blending(int horiz_offset, int vert_offset, int background_color, unsigned char alpha, unsigned char *red, unsigned char *green, unsigned char *blue);  
    inline void Merge_Color_Channels(unsigned char red, unsigned char green, unsigned char blue, unsigned char * color);  
  
public:  
    void Print_Char_Alpha(int horiz_offset, int vert_offset, int color, char character, int background_color, font_struct font[]);  
    void Print_String_Alpha(int horiz_offset, int vert_offset, int color, int background_color, font_struct font[], const char string[]);  
    int Get_String_Pixel_Length_Alpha(font_struct font[], char string[]);  
};
```

Adding OSD overlay – SW flow

Using the graphics library – 2/5

■ Draw_Rounded_Box() example

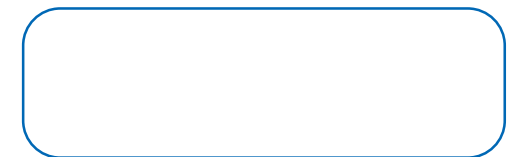
void Draw_Rounded_Box(**int** horiz_start, **int** vert_start, **int** horiz_end, **int** vert_end, **int** radius, **int** color, **int** fill, **char** transparency);

- **int** horiz_start: horizontal offset from the origin
- **int** vert_start: vertical offset from the origin
- **int** horiz_end: where to finish. Width can then be calculated as (horiz_end – horiz_start)
- **int** vert_end: where to finish. Height can then be calculated as (vert_end – vert_start)
- **int** radius: to apply on the rounded corners
- **int** color: color in RGB format (24bit) of the box
- **int** fill: '1' means filled with same color, '0' means only the outline is drawn
- **char** transparency: 0 means fully opaque, 255 means fully transparent. There are 255 possible transparency levels applicable.

filled = 1



filled = 0



Adding OSD overlay – SW flow

Using the graphics library – 3/5

■ Print_String_Alpha() example

```
void Print_String_Alpha(int horiz_offset, int vert_offset, int color, int background_color,  
font_struct font[], const char string[]);
```

- **int** horiz_offset: horizontal offset from the origin
- **int** vert_offset: vertical offset from the origin
- **int** color: foreground/font color
- **int** background_color: background color
- **font_struct** font[]: selected font (we are providing some sample fonts in the software application)
- **const char** string[]: text information to print as a string of characters.

Adding OSD overlay – SW flow

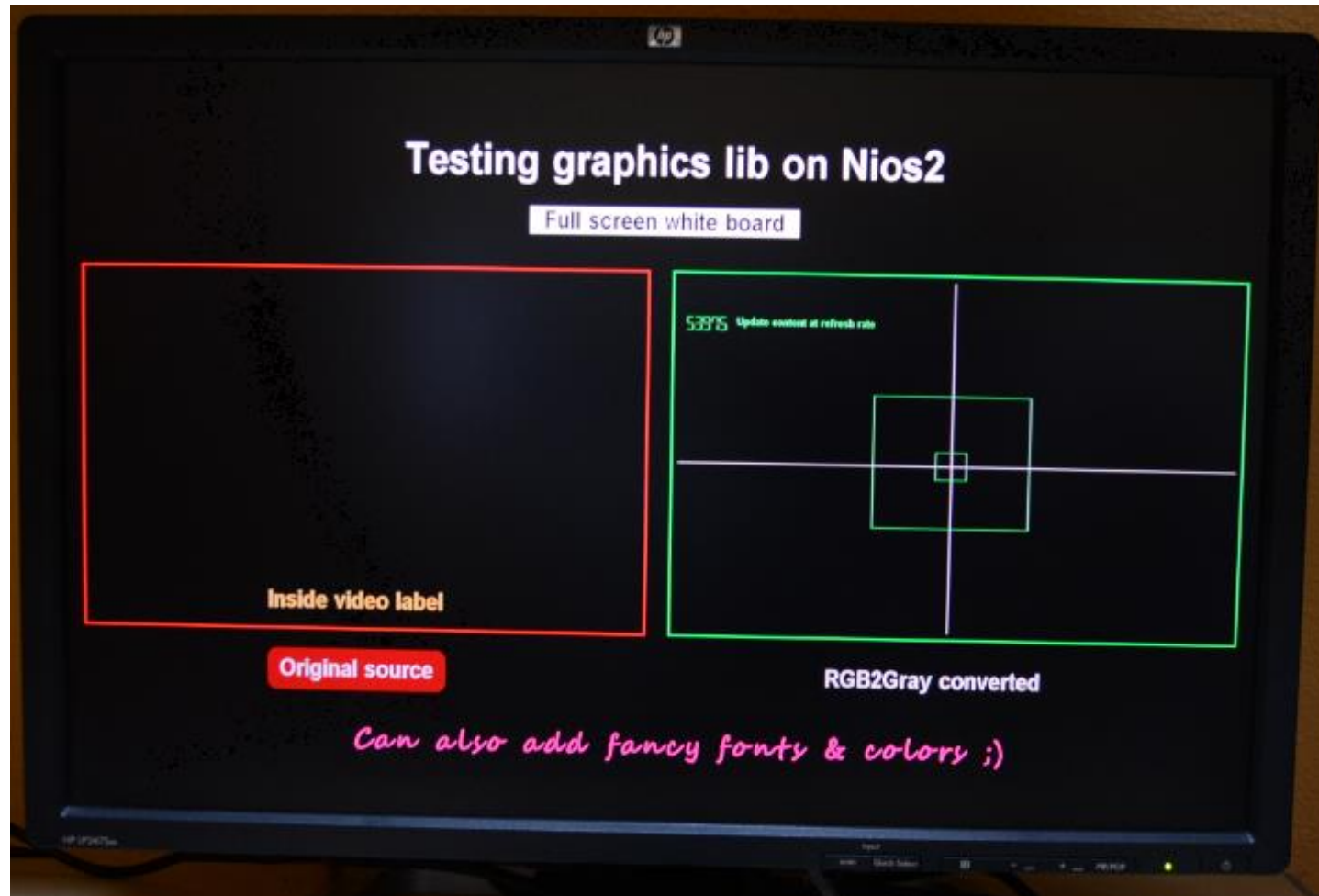
Using the graphics library – 4/5

■ Graphic composition example

```
232  osd.graphic_layer_1.Print_String_Alpha(550, 100, WHITE_24, BLACK_24, arialbold_60, "Testing graphics lib on Nios2");
233  osd.graphic_layer_1.Print_String_Alpha(750, 200, BLACK_24, WHITE_24, arialbold_34, " Full screen white board ");
234
235  osd.graphic_layer_1.Draw_Box(30,290,940,810,RED_24,0,0);
236  osd.graphic_layer_1.Draw_Box(29,289,941,811,RED_24,0,0);
237  osd.graphic_layer_1.Draw_Box(28,288,942,812,RED_24,0,0);
238
239  osd.graphic_layer_1.Draw_Box(980,290,1890,810,GREEN_24,0,0);
240  osd.graphic_layer_1.Draw_Box(979,289,1891,811,GREEN_24,0,0);
241  osd.graphic_layer_1.Draw_Box(978,288,1892,812,GREEN_24,0,0);
242
243
244  osd.graphic_layer_1.Draw_Rounded_Box(330,840,620,900,15,DARKRED_24,1,0);
245  osd.graphic_layer_1.Print_String_Alpha(350, 850, SILVER_24, DARKRED_24, arialbold_34, "Original source");
246
247  osd.graphic_layer_1.Print_String_Alpha(1230, 850, SILVER_24, BLACK_24, arialbold_34, "RGB2Gray converted");
248
249  osd.graphic_layer_1.Print_String_Alpha(320, 750, GOLDENROD_24, BLACK_24, arialbold_34, " Inside video label ");
250  osd.graphic_layer_1.Print_String_Alpha(1080, 350, GREEN_24, BLACK_24, arialbold_15, "Update content at refresh rate");
251
252  osd.graphic_layer_1.Print_String_Alpha(470, 940, DEEPPINK_24, BLACK_24, segoescriptbold_42, "Can also add fancy fonts & colors ;)");
253
254  osd.graphic_layer_1.Draw_Box(1400,540,1450,580,GREEN_24,0,0);
255  osd.graphic_layer_1.Draw_Box(1300,460,1550,650,GREEN_24,0,0);
256  osd.graphic_layer_1.Draw_Line(1425,300,1425,800,2,WHITE_24);
257  osd.graphic_layer_1.Draw_Line(990,560,1880,560,2,WHITE_24);
258
259  mixer[3].enable_layer();
```

Adding OSD overlay – SW flow

Using the graphics library – 5/5

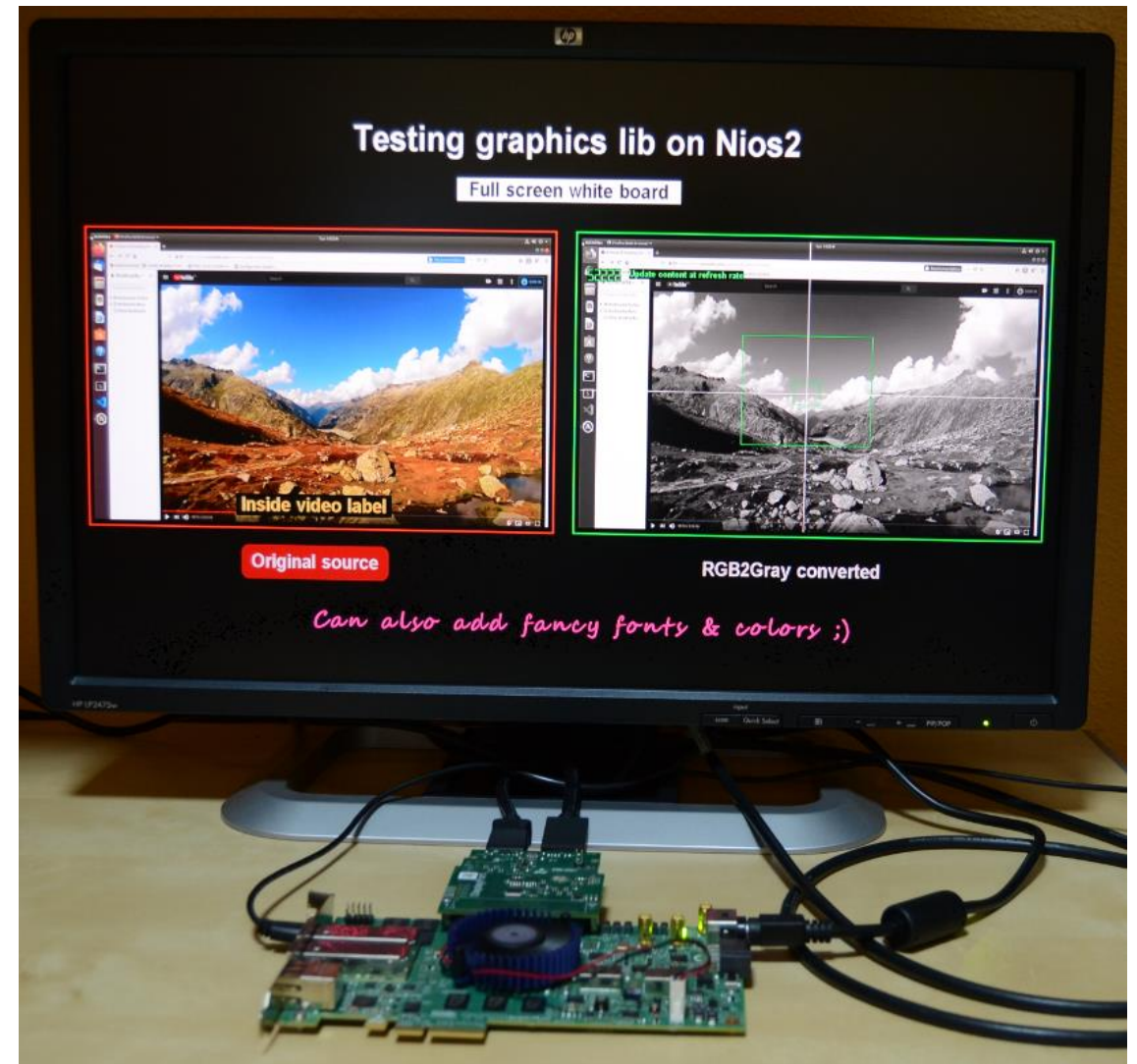


Session 4 – Adding OSD overlay

Running the application

Running the application

- Connect a display port video source and a monitor to the kit
- Open the Quartus programmer and download .sof
- In eclipse, launch the application for the Nios CPU
- See how the live captured video is converted to gray scale and displayed on the monitor



LIVE DEMO



Video processing on FPGAs made easy

Content available in the GitHub repo:

https://github.com/perezfra/VIP_webinars_Intel_FPGA

Summary

- We have followed the steps to create a video pipeline able to duplicate a video stream and apply different processing before getting them mixed in PiP in the global layout
- We have configured a Frame_Reader and the Mixer to allow overlay graphic content from a memory buffer with the live video
- We have learnt how to configure and use the graphic library to enrich the information we show on screen.

