# The Data Acquisition System of the Silicon Vertex Tracker for the Heavy Photon Search Experiment

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**Abstract**

The Heavy Photon Search (HPS) experiment at the Thomas Jefferson National Accelerator Facility (JLab) search for heavy photons which are new hypothesized massive vector bosons. The experiment consists of an electromagnetic calorimeter for triggering and particle identification and a a Silicon Vertex Tracker (SVT) for momentum and vertex position measurements. The data acquisition system (DAQ) for the SVT supports readout and processing of signals from 36 silicon strip sensors of the SVT. It also selects and transfers those events that were identified by the trigger system to the JLab DAQ for further event processing at rates approaching 50 kHz. Complex front-end electronics for digitization and power distribution are deployed inside the SVT vacuum box in order to reduce vacuum penetration count. A strong magnetic field used by the experiment also complicates the electronics design. The SLAC RCE Platform is utilized upstream to process and filter raw sensor data for delivery to the JLab DAQ. The system is currently deployed and running.

*Keywords:* data acquisition, atca, silicon, heavy photon, dark photon

**Contents**



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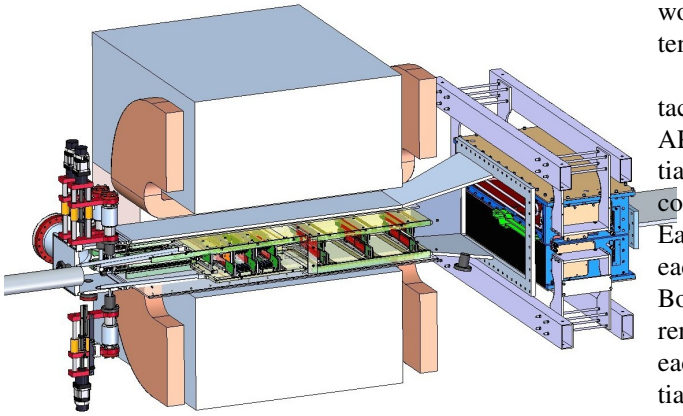

Figure 1: A rendered overview of the HPS detector.

## 1. Introduction

The Heavy Photon Search experiment (HPS) is a new fixed-target experiment [**?** ] specifically designed to discover an A′ with $m_{A'} = 20-500$ MeV, produced through bremsstrahlung in a tungsten target and decaying into an $e^+e^-$ pair. In particular, the HPS experiment has sensitivity to the challenging region with small cross sections out of reach from collider experiments and where thick absorbers, as used in beam-dump experiments to reject backgrounds, are ineffective due to the relatively short A′ decay length ($<$ 1 m) [**?** ]. This is accomplished by placing a compact silicon tracking and vertex detector (SVT) in a magnetic field, immediately downstream (10 cm) of a thin ($\sim$ 0.125% $X_0$) target to reconstruct the mass and decay vertex position of the A′. A rendered overview of HPS is shown in Fig. 1.

HPS runs in Hall B at Thomas Jefferson National Accelerator Facility (JLab) using the CEBAF accelerator electron beam with an energy of 1.05 GeV and 50 nA current, with planned operation of up to 6.6 GeV and 450 nA. The kinematics of A′ production typically result in final state particles within a few degrees of the beam, especially at low $m_{A'}$ . Because of this, the detector must accommodate passage of the beam downstream of the target and operate as close to the beam as possible. Because background rates in this region from the scattered beam are very large, a fast lead-tungstate crystal calorimeter trigger with 250 MHz flash ADC readout [**?** ] and excellent time tagging of hits is used to trigger on interesting events and reduce the bandwidth required to transfer data from the detector. This method of background reduction is the motivation for operating HPS in a nearly continuous beam: in a beam with large per-bunch charge, background from a single bunch would fully occupy the detector at the required beam intensity.

The SVT comprises 36 silicon strip sensors, each attached to a hybrid board incorporating five 128-channel APV25 front-end ASICs. The APV25 ASIC was initially developed for the Compact Muon Solenoid silicon tracker at the Large Hadron Collider at CERN [2]. Each hybrid board has five analog output lines (one for each of the APV25 ASICs) which are sent to Front End Boards (FEBs) using low power LVDS differential current sig-nals over about 1 m of twisted pair cable. At each FEB, a pre-amplifier scales the APV25 differential current output to match the range of a 14-bit Analog to Digital Converter (ADC). Both the ADCs and the APV25s operate at the system clock frequency of 41.667 MHz. There are 10 FEBs deployed in the SVT, each serving up to four hybrids. Each FEB also distributes low voltage power and high voltage bias to each attached hybrid. The deployment of readout electronics within the experiment vacuum chamber and 2 T magnetic field presents many challenges for the DAQ system design. The SLAC RCE general purpose DAQ System [3] is utilized on the back end for data filtering, formatting, and transmission for storage. An electro-magnetic calorimeter downstream of the SVT issues readout triggers through the JLab timing system

There should be a list of requirements and design goal for the DAQ listed below. These can be addressed and referred to in the later sections.

- S/N, number of channels
- time resolution
- trigger rate
- data rate
- integration with JLab DAQ
- radiation hardness
- operation, maintenance and longevity

## 2. The Heavy Photon Search Experiment

### *2.1. Electromagnetic Calorimeter Trigger*

### *2.2. The Silicon Vertex Tracking Detector*

The Silicon Vertex Tracker (SVT) allows for precise and efficient reconstruction of charged particles and their trajectories. At beam energies between 1.0-6.6 GeV, the electron and positron from the A′ decay will be produced with momenta in the range of 0.4-2 GeV/$c$ and angles of 10-100 mrad from the beam. The

| Layer → | 1-3 | 4-6 |
|---|---|---|
| $z$ pos. (cm) | 10-30 | 50-90 |
| Stereo angle (mrad) | 100 | 50 |
| Non-bend plane resolution ($\mu$m) | $\approx 6$ | $\approx 6$ |
| Bend plane resolution ($\mu$m) | $\approx 60$ | $\approx 120$ |

Table 1: Main tracker parameters.

dominant tracking uncertainty in this regime is multiple Coulomb scattering, so the SVT needs to minimize the amount of material in the tracking volume. With an approximate goal of 2% mass resolution in the 1 m long tracking volume (determined by an existing magnet and vacuum chamber) with 0.25 T magnetic field (for 1 GeV beam energy); 1% $X_0$ or less material per 3D tracking hit and six layers was deemed adequate. For weak couplings, the A′ may be long-lived and the $e^+e^-$ pair decay vertex might be displaced several cm downstream of the target foil. To discover rare A′ displaced decays, the SVT typically needs a prompt rejection of roughly $10^7$ at 1 cm vertex resolution [**?** ]. In order to reach that performance, the first layer of the SVT needs to be placed 10 cm from the target. At that distance, the large hit rates from beam electrons undergoing Coulomb scattering in the target allow placing the first layer 1.5 mm from the beam. No instrumentation can be placed inside that 15 mrad angle creating a "dead zone" throughout the experiment. The expected radiation dose peaks at $10^{15}$ electrons/cm$^2$/month, or roughly $3 \times 10^{13}$ 1 MeV neutron equivalent/cm$^2$/month [**?** ], close to the beam and places further constraints on the sensor technology. Furthermore, the whole tracker has to operate in vacuum to avoid secondary backgrounds from beam gas interactions, and have retractable tracking planes and easy access for sensor replacement to increase safety. Given the high hit density, the fast time response, and good resolution and radiation hardness needed; silicon microstrip sensors are the technology of choice for the tracker. Pixel sensors suitable for instrumenting our large acceptance are either too slow or have an unacceptable material budget.

The SVT overall layout is rendered in Fig. 2 and summarized in Tab. 1. Each of the six tracking layers, arranged in two halves both above and below the beam to avoid the "dead zone", consists of silicon microstrip sensors placed back-to-back. The first three layers have a 100 mrad stereo angle between the sensors and the last three have 50mrad in order to improve the pointing resolution to the vertex. The first layer is located only 10 cm downstream of the target to give excellent 3D vertexing performance which, with the 15 mrad dead zone above

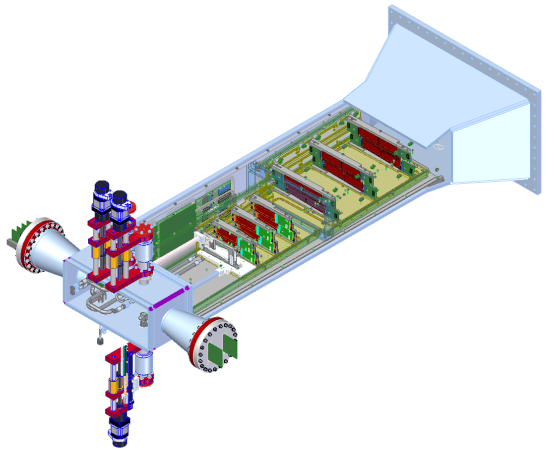

Figure 2: A rendered overview of the SVT installed on the beamline.

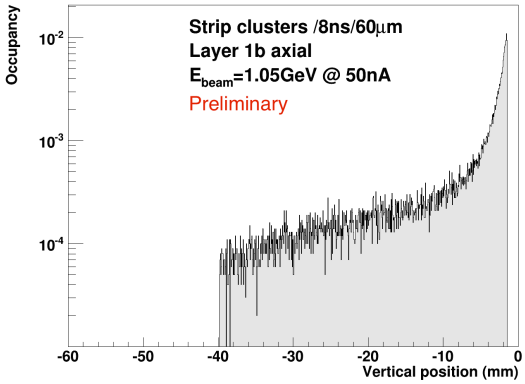


Figure 3: Background occupancy for layer 1 during nominal operation conditions.

and below the beam axis, puts the active silicon only 1.5 mm from the center of the beam. Hit densities in the most active region reach 4 MHz/mm$^2$ and about 1% occupancy for the strips closest to the beam, see Fig. 3.

## 3. Data Acquisition System

Discussion about the specific requirements that the DAQ have to fulfill. The description of HPS and the SVT should be enough to be able to give this section a solid context.

### *3.1. Overview*

Analog samples at 41.667 MSPS from the APV25 chips are sent on twisted pair magnet wire to a total of 10 Front End Boards (FEB) seen in Fig. 10. Each FEB digitizes and transfers data, from up to four hybrids,

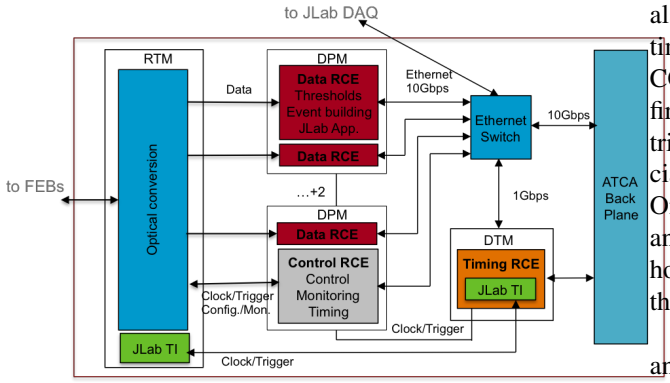


Figure 4: Schematic overview of the SVT DAQ.

at up to 3.3 Gb/s using high-speed serial links to Xilinx Zynq based data processing modules on the ATCA based SLAC RCE platform [1] for zero suppression and event building. Each FEB also handles power regulation and monitoring as well as high voltage sensor bias distribution to each of the attached hybrids. To shorten the analog signal distance, the FEBs are placed inside the vacuum chamber, pressed against thermal pads on each side of a 1/2" cooled support plate on the upstream positron side, rendering a less intense radiation environment. Borated high-density polyethylene is used to further lower the risk of damage from radiation emitted by the nearby target. Data from the FEBs are routed via short, flexible miniSAS cables to four flange boards. These are FR4 boards potted through slots in the 8" vacuum flange on the upstream positron side of the vacuum box. On the out side of the boards, signals are converted to optical and transferred to the DAQ platform about 30 m away. A similar mechanical technique is used on the opposite side of the vacuum box to bring in low voltage power and high voltage sensor bias into the chamber; this can be seen in Fig. 12.

An overview of the data flow across the RCE platform is shown in Fig. 4. Data from 10 FEBs are split and sent to 14 processing nodes on two ATCA blades, called COBs (Cluster on board). The processing nodes, known as Reconfigurable Cluster Elements (RCE) are based on Xilinx Zync 7000 series system-on-chip which has a dual ARM Cortex A9 processor tightly coupled to a 28nm FPGA fabric. The independent operating nodes receive data from up to four hybrids, apply calibrated thresholds and build event frames in the firmware. A readout application from the JLab DAQ [3], running on the ARM processor, pulls the event frames from memory via DMA and transfers the event frames to the JLab DAQ event builder over 10 Gb/s ethernet. The COB also hosts a special RCE that handles the trigger and timing distribution across the processing nodes on each COB. This RCE implements the JLab trigger interface firmware and accepts the master clocks together with trigger information from the JLab DAQ from a special fiber attached on the custom rear transition board. One of the RCEs is allocated to handle control, trigger and timing signals to and from all the hybrids. It also hosts the slow control and environmental interfaces to the EPICS control system.

During running the system operated at about 20 kHz and with data rates up to 150 MB/s. It has been tested to 50 kHz and 200 MB/s.

### 3.2. *Sensors and Front-End Readout*

The sensors are $p$+-on-$n$, single-sided, AC-coupled, polysilicon-biased microstrip sensors fabricated by Hamamatsu Photonics Corporation for the cancelled DØ Run 2b upgrade [**?** ]. These 320 $\mu$m thick sensors are $4 \times 10$ cm$^2$ with 30 and 60 $\mu$m pitch for sense and readout strips, respectively, matching the required material budget and single hit spatial resolution. The sensors were qualified to withstand at least 1 kV bias in order to tolerate the $1.5 \times 10^{14}$ 1 MeV neutron equivalent/cm$^2$ for a six month run without significant degradation.

One of the key requirements for the SVT is hit time resolution of $< 2$ ns in order to reject background and improve pattern recognition accuracy for close to the beam where occupancies are high. This is achieved by using the APV25 front-end readout ASIC [**?** ], developed for the Compact Muon Solenoid experiment at the Large Hadron Collider. The APV25 is an analog pipeline ASIC with 128 channels of preamplifier and shaper, feeding a 192 long analog memory pipeline. In the so-called "multi-peak" readout mode, the APV25 presents three consecutive samples of the pulse height in response to an APV25 readout trigger signal. By sending two APV25 readout triggers for every event trigger signal from the electromagnetic calorimeter, six analog samples of the pulse shape, see Fig. 8, are obtained at a sampling rate of 41 MSPS. This pulse shape can be analyzed and fitted to extract the $t_0$ of the hit [**?** ]. The main parameters of the APV25 ASIC are shown in Tab. 2: the 44 $\mu$m pitch, low noise and operation using either polarity together with the proven robustness and radiation hardness is a good fit for HPS. The sensor and APV25 chip can be seen in Figure 6.

### 3.3. *Hybrid*

The SVT modules are built by placing two identical, so-called half-modules back-to-back at a stereo angle.

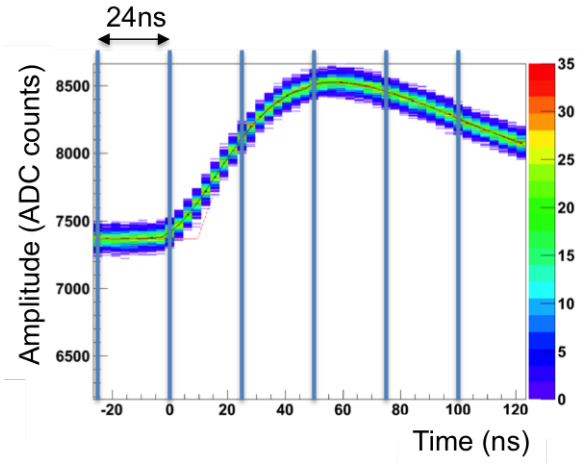


Figure 5: Pulse shape of the APV25 ASIC.

| | |
|---|---|
| Technology | 0.25 $\mu$m |
| Channels | 128 |
| Input pitch | 44 $\mu$m |
| Noise [ENC $e^-$] | 270 + 36×C (pF) |
| Power consumption | 350mW |

Table 2: Main APV25 ASIC parameters.

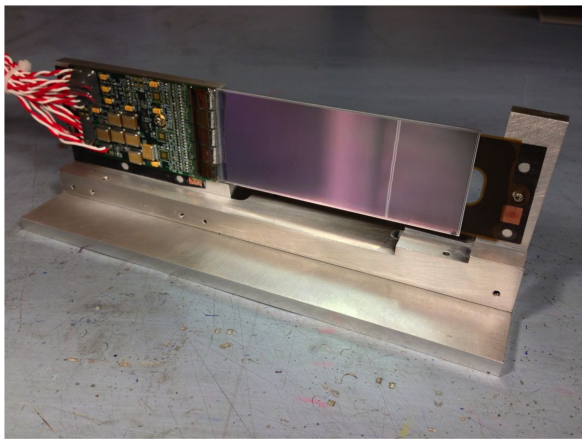

Figure 6: A half-module for layer 1-3 mounted on the module support.

Each half-module is built by gluing silicon sensors and an accompanied hybrid readout board to a polyimide-laminated carbon fiber frame. The first three layers of the SVT inherits the half-module from the HPS Test detector [1], shown in Fig. 6 while the last three layers are larger to increase tracking acceptance as shown in Fig. 7. The hybrid board caries five APV25 ASICs that are wire-bonded to 128 silicon strip lines each, except for the last channel on one of the outermost chips, for a total of 639 sensor lines. There are 36 hybrid boards in the SVT, and therefore 23,004 readout channels in total. The APV25 samples each of the attached channels at 41.667 MHz into a 192 entry analog memory pipeline. Upon reception of a system trigger signal, samples for each channel are read out from a preselected pipeline depth. The readout frame consists of a ± 4 mA rail-to-rail digital header followed by an analog differential current representing each channel. The APV25 is configured in "multi-peak" mode, so that three consecutive frames are output per trigger. Hit time reconstruction with 2 ns resolution requires six consecutive samples, thus two APV25 triggers are issued back-to-back in response to each DAQ system trigger. Figure 8 shows the measured pulse shape. A six sample trigger readout takes 20.1 $\mu$s. This limits the maximum trigger rate to 49.7 kHz. The APV25 can accept new triggers before

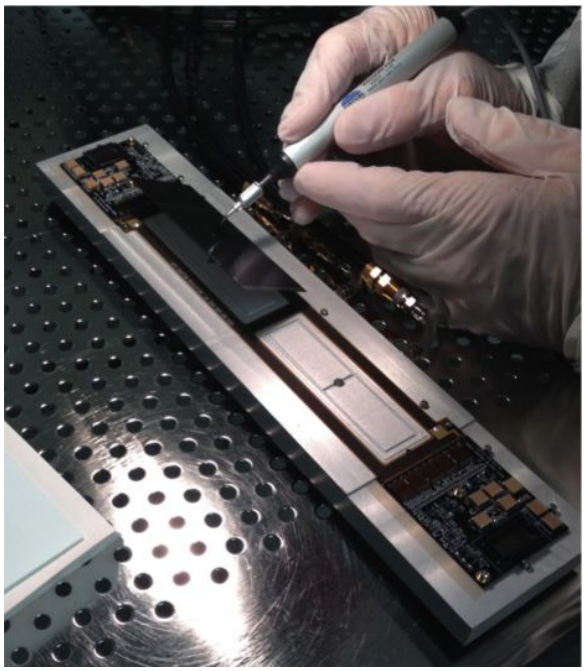

Figure 7: A layer 4-6 half-module under assembly.

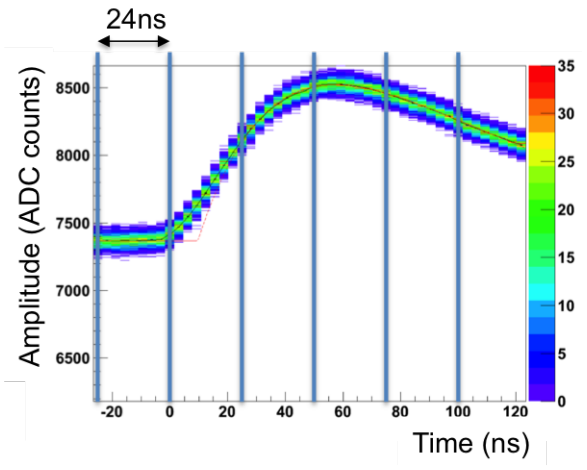


Figure 8: Pulse shape of the APV25 ASIC.

the previous trigger data are read out. Up to five triggers may be stacked in this manner.

The APV25 chips are configured via an $I^2C$ interface. An additional $I^2C$ temperature monitor is also present on each hybrid to monitor that the silicon sensors are being properly cooled. Each hybrid requires 2.5 V (AVDD) and 1.25 V references to power the APV25s, and an additional 2.5 V (DVDD) source to power digital components such as the $I^2C$ temperature monitor and differential clock and trigger fanouts. High voltage (¡1 kV) bias for the silicon detectors strips is routed directly to wire bond pads with local bypassing.

### *3.4. Front End Board*

The FEB serves two purposes: distribute power to the hybrids and digitize analog readout data from each hybrid APV25. Its design and placement inside the SVT vacuum chamber is motivated by a desire to reduce vacuum penetration count and analog signal length. The design centers around a Xilinx Artix-7 FPGA to interface to the ADCs, transmit digitized data up-stream, distribute clock, trigger, and $I^2C$ communication to the hybrids, and control and monitor hybrid power distribution. Deployment of FEBs inside the SVT chamber presents a number of challenges. Due to the presence of a 2 T magnetic field, great care was taken with the design of all onboard power regulators. Ferrite core inductors commonly used with DC-DC switching regulators will saturate in such high fields and lose effectiveness. It was also desired that no magnetically conduct-ing material be used on the board, so as not to distort the magnetic field inside the chamber. This necessitated the use air-core inductors in power regulation circuits and throughout the board. Radiation is

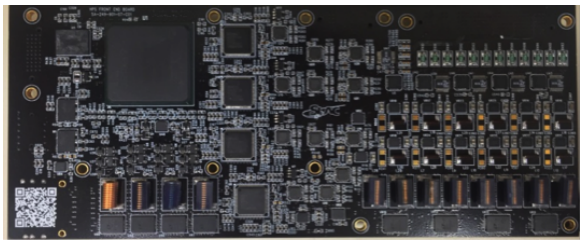

Figure 9: One COB ATCA blade used in the RCE platform.

also a concern inside of the SVT chamber. Beam interactions with the Tungsten target produce both neutrons and x-rays, which can have adverse effects on the FEBs. Neutrons can cause Single Event Upsets (SEUs) in the digital circuits of the FPGA, and x-ray doses can degrade integrated circuits over time. Simulations indicated that these sources should be within acceptable limits, but additional measures were taken just in case. A Borated-Polyethylene shield was installed around the FEBs to block neutrons, and the boards are installed on a serviceable custom cooling plate so that they can be replaced if needed. Each FEB connects to 4 hybrids, for a total of 20 APV25 analog channels. A preamplifier circuit converts the 4 mA signal from each APV25 into a voltage scaled to the range of the AD9252 14-bit ADC. The ADC sample clock runs at the same frequency as the APV25 clock, but has a programmable phase offset so that each sample can be taken at the center-point be-tween analog transitions. The FPGA monitors each APV25 ADC stream looking for readout frames. Every readout frame is then sent upstream by a multi-gigabit transceiver (MGT). The FEB has four upstream-only MGTs, with one dedicated to each hybrid. By dropping the two least significant noise bits from each ADC sample, each hybrids readout data can be packed on to a 3.125 Gbps link at rates approaching 50 kHz. Performing APV25 frame recovery on the FPGA in this manner allows the link speed to scale with the trigger rate, as well as robust error recovery on the upstream end. At the maximum trigger rate of 48.7 kHz, the combined data output rate from all of the FEBs is 89.6 Gbps. An additional full duplex MGT provides for configuration, trigger, and clock to be received from the upstream system. This link operates in a special fixed-latency mode so that every FEB in the system can recover the same 125 MHz beam-synchronous clock with minimal skew. The recovered clock is divided on each FEB to create the 41.667 MHz APV25 and ADC clocks. Triggers and clock alignment commands can be sent down these links with a guaranteed latency, assuring that all APV25s in the system receive the same clock and triggers in lock-

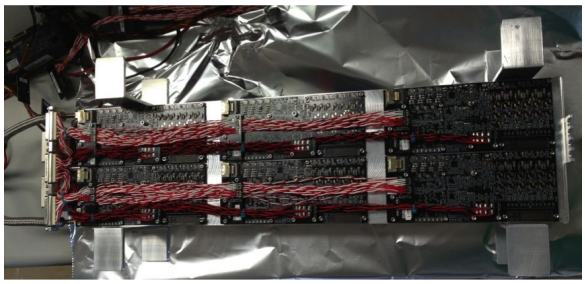

Figure 10: The partially cabled data acquisition front end boards screwed to the aluminum support plate before installation .


Figure 11: Flange board.

step with each other. The FEB is also responsible for distributing and monitoring hybrid power. Switched-mode regulators are used to efficiently step down a 6V reference to three intermediate voltages 2.9V, 2.9V and 1.4V. Linear regulators then convert these voltages into the 2.5V (DVDD), 2.5V (AVDD) and 1.25V needed by each hybrid. AD5144 SPI digital potentiometers placed in the resistor feedback of each regulator allow for all of the regulated voltages to be trimmed by the FPGA to account for cable drops. LTC2991 $I^2C$ ADCs are deployed to monitor the output voltage, feedback voltage and output current on each of the twelve hybrid voltage outputs. All of these monitors are accessible on the control link, and are sampled every second for delivery to EPICS slow controls.

### *3.5. Flange Board*

High speed differential signals from the FEB MGTs are sent through compact 8-pair mini-SAS cables to custom built vacuum flange board as seen in Fig. 11. Each of these boards is potted into the flange across its midpoint, with optical conversion of the differential signals occurring on the outside portion of the board. The optical signals are then transmitted over 30 m fibers to the SLAC RCE crate. Each of these flange boards can connect up to three FEBs, so four identical boards are potted into a single flange to handle all 10 FEBs. Separate custom flange boards carry low voltage power and high voltage bias through the vacuum penetration to the

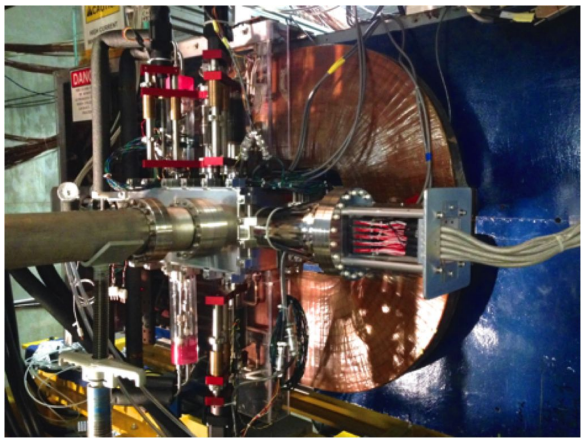

Figure 12: View from upstream, electron side, of the SVT after installation on the beamline. The vacuum box, that interfaces the beamline with the vacuum chamber, can be seen with its three linear shifts, two on the top and one on the bottom side. The flange holding the power and high-voltage sensor bias vacuum penetration boards extends to the right from the support box and the high-speed signal flange boards are attached to the opposite side.

FEBs. A picture of the installed boards is shown in Fig. 12.

### *3.6. RCE Platform*

#### *3.6.1. Overview*

The SVT DAQ uses the SLAC RCE Platform for high speed data transfer. This is a general purpose data processing cluster based on the Xilinx Zynq-7000 SOC and ATCA backplane. Each ATCA blade is called a Cluster on Board (COB) and contains eight Zynq-7040 nodes (RCEs) for data processing and one Zynq-7020 node for timing and trigger distribution (DTM). Each of these nodes has a dual-core ARM CPU with 1 GB of DDR3 memory tightly integrated with on-chip programmable logic (FPGA). A Rear Transition Module (RTM) specific to each experiment distributes high speed serial links to the RCEs and DTM. An Ethernet switch connects each node to the ATCA backplane and to front panel SFPs for upstream connectivity. Figure 13 shows a typical COB used in the RCE platform.

The RCE configuration for the HPS SVT DAQ is shown in Fig. 14.

#### *3.6.2. Layout and Data Flow*

Two COBs are deployed for a total of 16 RCE nodes. Optical signals from the vacuum flanges arrive at the RTMs and are converted to differential signals for the RCEs. Each RCE processes up to four high speed links, with each link containing APV25 readout data from one hybrid. One RCE is configured as the exclusive FEB

Figure 13: One COB ATCA blade used in the RCE platform.

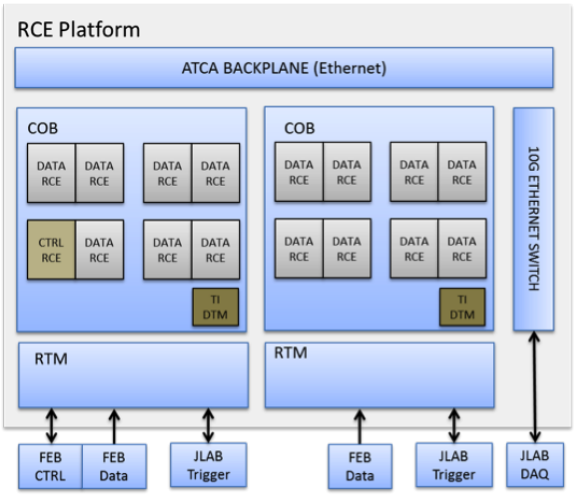


Figure 14: Block diagram of the RCE layout for the HPS experiment.

control node. It provides fixed-latency MGT control links at 2.5 Gbps to each of the 10 FEBs through the RTM. These links carry configuration, clock and trigger data.

The RTM also provides an interface to the JLab timing system for the DTM. FPGA logic in the DTM implements a full JLab Trigger Interface (TI), eliminating the need for a discrete TI card. Clock and trigger data are decoded by the TI logic and distributed to each of the DPMs via COB interconnects. Each RCE has an interface back to the DTM to indicate how many trigger events it has processed. The TI logic then communicates this back to the JLab Trigger System.

All other RCE are configured for data processing. Each of these nodes receives the digitized APV25 readouts from each trigger, applies thresholds for data reduction, and puts the data into RAM via DMA transfers. Software running on the Zynq ARM CPU then organizes the data into Ethernet frames and sends them to the higher level JLab DAQ system described in Sec. 4.3.

#### *3.6.3. Data Processing*

Detailed discussion of the data processing on the data DPM's.

#### *3.6.4. Timing Distribution*

Detailed discussion on the timing and trigger distribition on the COB. Note that Sec. **??** talks in detail about integration with JLab.

#### *3.6.5. Control and Monitoring*

Detailed description on how the system is controlled and monitored. Servers running on each DPM. Specifically how the control DPM monitor and control hybrids.

## 4. Integration with the JLab Data Acquisition

### *4.1. Overview*

Give general context of the JLab DAQ to the extent that the integration discussion below have some context.

### *4.2. Trigger and Timing Interface*

The RTM provides an interface to the JLab timing system for the DTM. FPGA logic in the DTM implements a full JLab Trigger Interface (TI), eliminating the need for a discrete TI card. Clock and trigger data are decoded by the TI logic and distributed to each of the DPMs via COB interconnects. Each RCE has an interface back to the DTM to indicate how many trigger events it has processed. The TI logic then communicates this back to the JLab Trigger System.

*4.3. Event Building*

Description of the data flow and how events are built and transferred from the firmware to the ROC and onwards to the CODA event builder.

*4.4. Operation*

Description of software including GUIs and EPICS interface that us used to operate the DAQ.

## 5. Performance

Define what belongs here, examples:

- data and trigger rates
- dead/bad channels, signal to noise
- hit time resolution,
- APV25 issues (occupancy dependent baseline, header noise)
- SEU candidate event

## 6. Summary

HPS completed a successful two week engineering run in the Spring of 2015. Nominal trigger rates of up to 20 kHz were demonstrated, with data rates of up to 150 MB/s. Trigger rates up to 47 kHz have been demonstrated offline. Additional enhancements are currently being implemented to reduce dead-time by fully utilizing of the APV25 output pipeline. Another data run is expected in the Spring of 2016.

## 7. Acknowledgements

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