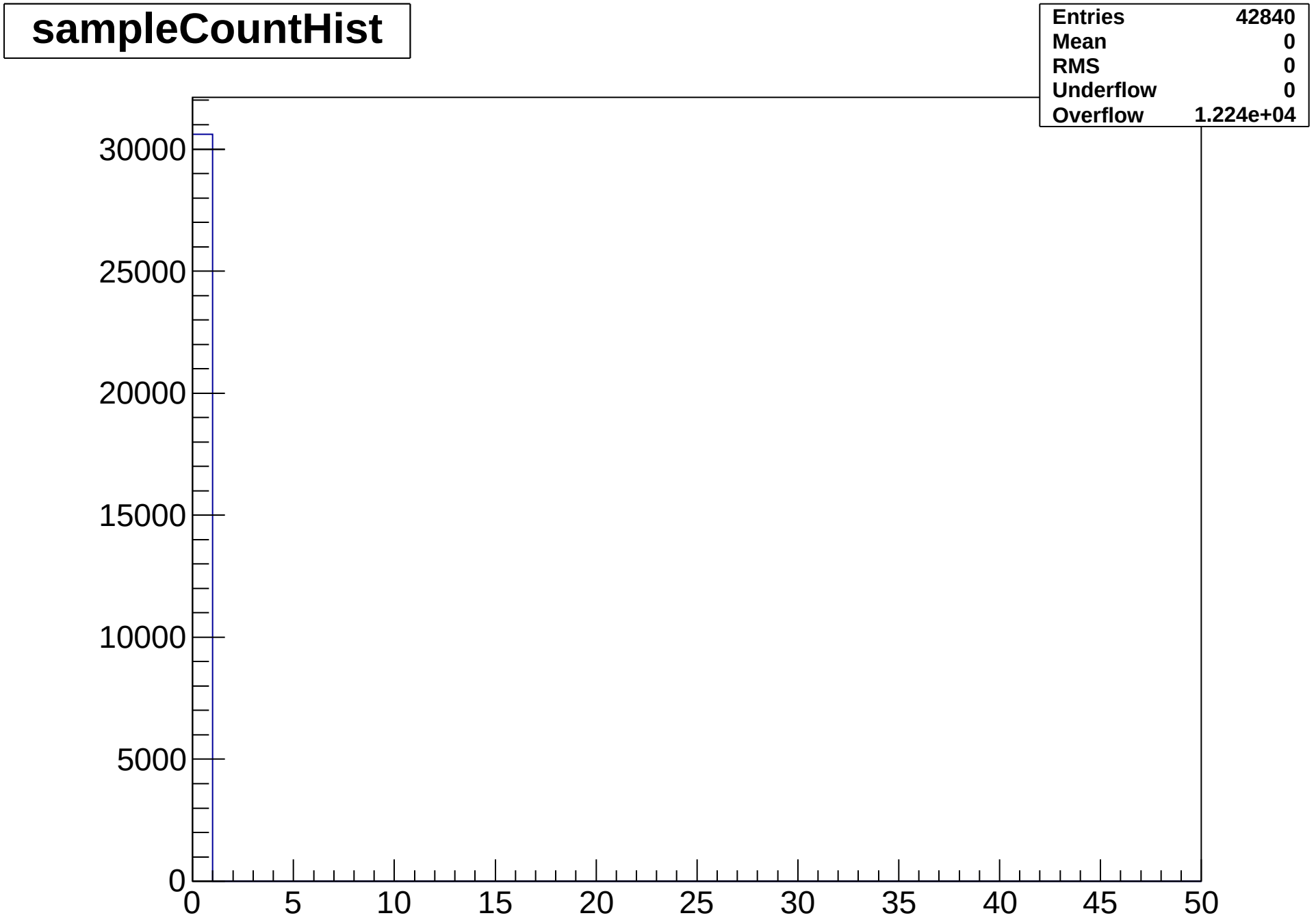
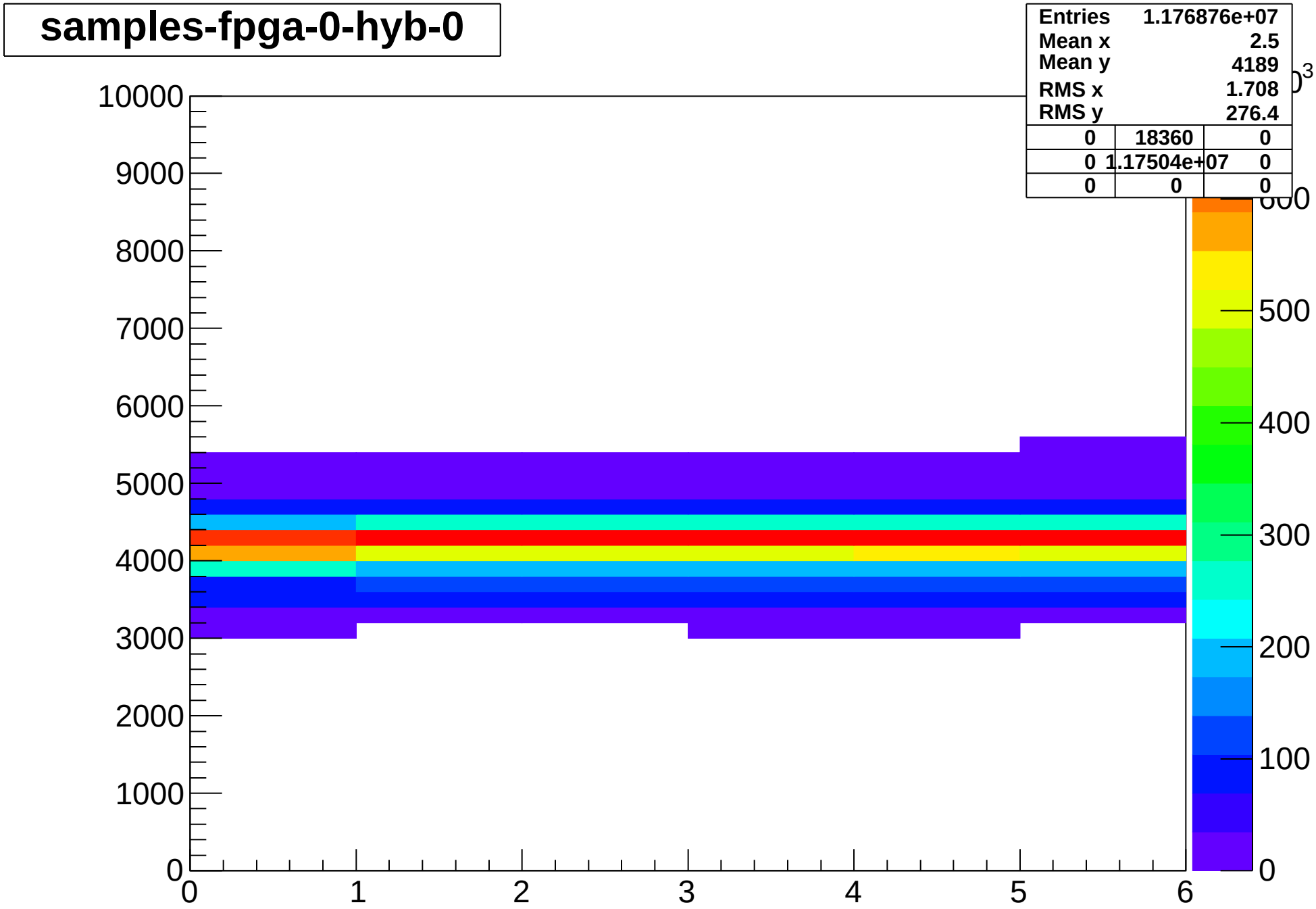
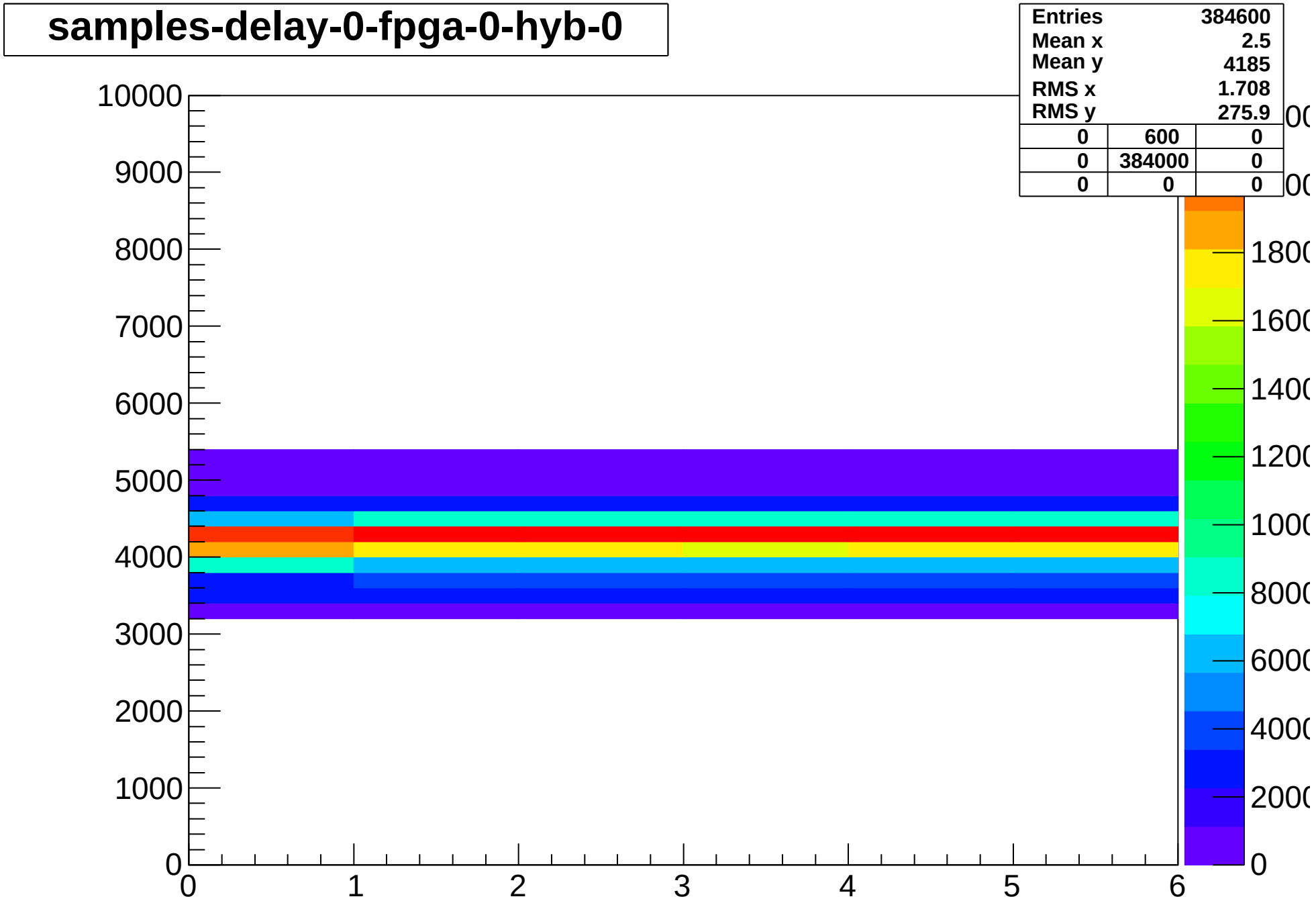
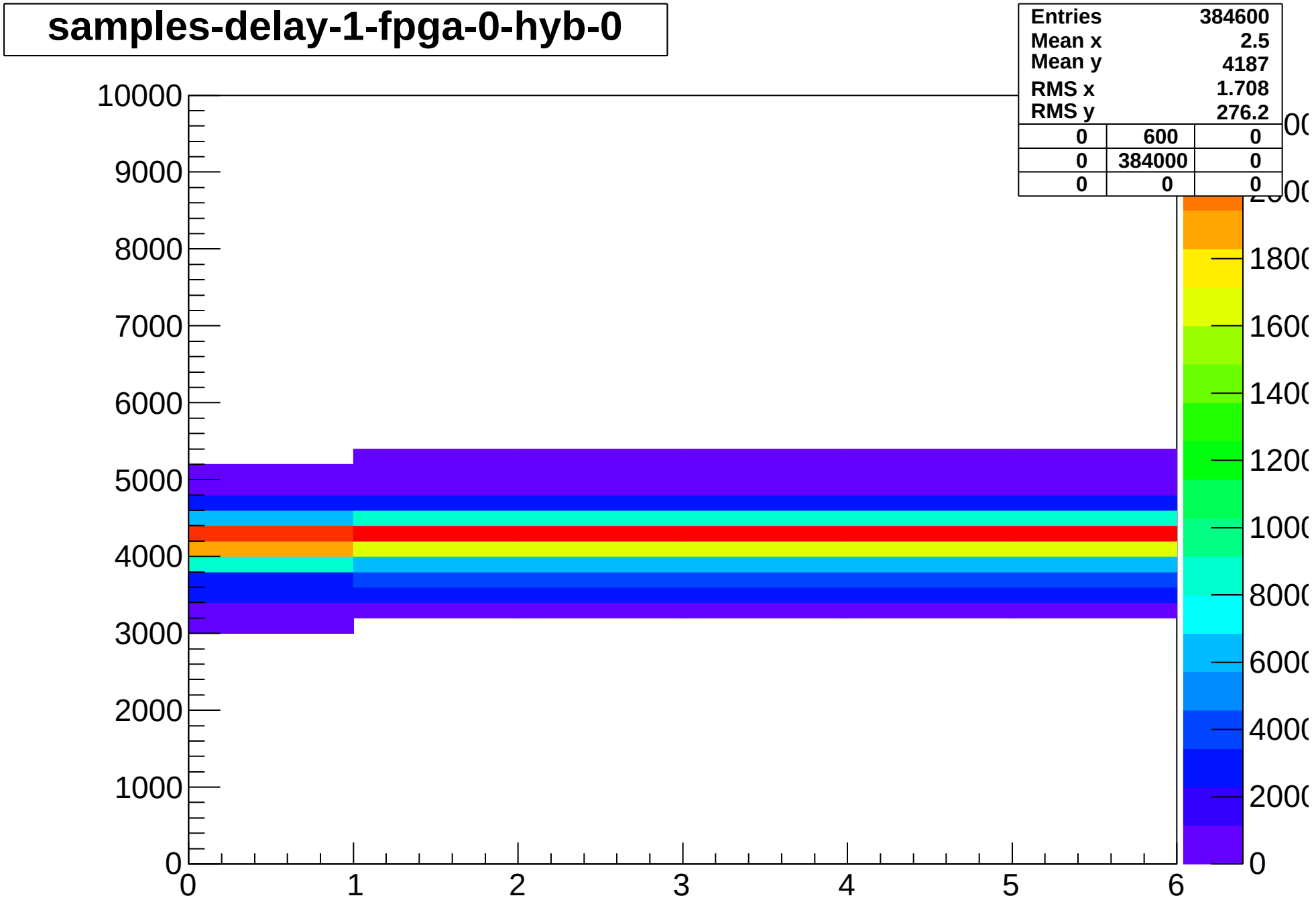
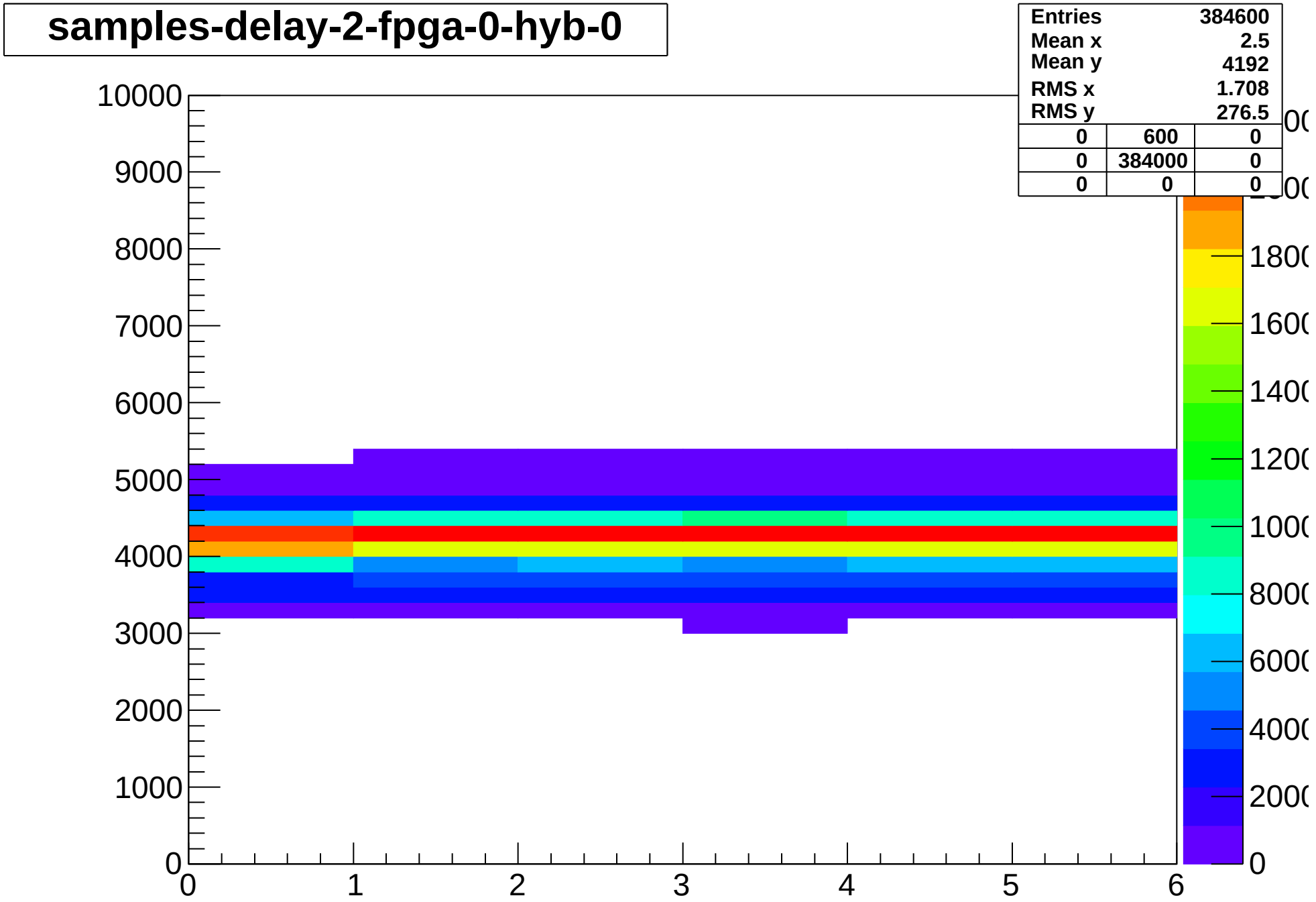
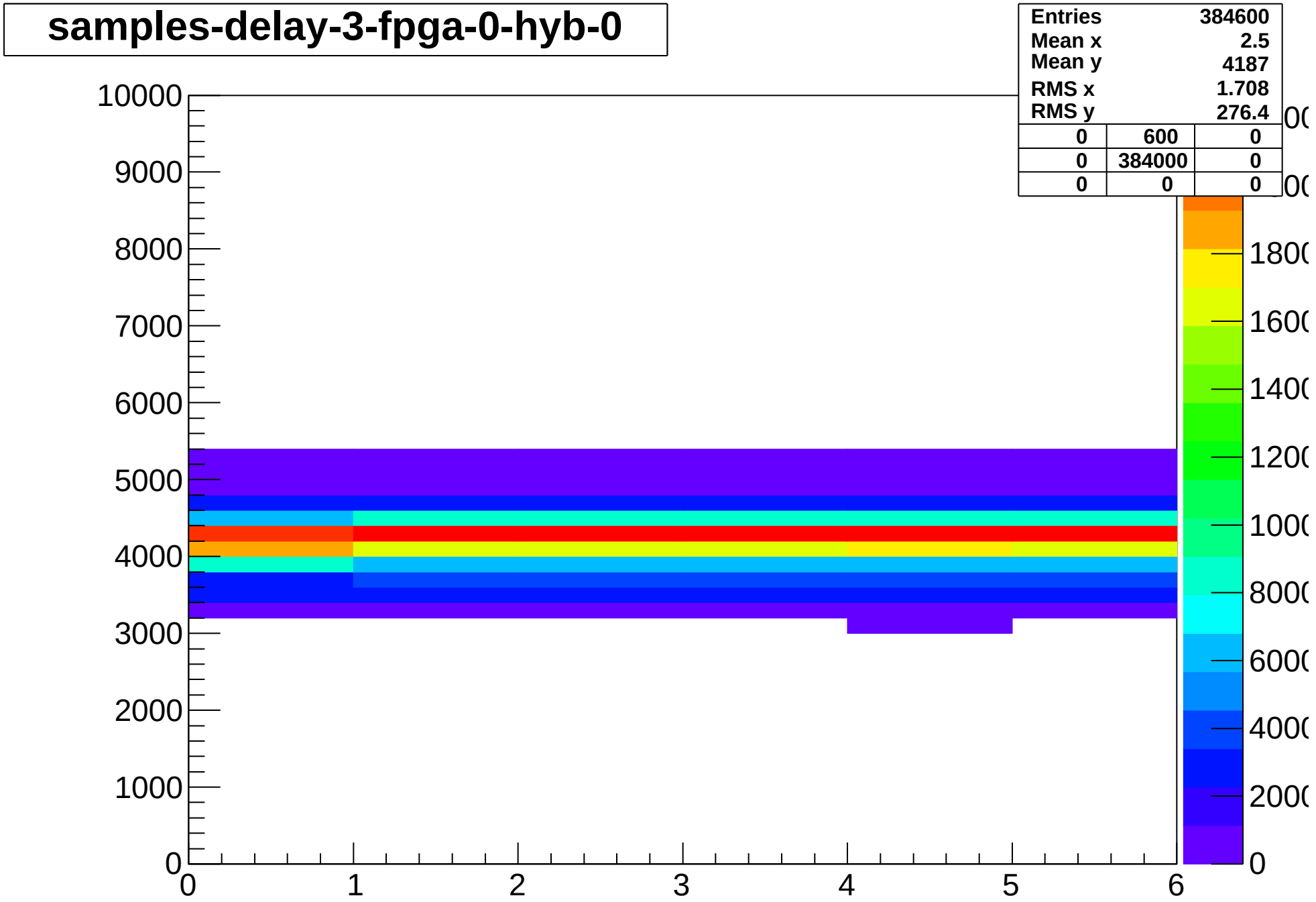

sampleCountHist
Entries 42840
Mean 0
RMS 0
Underflow 0
Overflow 1.224e+04
30000
25000
20000
15000
10000
5000
0
0
5
10
15
20
25
30
35
40
45
50

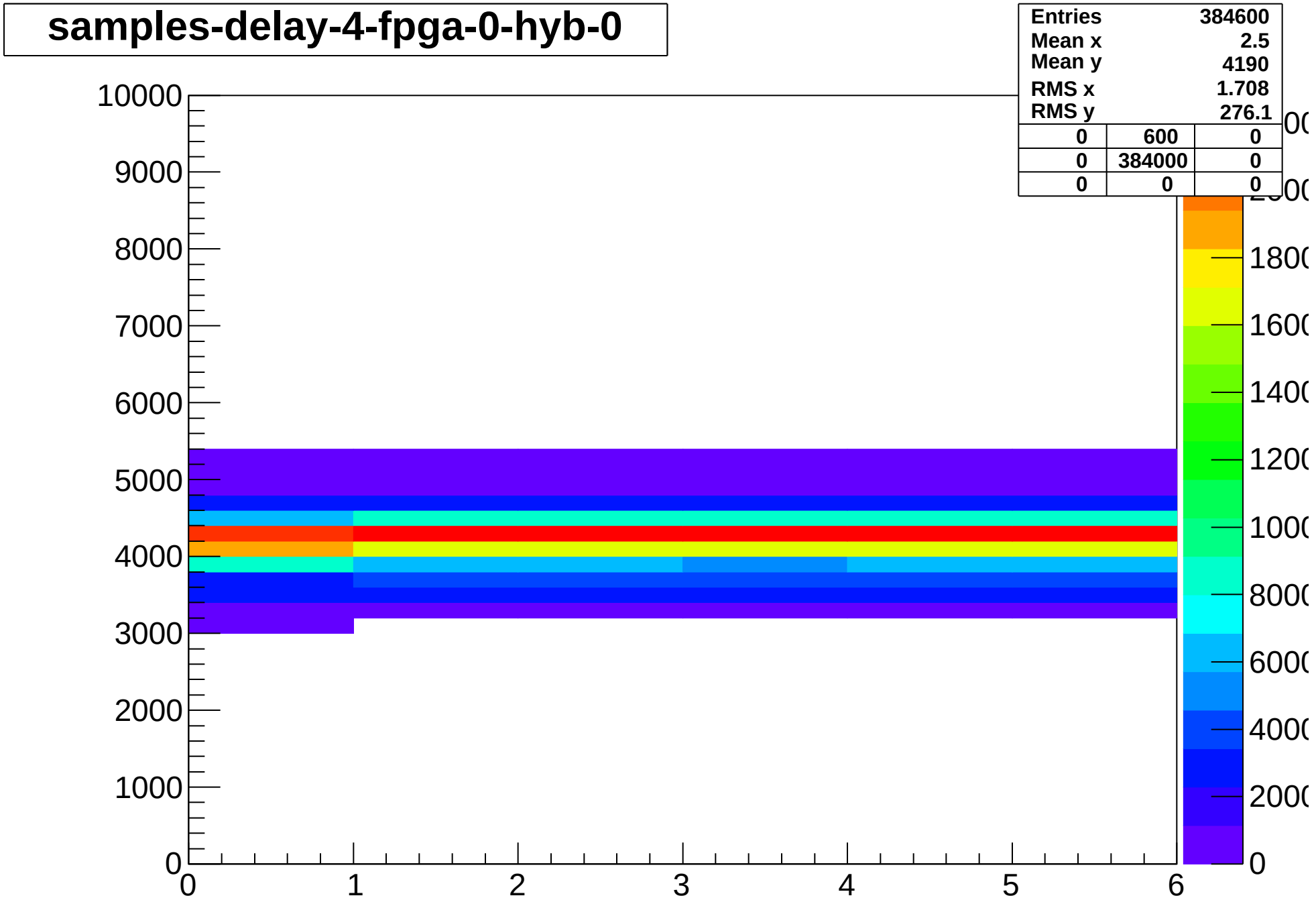

samples-fpga-0-hyb-0
Entries 1.176876e+07
Mean x 2.5
Mean y 4189
RMS x 1.708
RMS y 276.4
0 18360 0
0 1.17504e+07 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
500
400
300
200
100
0

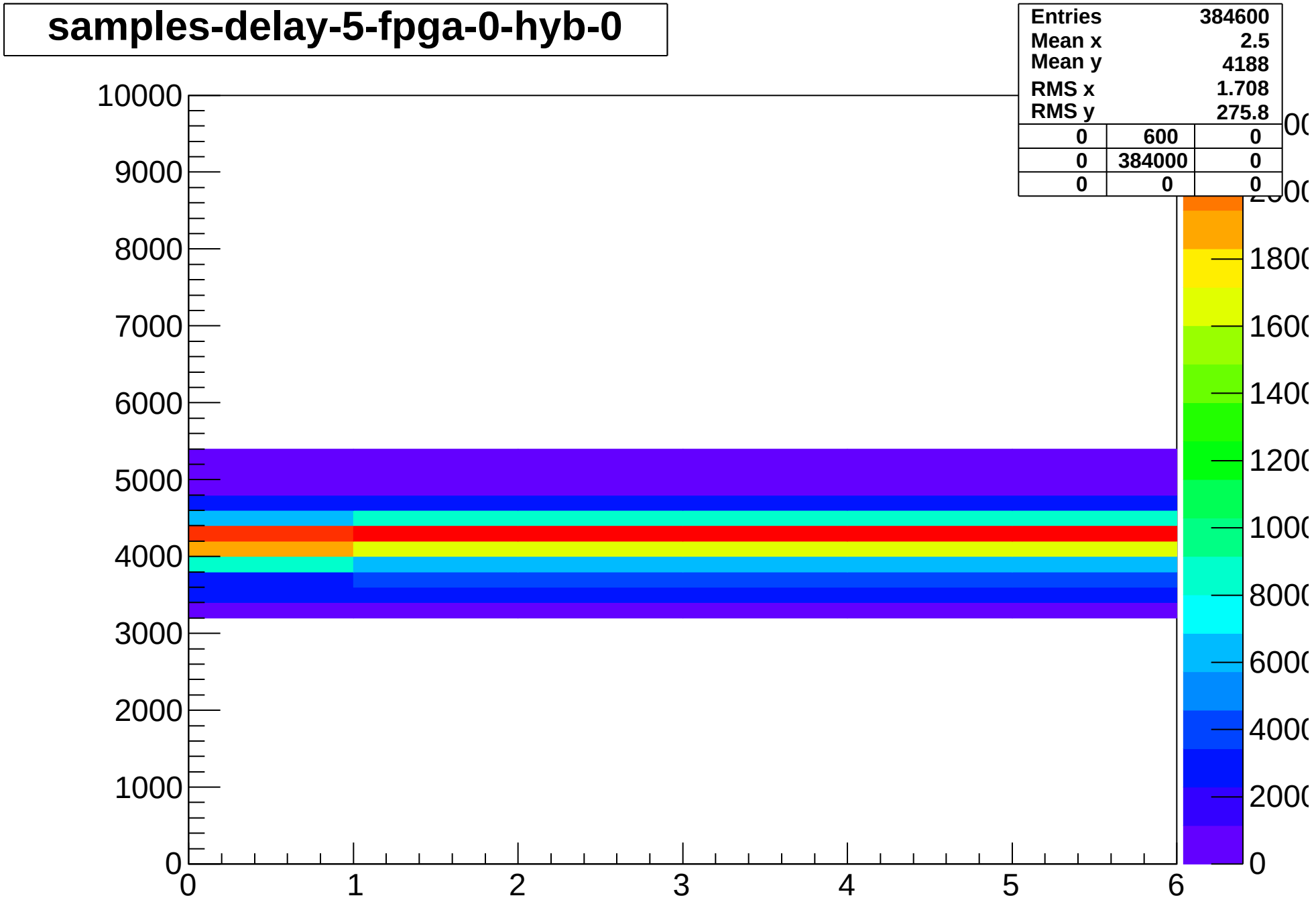

samples-delay-0-fpga-0-hyb-0
Entries 384600
Mean x 2.5
Mean y 4185
RMS x 1.708
RMS y 275.9
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

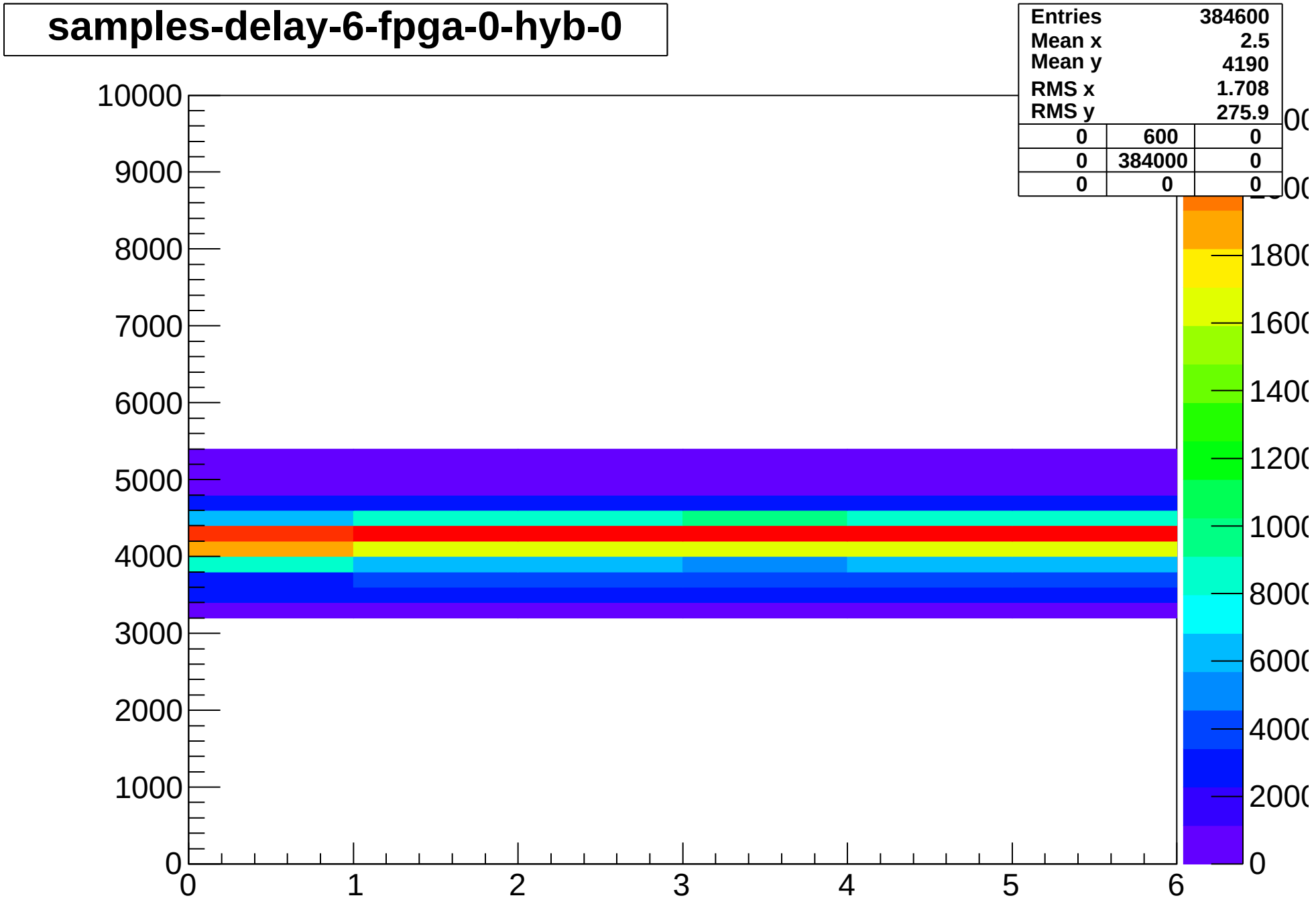

samples-delay-1-fpga-0-hyb-0
Entries 384600
Mean x 2.5
Mean y 4187
RMS x 1.708
RMS y 276.2
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

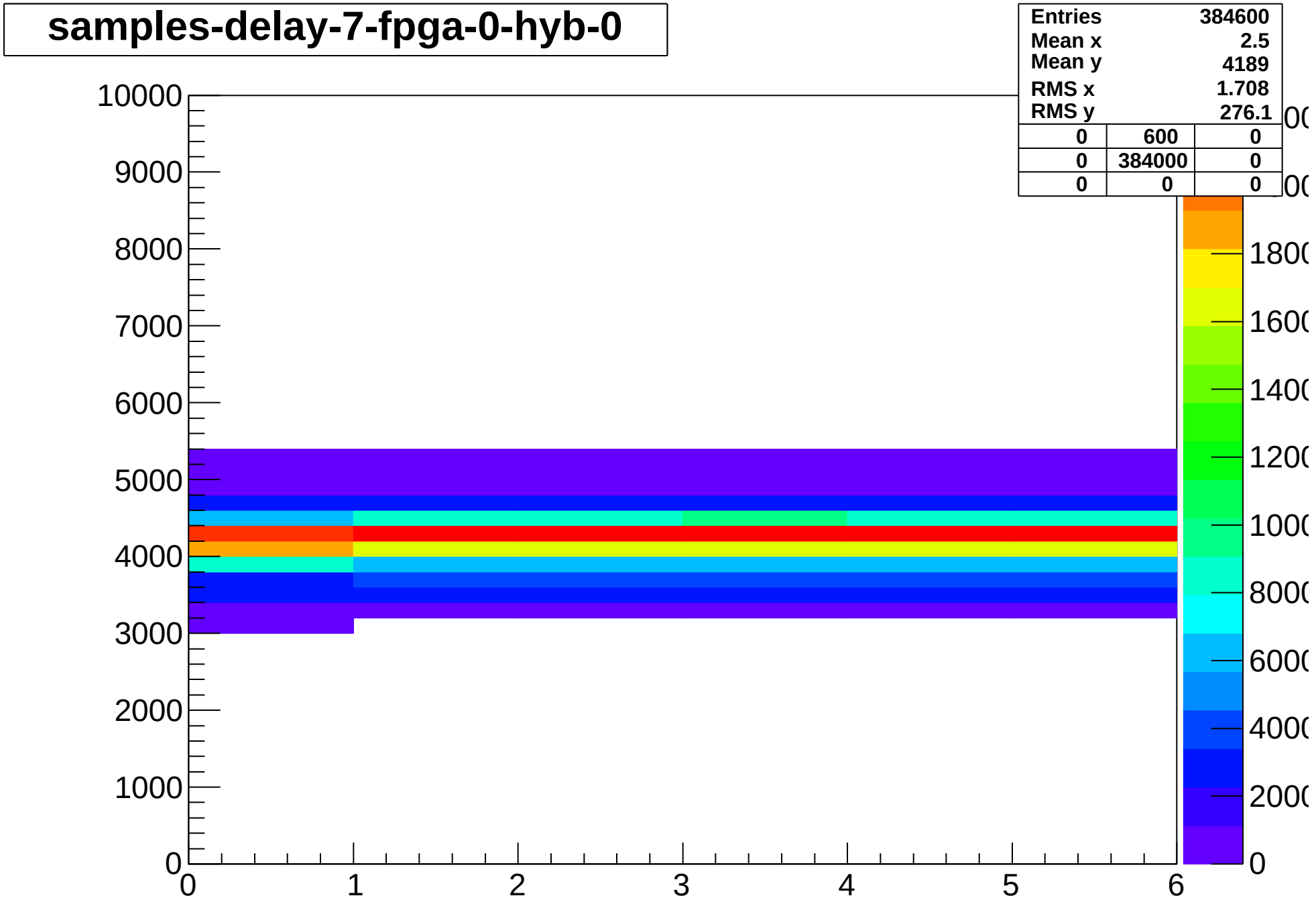

samples-delay-2-fpga-0-hyb-0
Entries 384600
Mean x 2.5
Mean y 4192
RMS x 1.708
RMS y 276.5
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

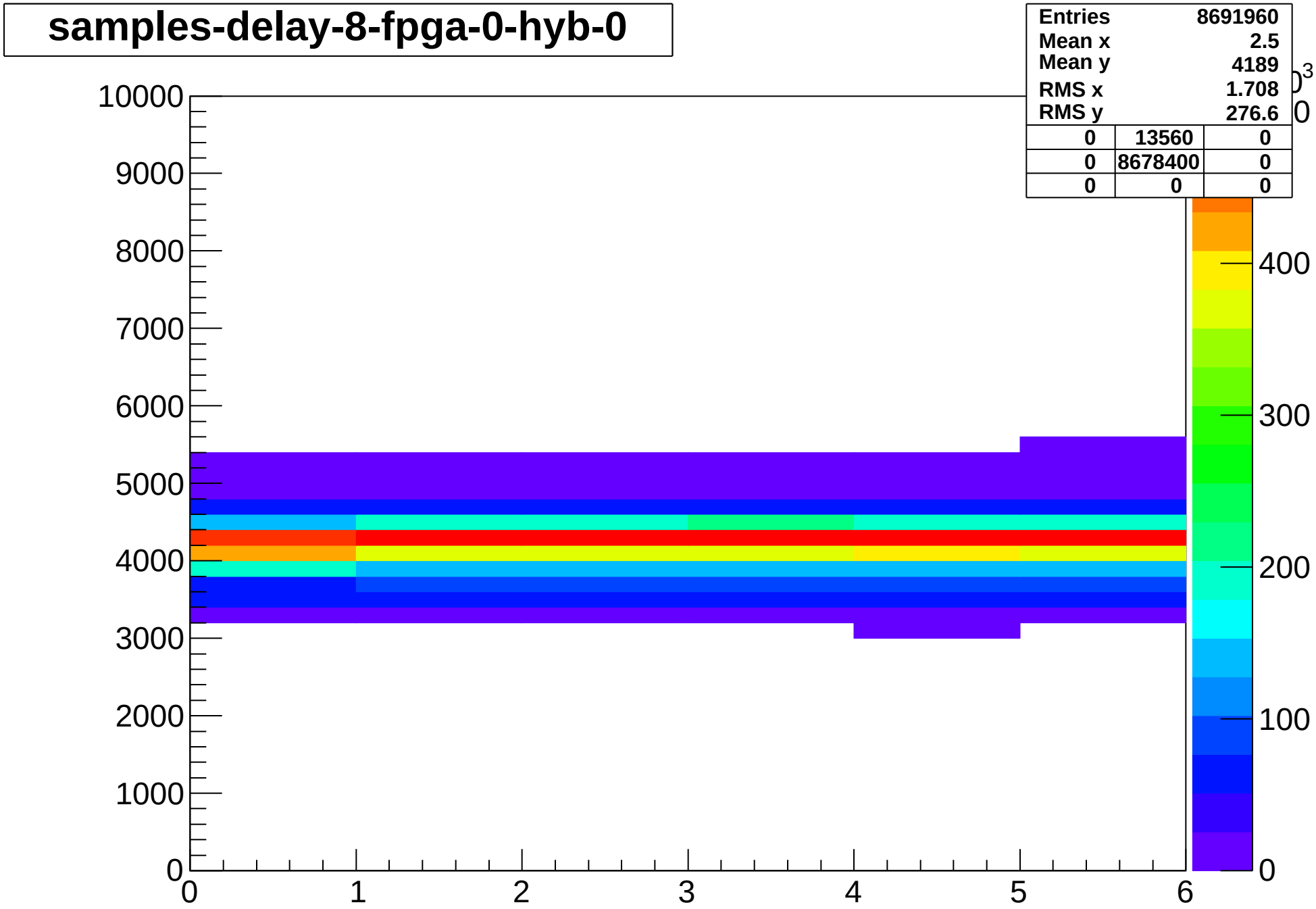

samples-delay-3-fpga-0-hyb-0
Entries 384600
Mean x 2.5
Mean y 4187
RMS x 1.708
RMS y 276.4
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

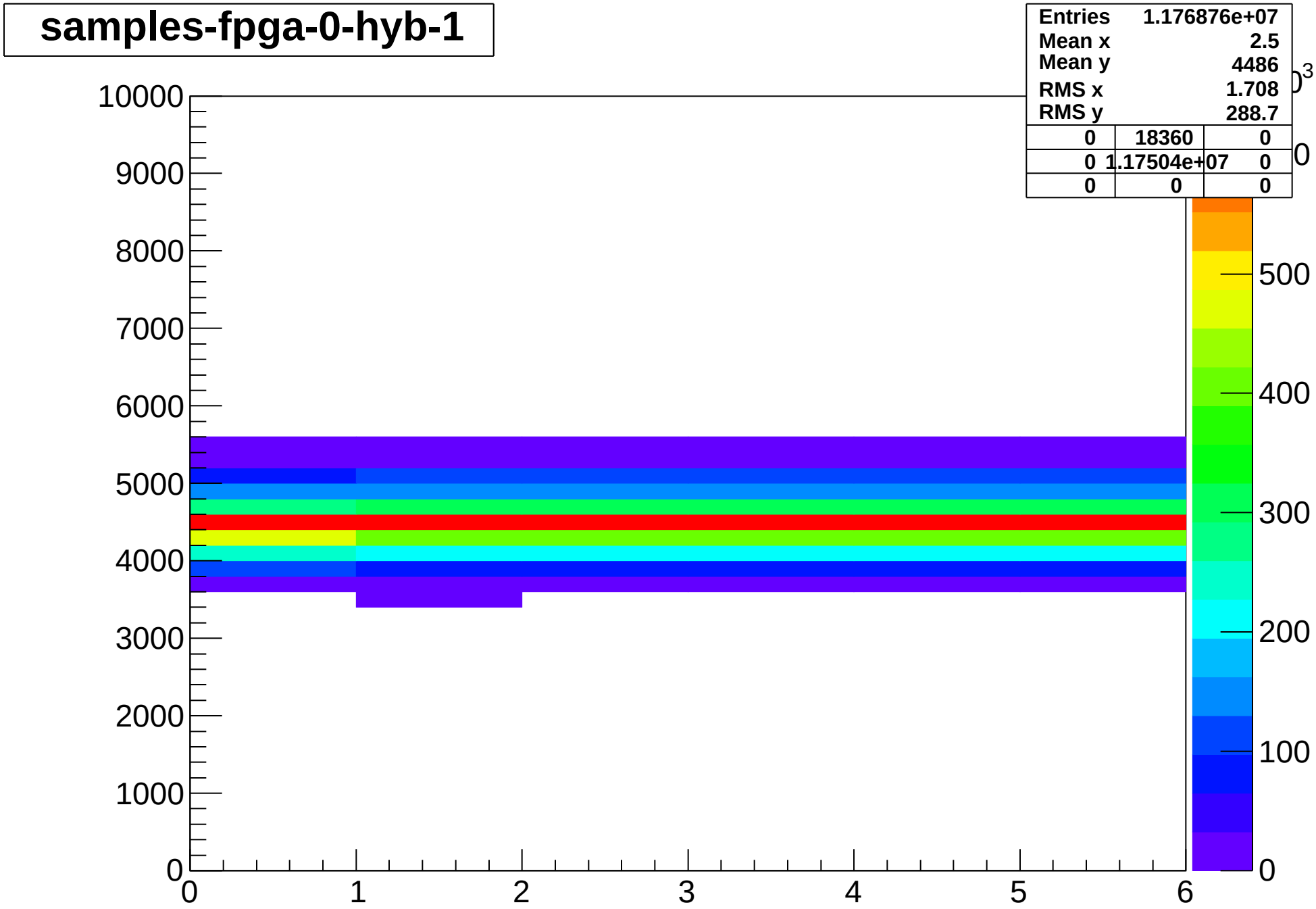

samples-delay-4-fpga-0-hyb-0
Entries 384600
Mean x 2.5
Mean y 4190
RMS x 1.708
RMS y 276.1
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

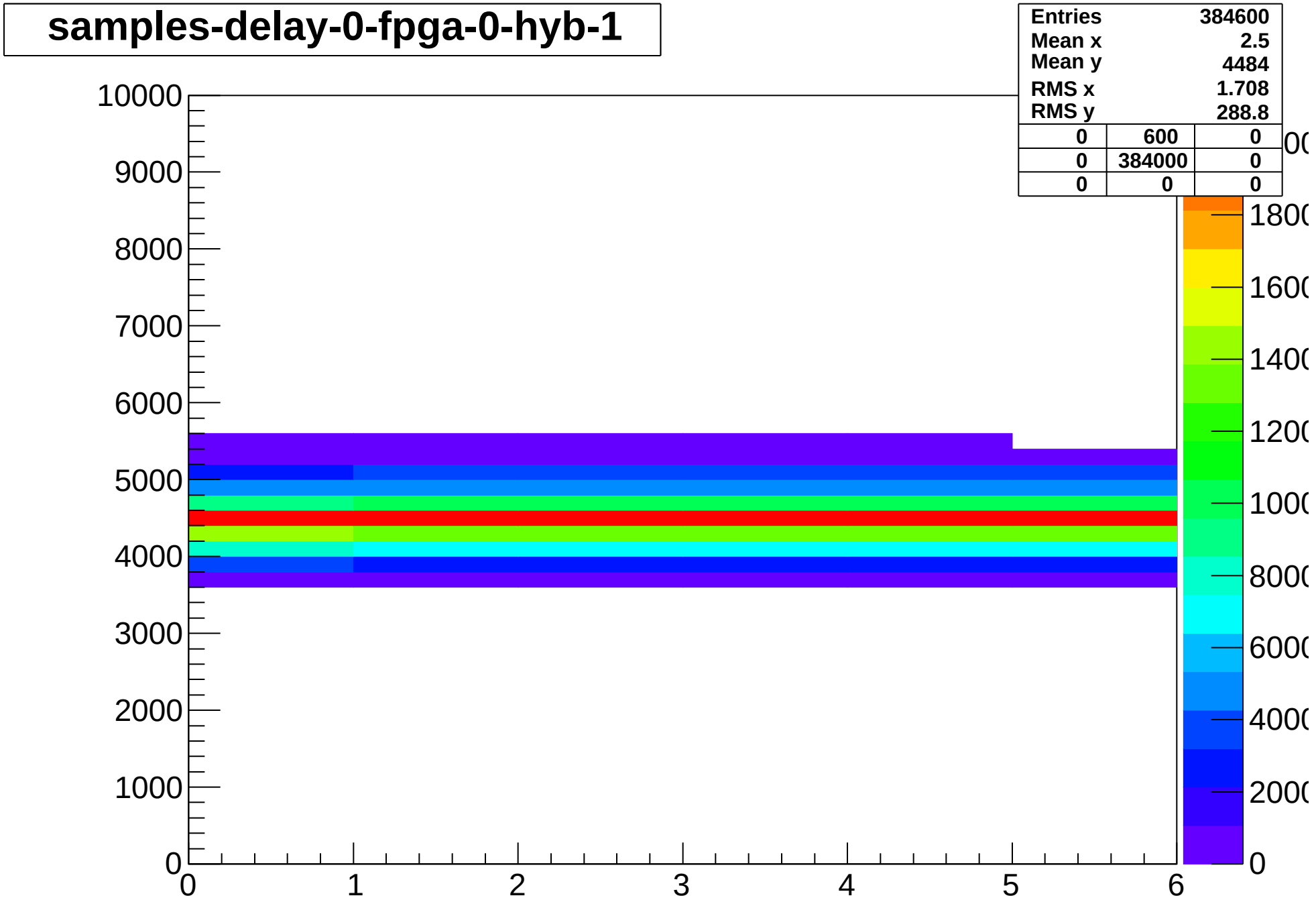

samples-delay-5-fpga-0-hyb-0
Entries 384600
Mean x 2.5
Mean y 4188
RMS x 1.708
RMS y 275.8
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

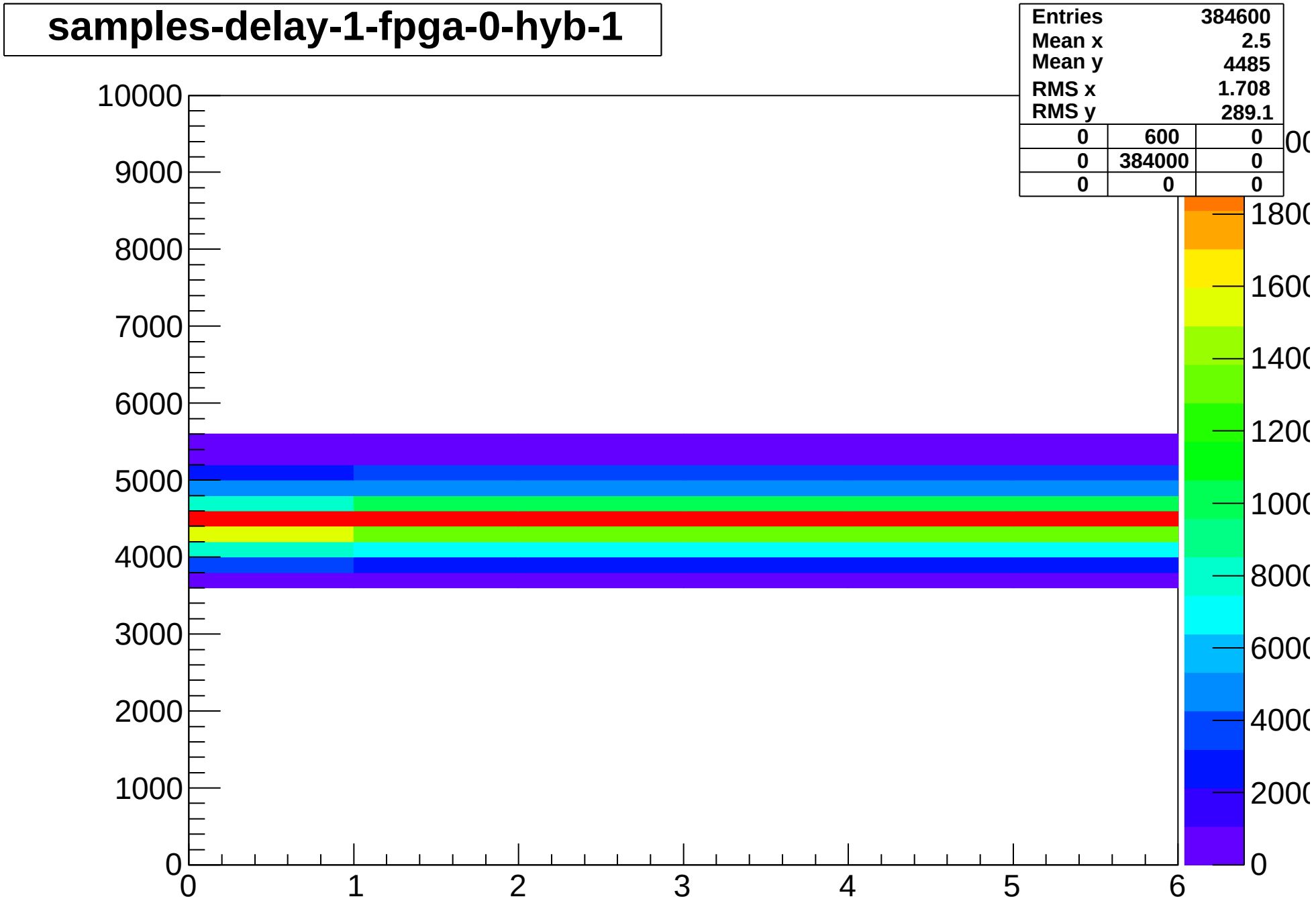

samples-delay-6-fpga-0-hyb-0
Entries 384600
Mean x 2.5
Mean y 4190
RMS x 1.708
RMS y 275.9
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

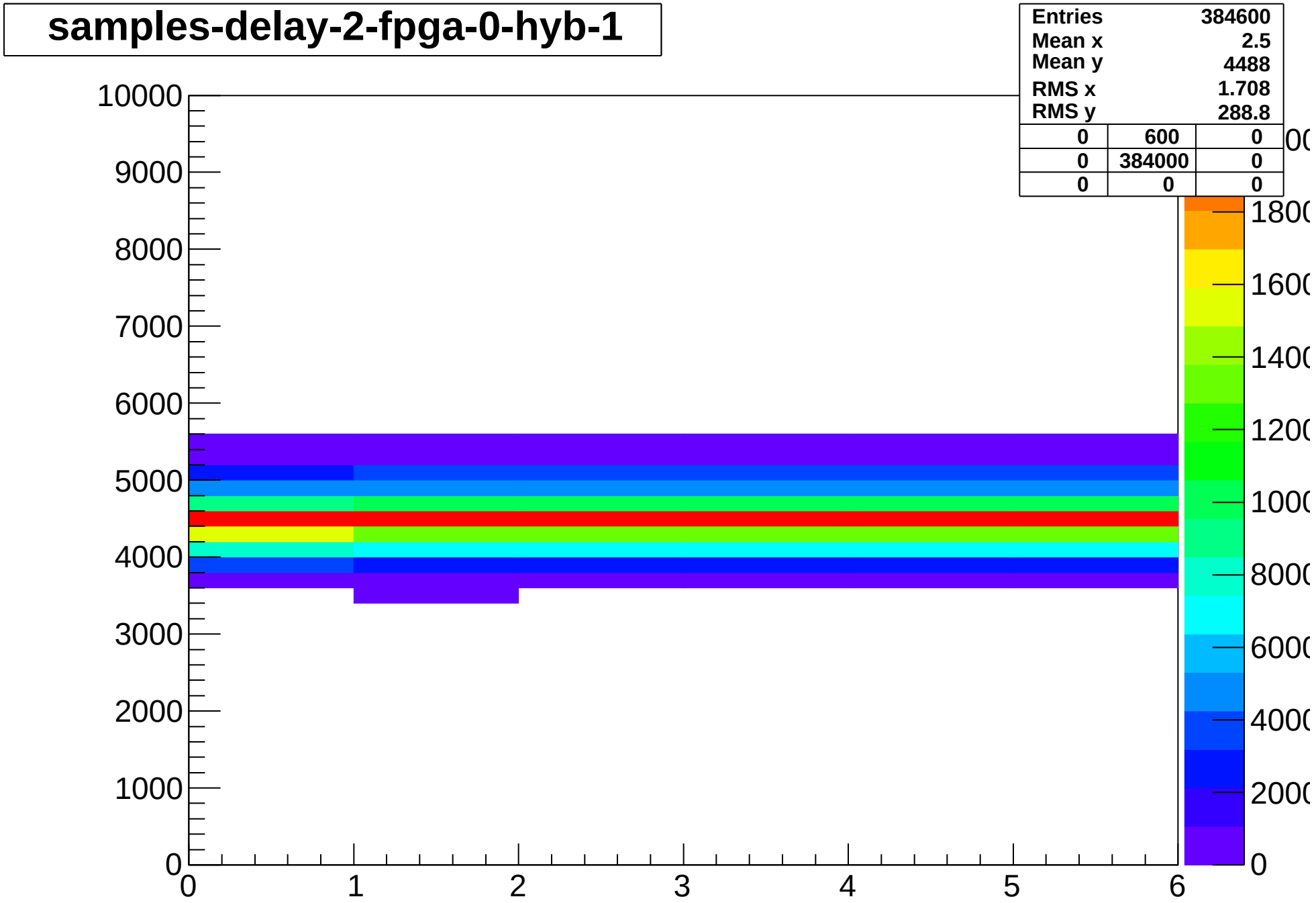

samples-delay-7-fpga-0-hyb-0
Entries 384600
Mean x 2.5
Mean y 4189
RMS x 1.708
RMS y 276.1
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

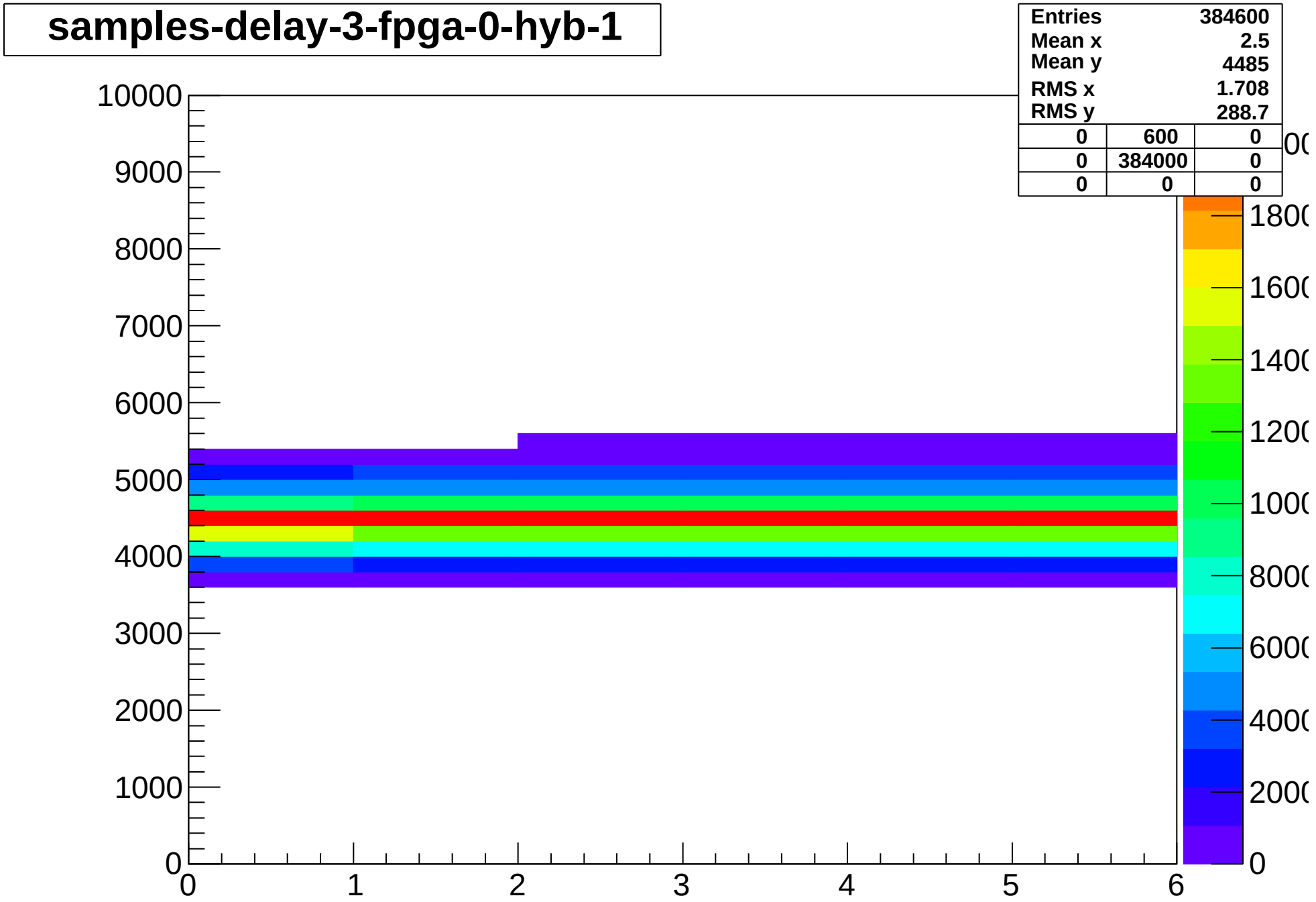

samples-delay-8-fpga-0-hyb-0
Entries 8691960
Mean x 2.5
Mean y 4189
RMS x 1.708
RMS y 276.6
0 13560 0
0 8678400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
400
300
200
100
0


samples-fpga-0-hyb-1
Entries 1.176876e+07
Mean x 2.5
Mean y 4486
RMS x 1.708
RMS y 288.7
0 18360 0
0 1.17504e+07 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
500
400
300
200
100
0


samples-delay-0-fpga-0-hyb-1
Entries 384600
Mean x 2.5
Mean y 4484
RMS x 1.708
RMS y 288.8
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0


samples-delay-1-fpga-0-hyb-1
Entries 384600
Mean x 2.5
Mean y 4485
RMS x 1.708
RMS y 289.1
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0


samples-delay-2-fpga-0-hyb-1
Entries 384600
Mean x 2.5
Mean y 4488
RMS x 1.708
RMS y 288.8
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0


samples-delay-3-fpga-0-hyb-1
Entries 384600
Mean x 2.5
Mean y 4485
RMS x 1.708
RMS y 288.7
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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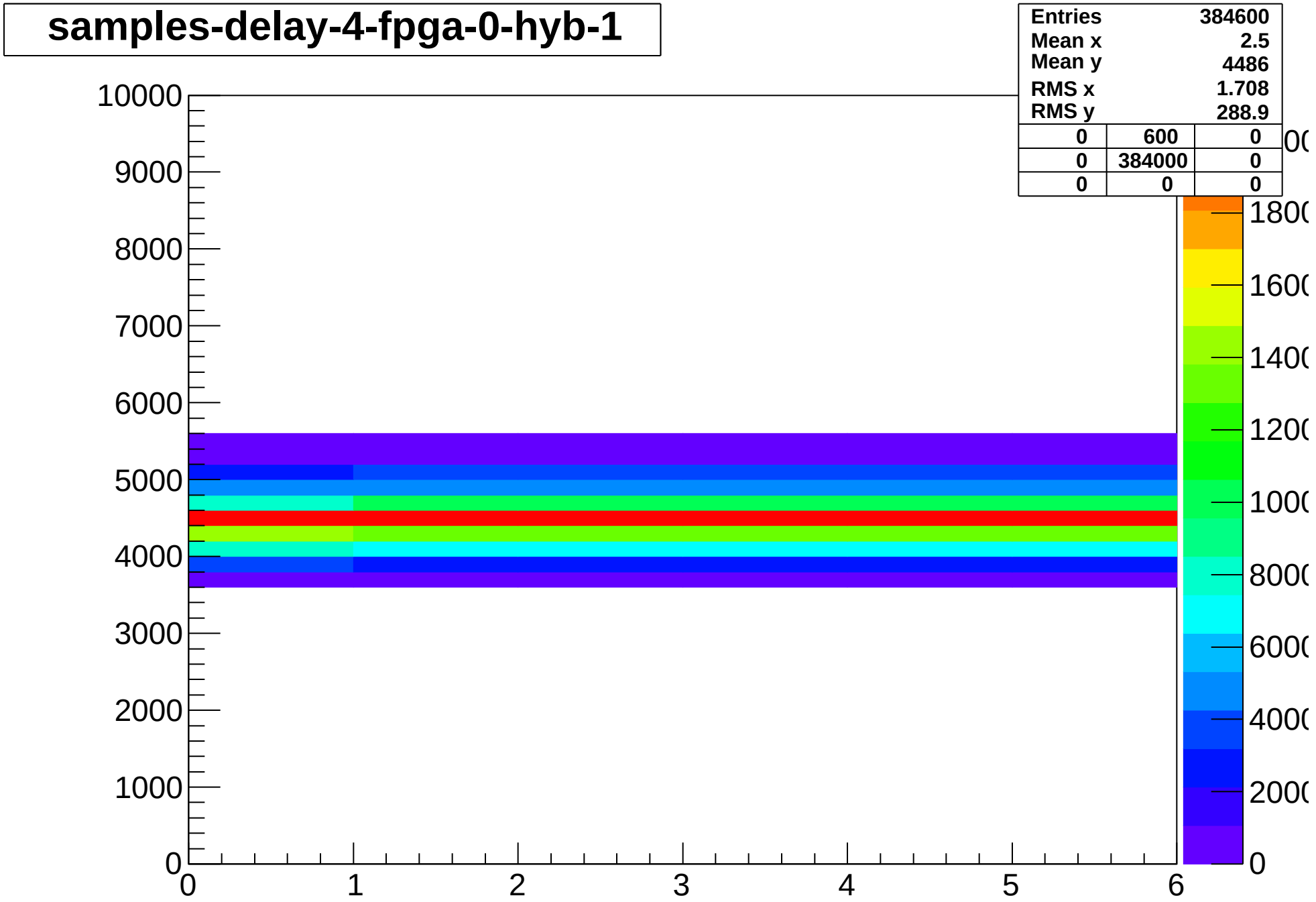
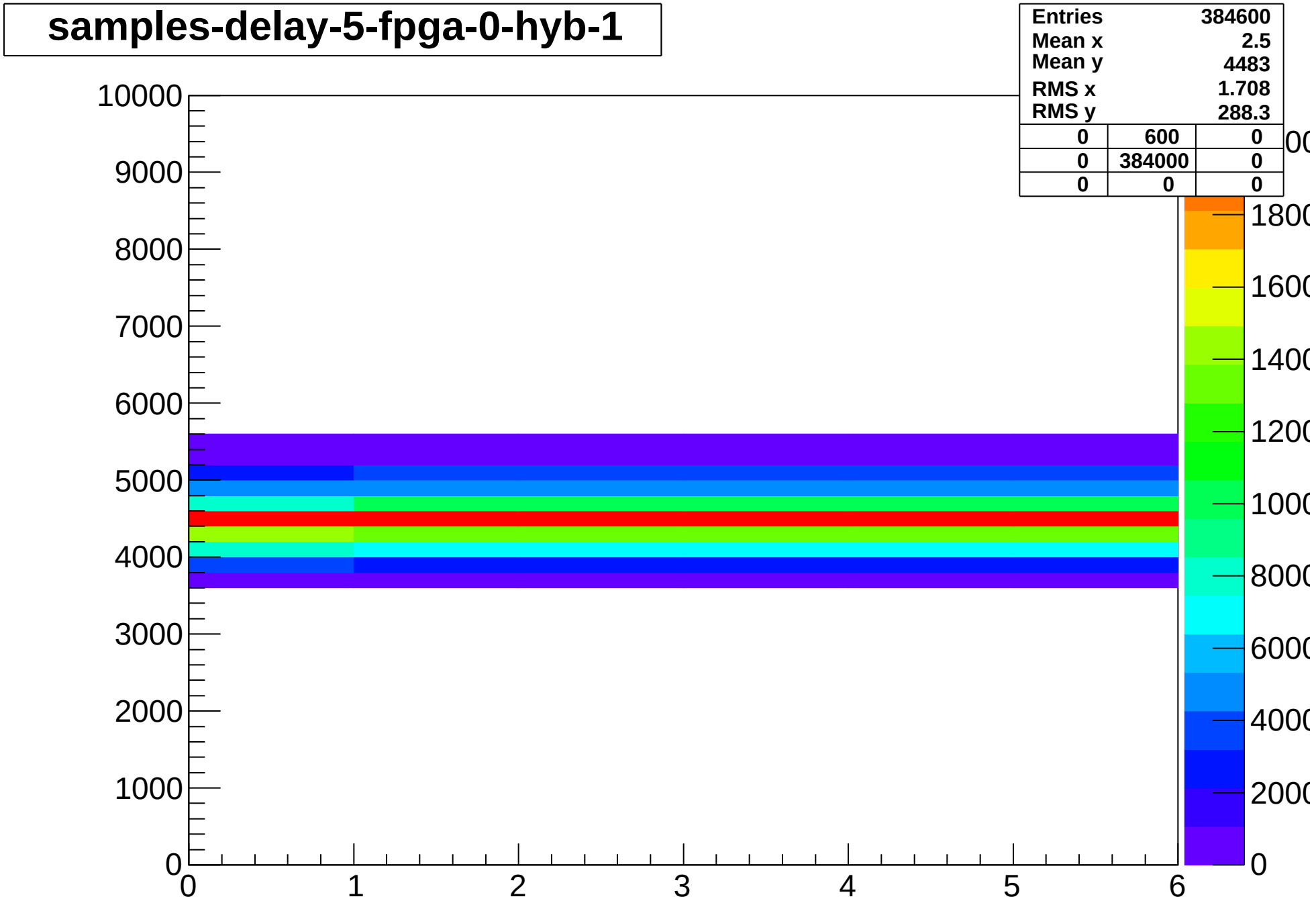
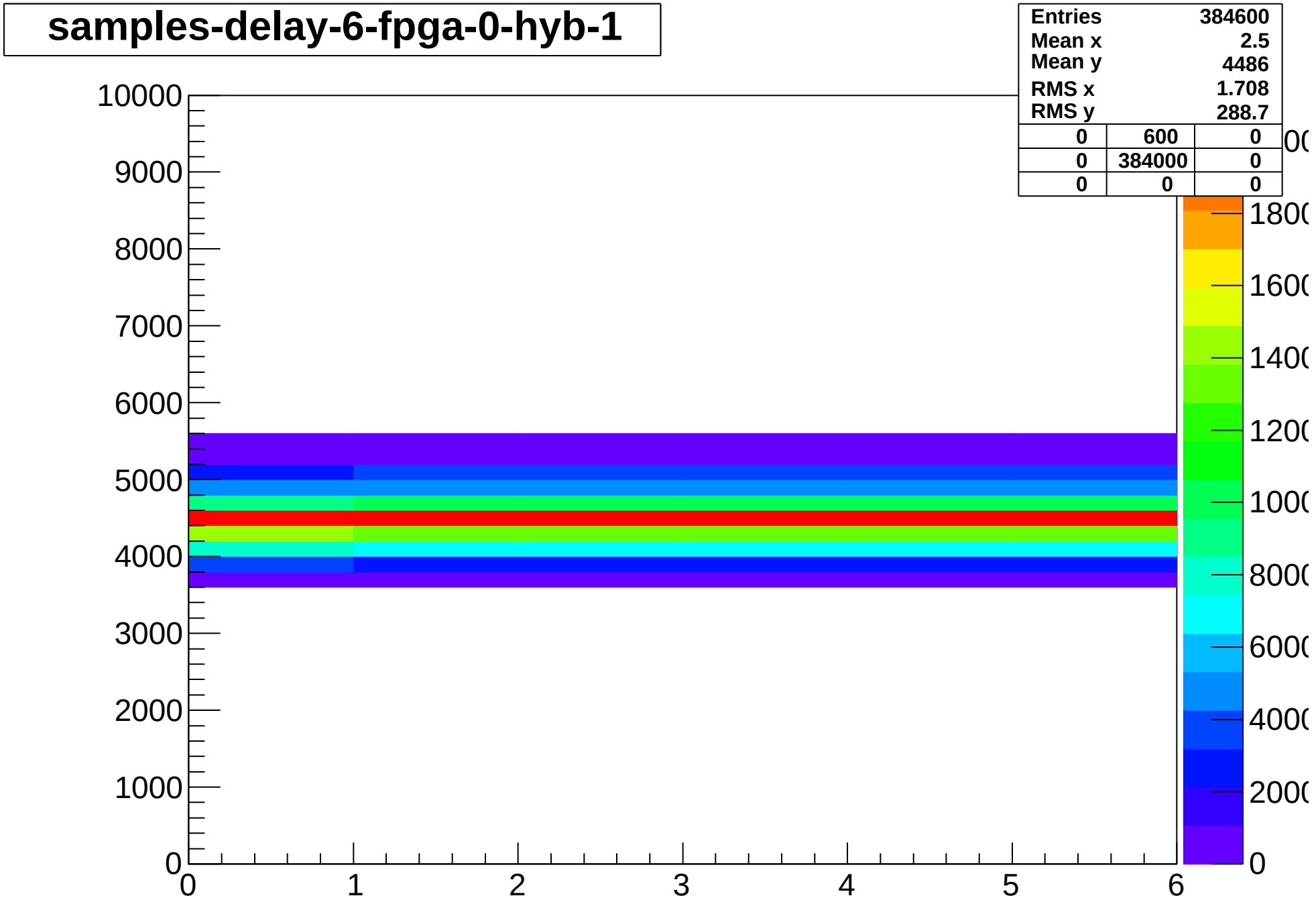
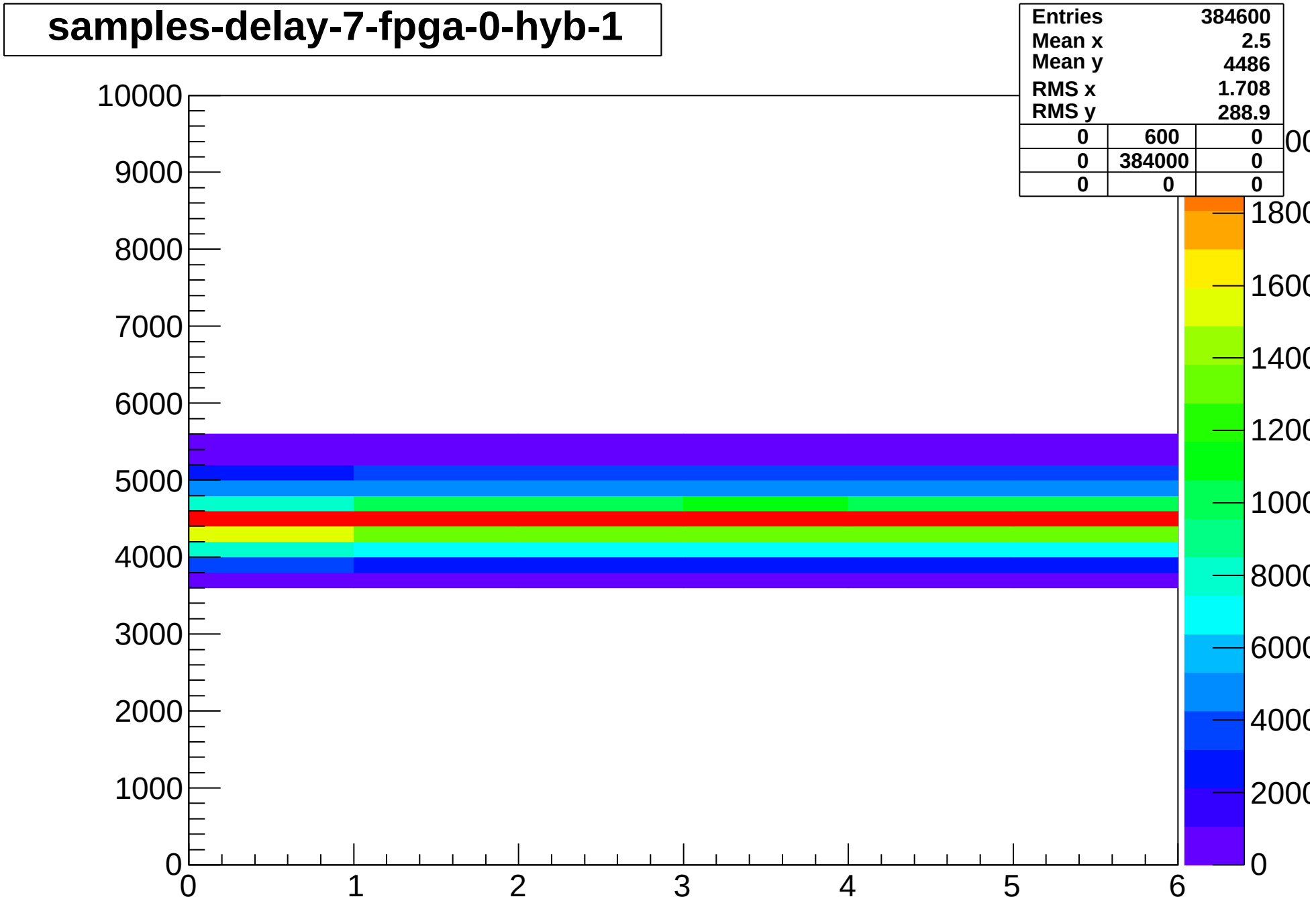
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0


samples-delay-4-fpga-0-hyb-1
Entries 384600
Mean x 2.5
Mean y 4486
RMS x 1.708
RMS y 288.9
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0


samples-delay-5-fpga-0-hyb-1
Entries 384600
Mean x 2.5
Mean y 4483
RMS x 1.708
RMS y 288.3
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0


samples-delay-6-fpga-0-hyb-1
Entries 384600
Mean x 2.5
Mean y 4486
RMS x 1.708
RMS y 288.7
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0


samples-delay-7-fpga-0-hyb-1
Entries 384600
Mean x 2.5
Mean y 4486
RMS x 1.708
RMS y 288.9
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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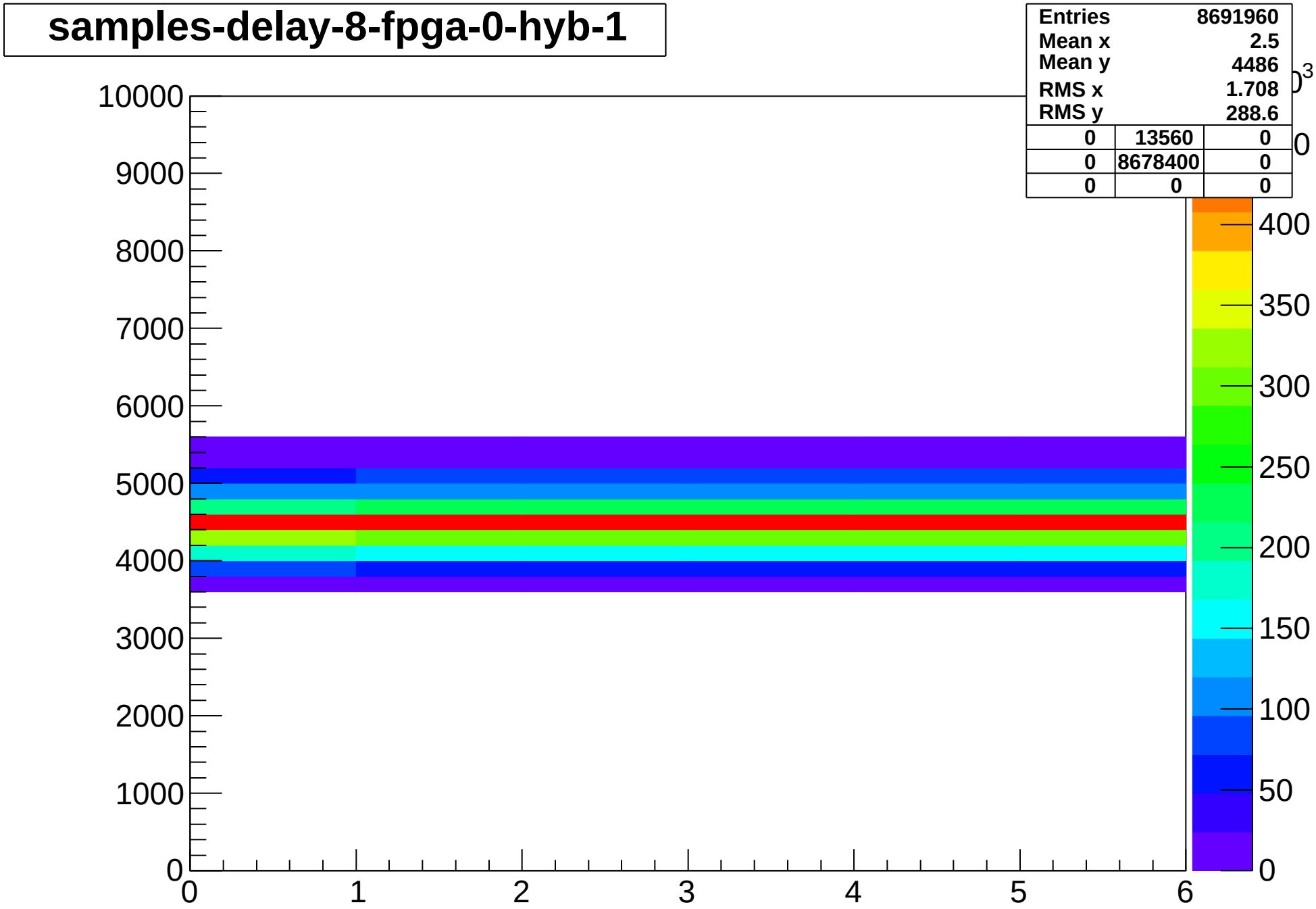
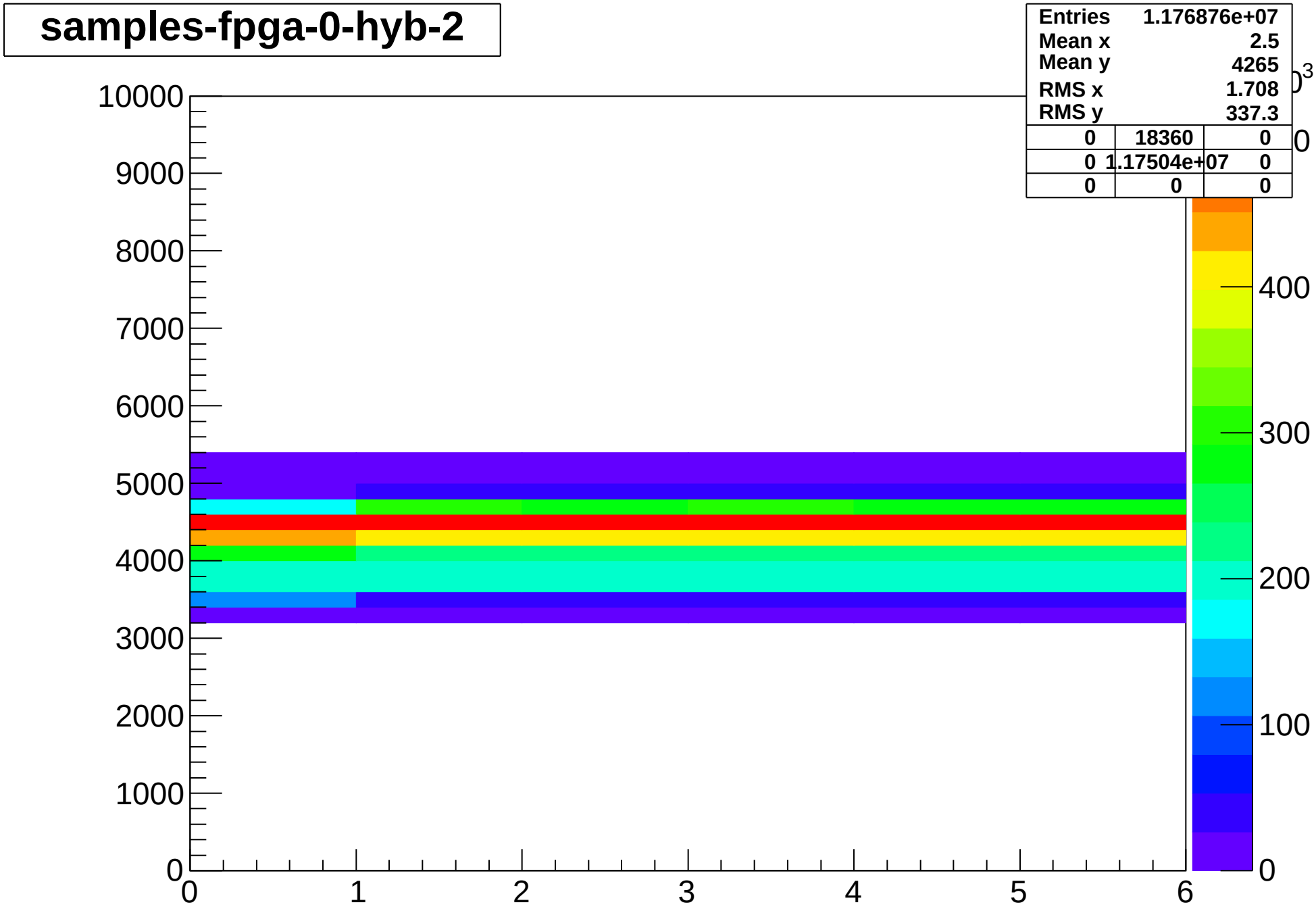
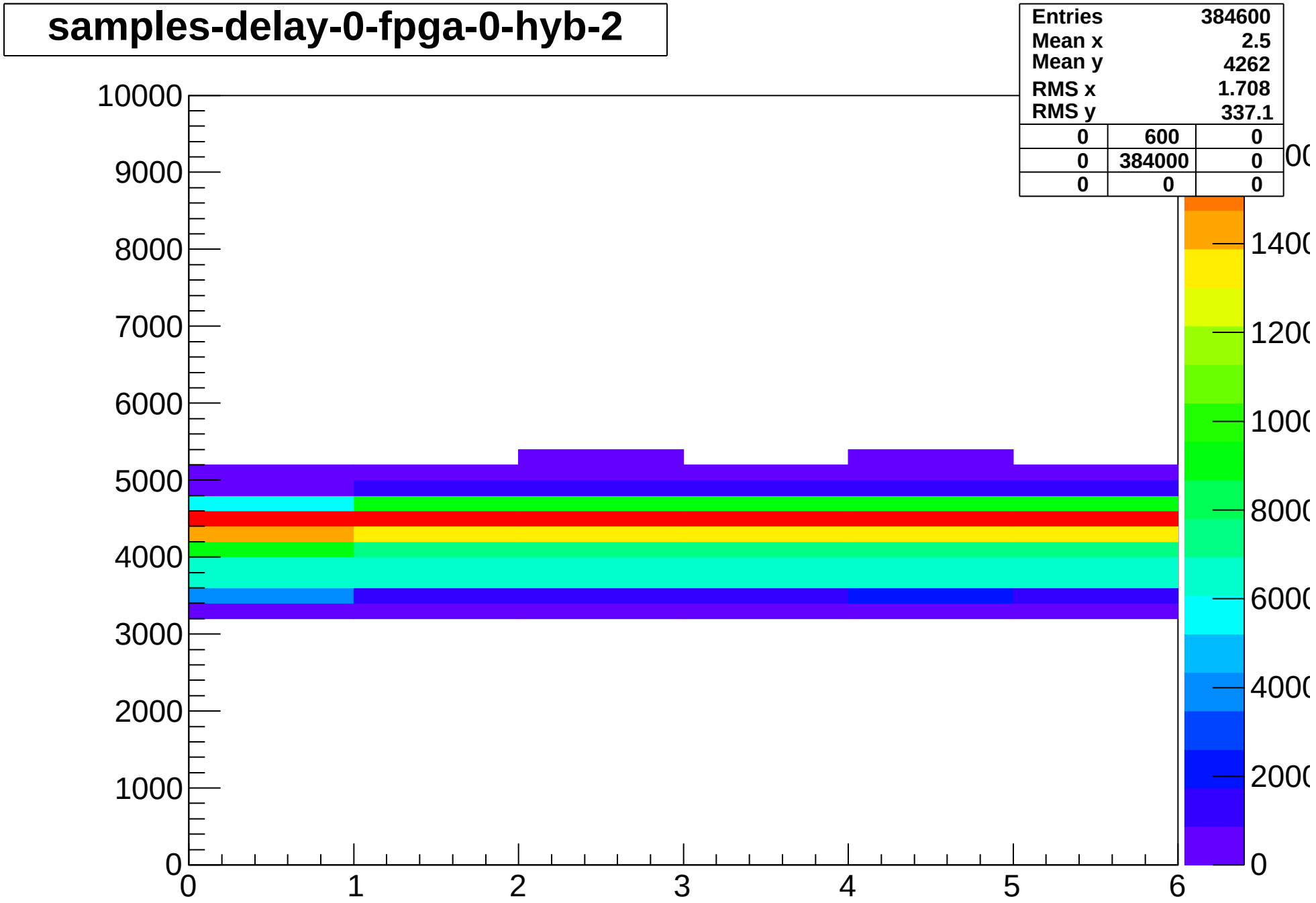
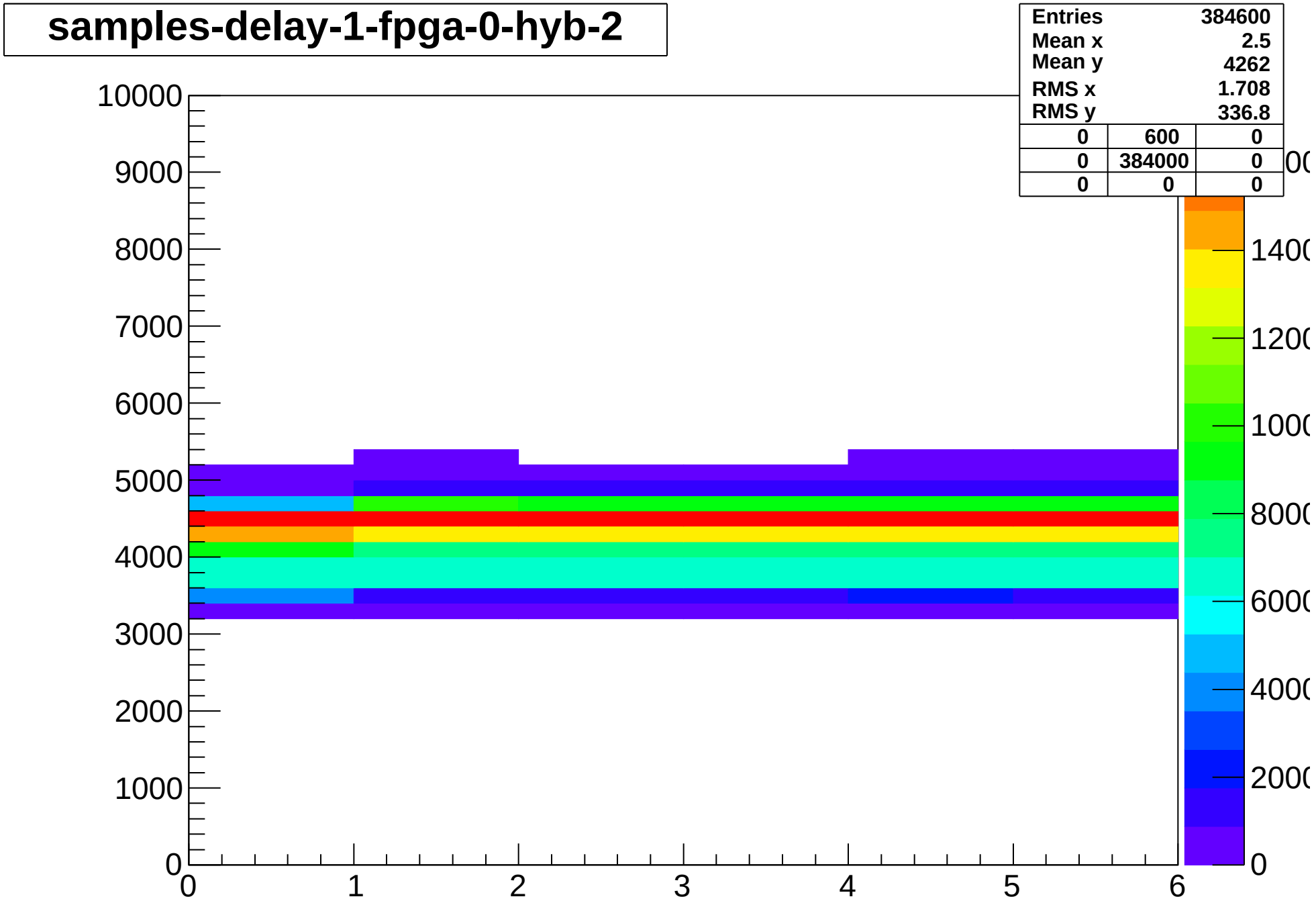
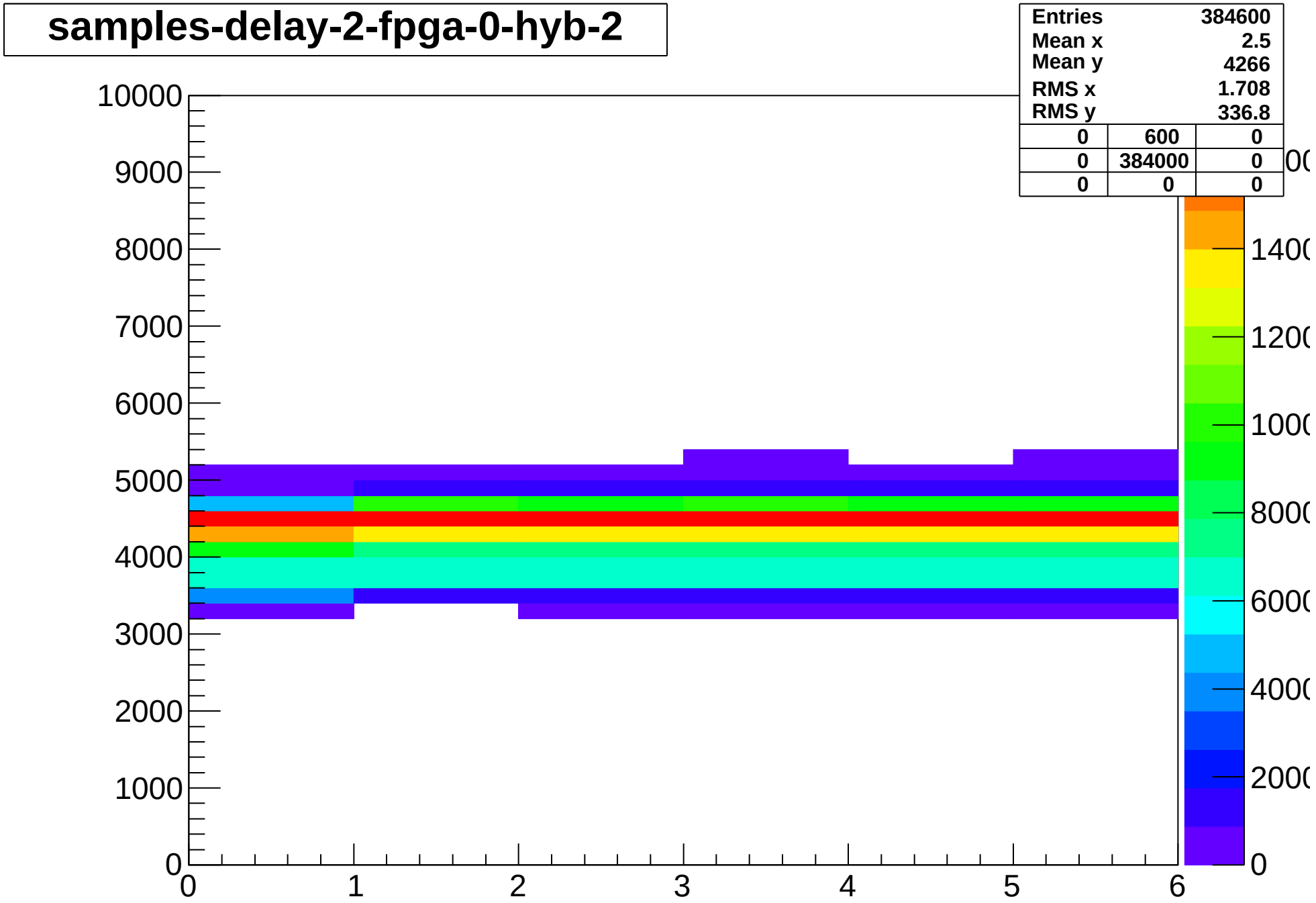
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

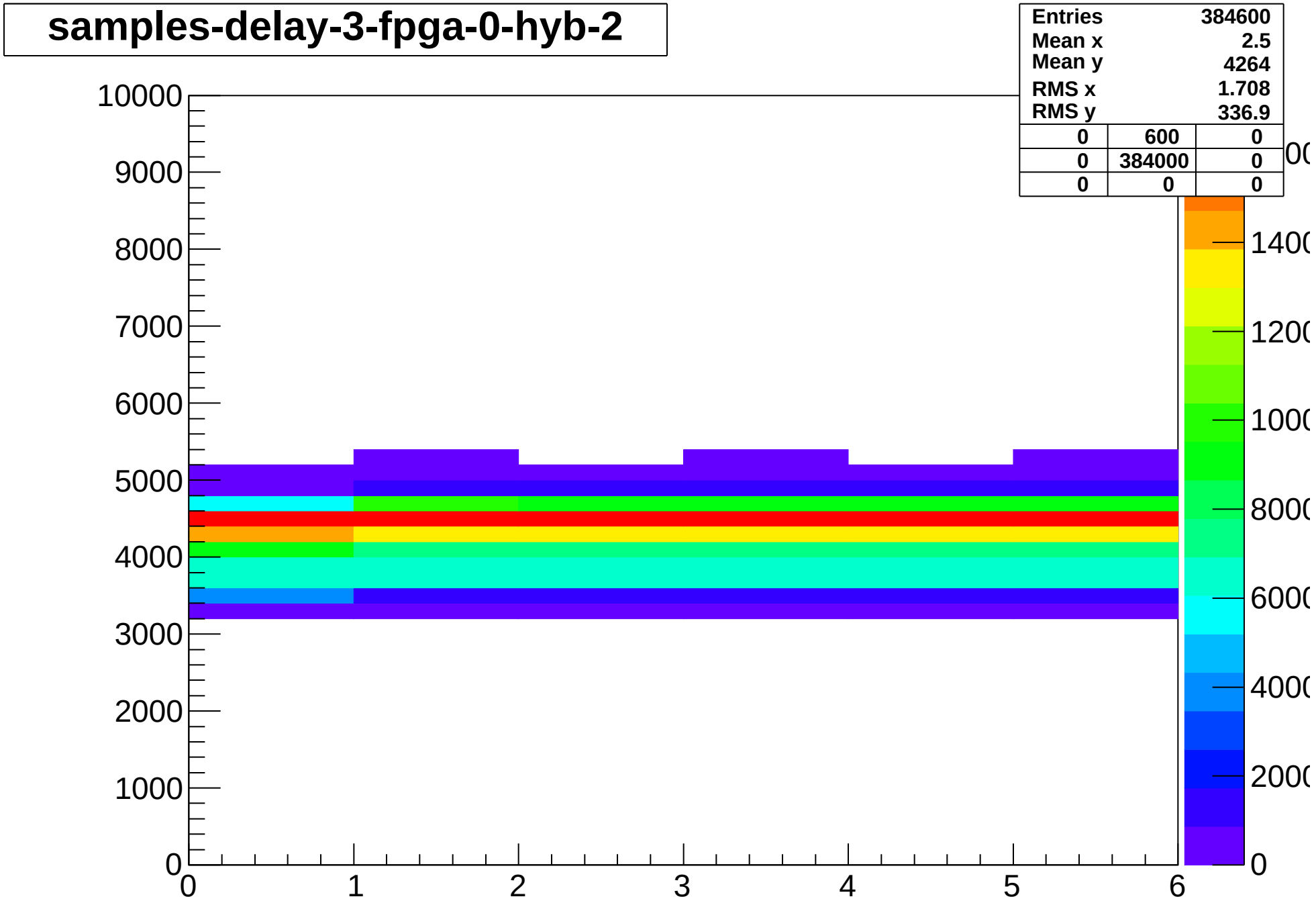

samples-delay-8-fpga-0-hyb-1
Entries 8691960
Mean x 2.5
Mean y 4486
RMS x 1.708
RMS y 288.6
0 13560 0
0 8678400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
400
350
300
250
200
150
100
50
0

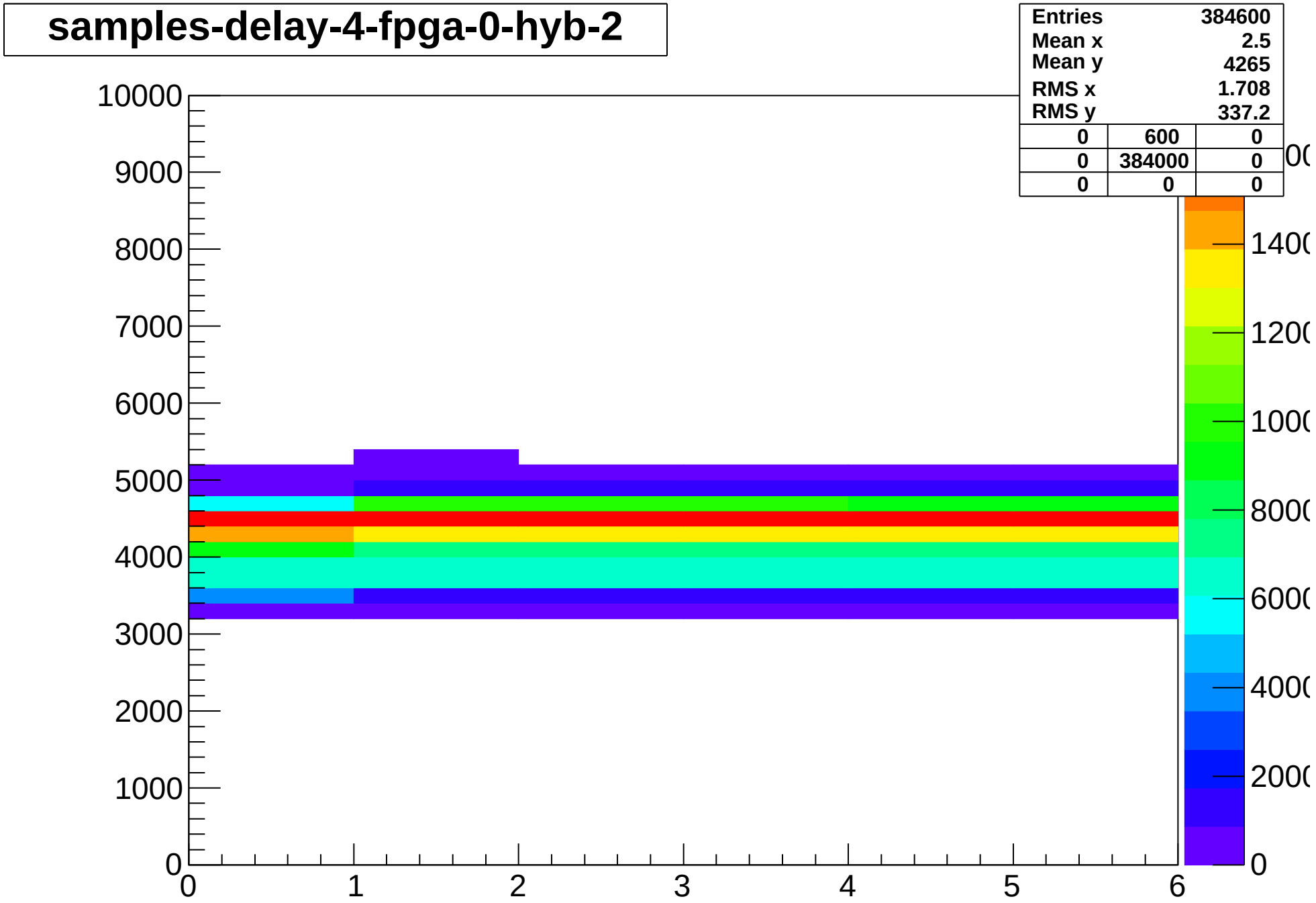

samples-fpga-0-hyb-2
Entries 1.176876e+07
Mean x 2.5
Mean y 4265
RMS x 1.708
RMS y 337.3
0 18360 0
0 1.17504e+07 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
400
300
200
100
0

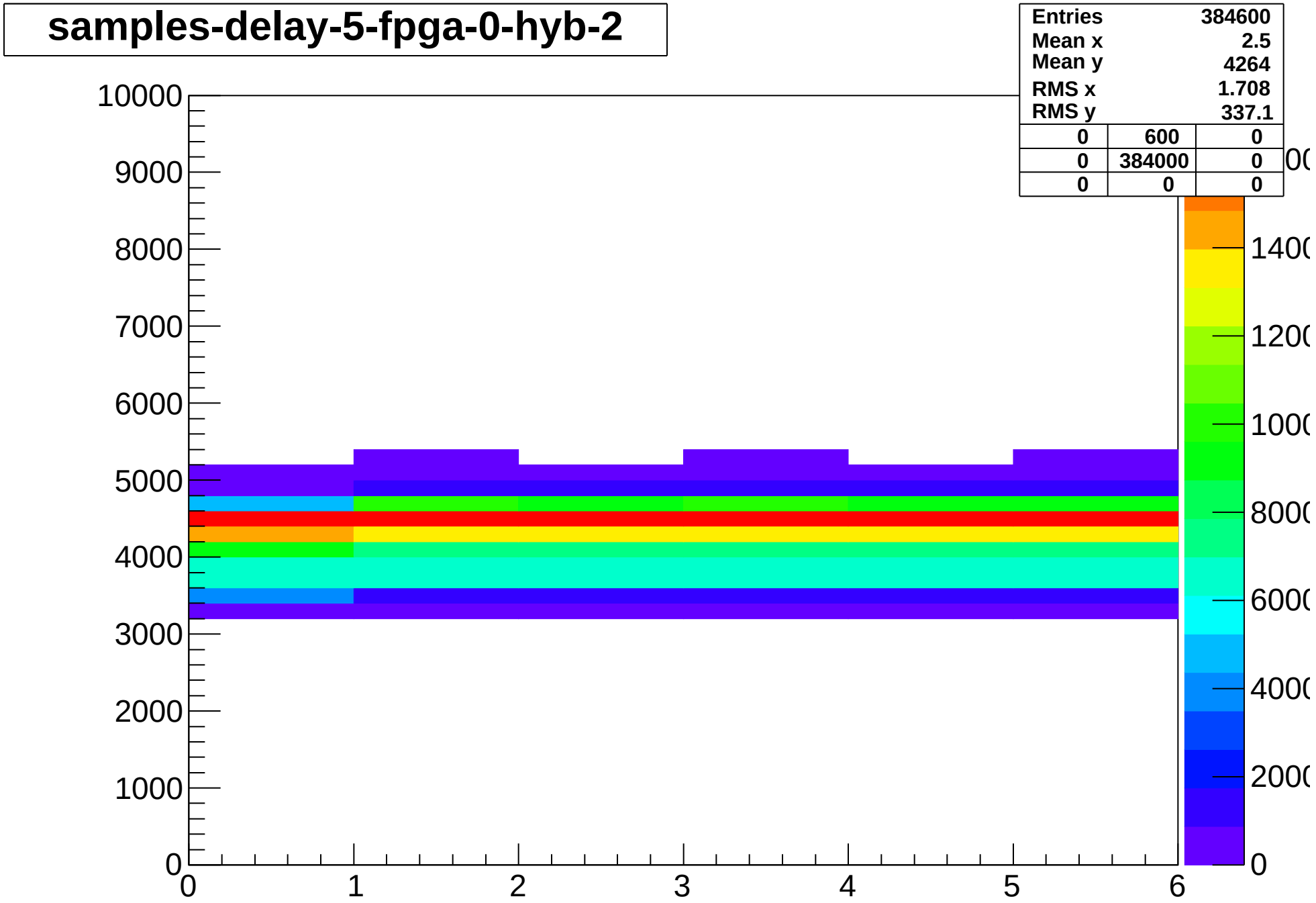

samples-delay-0-fpga-0-hyb-2
Entries 384600
Mean x 2.5
Mean y 4262
RMS x 1.708
RMS y 337.1
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1400
1200
1000
8000
6000
4000
2000
0

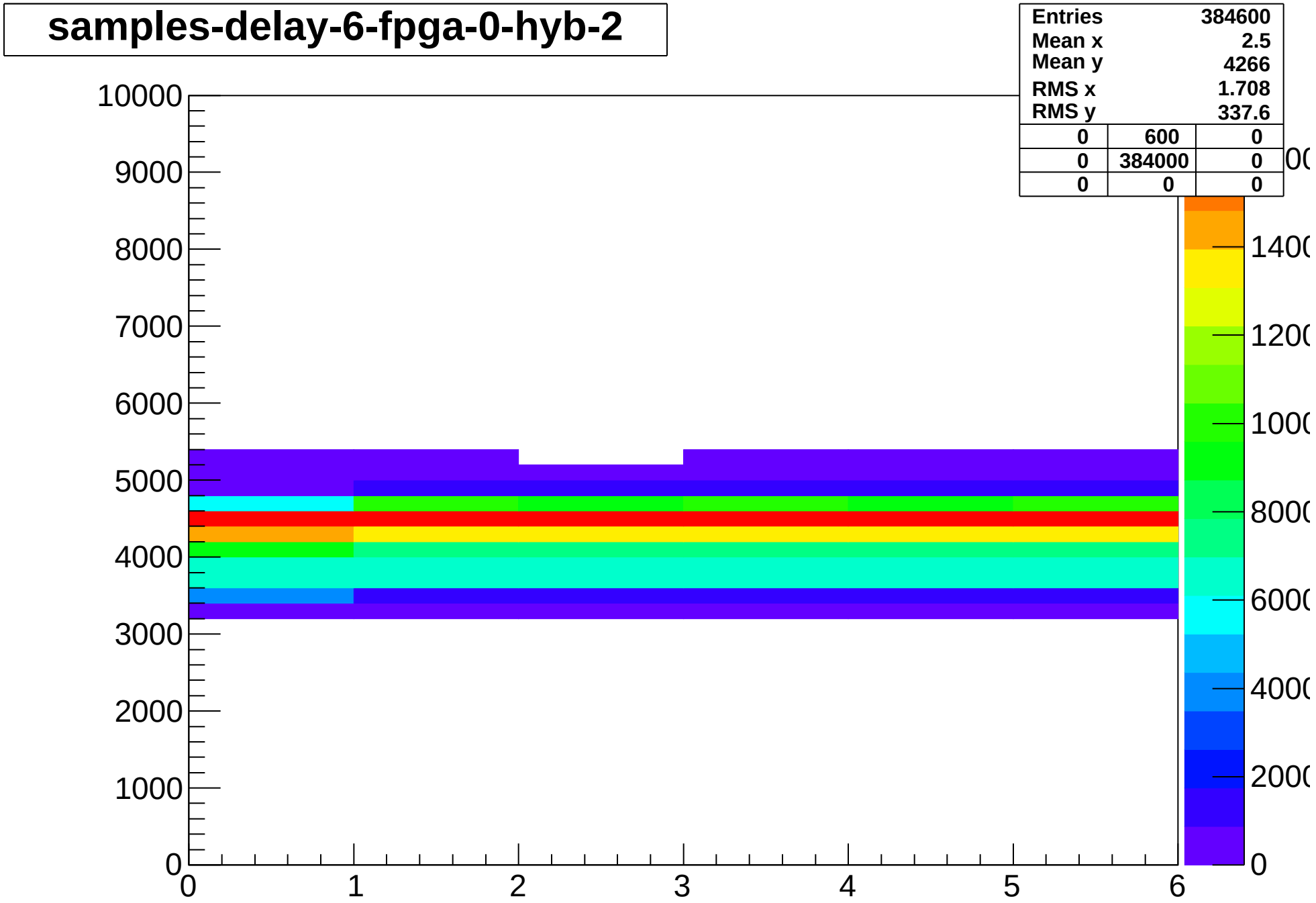

samples-delay-1-fpga-0-hyb-2
Entries 384600
Mean x 2.5
Mean y 4262
RMS x 1.708
RMS y 336.8
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1400
1200
1000
8000
6000
4000
2000
0

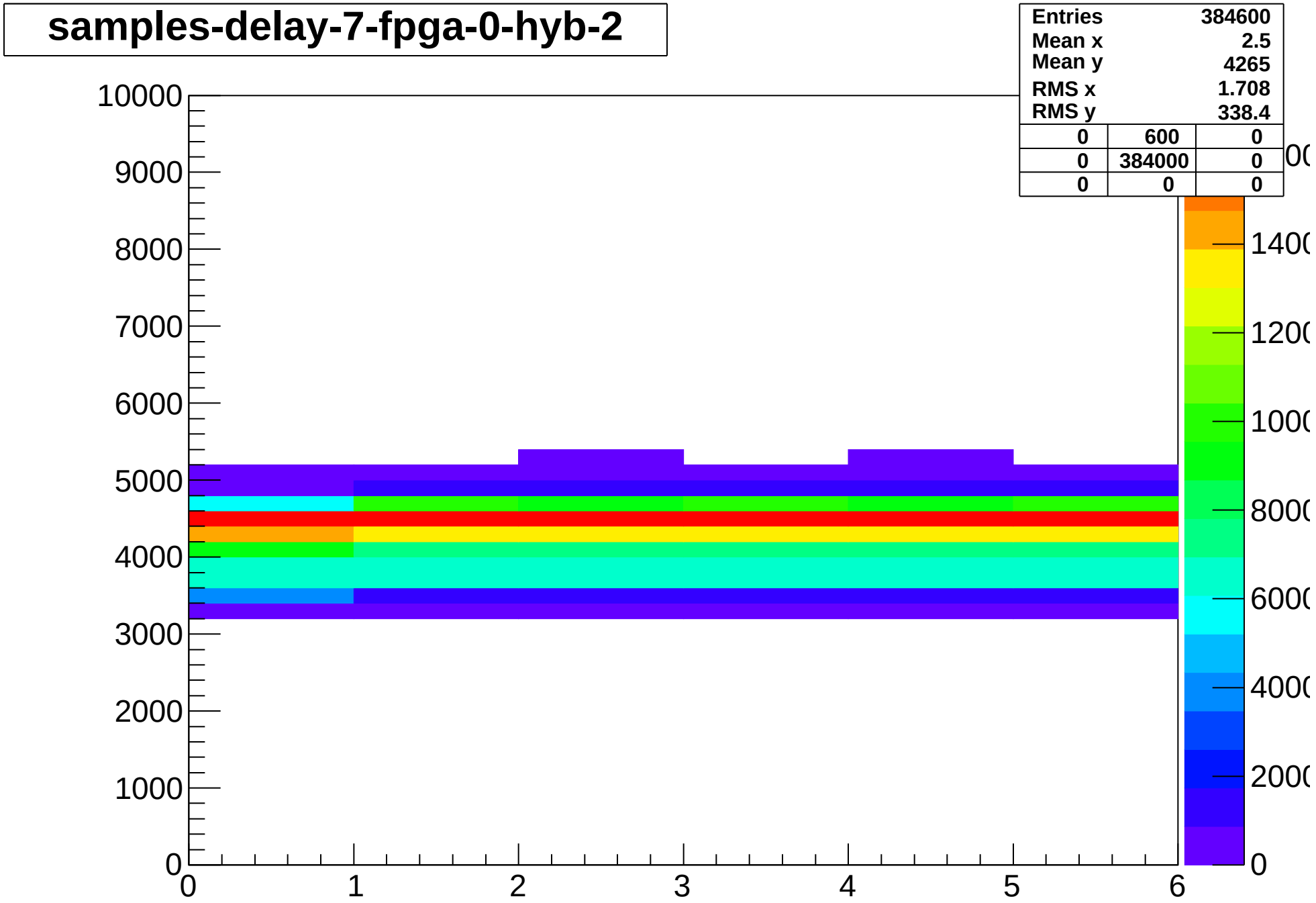

samples-delay-2-fpga-0-hyb-2
Entries 384600
Mean x 2.5
Mean y 4266
RMS x 1.708
RMS y 336.8
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1400
1200
1000
8000
6000
4000
2000
0

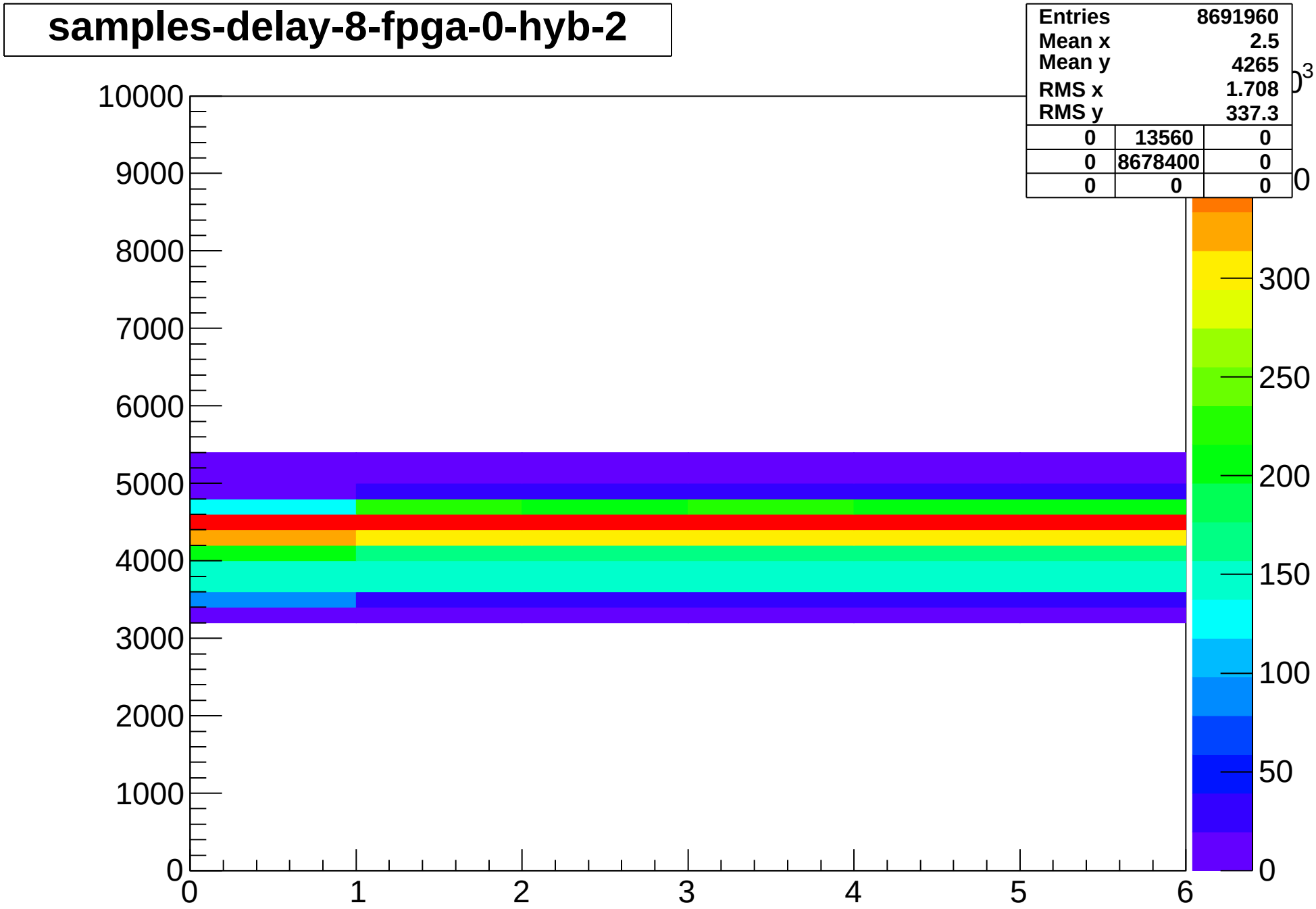

samples-delay-3-fpga-0-hyb-2
Entries 384600
Mean x 2.5
Mean y 4264
RMS x 1.708
RMS y 336.9
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1400
1200
1000
8000
6000
4000
2000
0

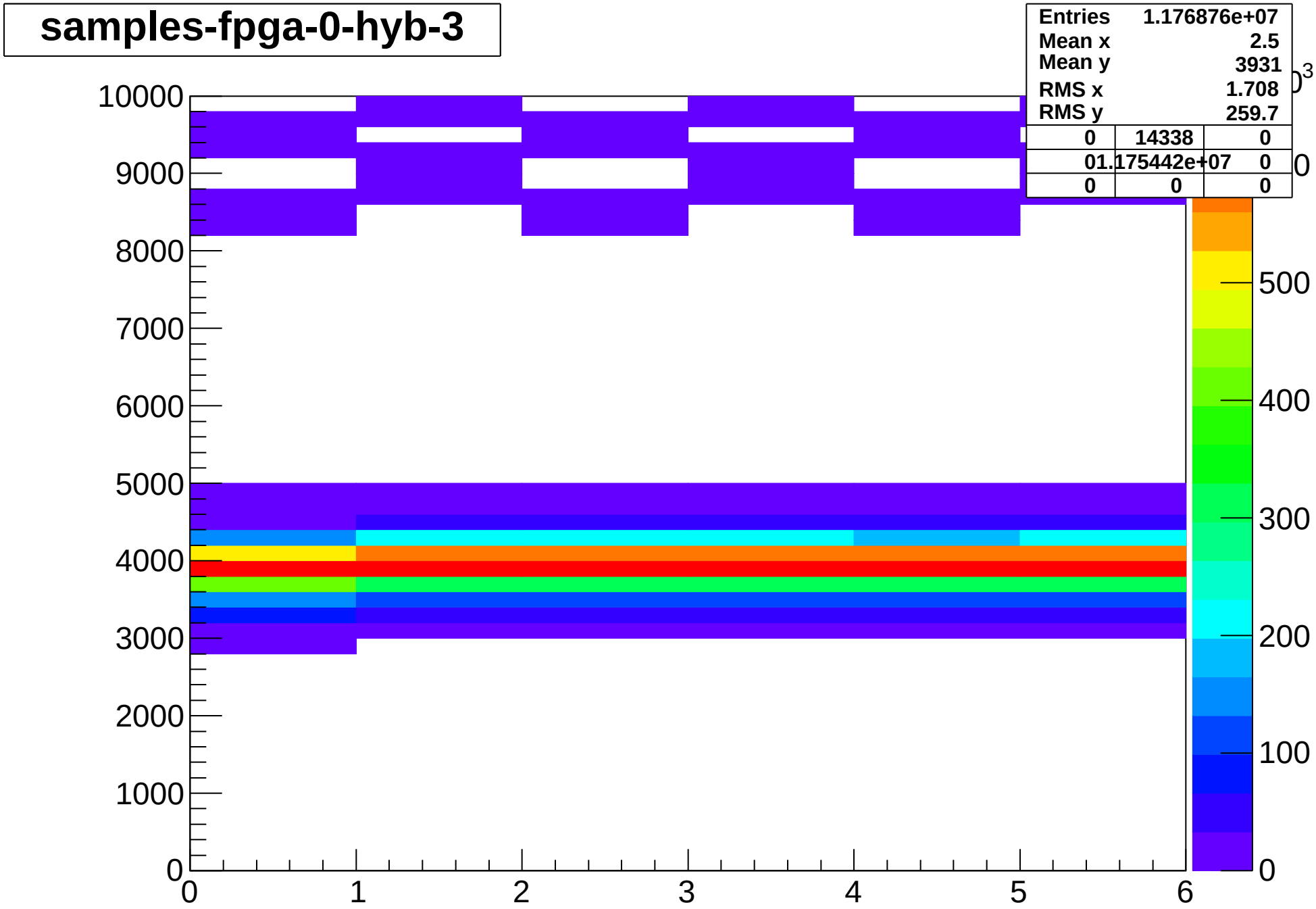

samples-delay-4-fpga-0-hyb-2
Entries 384600
Mean x 2.5
Mean y 4265
RMS x 1.708
RMS y 337.2
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1400
1200
1000
8000
6000
4000
2000
0

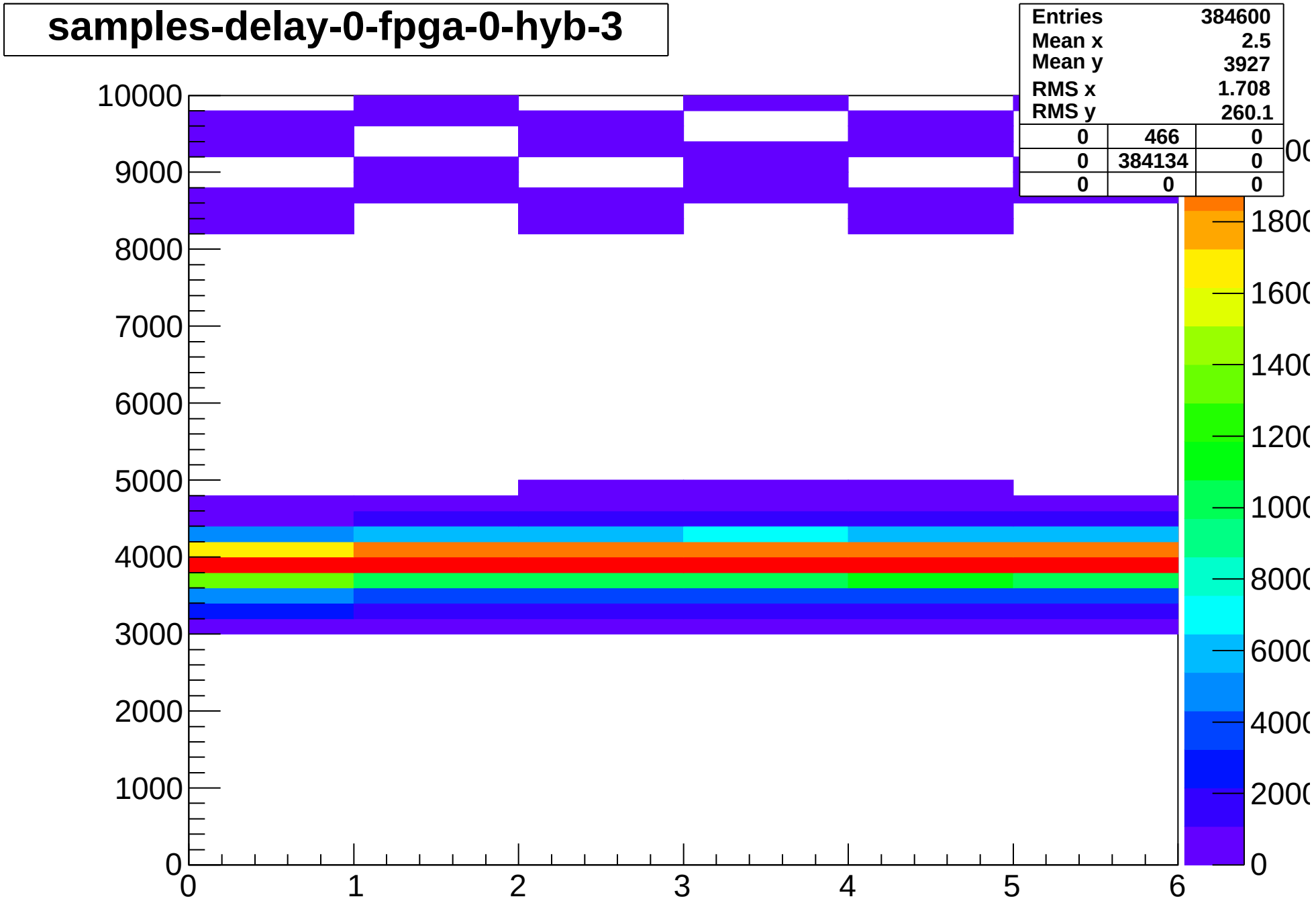

samples-delay-5-fpga-0-hyb-2
Entries 384600
Mean x 2.5
Mean y 4264
RMS x 1.708
RMS y 337.1
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1400
1200
1000
8000
6000
4000
2000
0

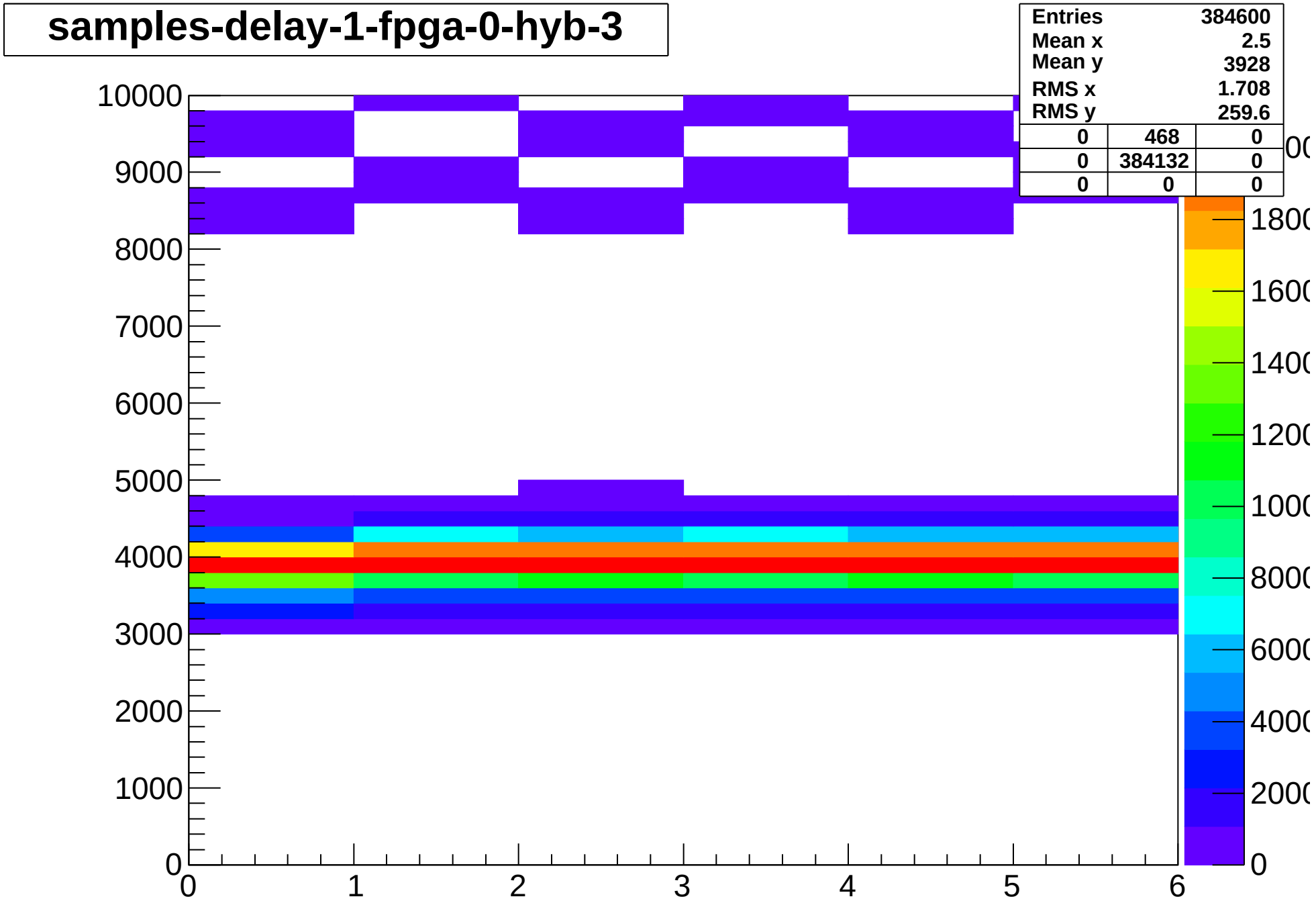

samples-delay-6-fpga-0-hyb-2
Entries 384600
Mean x 2.5
Mean y 4266
RMS x 1.708
RMS y 337.6
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1400
1200
1000
8000
6000
4000
2000
0

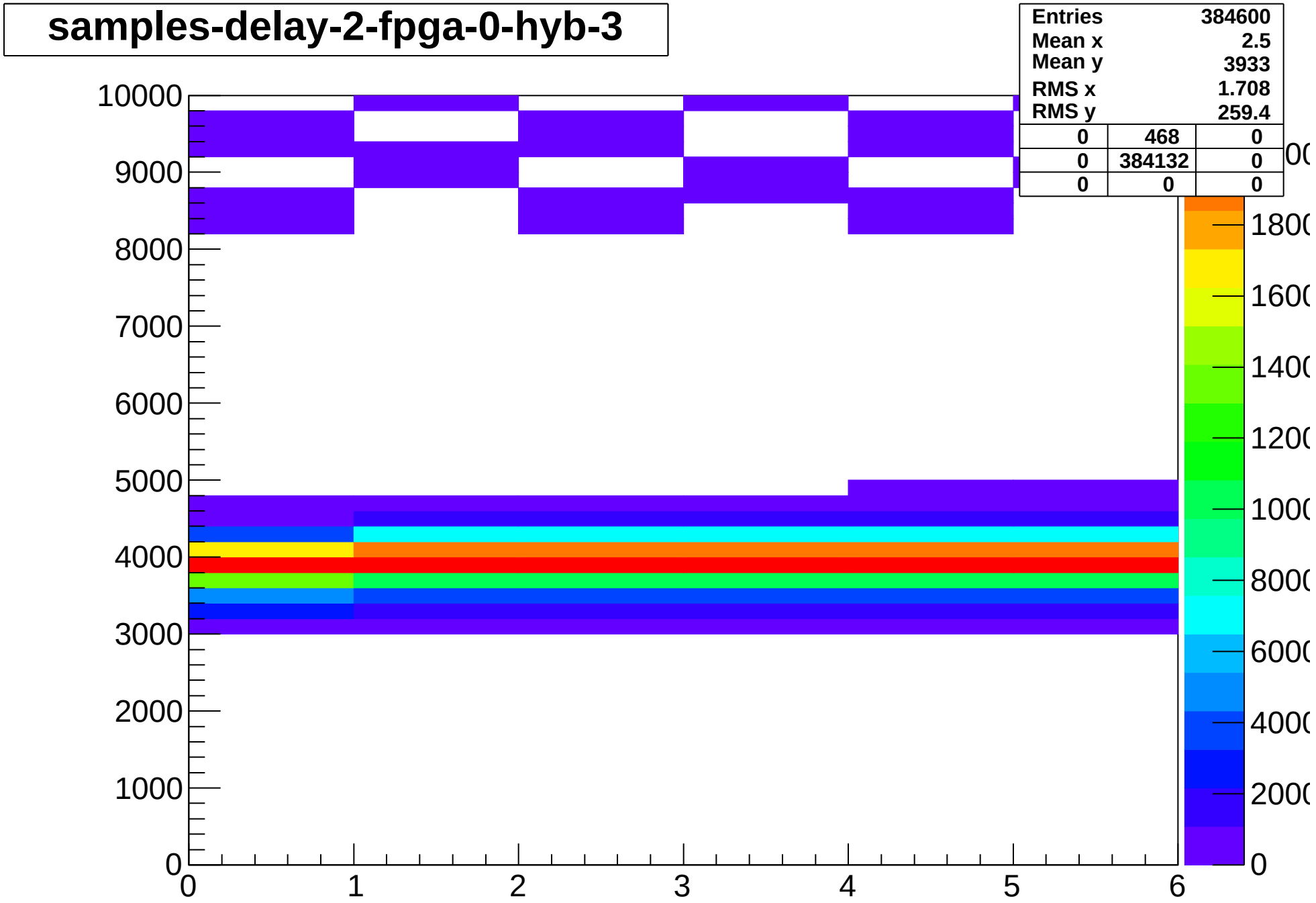

samples-delay-7-fpga-0-hyb-2
Entries 384600
Mean x 2.5
Mean y 4265
RMS x 1.708
RMS y 338.4
0 600 0
0 384000 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1400
1200
1000
8000
6000
4000
2000
0

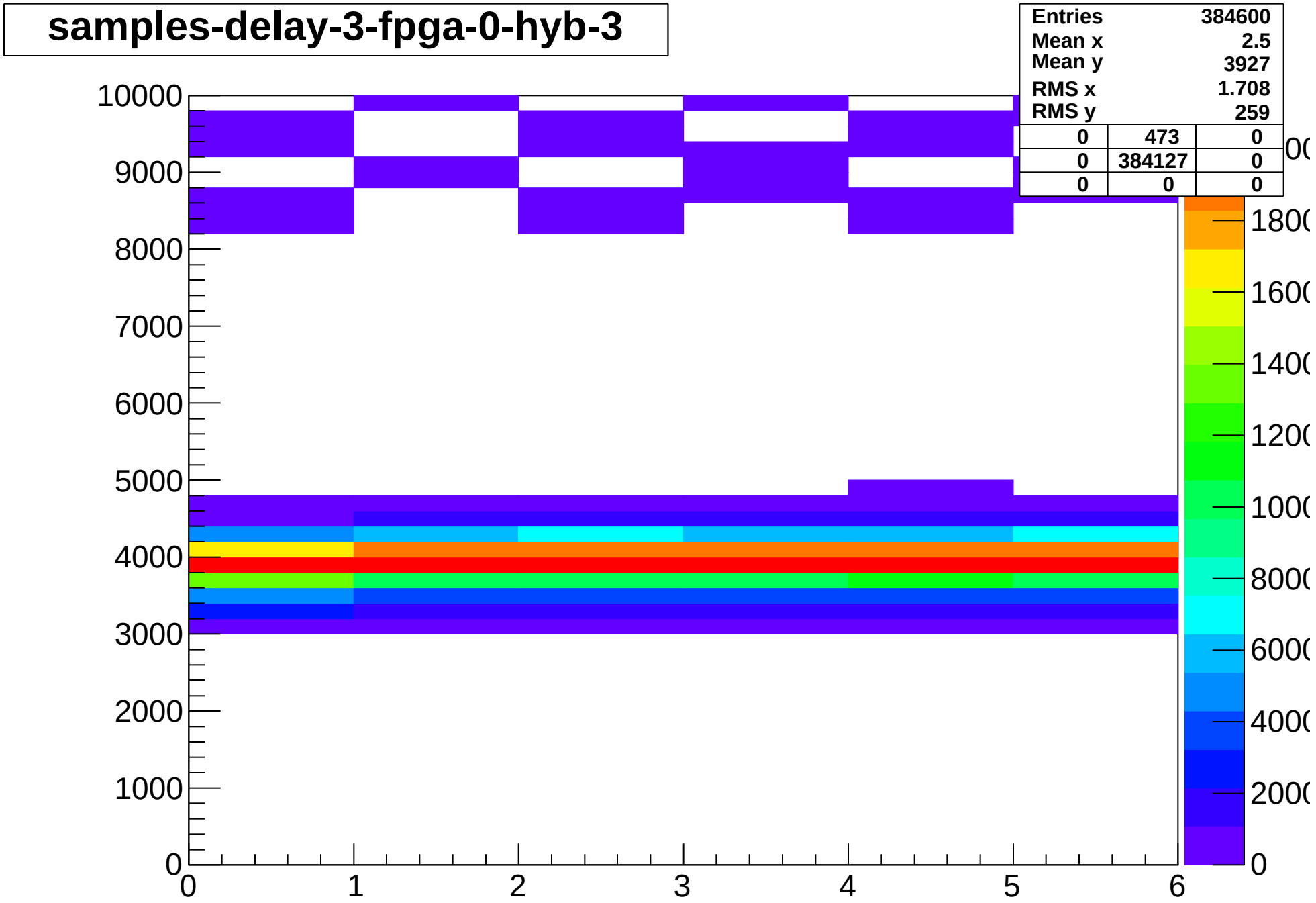

samples-delay-8-fpga-0-hyb-2
Entries 8691960
Mean x 2.5
Mean y 4265
RMS x 1.708
RMS y 337.3
0 13560 0
0 8678400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
300
250
200
150
100
50
0

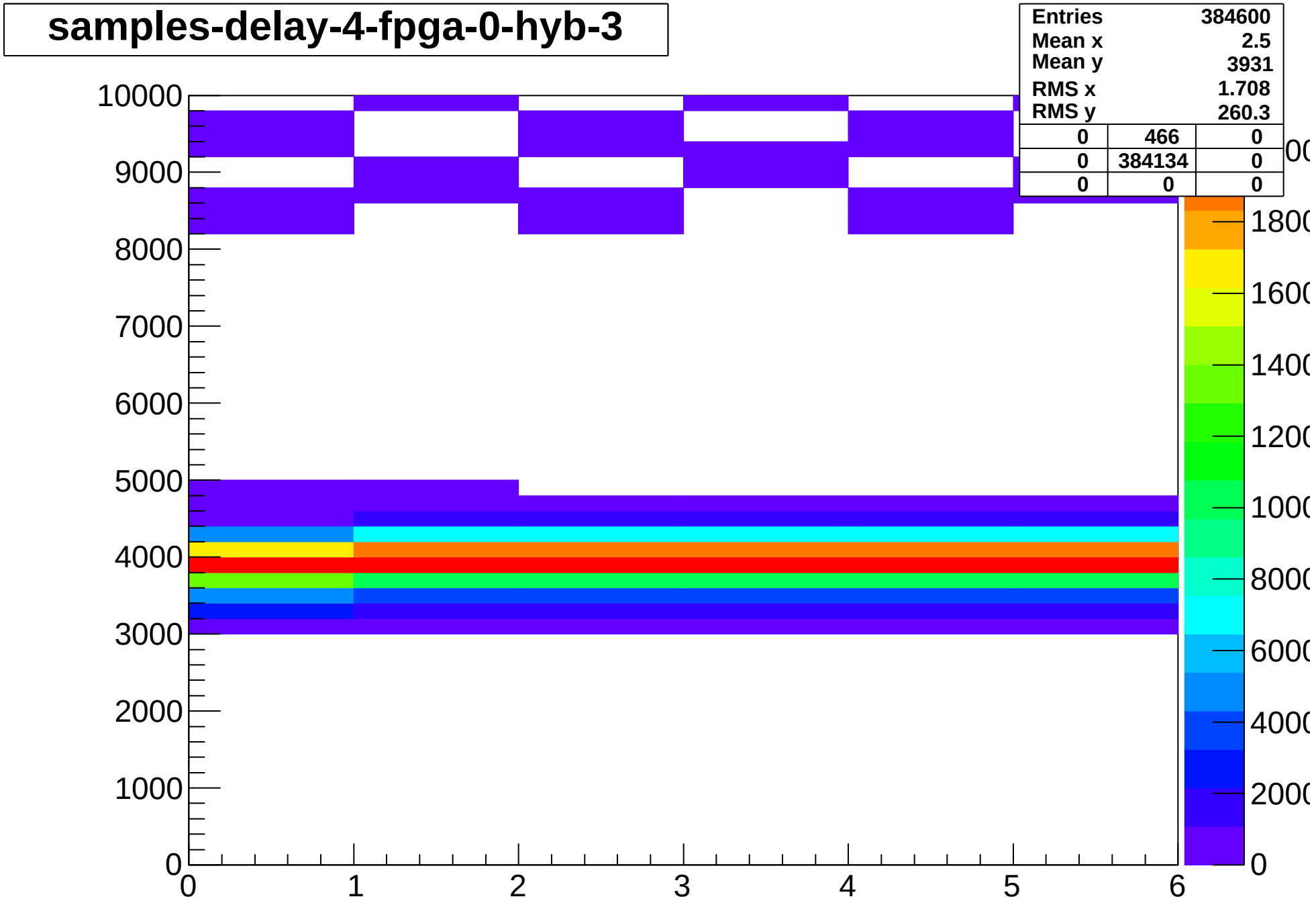

samples-fpga-0-hyb-3
Entries 1.176876e+07
Mean x 2.5
Mean y 3931
RMS x 1.708
RMS y 259.7
0 14338 0
0 1.175442e+07 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
500
400
300
200
100
0

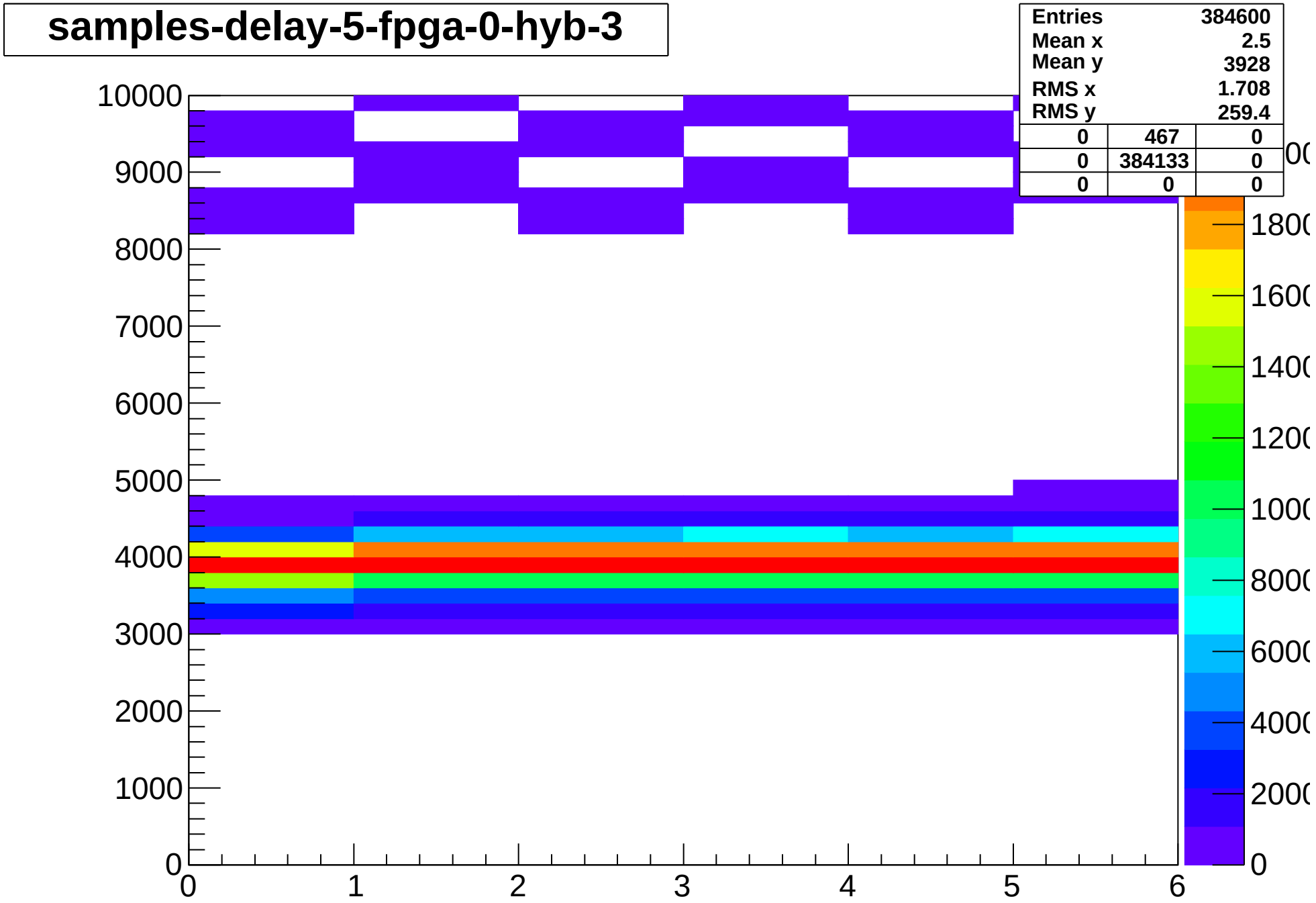

samples-delay-0-fpga-0-hyb-3
Entries 384600
Mean x 2.5
Mean y 3927
RMS x 1.708
RMS y 260.1
0 466 0
0 384134 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

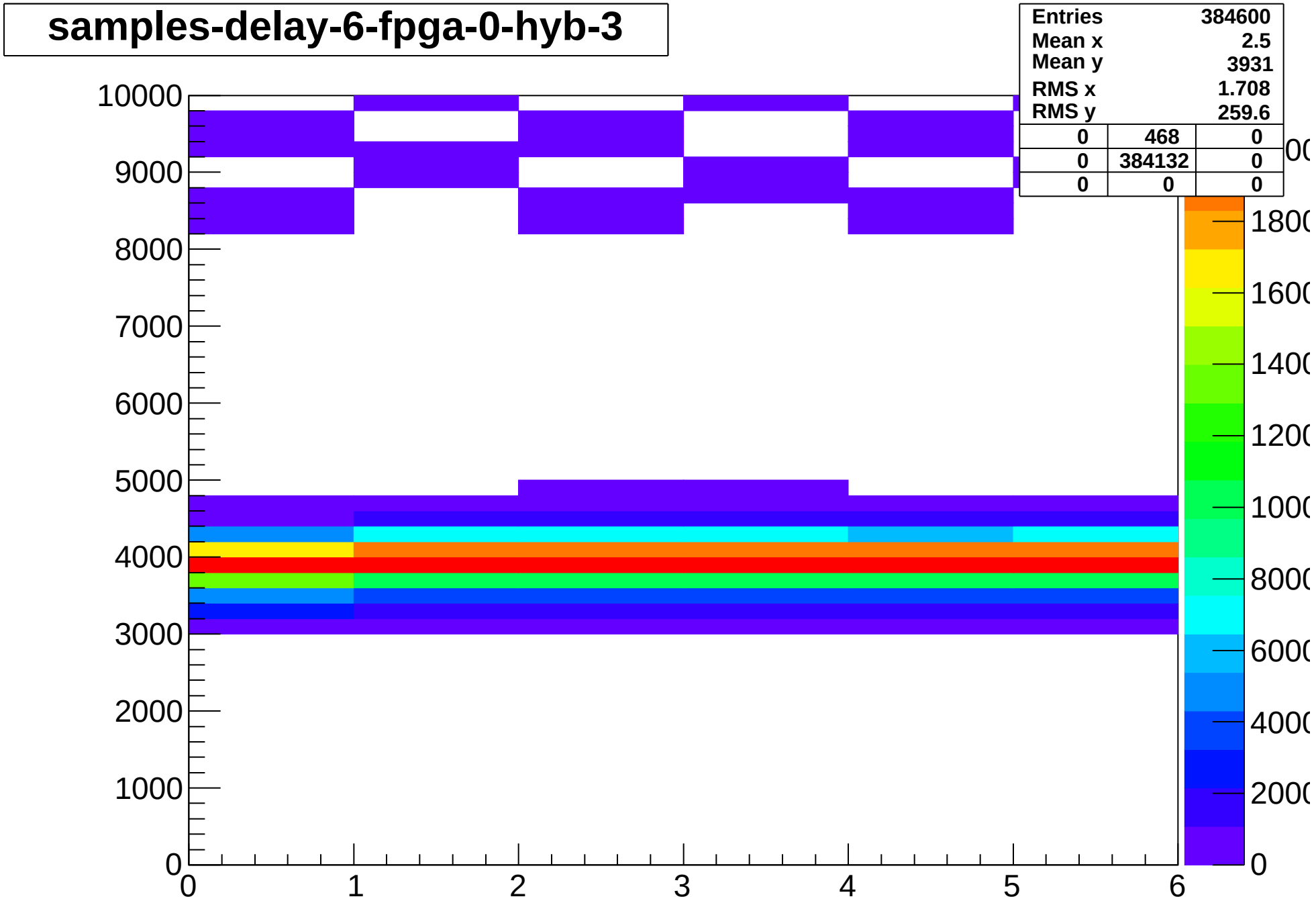

samples-delay-1-fpga-0-hyb-3
Entries 384600
Mean x 2.5
Mean y 3928
RMS x 1.708
RMS y 259.6
0 468 0
0 384132 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

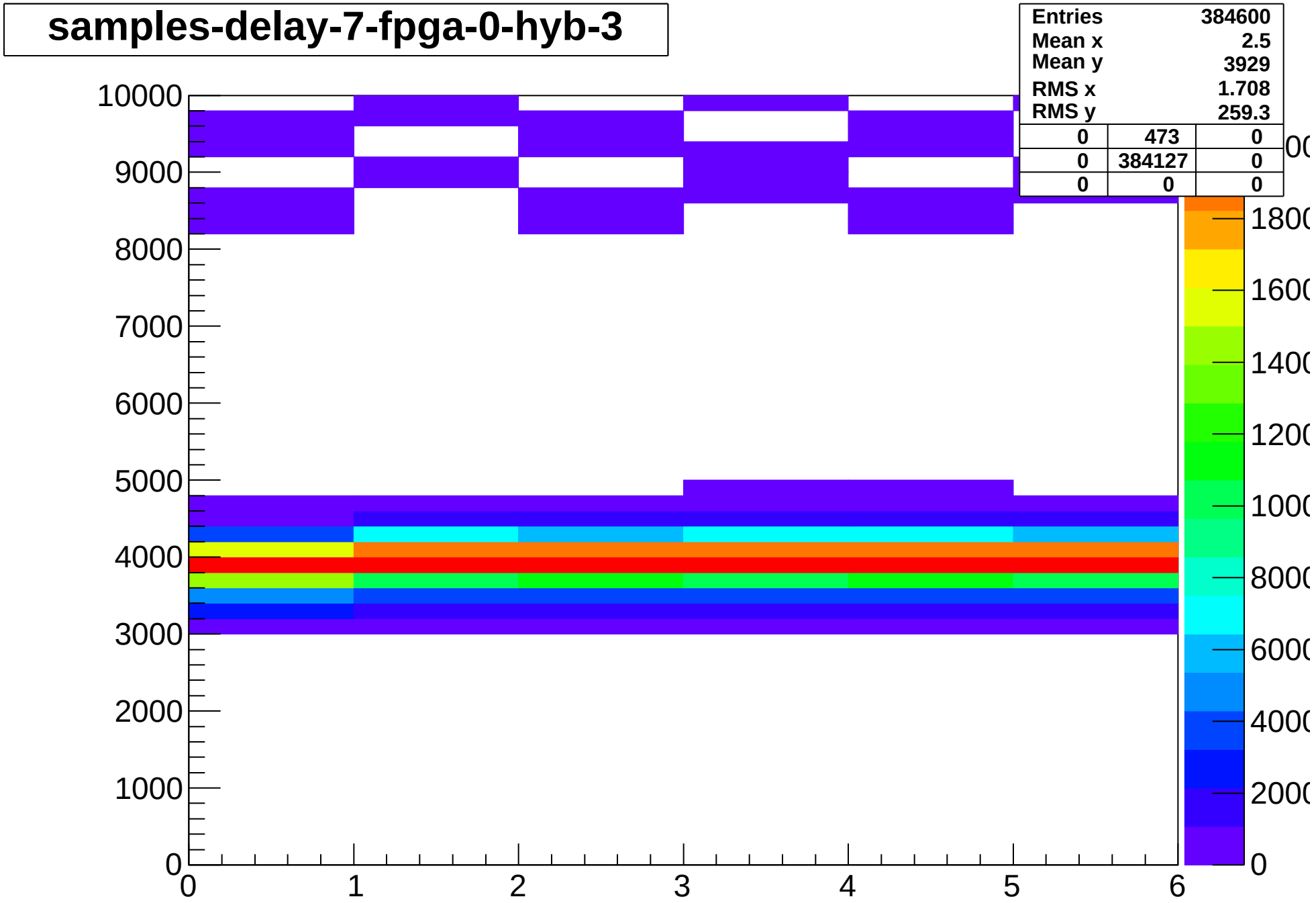

samples-delay-2-fpga-0-hyb-3
Entries 384600
Mean x 2.5
Mean y 3933
RMS x 1.708
RMS y 259.4
0 468 0
0 384132 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

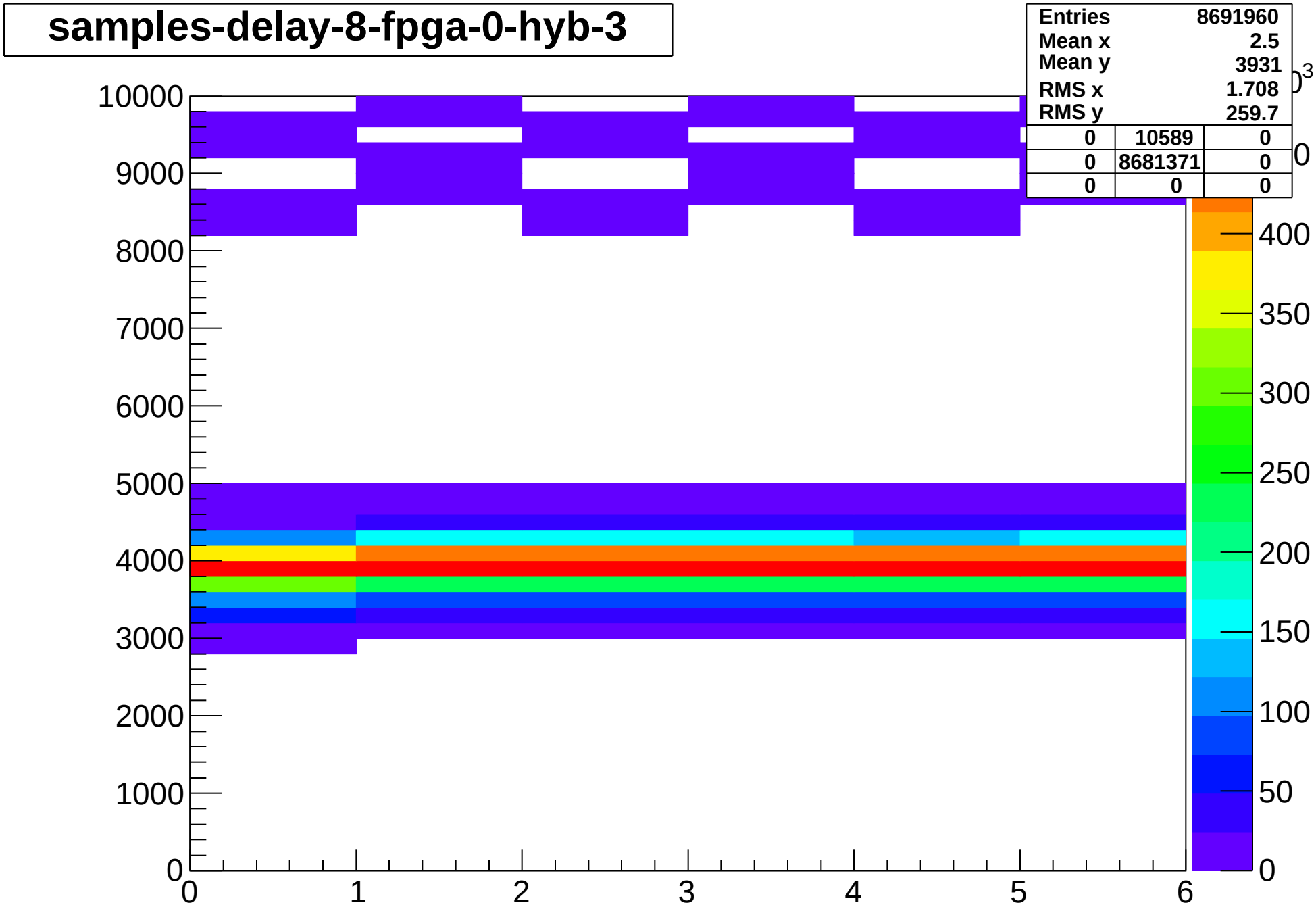

samples-delay-3-fpga-0-hyb-3
Entries 384600
Mean x 2.5
Mean y 3927
RMS x 1.708
RMS y 259
0 473 0
0 384127 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

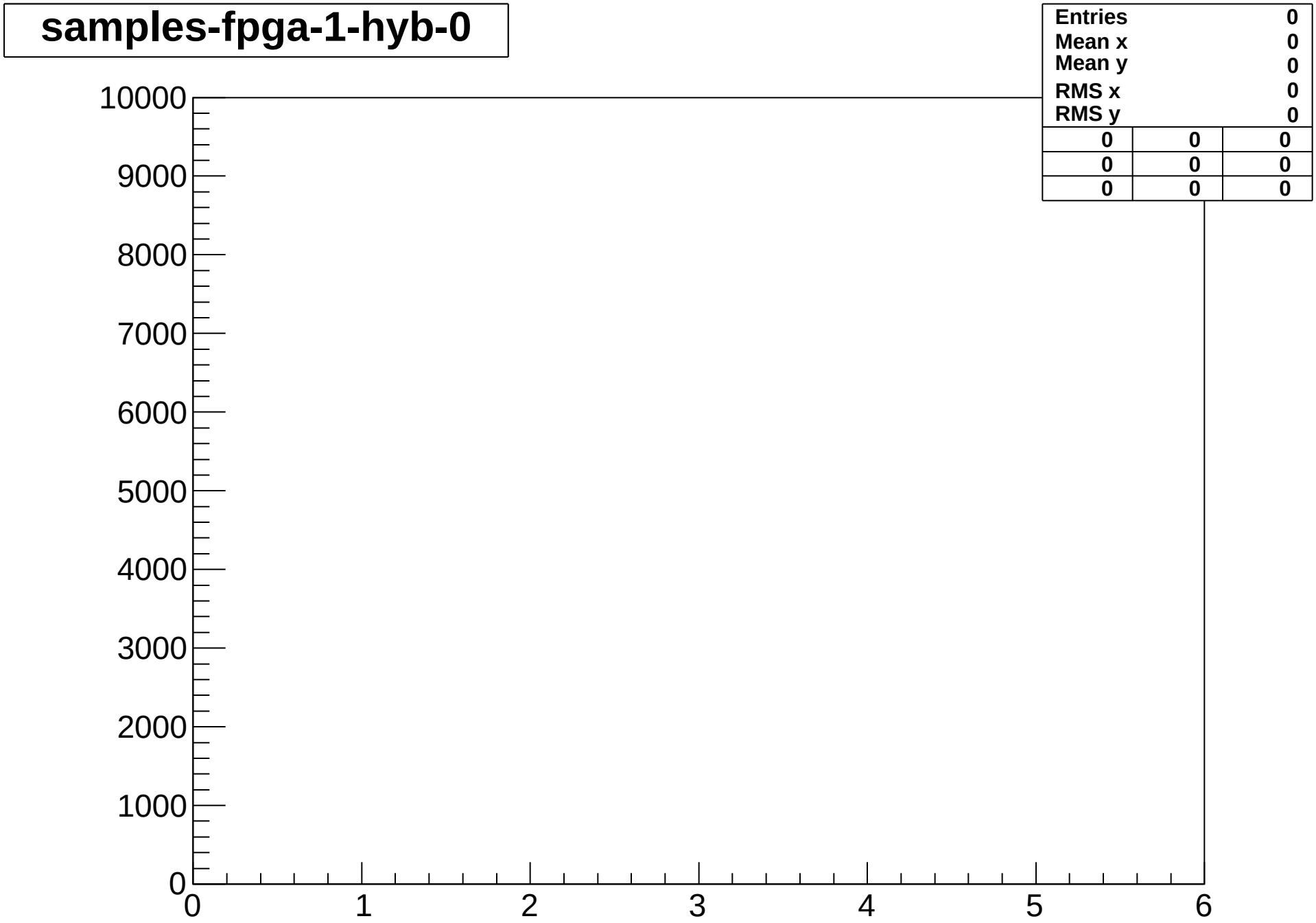

samples-delay-4-fpga-0-hyb-3
Entries 384600
Mean x 2.5
Mean y 3931
RMS x 1.708
RMS y 260.3
0 466 0
0 384134 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

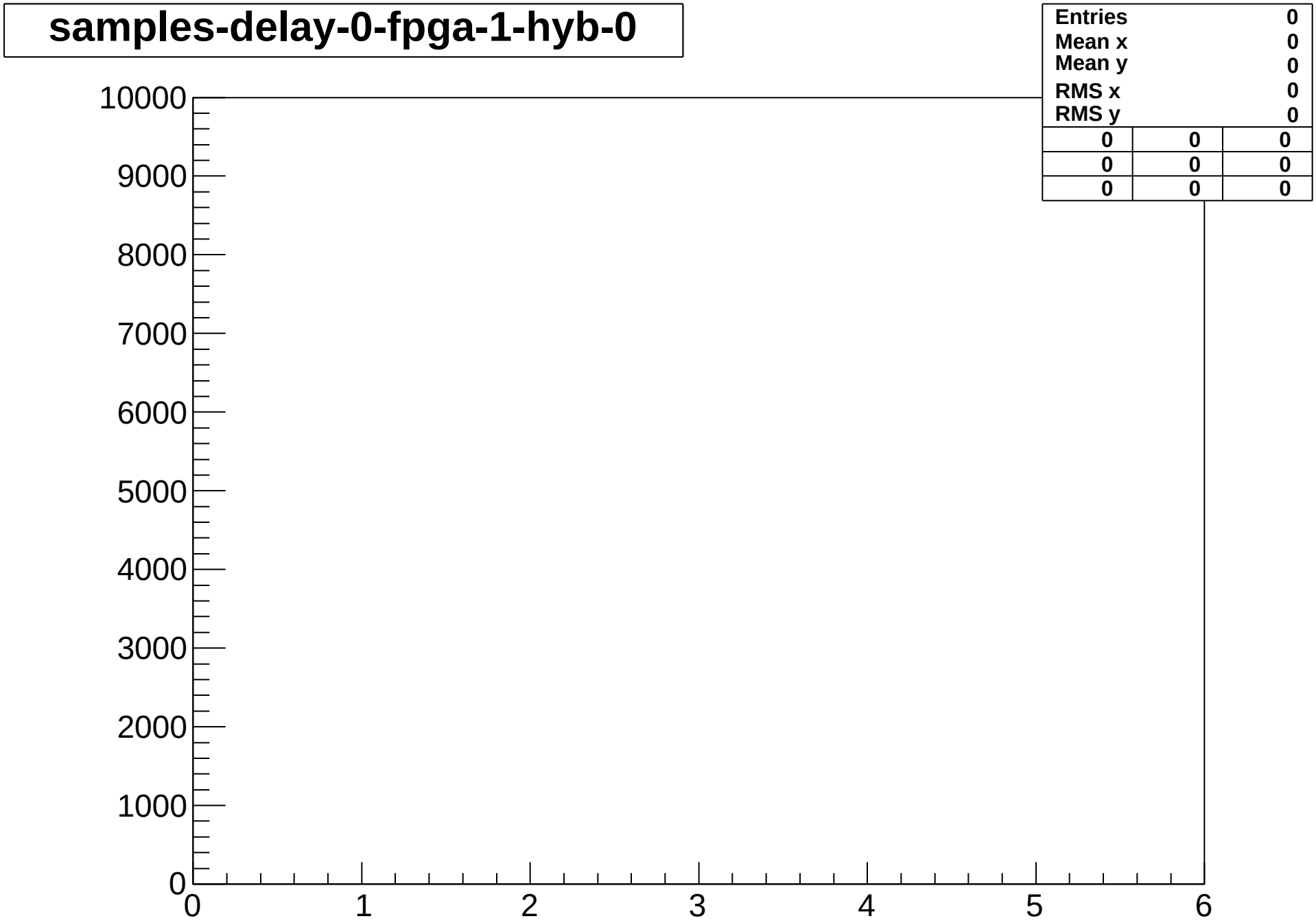

samples-delay-5-fpga-0-hyb-3
Entries 384600
Mean x 2.5
Mean y 3928
RMS x 1.708
RMS y 259.4
0 467 0
0 384133 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

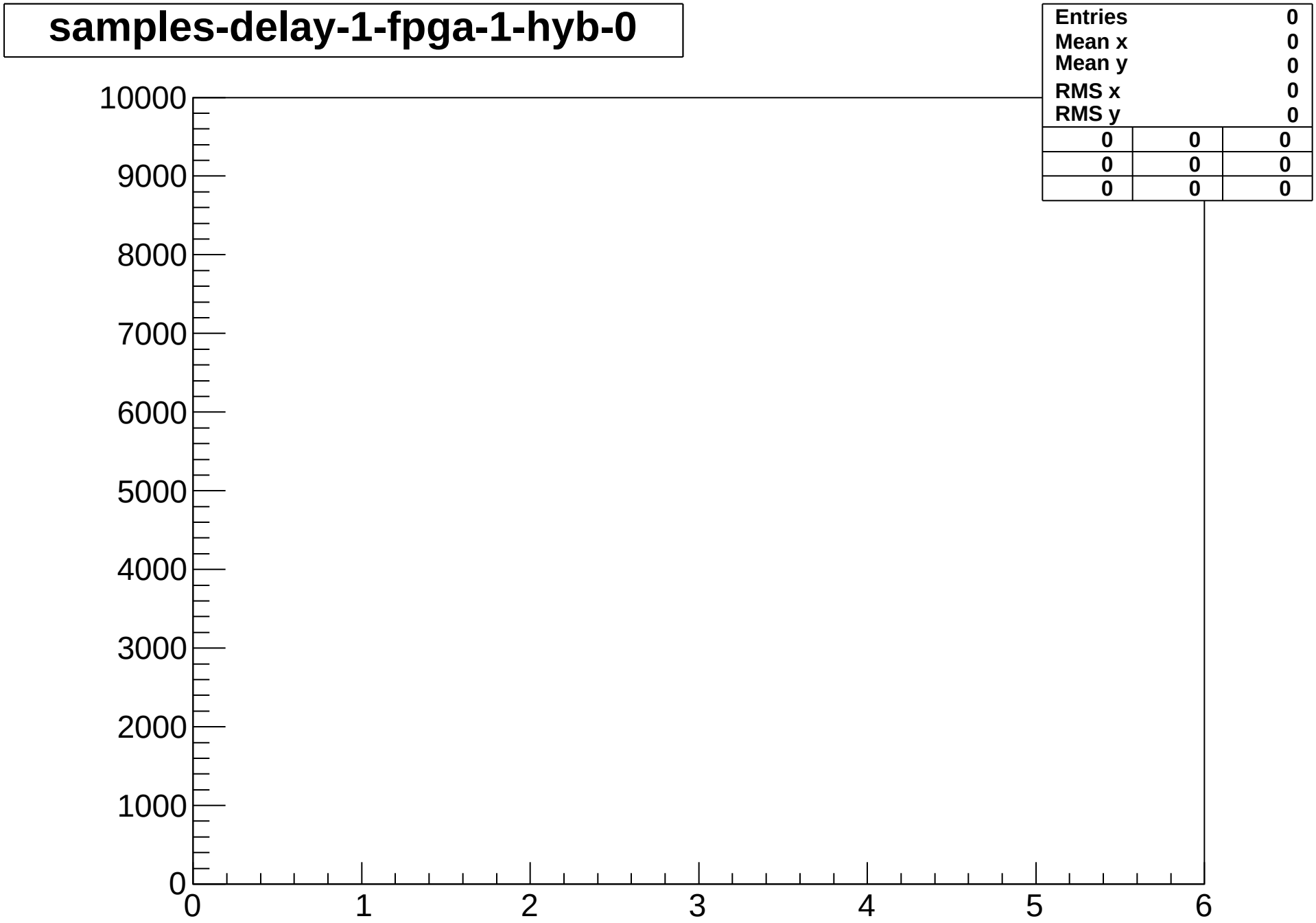

samples-delay-6-fpga-0-hyb-3
Entries 384600
Mean x 2.5
Mean y 3931
RMS x 1.708
RMS y 259.6
0 468 0
0 384132 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0


samples-delay-7-fpga-0-hyb-3
Entries 384600
Mean x 2.5
Mean y 3929
RMS x 1.708
RMS y 259.3
0 473 0
0 384127 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6
1800
1600
1400
1200
1000
8000
6000
4000
2000
0

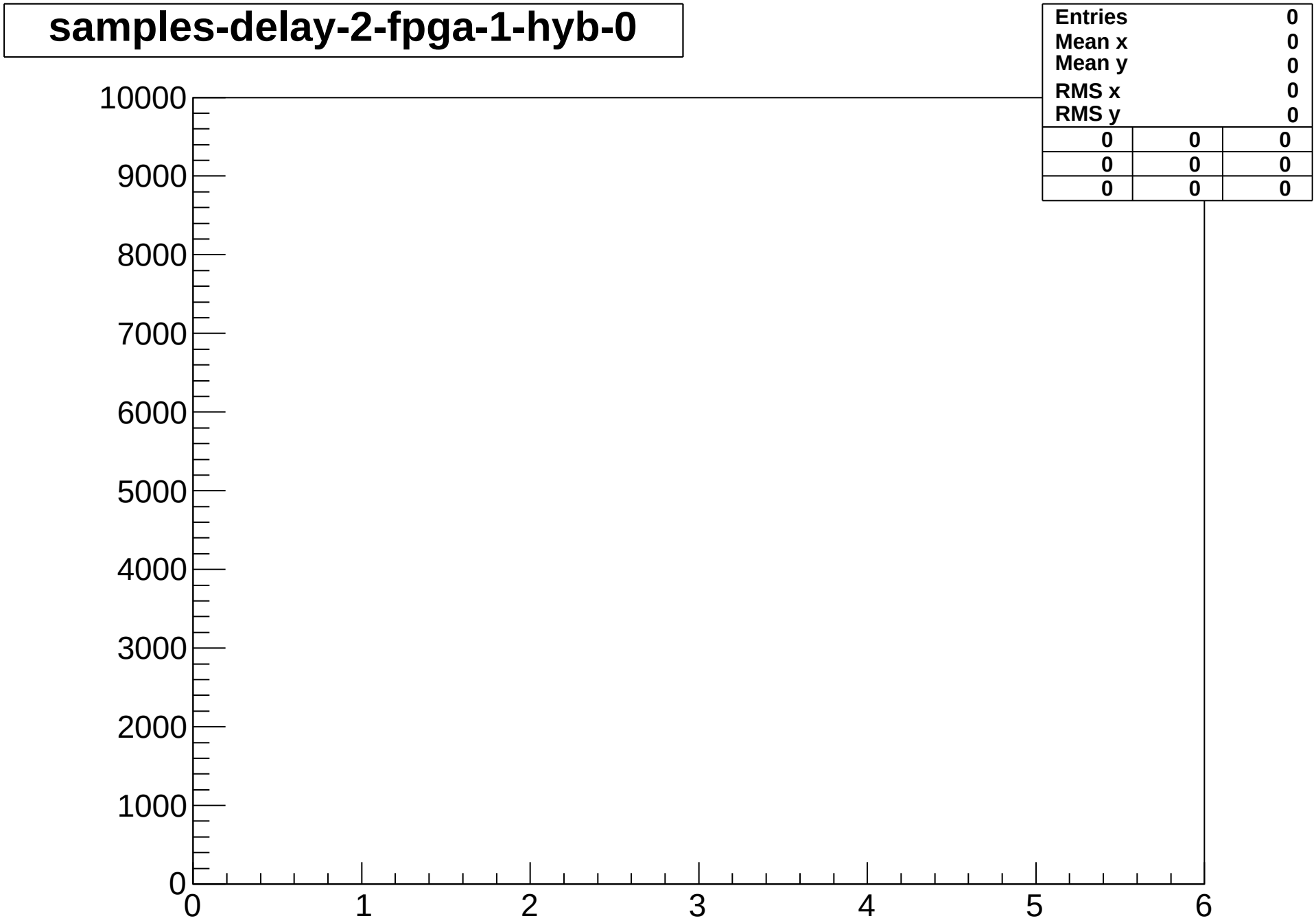

samples-delay-8-fpga-0-hyb-3
Entries 8691960
Mean x 2.5
Mean y 3931
RMS x 1.708
RMS y 259.7
0 10589 0
0 8681371 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0 1 2 3 4 5 6
400
350
300
250
200
150
100
50
0

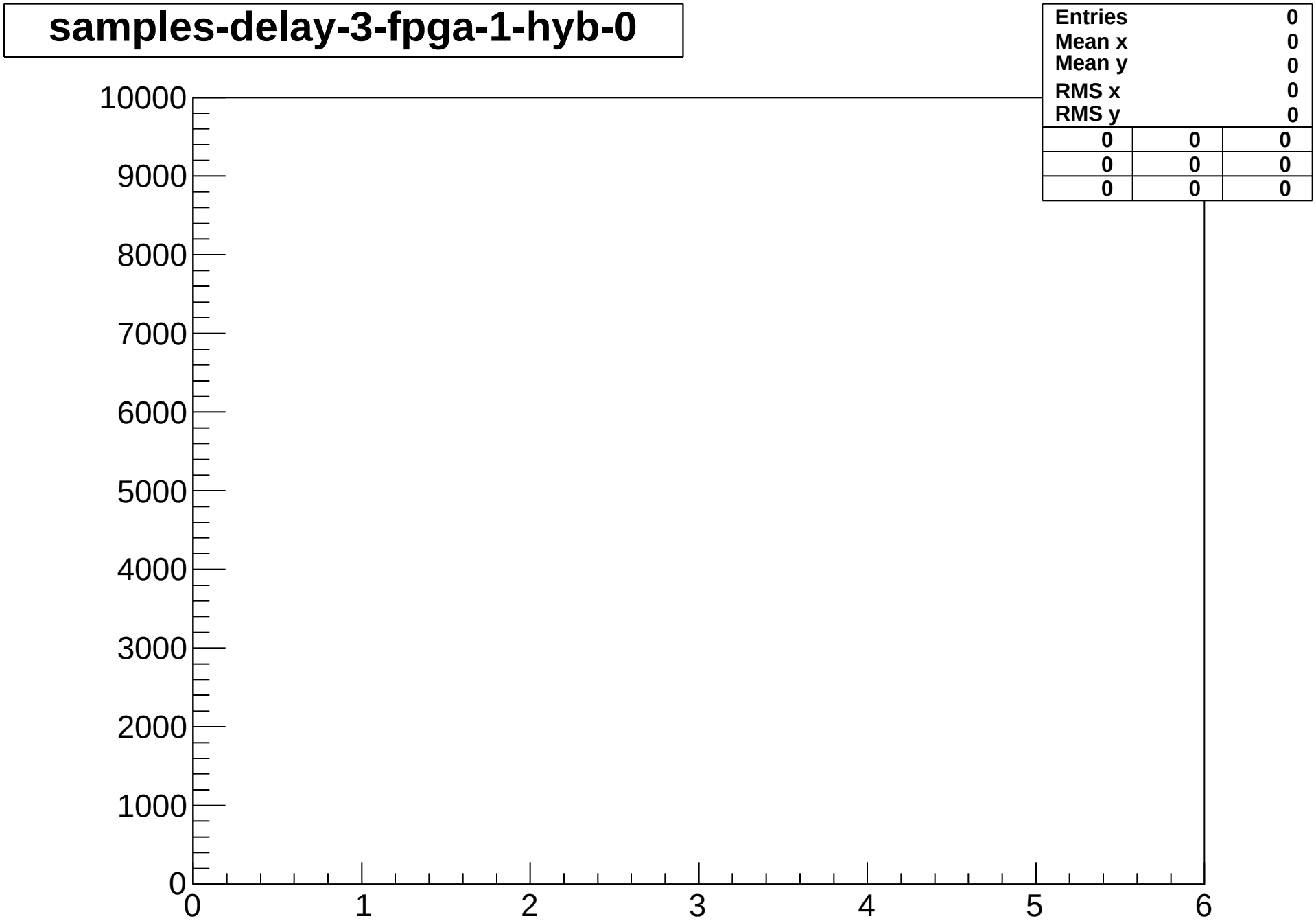

samples-fpga-1-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6

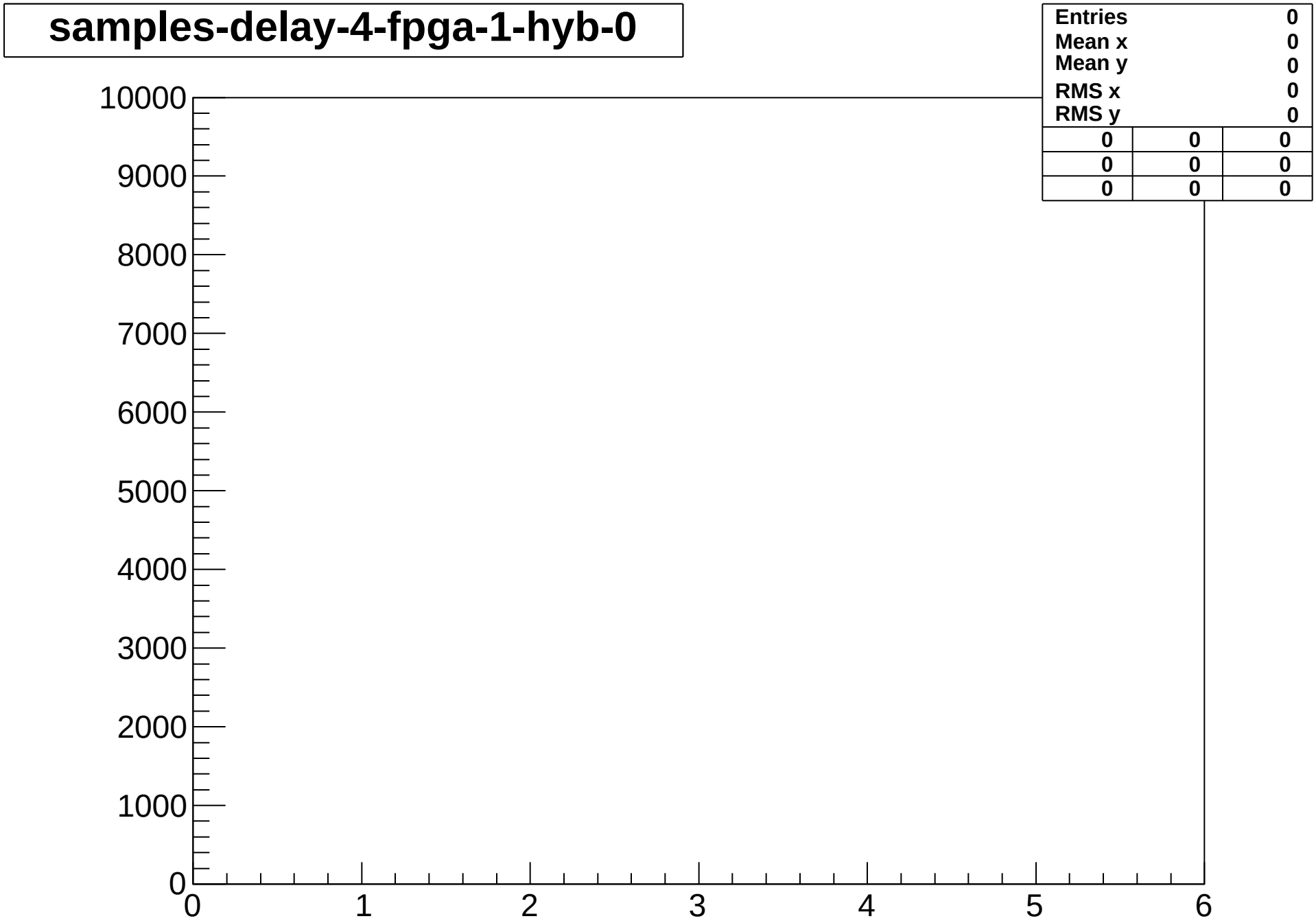

samples-delay-0-fpga-1-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6

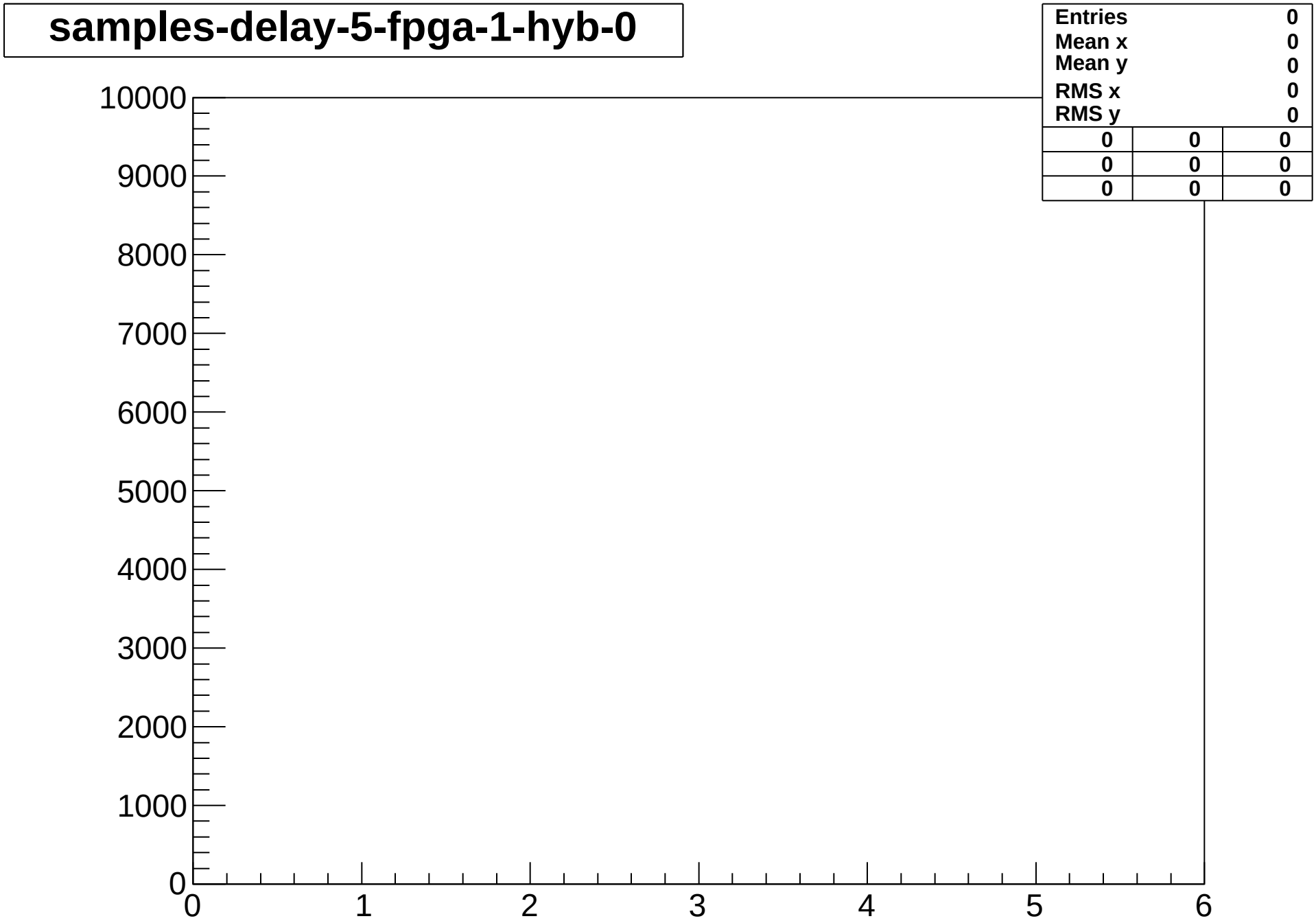

samples-delay-1-fpga-1-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6

samples-delay-2-fpga-1-hyb-0




samples-delay-3-fpga-1-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6


samples-delay-4-fpga-1-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6


samples-delay-5-fpga-1-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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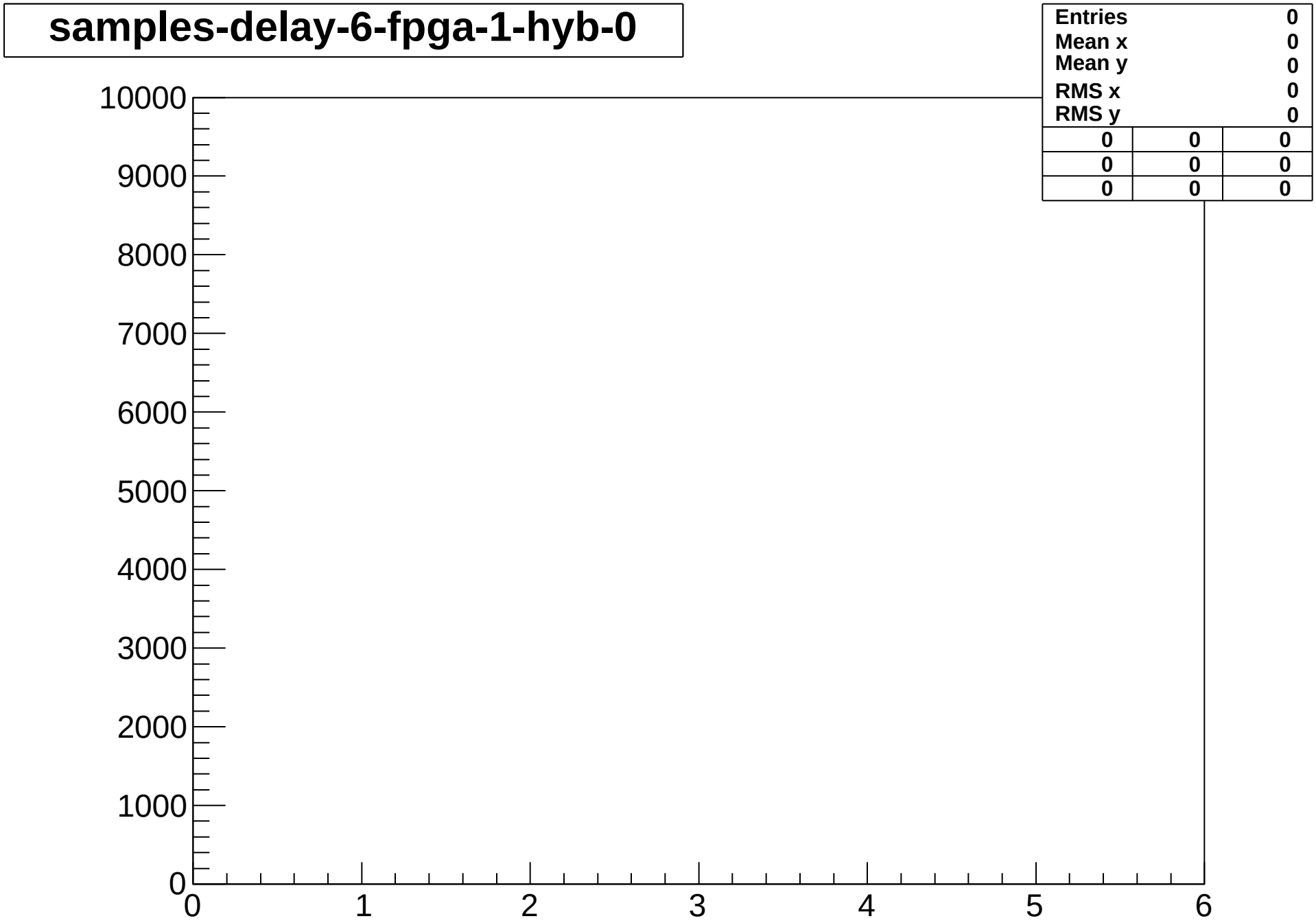
4
5
6


samples-delay-6-fpga-1-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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4
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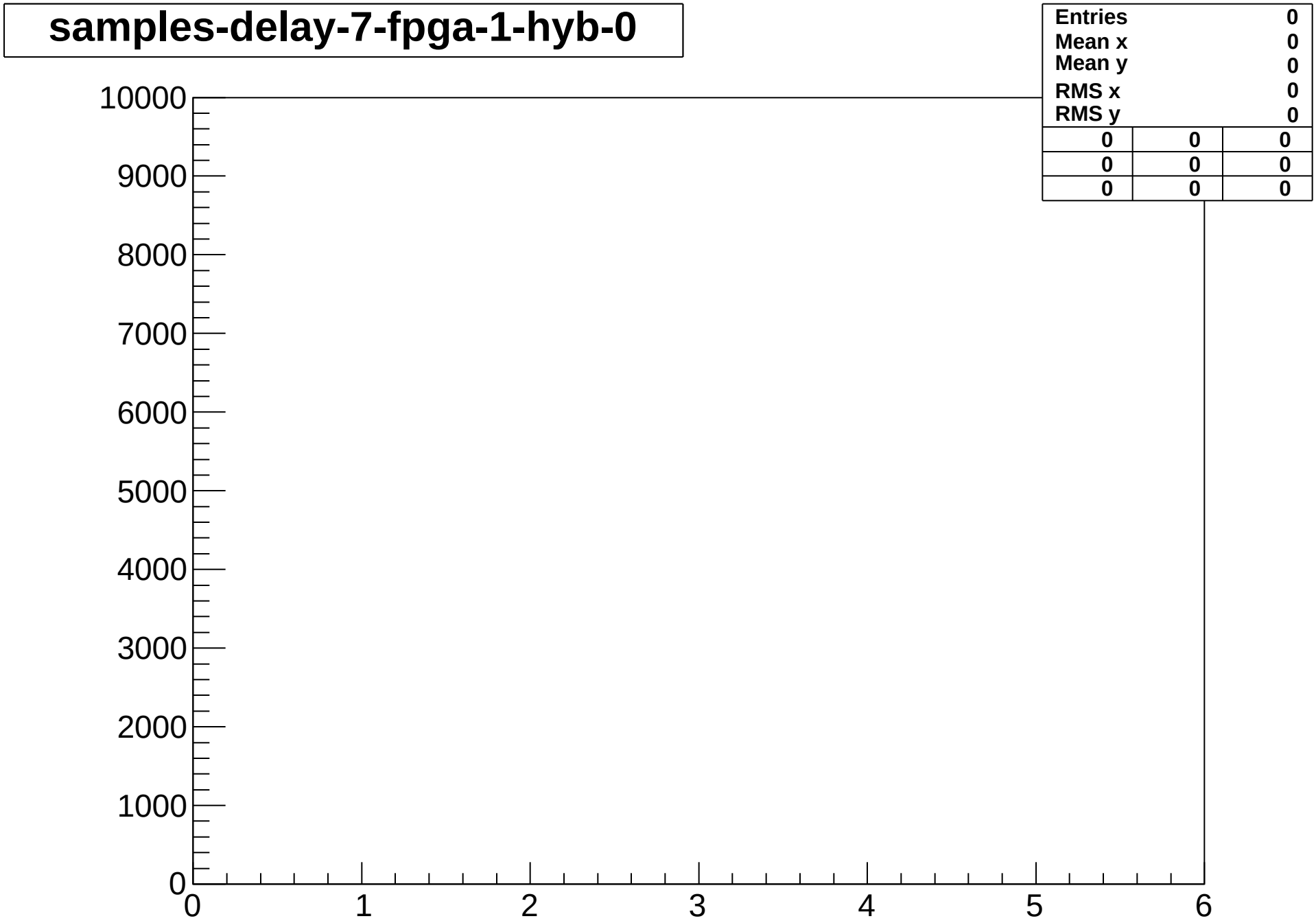
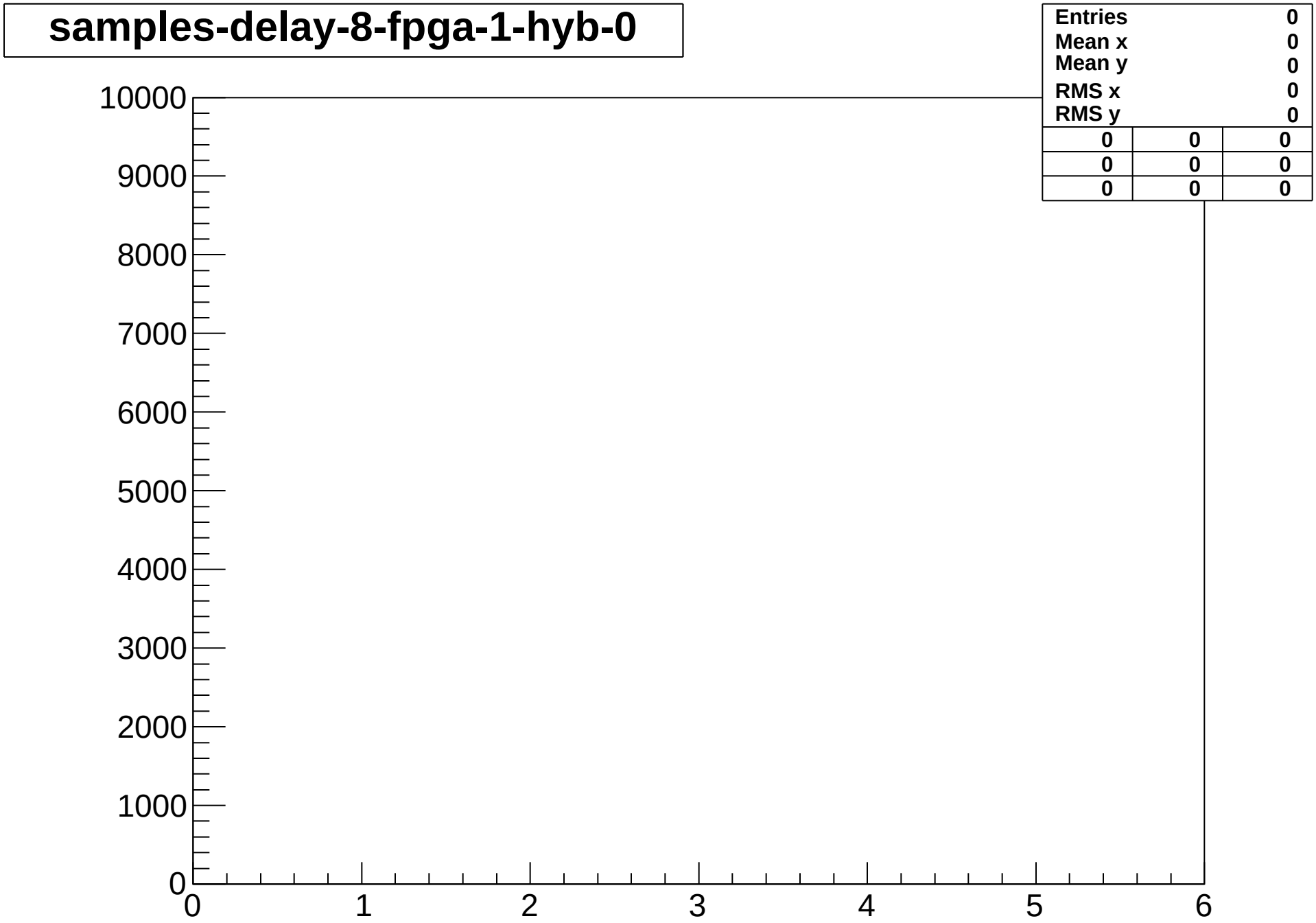
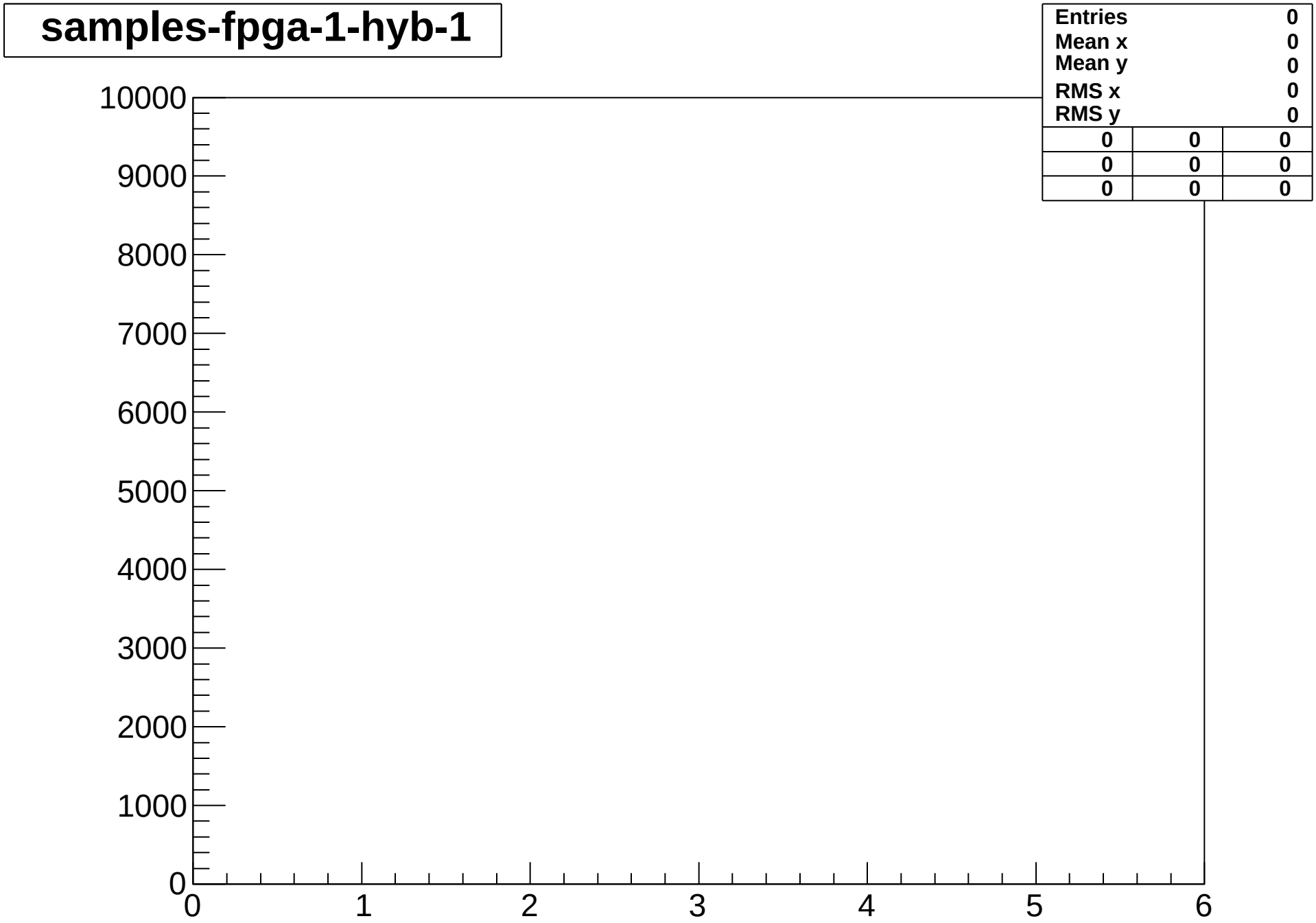
6


samples-delay-7-fpga-1-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6


samples-delay-8-fpga-1-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6


samples-fpga-1-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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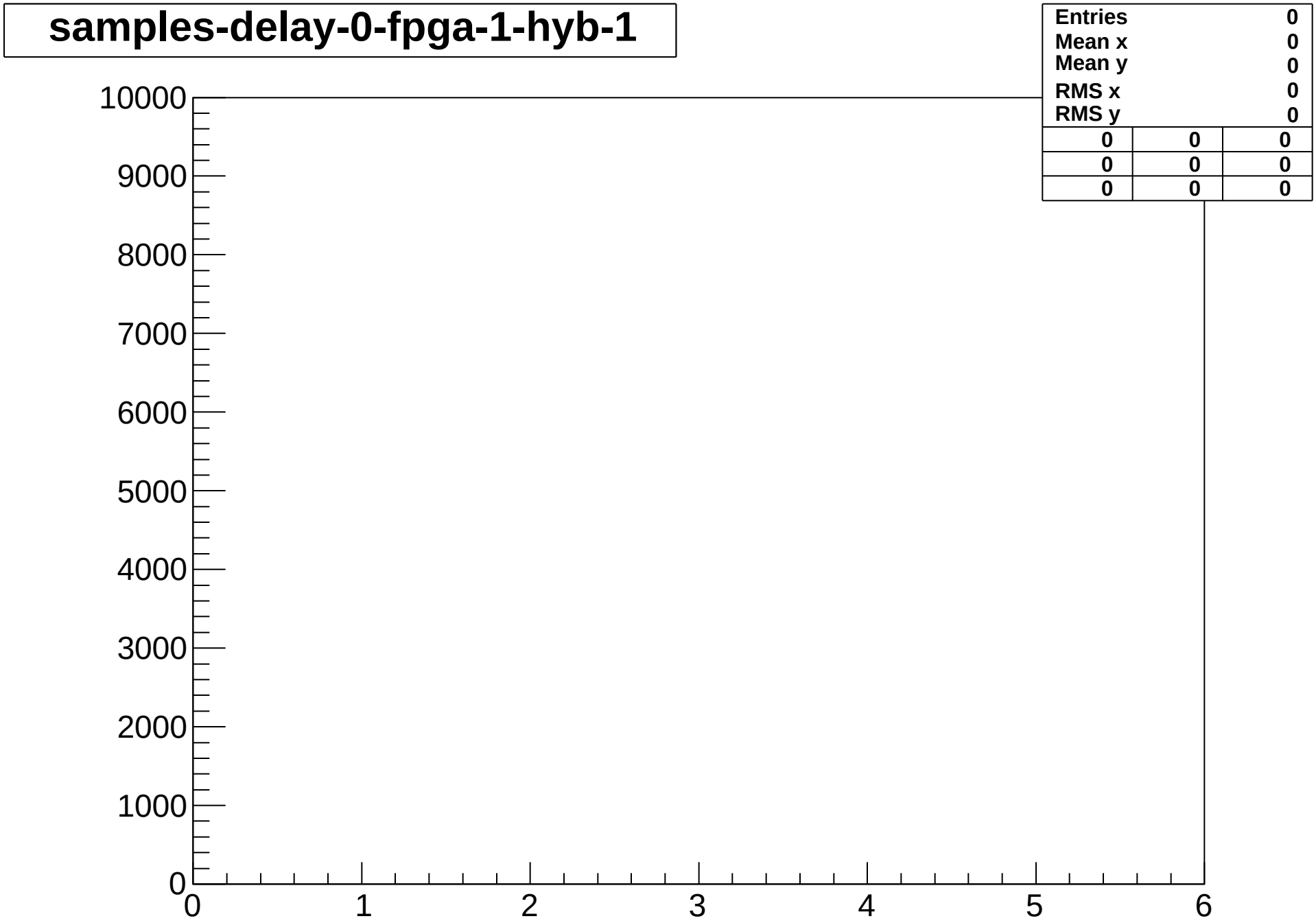
4
5
6


samples-delay-0-fpga-1-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
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1
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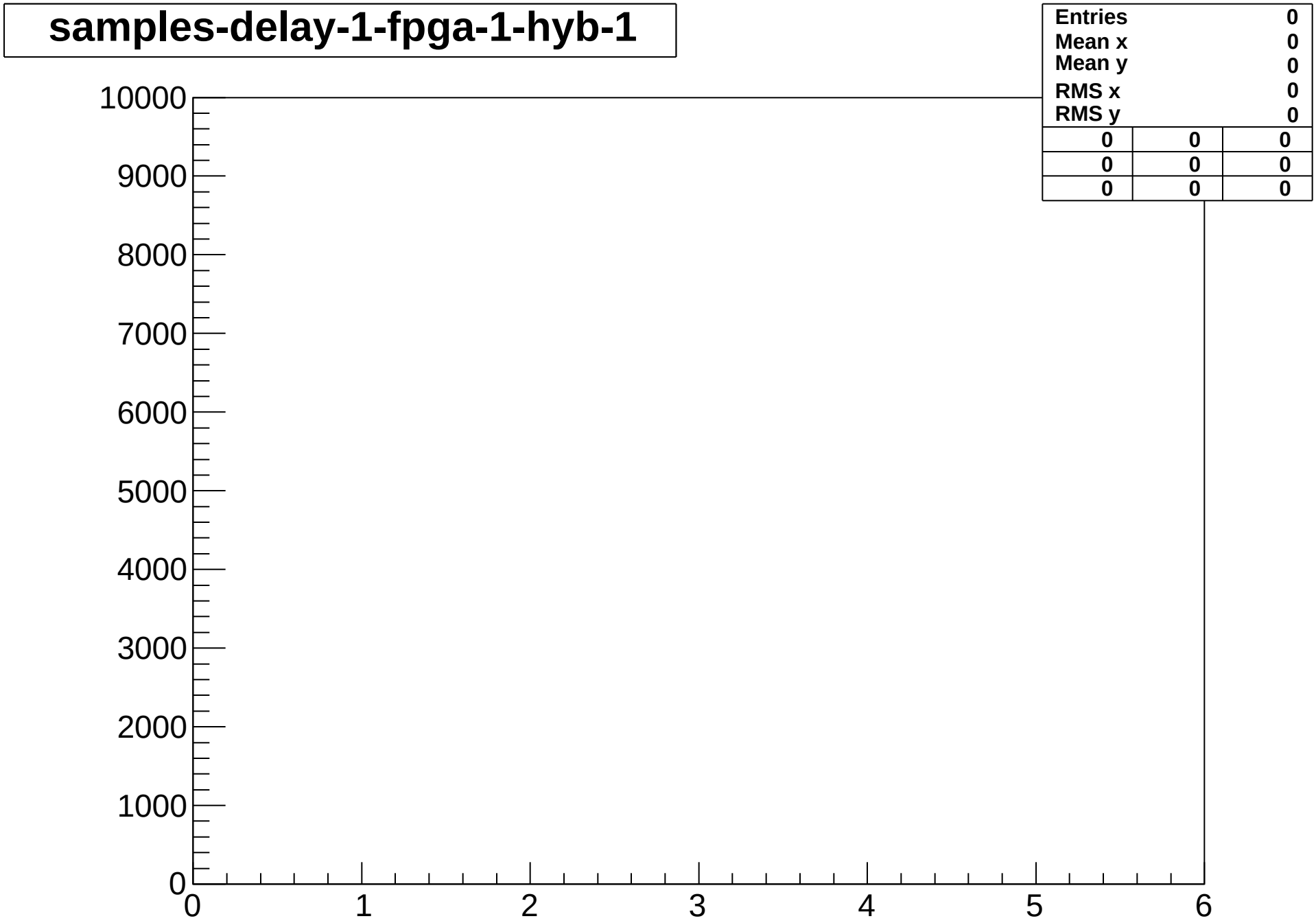
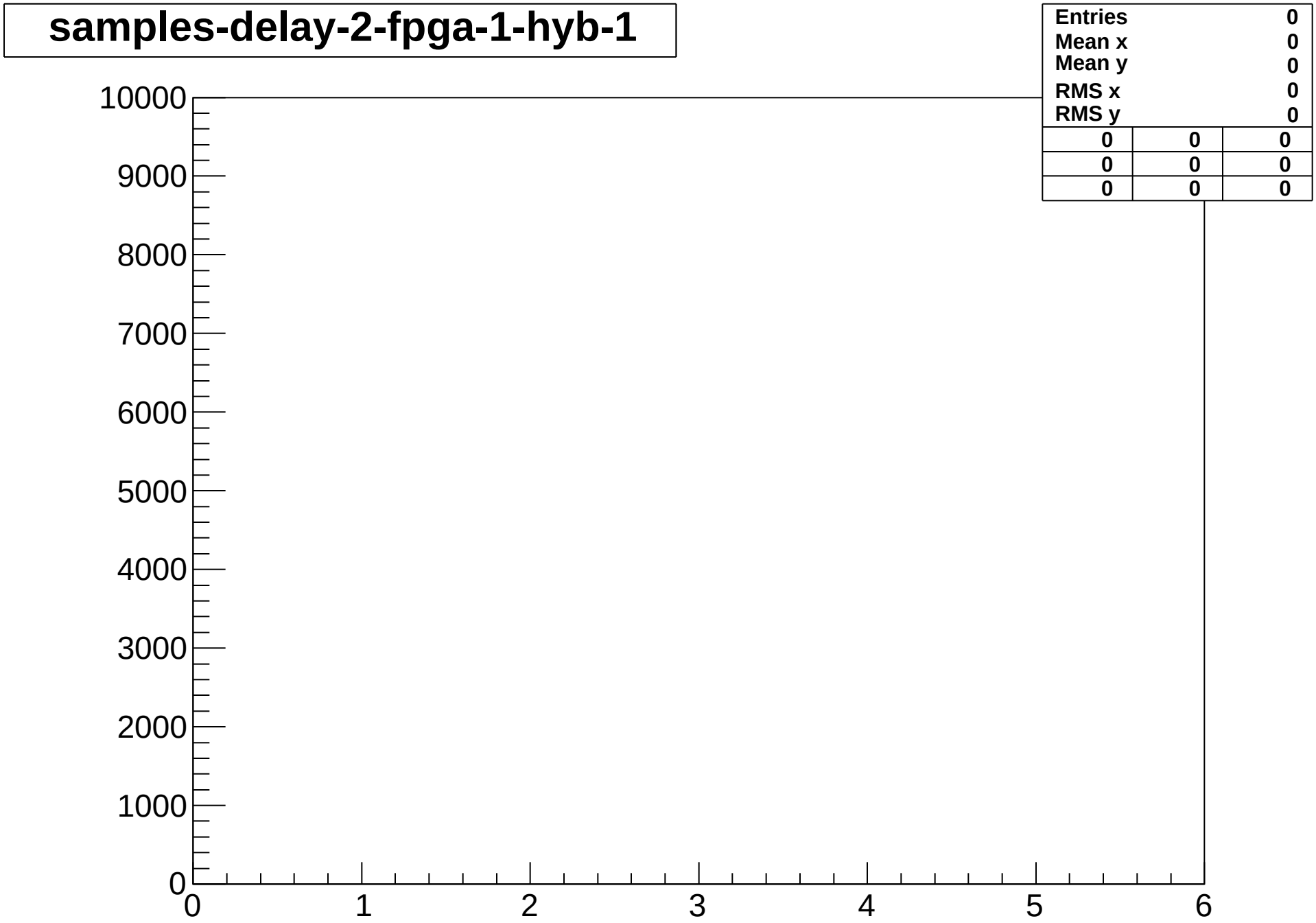
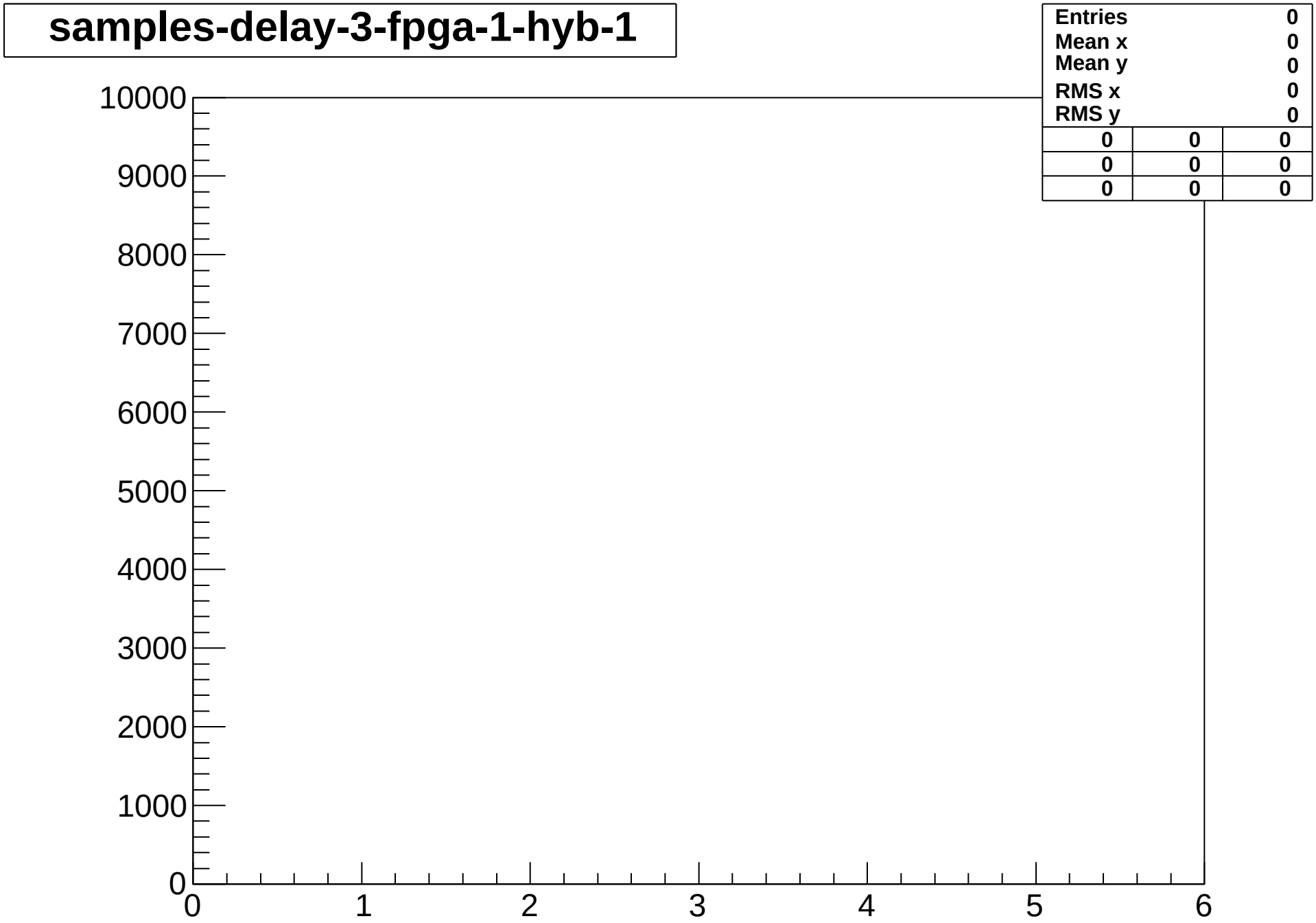
samples-delay-1-fpga-1-hyb-1

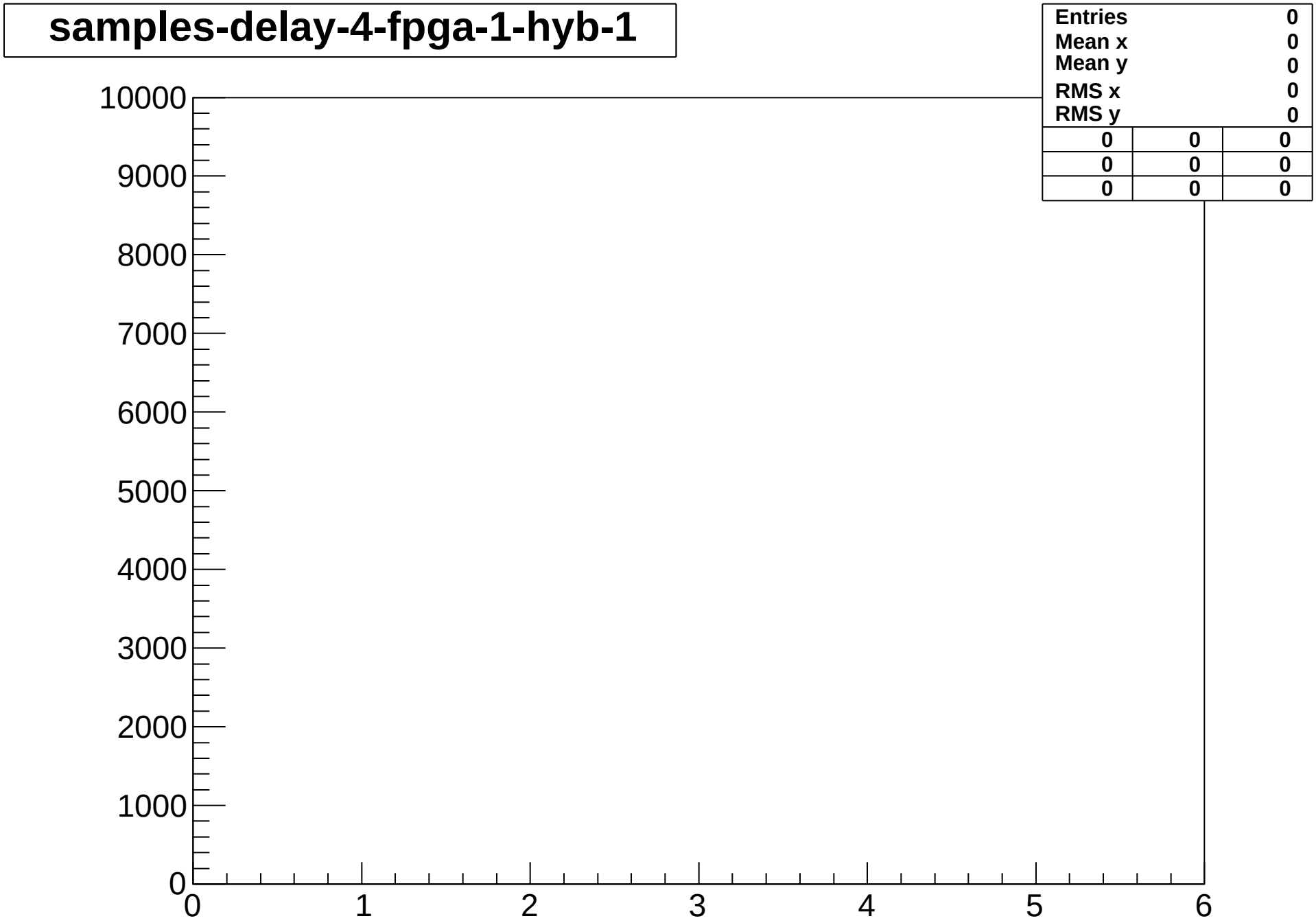



samples-delay-2-fpga-1-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6

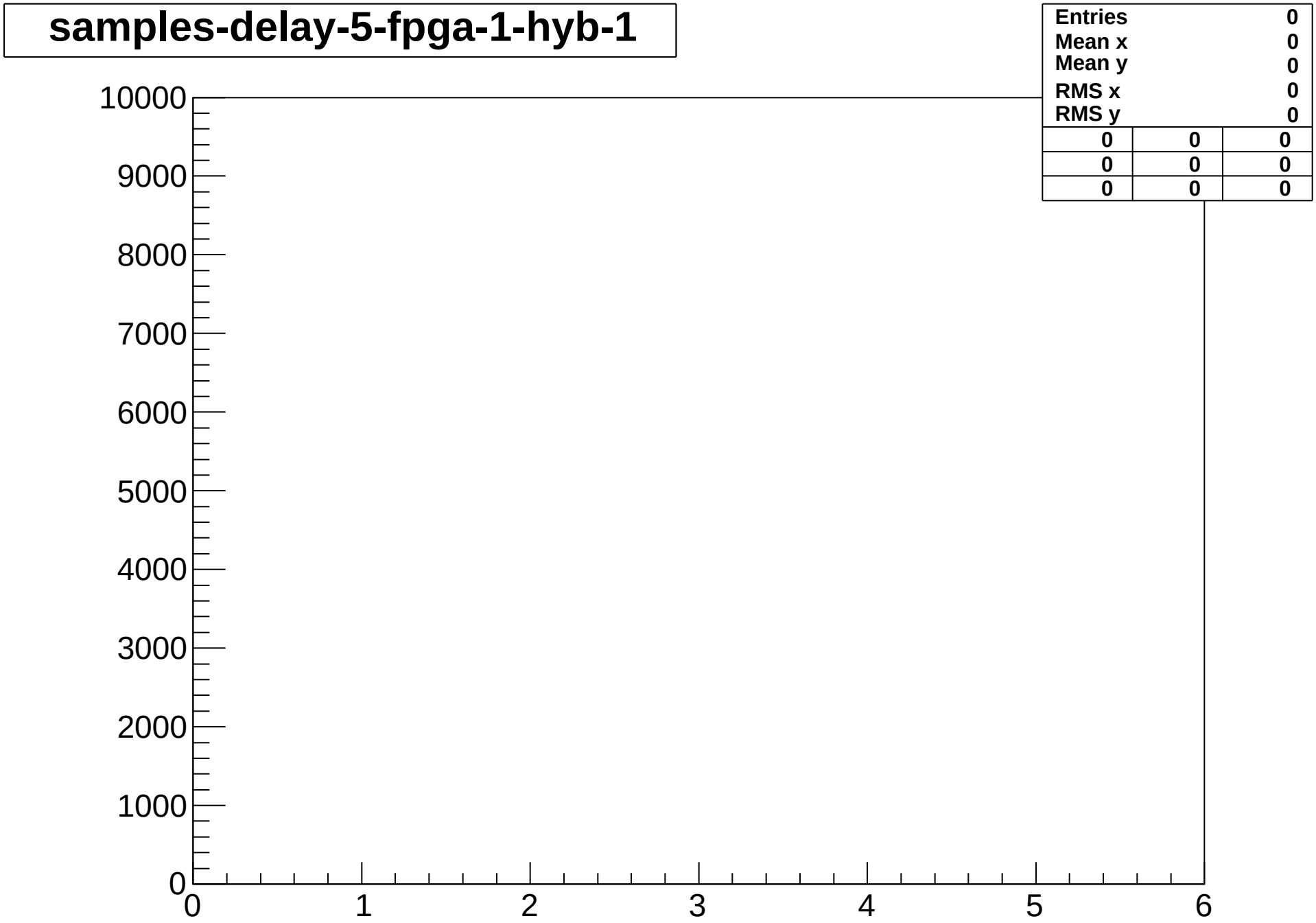
samples-delay-3-fpga-1-hyb-1



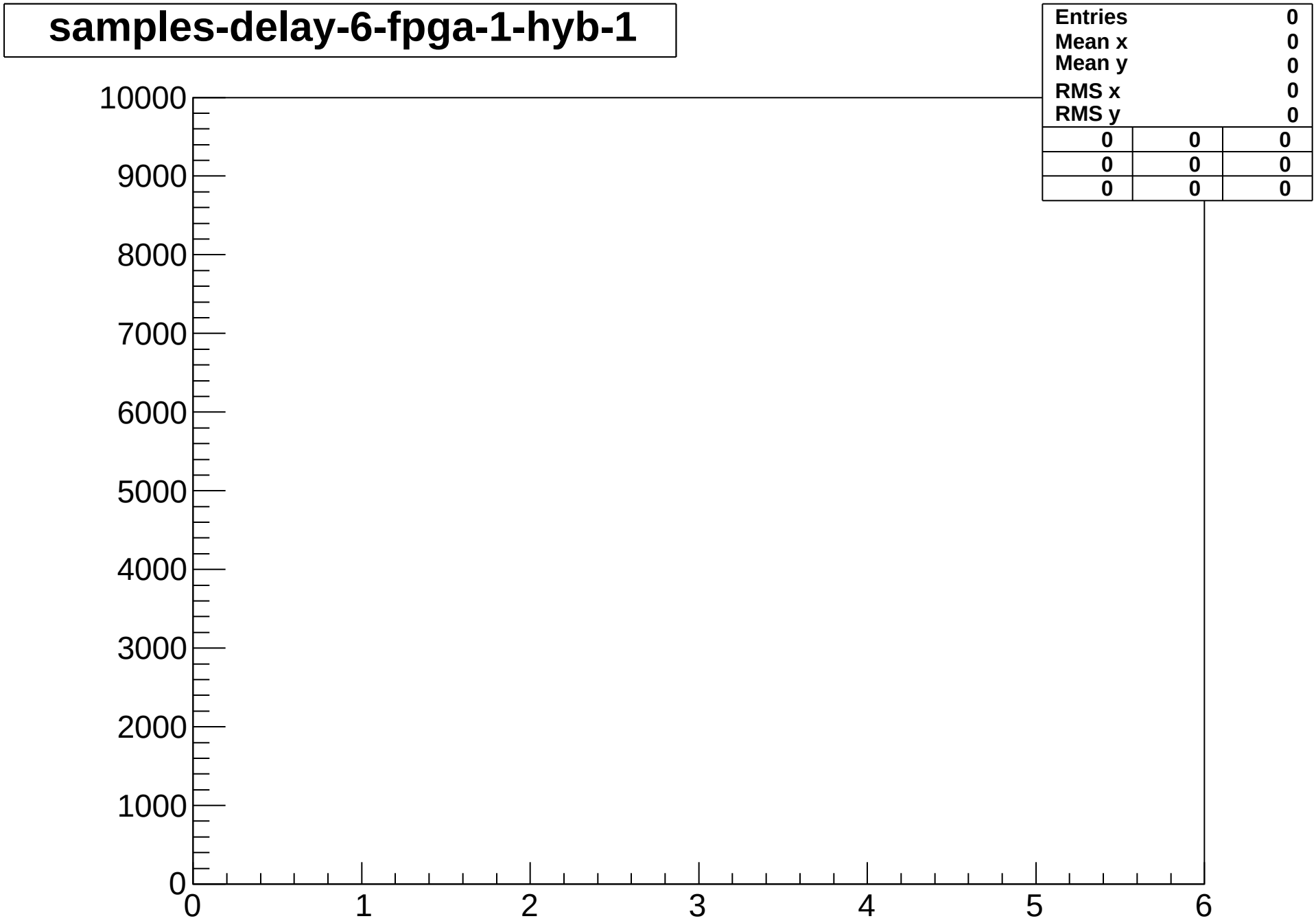
samples-delay-4-fpga-1-hyb-1



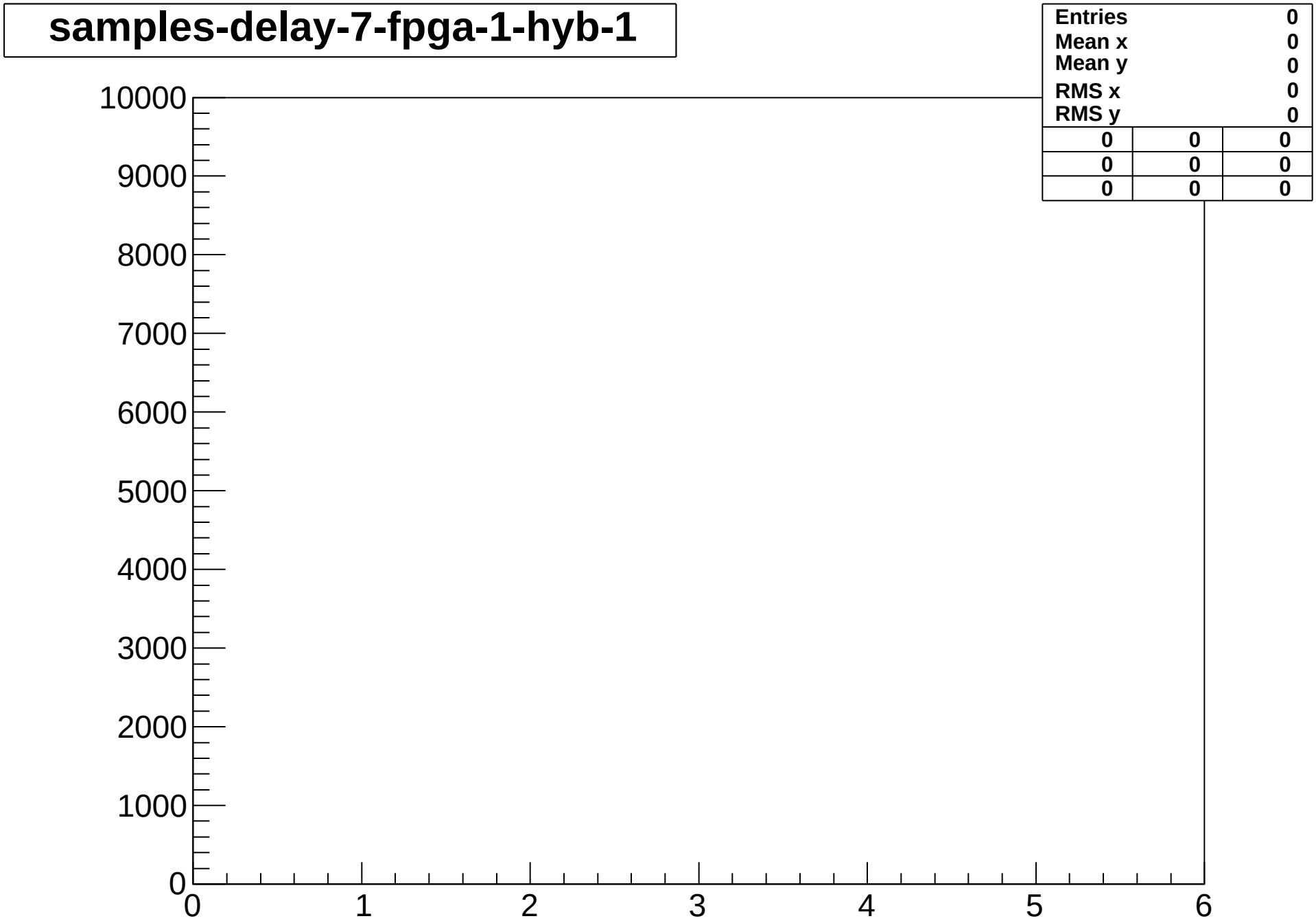
samples-delay-5-fpga-1-hyb-1



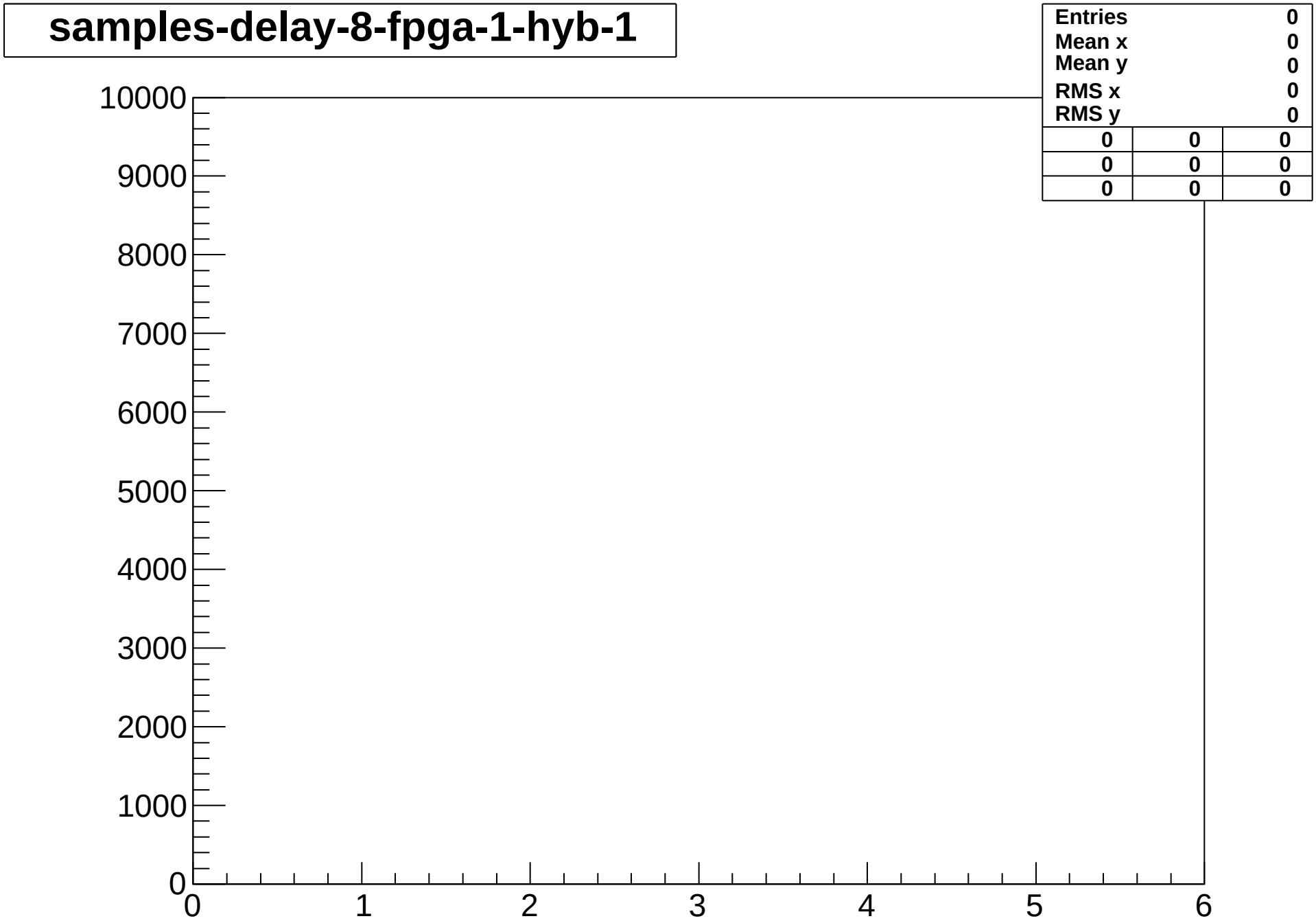
samples-delay-6-fpga-1-hyb-1

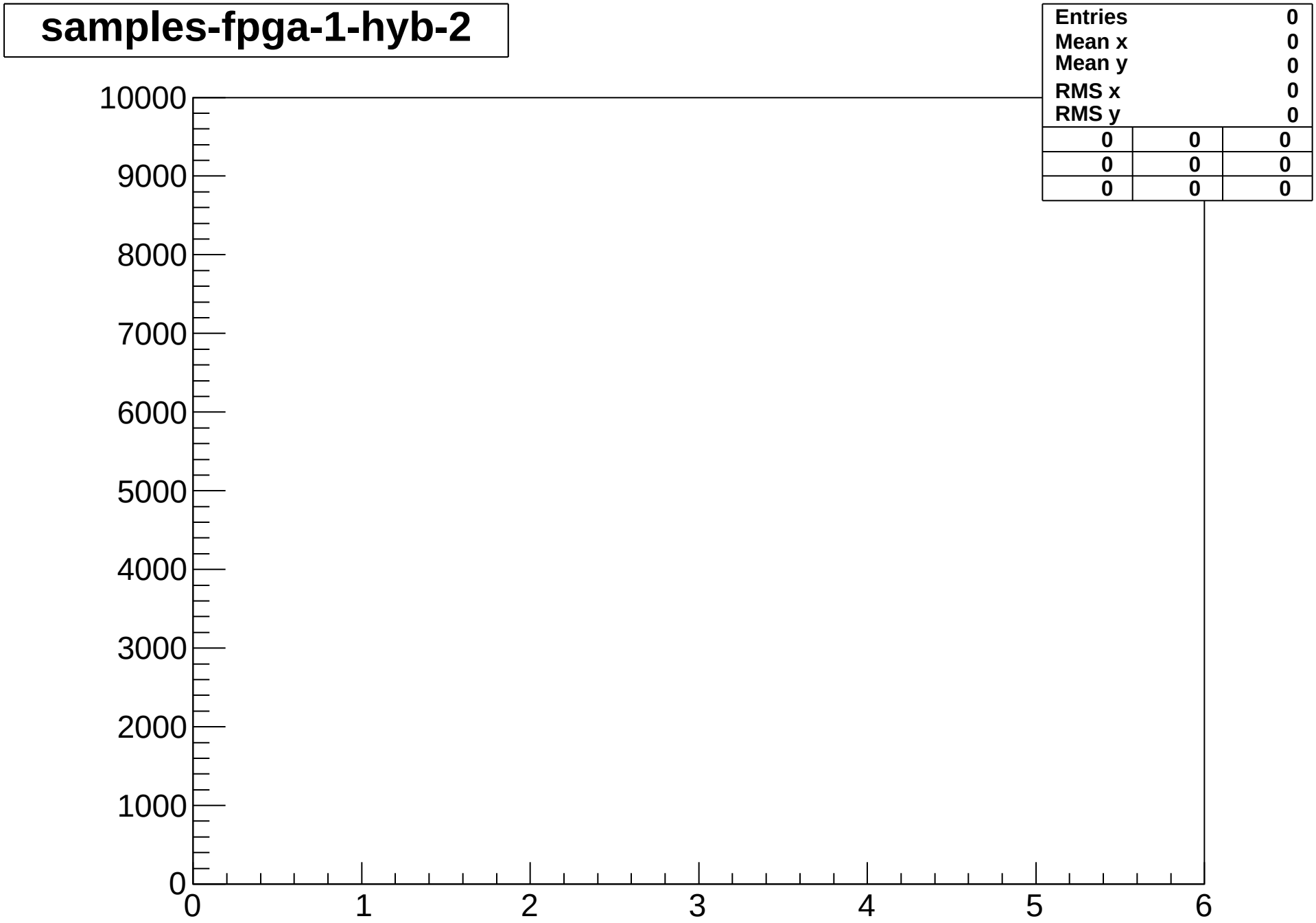


samples-delay-7-fpga-1-hyb-1



samples-delay-8-fpga-1-hyb-1




samples-fpga-1-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
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0
1
2
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4
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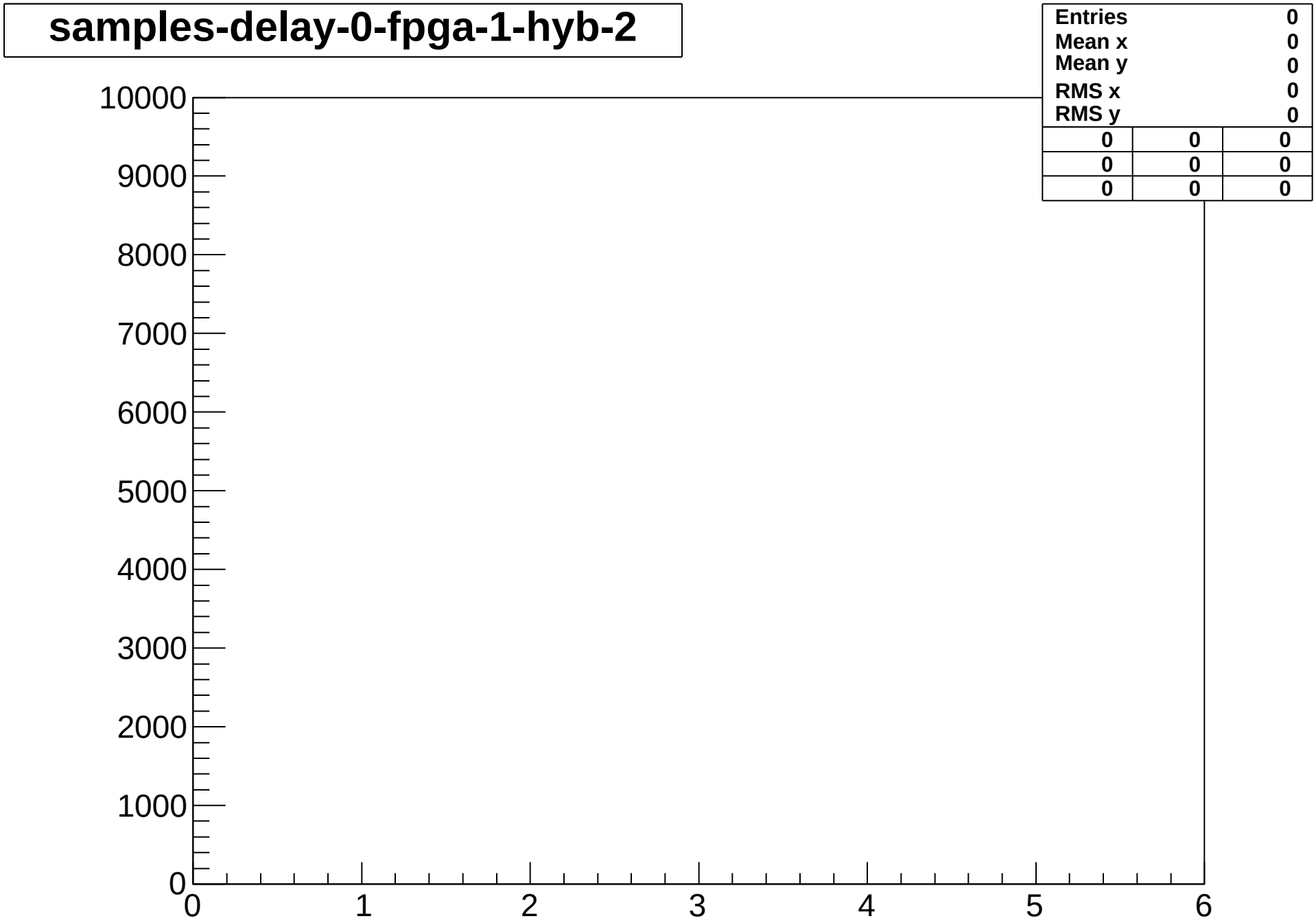
6


samples-delay-0-fpga-1-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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6000
5000
4000
3000
2000
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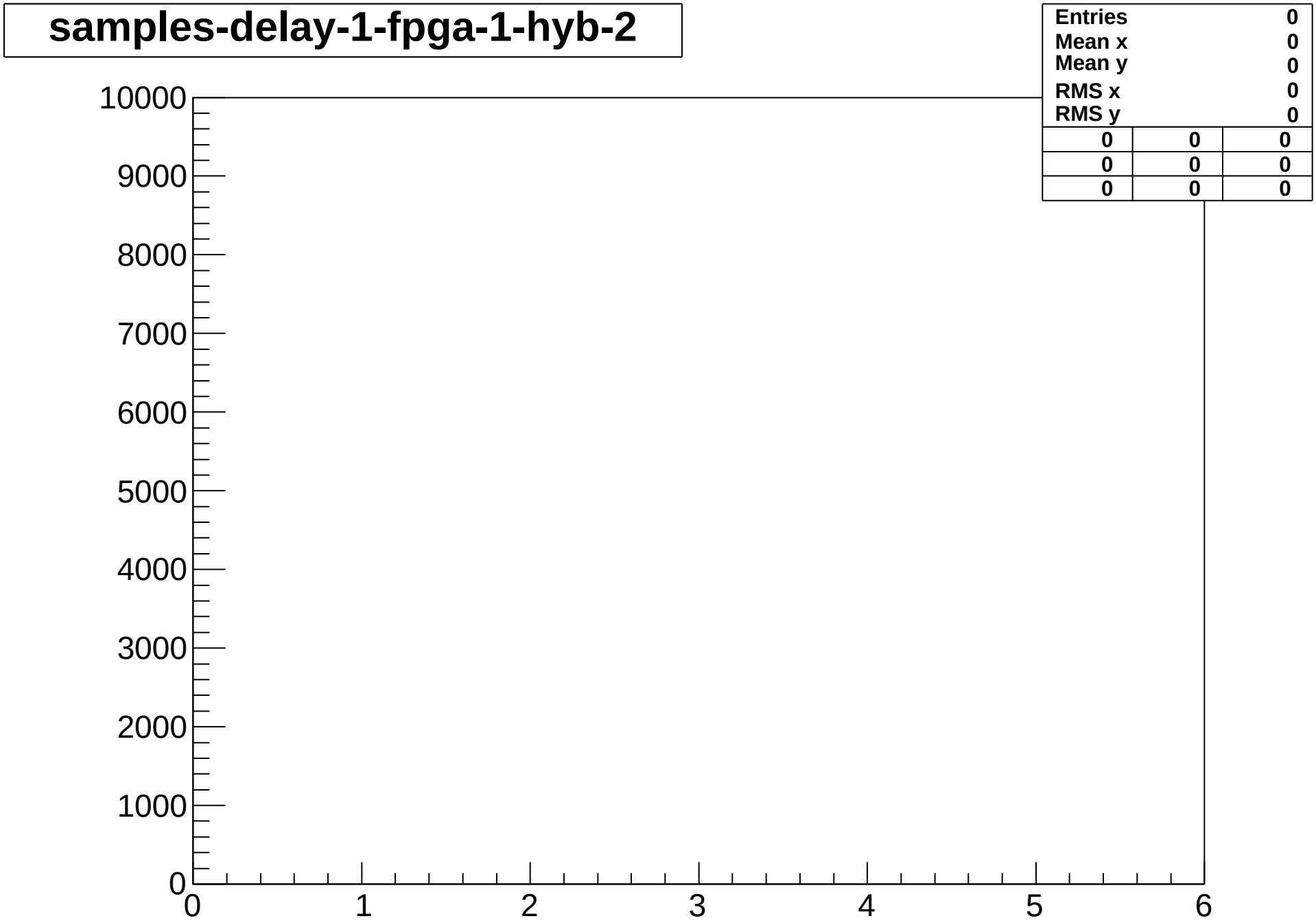
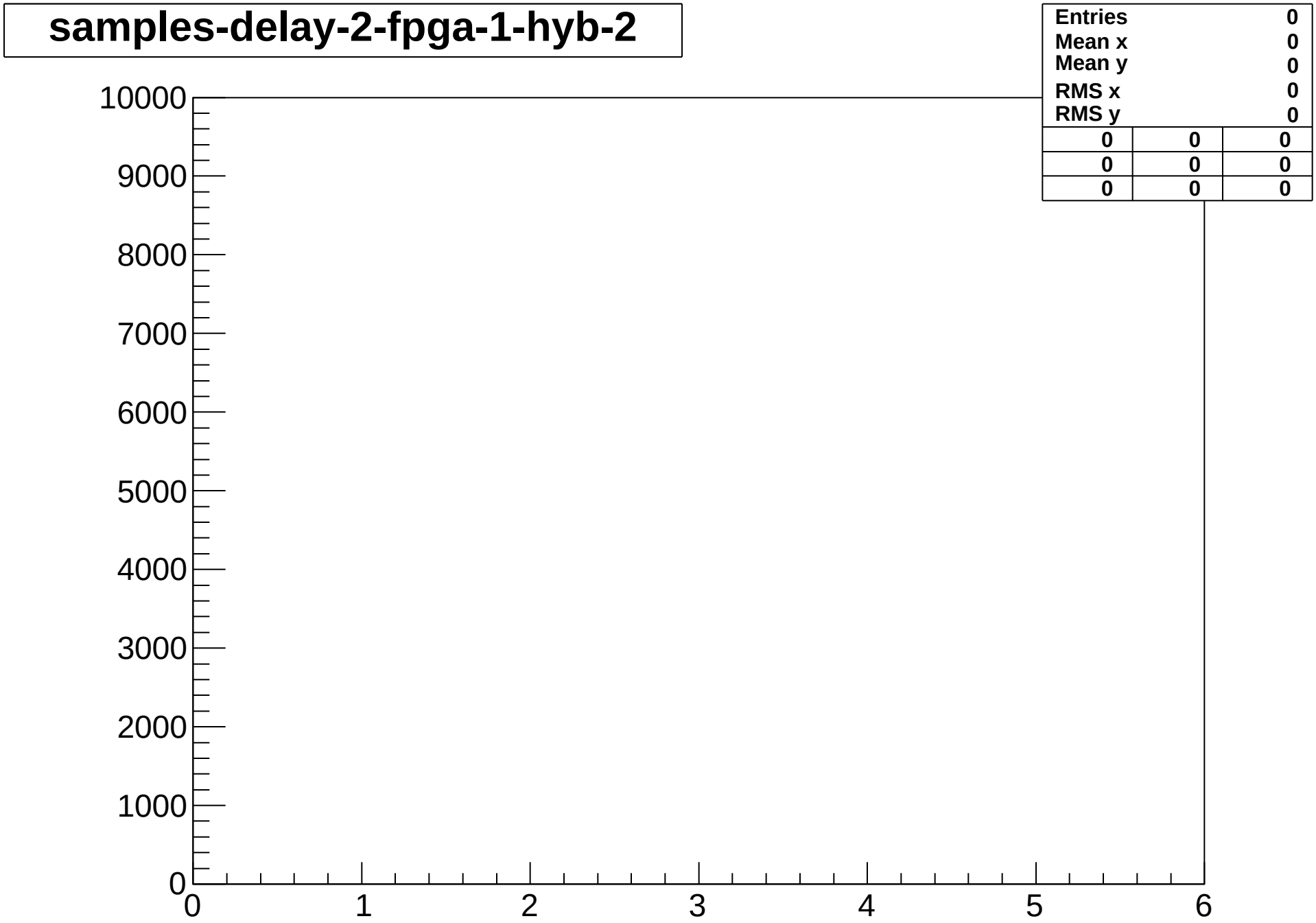
samples-delay-1-fpga-1-hyb-2




samples-delay-2-fpga-1-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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6000
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4000
3000
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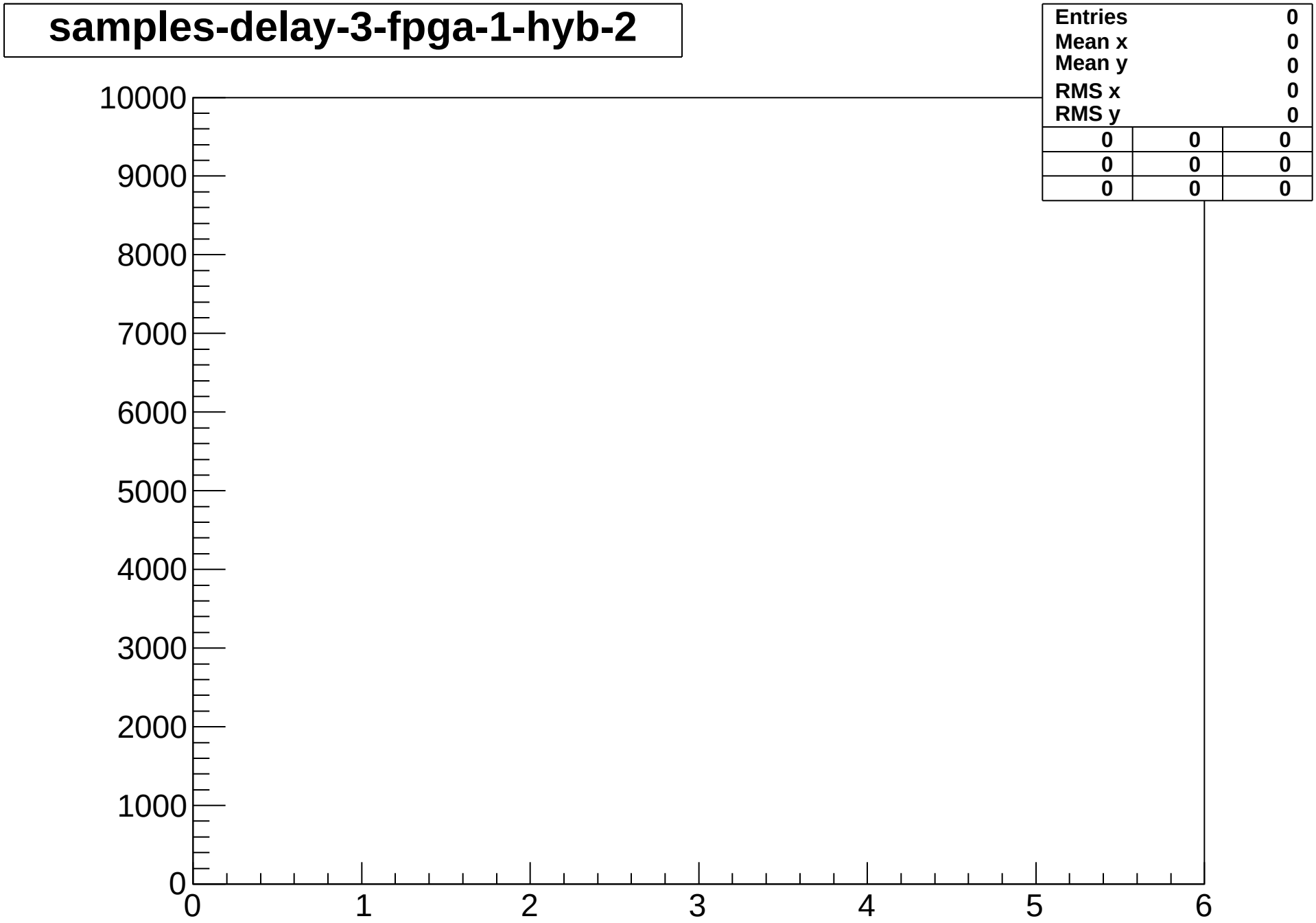
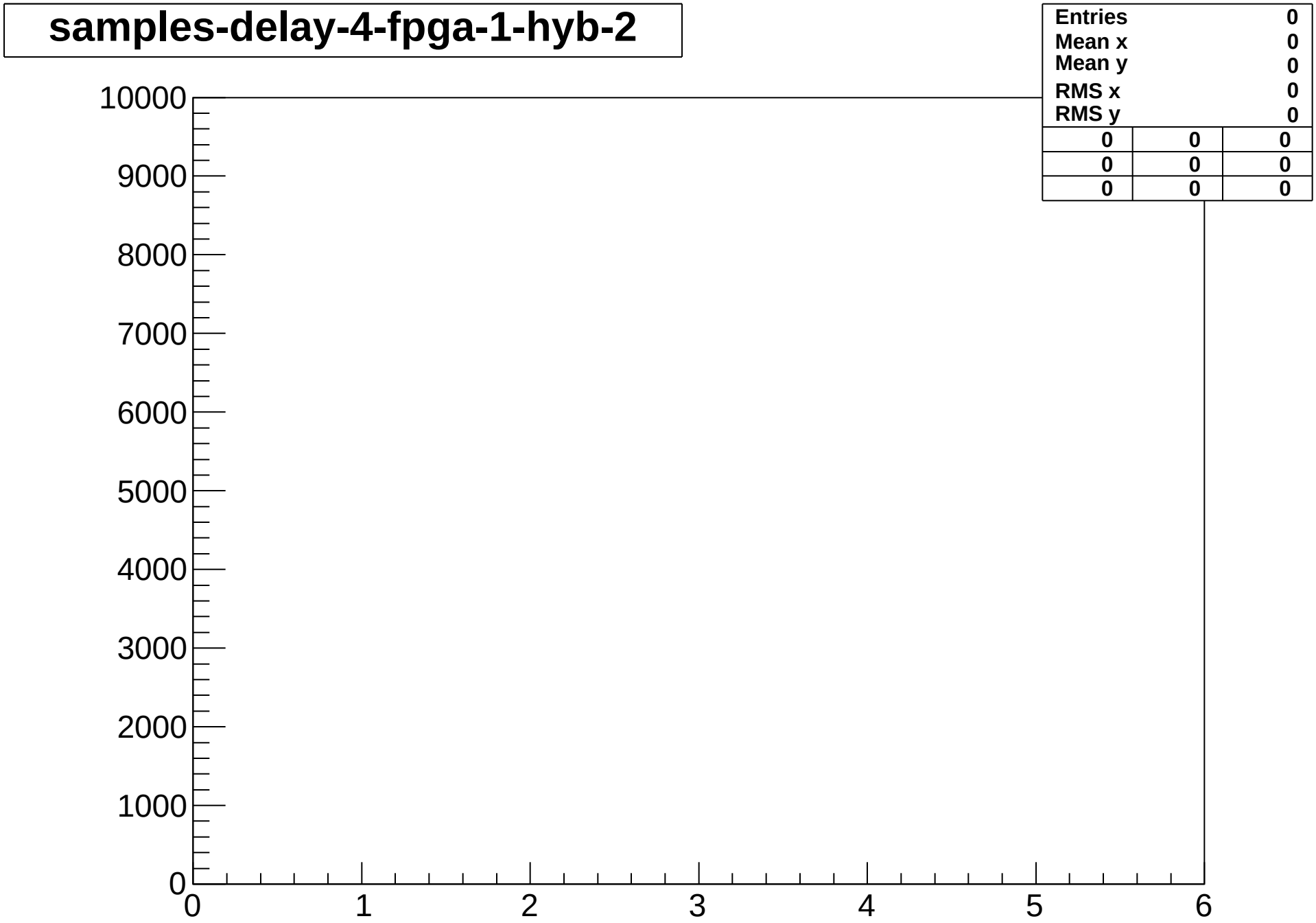
samples-delay-3-fpga-1-hyb-2




samples-delay-4-fpga-1-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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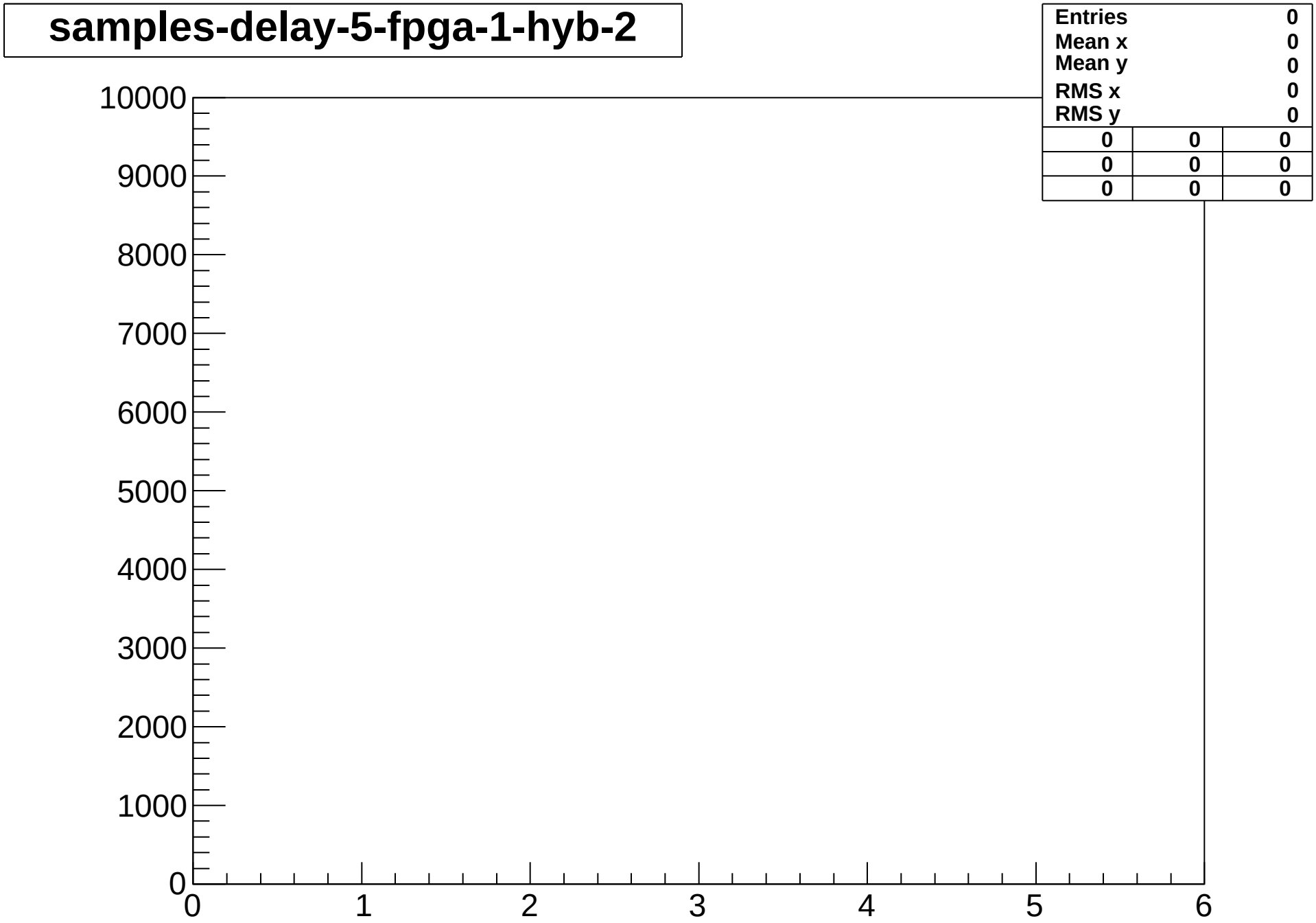
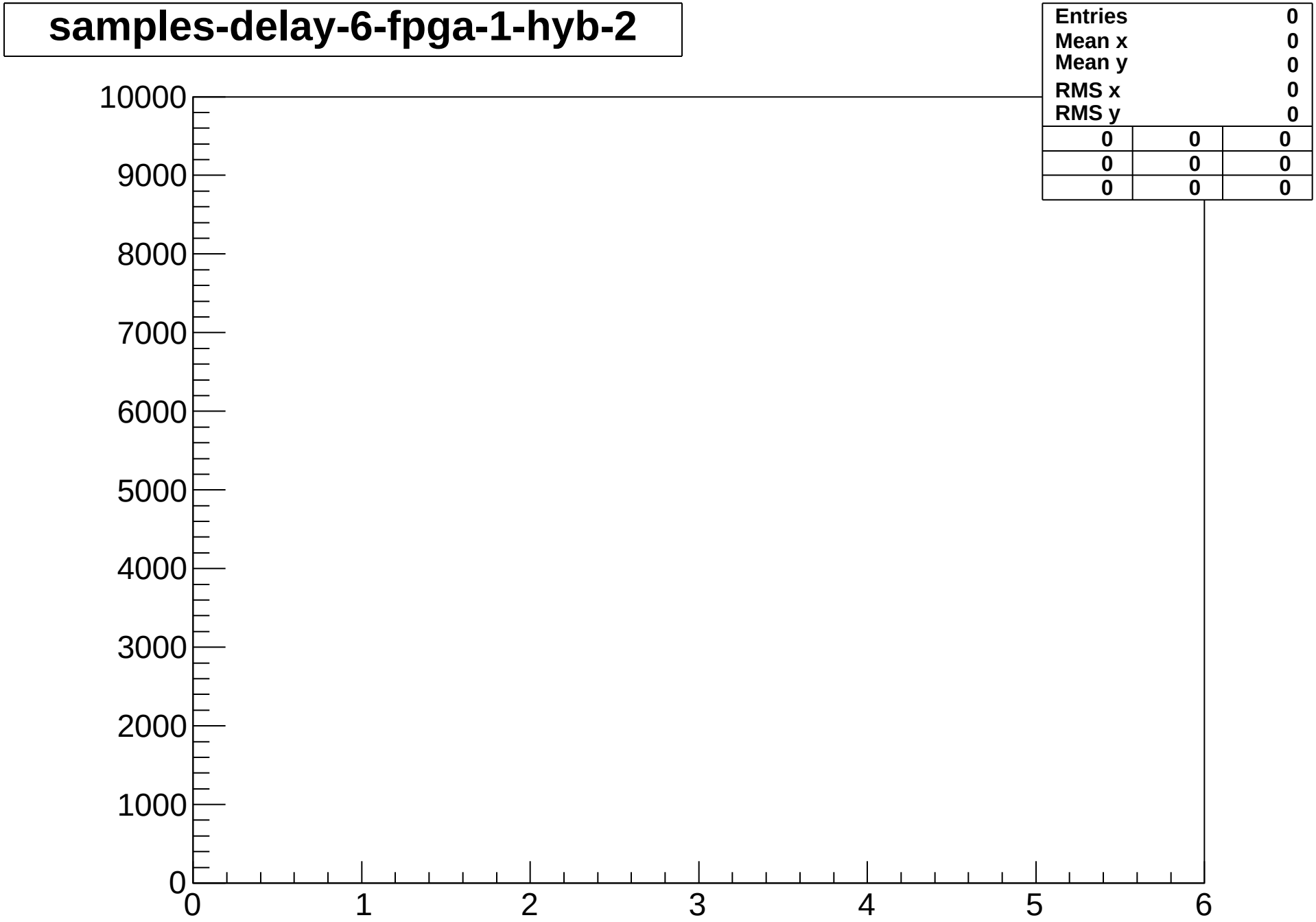
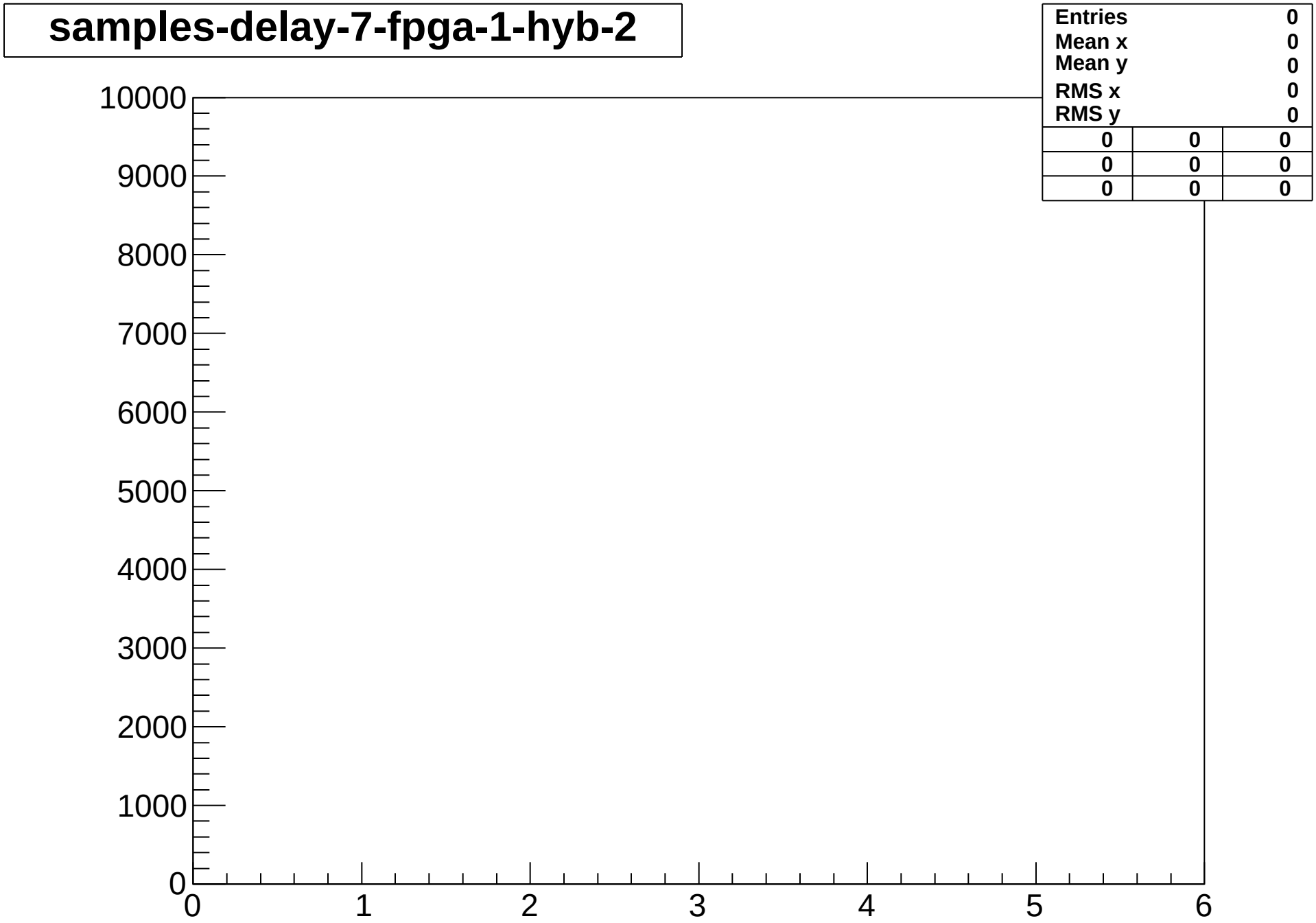
samples-delay-5-fpga-1-hyb-2



samples-delay-6-fpga-1-hyb-2




samples-delay-7-fpga-1-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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4000
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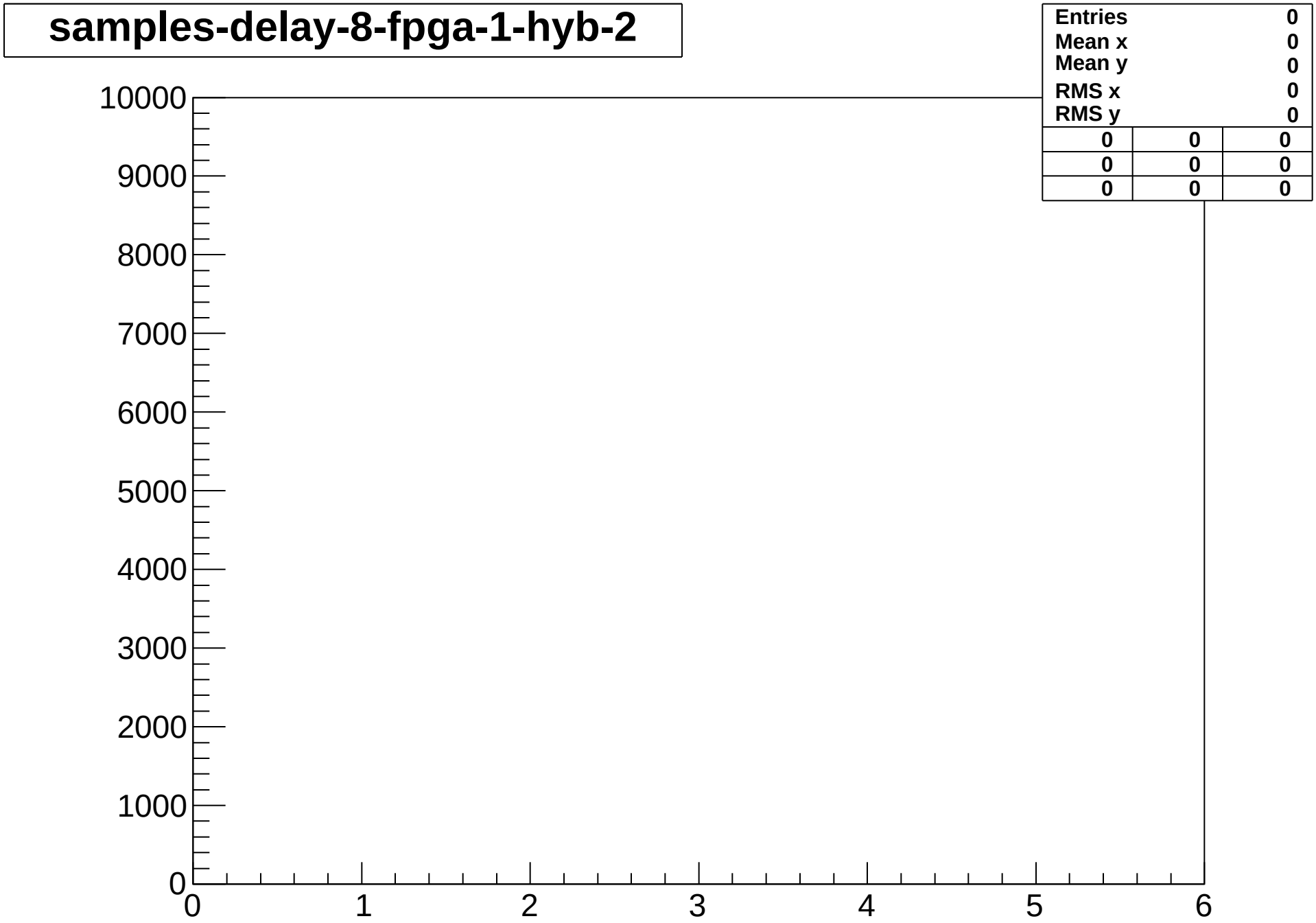
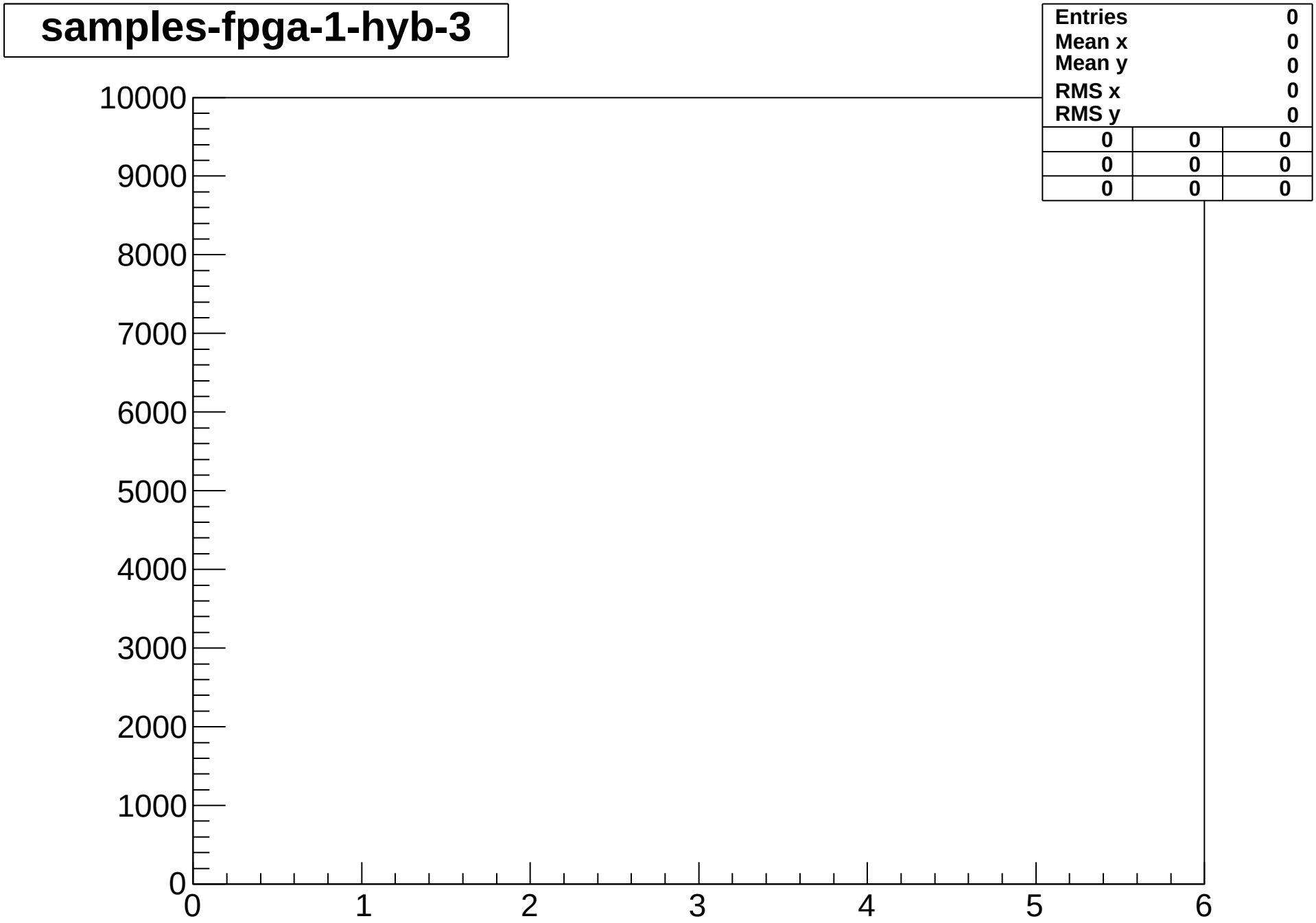
samples-delay-8-fpga-1-hyb-2




samples-fpga-1-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
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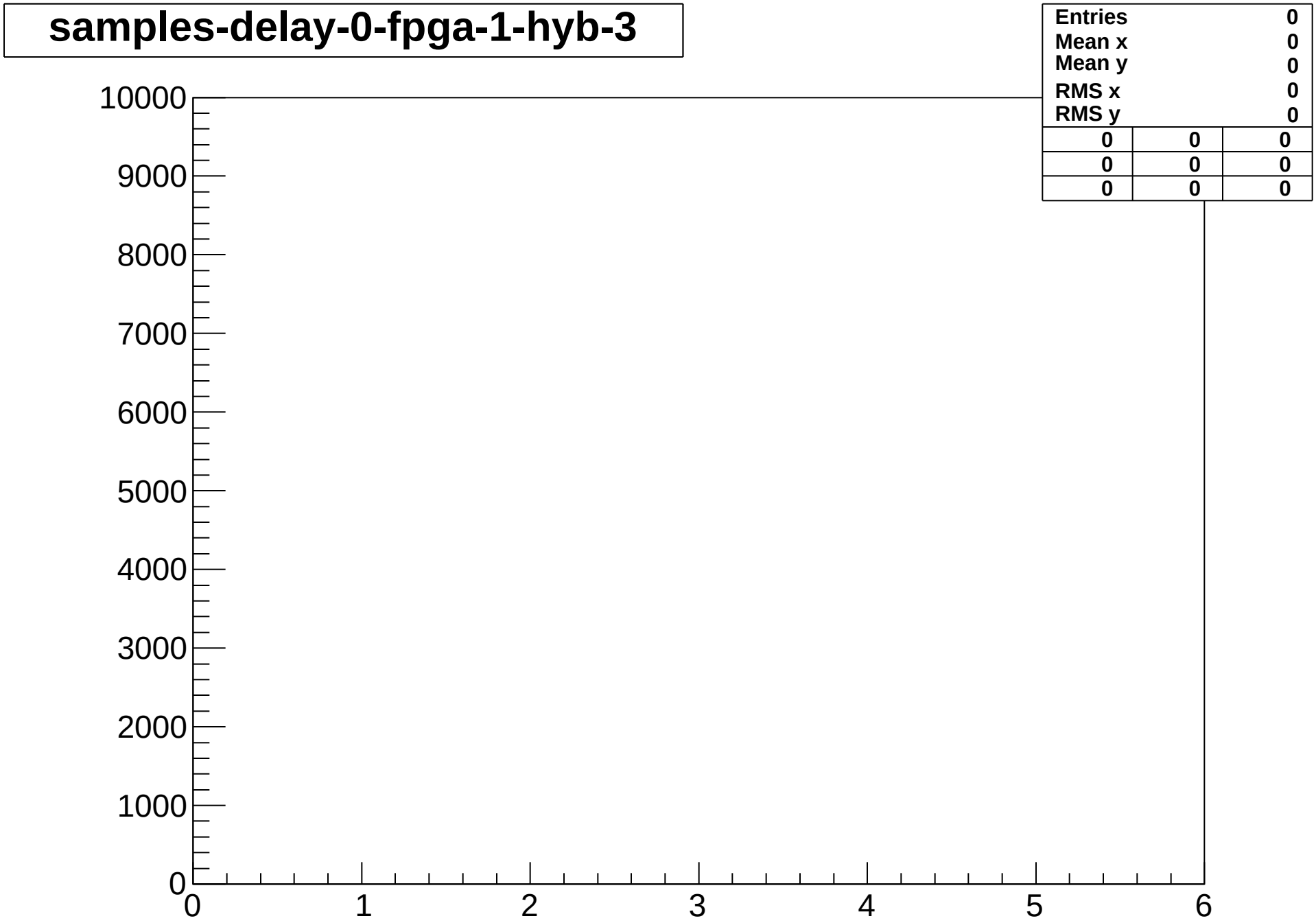
samples-delay-0-fpga-1-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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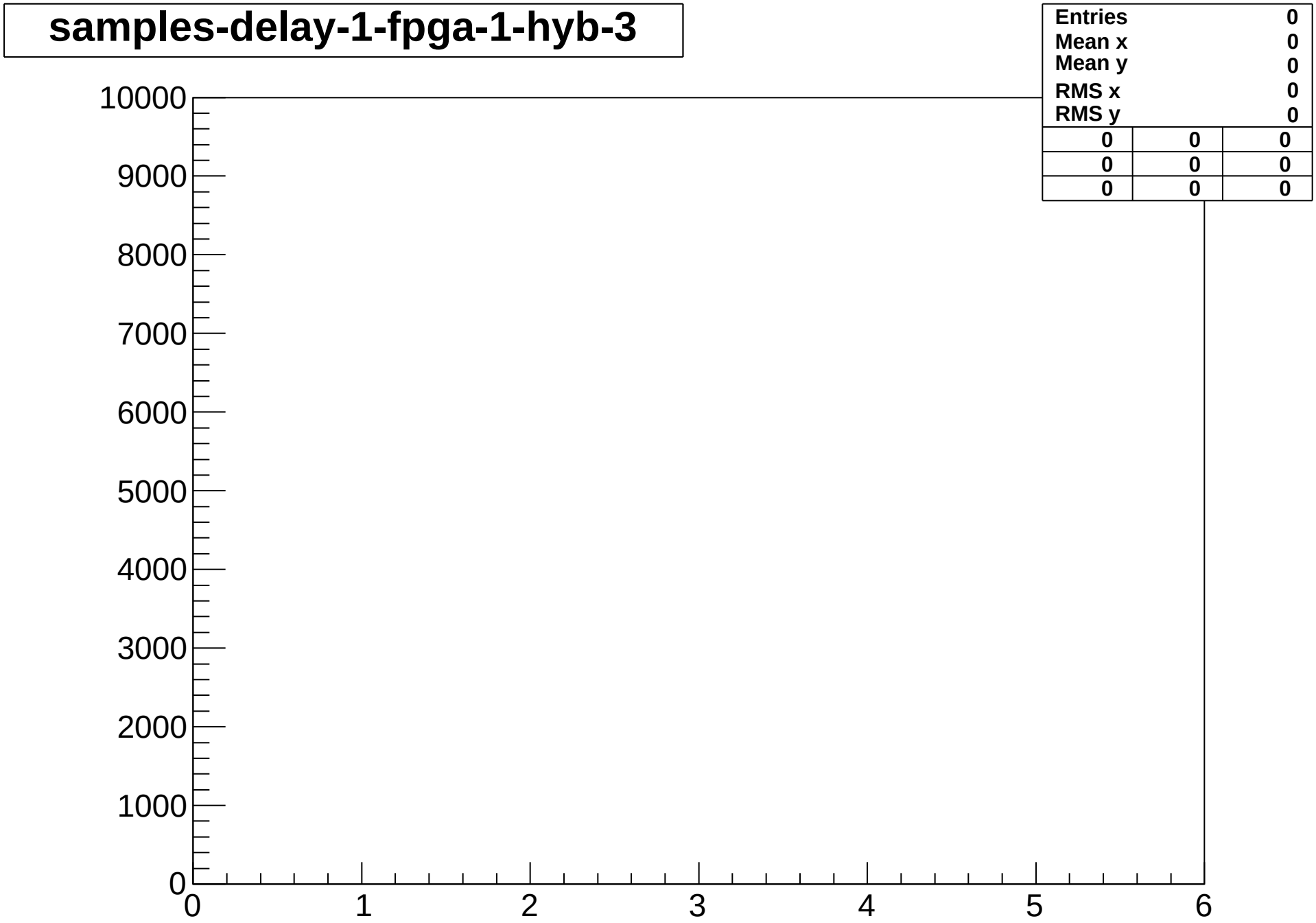
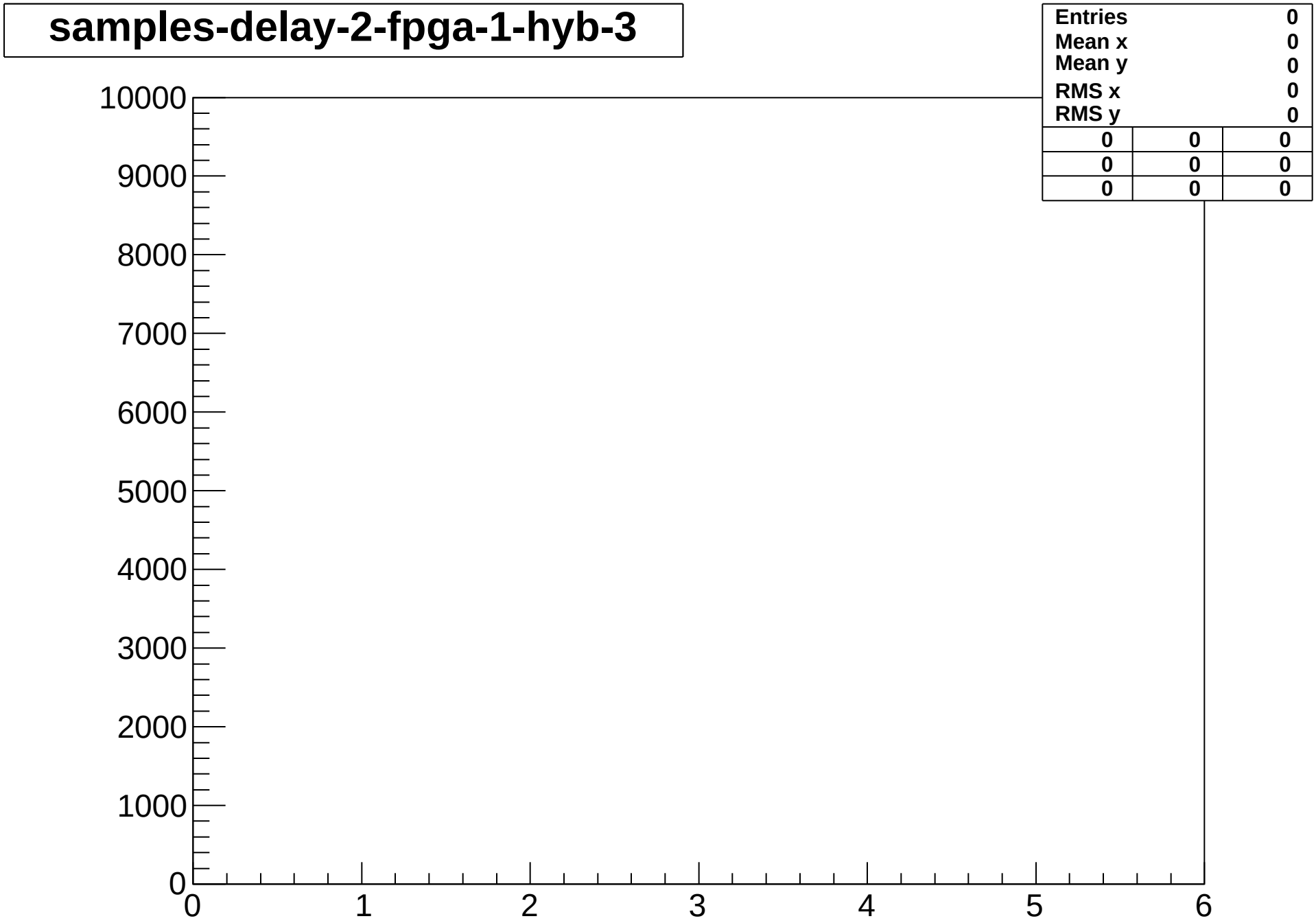
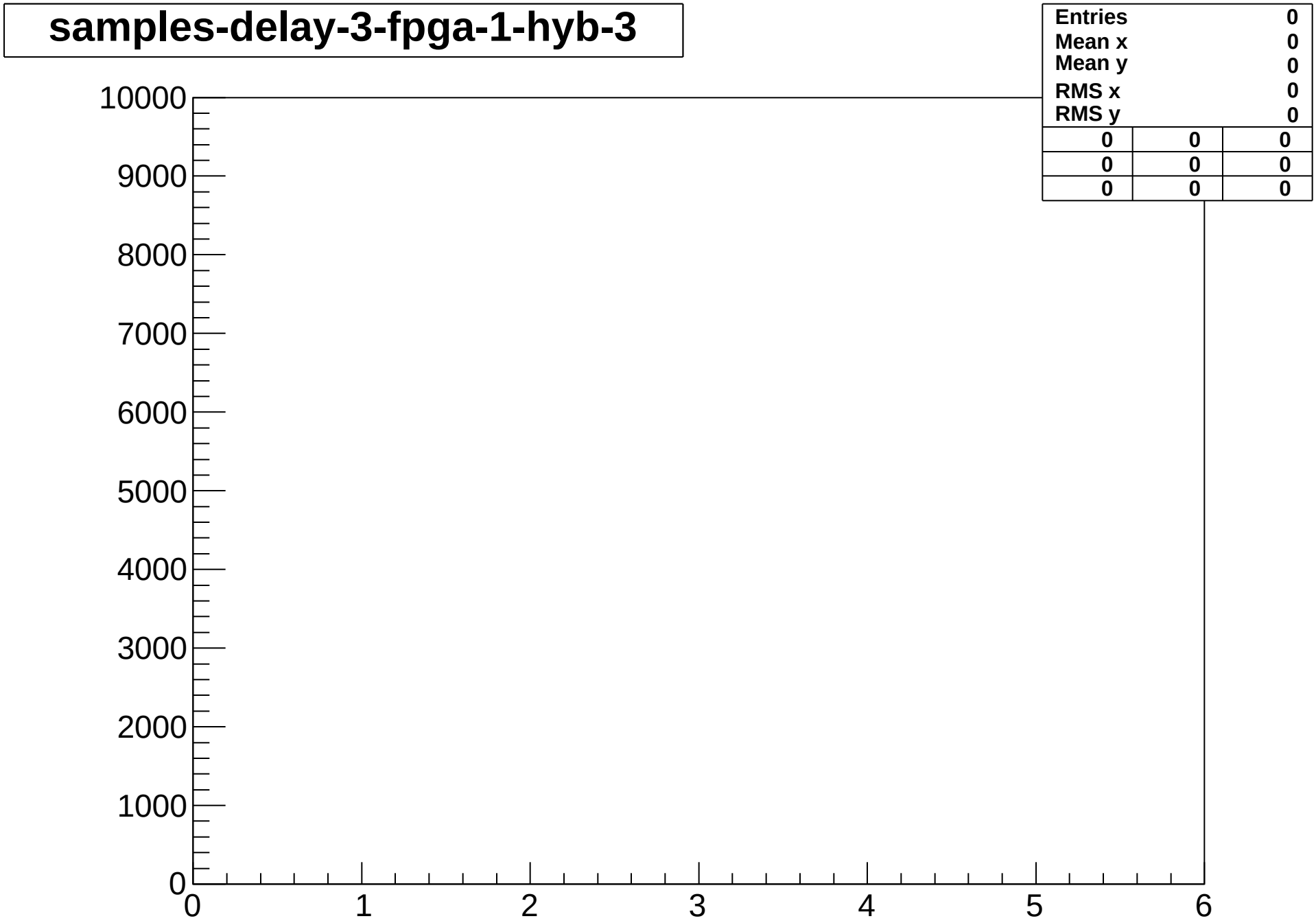
samples-delay-1-fpga-1-hyb-3



samples-delay-2-fpga-1-hyb-3




samples-delay-3-fpga-1-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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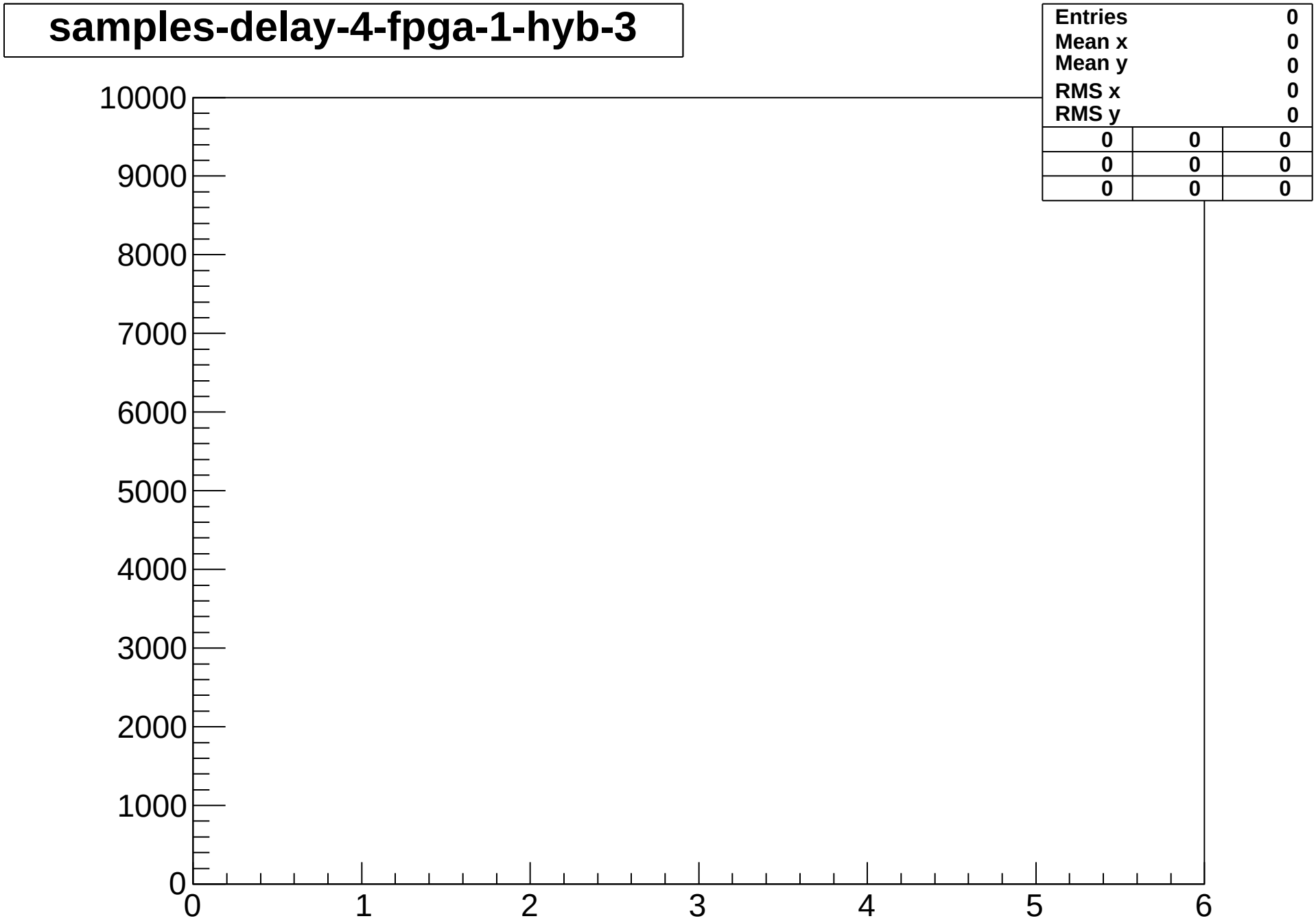
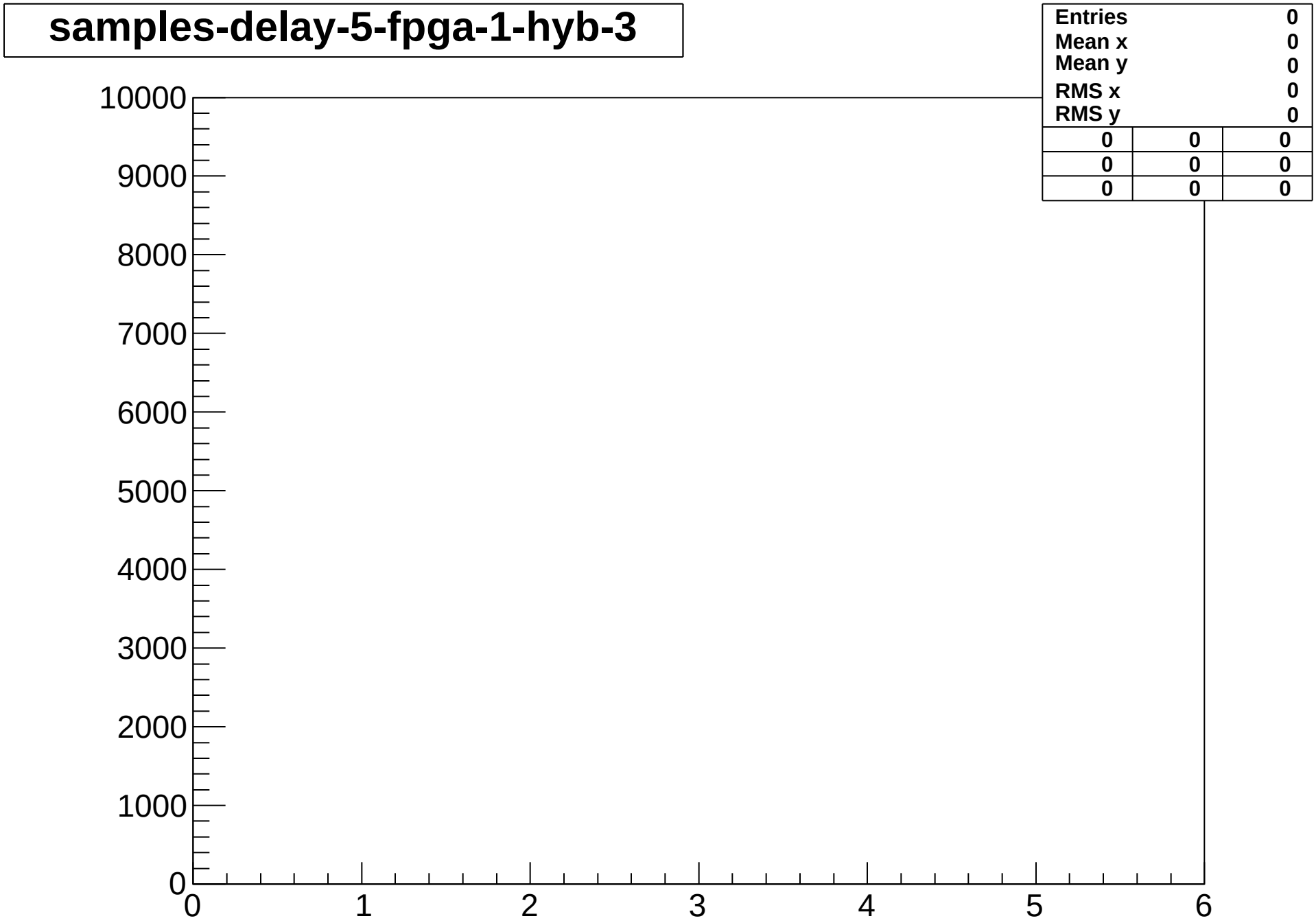
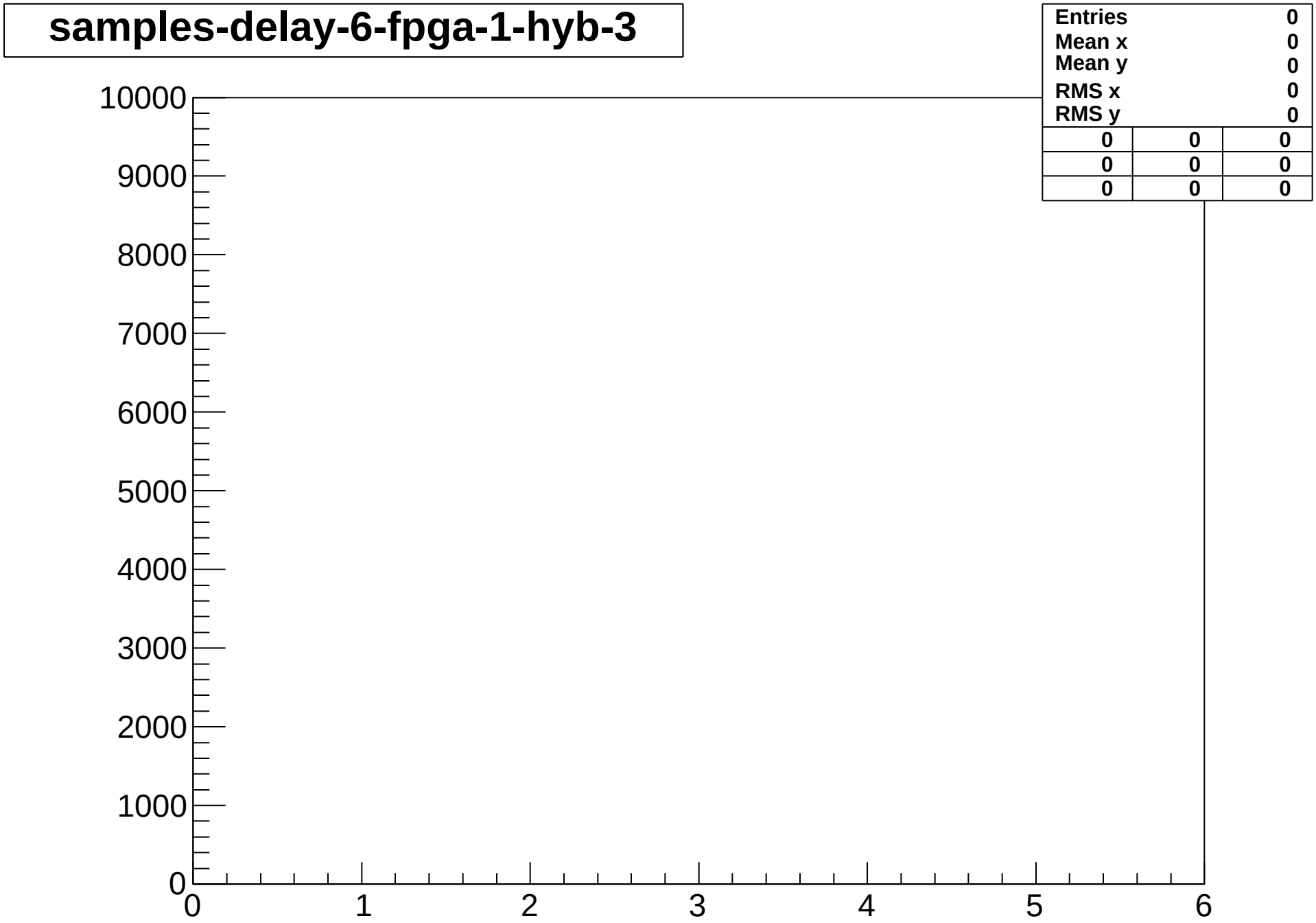
samples-delay-4-fpga-1-hyb-3

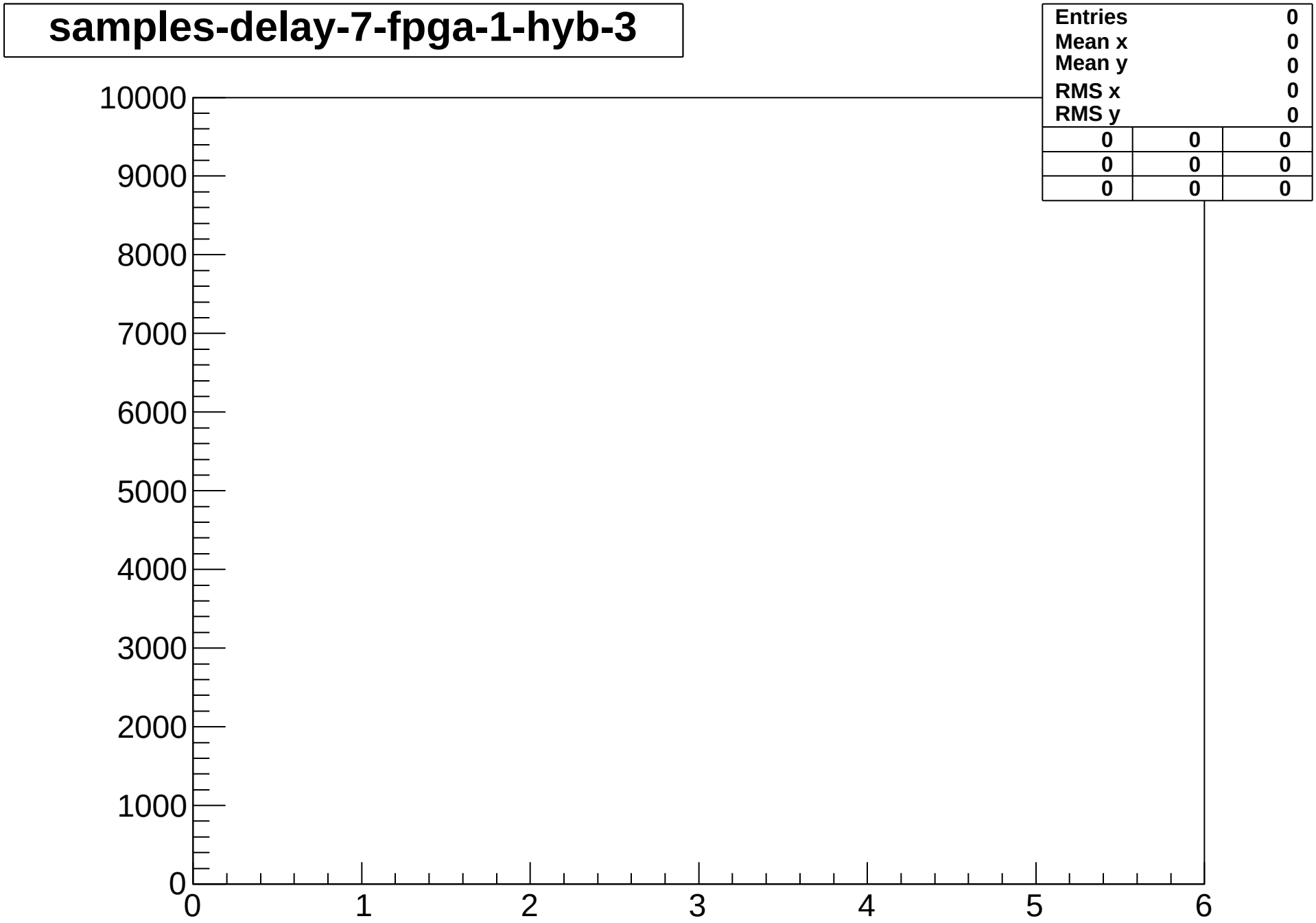


samples-delay-5-fpga-1-hyb-3



samples-delay-6-fpga-1-hyb-3




samples-delay-7-fpga-1-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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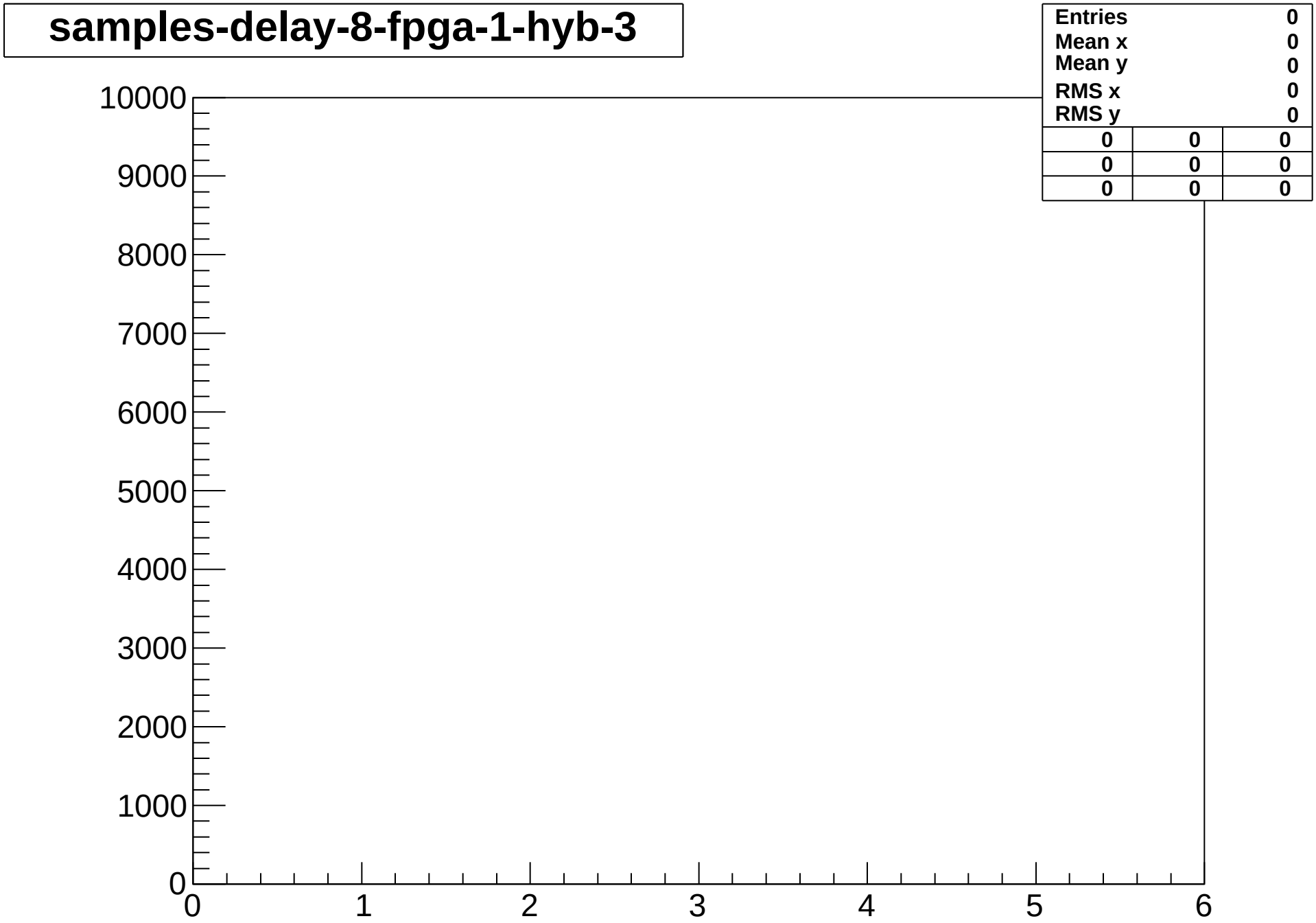
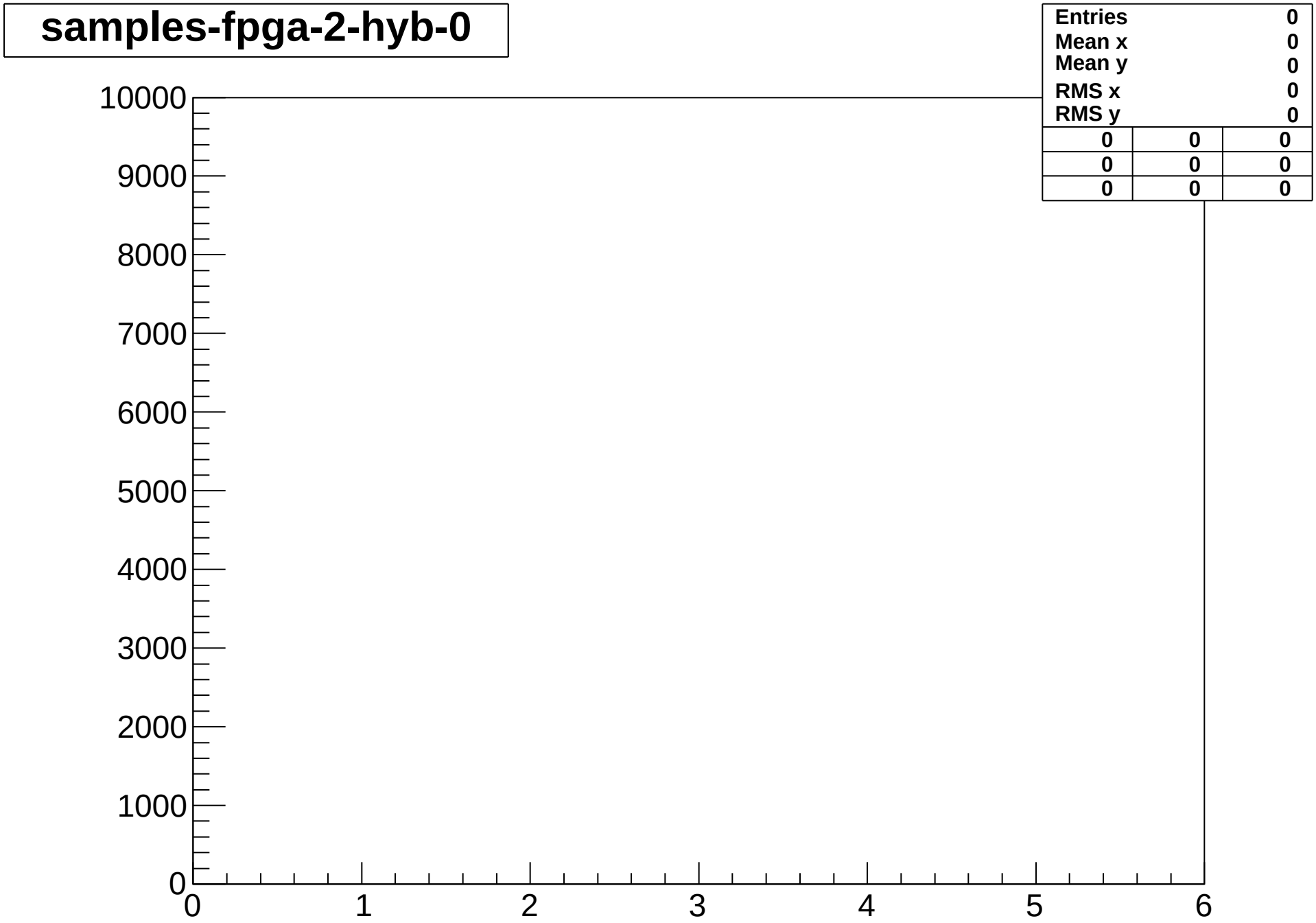
samples-delay-8-fpga-1-hyb-3




samples-fpga-2-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
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3000
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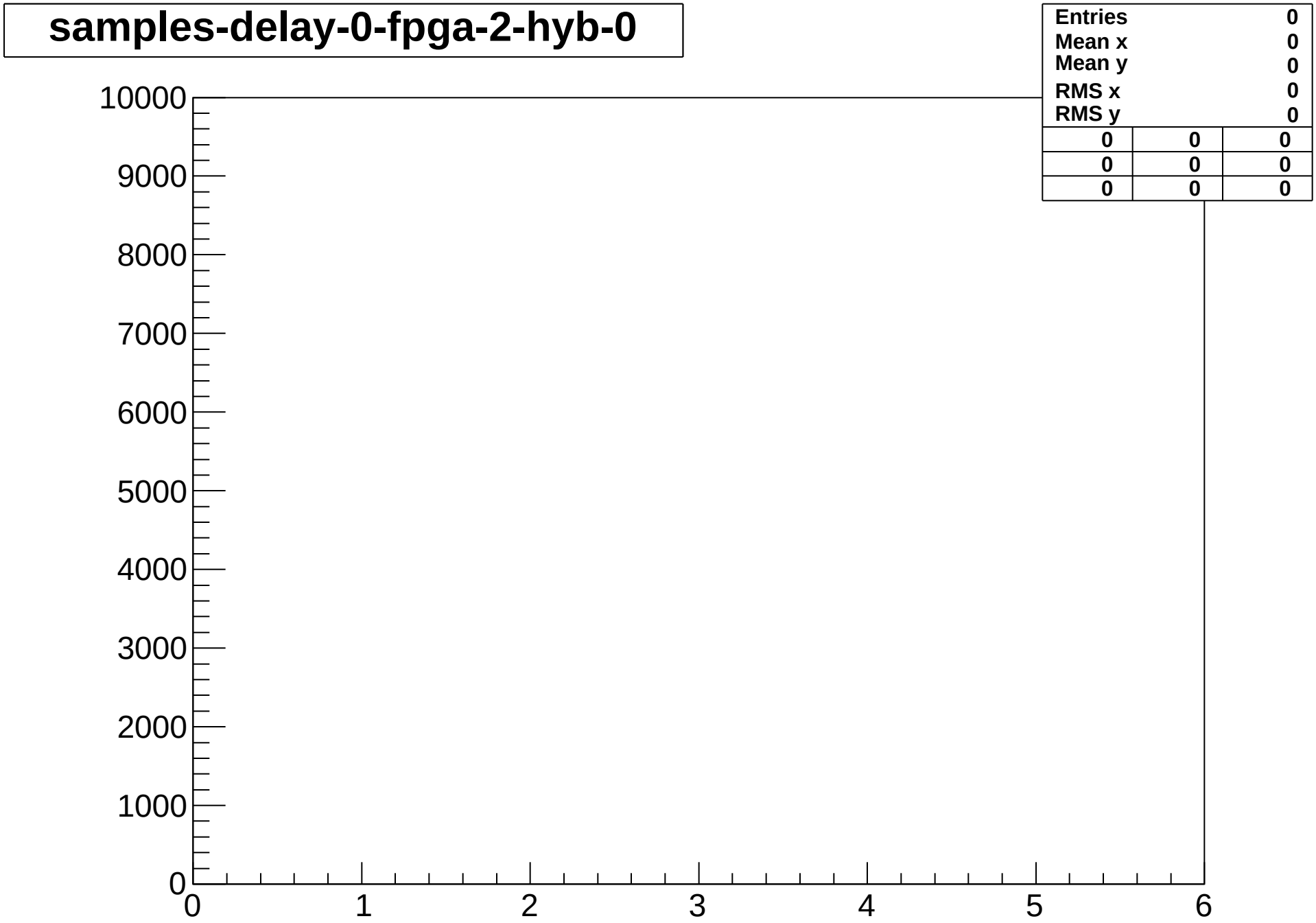
samples-delay-0-fpga-2-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
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0
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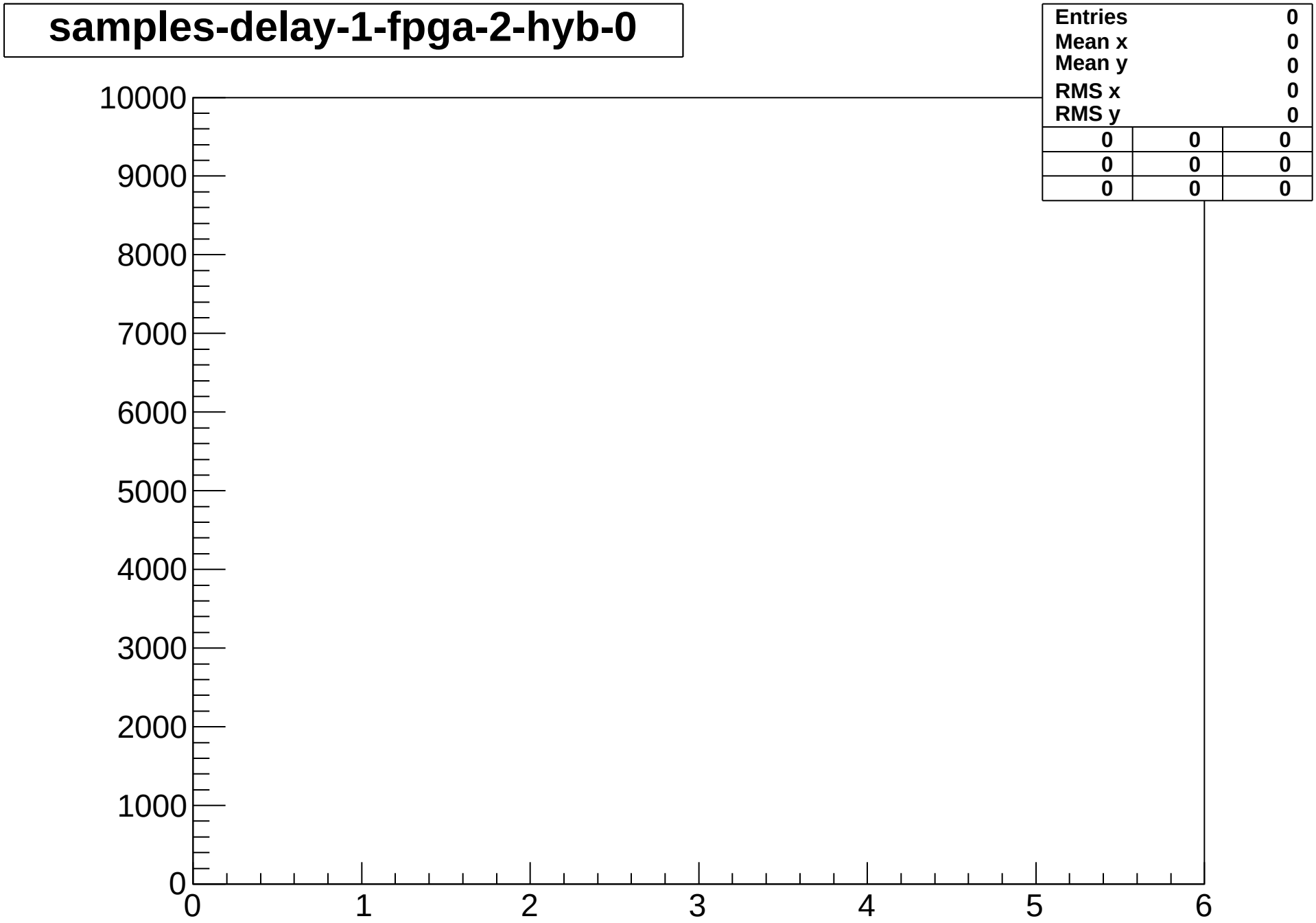
samples-delay-1-fpga-2-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
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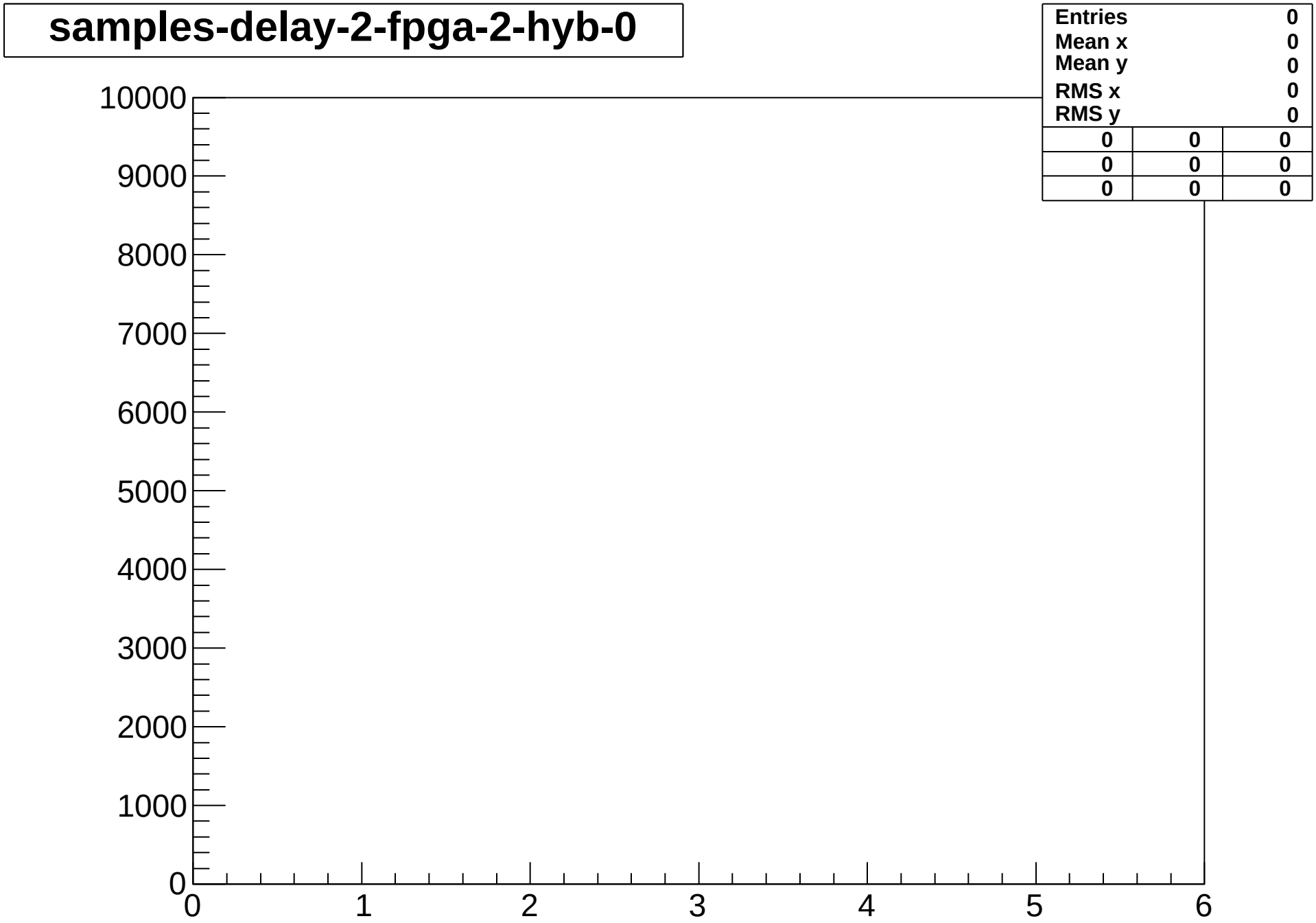
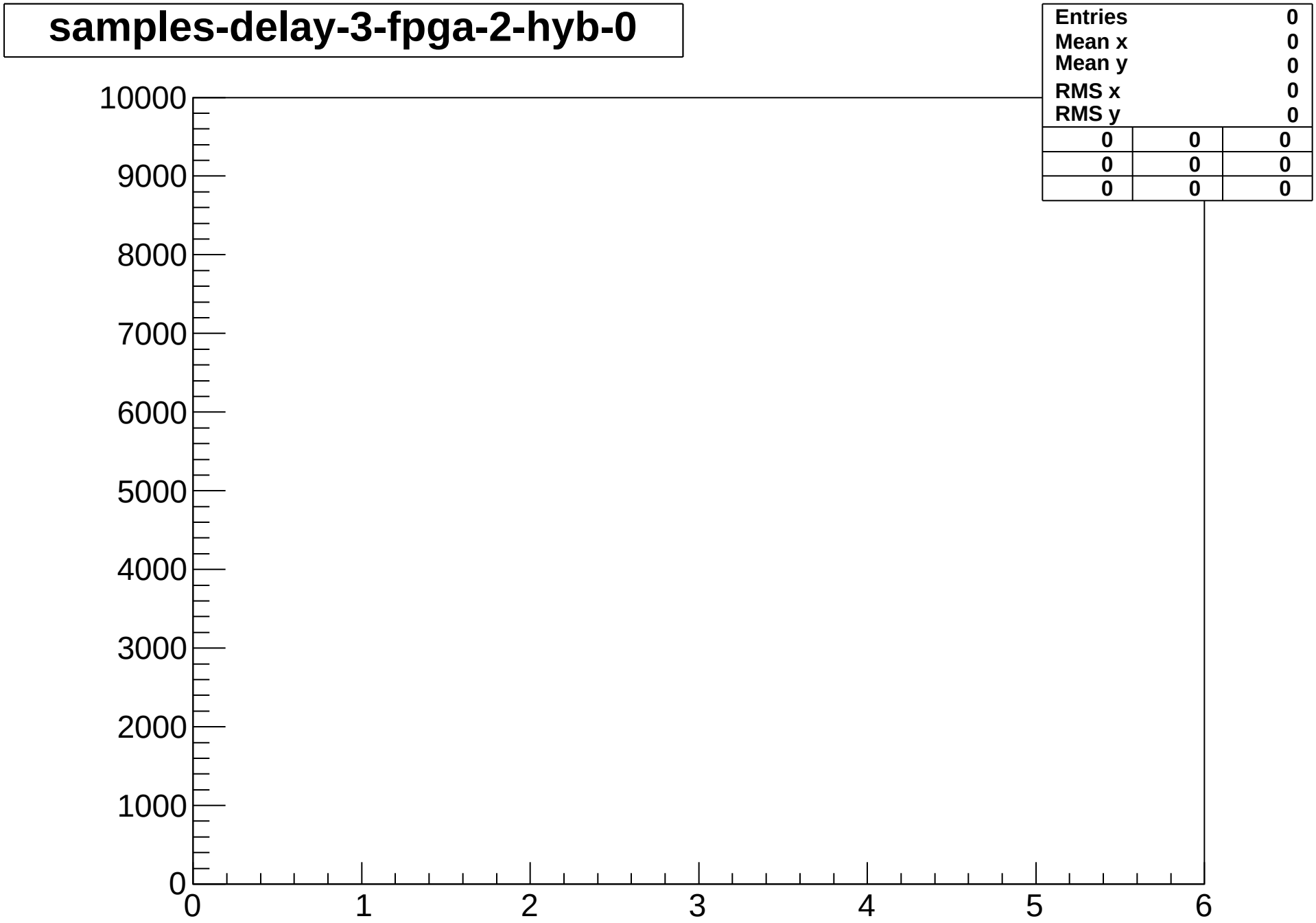
samples-delay-2-fpga-2-hyb-0




samples-delay-3-fpga-2-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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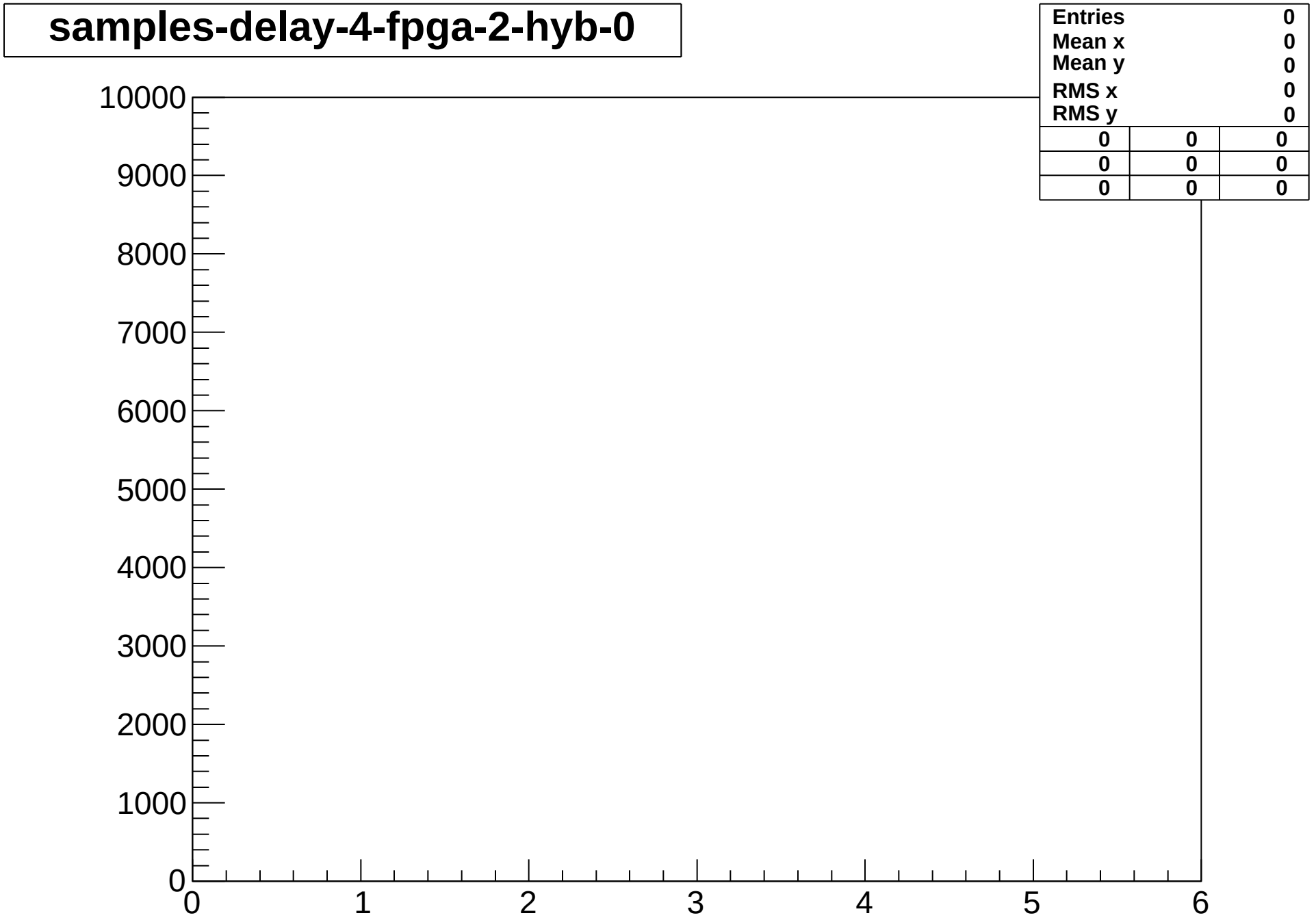
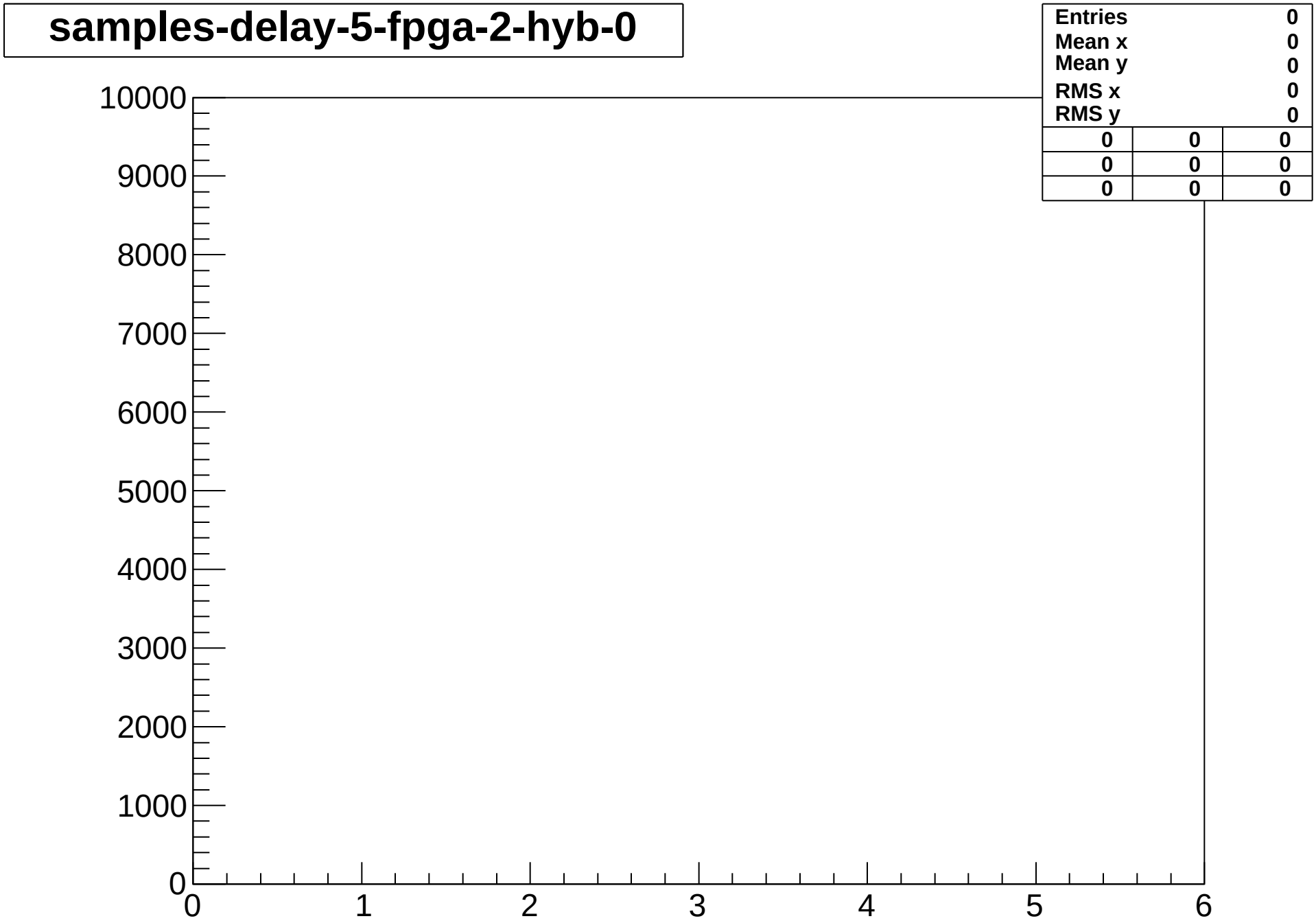
samples-delay-4-fpga-2-hyb-0




samples-delay-5-fpga-2-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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6000
5000
4000
3000
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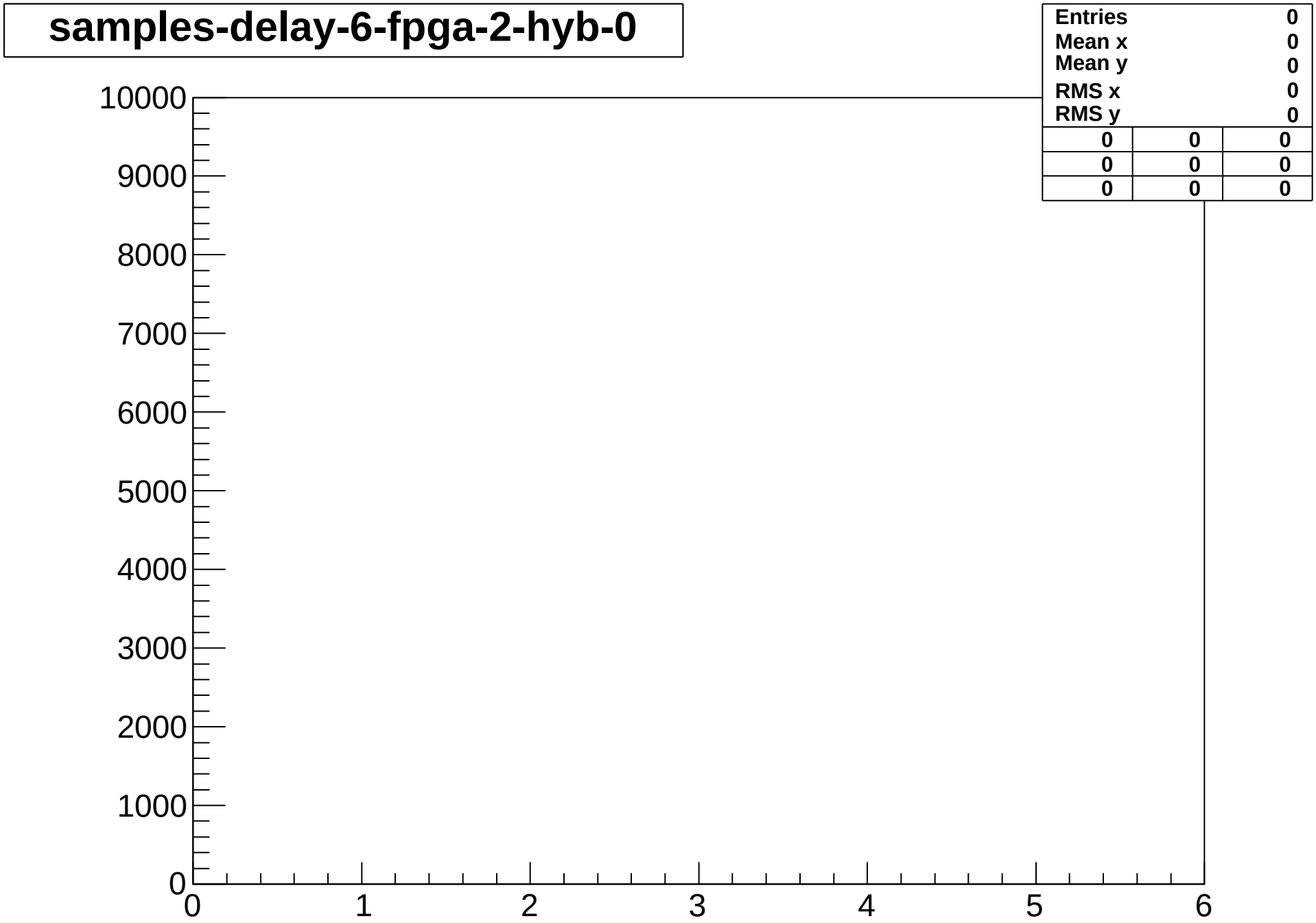
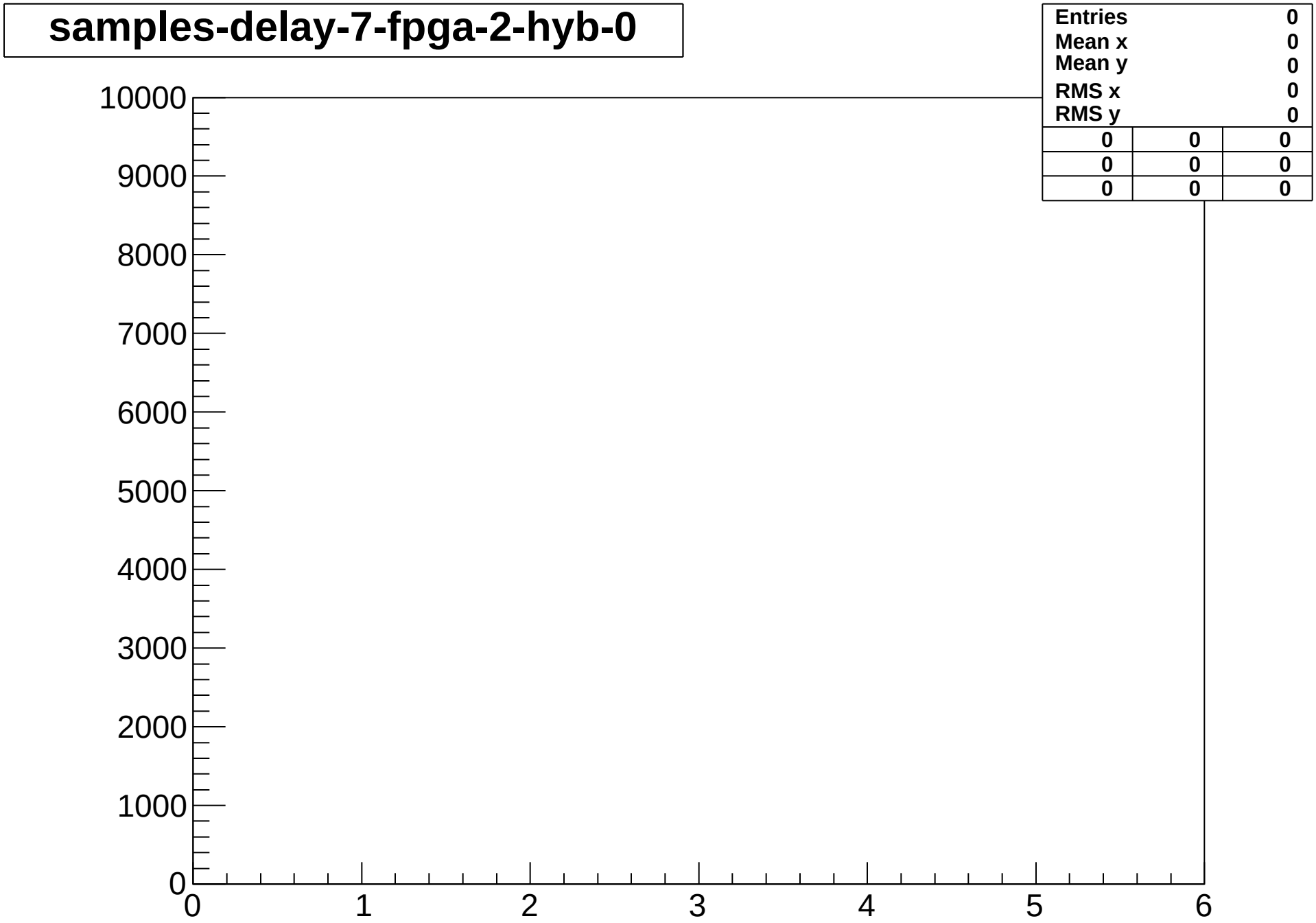
samples-delay-6-fpga-2-hyb-0




samples-delay-7-fpga-2-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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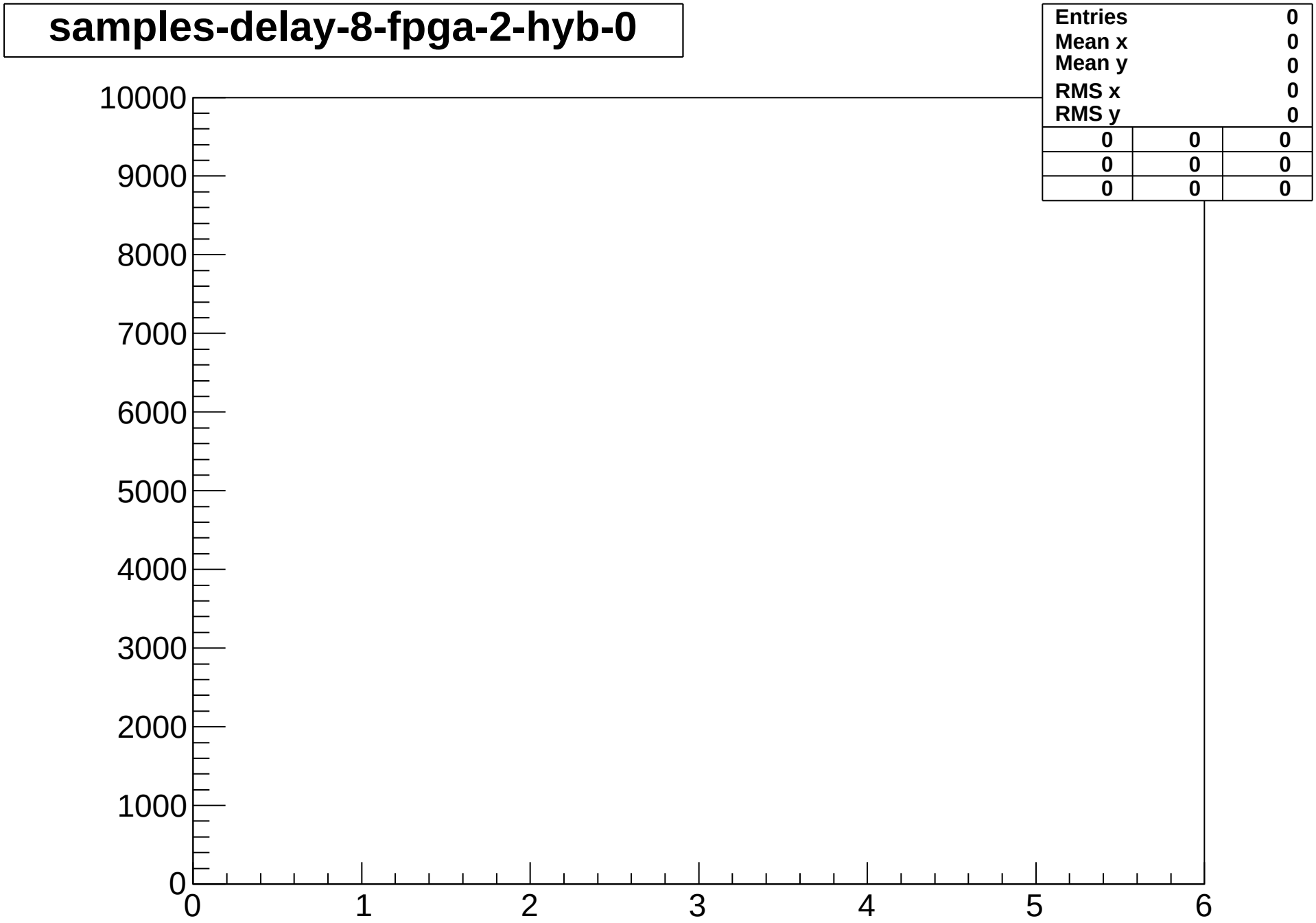
samples-delay-8-fpga-2-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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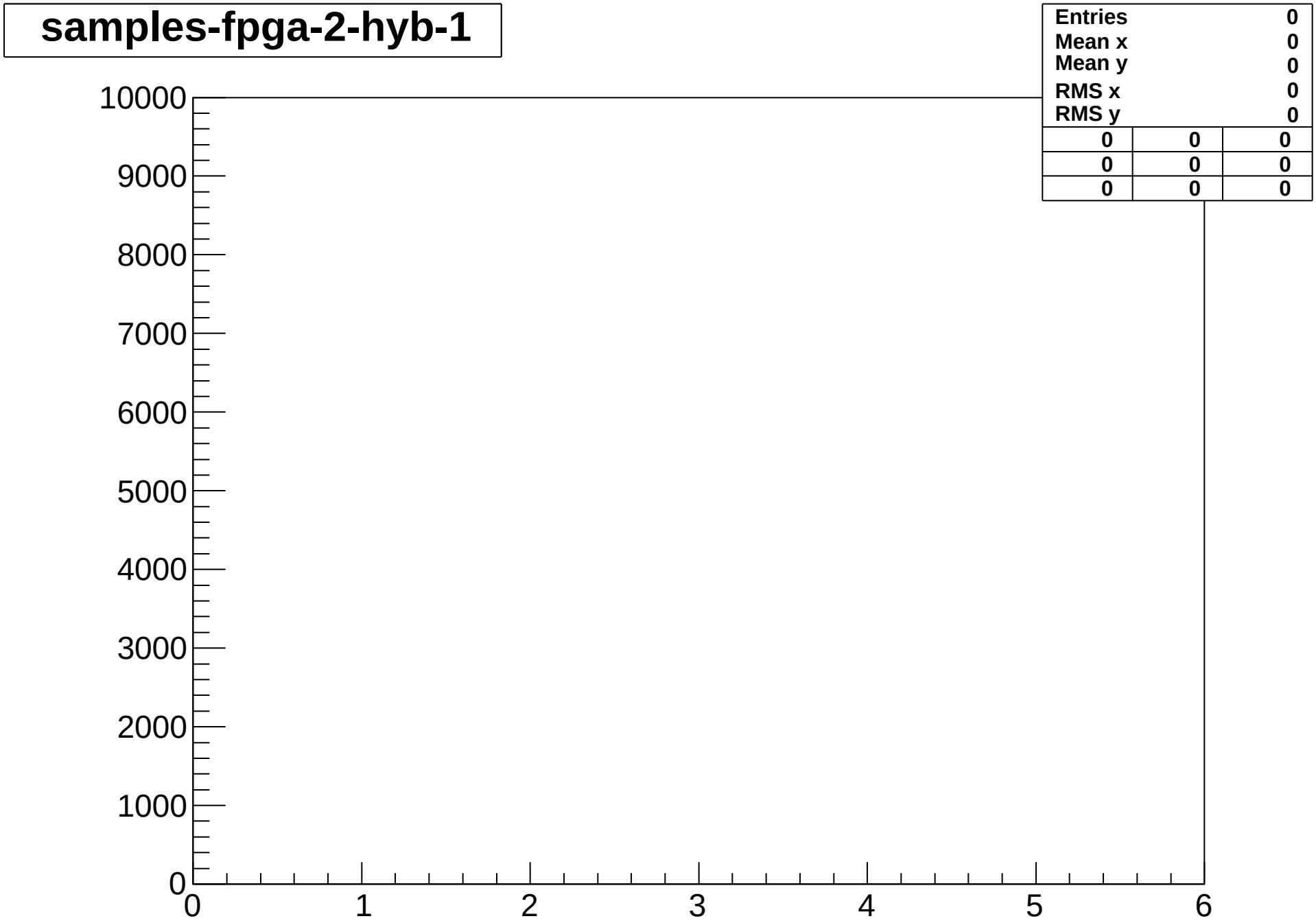
samples-fpga-2-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
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5000
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3000
2000
1000
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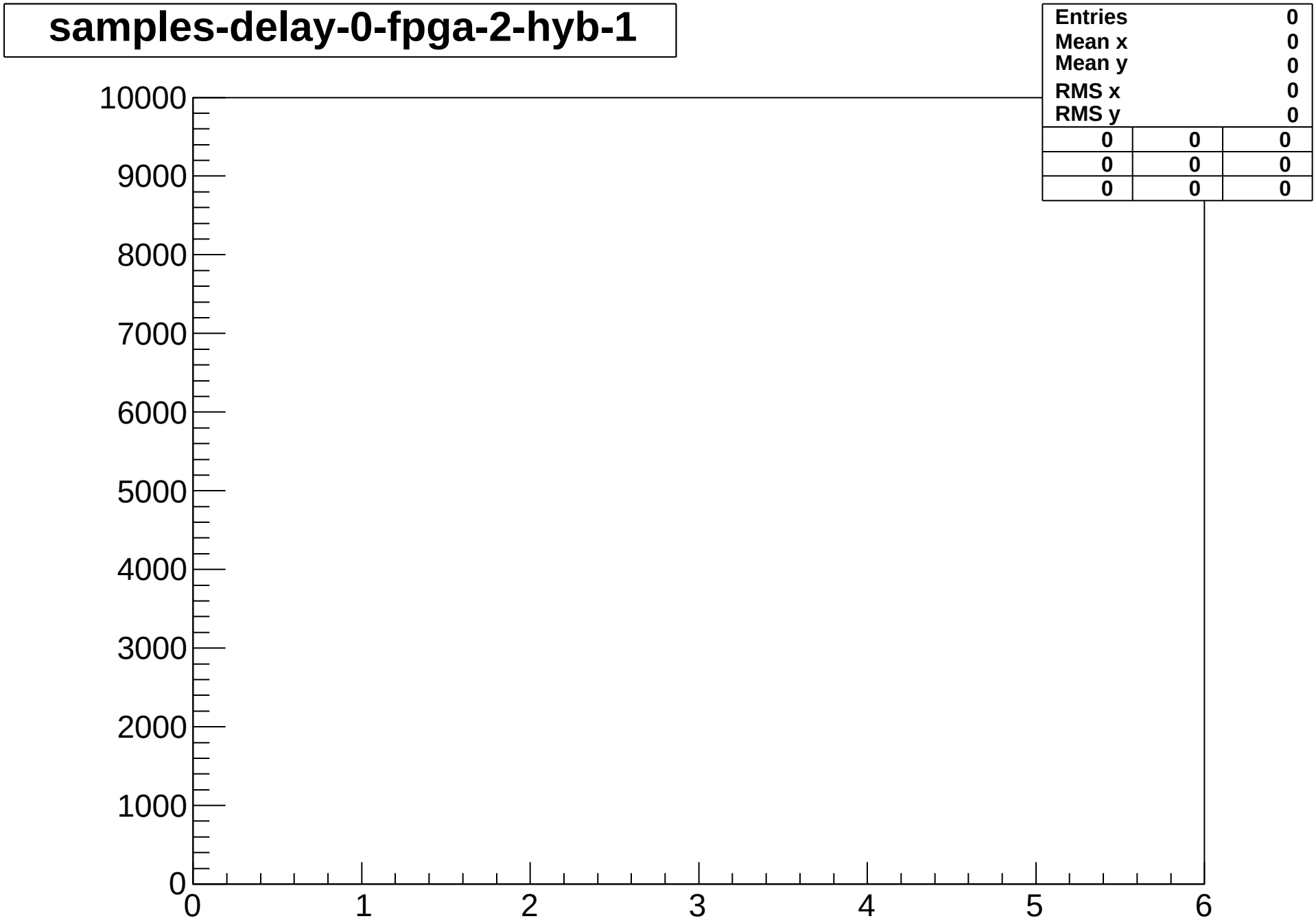
samples-delay-0-fpga-2-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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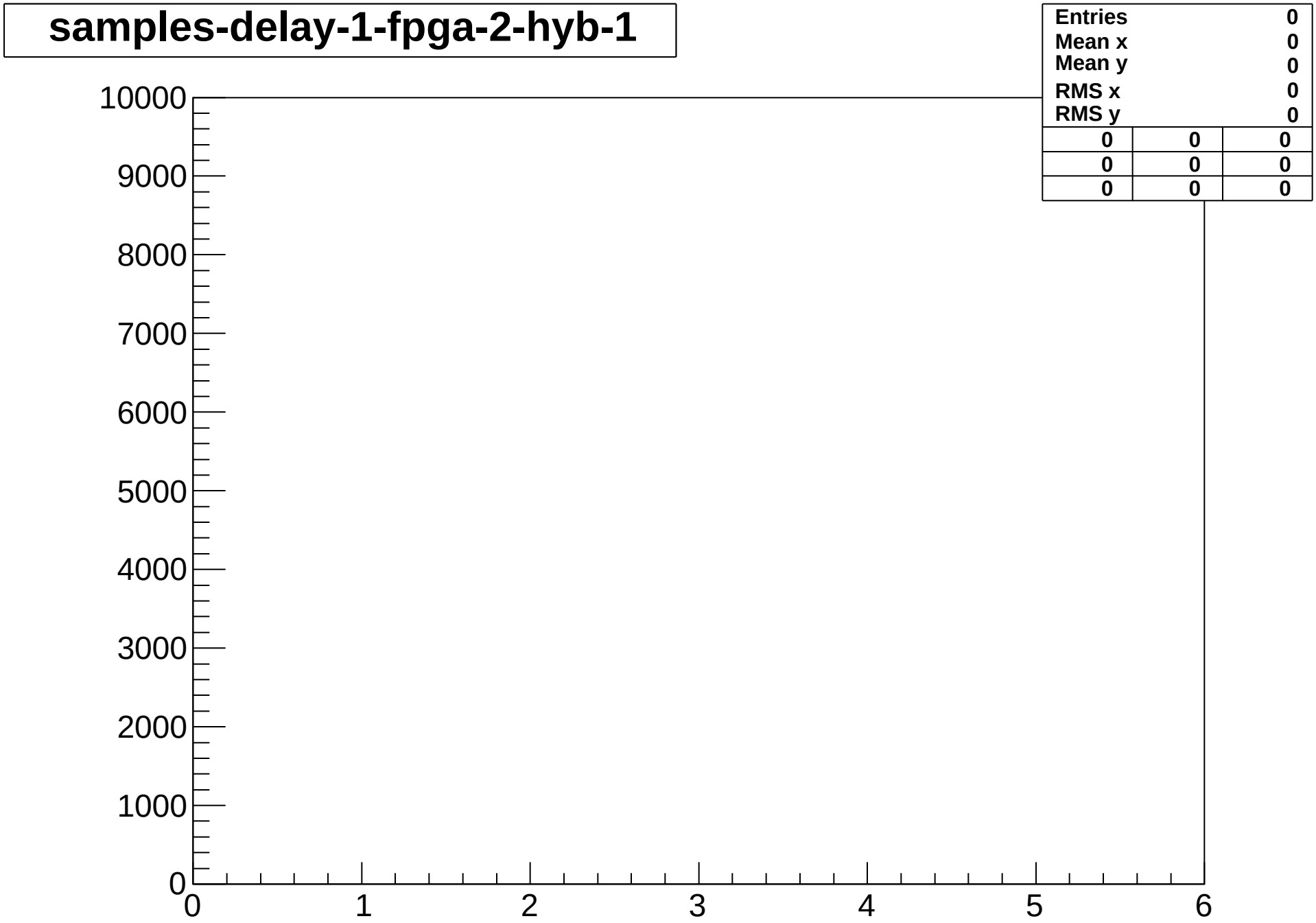
samples-delay-1-fpga-2-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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6000
5000
4000
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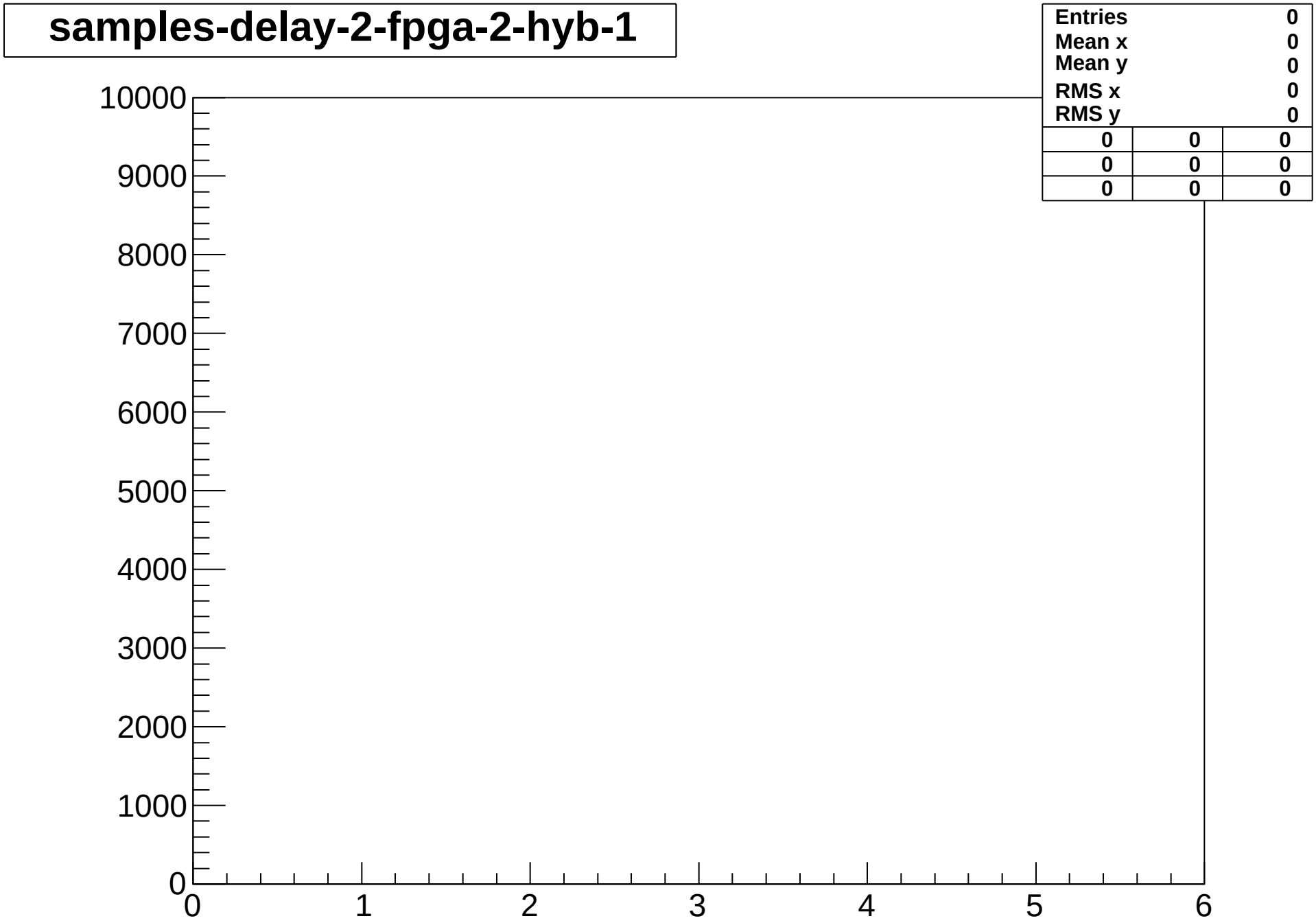
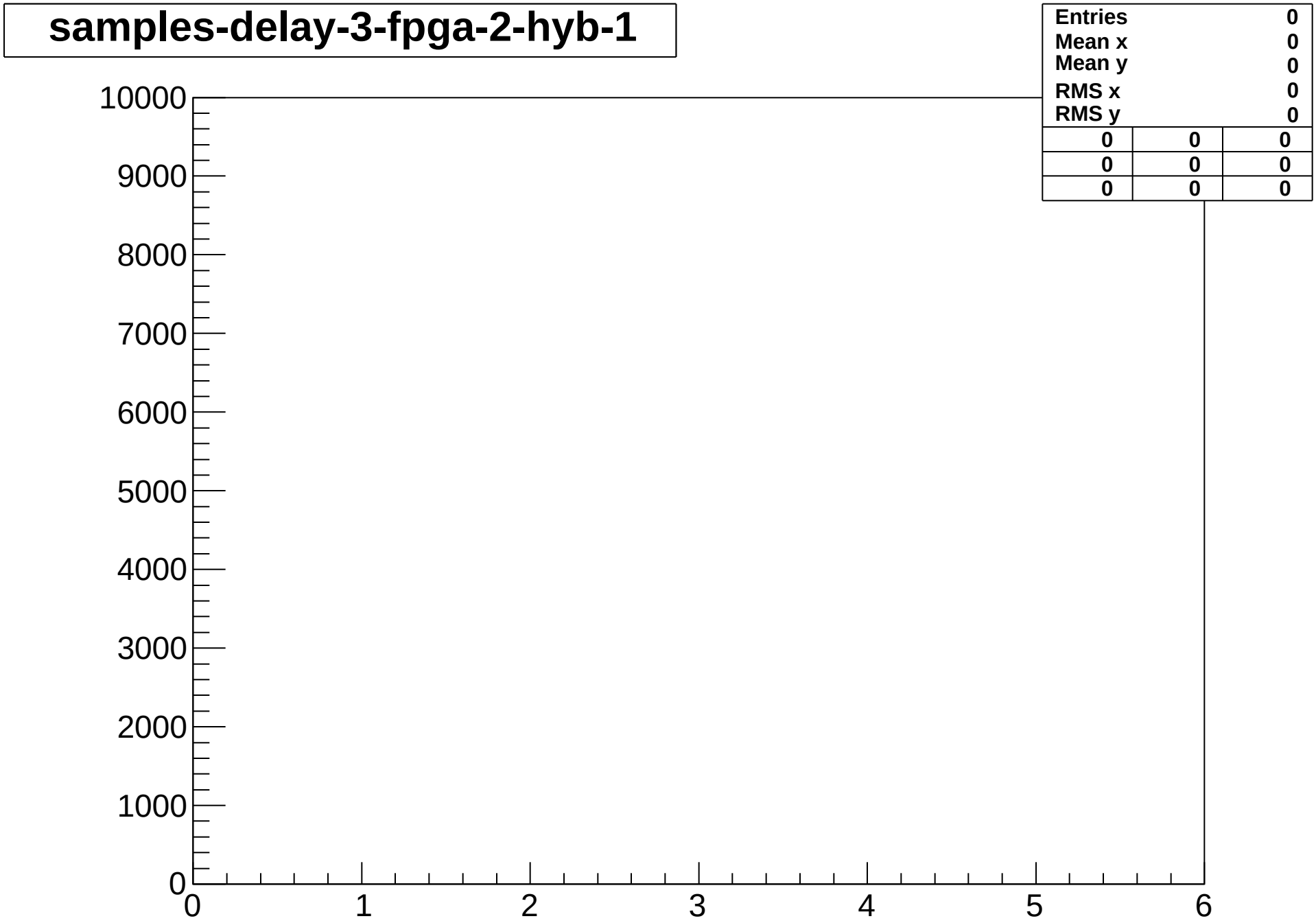
samples-delay-2-fpga-2-hyb-1




samples-delay-3-fpga-2-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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4000
3000
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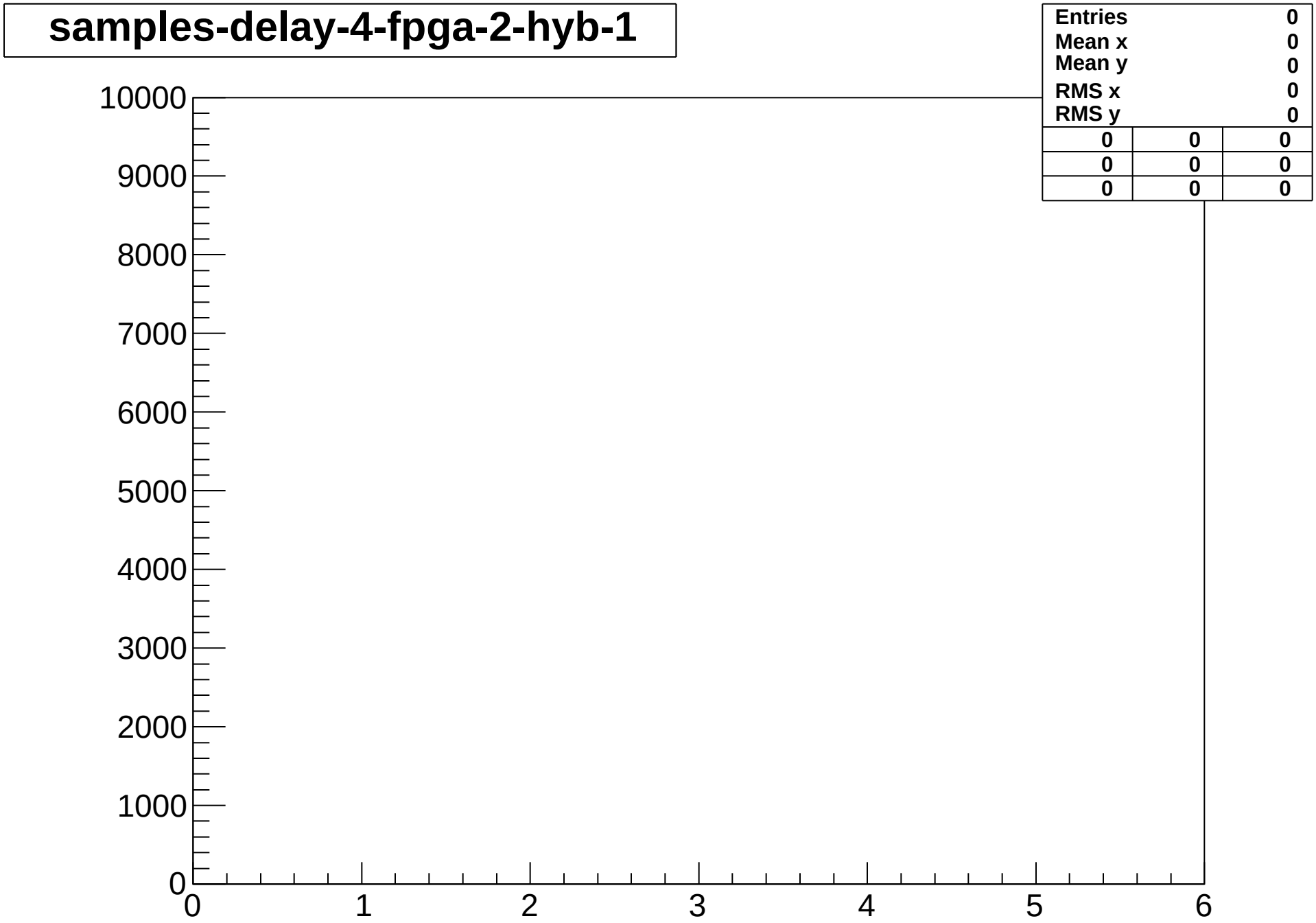
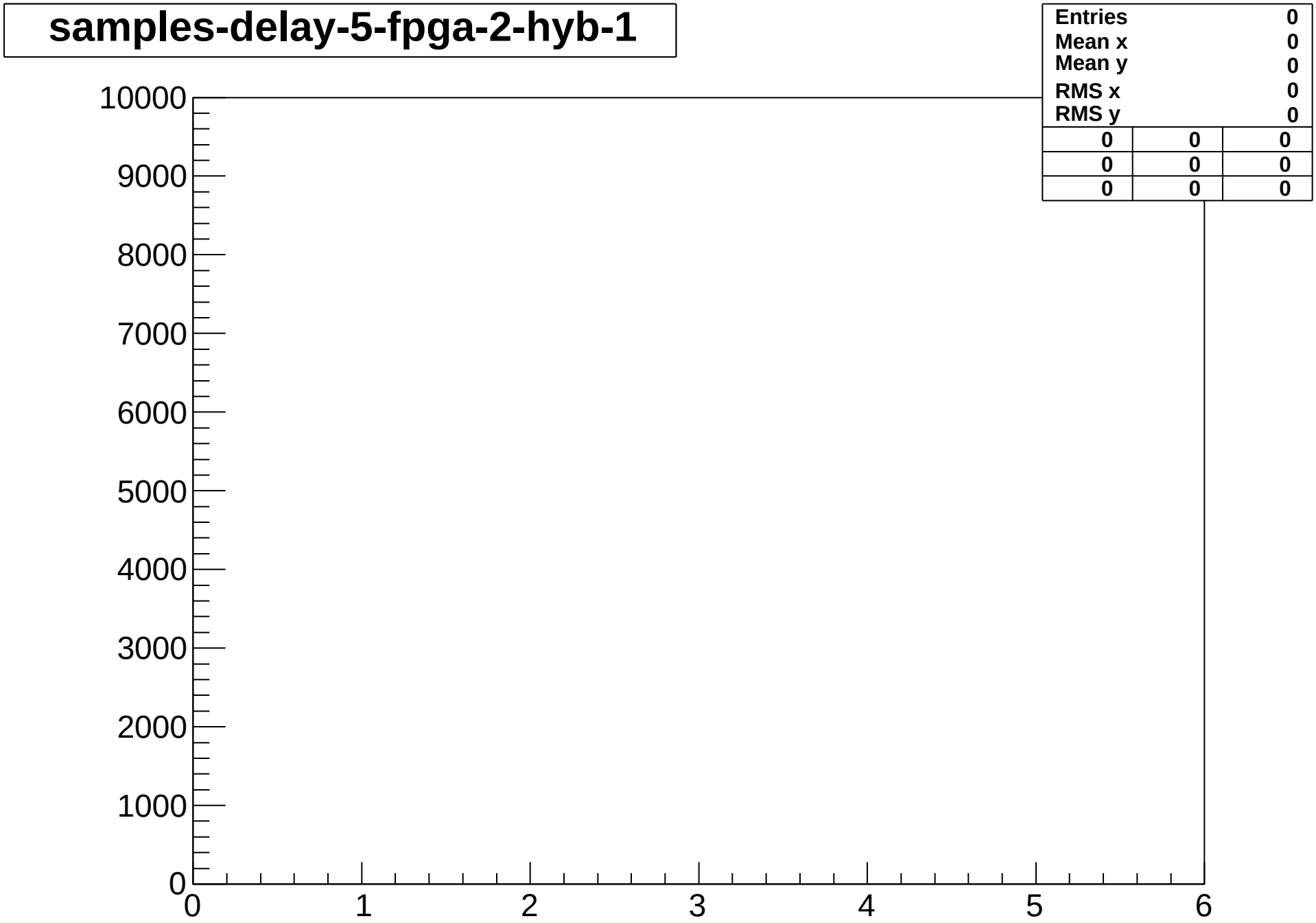
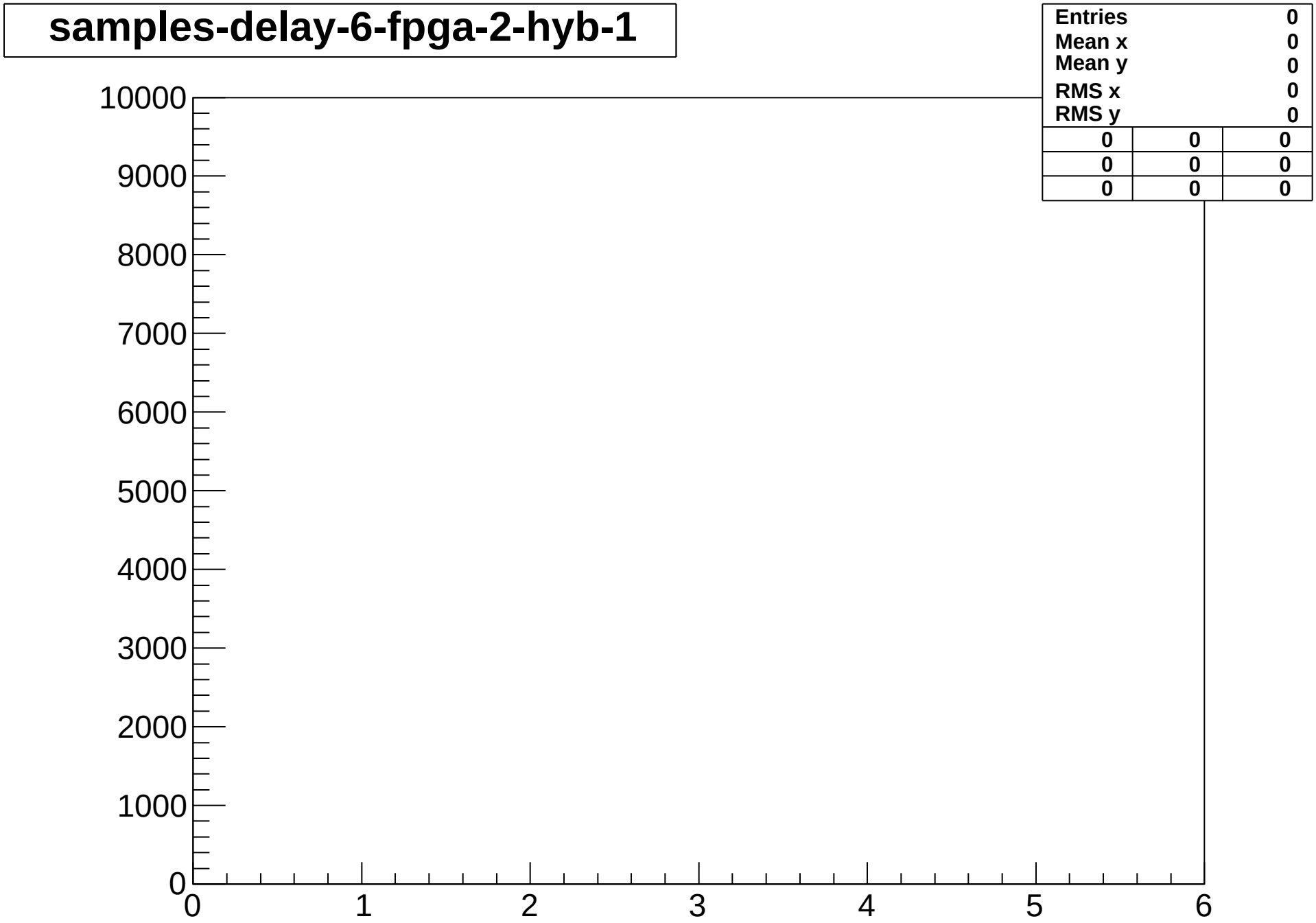
samples-delay-4-fpga-2-hyb-1



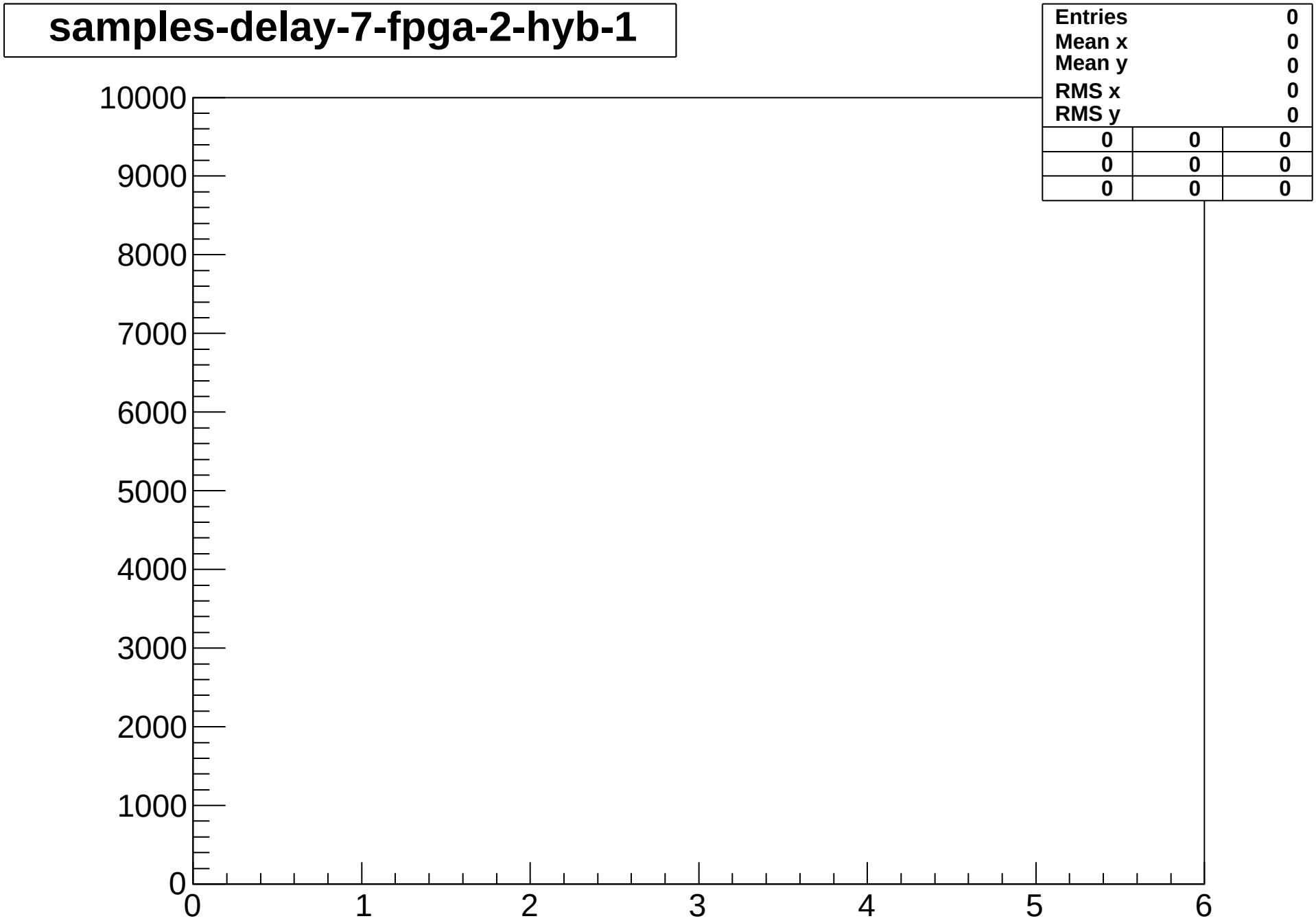
samples-delay-5-fpga-2-hyb-1



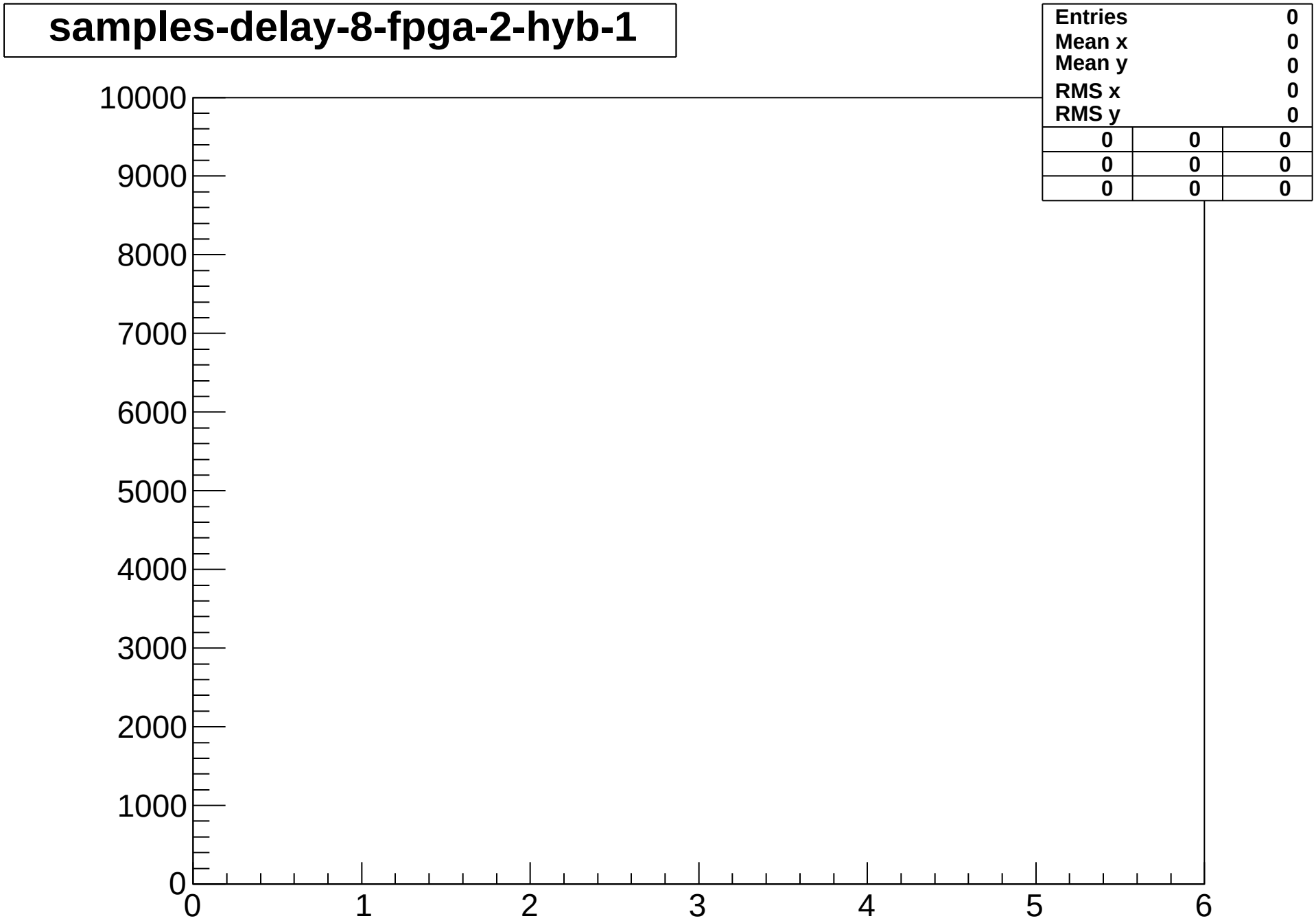
samples-delay-6-fpga-2-hyb-1

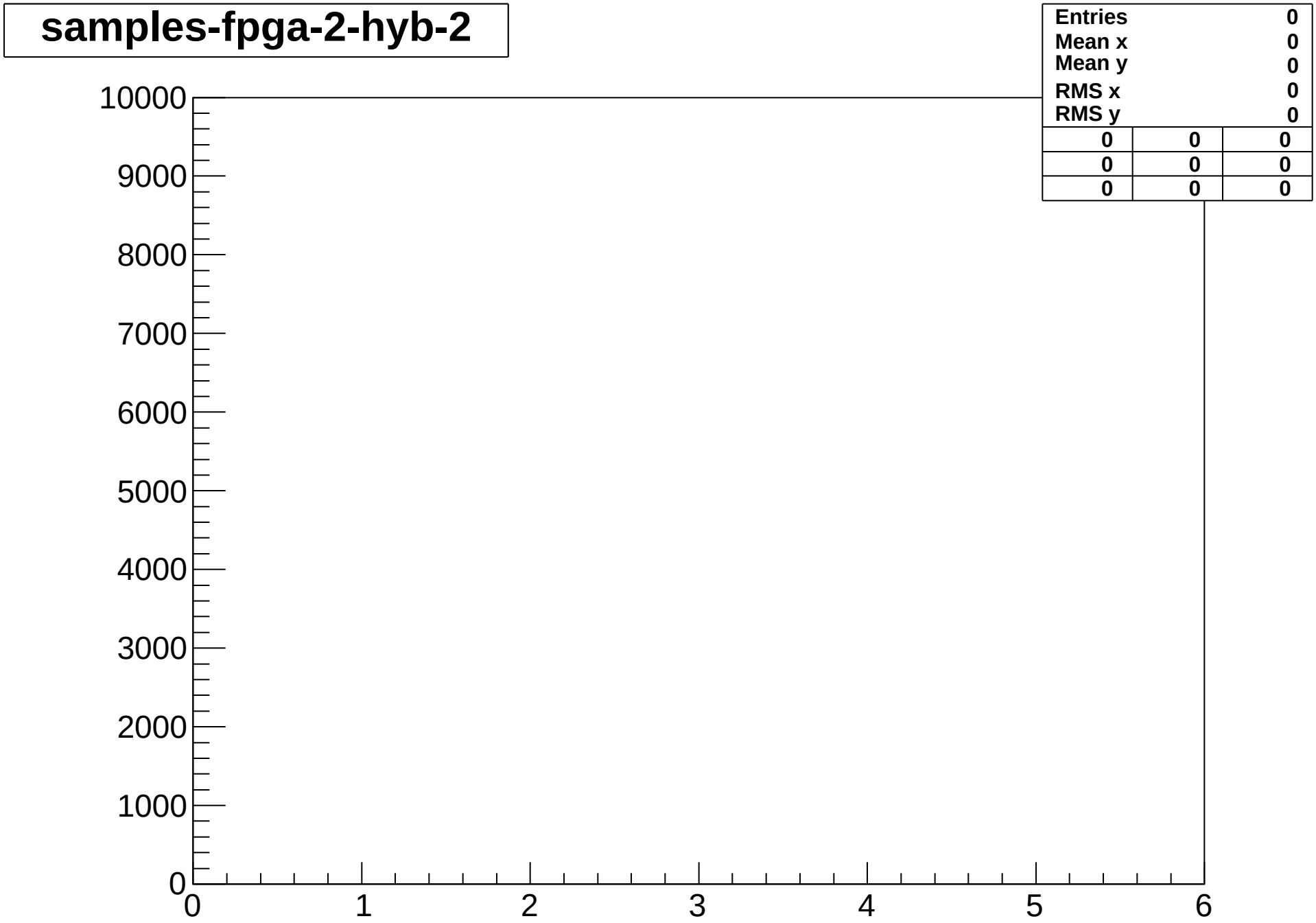


samples-delay-7-fpga-2-hyb-1



samples-delay-8-fpga-2-hyb-1




samples-fpga-2-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
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0
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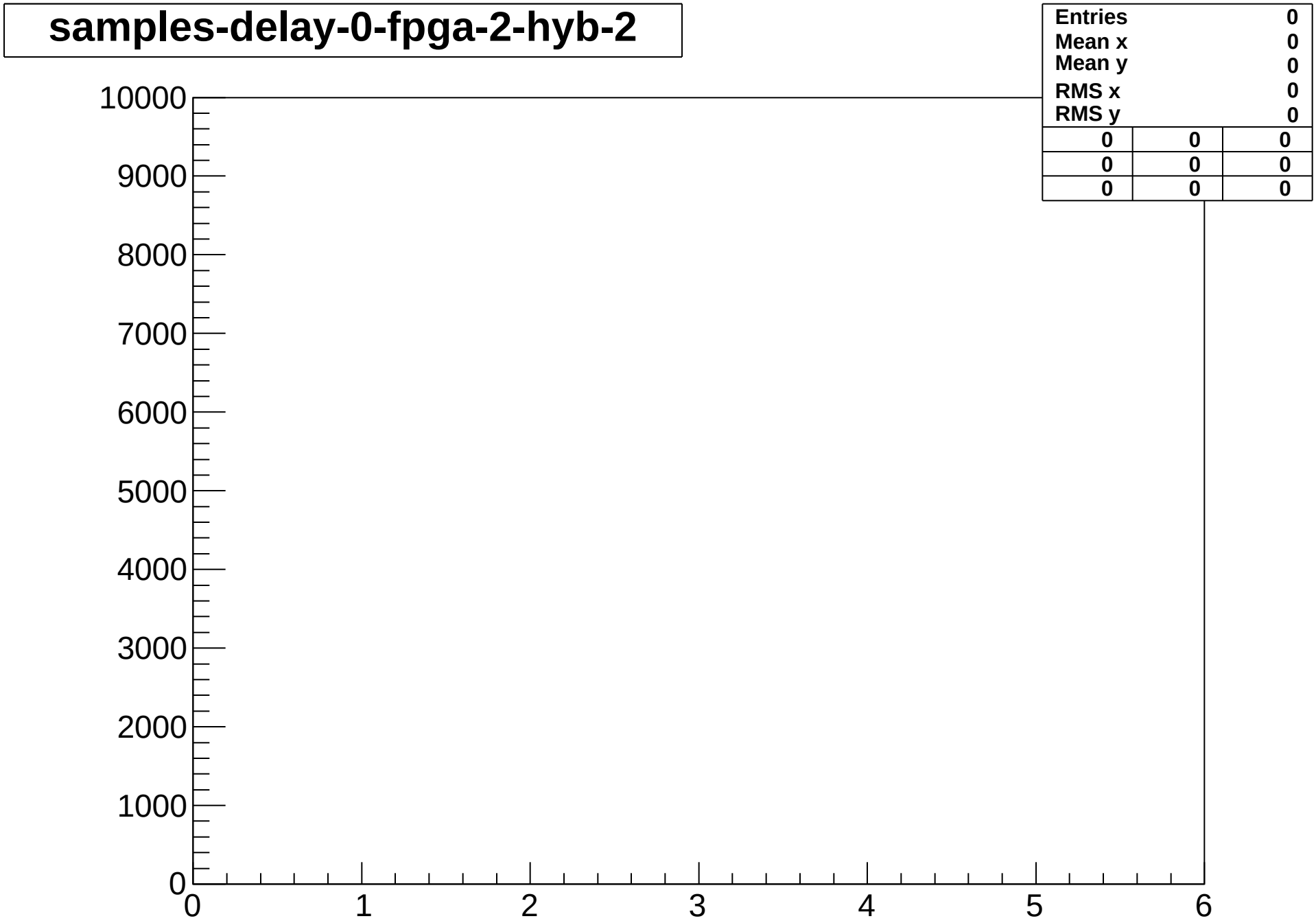
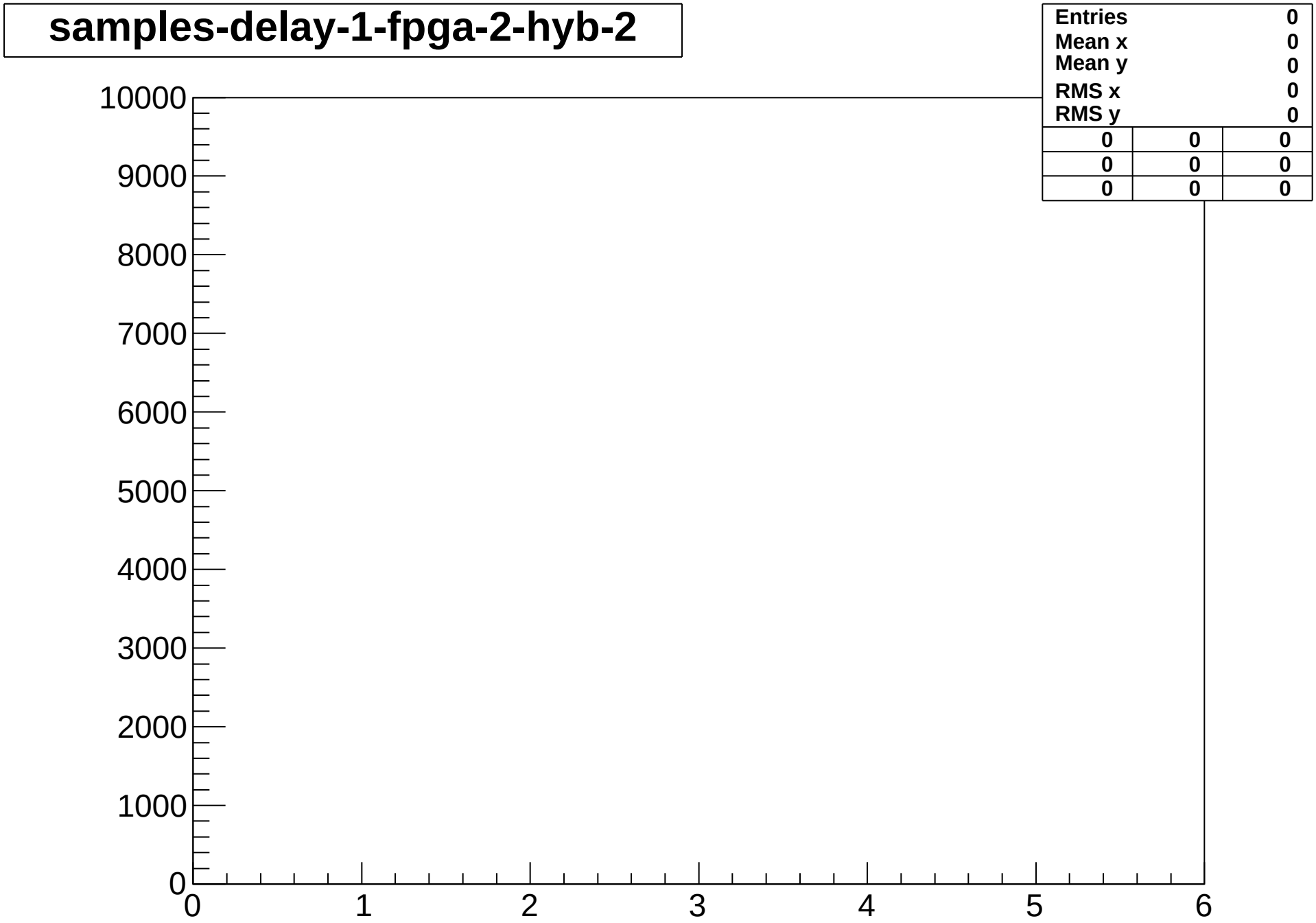
samples-delay-0-fpga-2-hyb-2




samples-delay-1-fpga-2-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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10000
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4000
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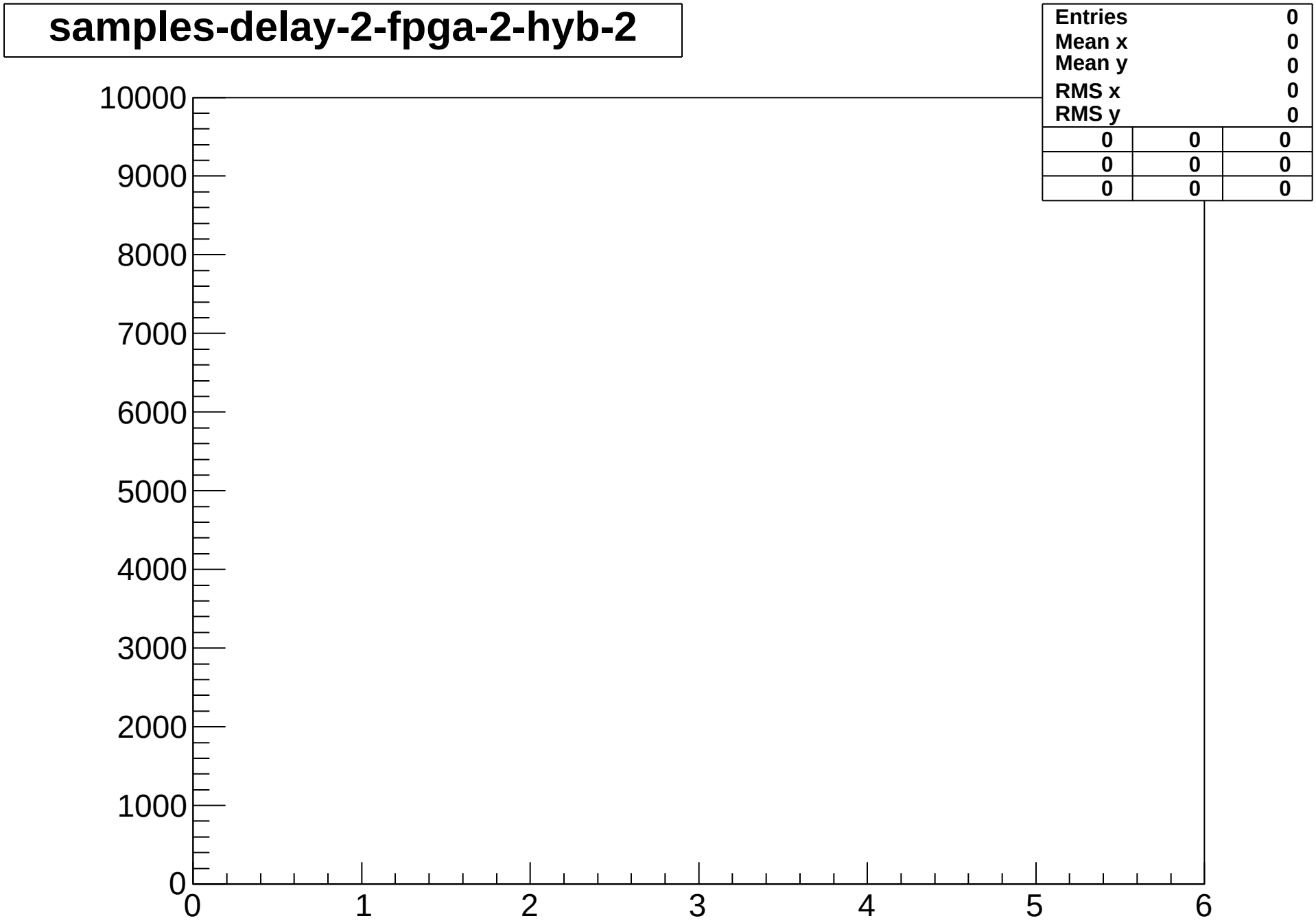
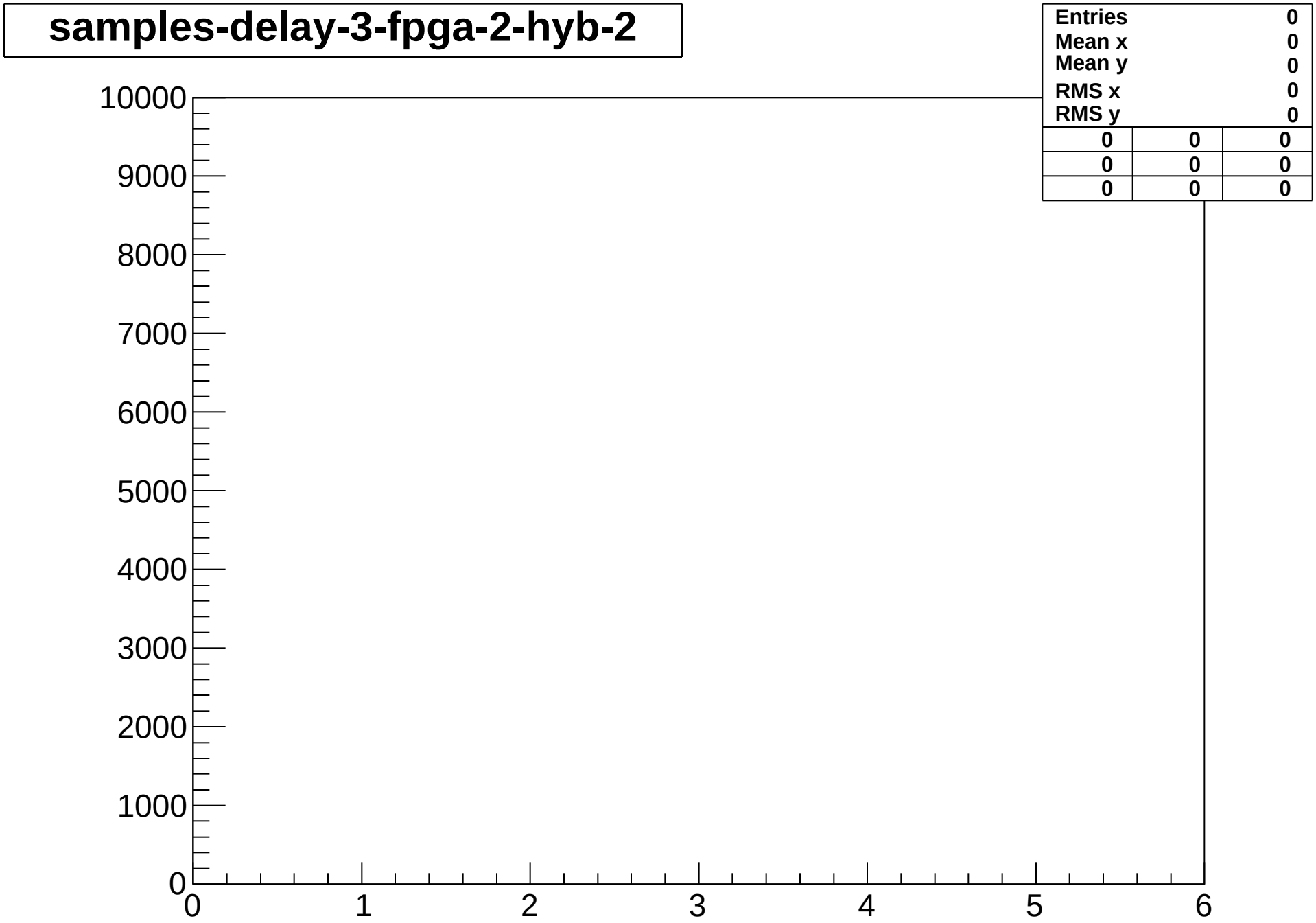
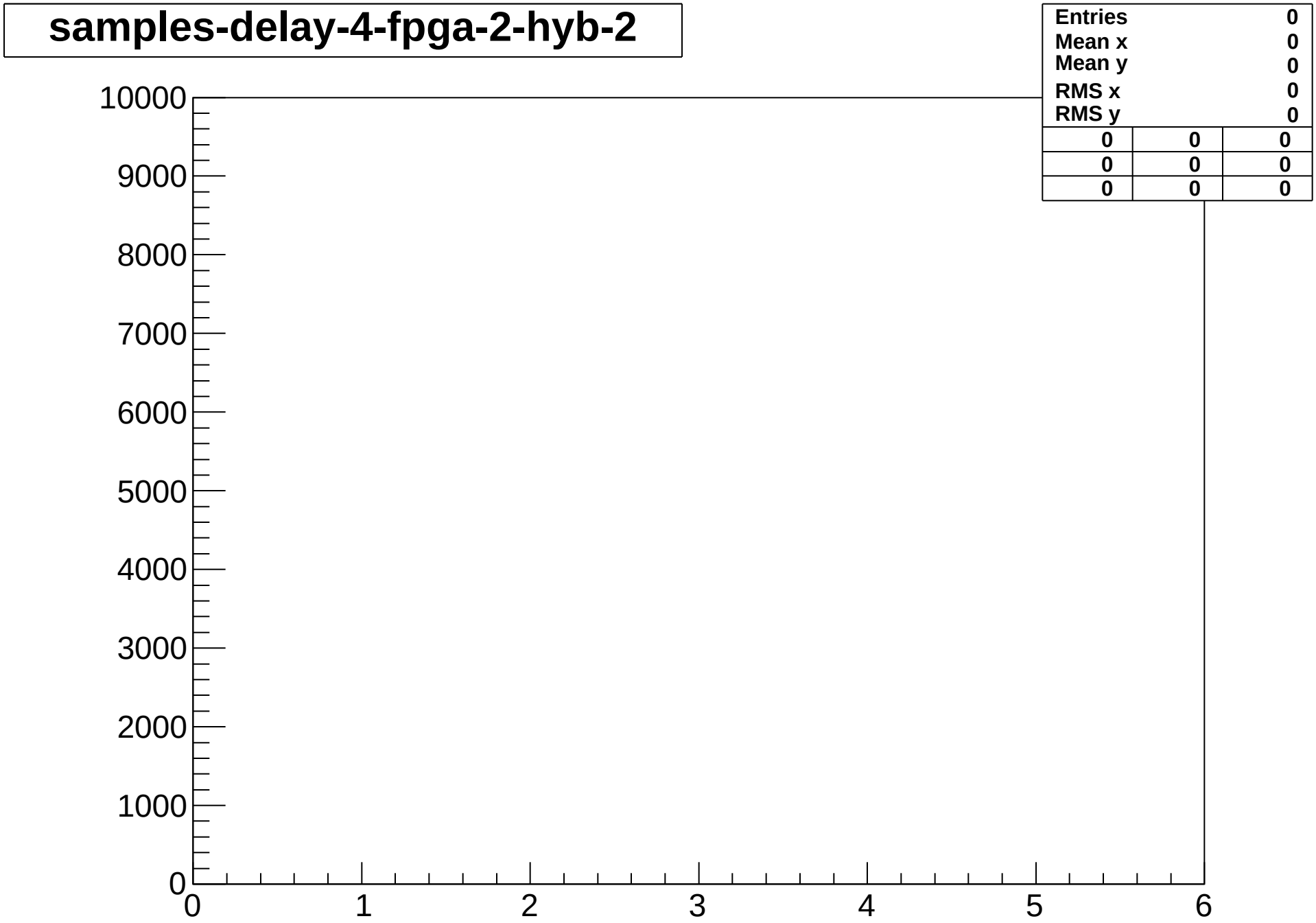
samples-delay-2-fpga-2-hyb-2

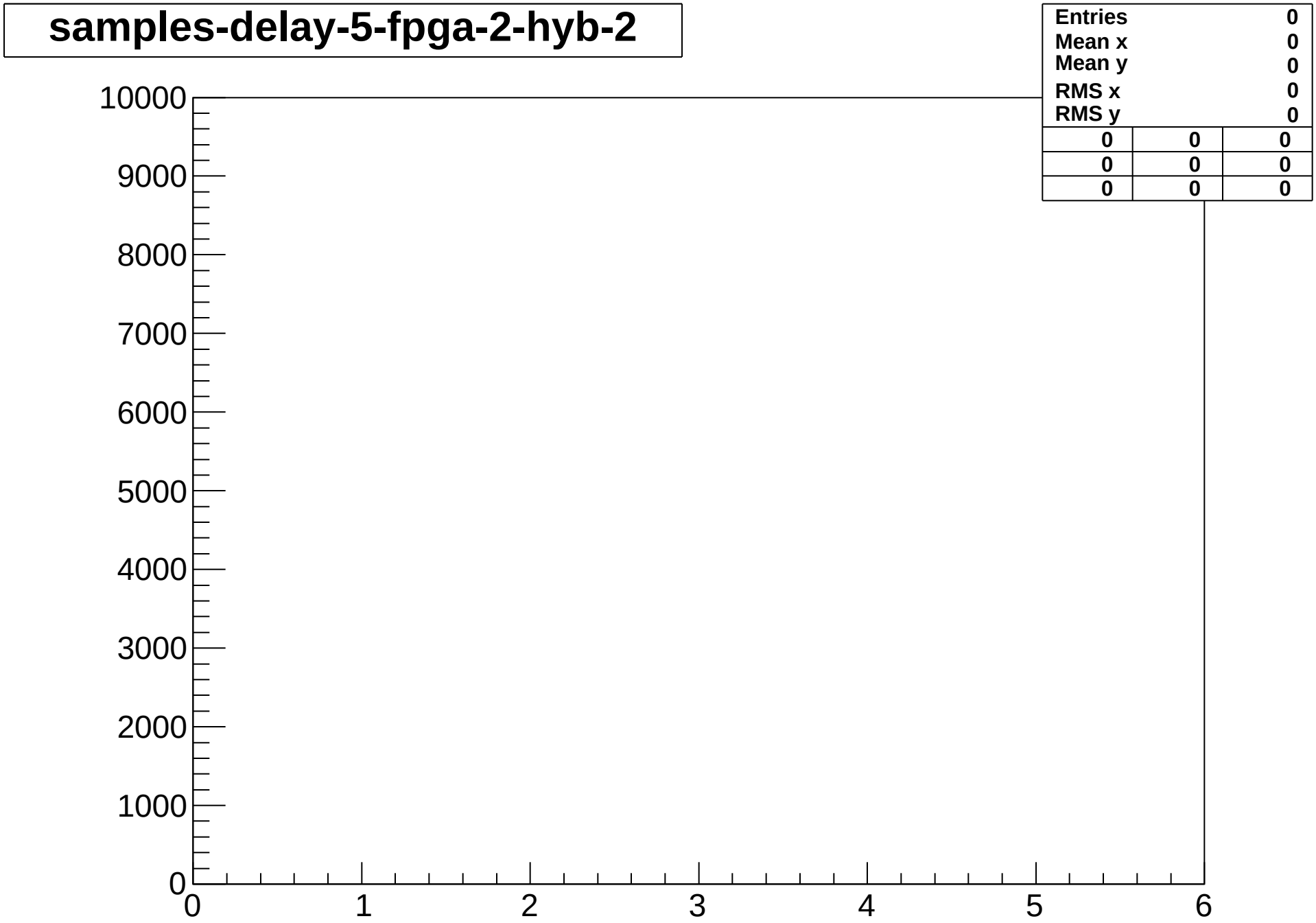


samples-delay-3-fpga-2-hyb-2



samples-delay-4-fpga-2-hyb-2




samples-delay-5-fpga-2-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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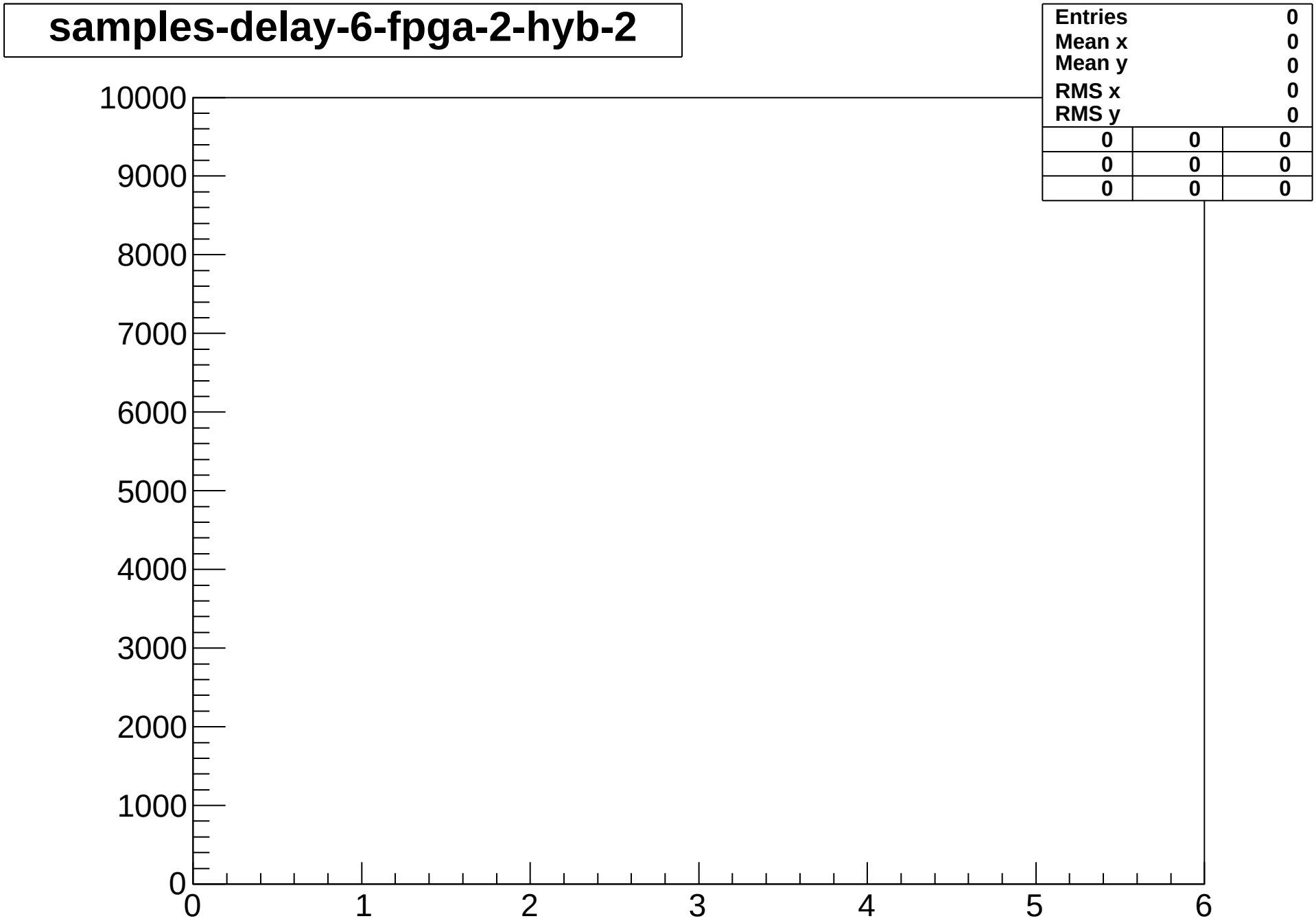
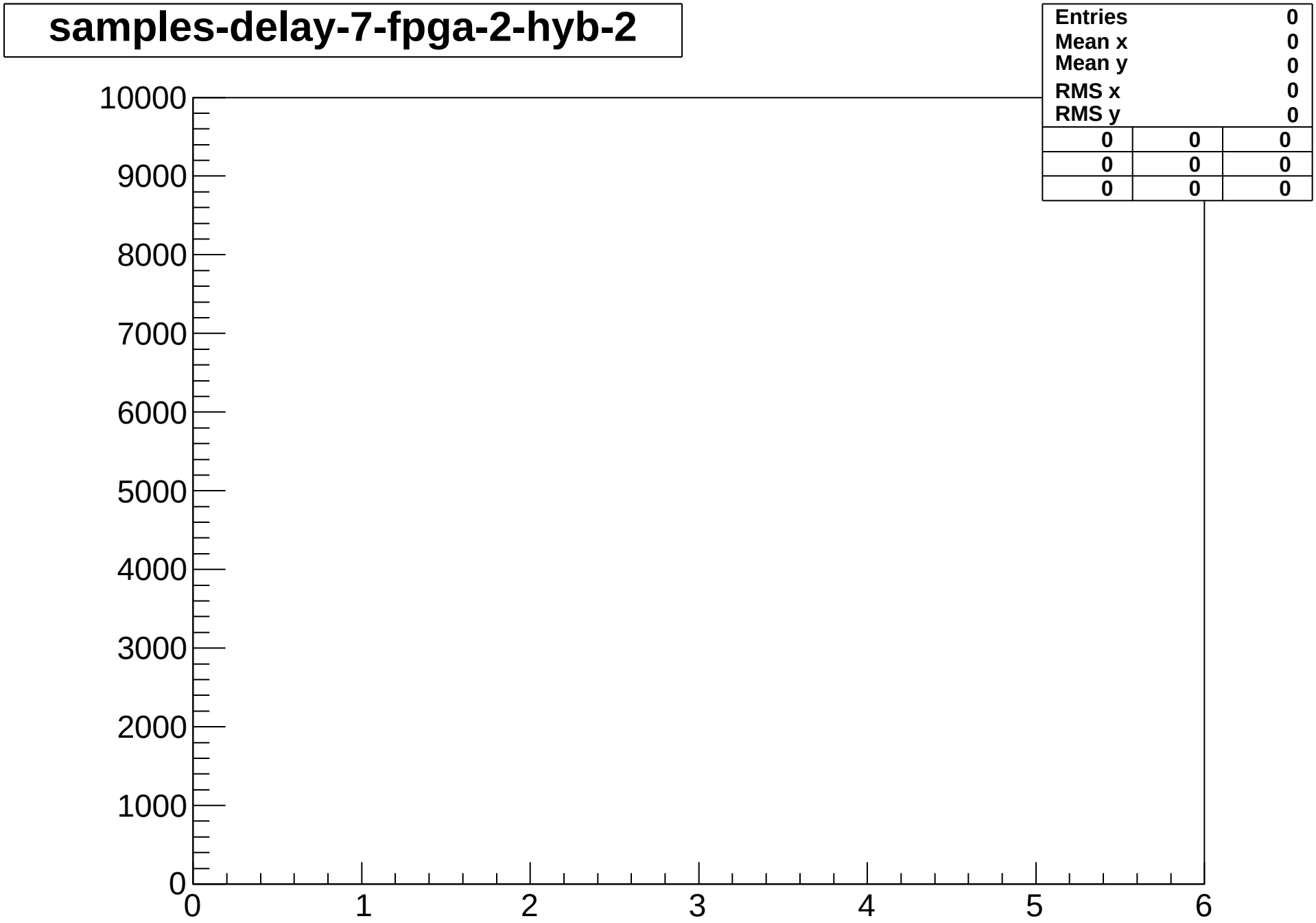
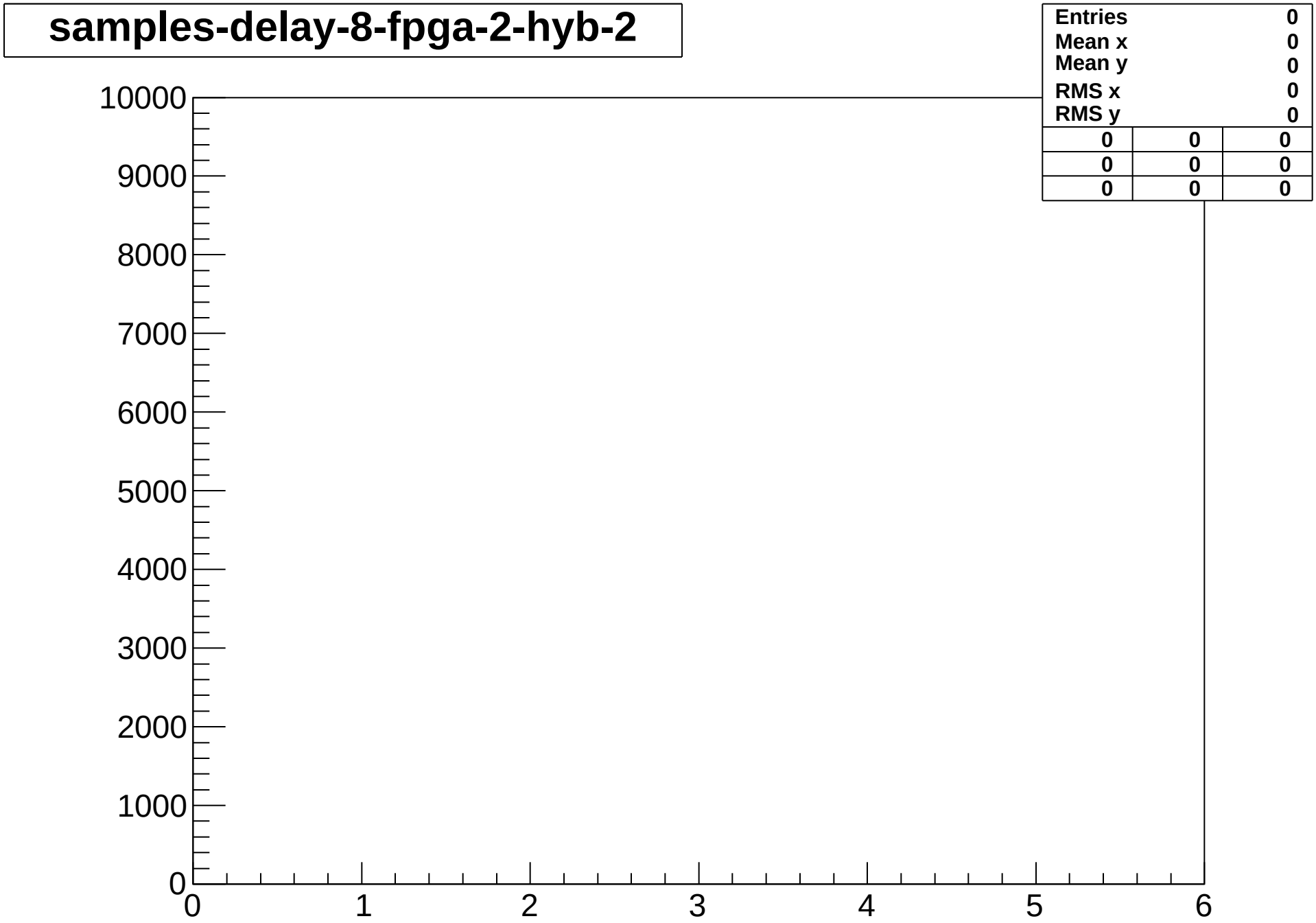
samples-delay-6-fpga-2-hyb-2



samples-delay-7-fpga-2-hyb-2




samples-delay-8-fpga-2-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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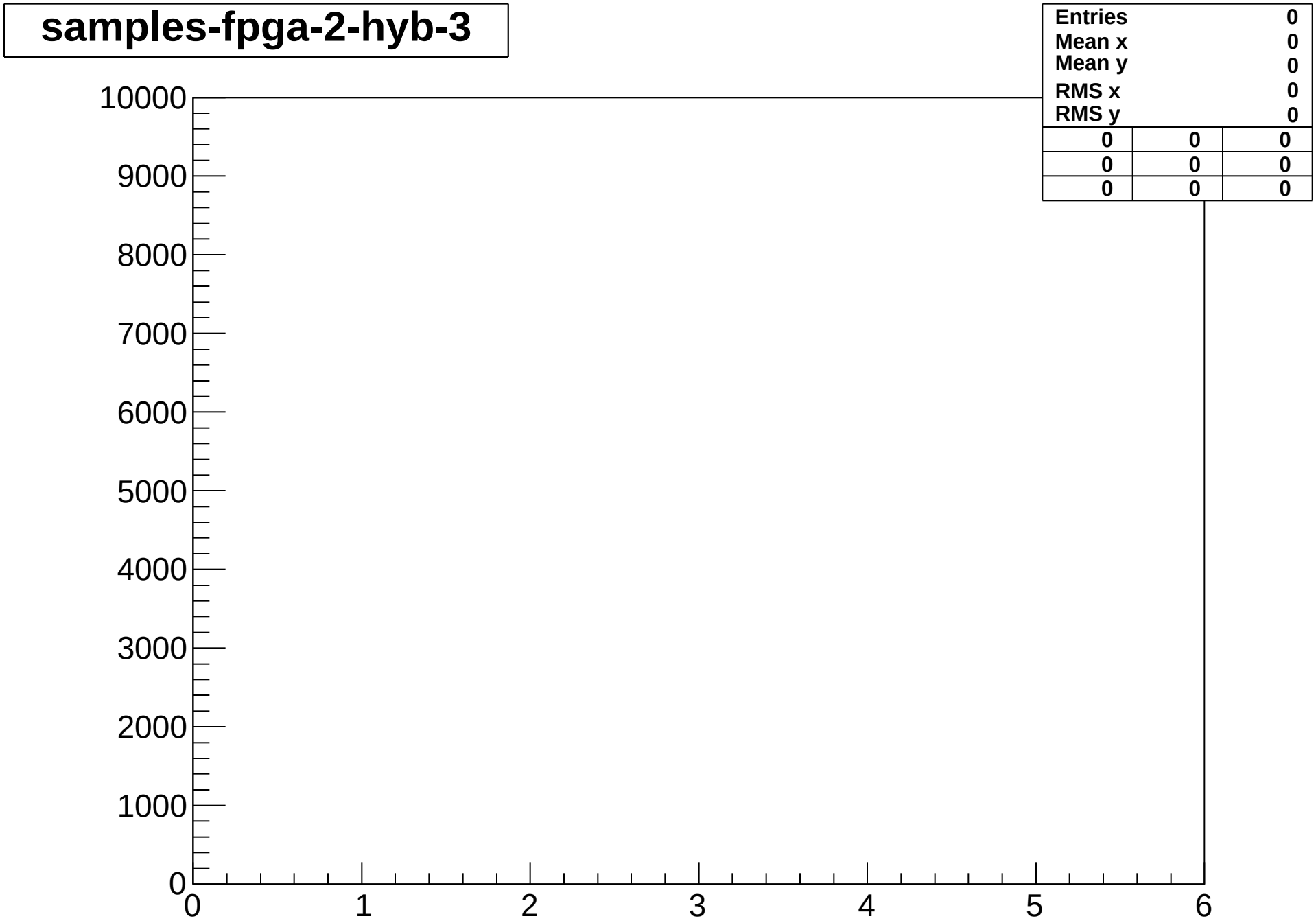
samples-fpga-2-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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7000
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5000
4000
3000
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1000
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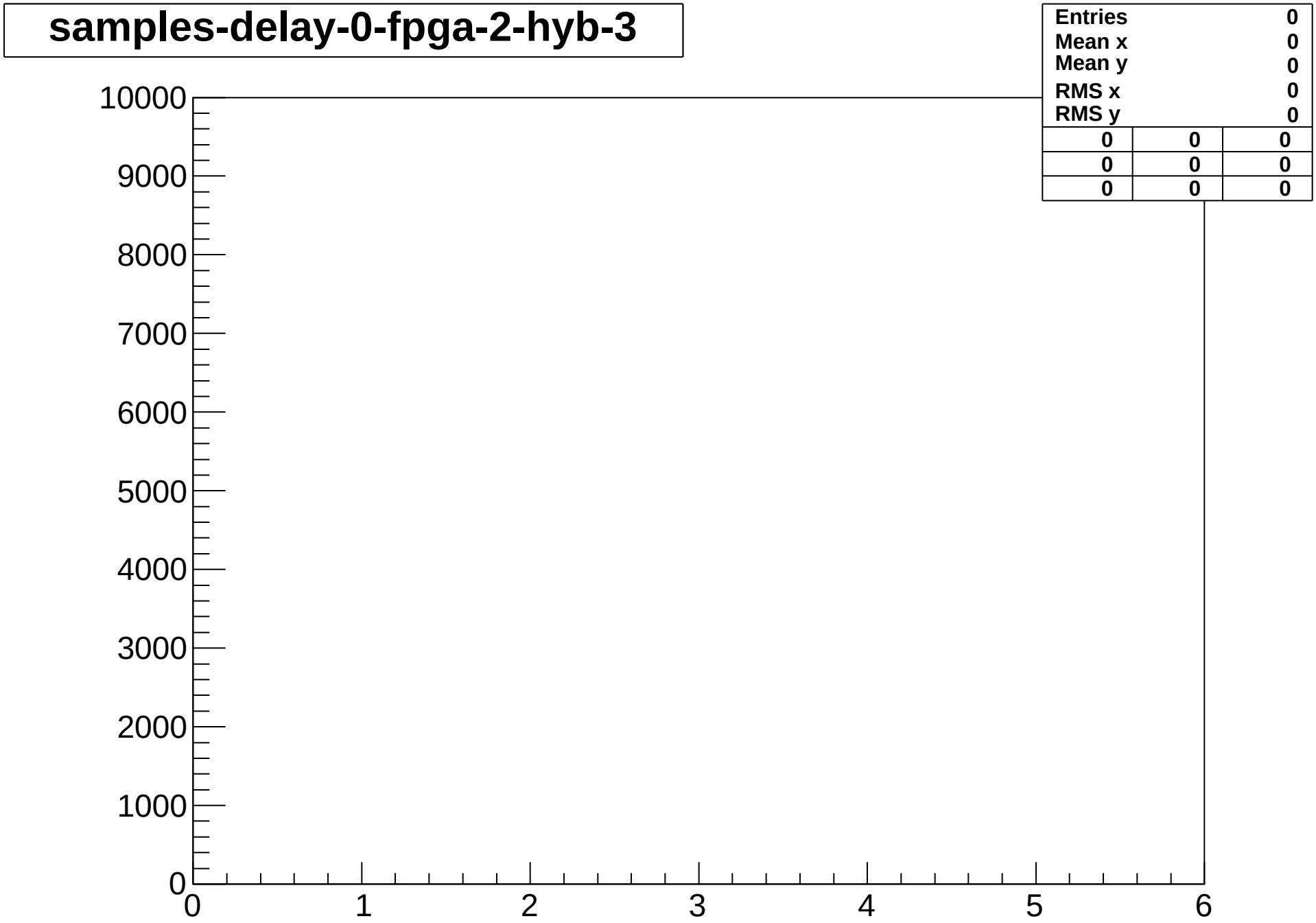
samples-delay-0-fpga-2-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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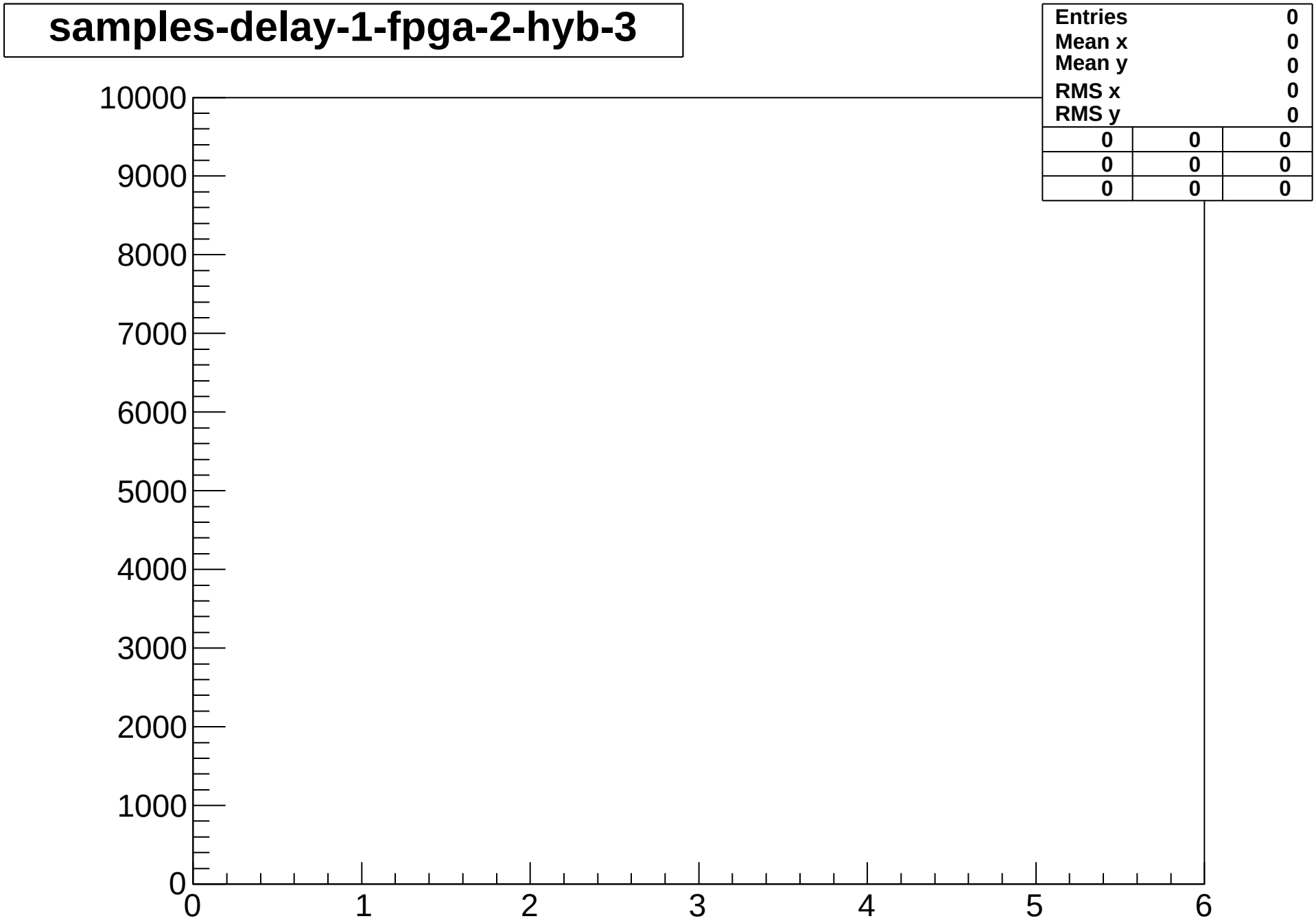
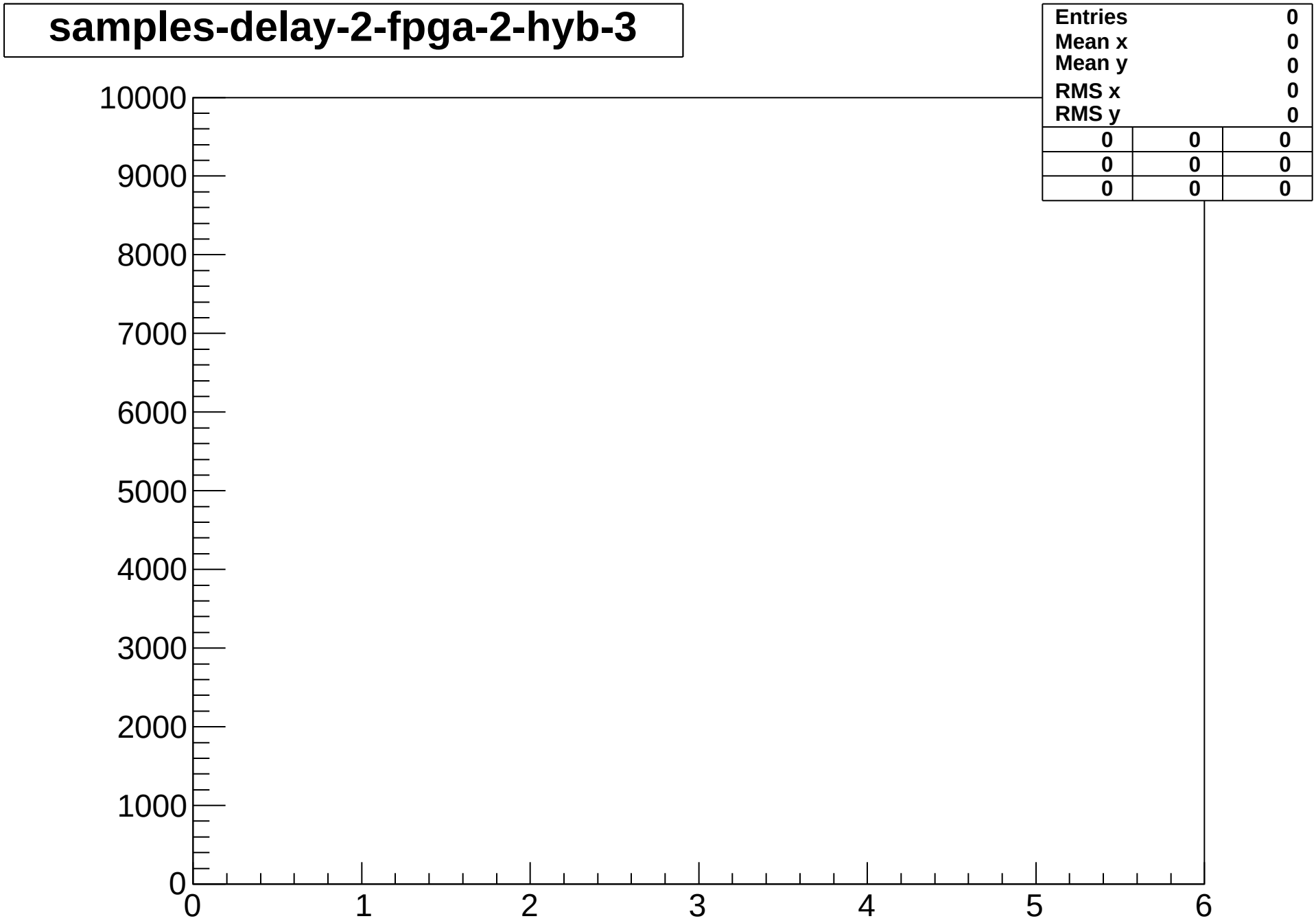
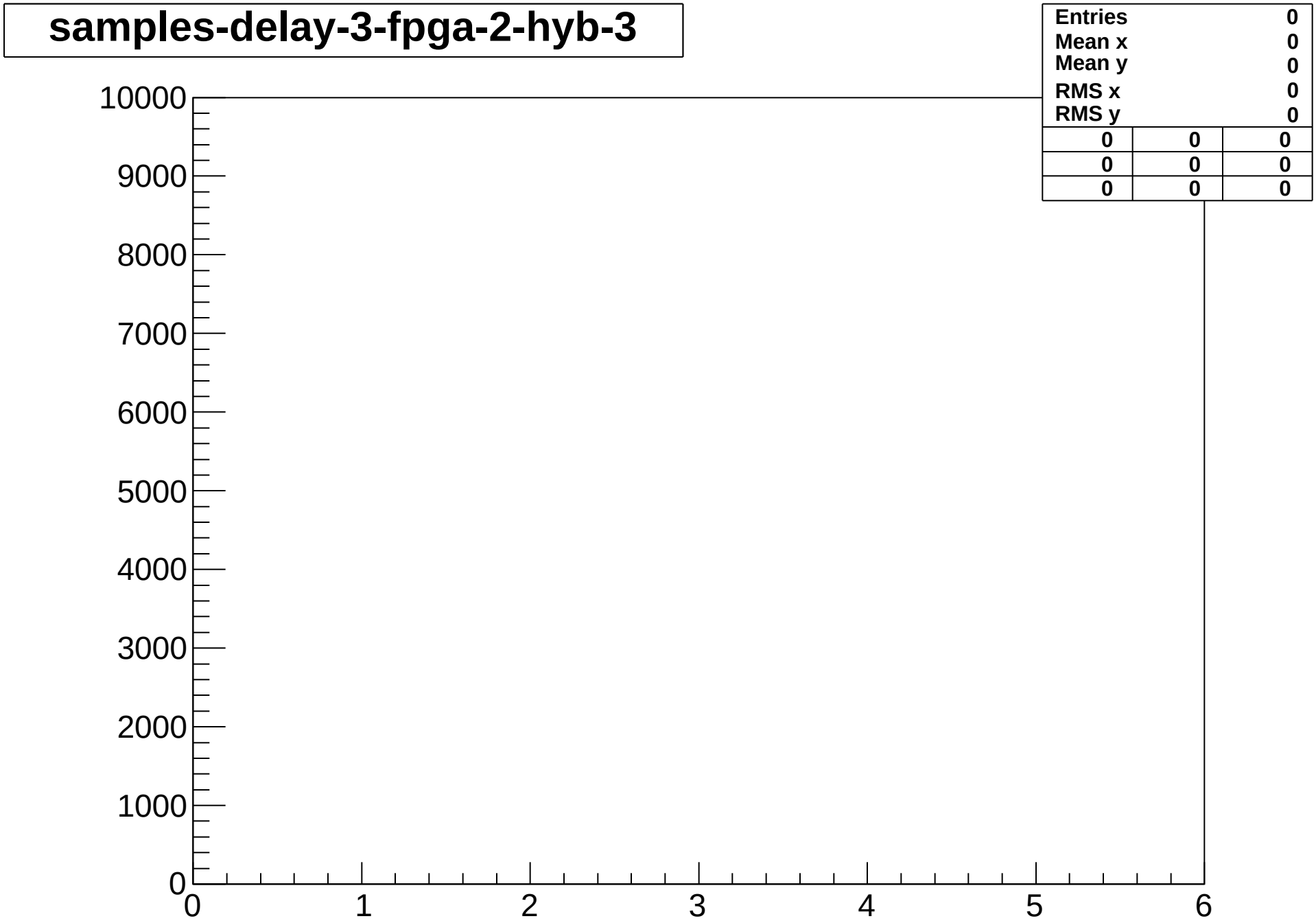
samples-delay-1-fpga-2-hyb-3



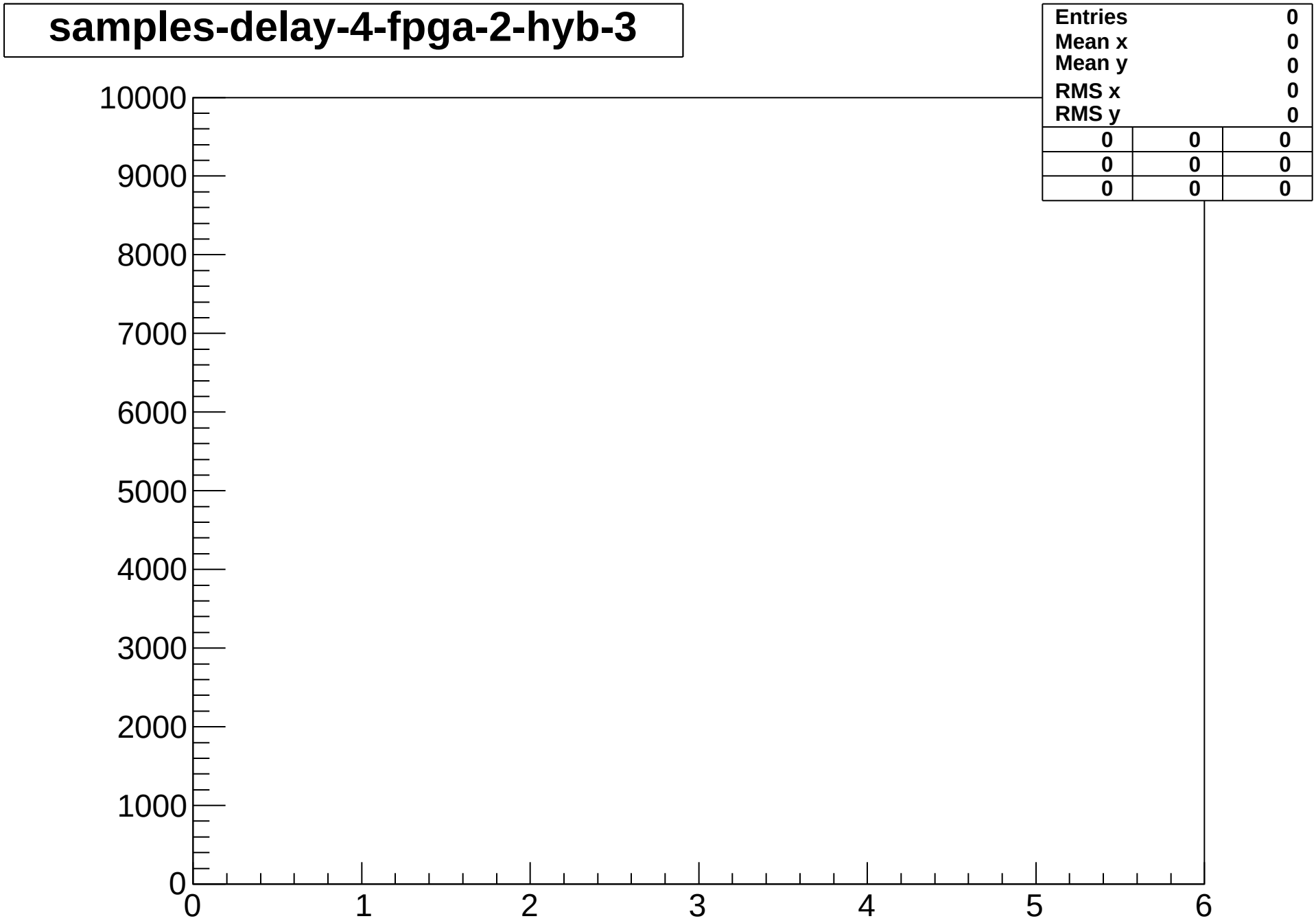
samples-delay-2-fpga-2-hyb-3



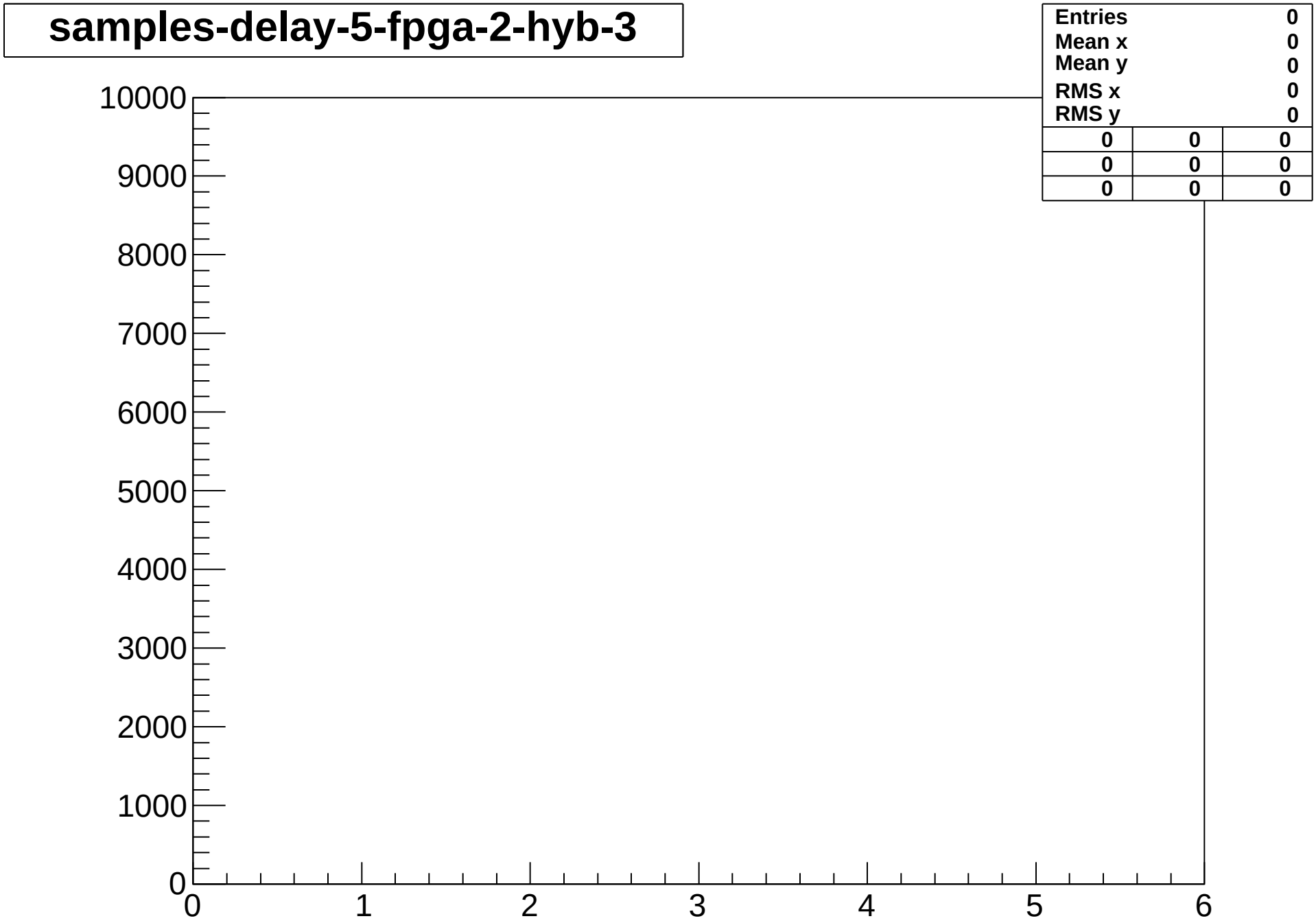
samples-delay-3-fpga-2-hyb-3

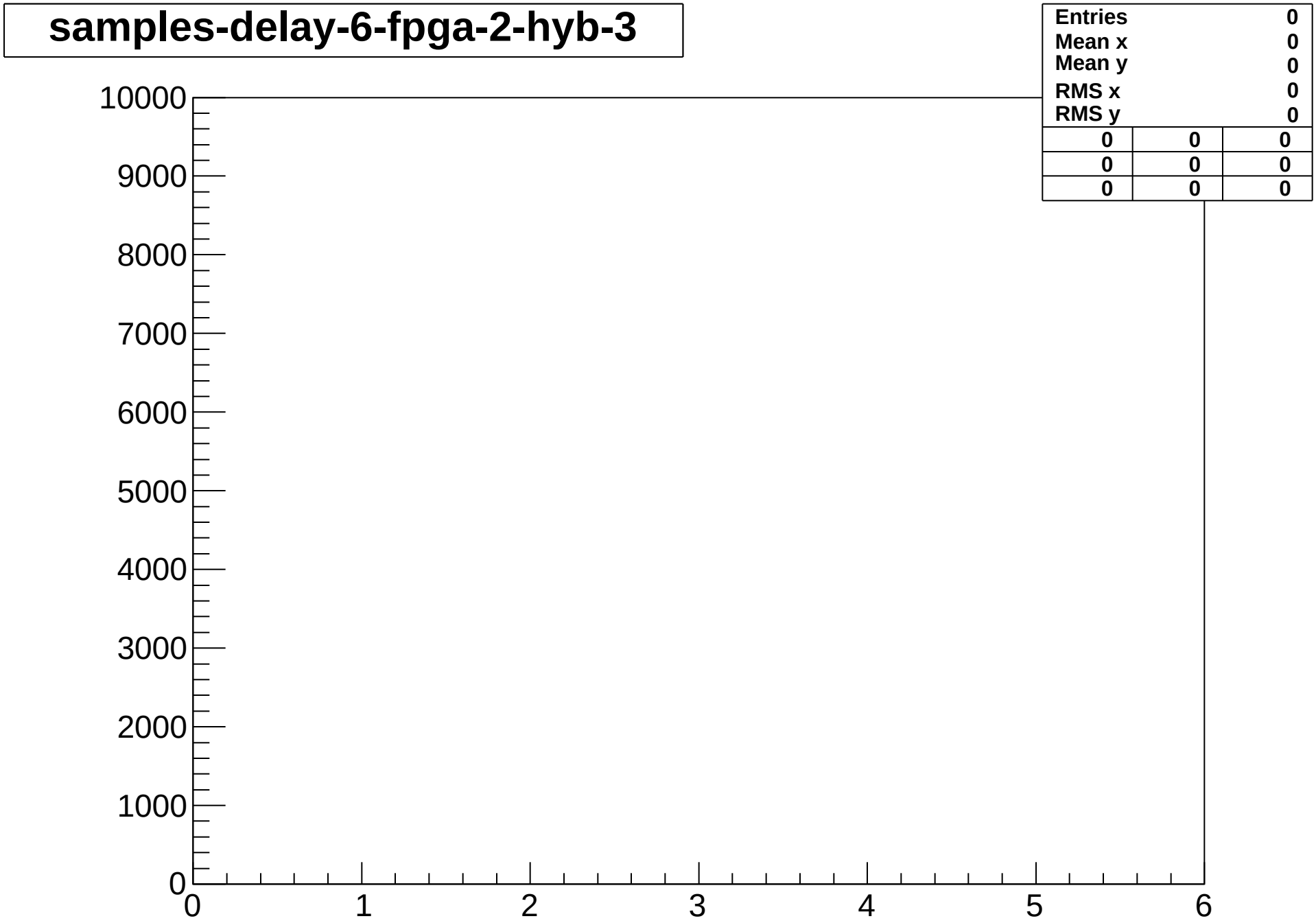


samples-delay-4-fpga-2-hyb-3



samples-delay-5-fpga-2-hyb-3




samples-delay-6-fpga-2-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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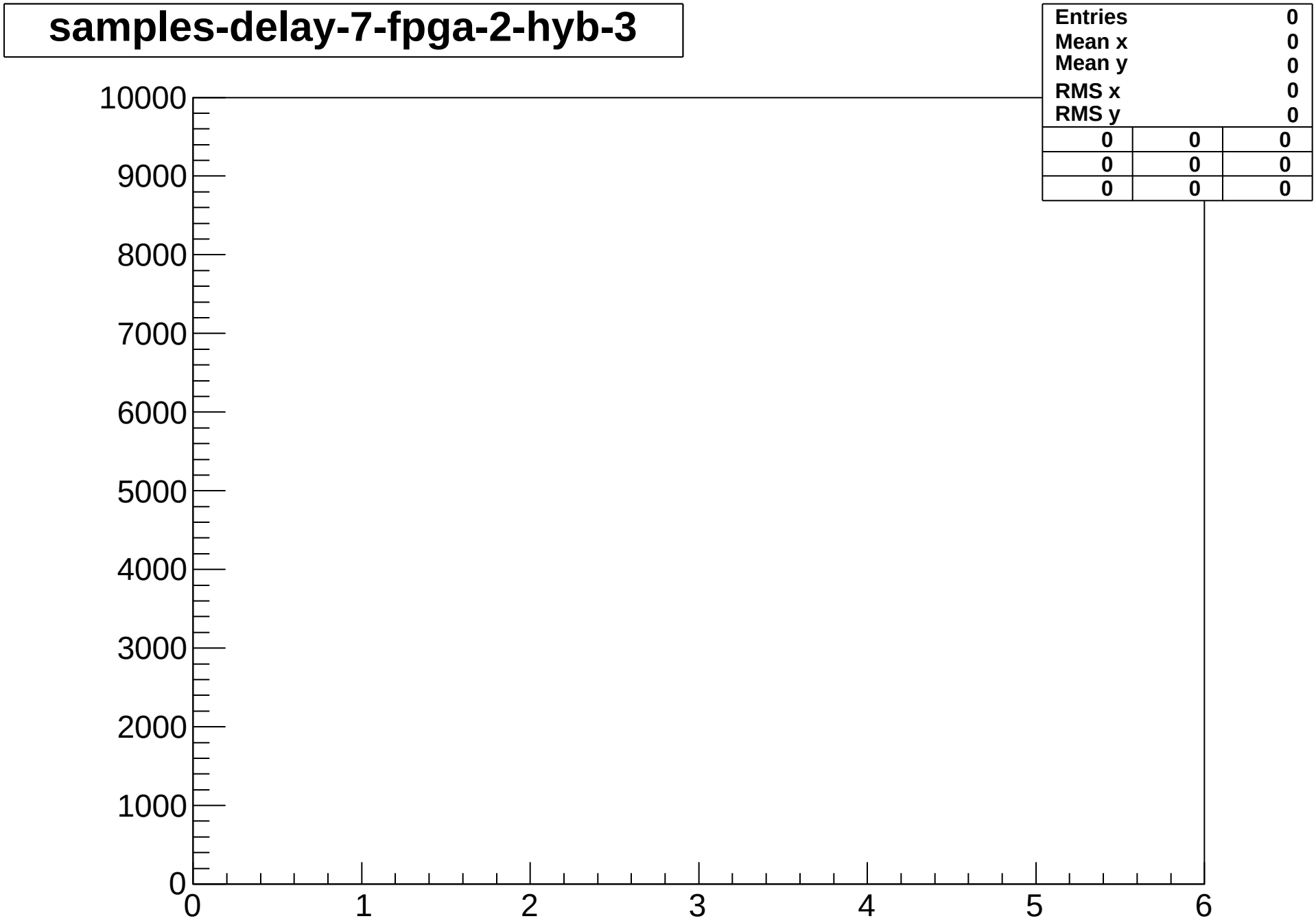
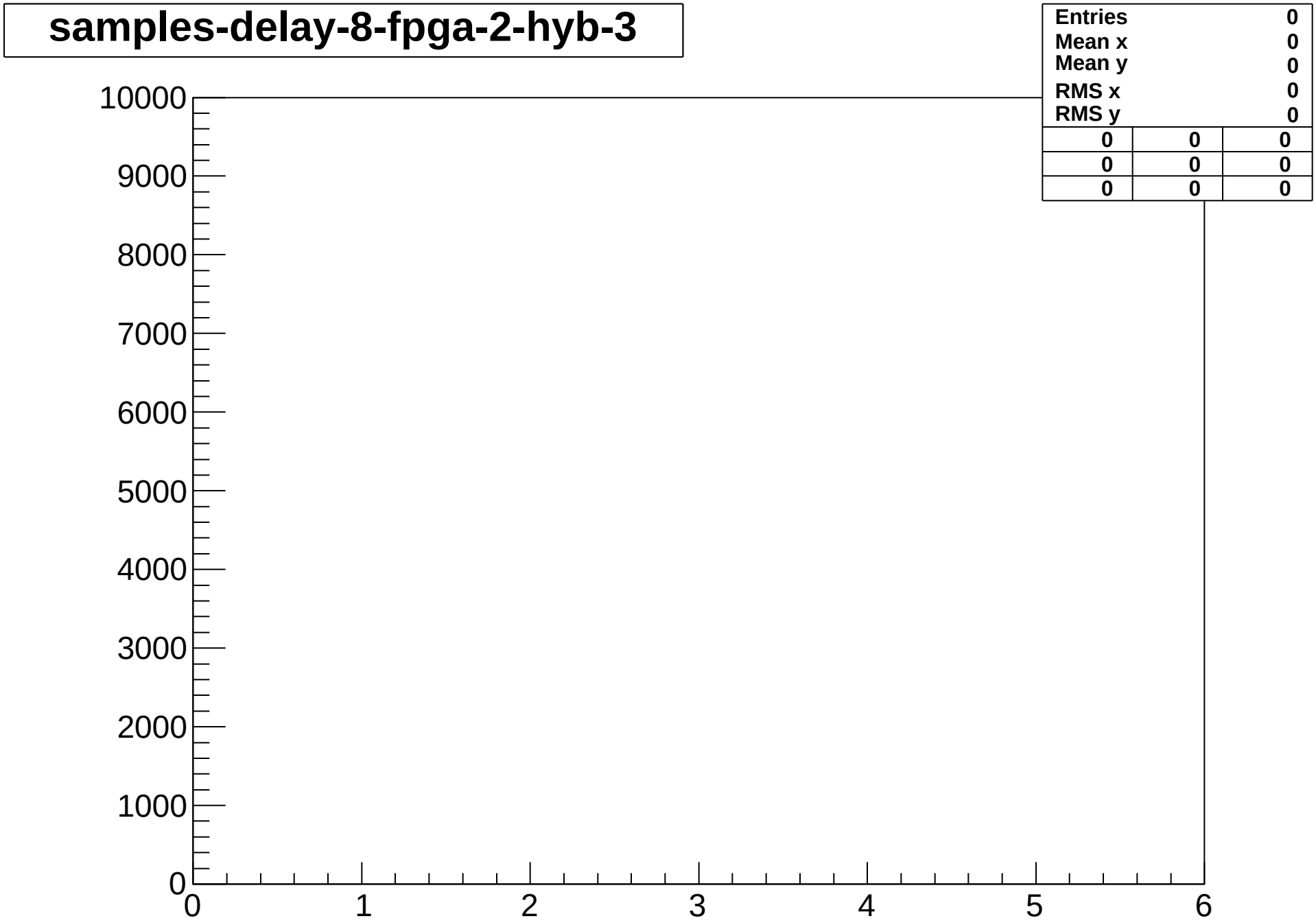
samples-delay-7-fpga-2-hyb-3




samples-delay-8-fpga-2-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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3000
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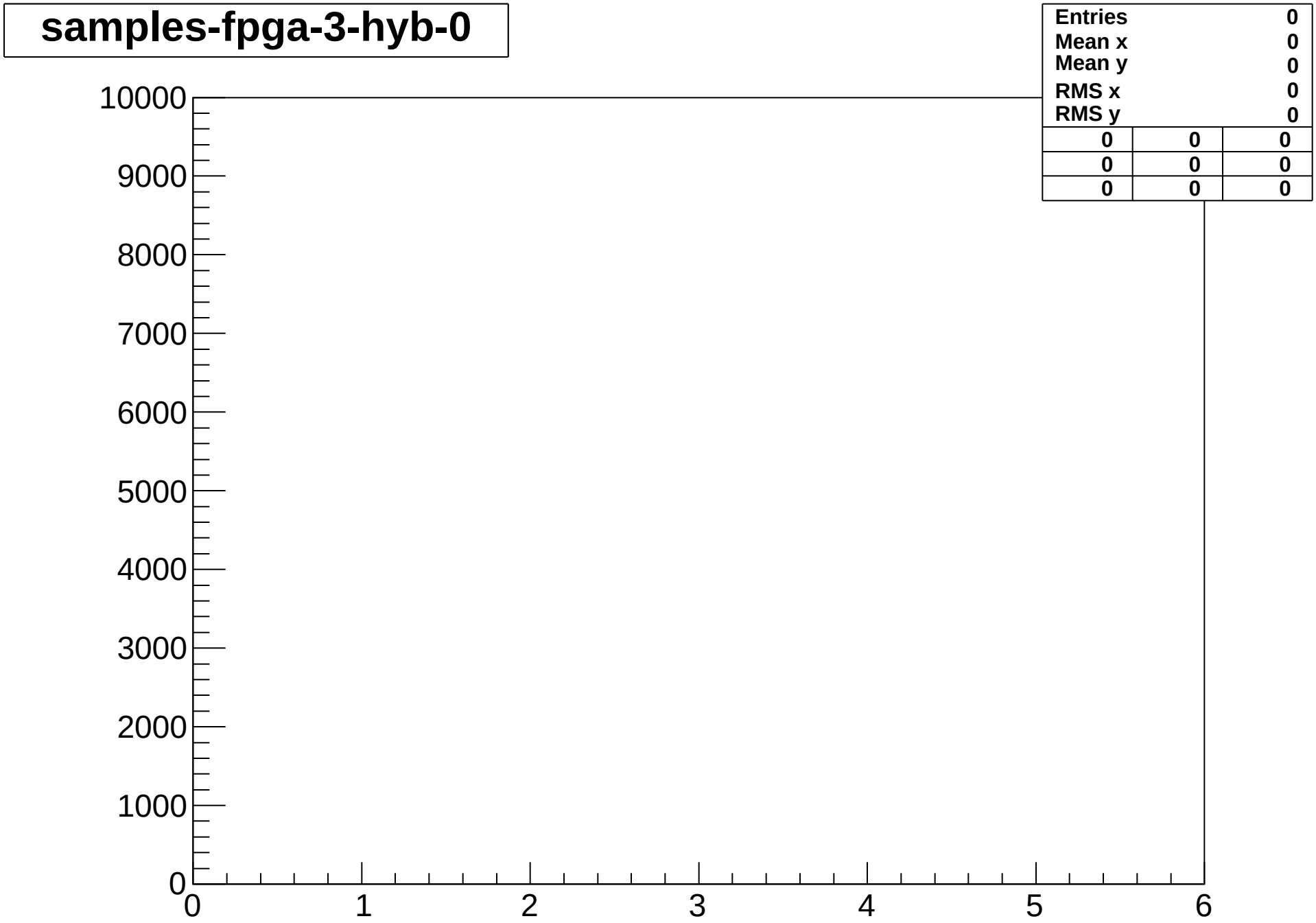
samples-fpga-3-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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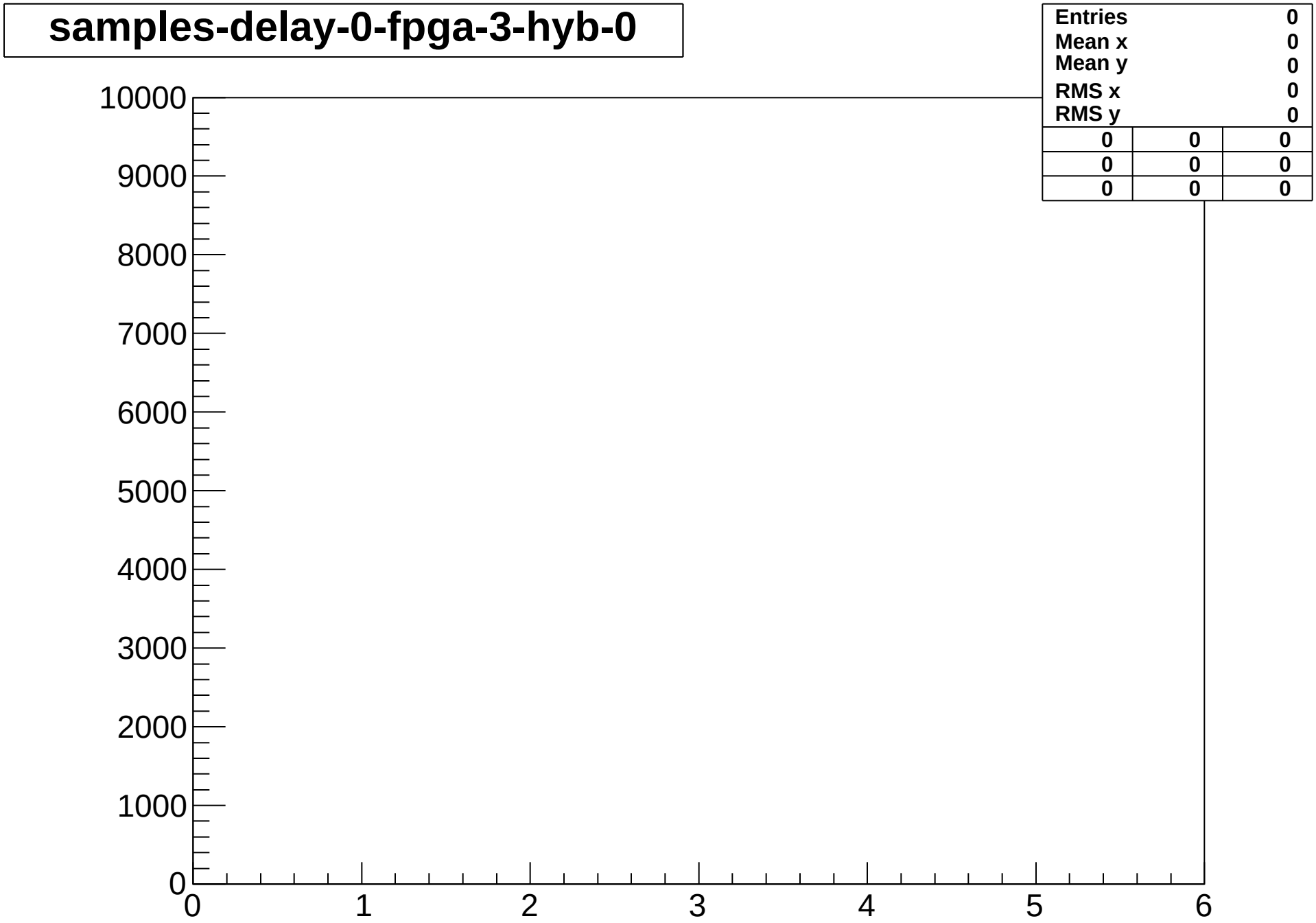
samples-delay-0-fpga-3-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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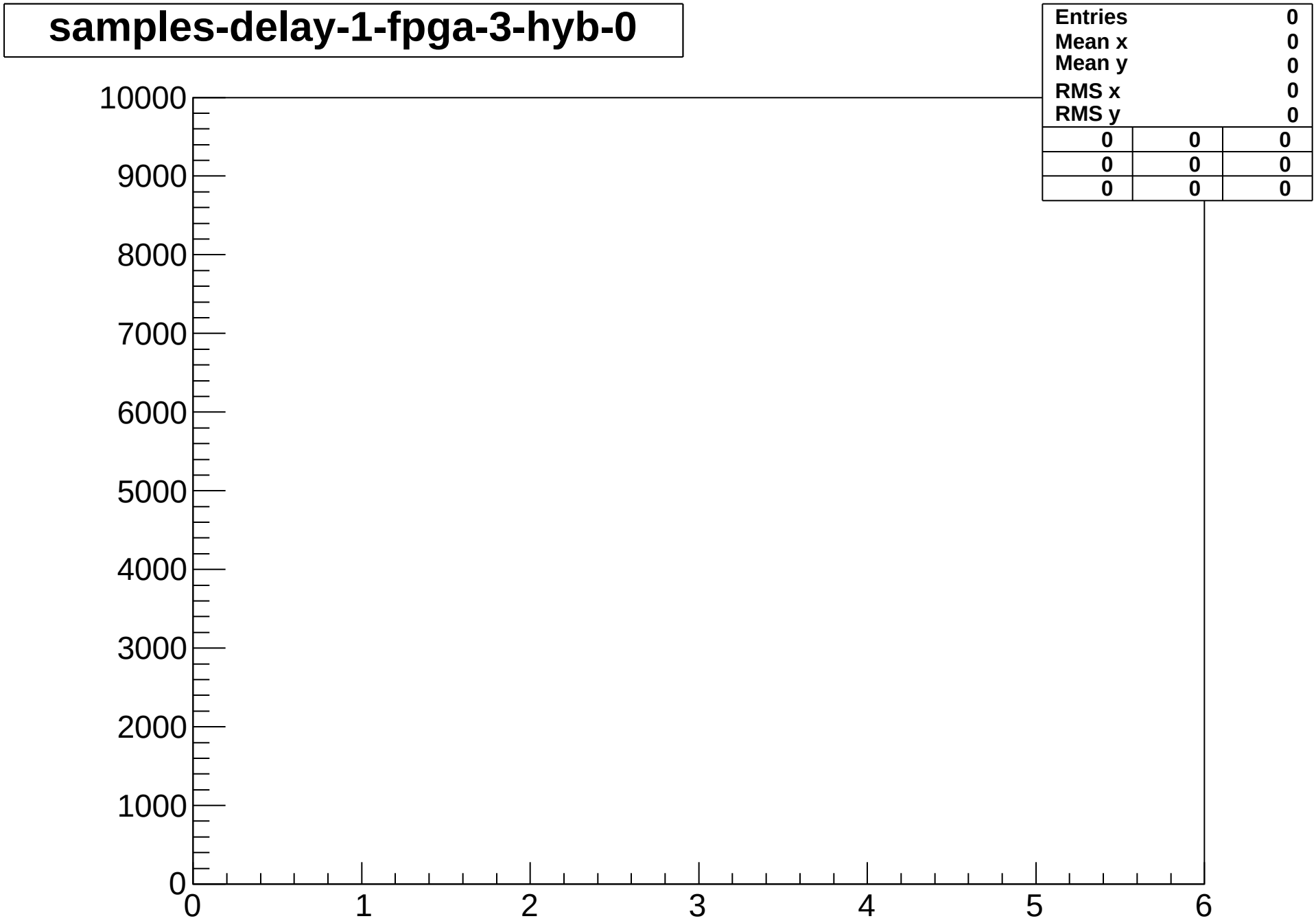
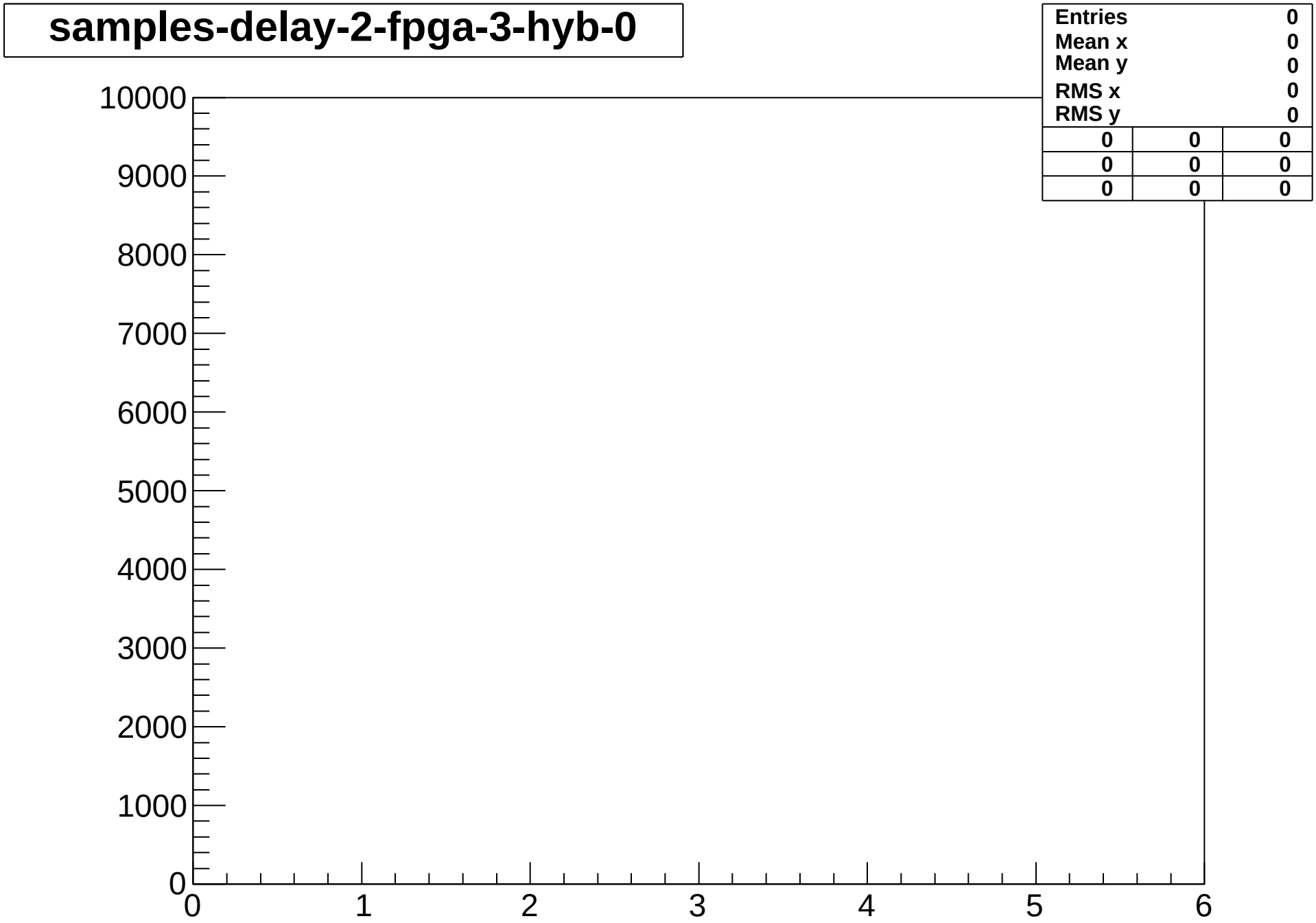
samples-delay-1-fpga-3-hyb-0




samples-delay-2-fpga-3-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
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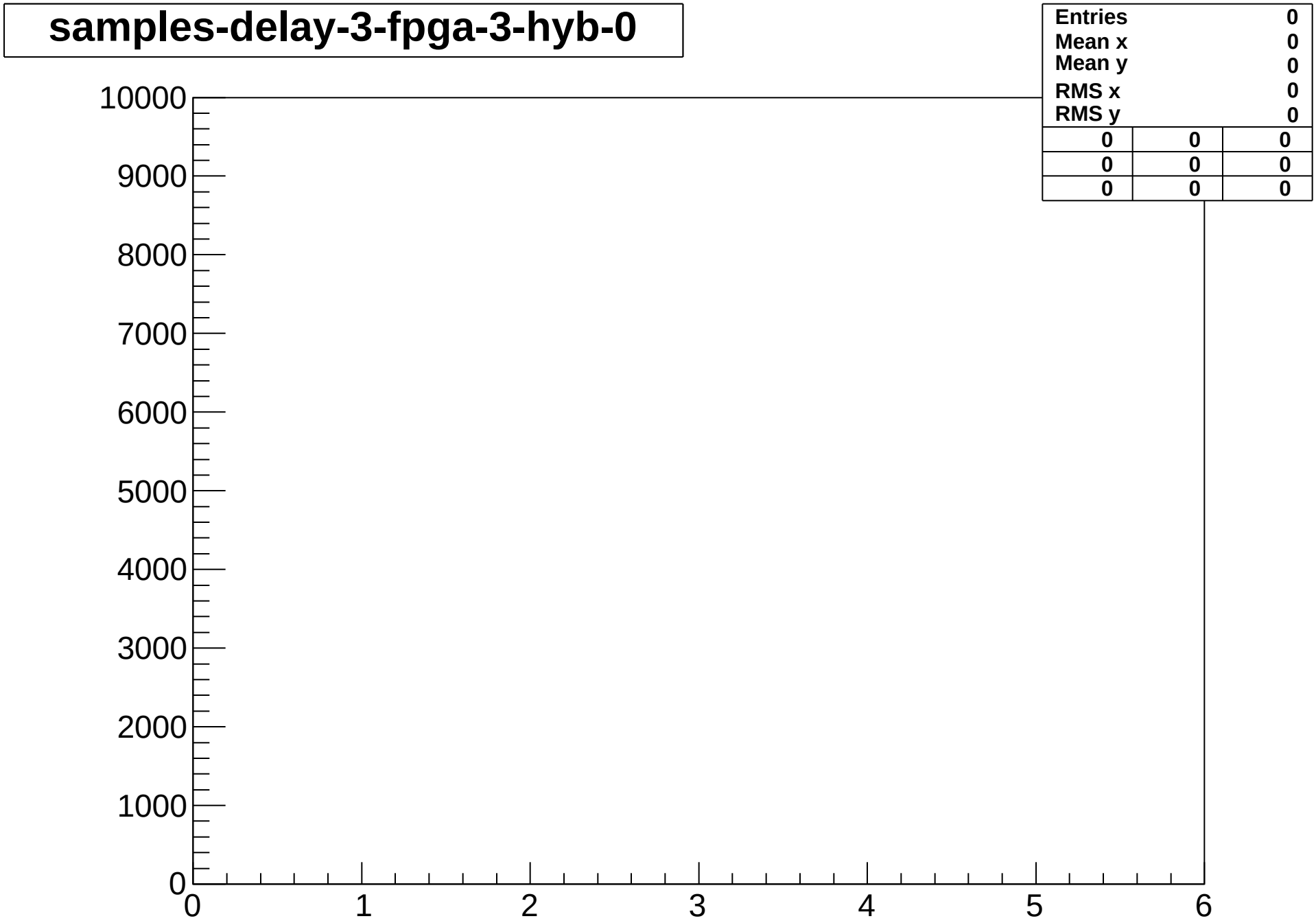
samples-delay-3-fpga-3-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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1000
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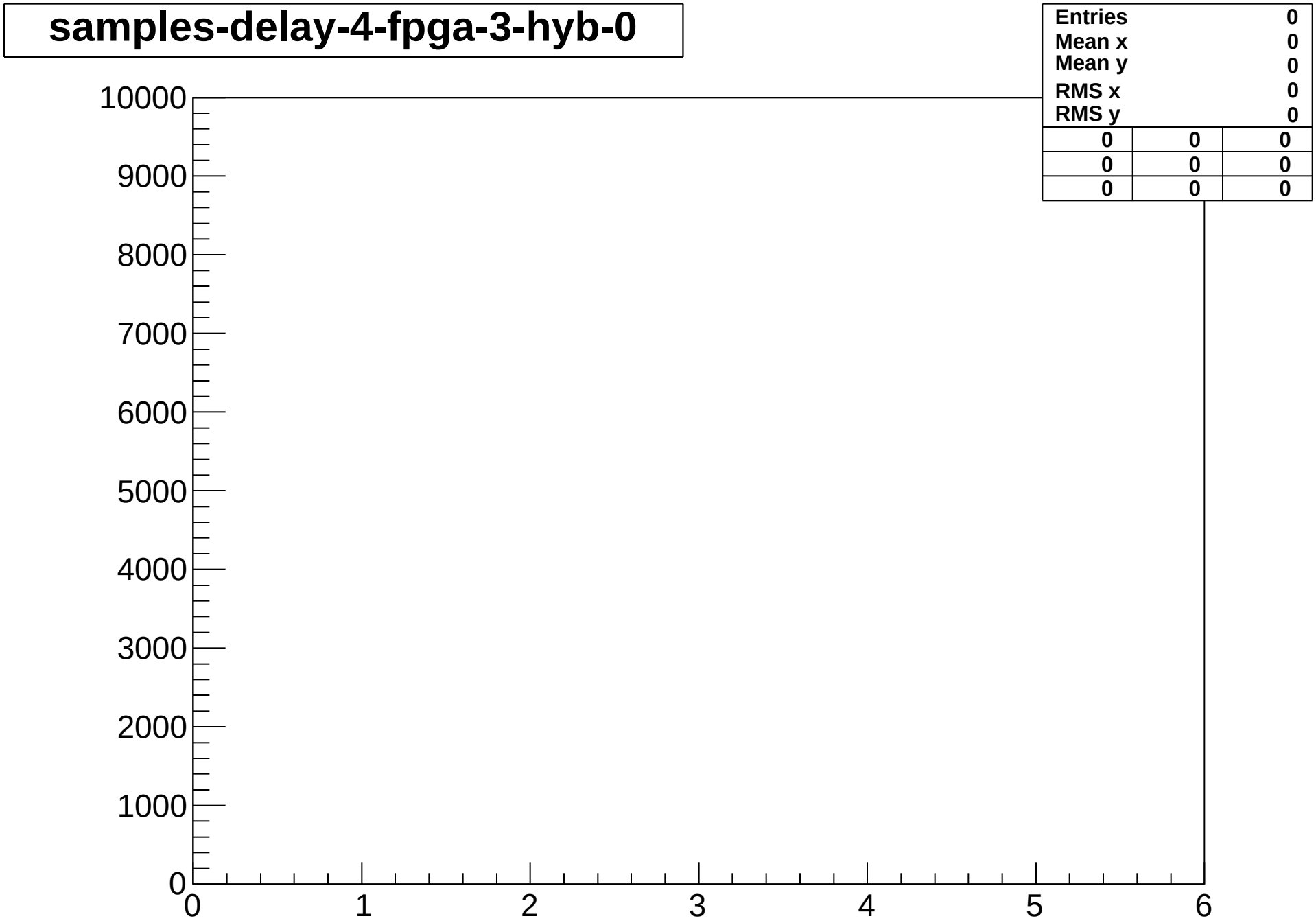
samples-delay-4-fpga-3-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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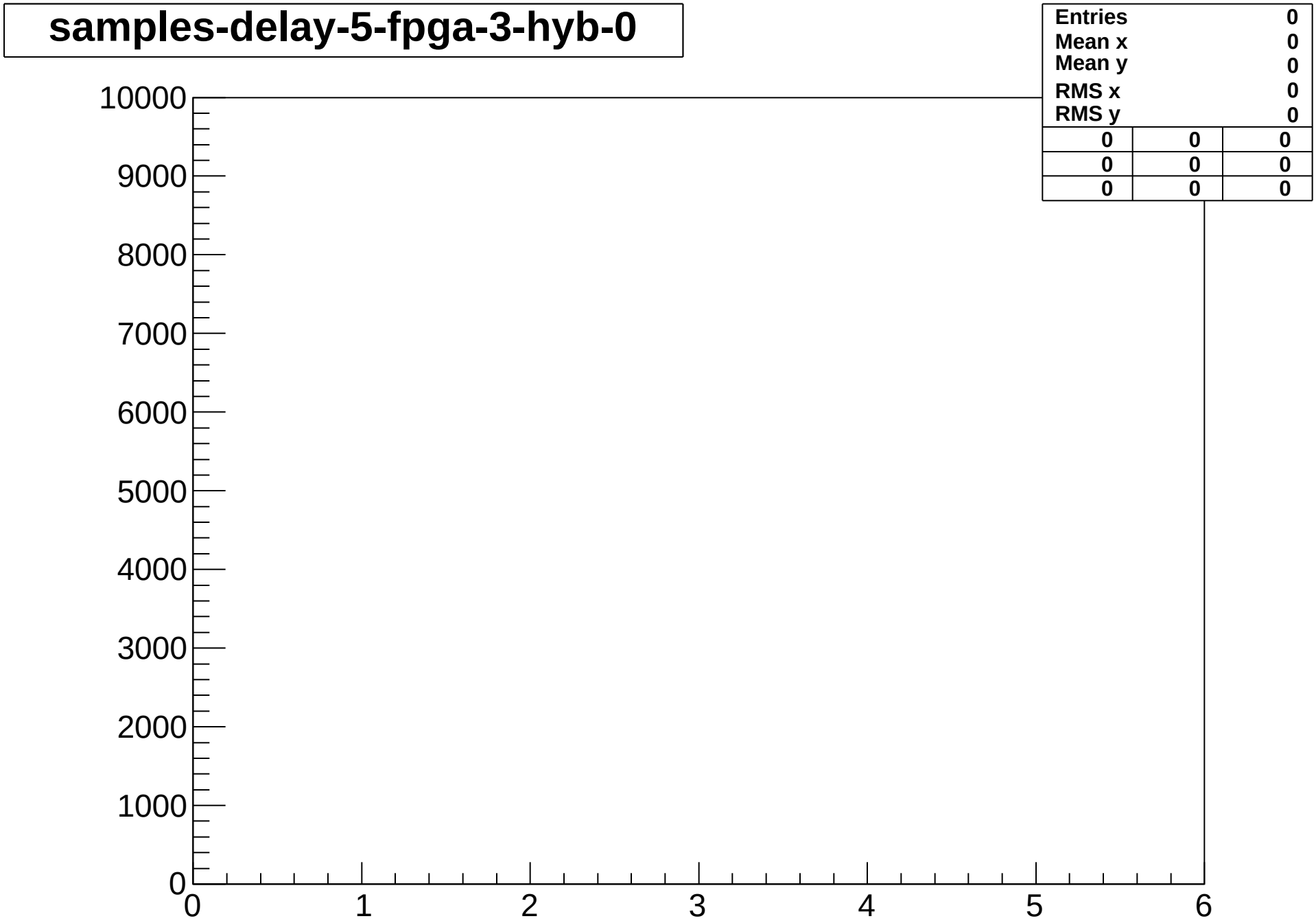
samples-delay-5-fpga-3-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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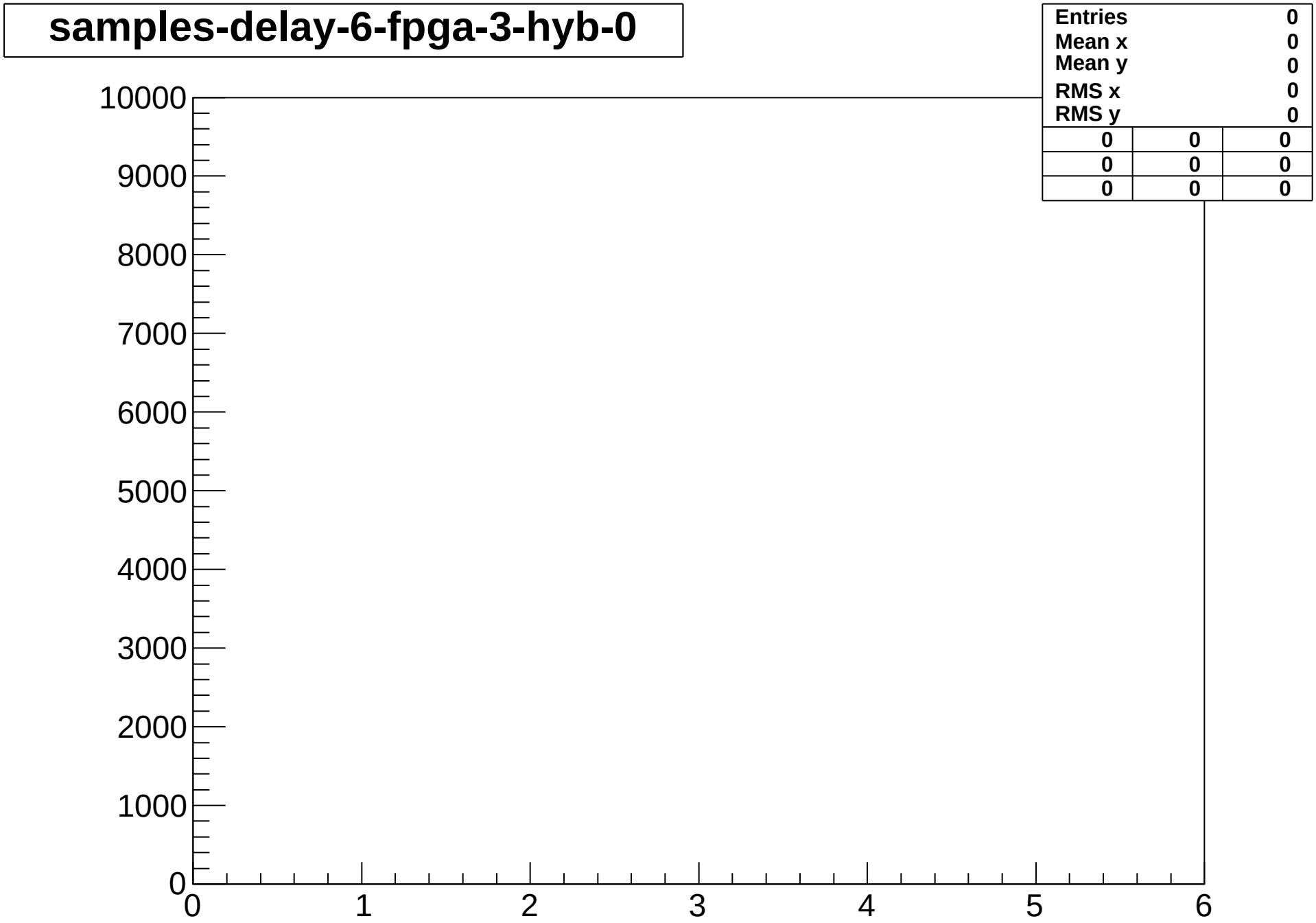
samples-delay-6-fpga-3-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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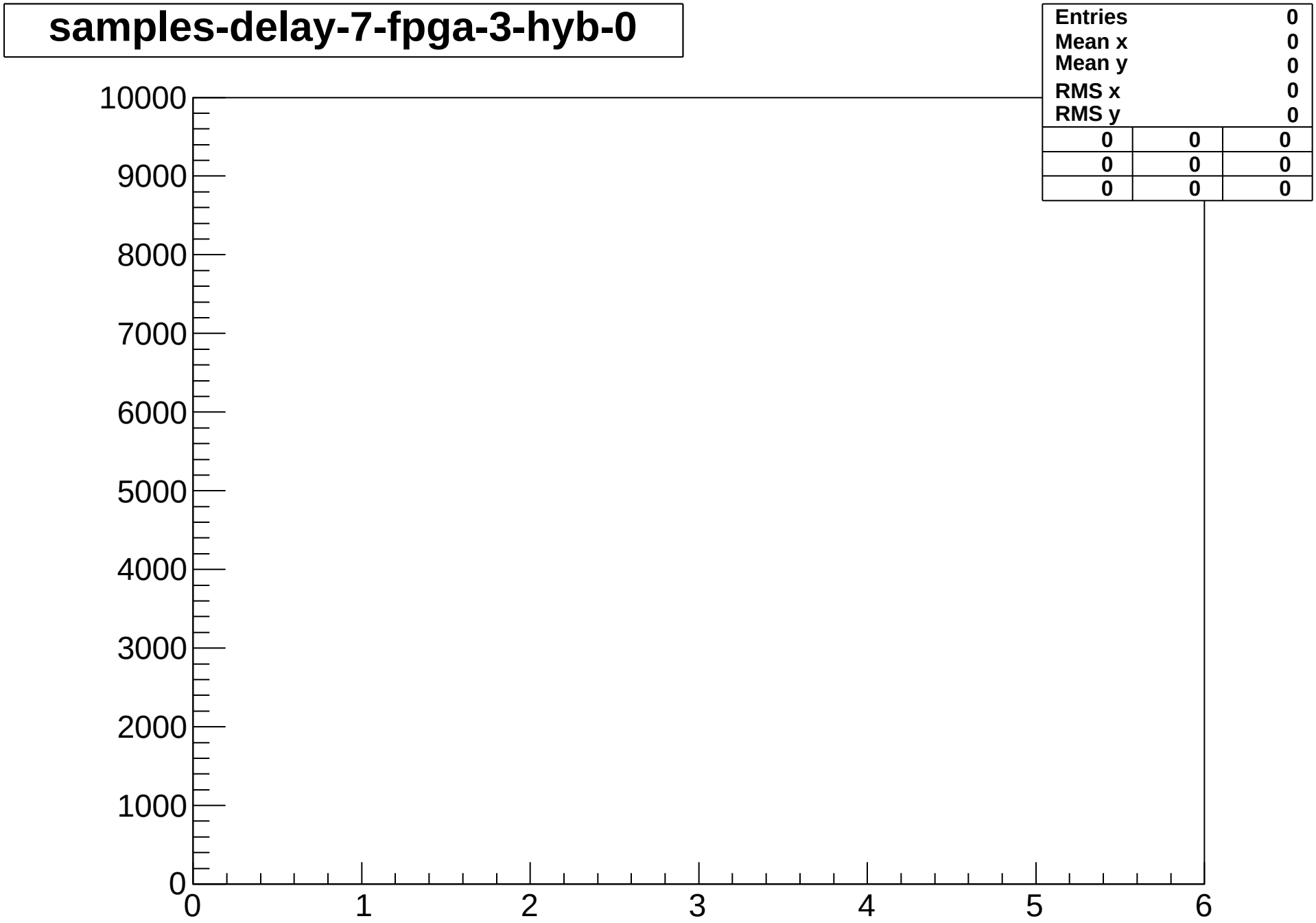
samples-delay-7-fpga-3-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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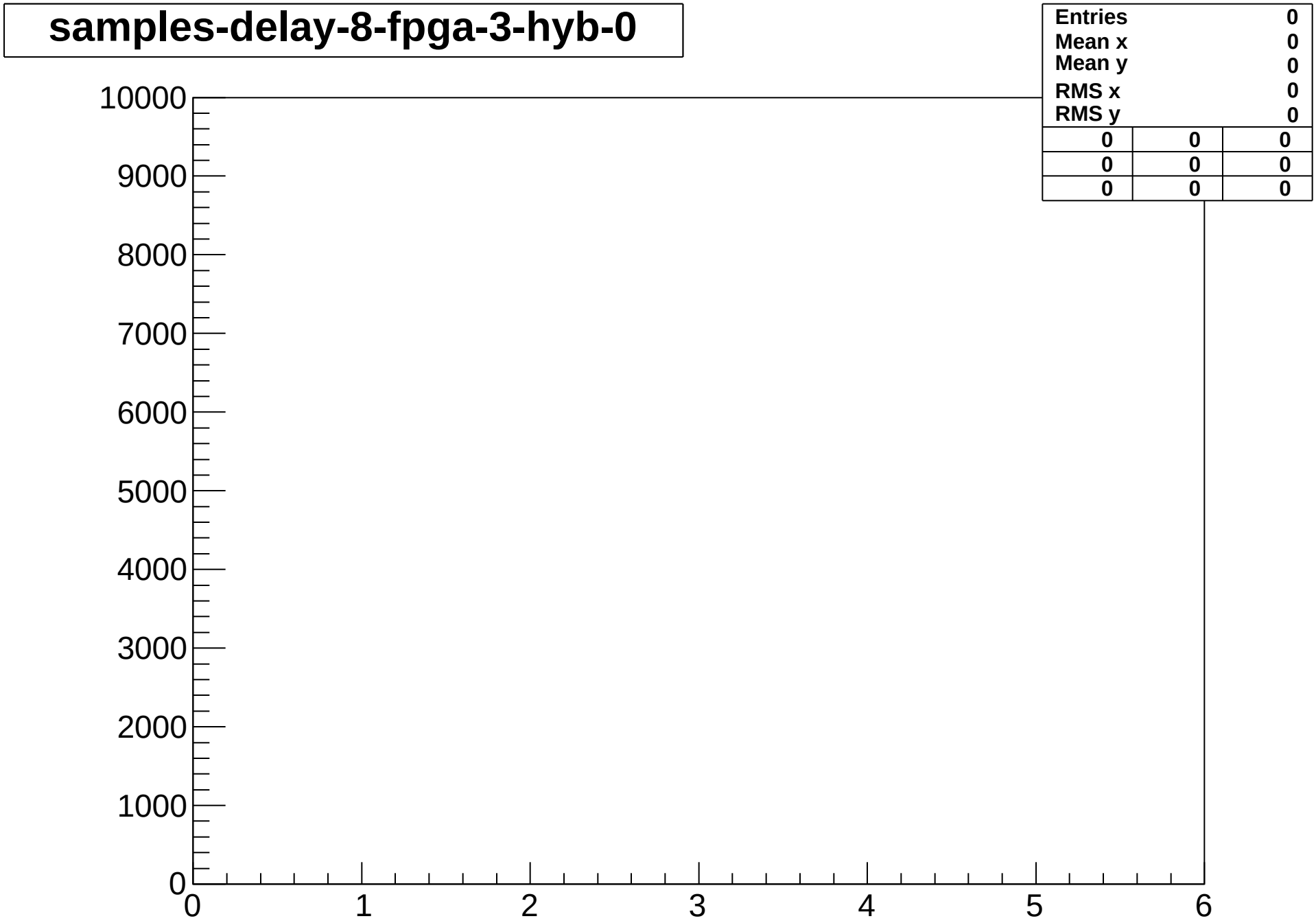
samples-delay-8-fpga-3-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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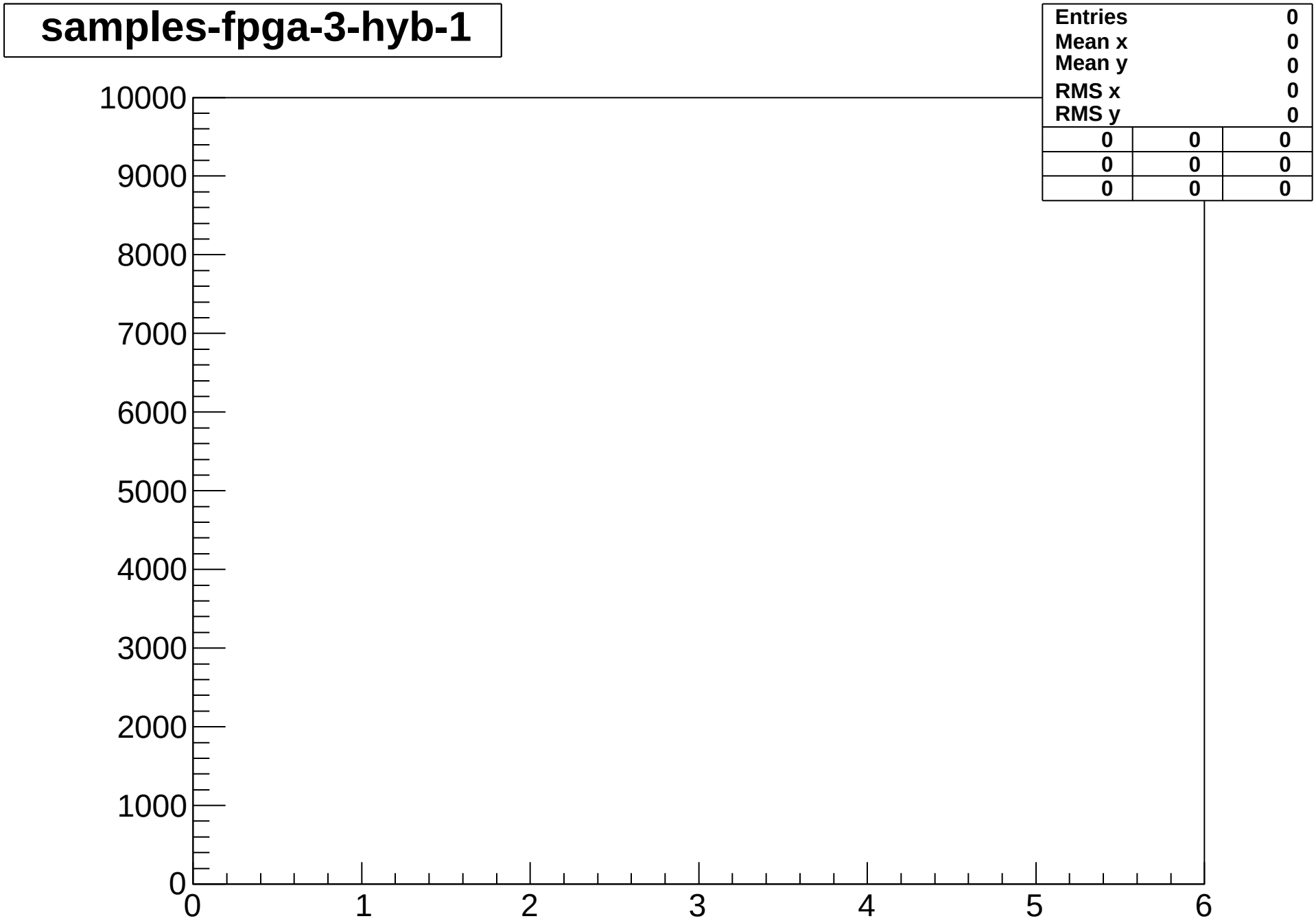
samples-fpga-3-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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7000
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5000
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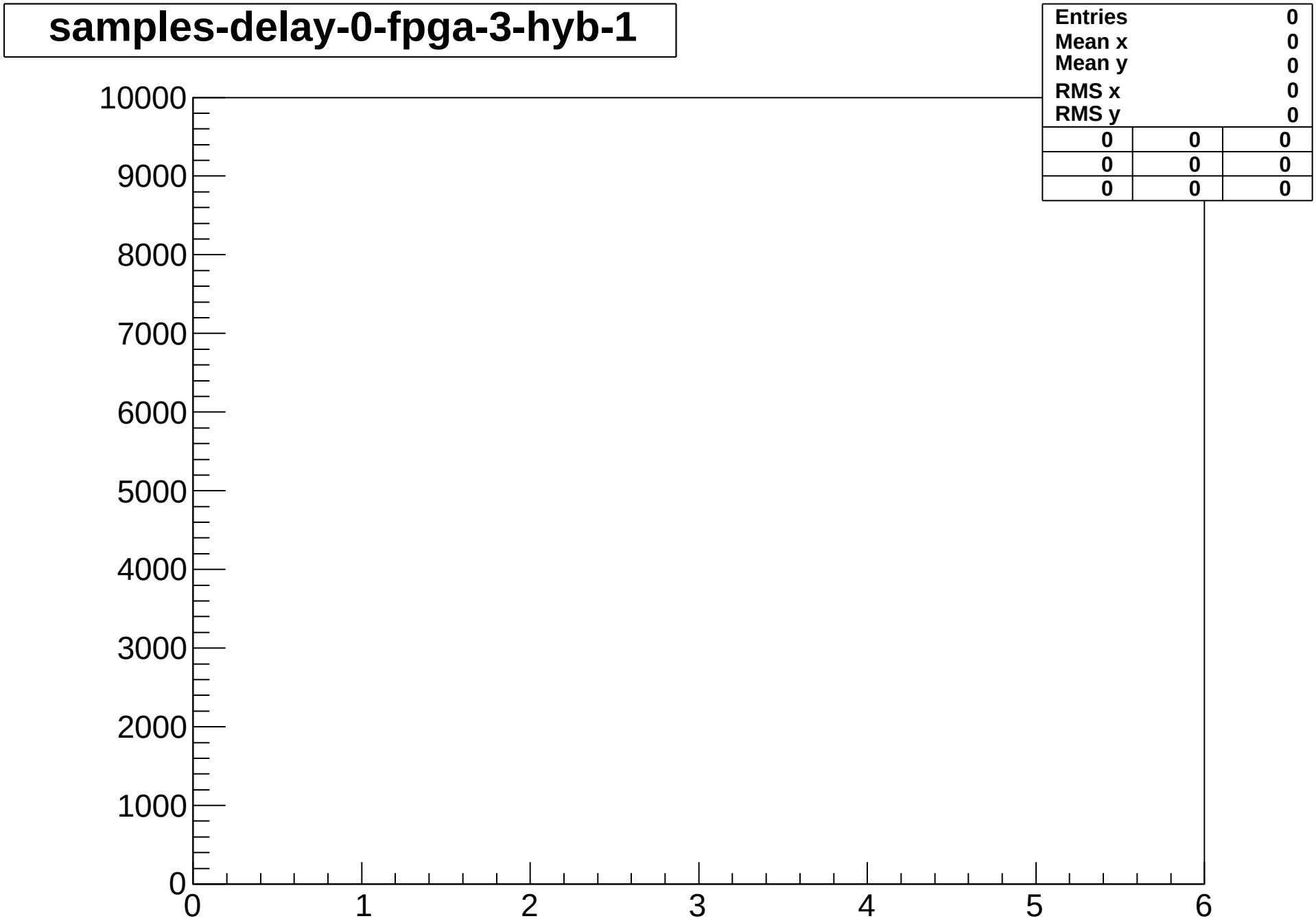
samples-delay-0-fpga-3-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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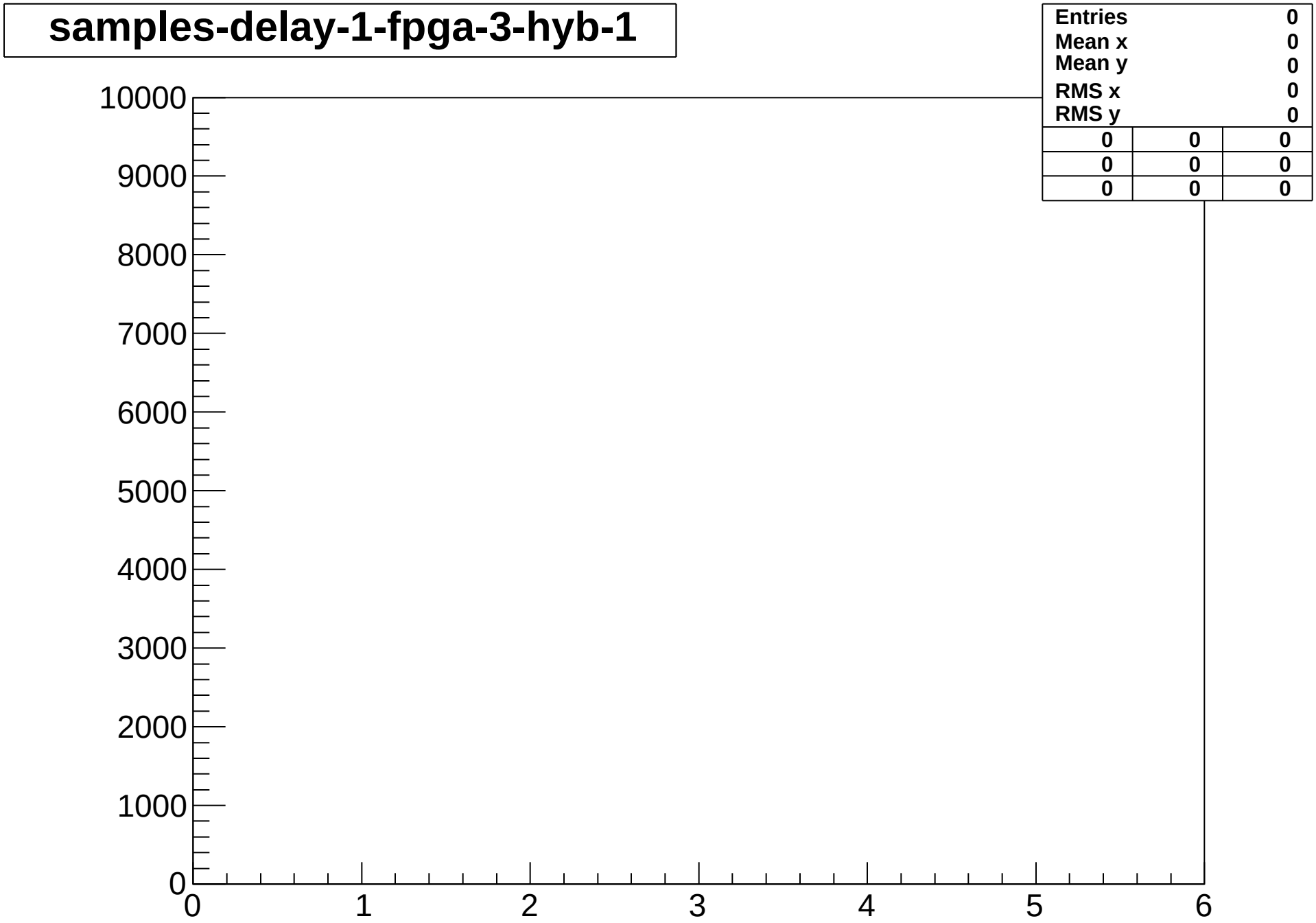
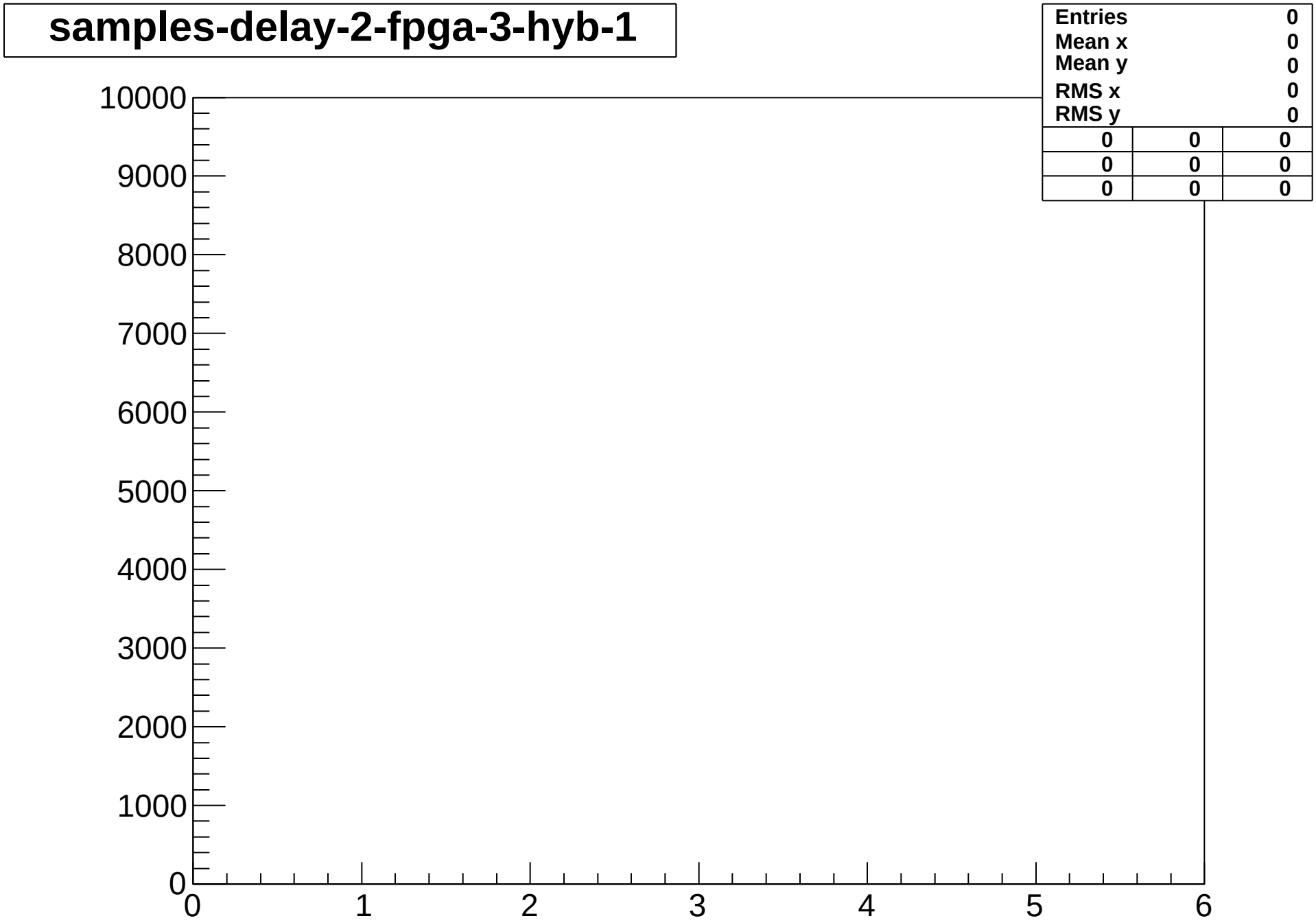
samples-delay-1-fpga-3-hyb-1




samples-delay-2-fpga-3-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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6000
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4000
3000
2000
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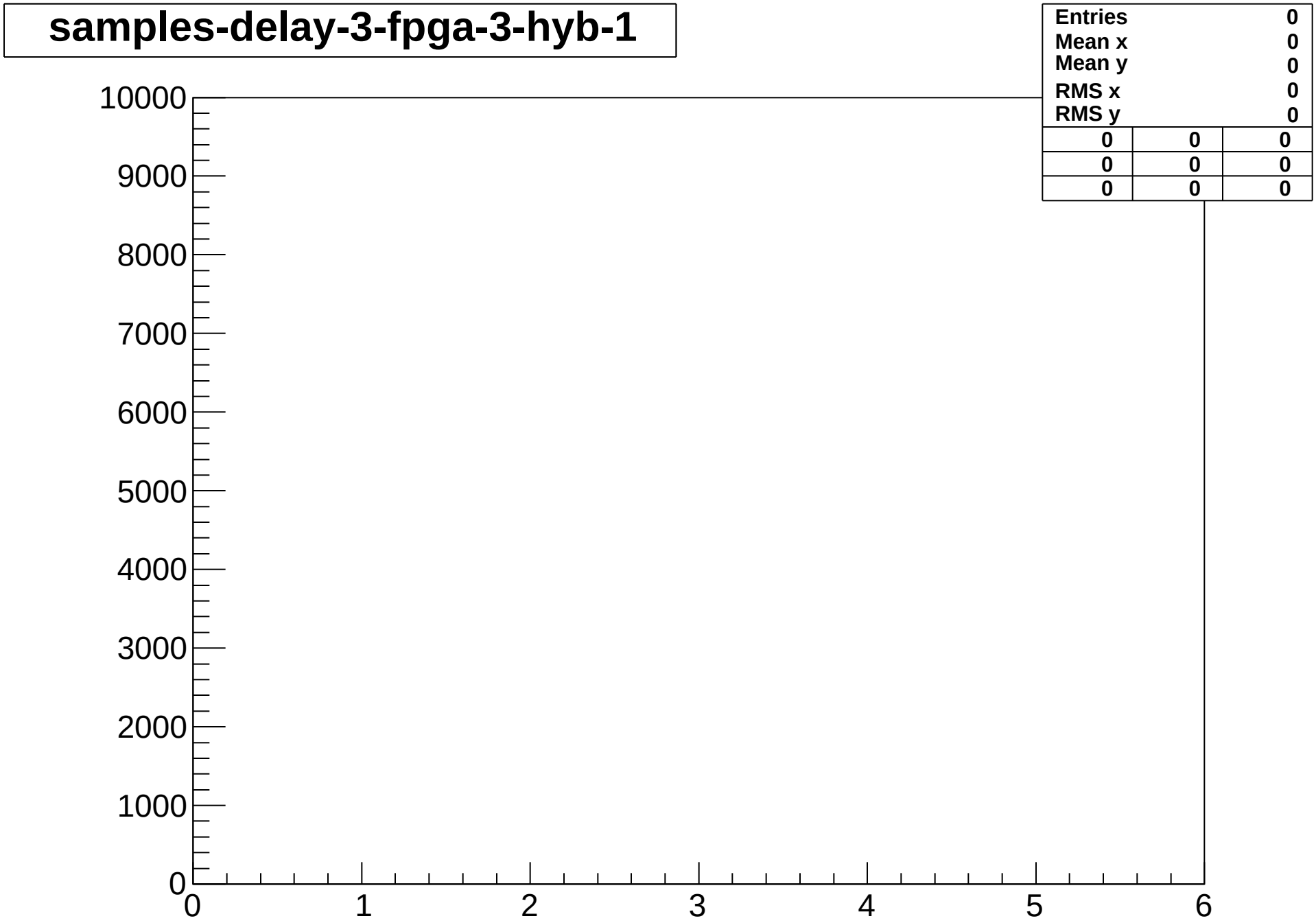
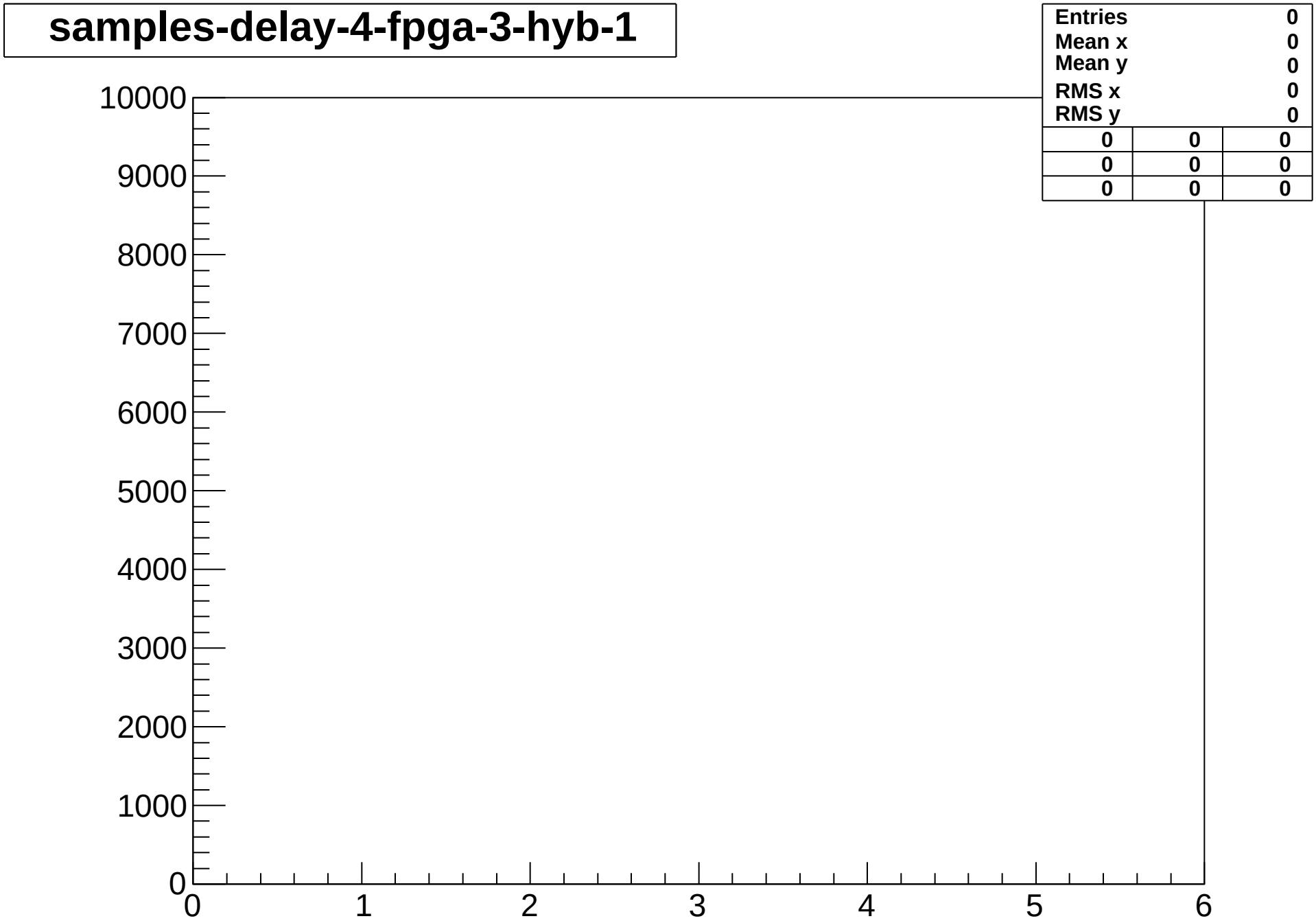
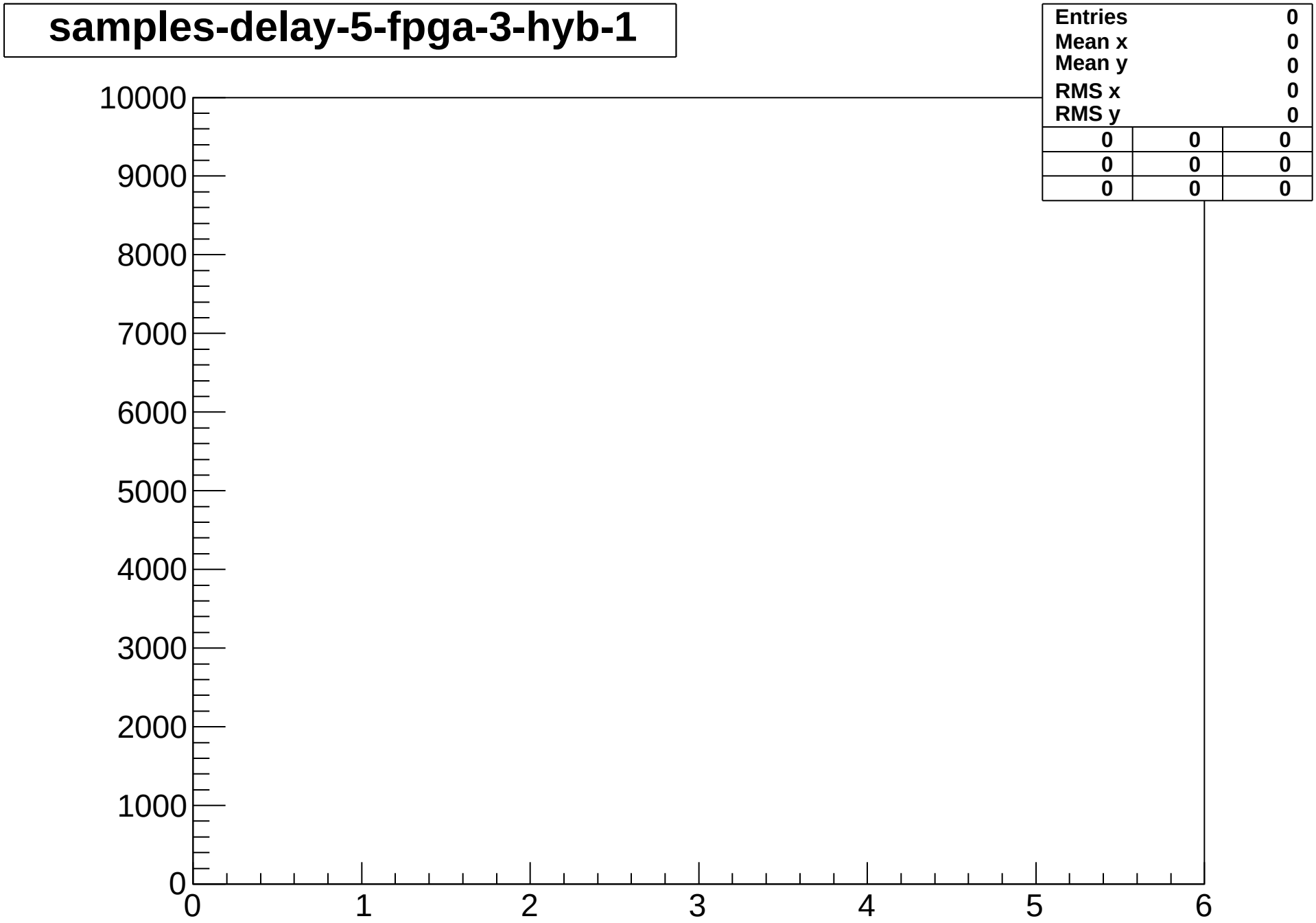
samples-delay-3-fpga-3-hyb-1



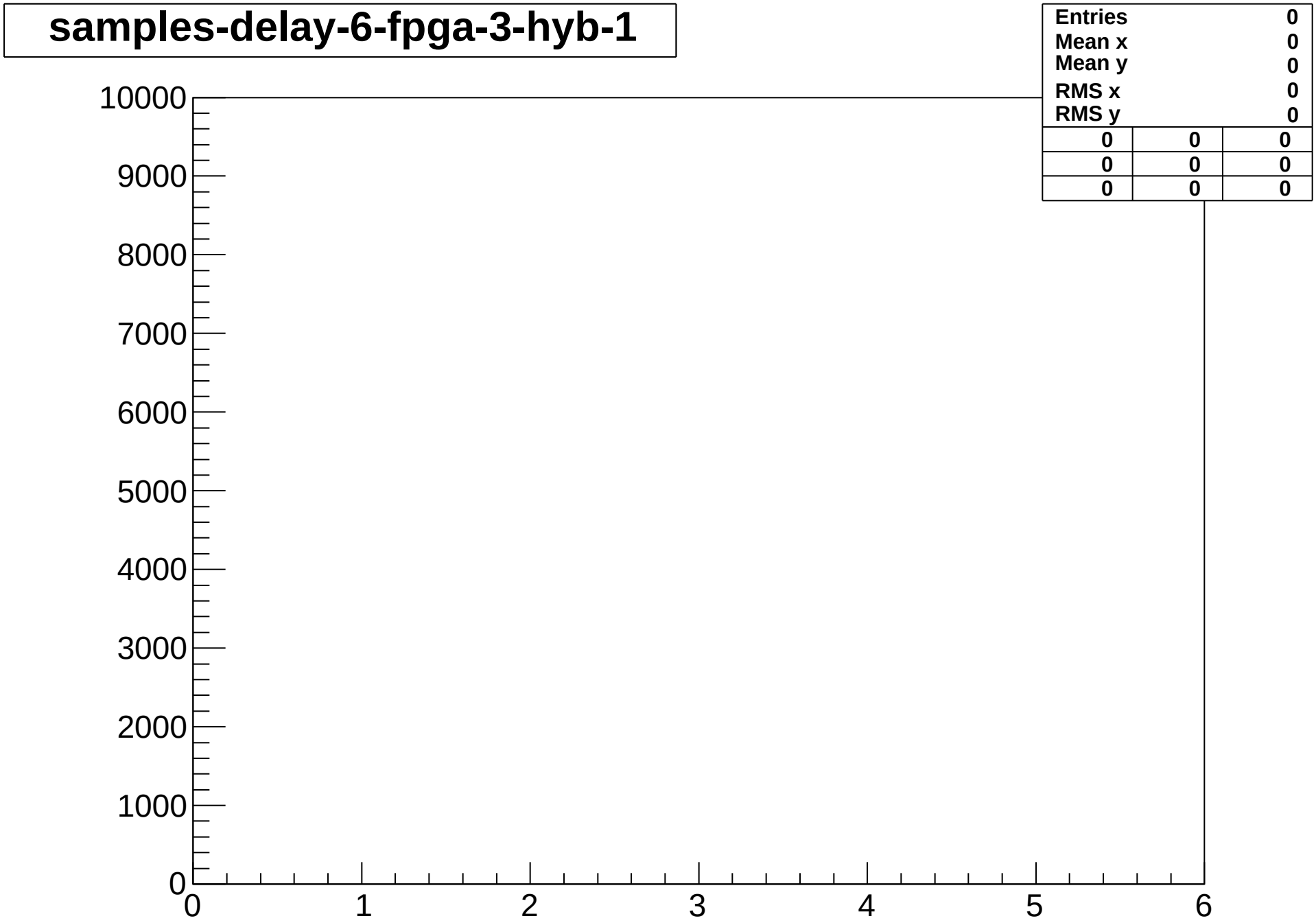
samples-delay-4-fpga-3-hyb-1



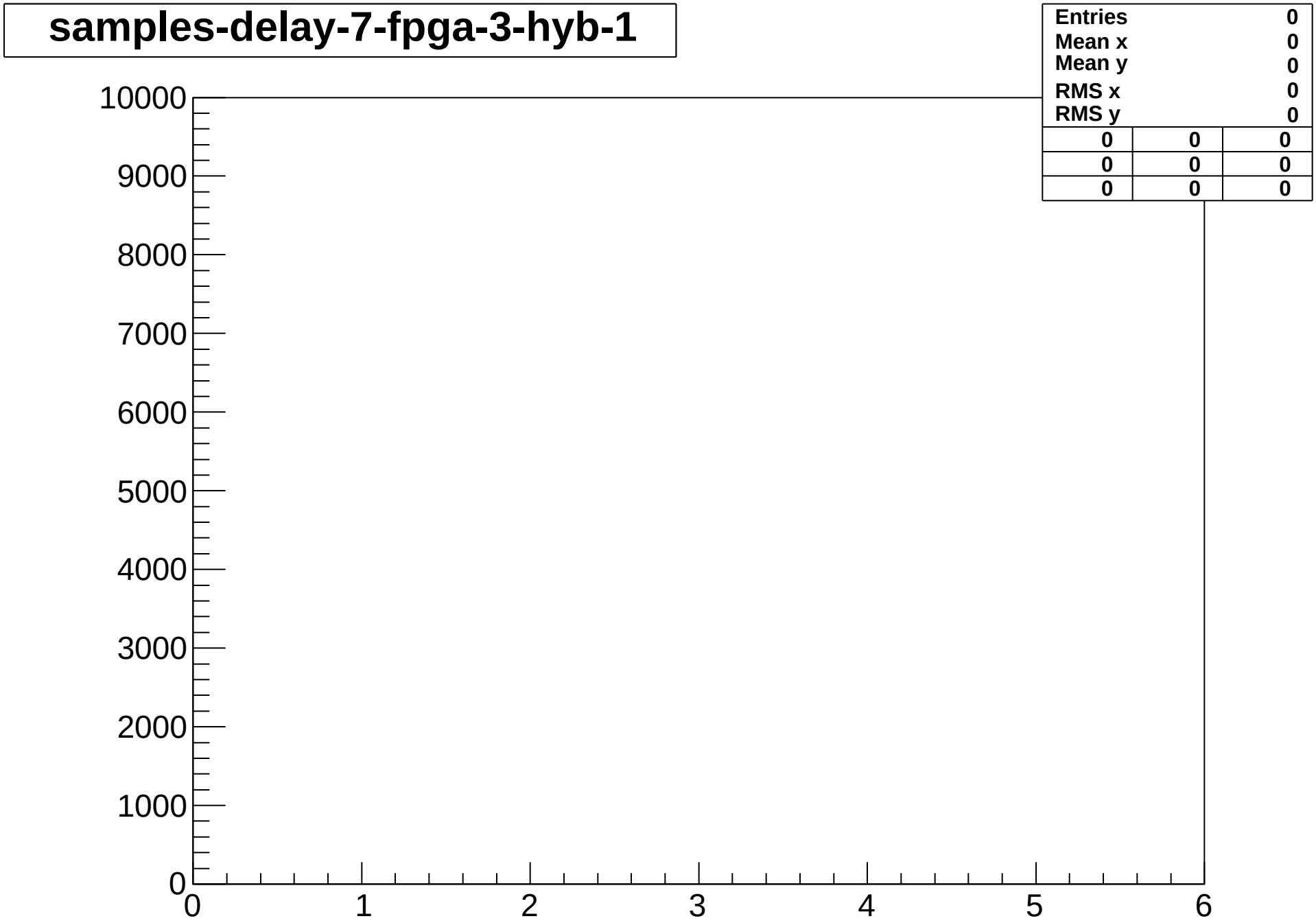
samples-delay-5-fpga-3-hyb-1



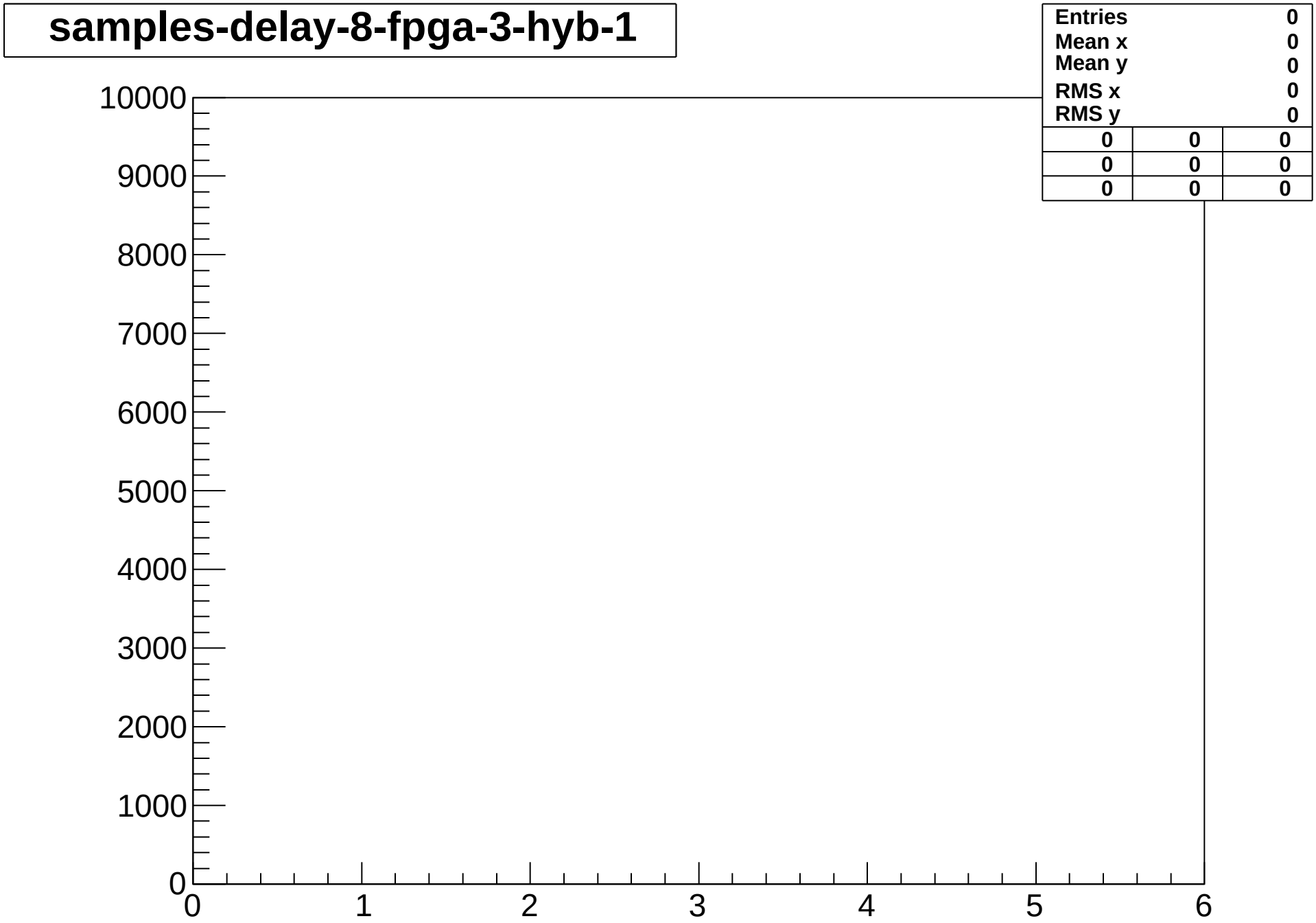
samples-delay-6-fpga-3-hyb-1

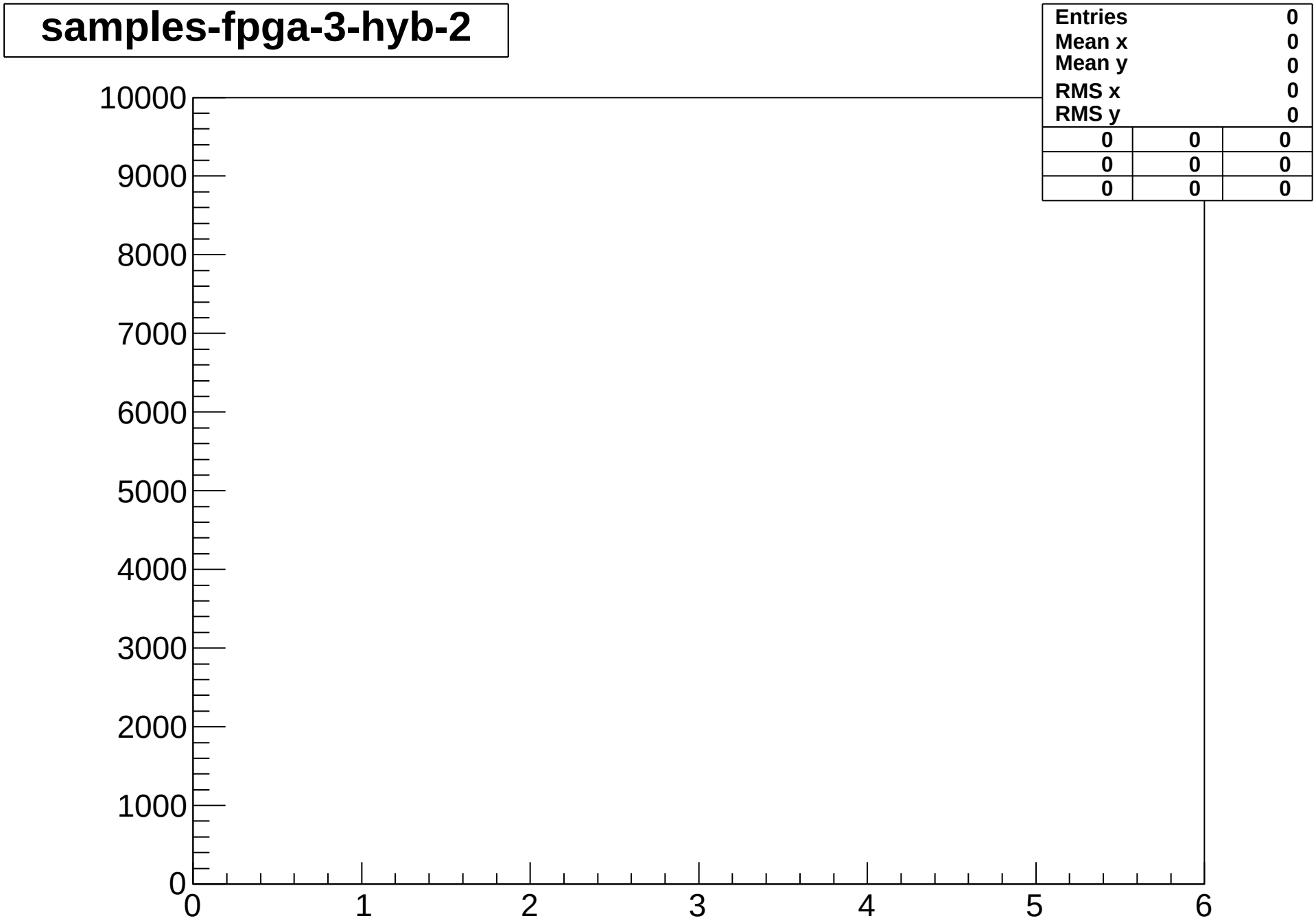


samples-delay-7-fpga-3-hyb-1



samples-delay-8-fpga-3-hyb-1




samples-fpga-3-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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4000
3000
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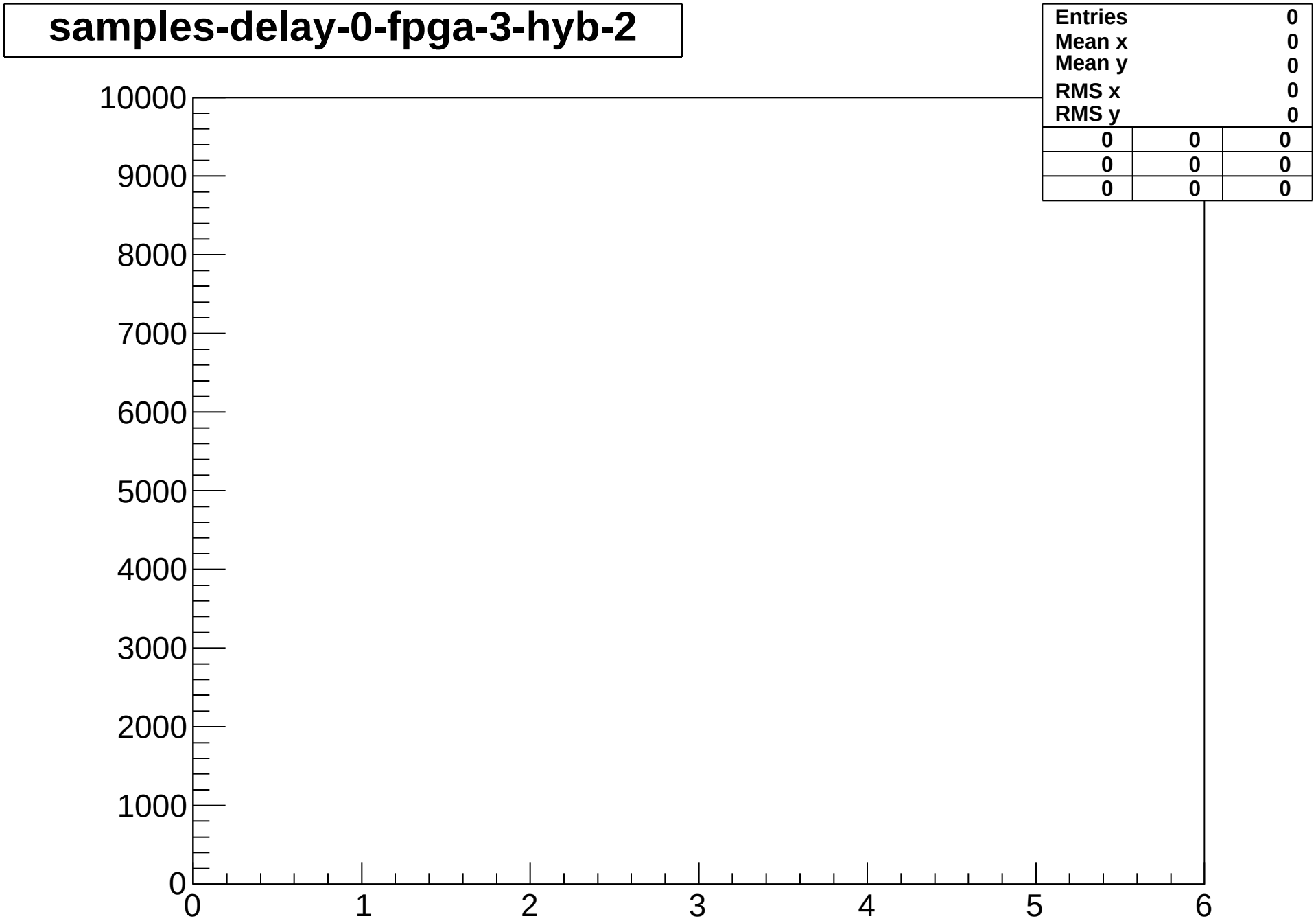
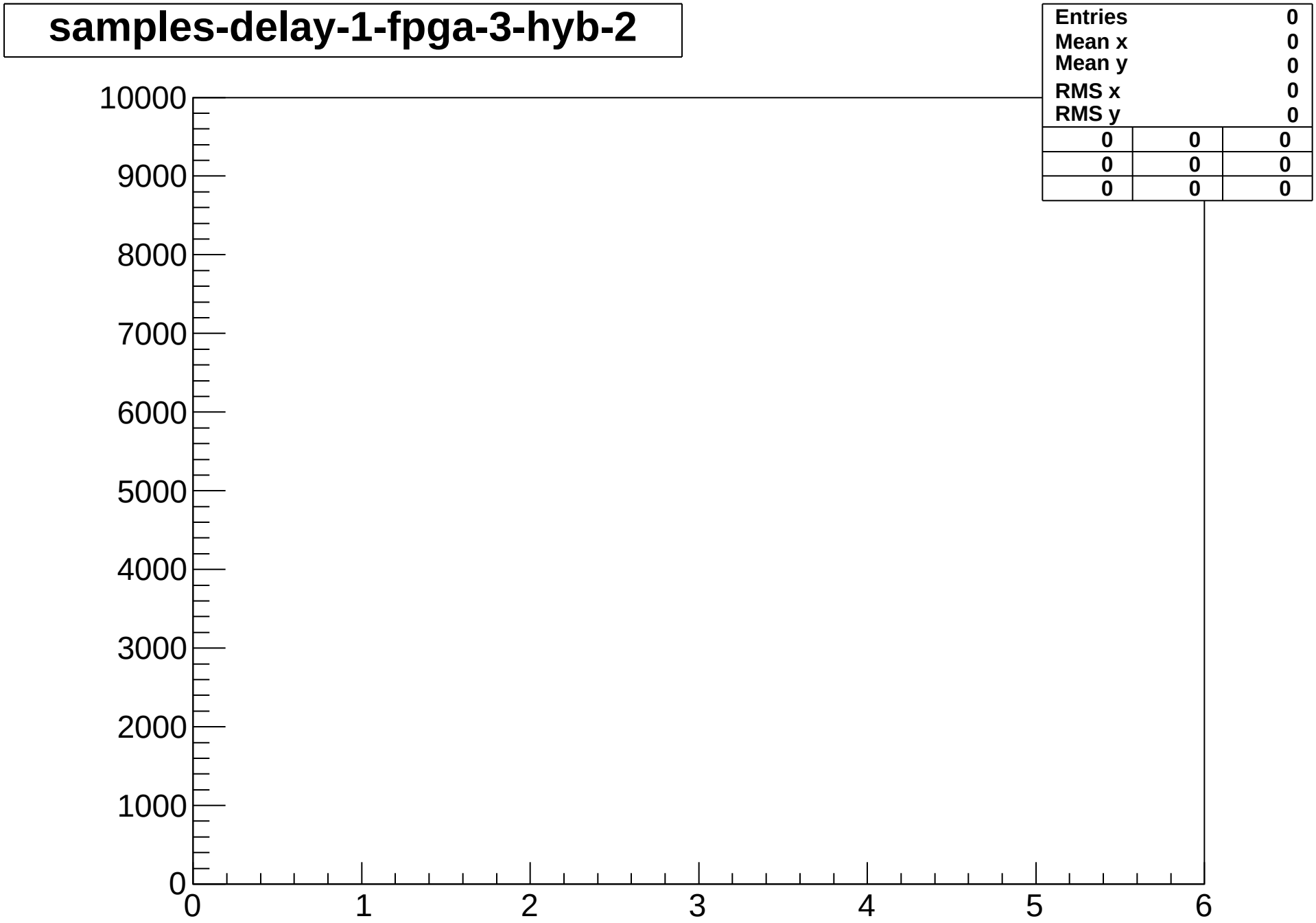
samples-delay-0-fpga-3-hyb-2




samples-delay-1-fpga-3-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
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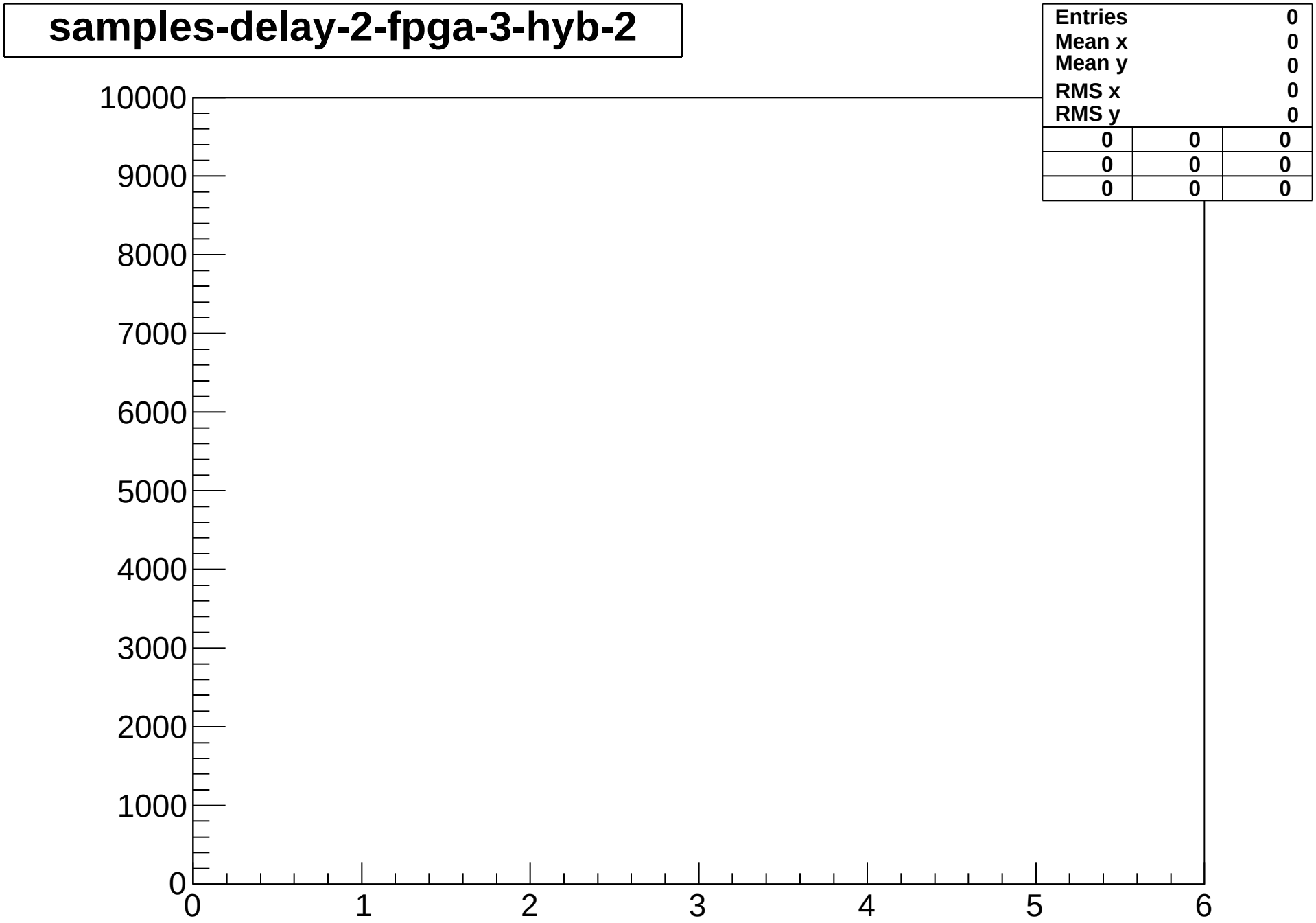
6


samples-delay-2-fpga-3-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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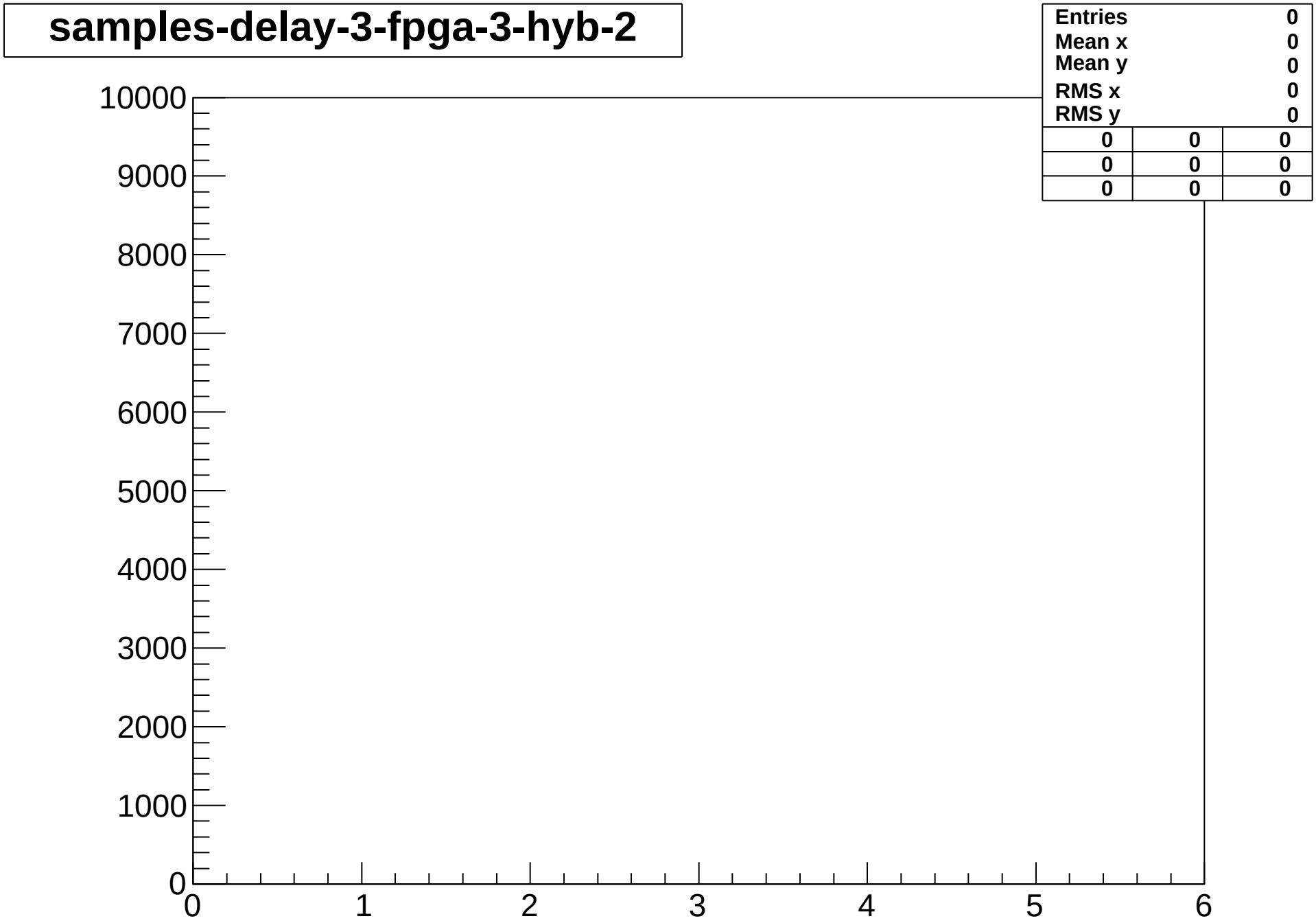
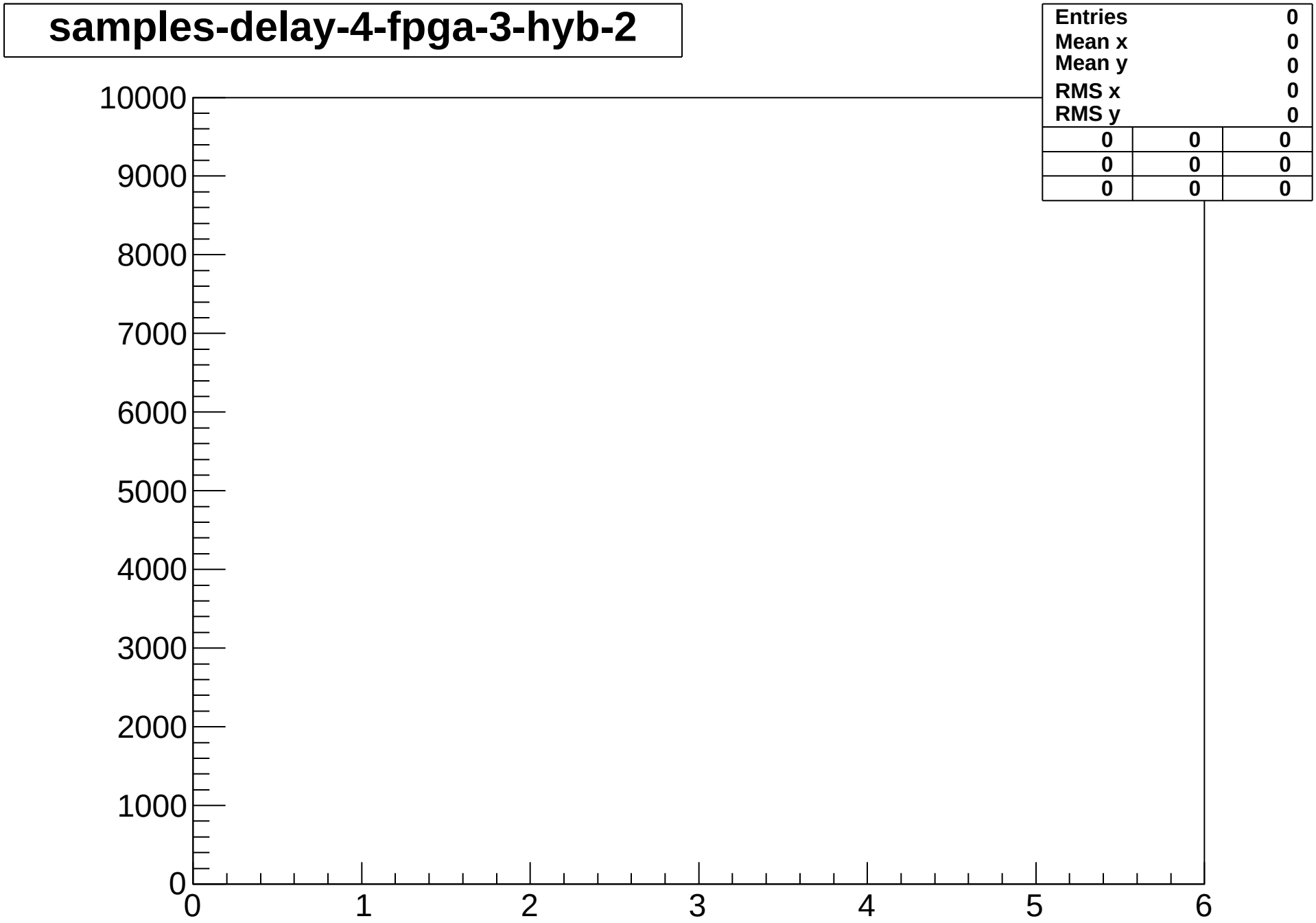
samples-delay-3-fpga-3-hyb-2




samples-delay-4-fpga-3-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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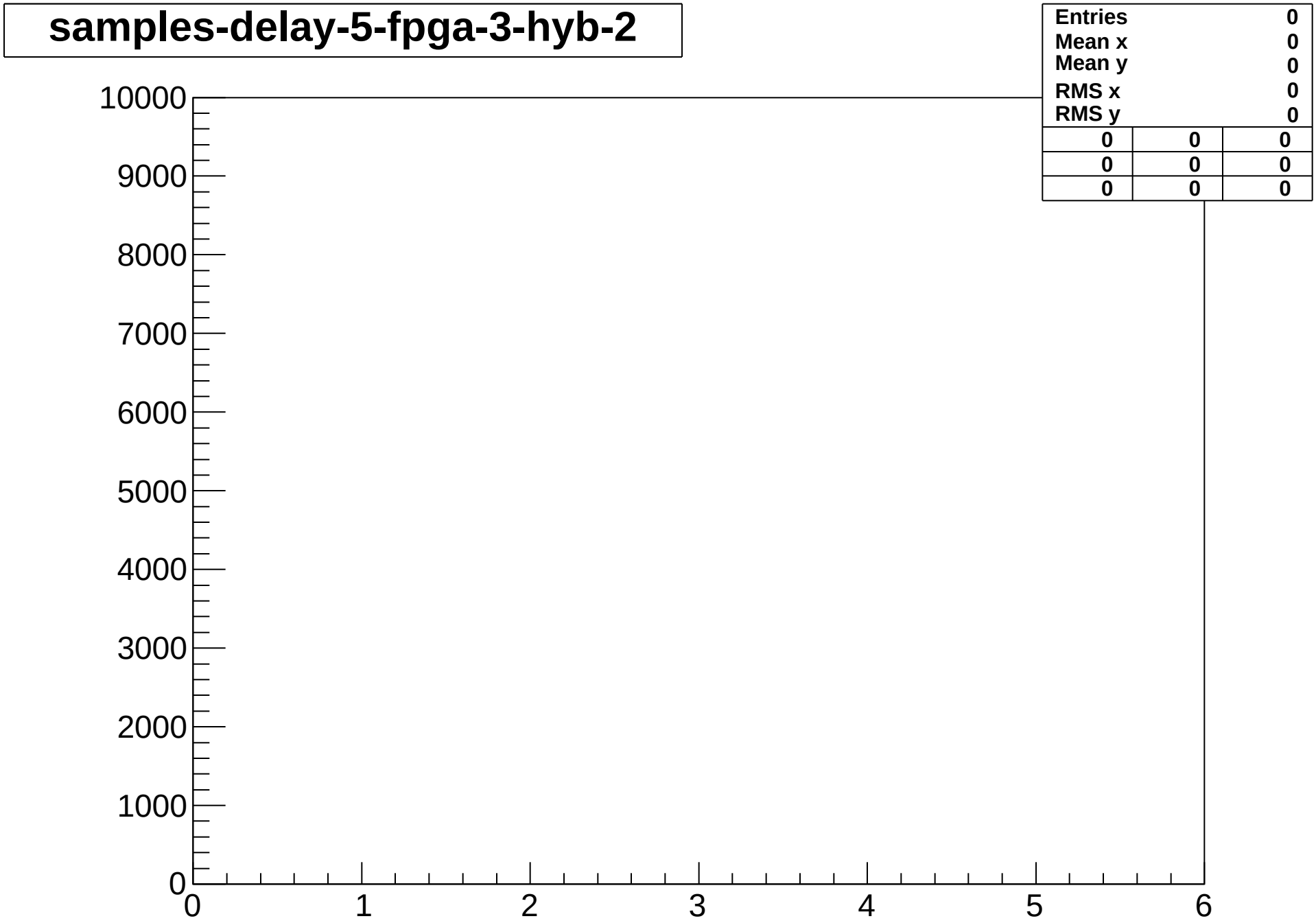
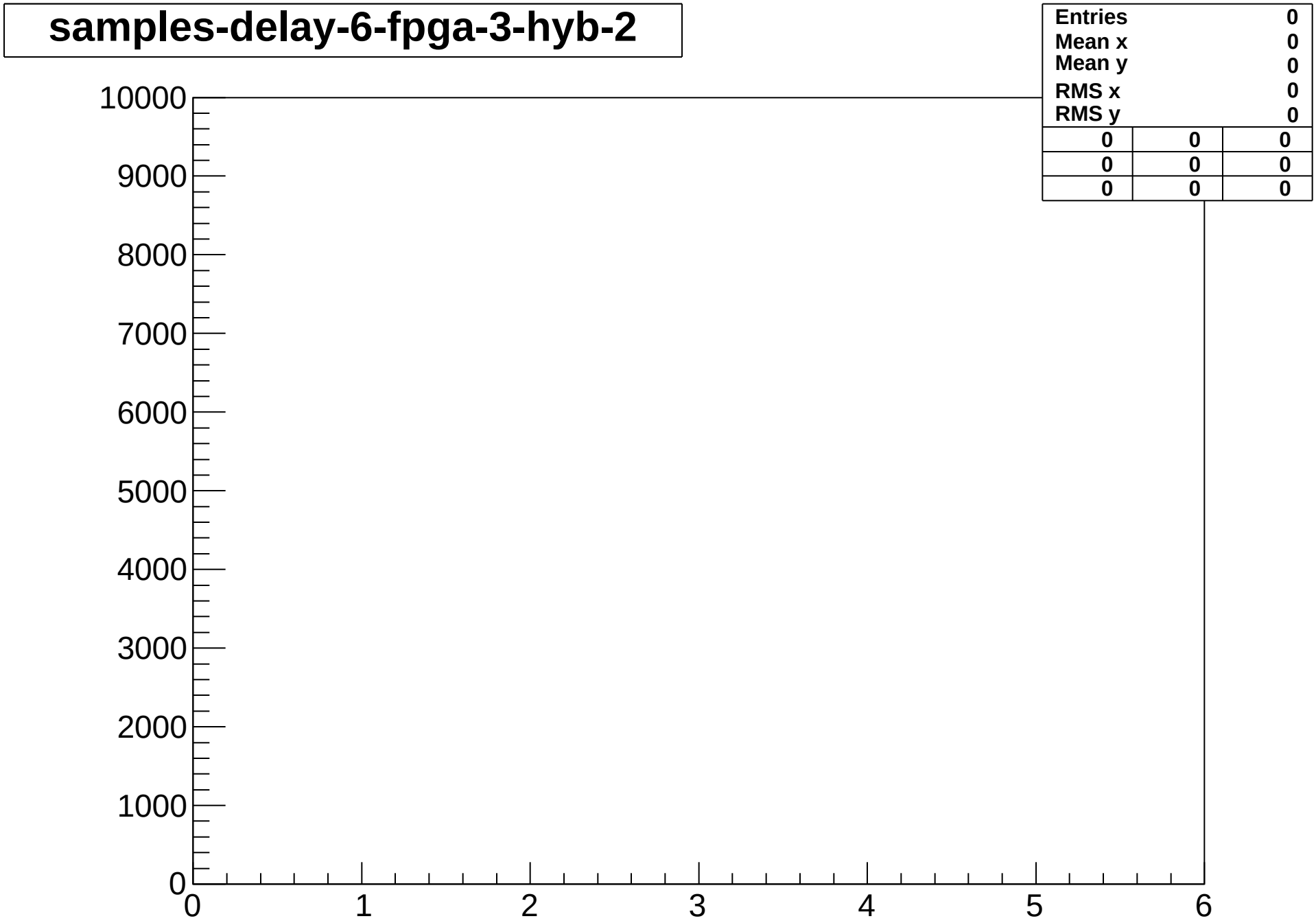
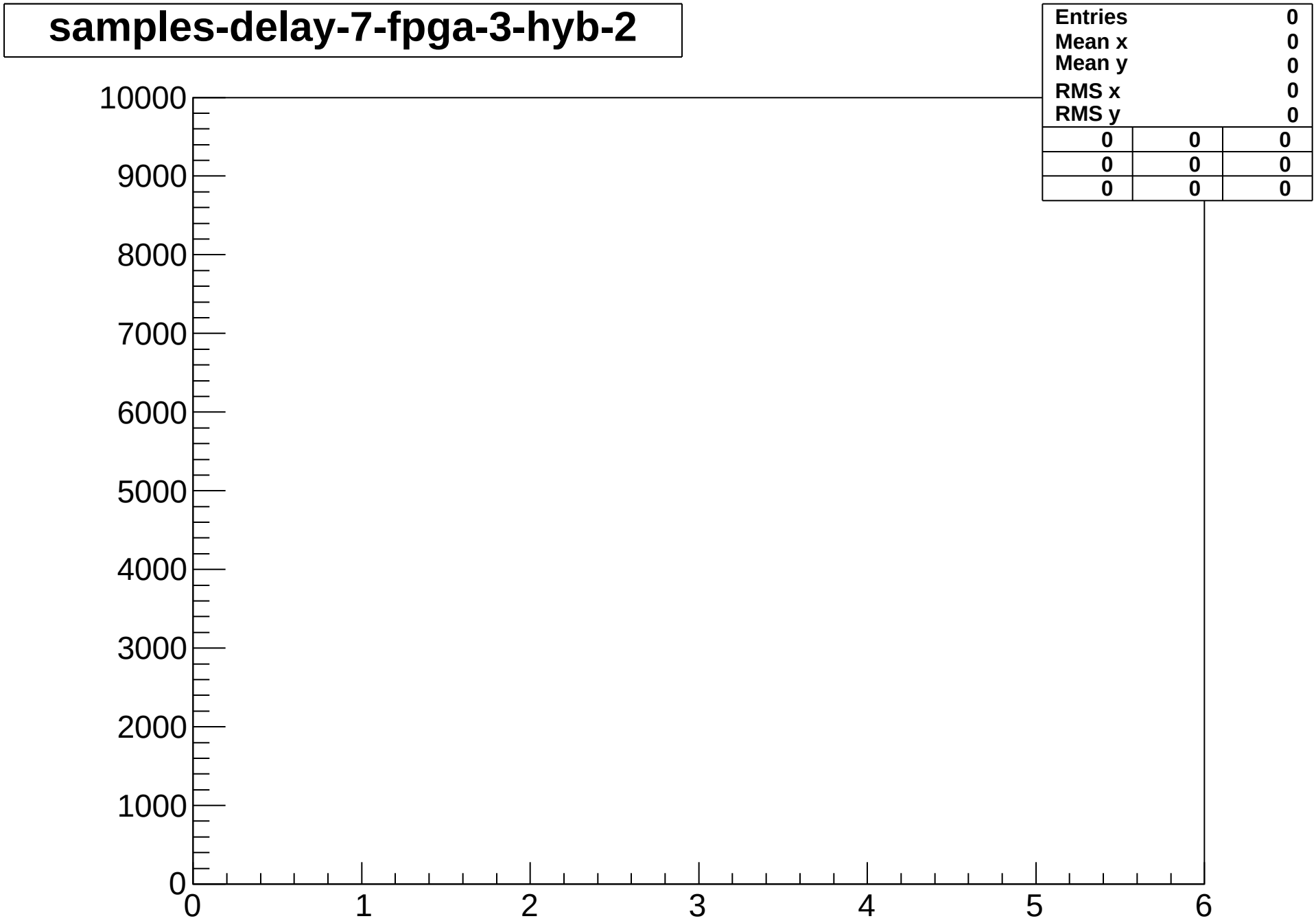
samples-delay-5-fpga-3-hyb-2



samples-delay-6-fpga-3-hyb-2




samples-delay-7-fpga-3-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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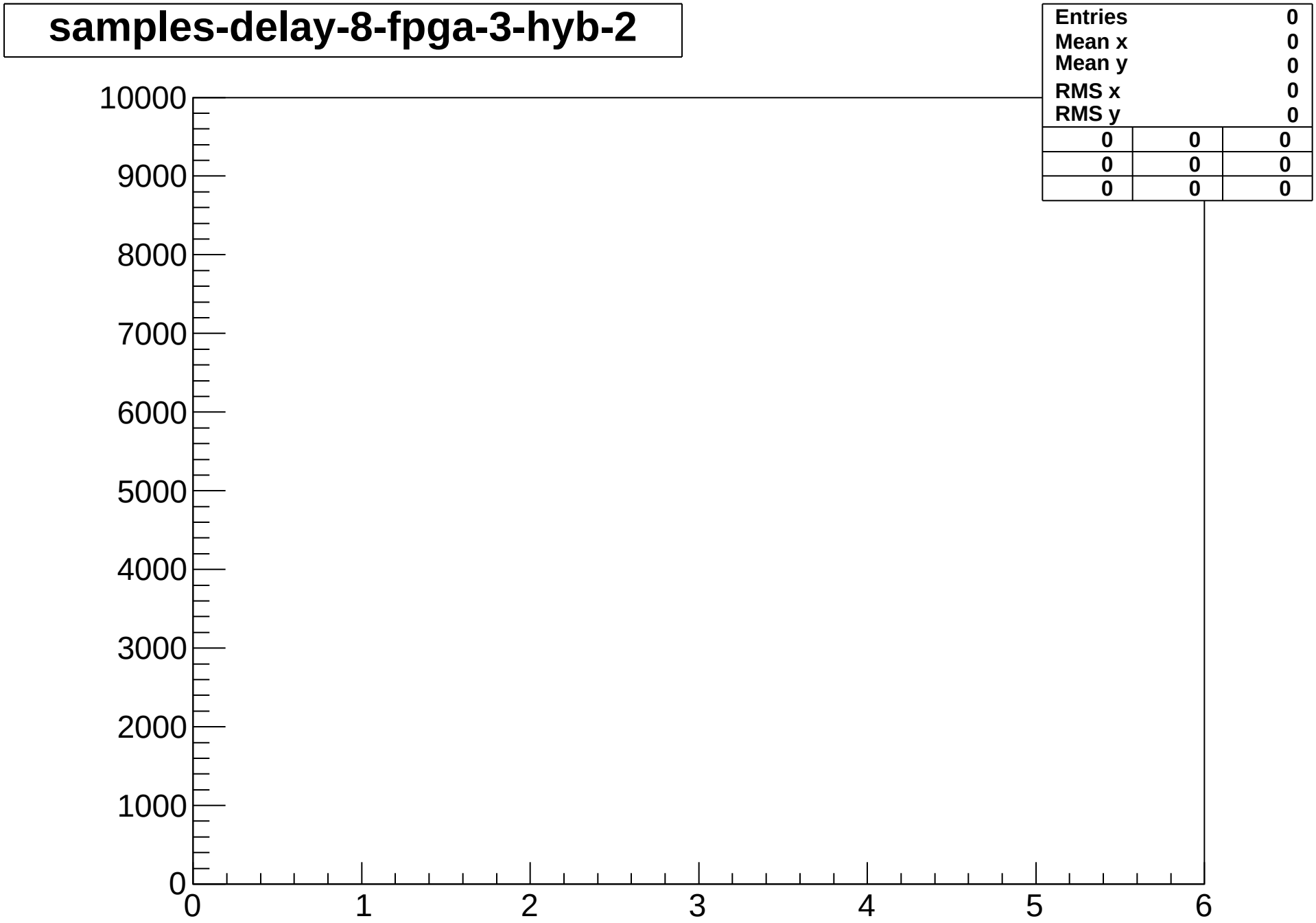
samples-delay-8-fpga-3-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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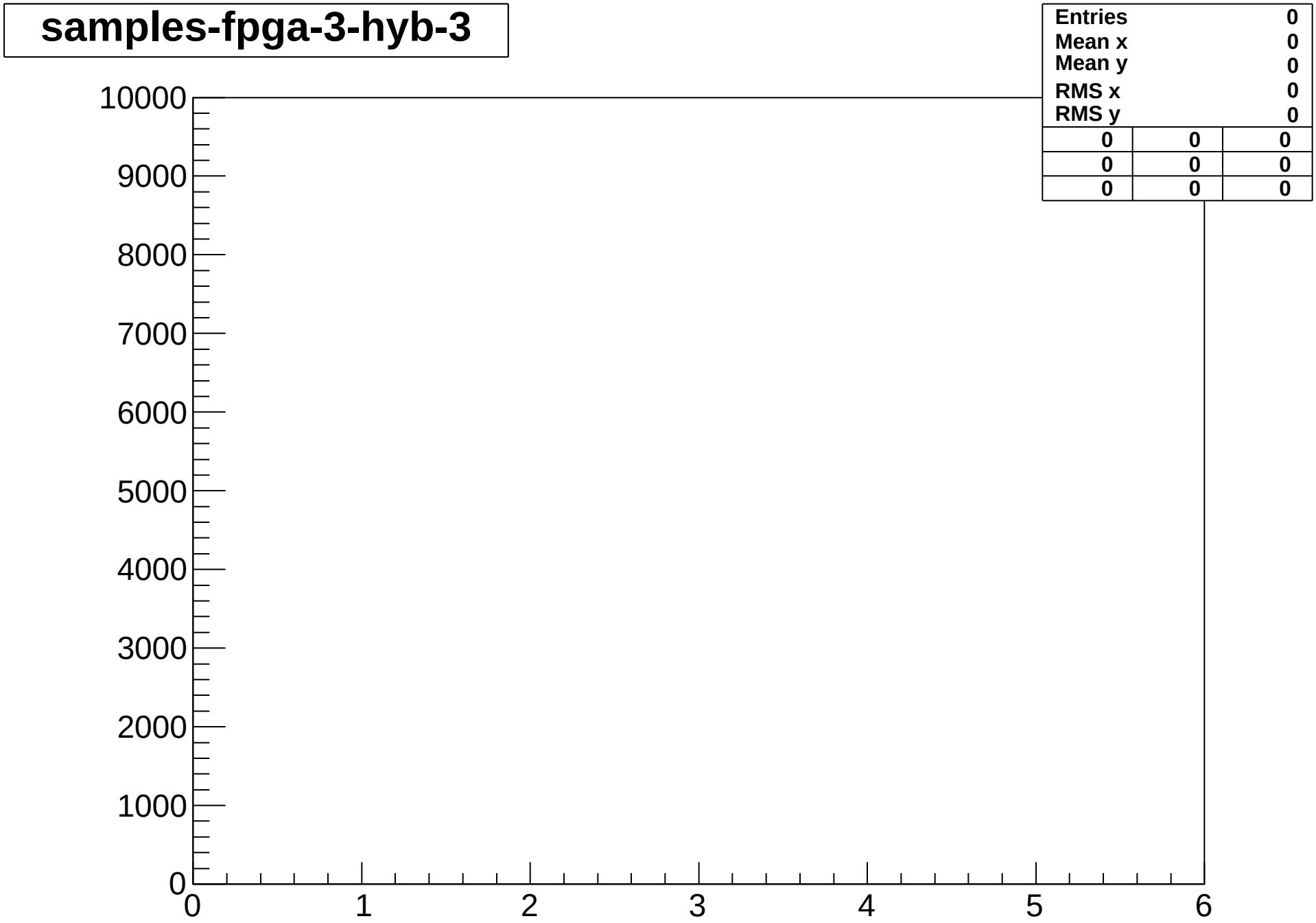
samples-fpga-3-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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9000
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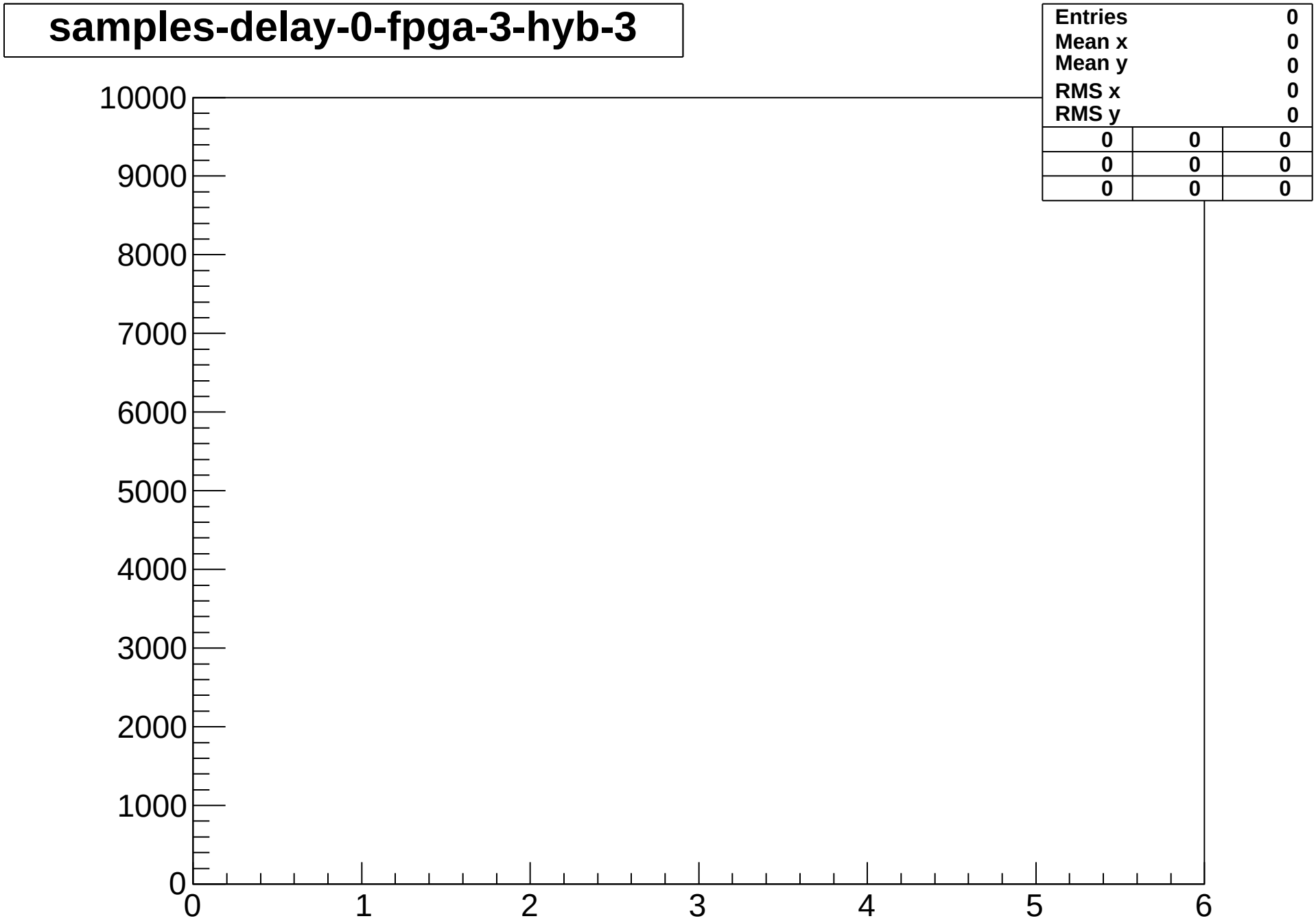
samples-delay-0-fpga-3-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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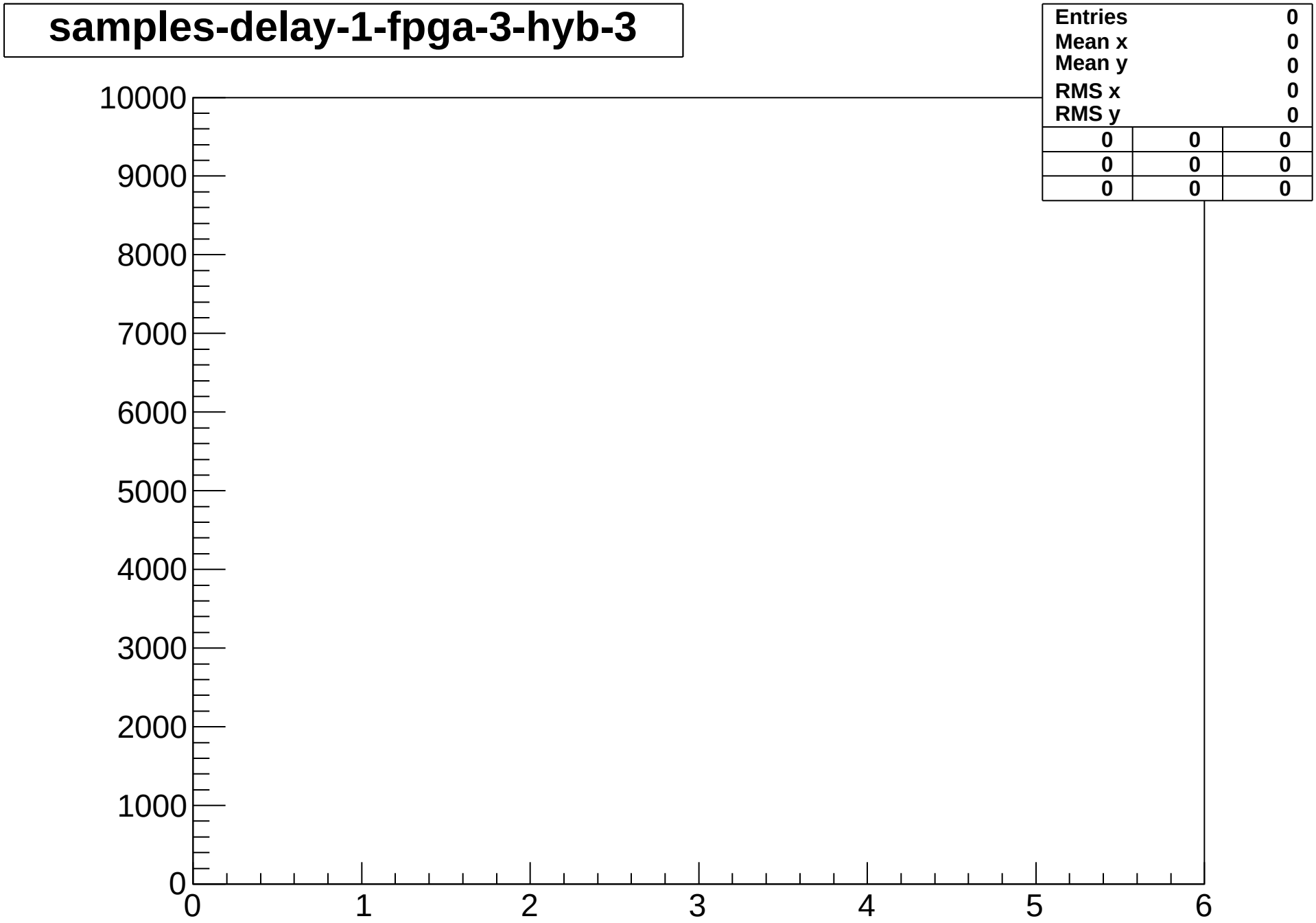
samples-delay-1-fpga-3-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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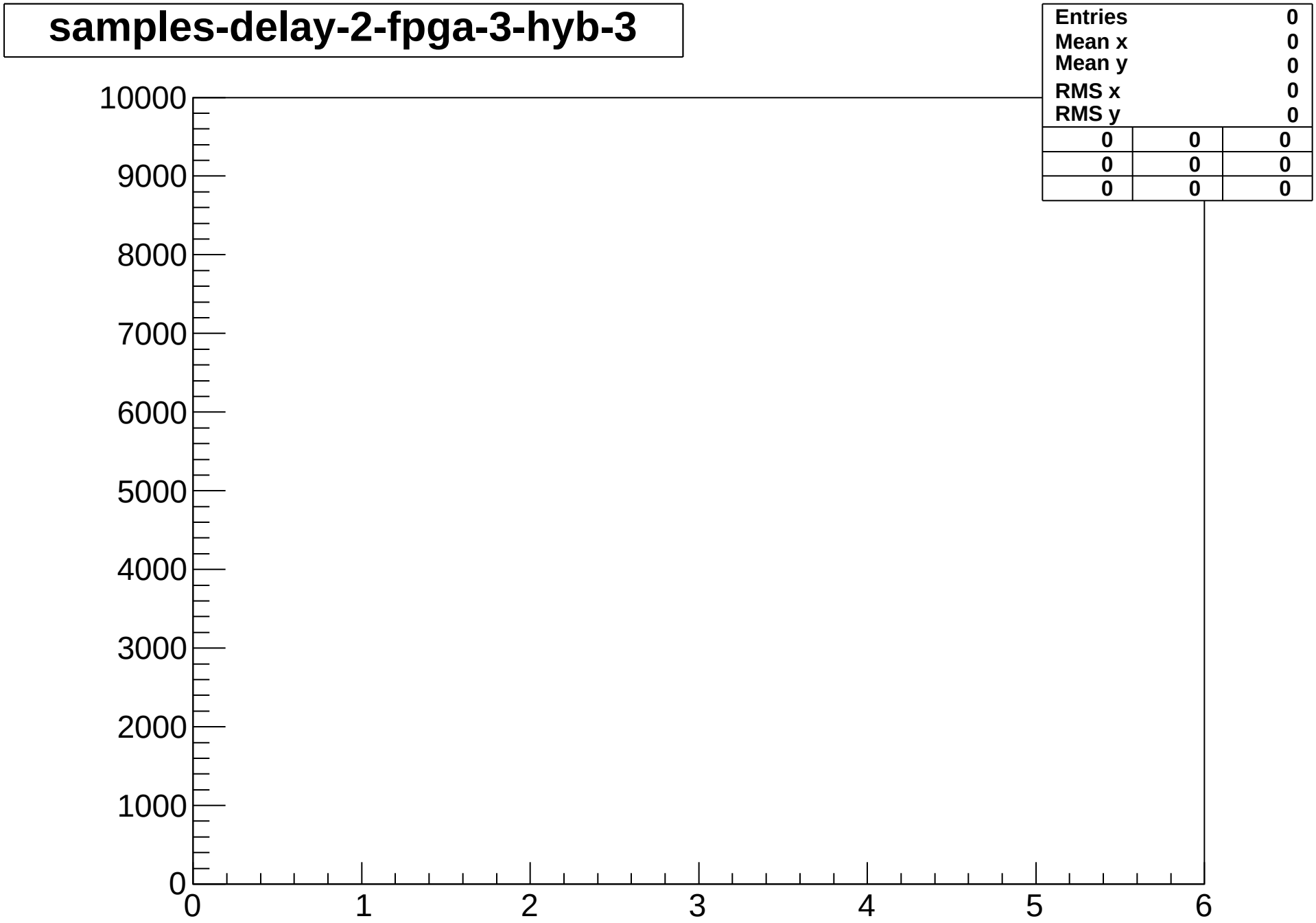
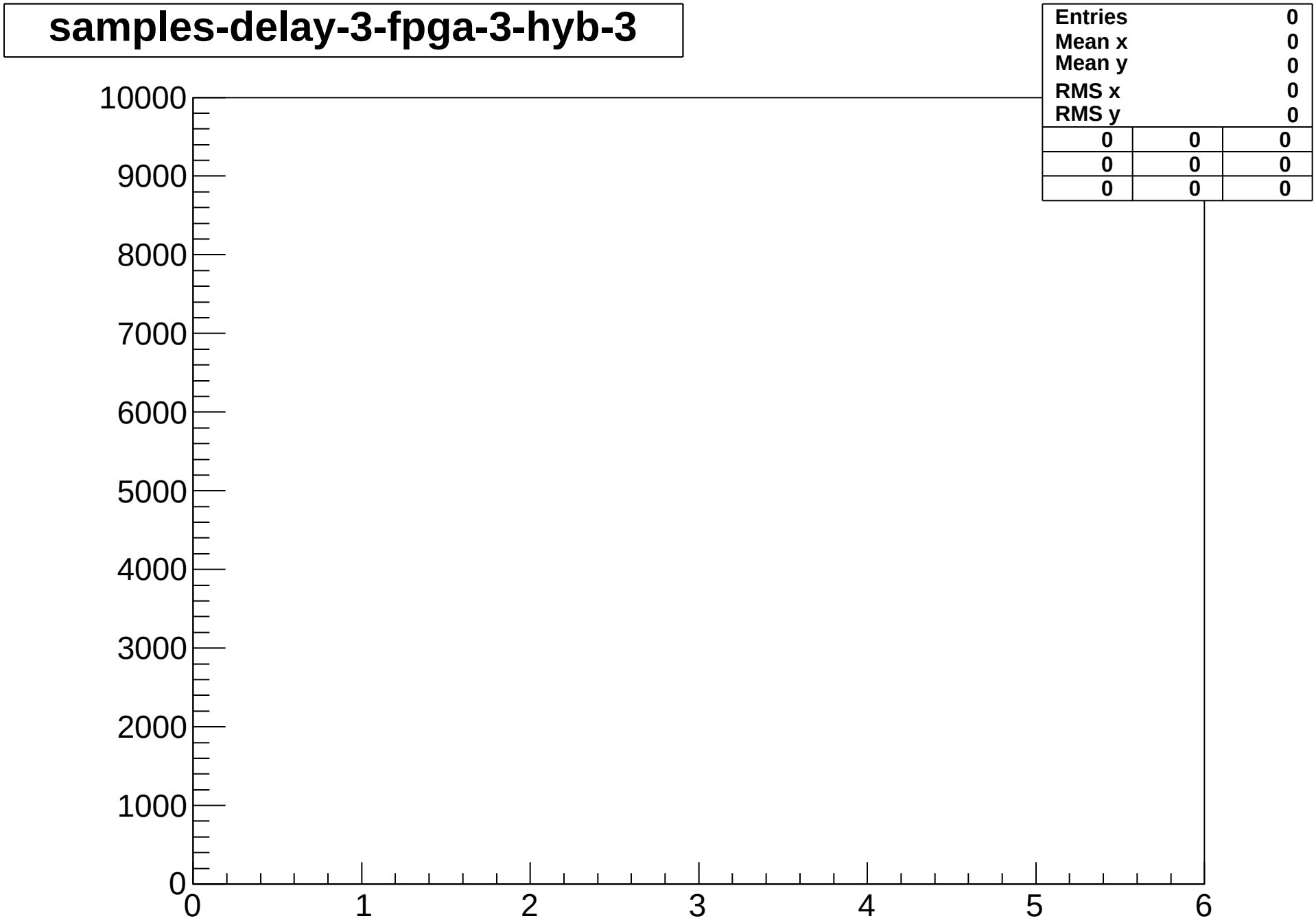
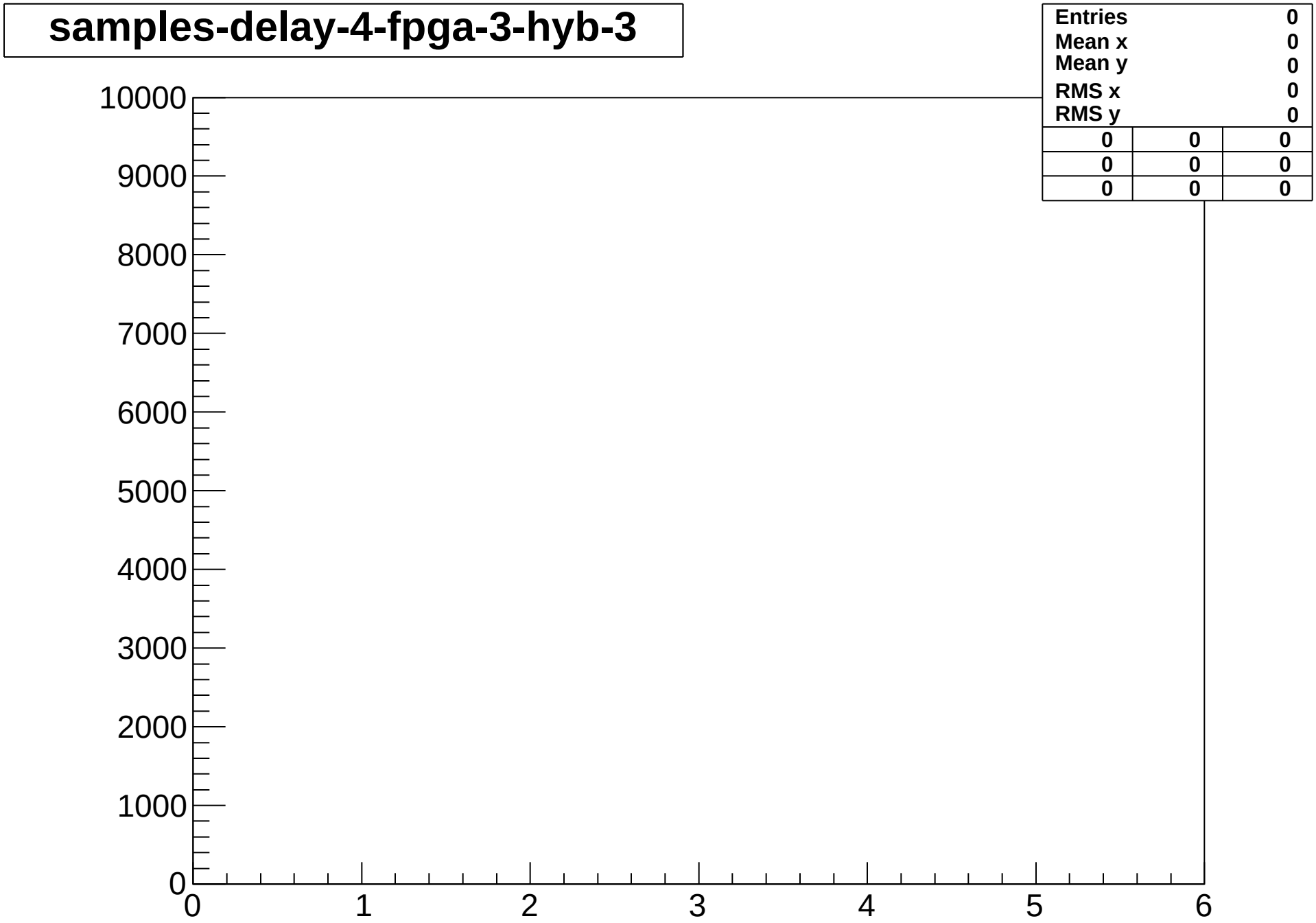
samples-delay-2-fpga-3-hyb-3



samples-delay-3-fpga-3-hyb-3




samples-delay-4-fpga-3-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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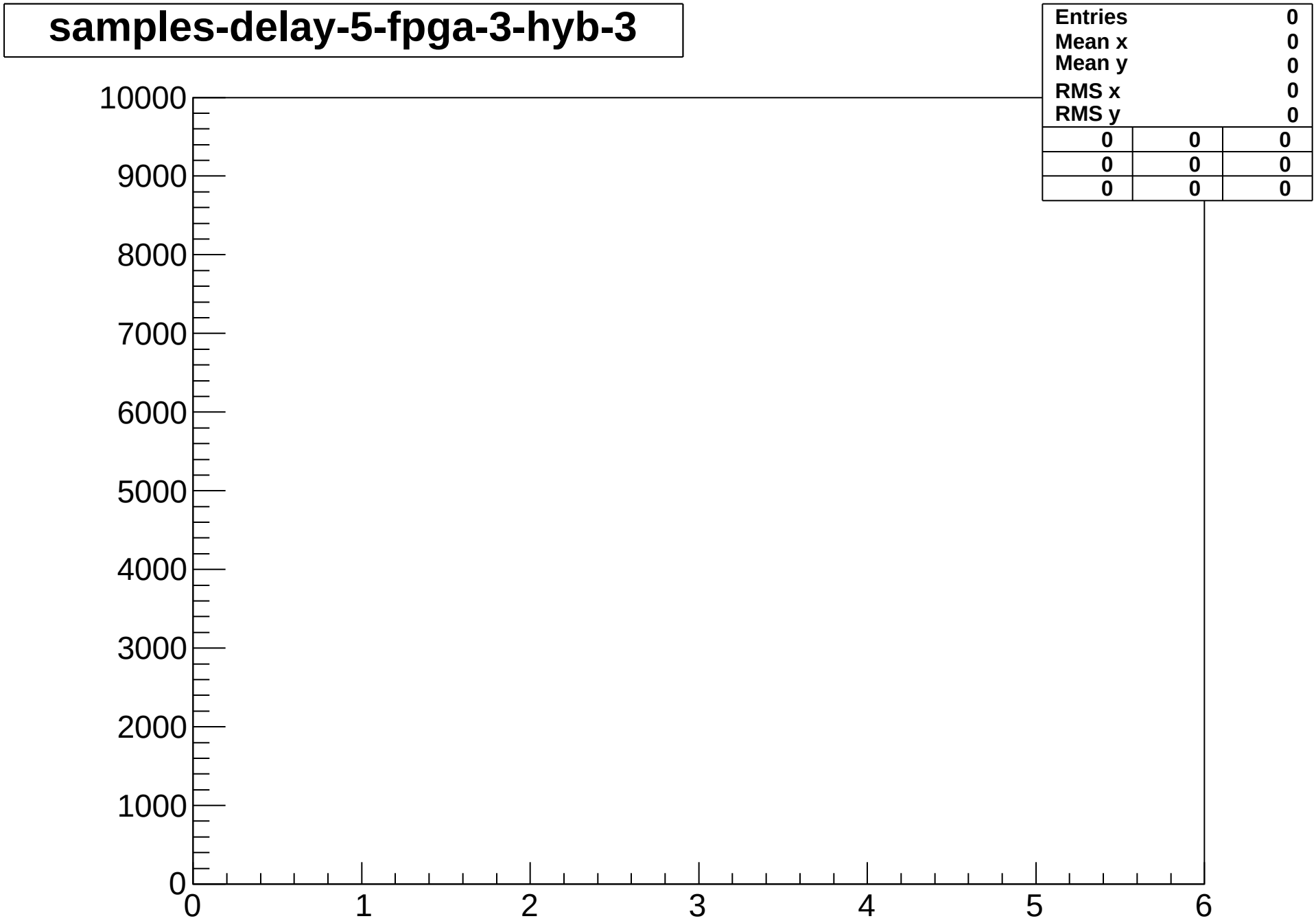
samples-delay-5-fpga-3-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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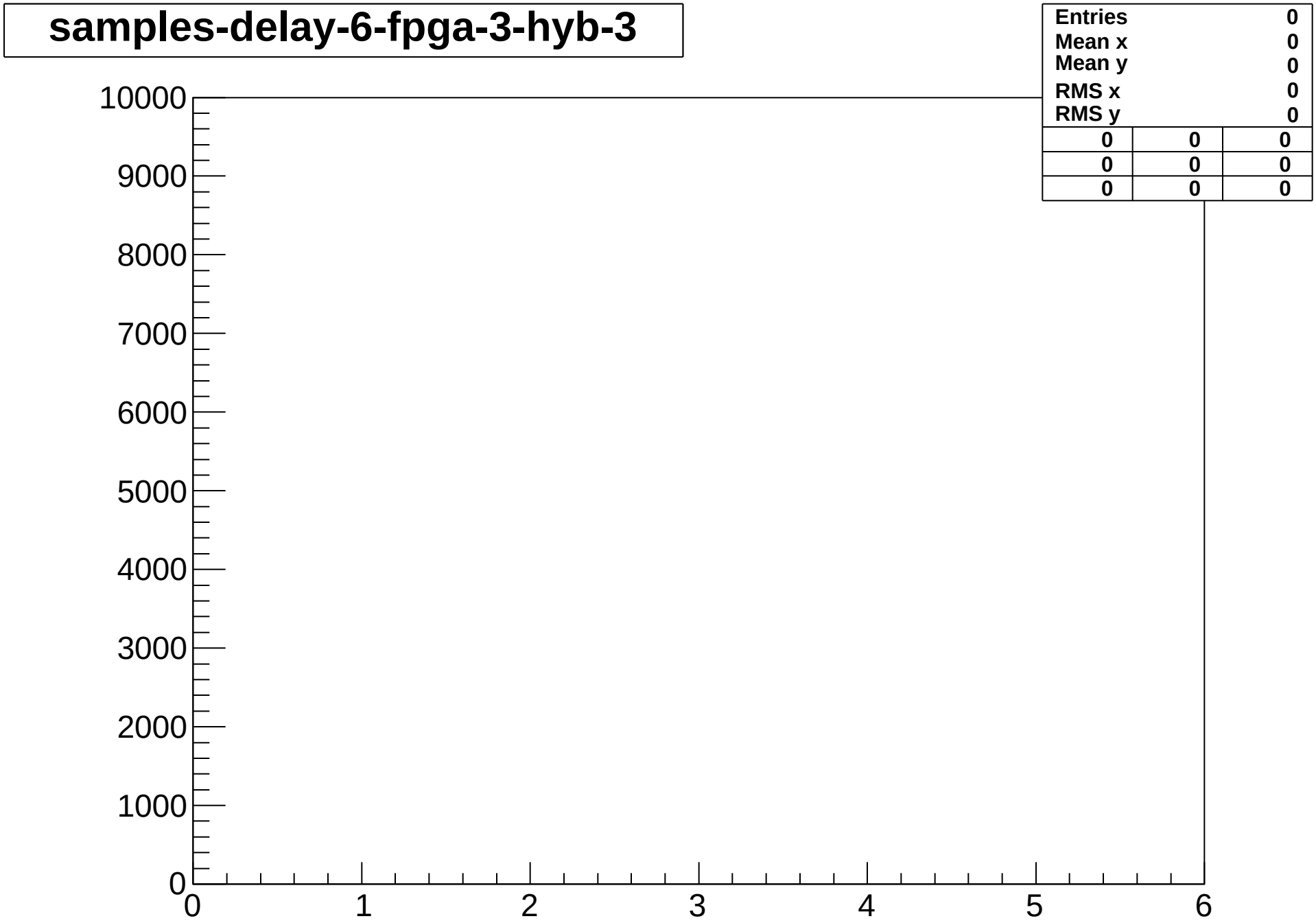
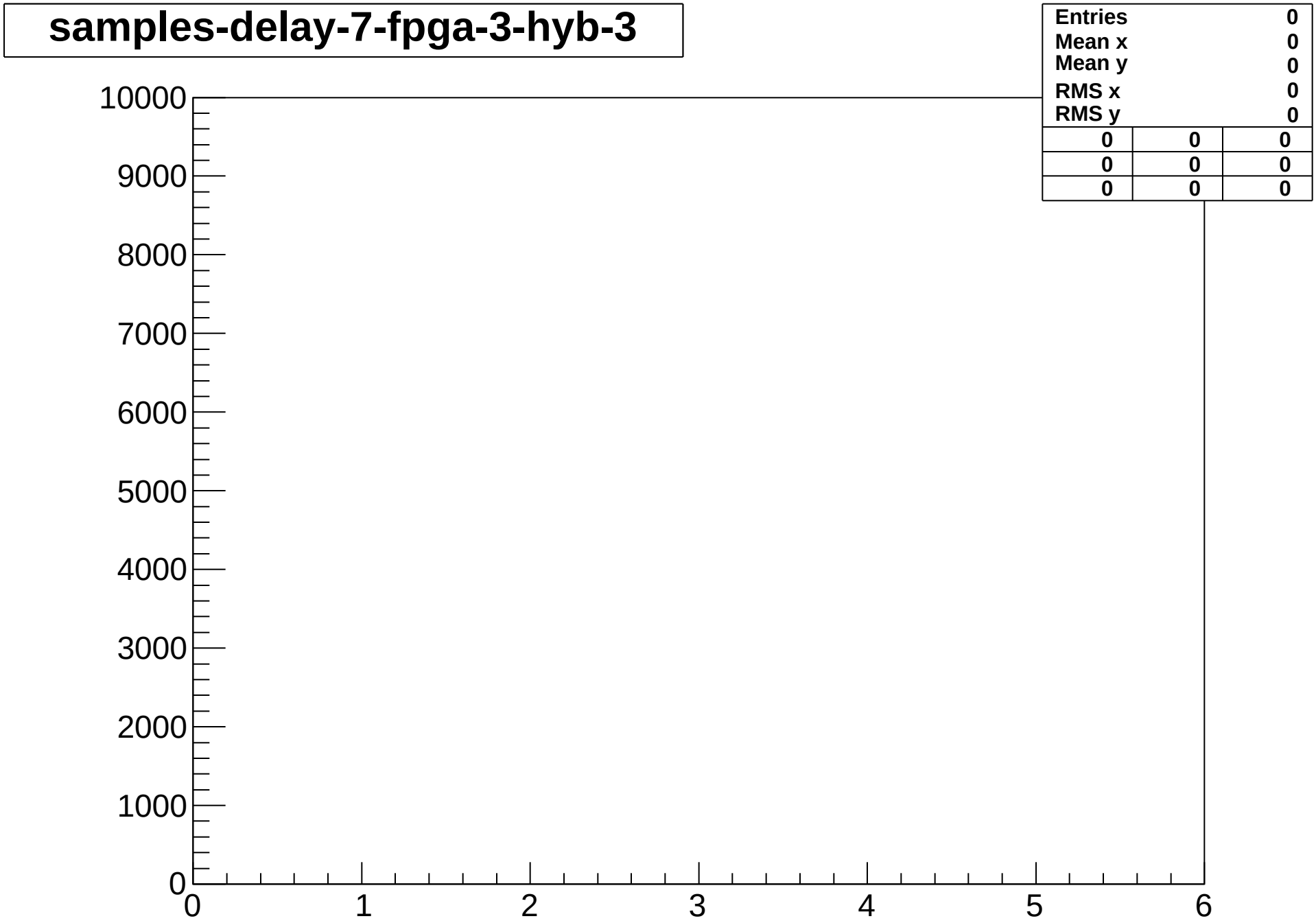
samples-delay-6-fpga-3-hyb-3




samples-delay-7-fpga-3-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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3000
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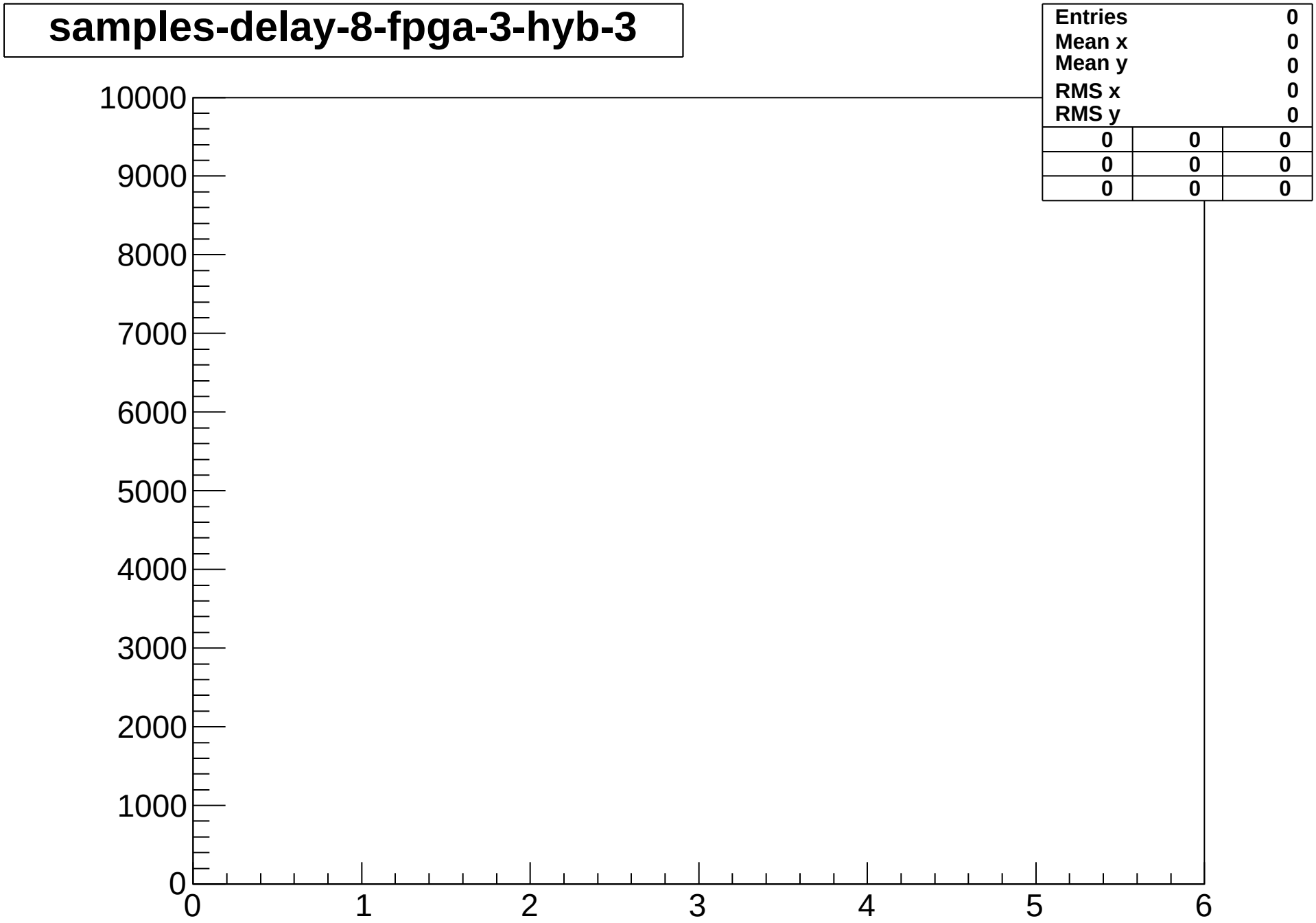
samples-delay-8-fpga-3-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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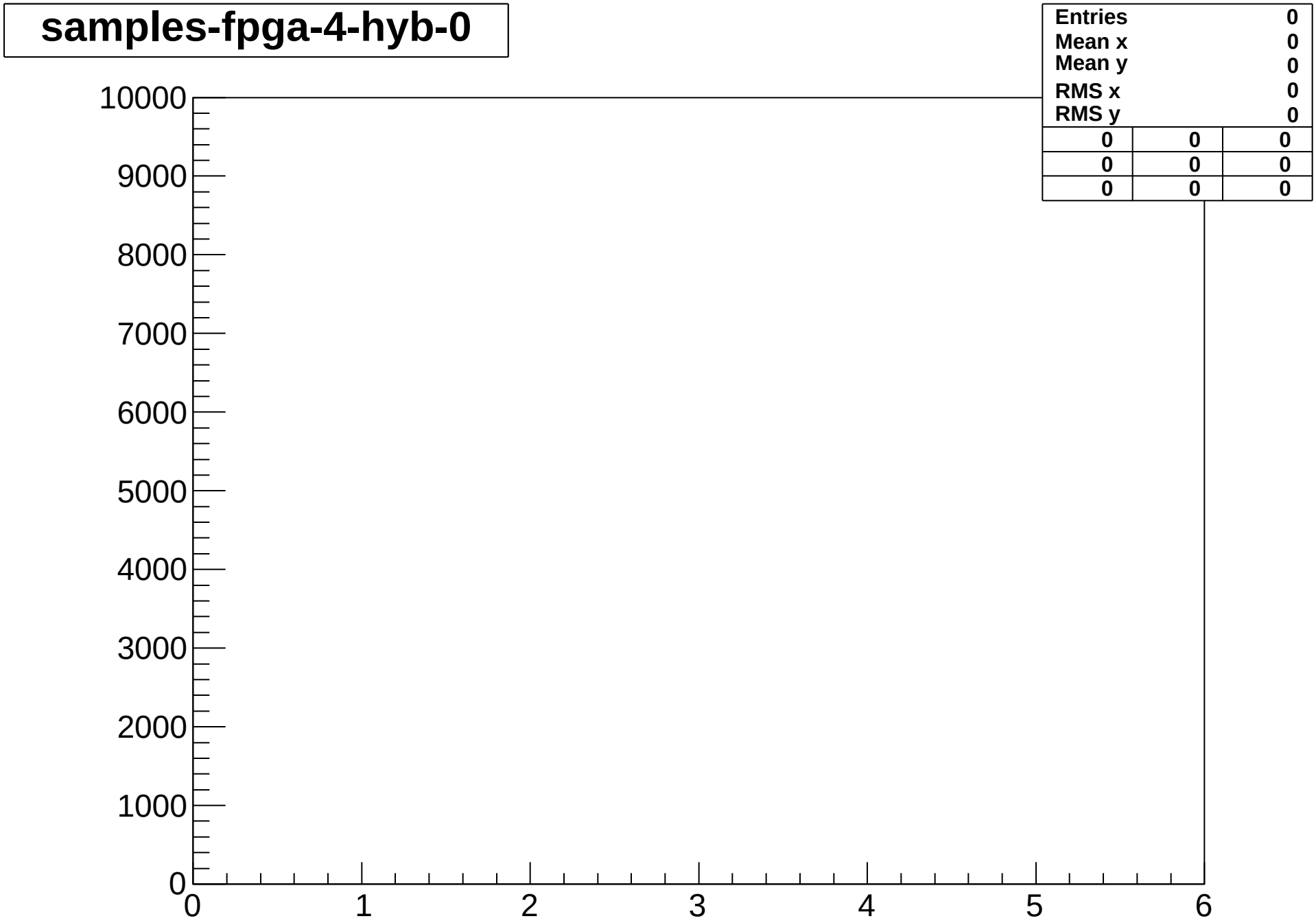
samples-fpga-4-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
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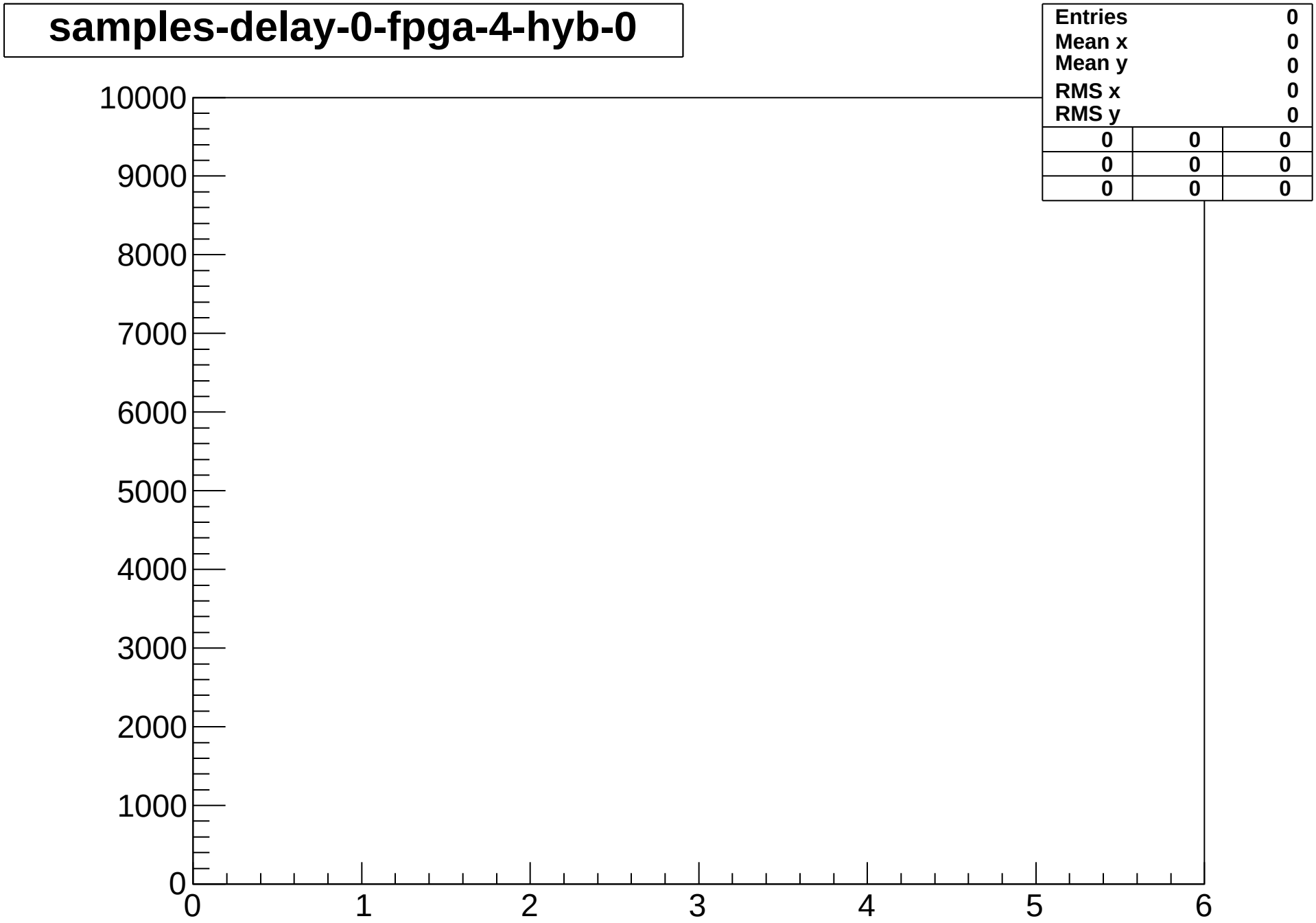
samples-delay-0-fpga-4-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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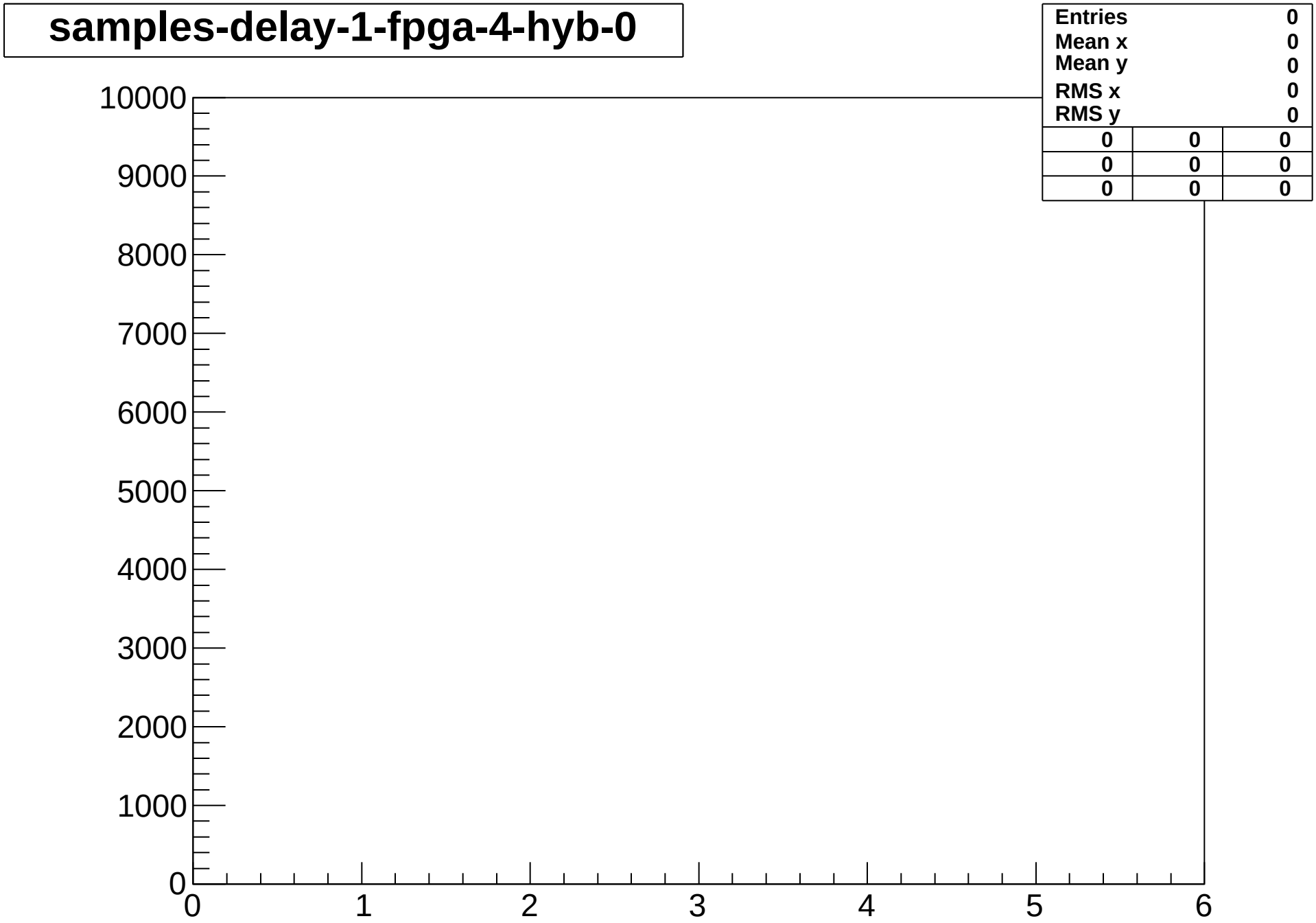
samples-delay-1-fpga-4-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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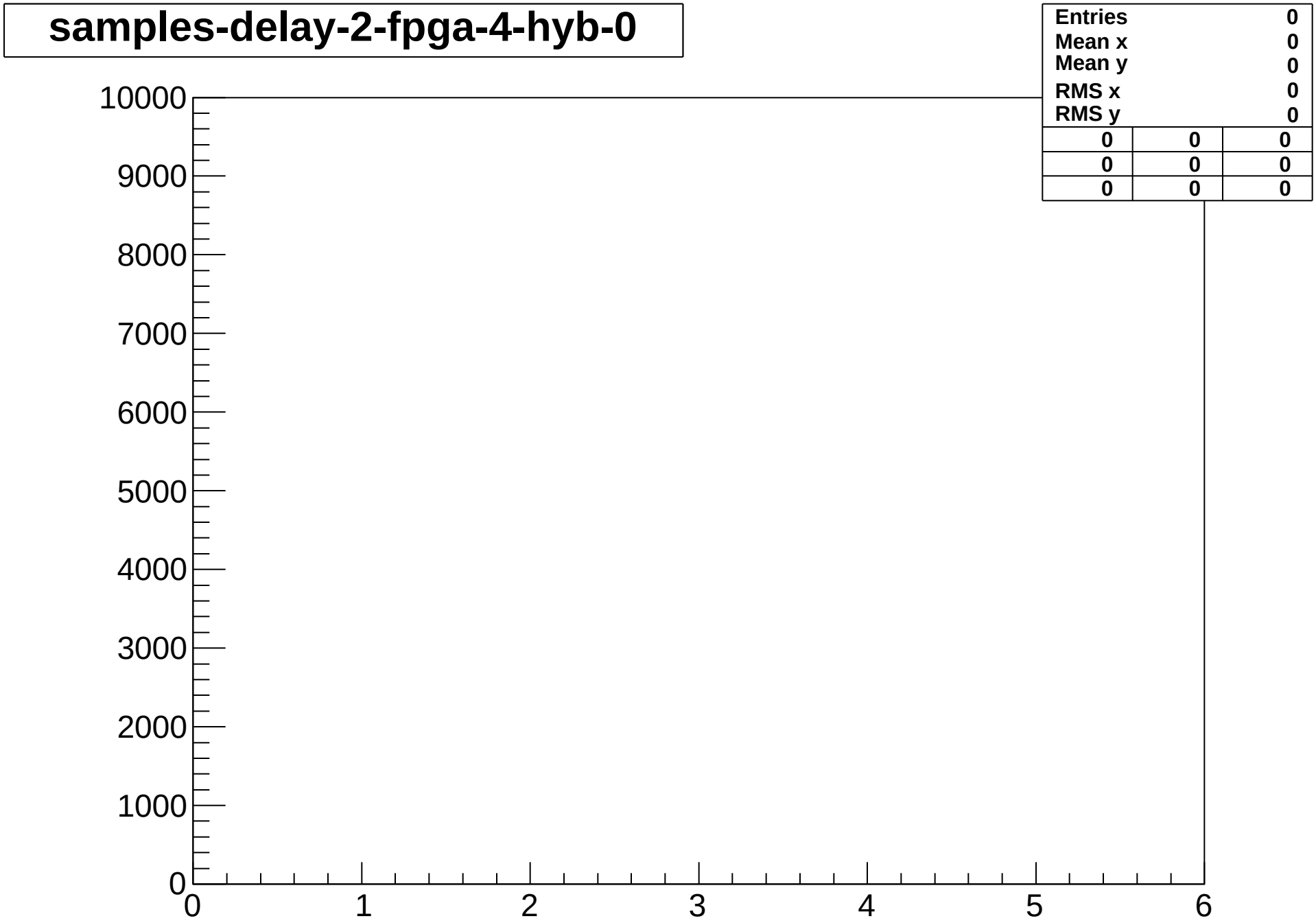
samples-delay-2-fpga-4-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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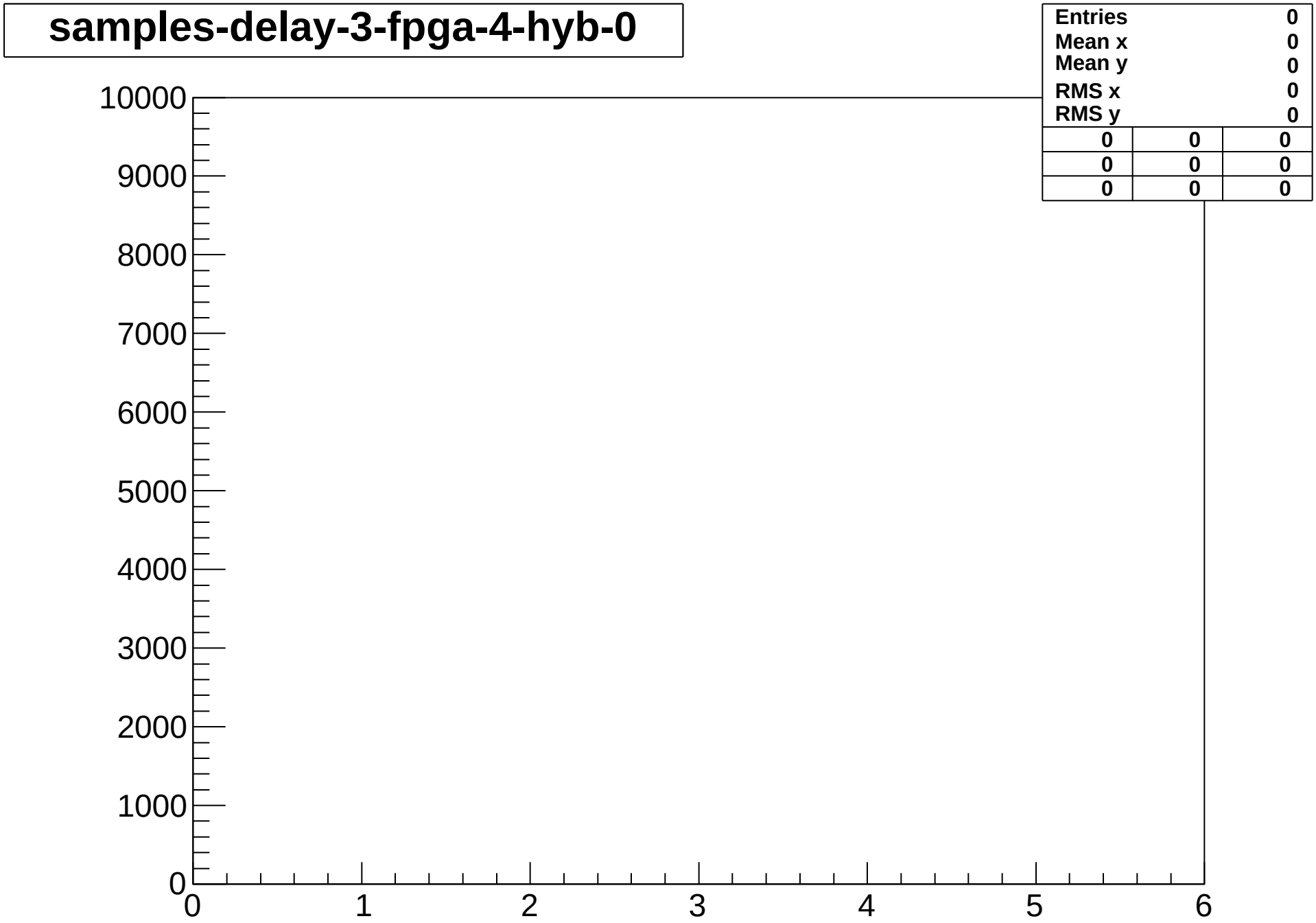
samples-delay-3-fpga-4-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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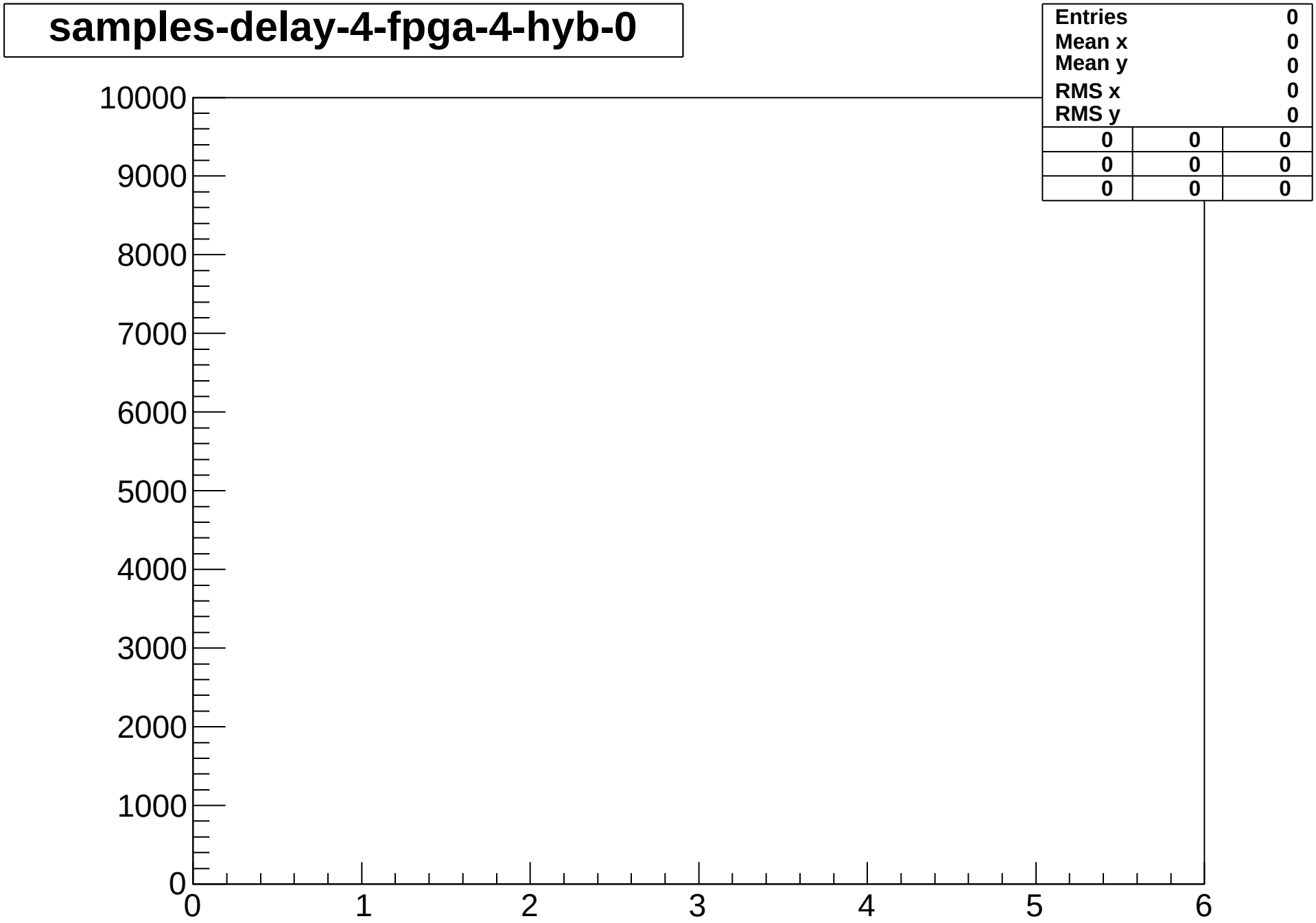
samples-delay-4-fpga-4-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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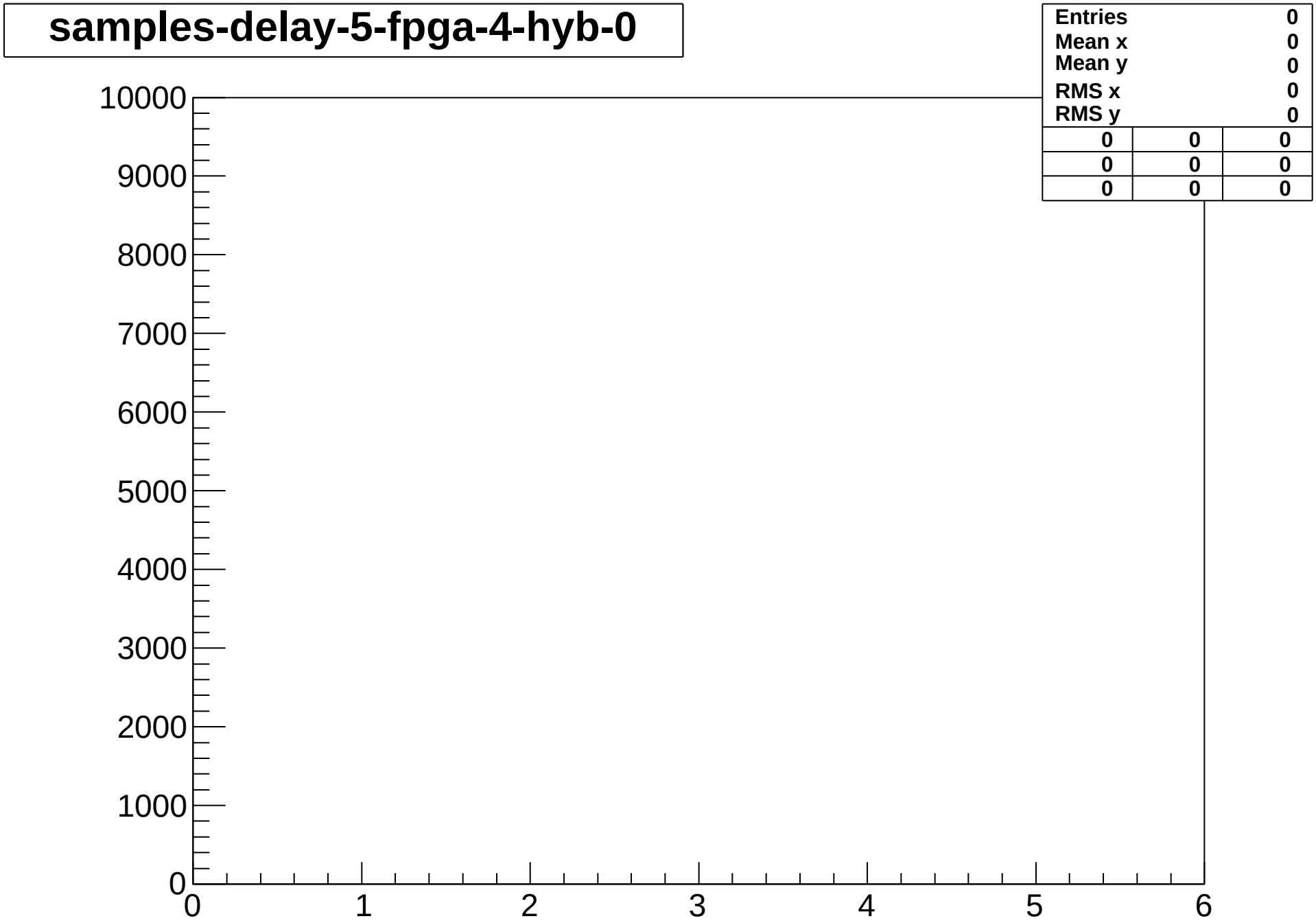
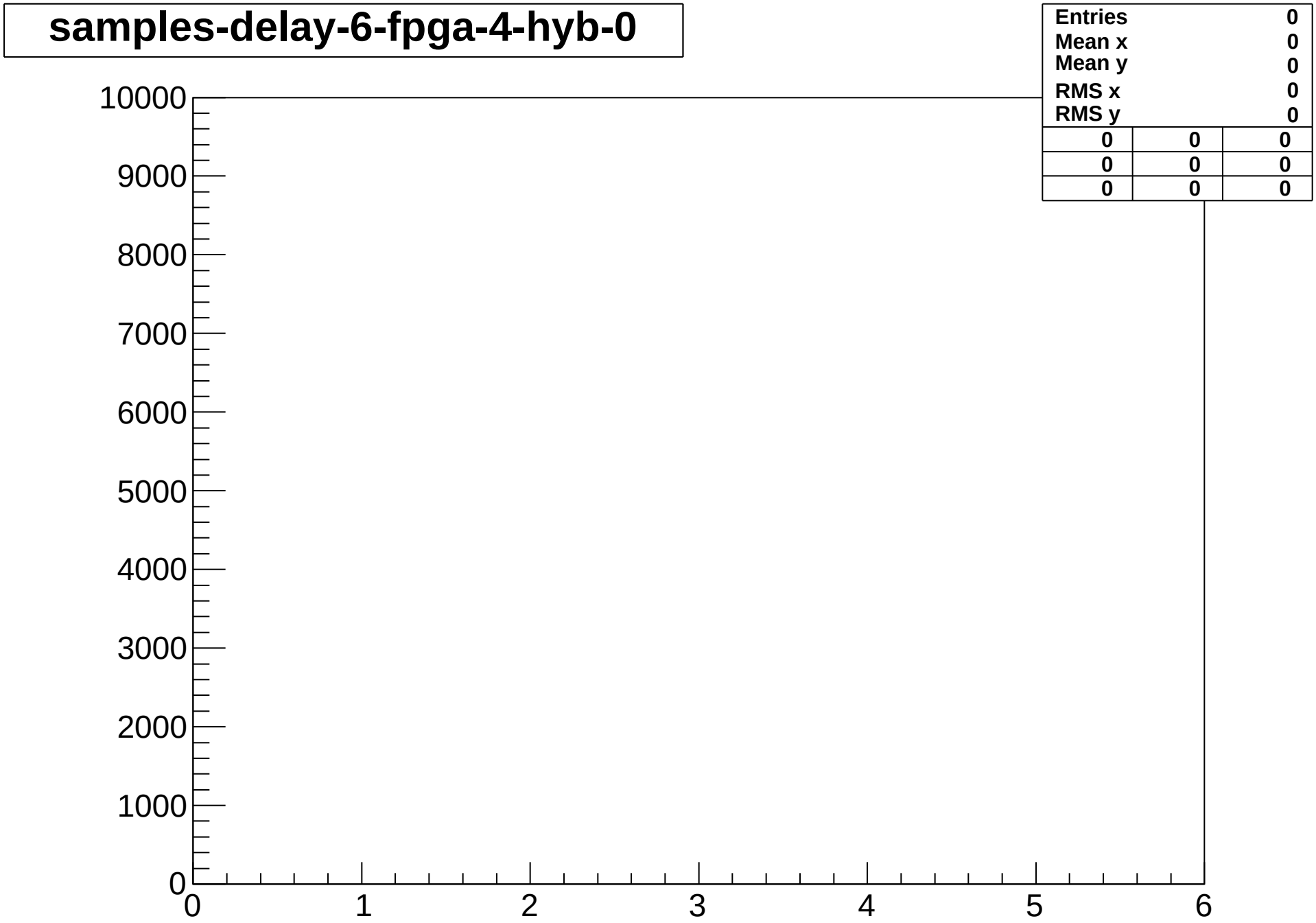
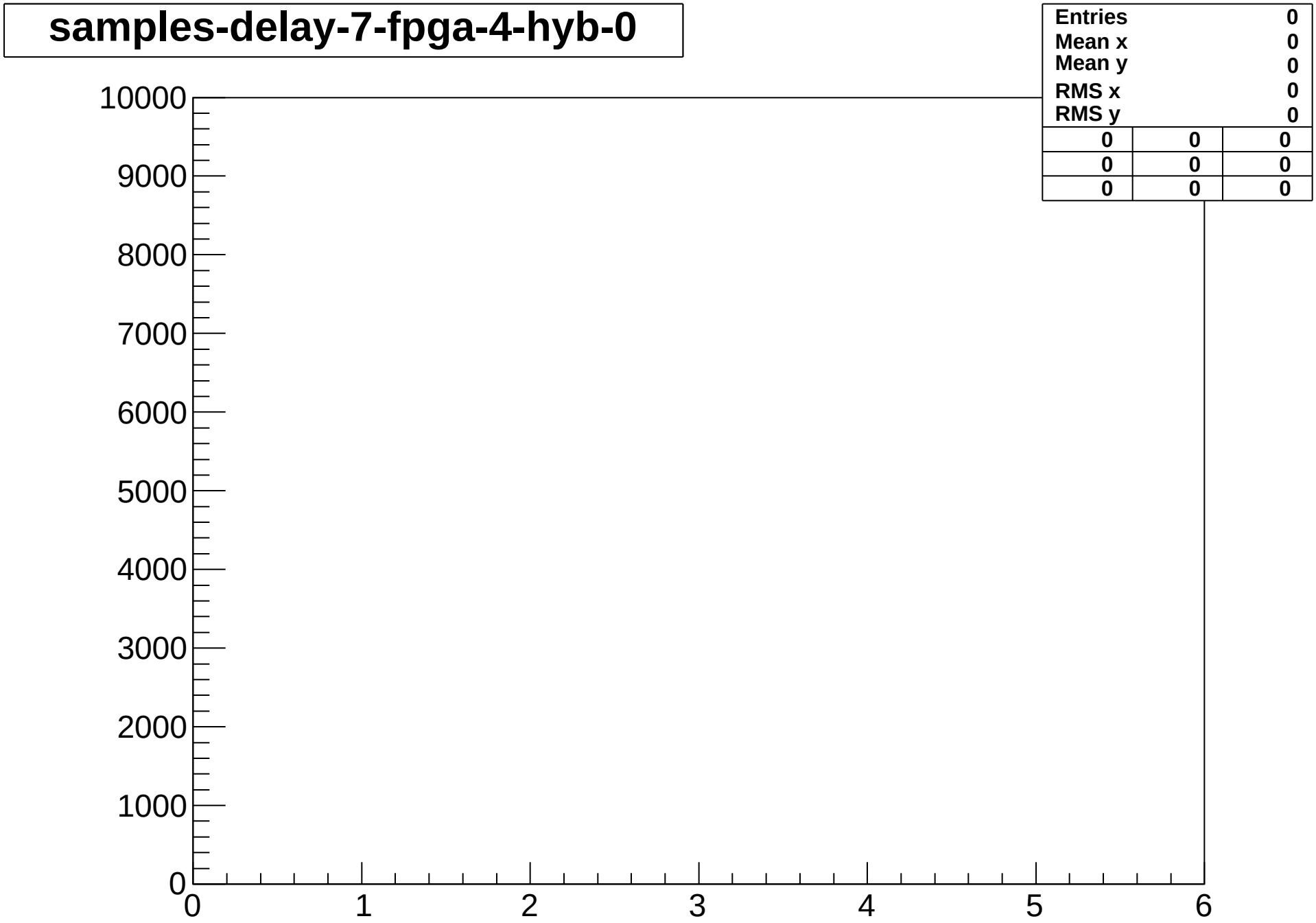
samples-delay-5-fpga-4-hyb-0



samples-delay-6-fpga-4-hyb-0




samples-delay-7-fpga-4-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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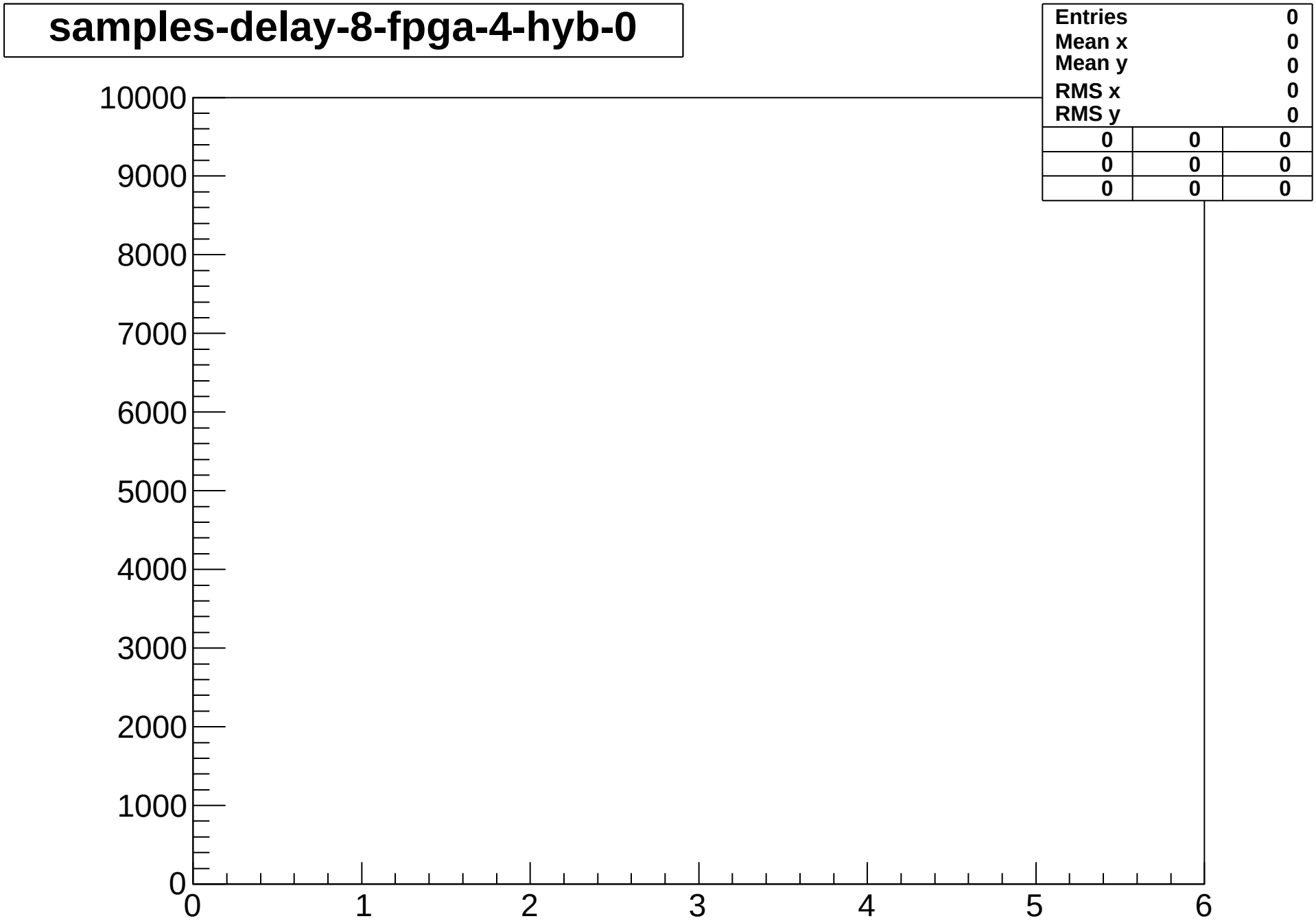
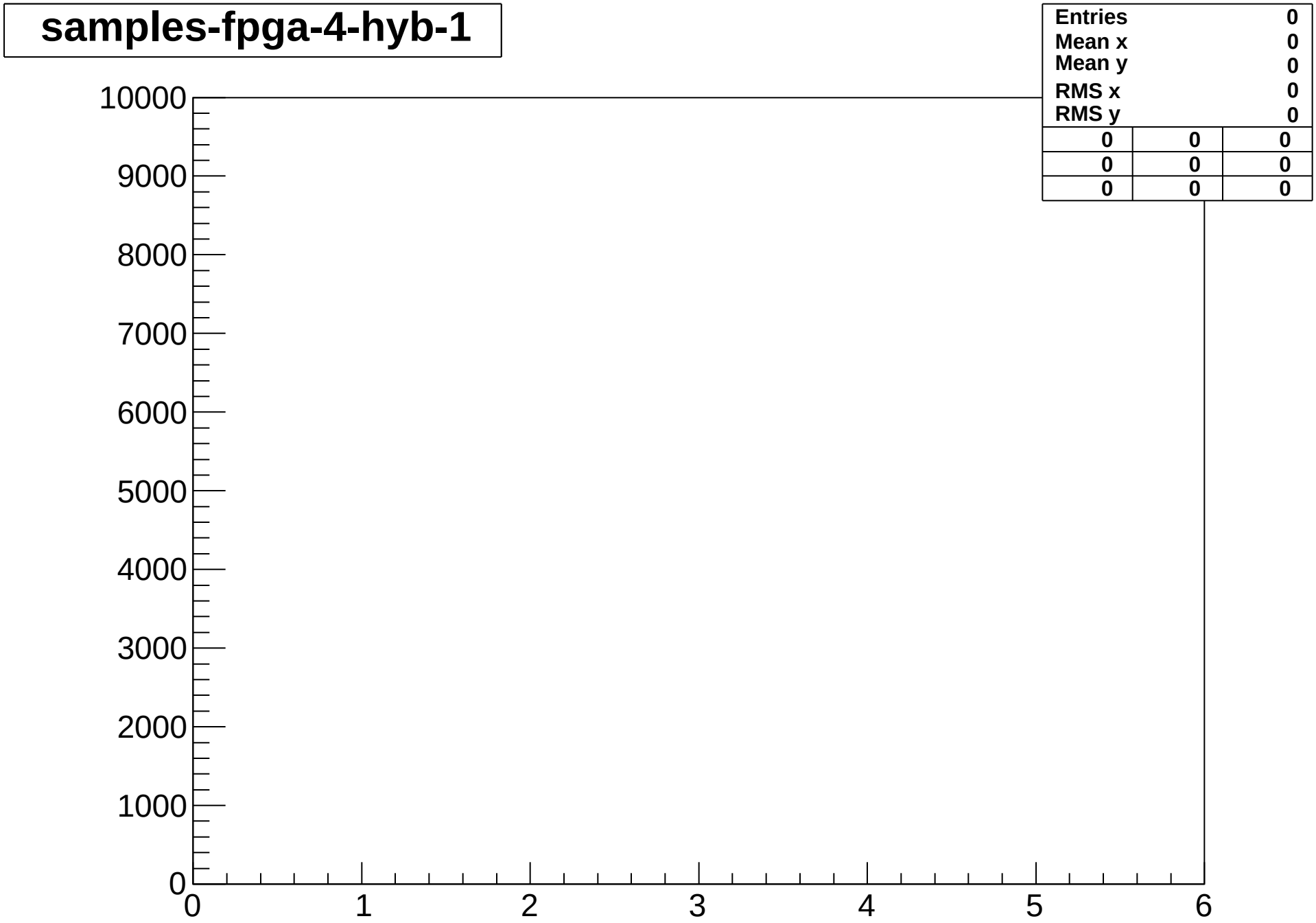
samples-delay-8-fpga-4-hyb-0




samples-fpga-4-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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5000
4000
3000
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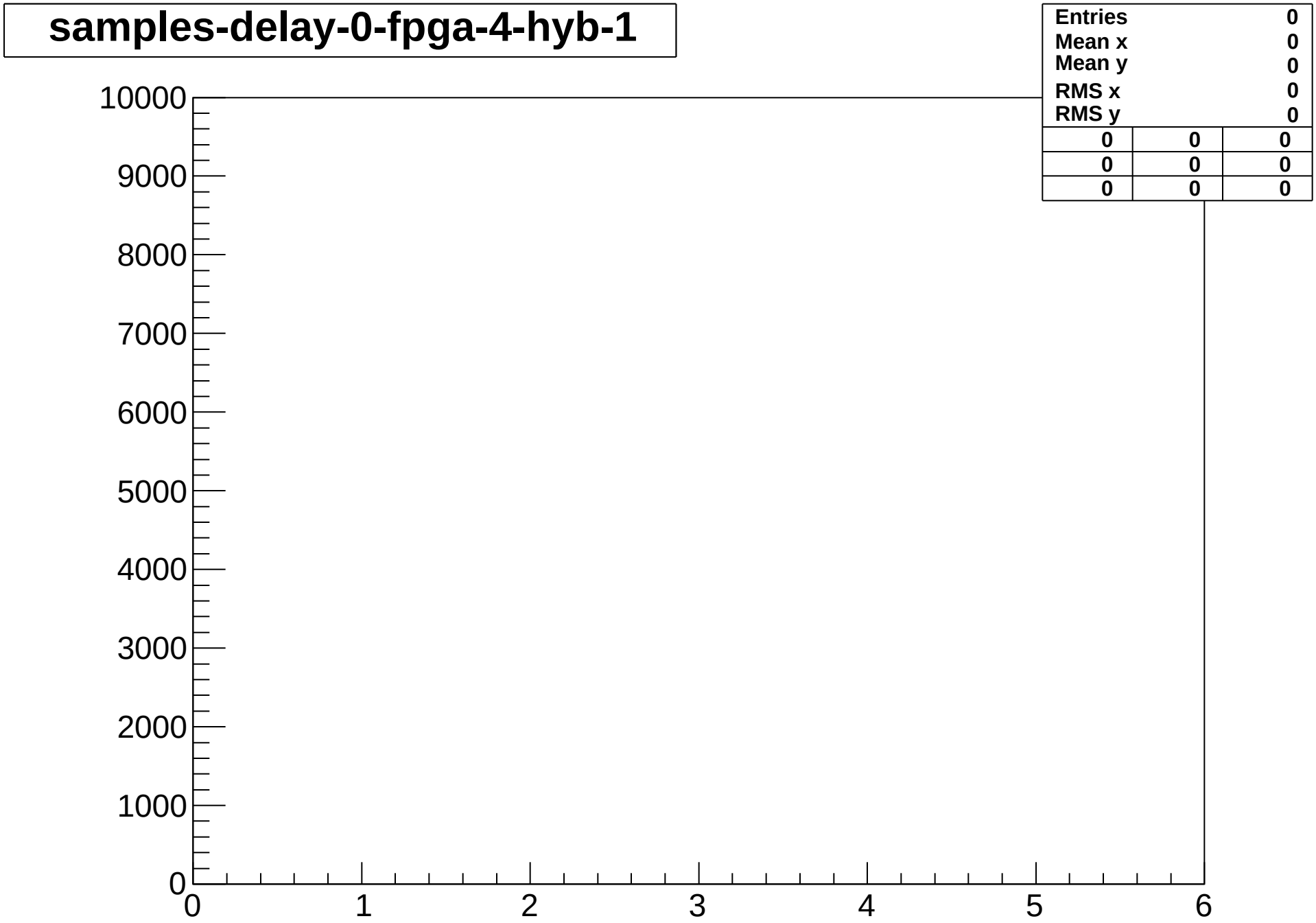
samples-delay-0-fpga-4-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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7000
6000
5000
4000
3000
2000
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0
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1
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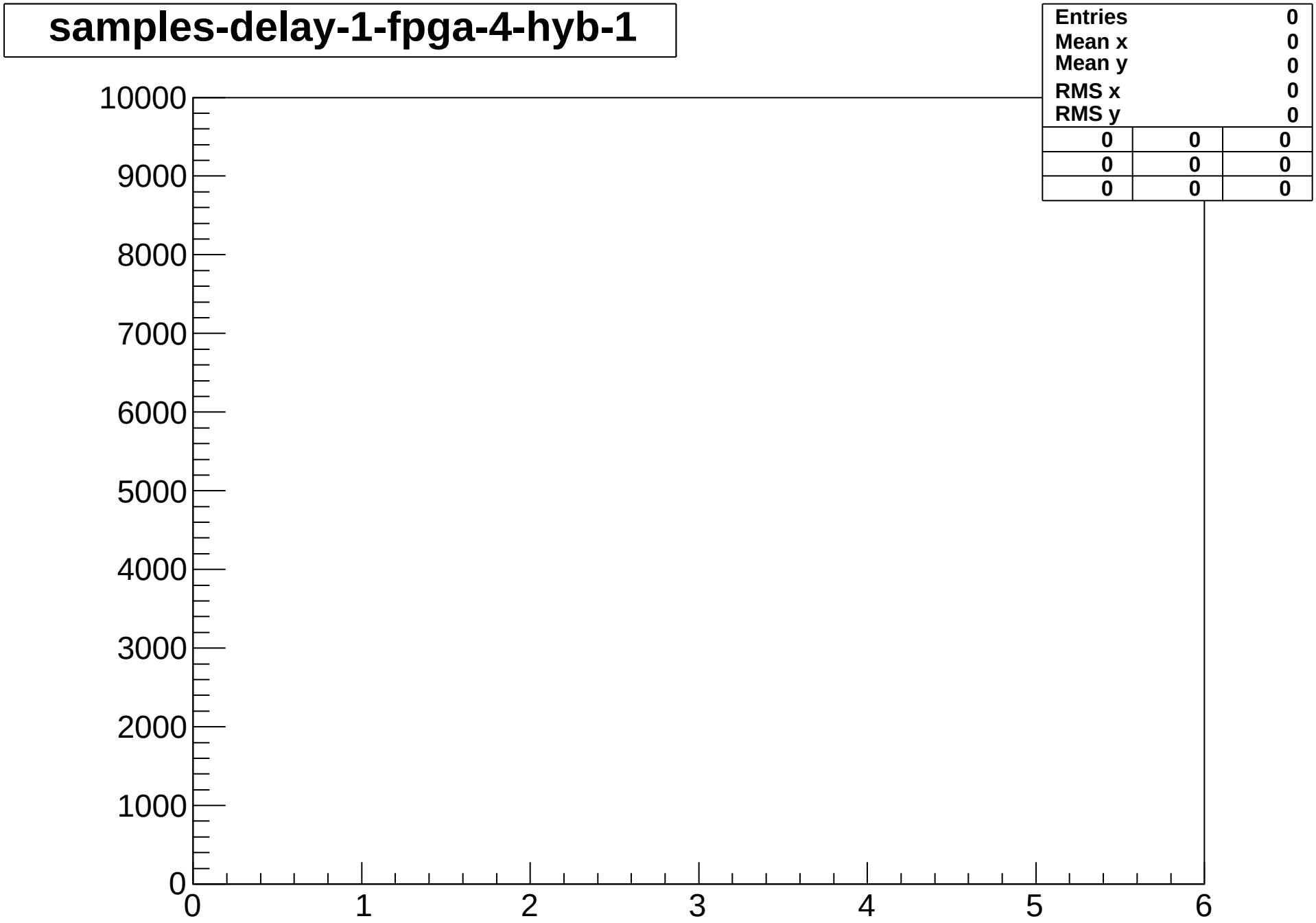
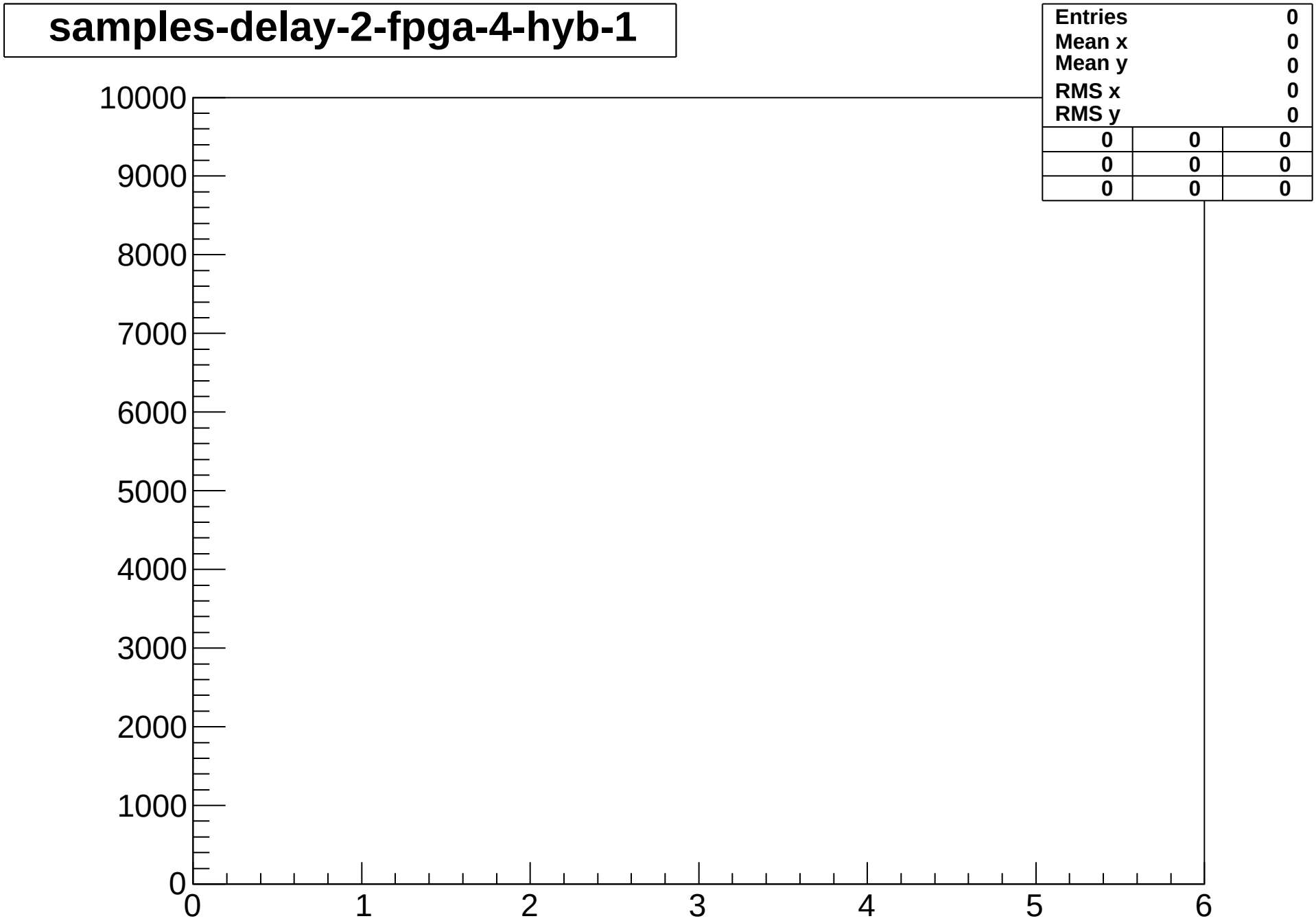
samples-delay-1-fpga-4-hyb-1




samples-delay-2-fpga-4-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
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5000
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3000
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0
1
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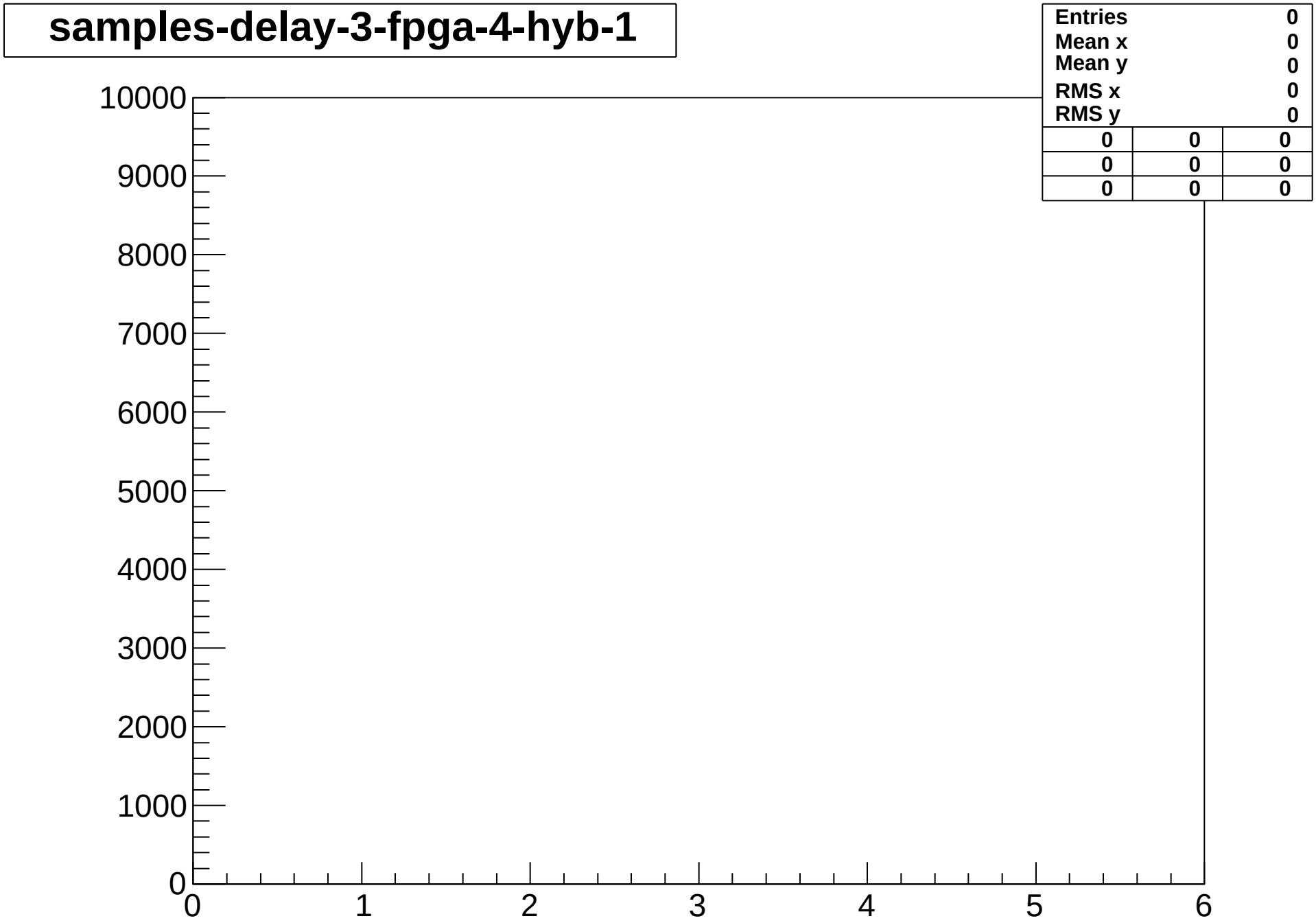
samples-delay-3-fpga-4-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
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3000
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1000
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0
1
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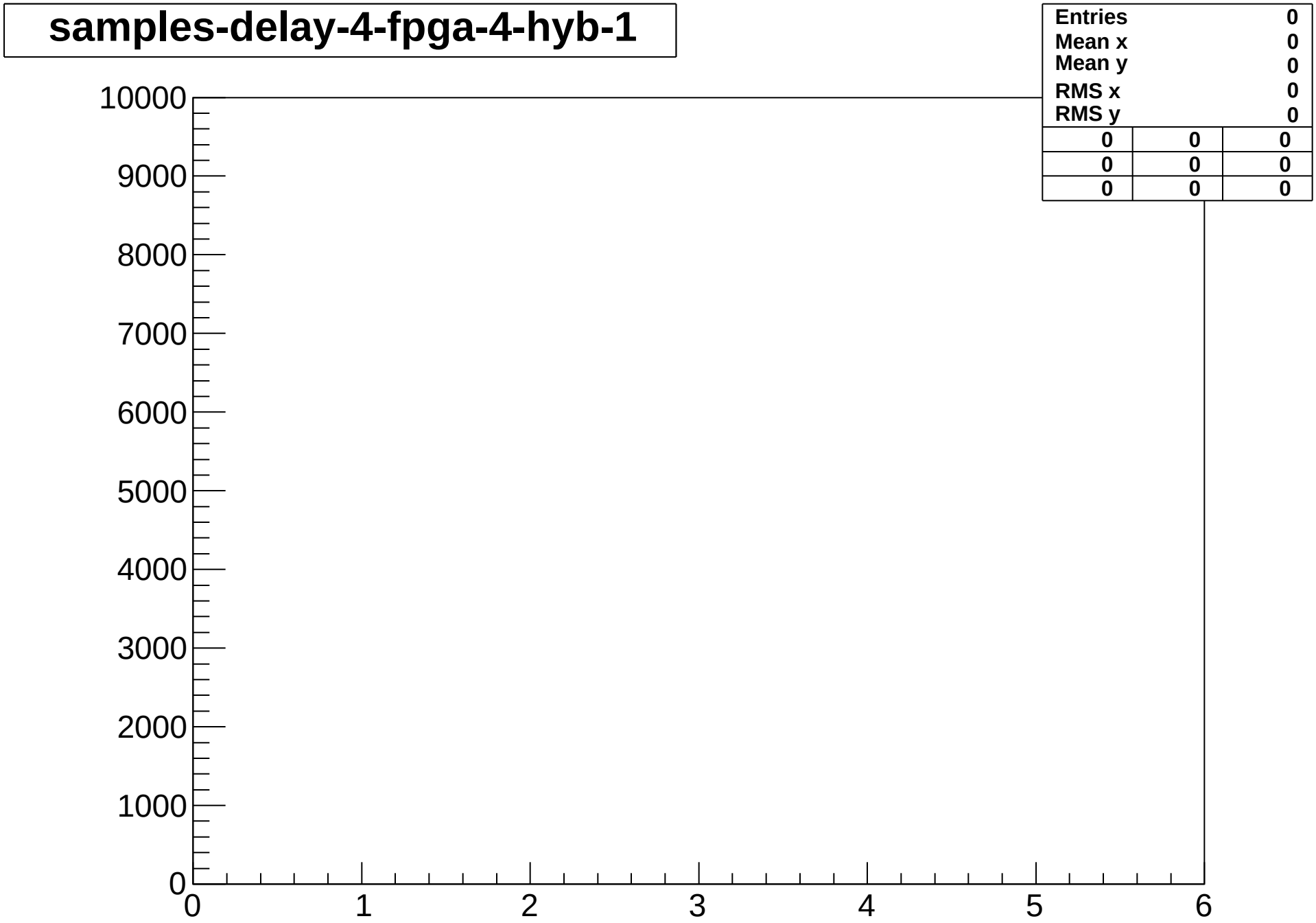
samples-delay-4-fpga-4-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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4
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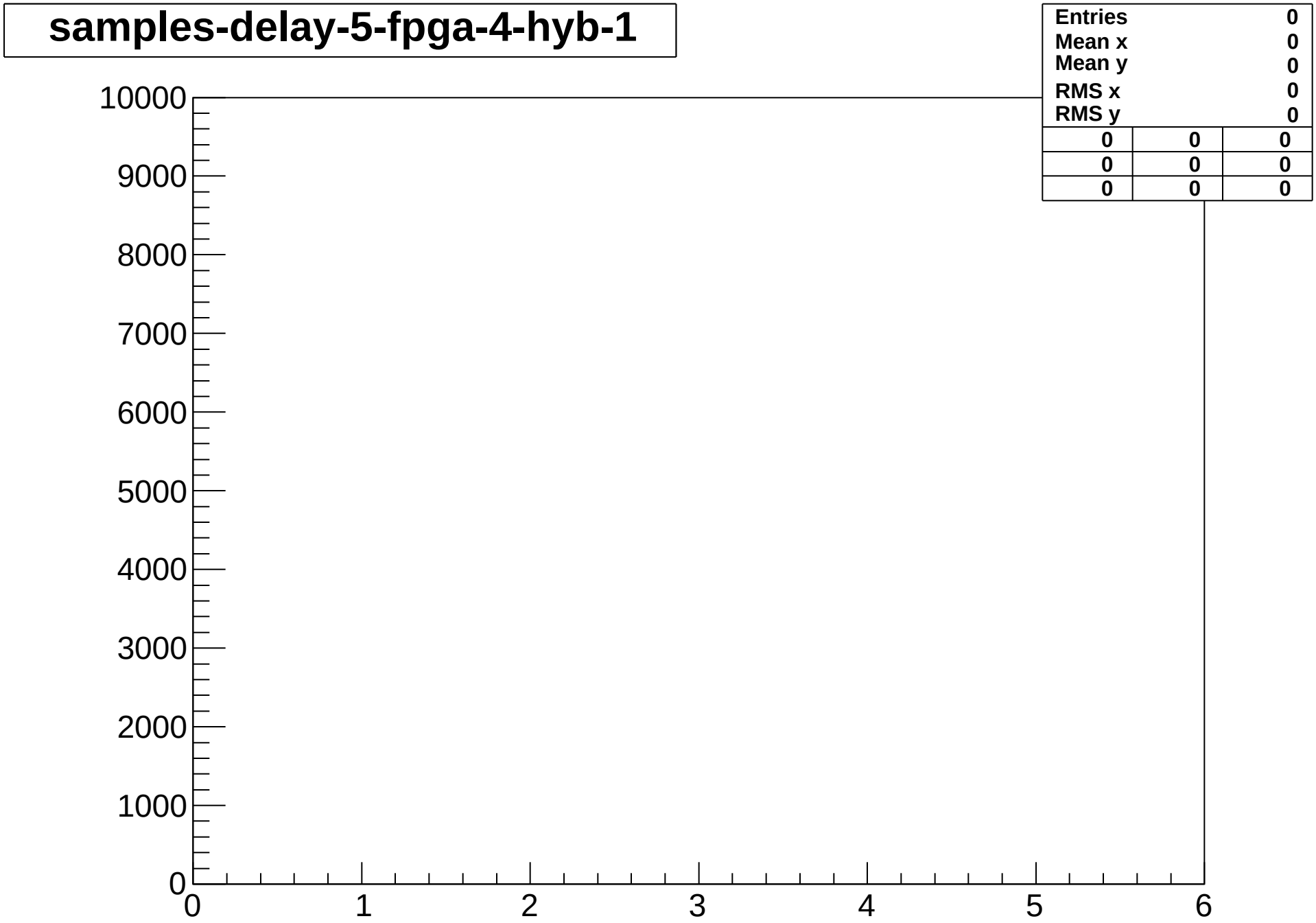
samples-delay-5-fpga-4-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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4000
3000
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1000
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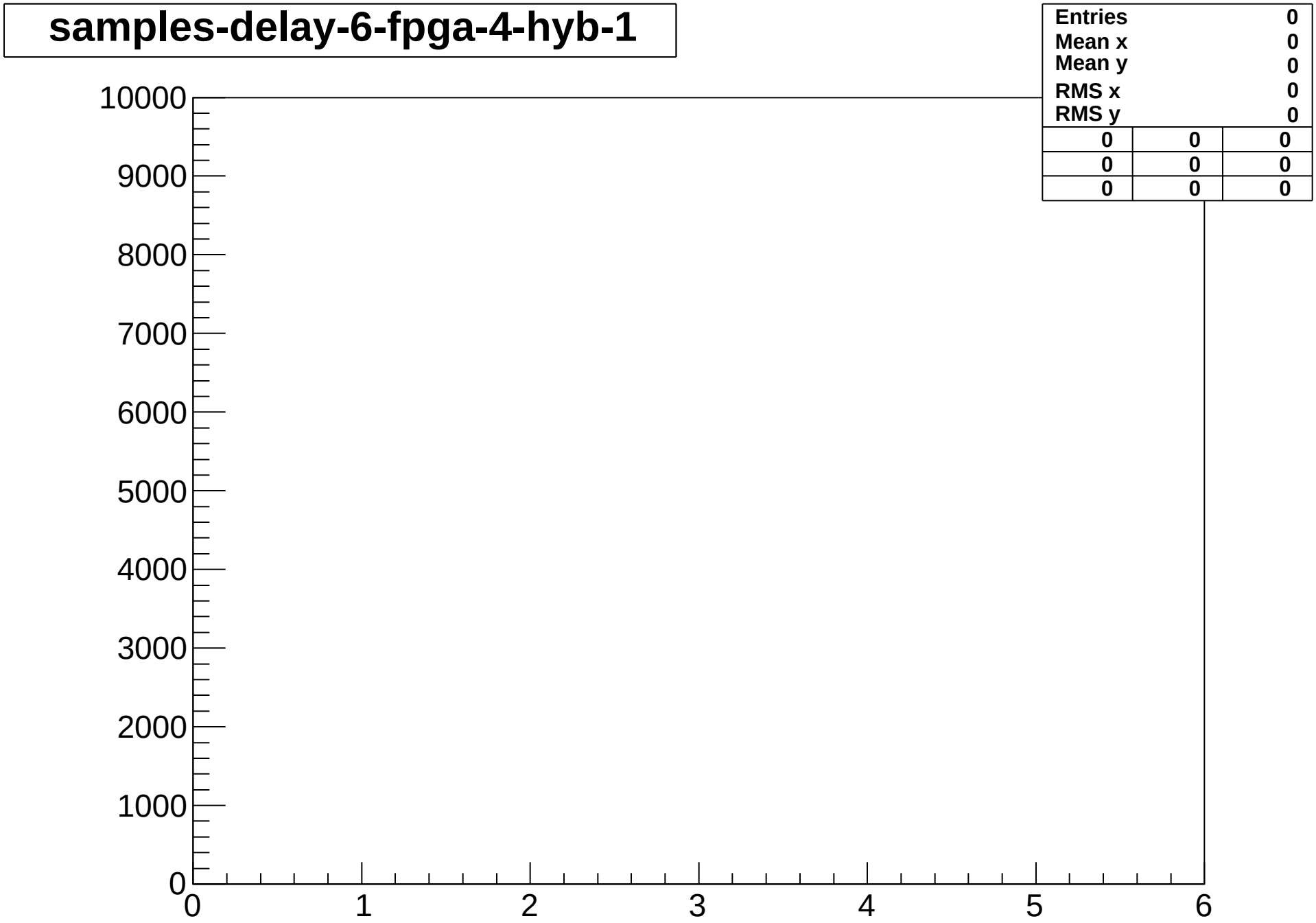
samples-delay-6-fpga-4-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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4000
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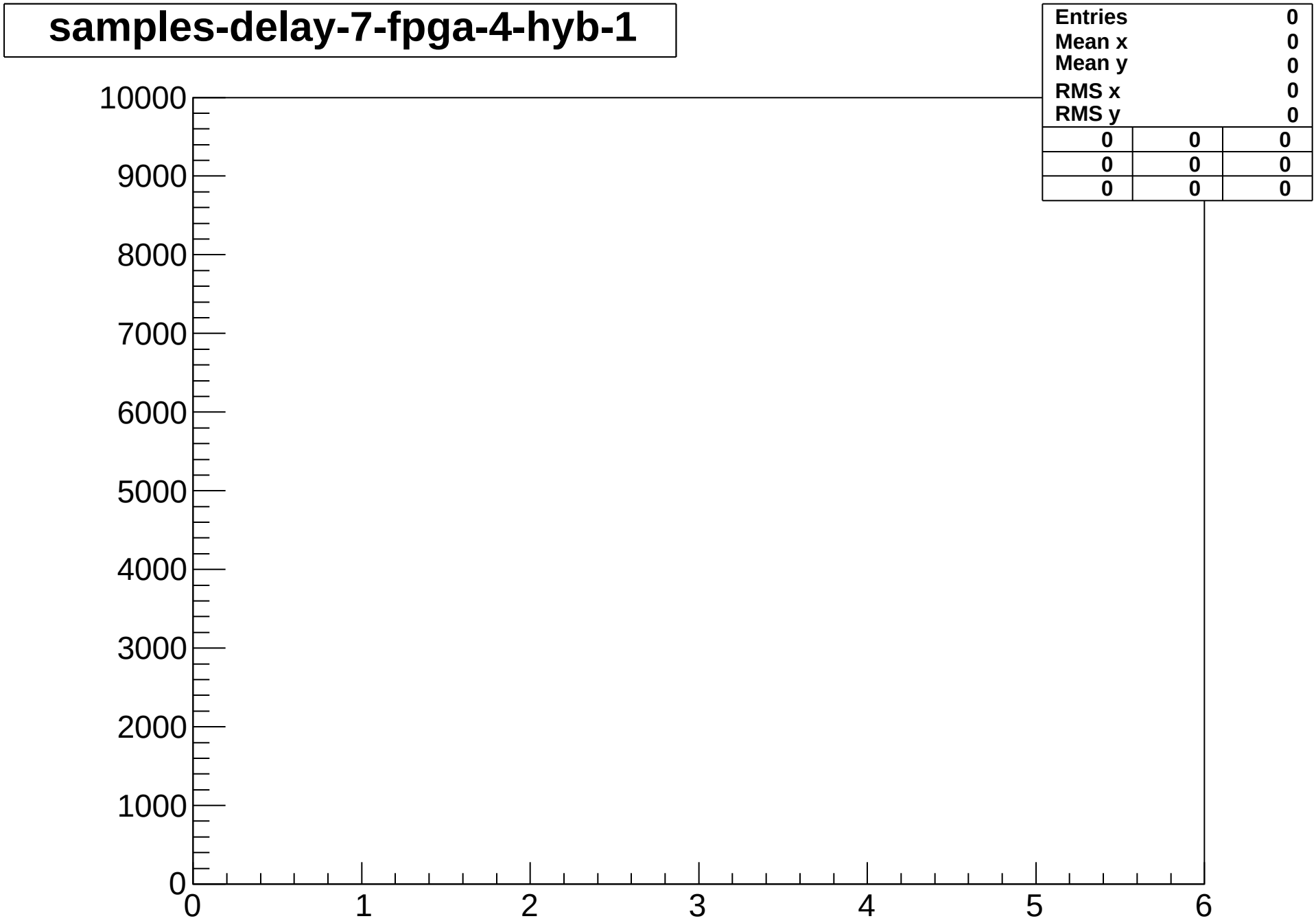
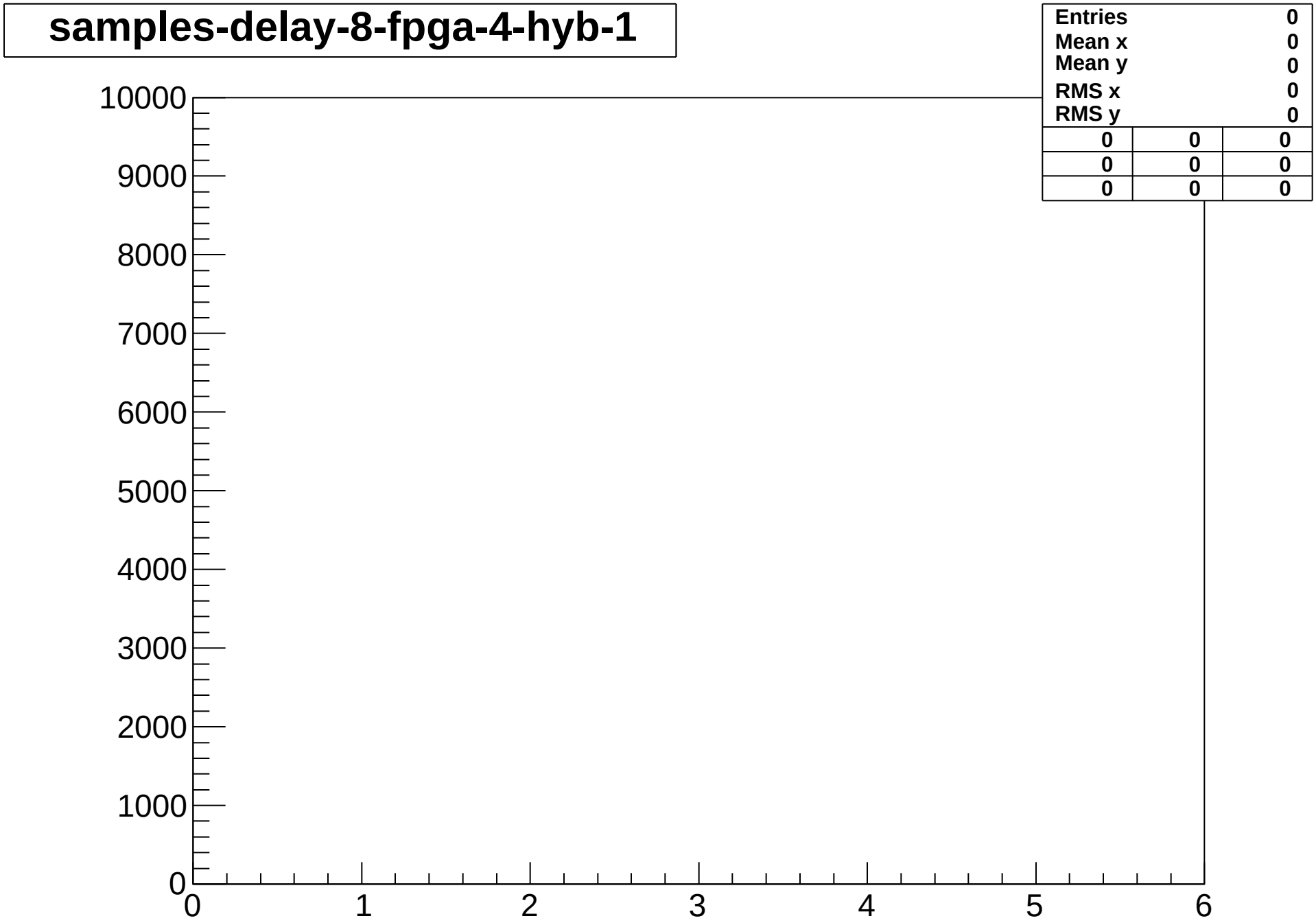
samples-delay-7-fpga-4-hyb-1




samples-delay-8-fpga-4-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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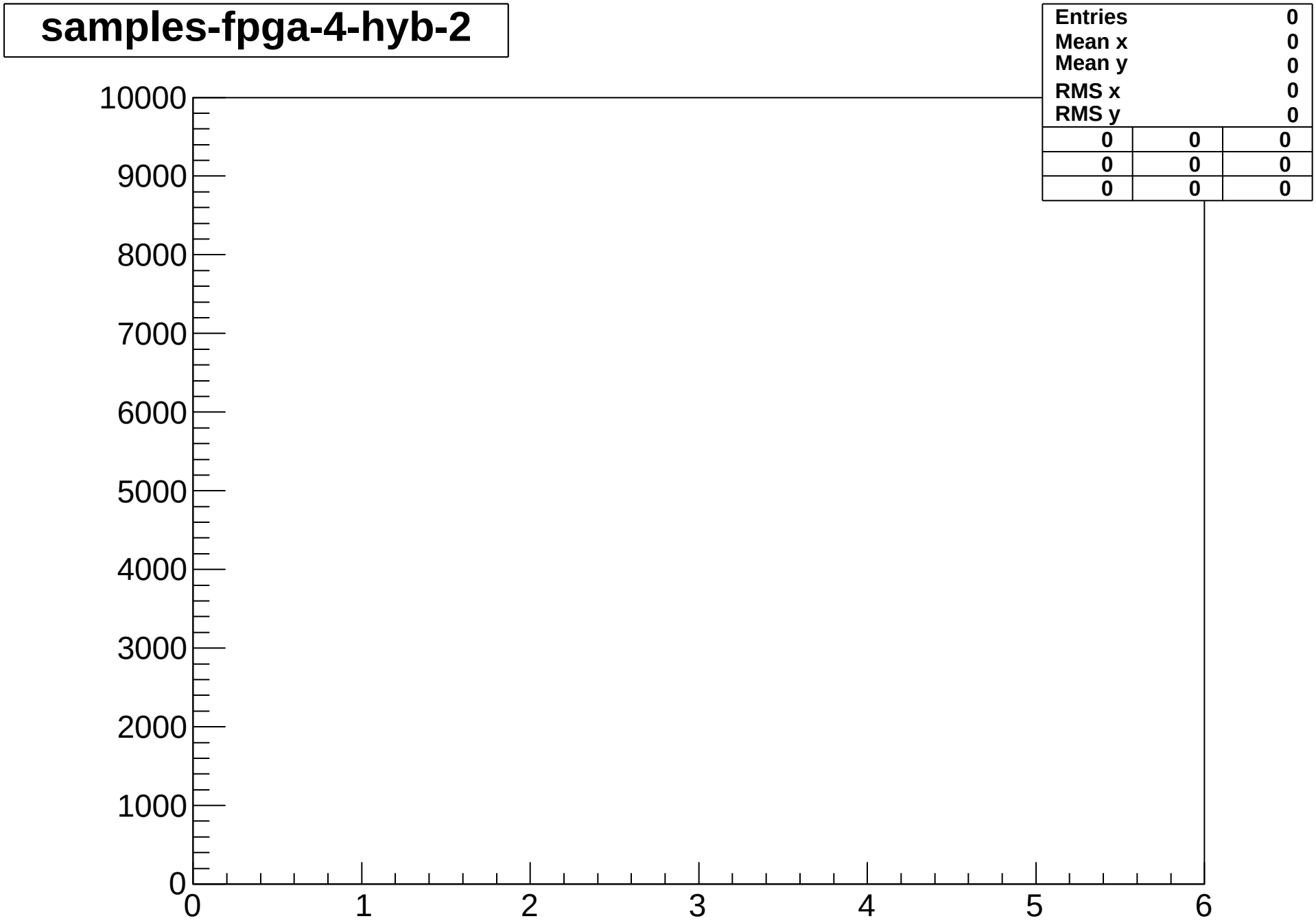
samples-fpga-4-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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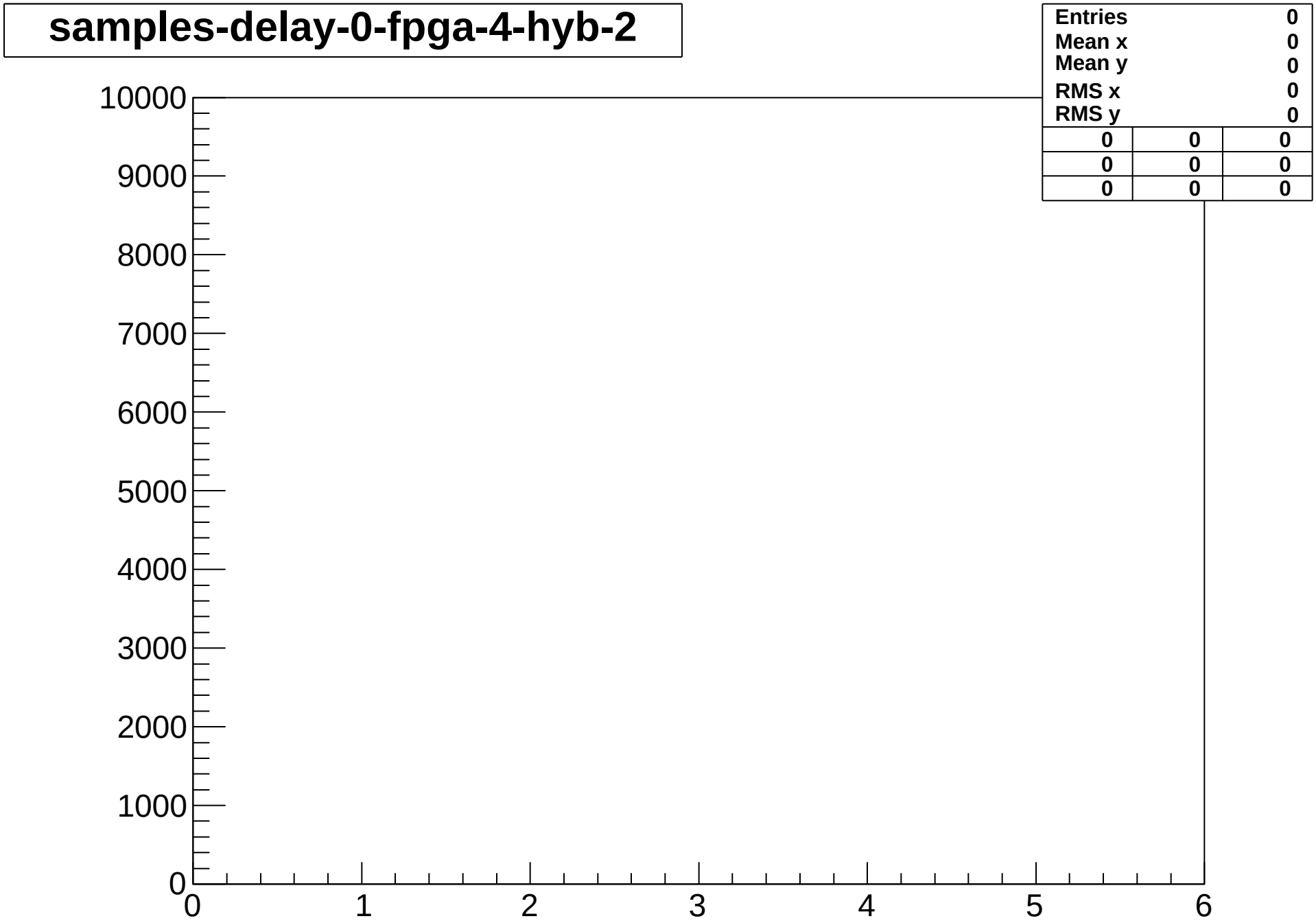
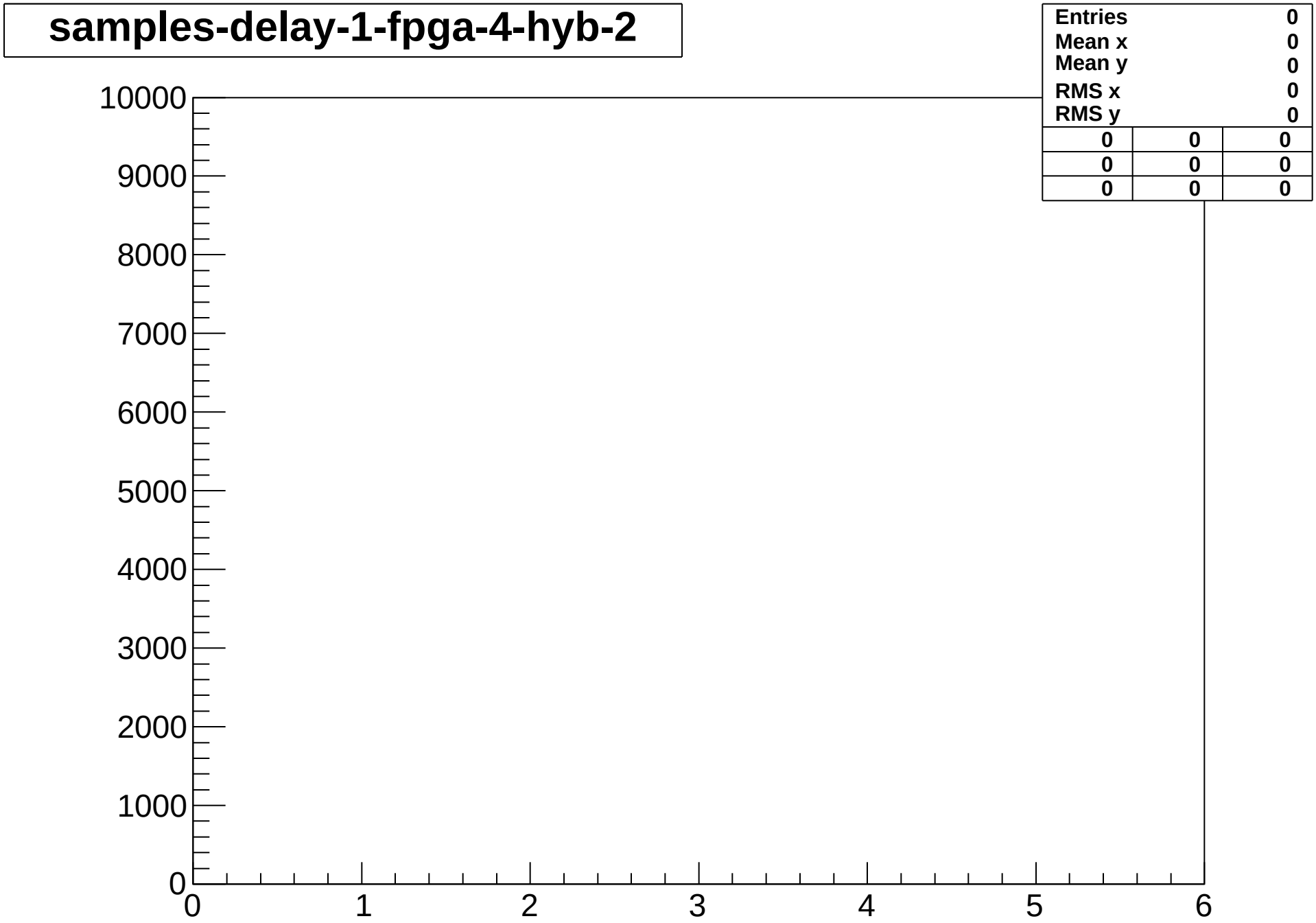
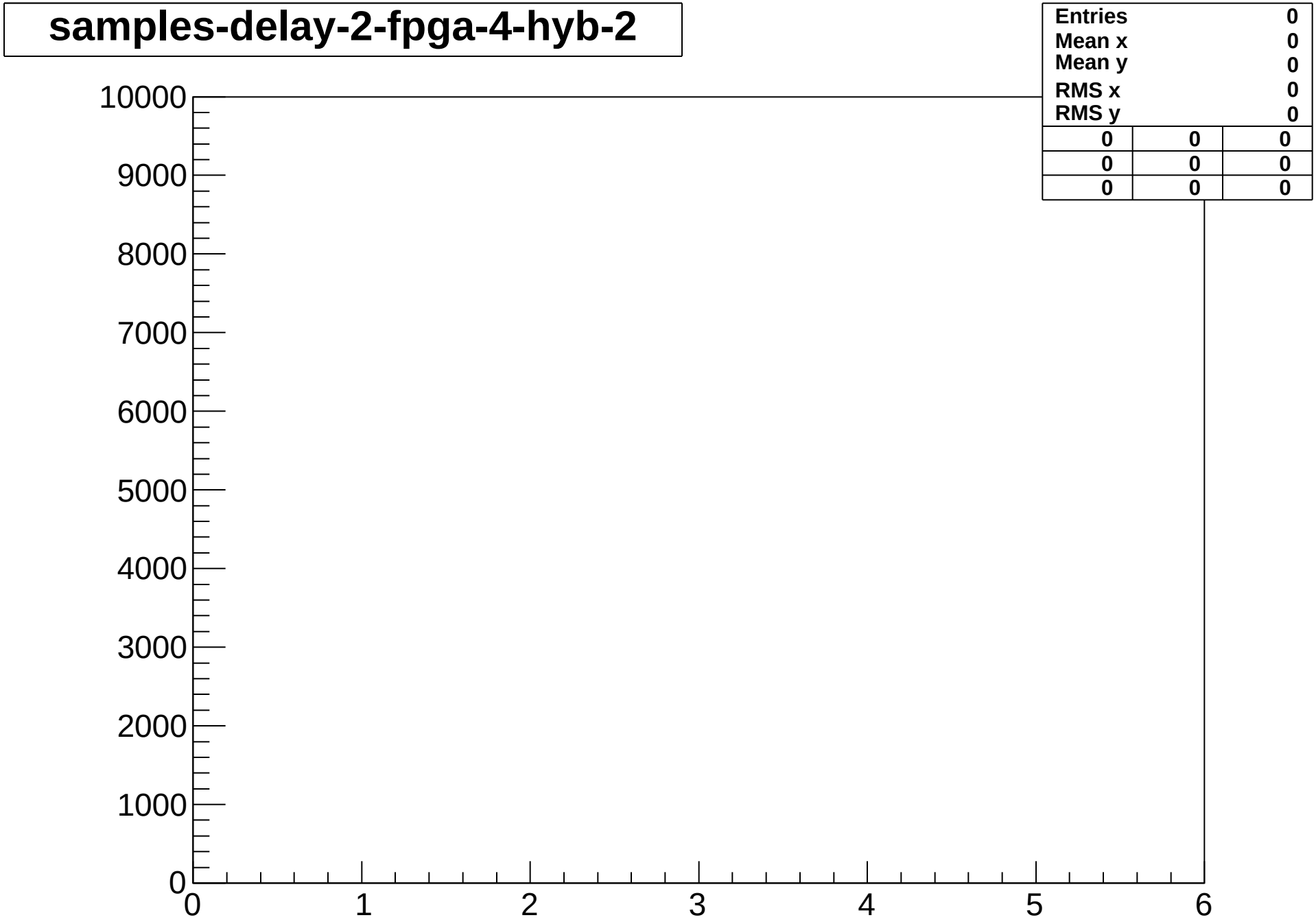
samples-delay-0-fpga-4-hyb-2

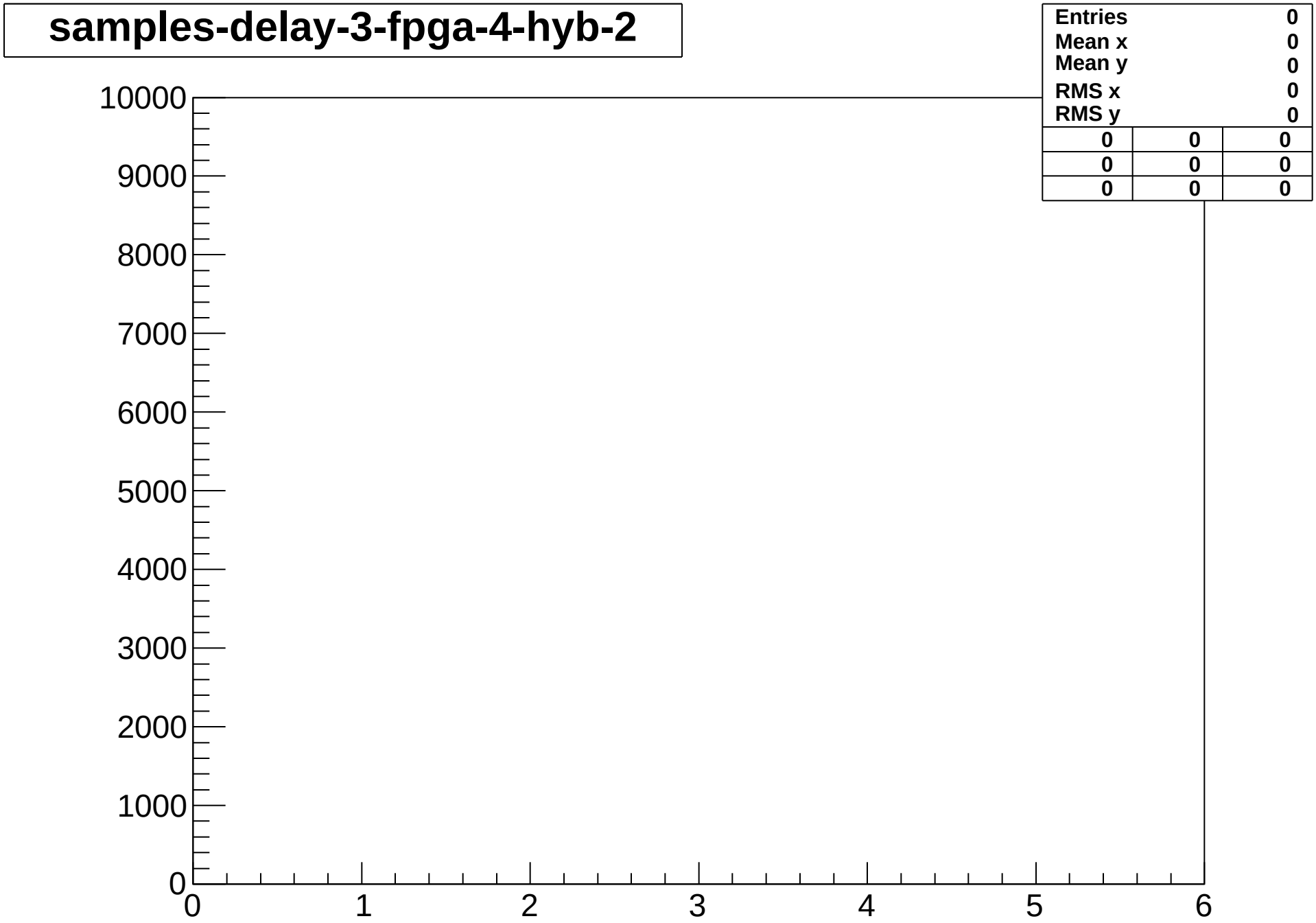


samples-delay-1-fpga-4-hyb-2



samples-delay-2-fpga-4-hyb-2




samples-delay-3-fpga-4-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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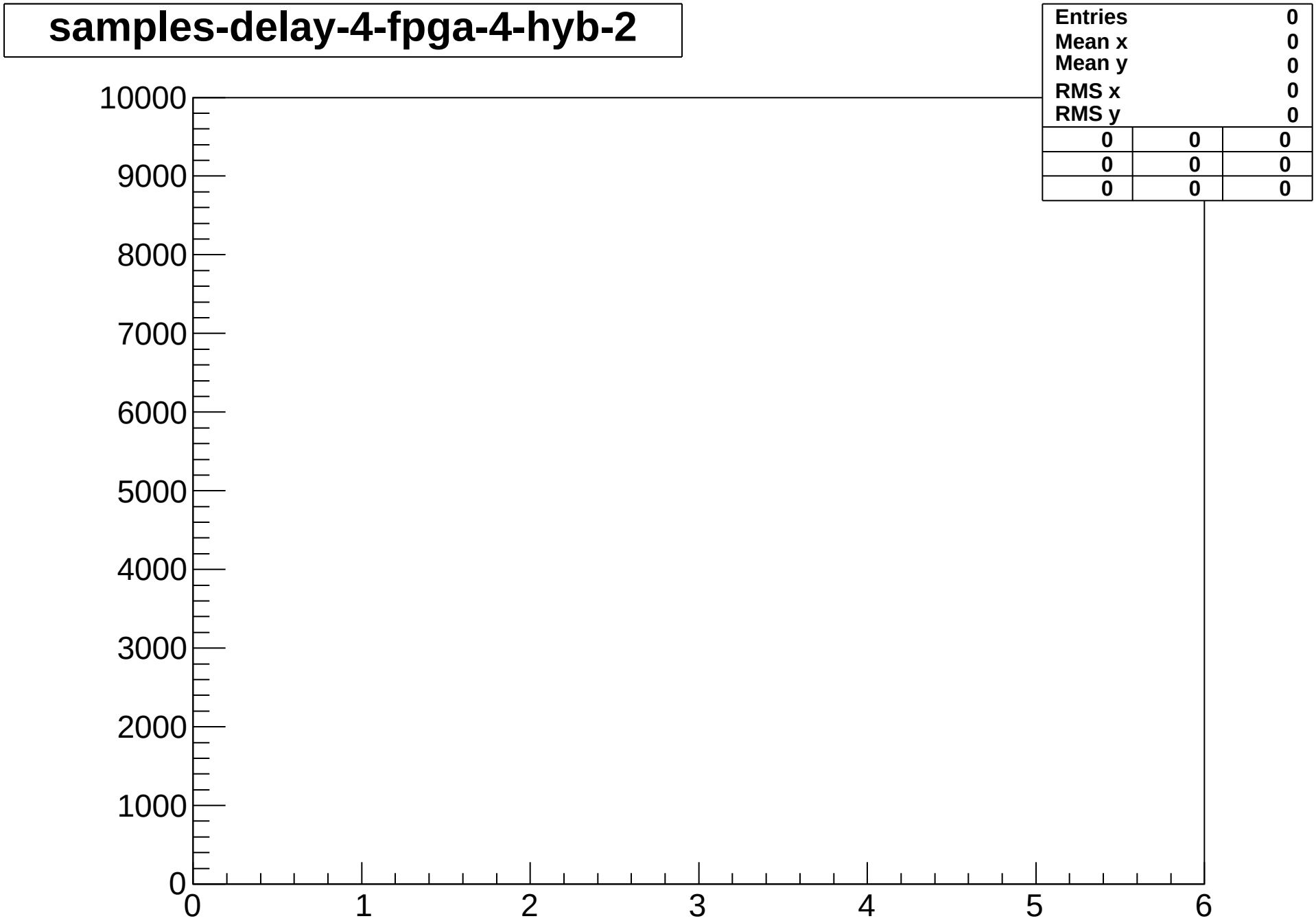
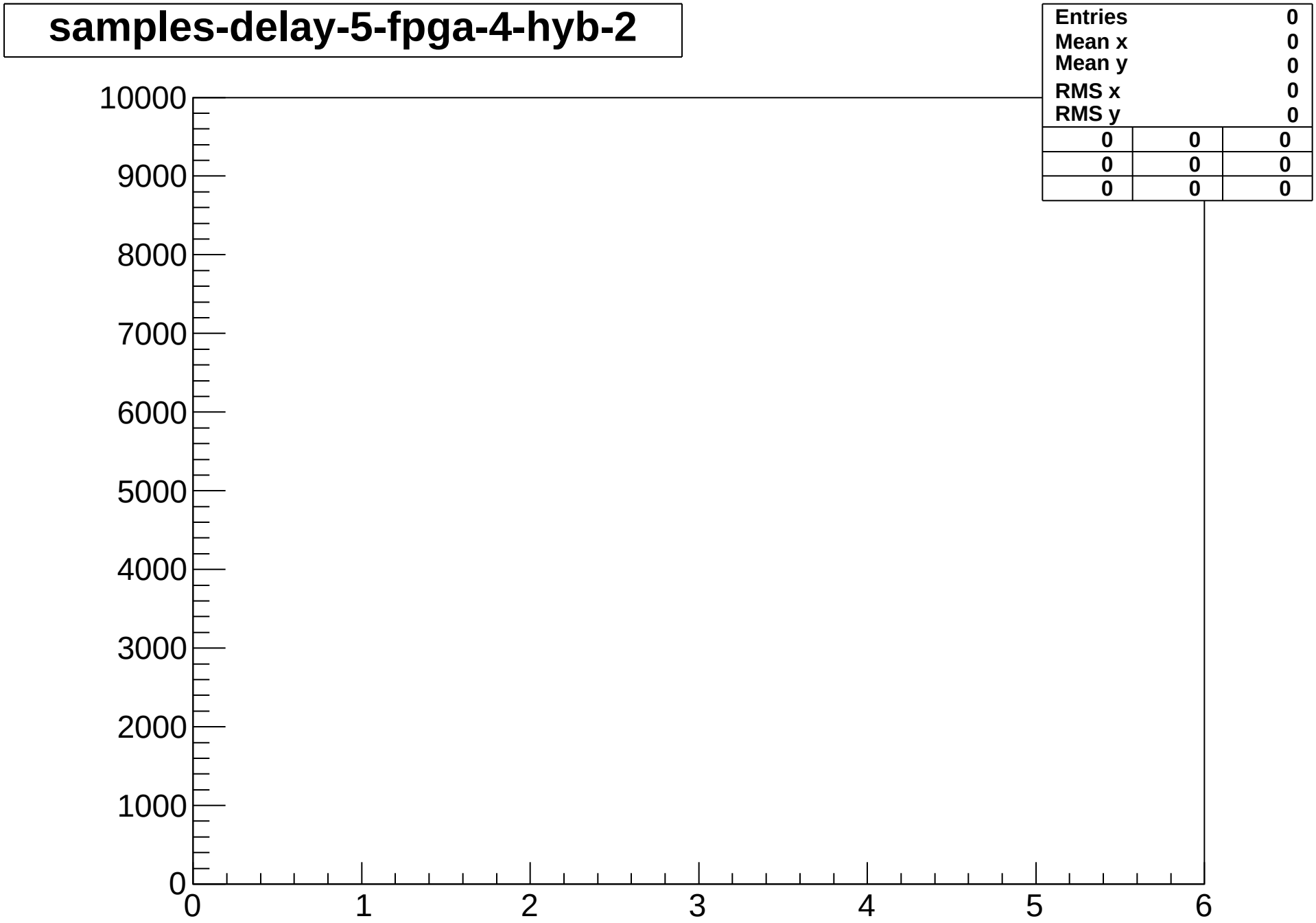
samples-delay-4-fpga-4-hyb-2




samples-delay-5-fpga-4-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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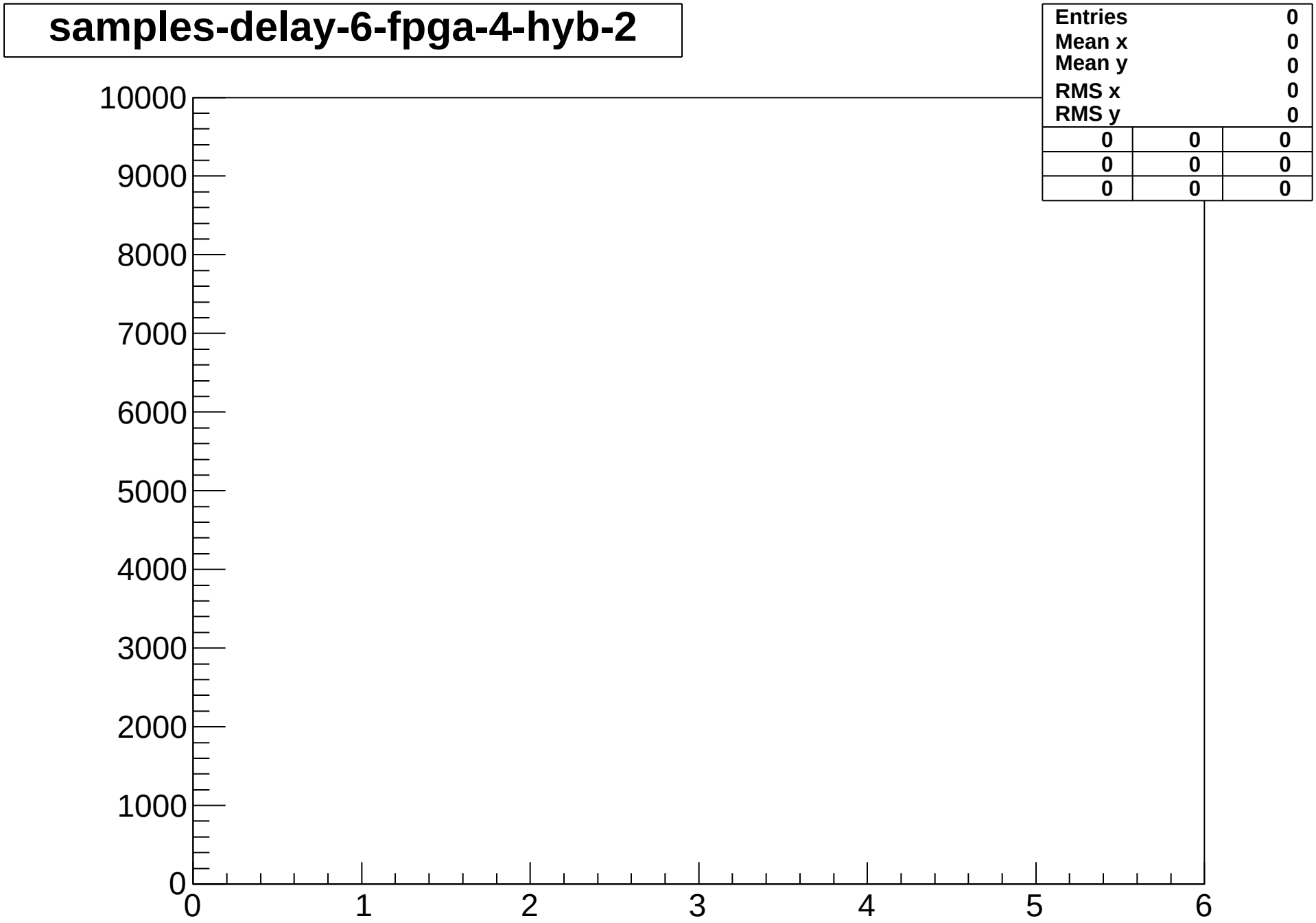
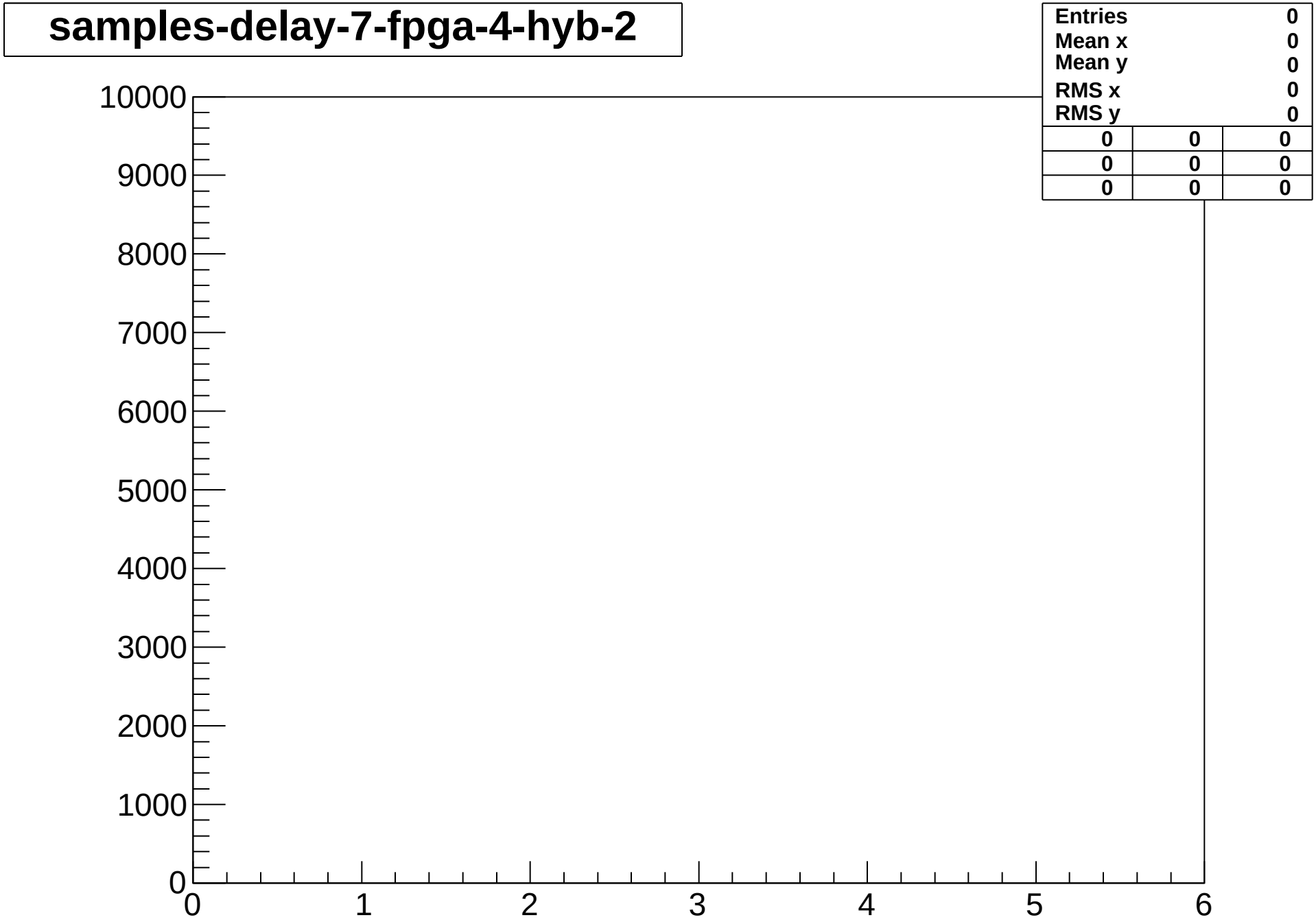
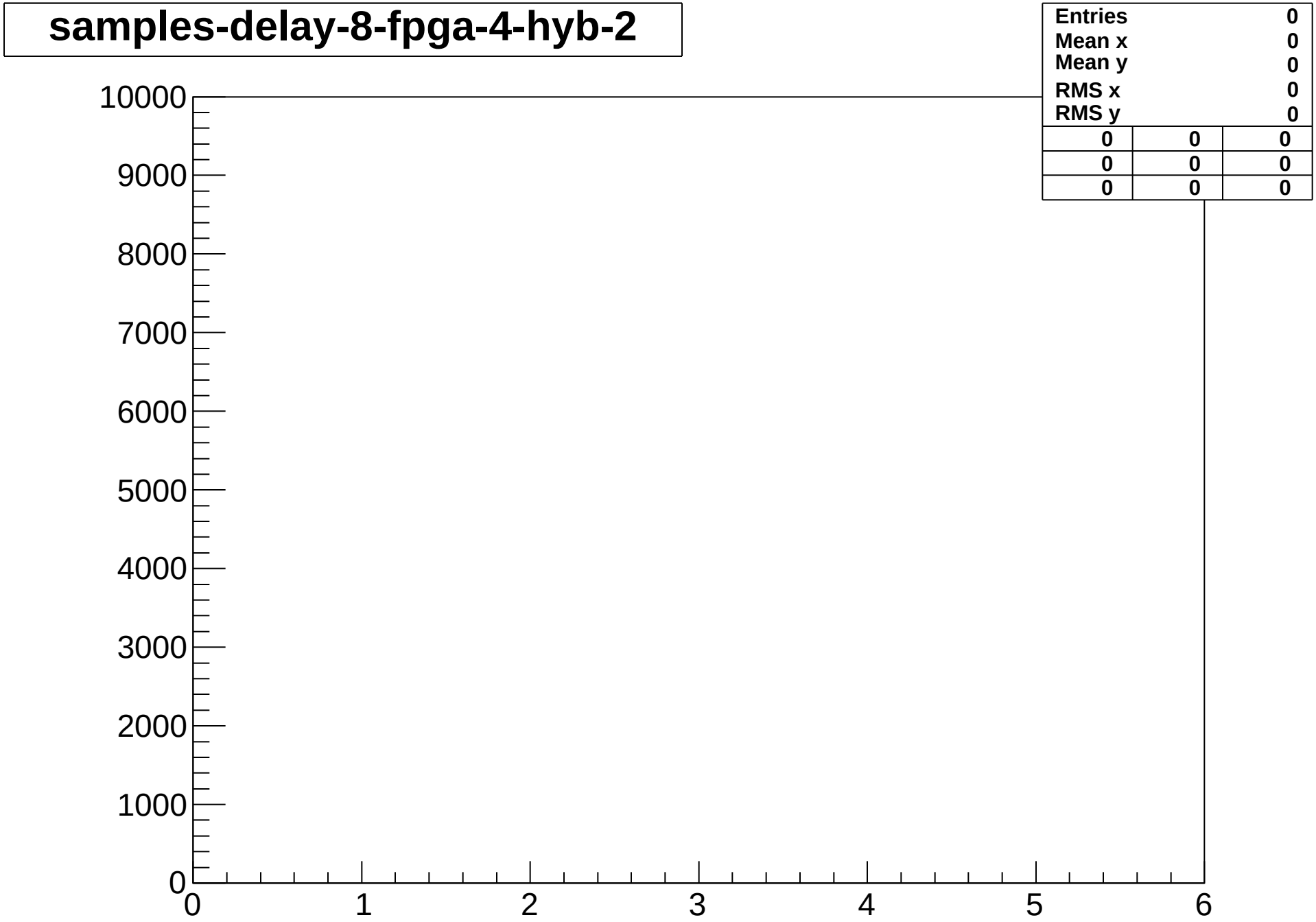
samples-delay-6-fpga-4-hyb-2

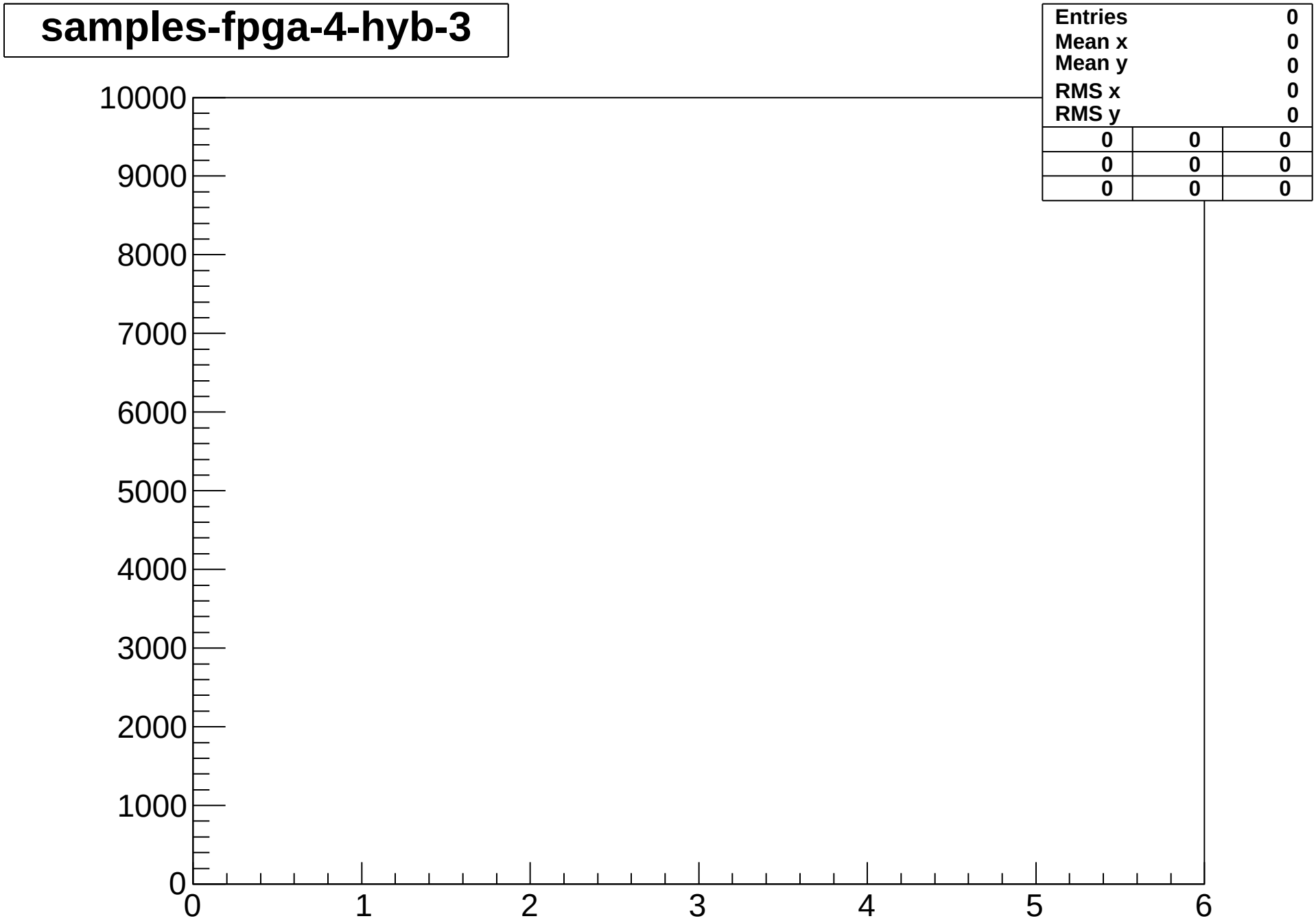


samples-delay-7-fpga-4-hyb-2



samples-delay-8-fpga-4-hyb-2




samples-fpga-4-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
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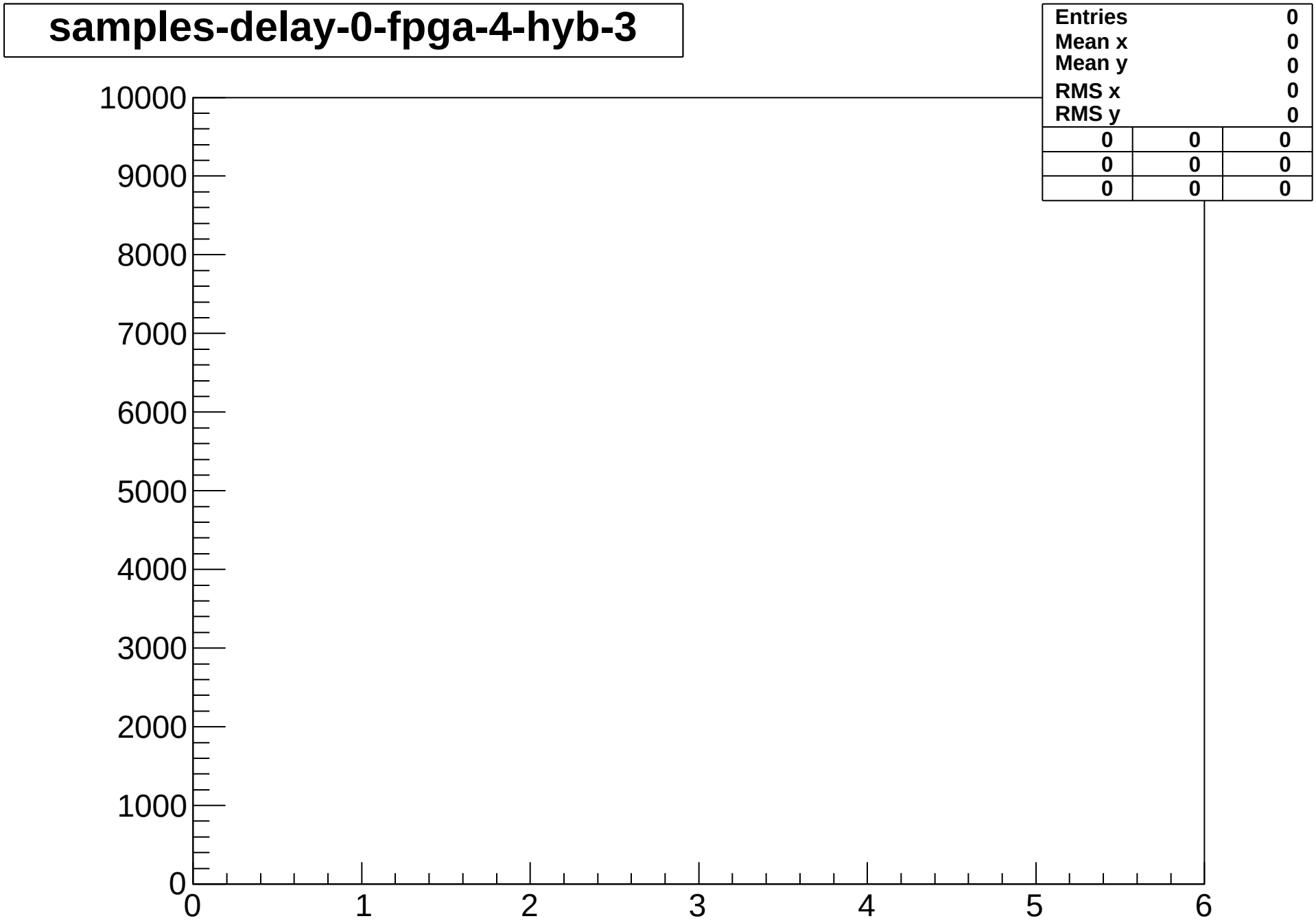
samples-delay-0-fpga-4-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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6000
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4000
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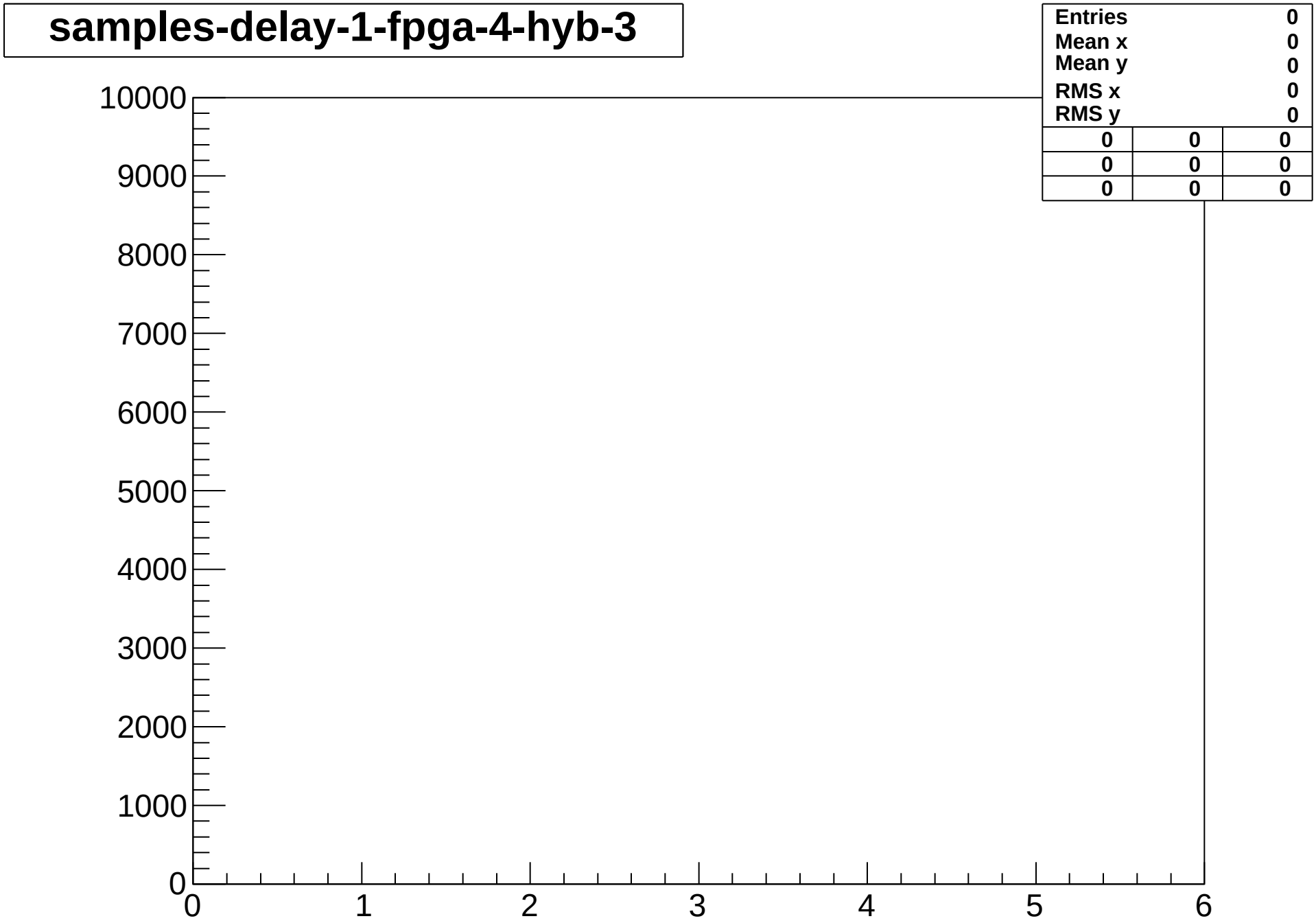
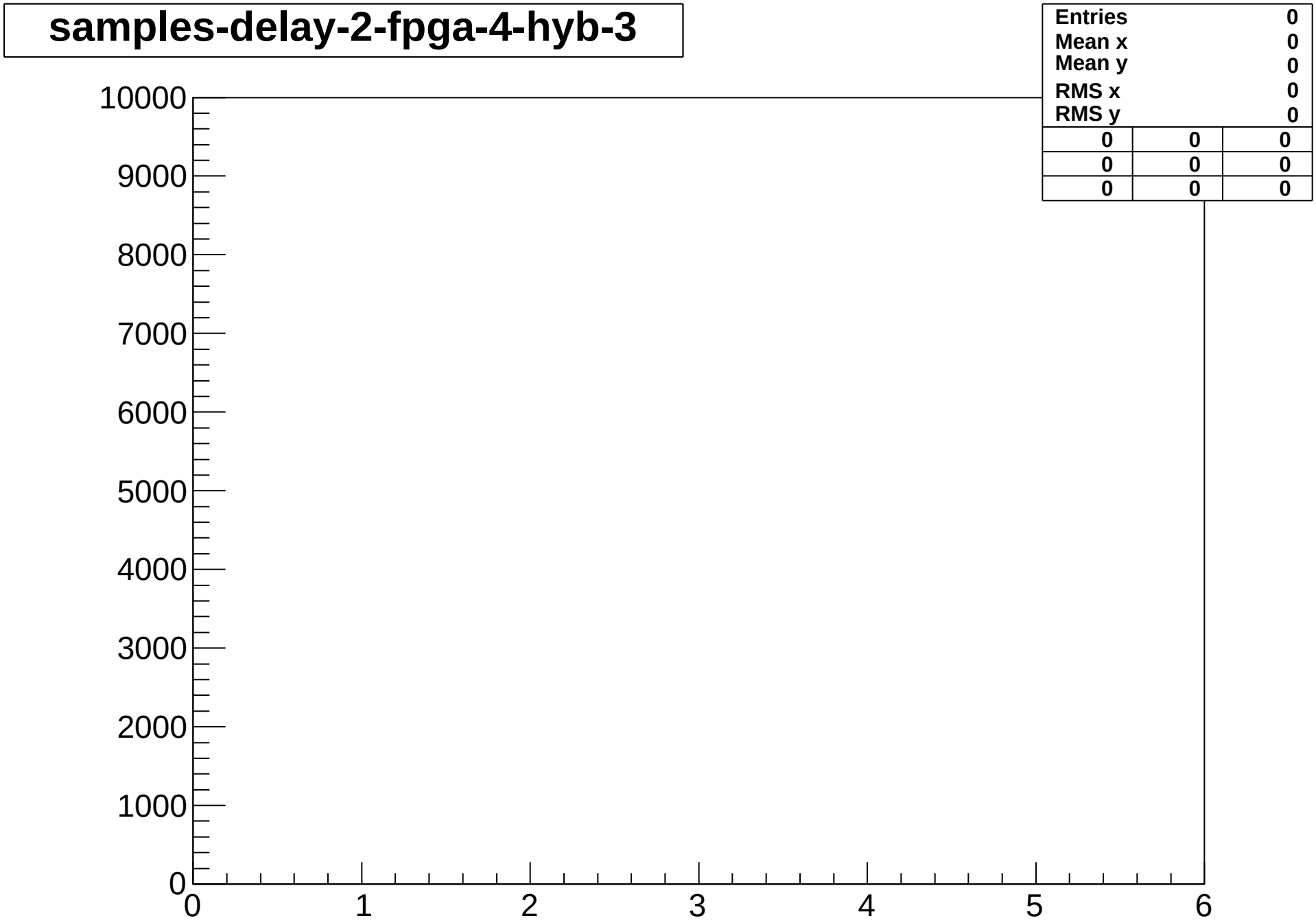
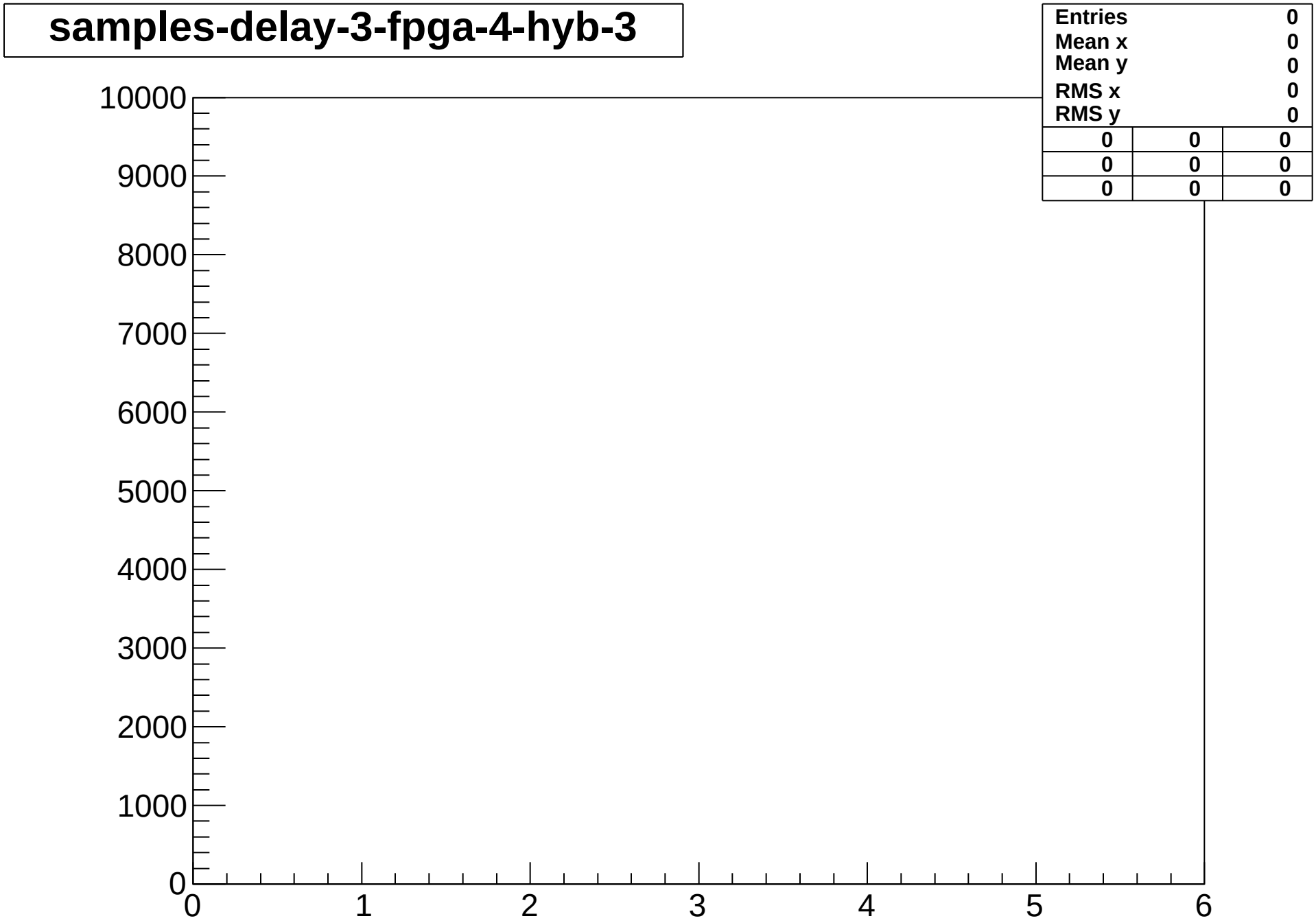
samples-delay-1-fpga-4-hyb-3



samples-delay-2-fpga-4-hyb-3




samples-delay-3-fpga-4-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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6000
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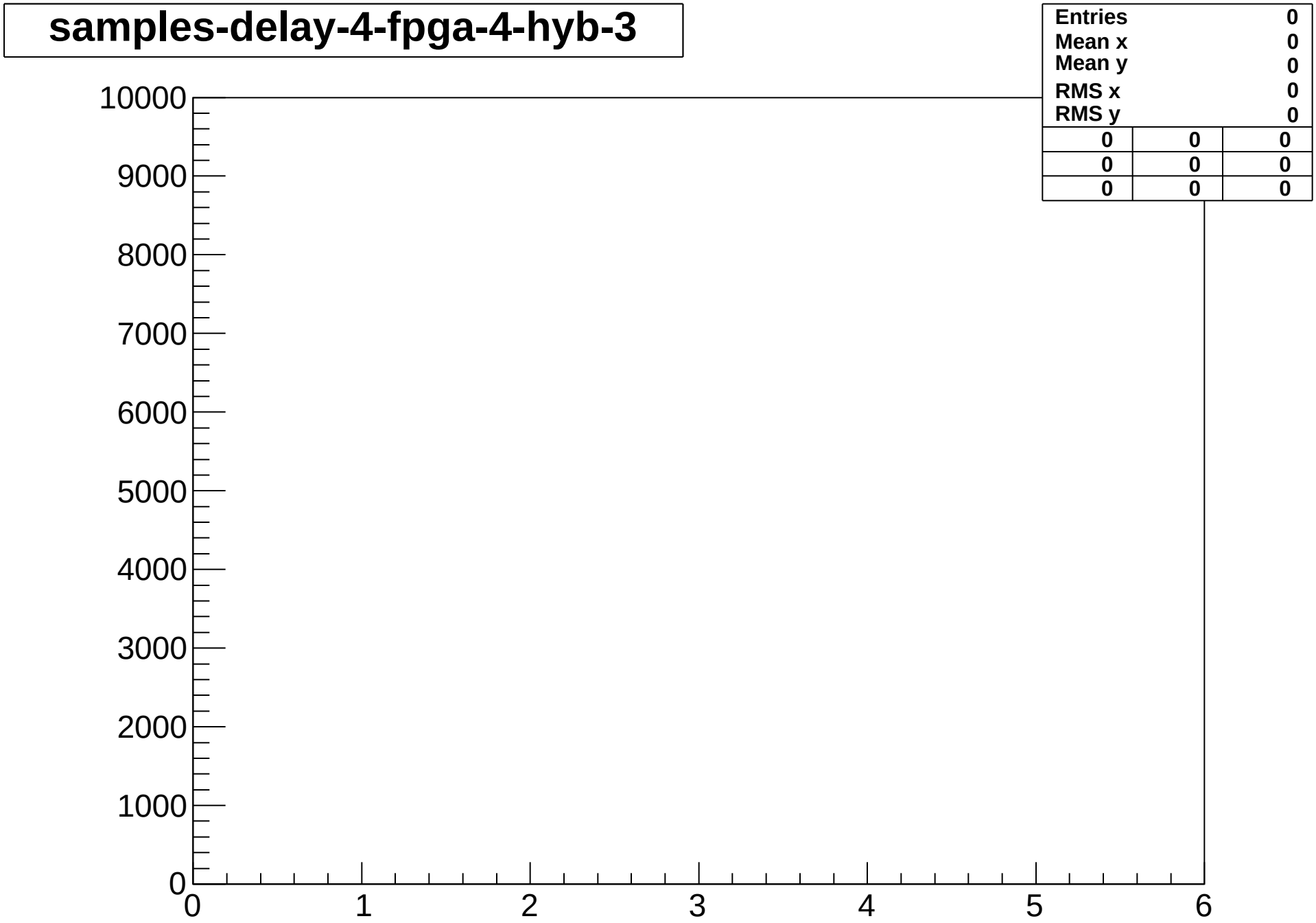
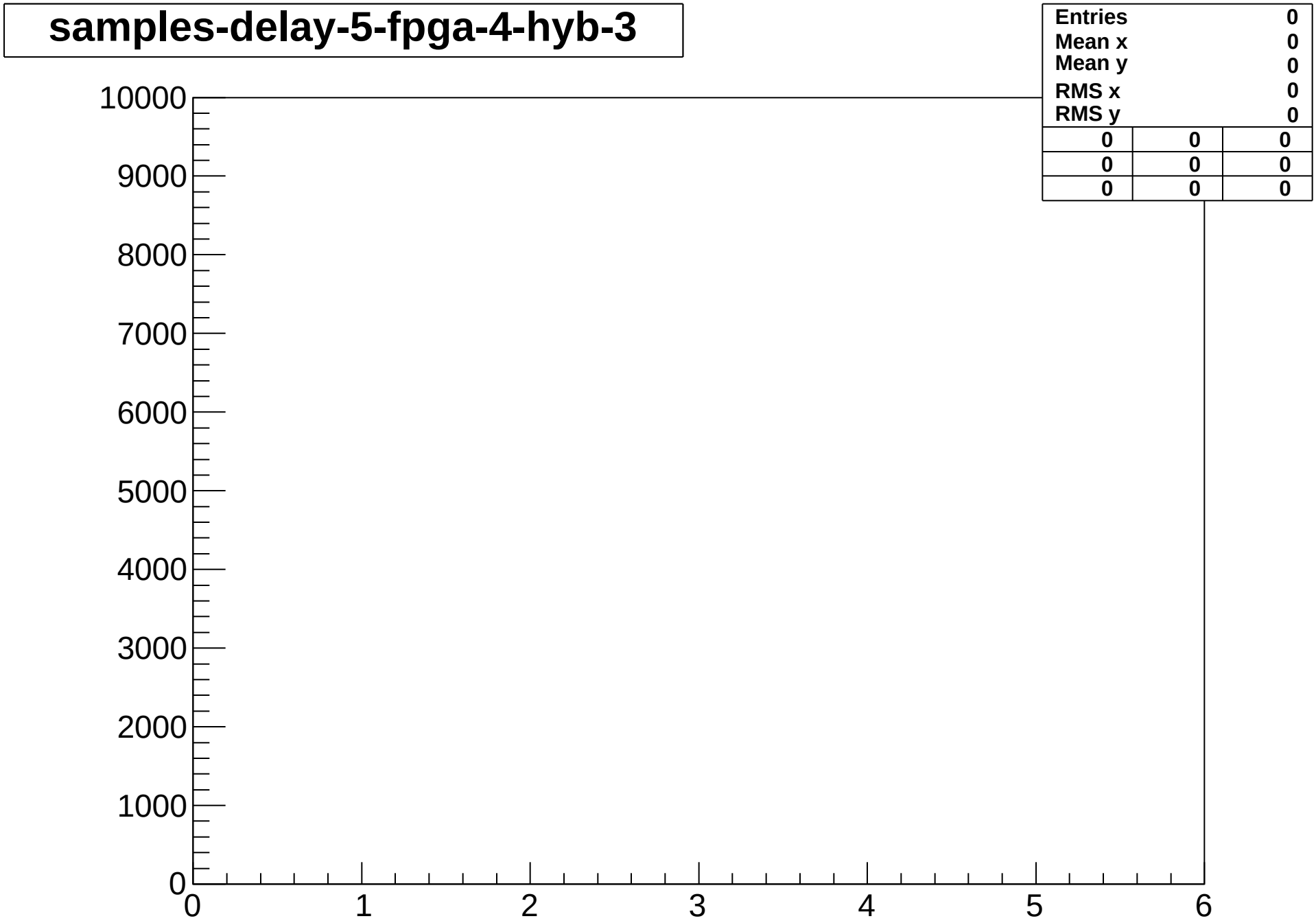
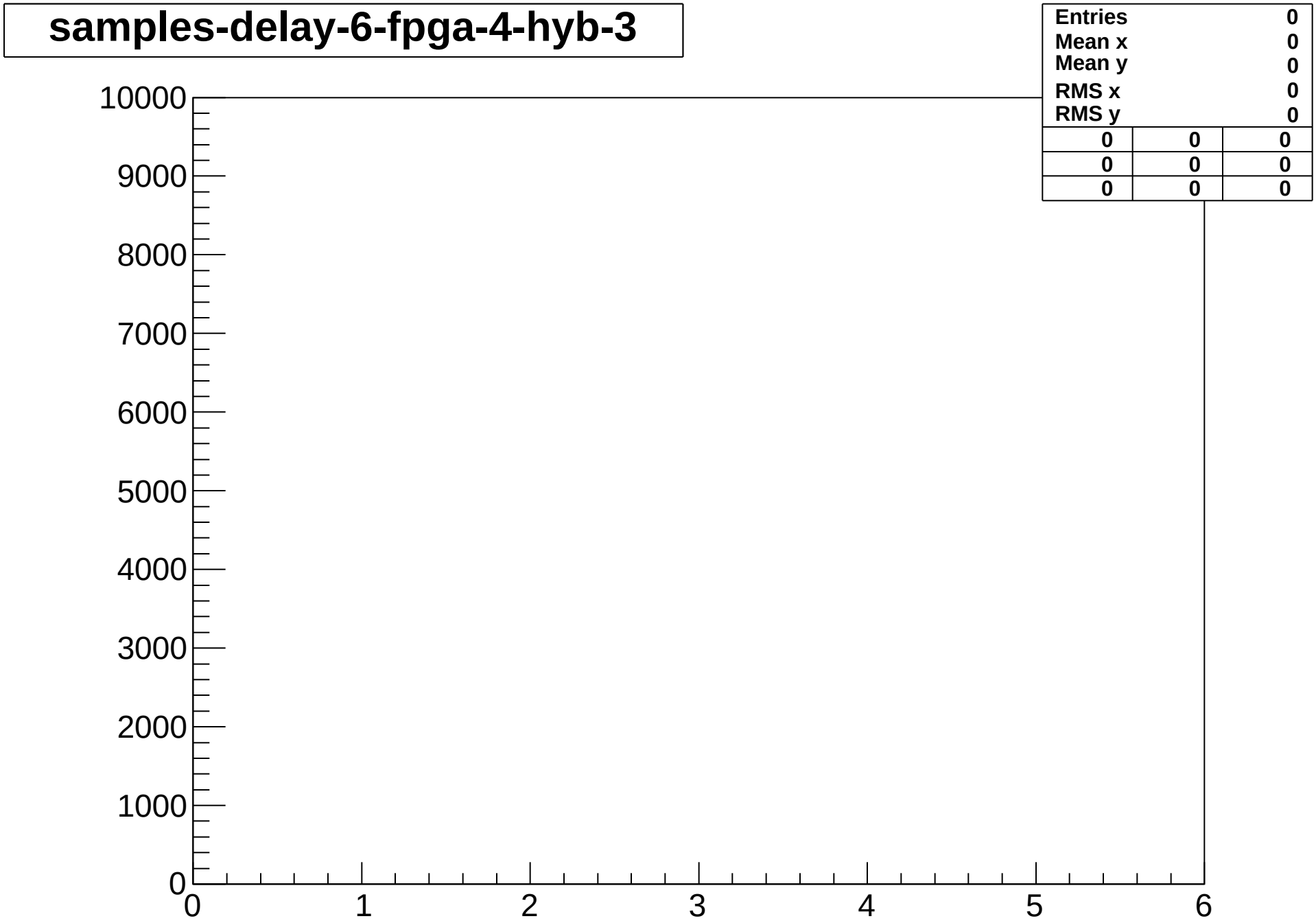
samples-delay-4-fpga-4-hyb-3



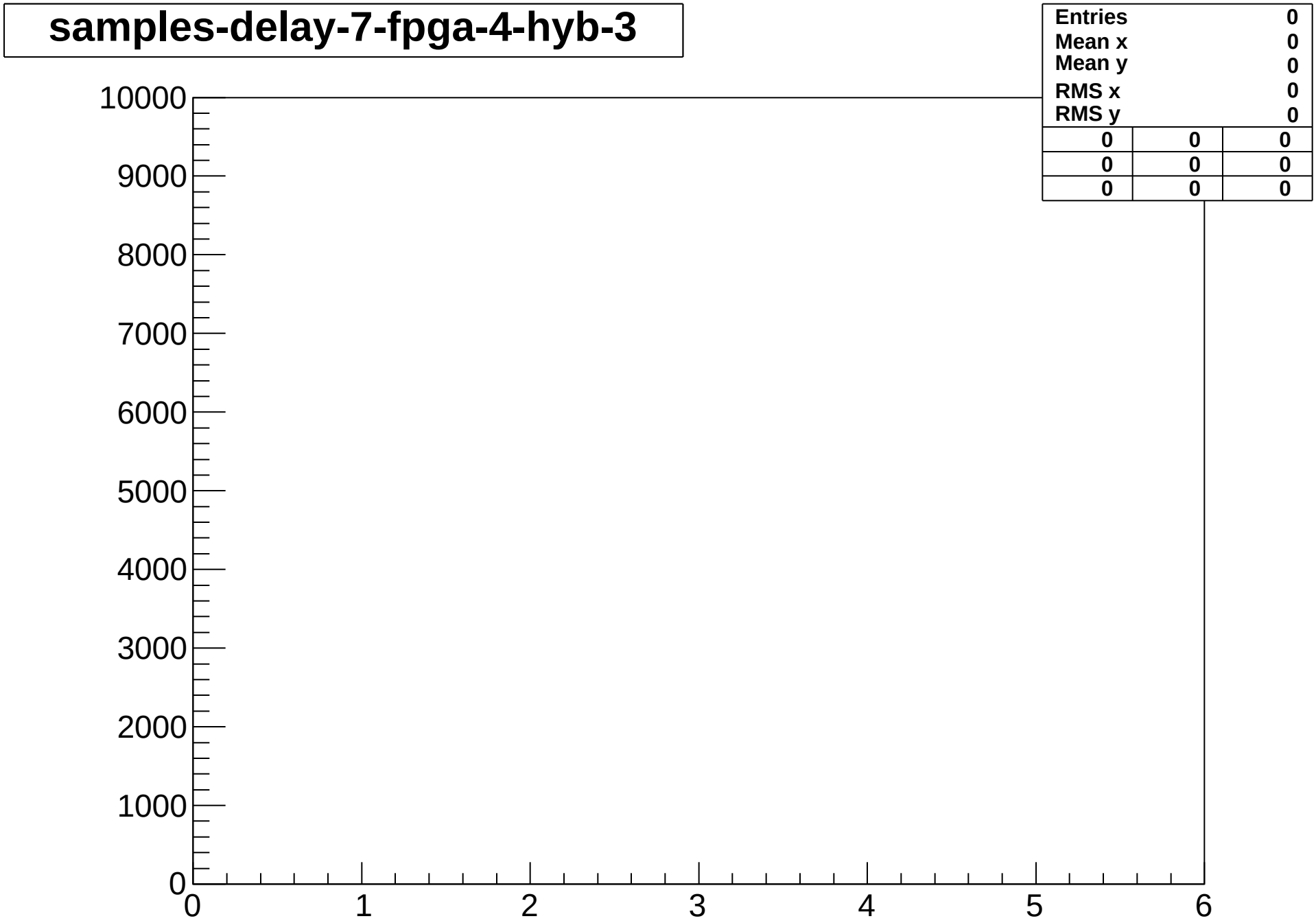
samples-delay-5-fpga-4-hyb-3

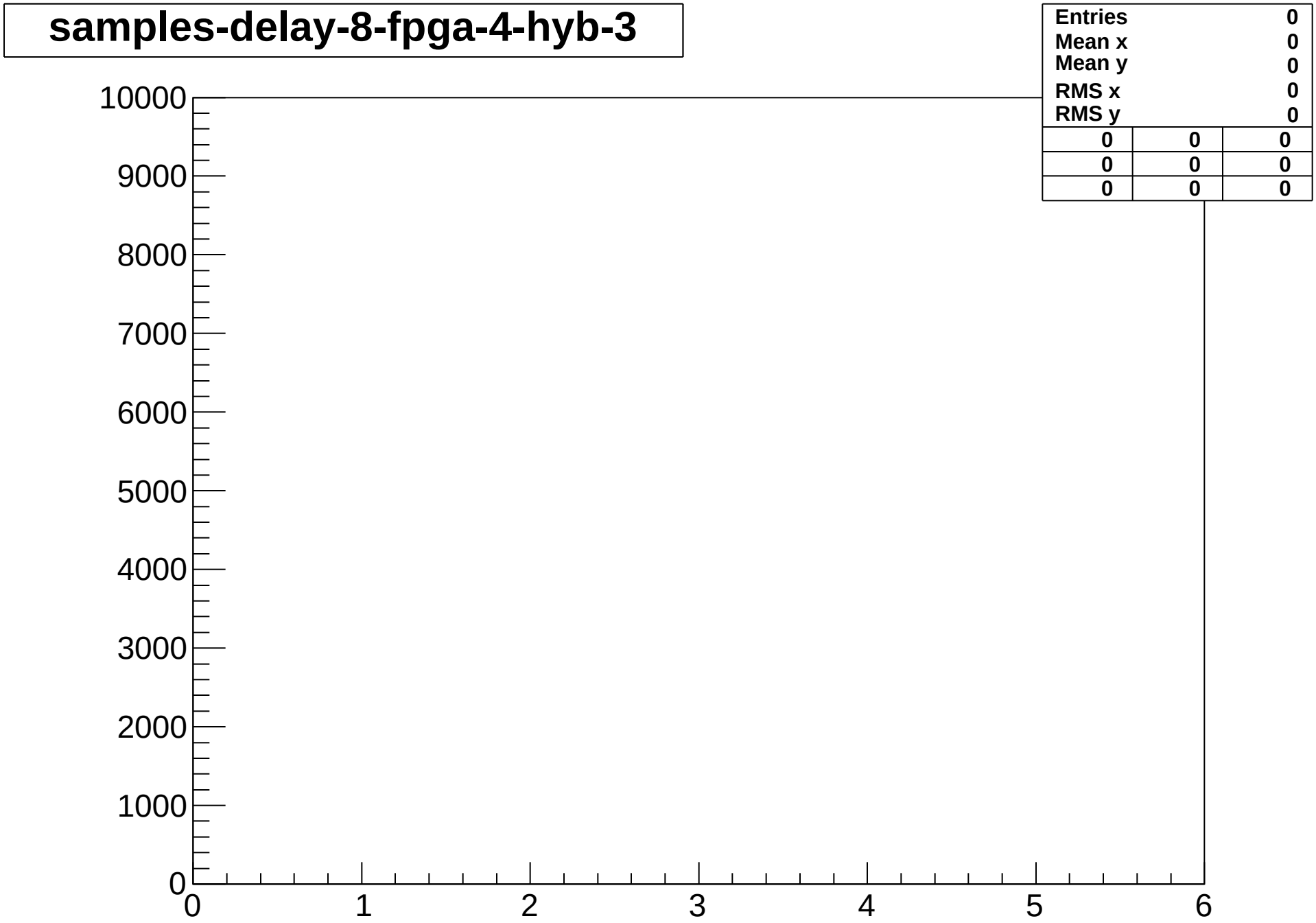


samples-delay-6-fpga-4-hyb-3



samples-delay-7-fpga-4-hyb-3




samples-delay-8-fpga-4-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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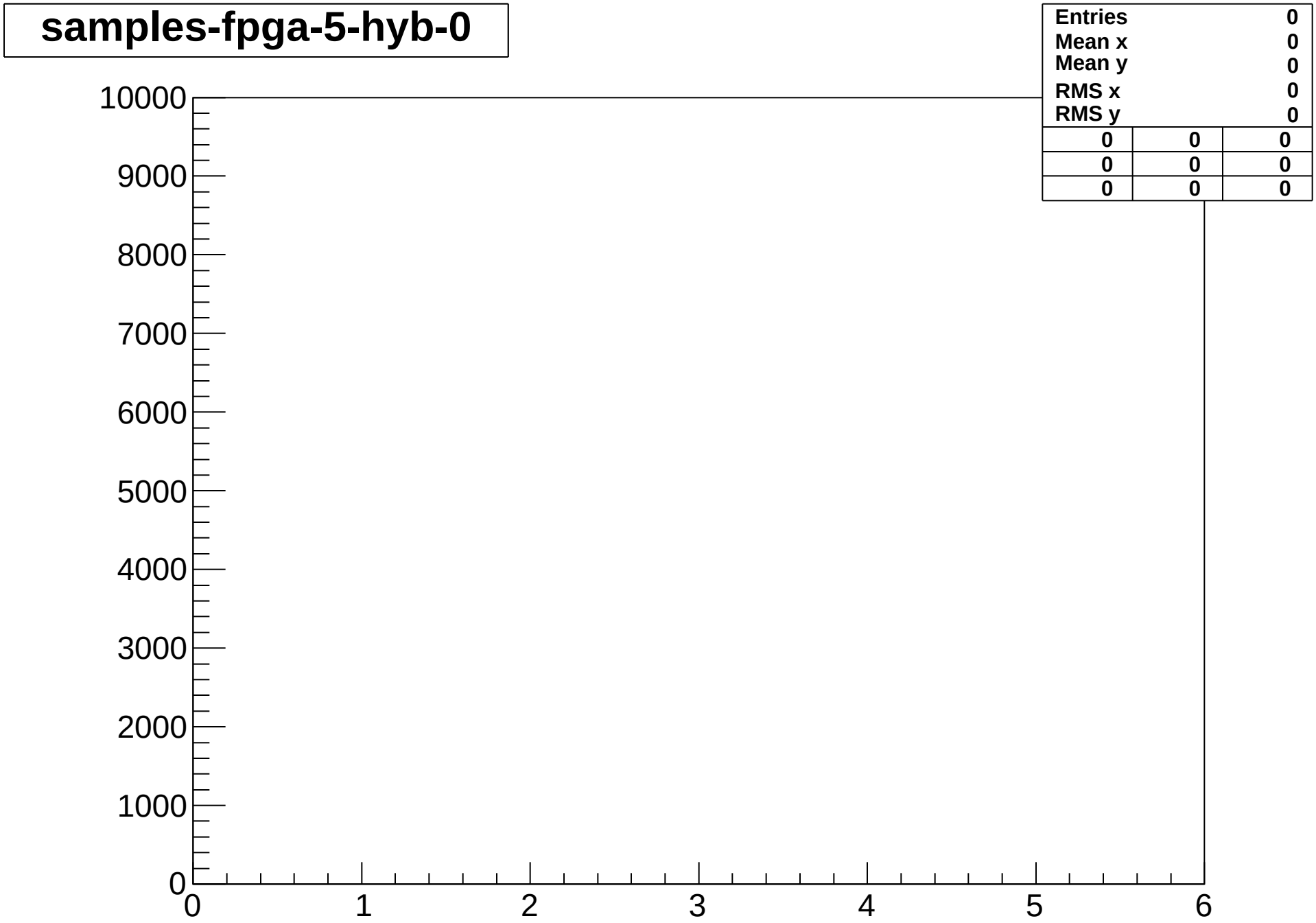
samples-fpga-5-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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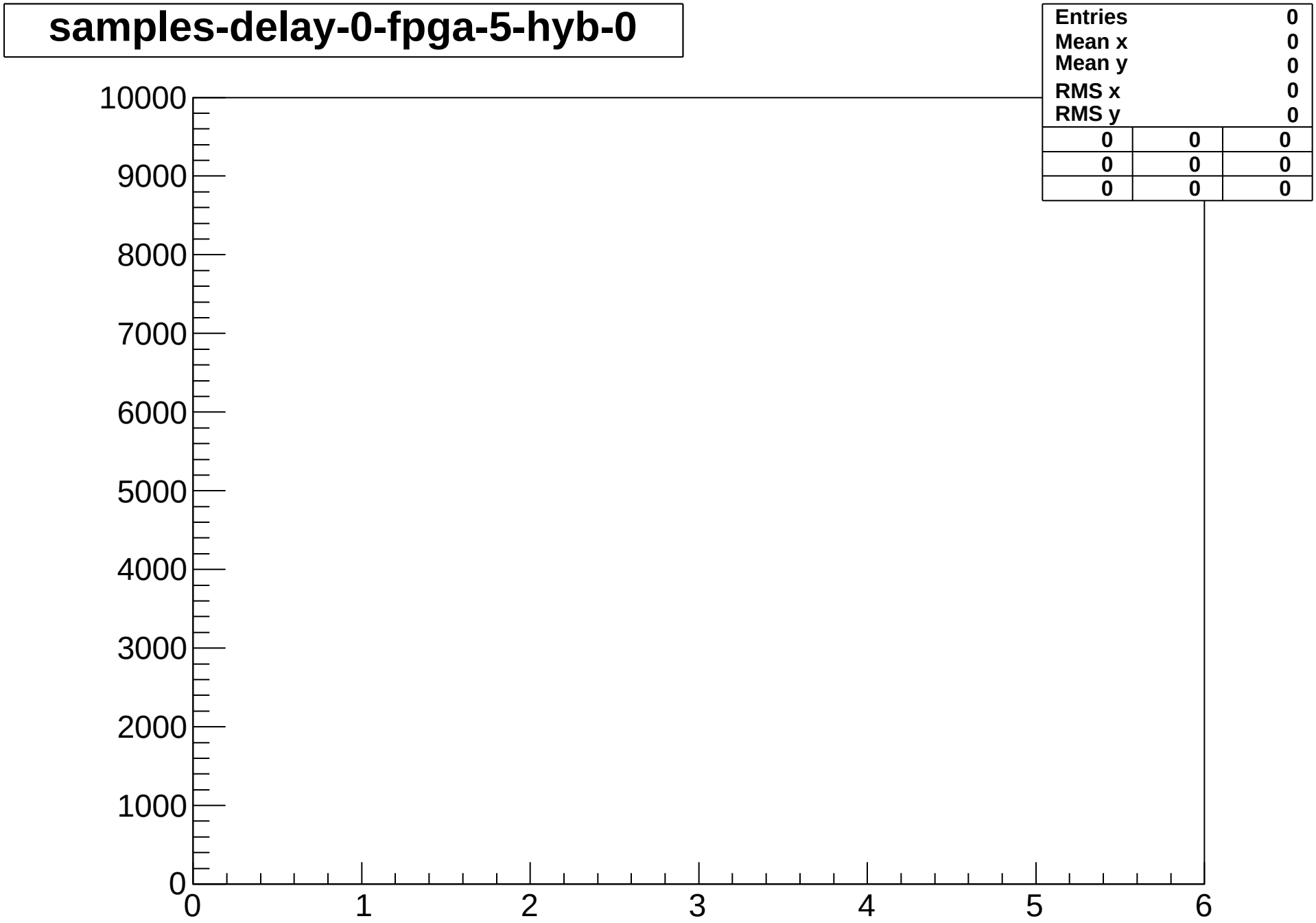
samples-delay-0-fpga-5-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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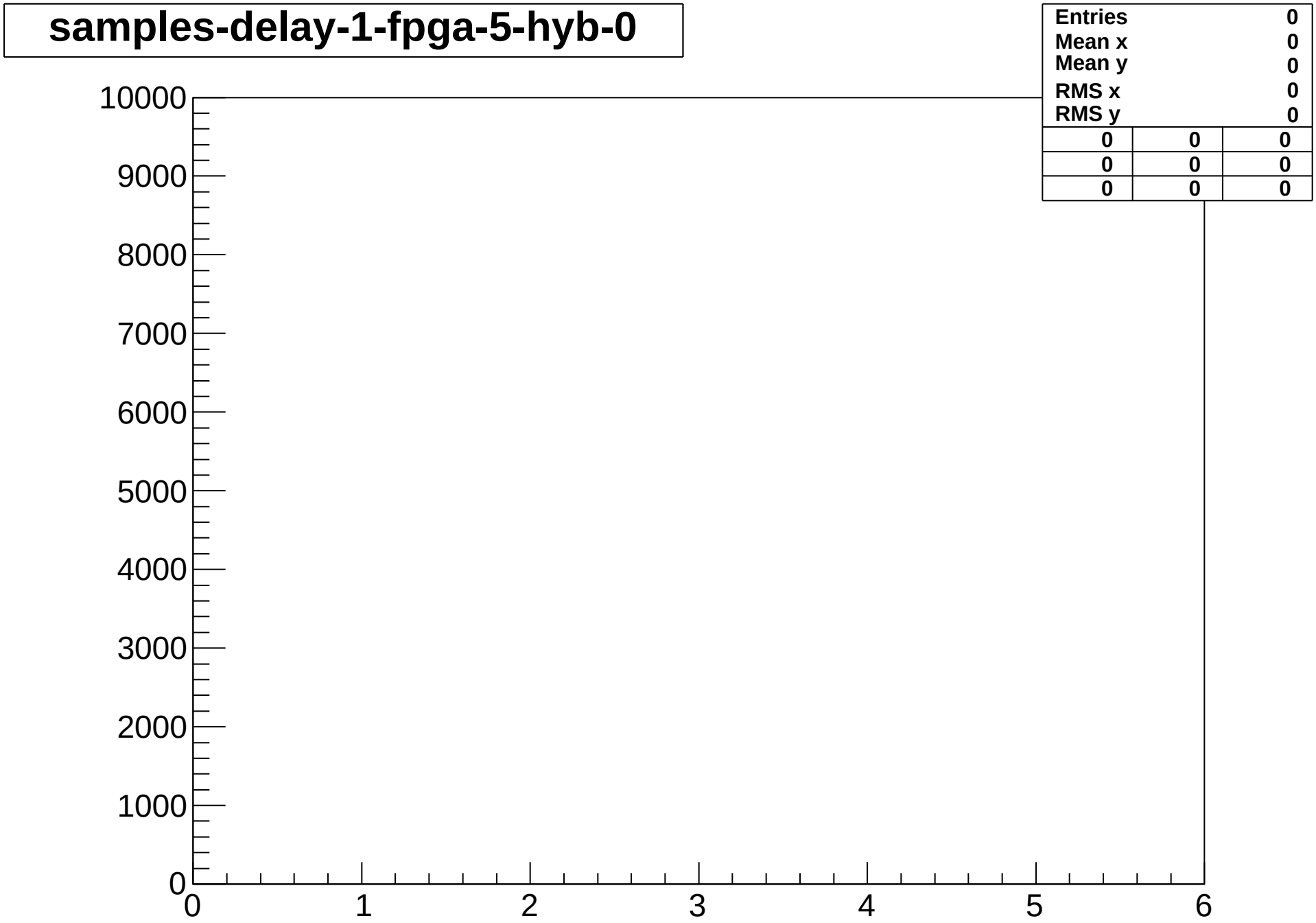
samples-delay-1-fpga-5-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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5000
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3000
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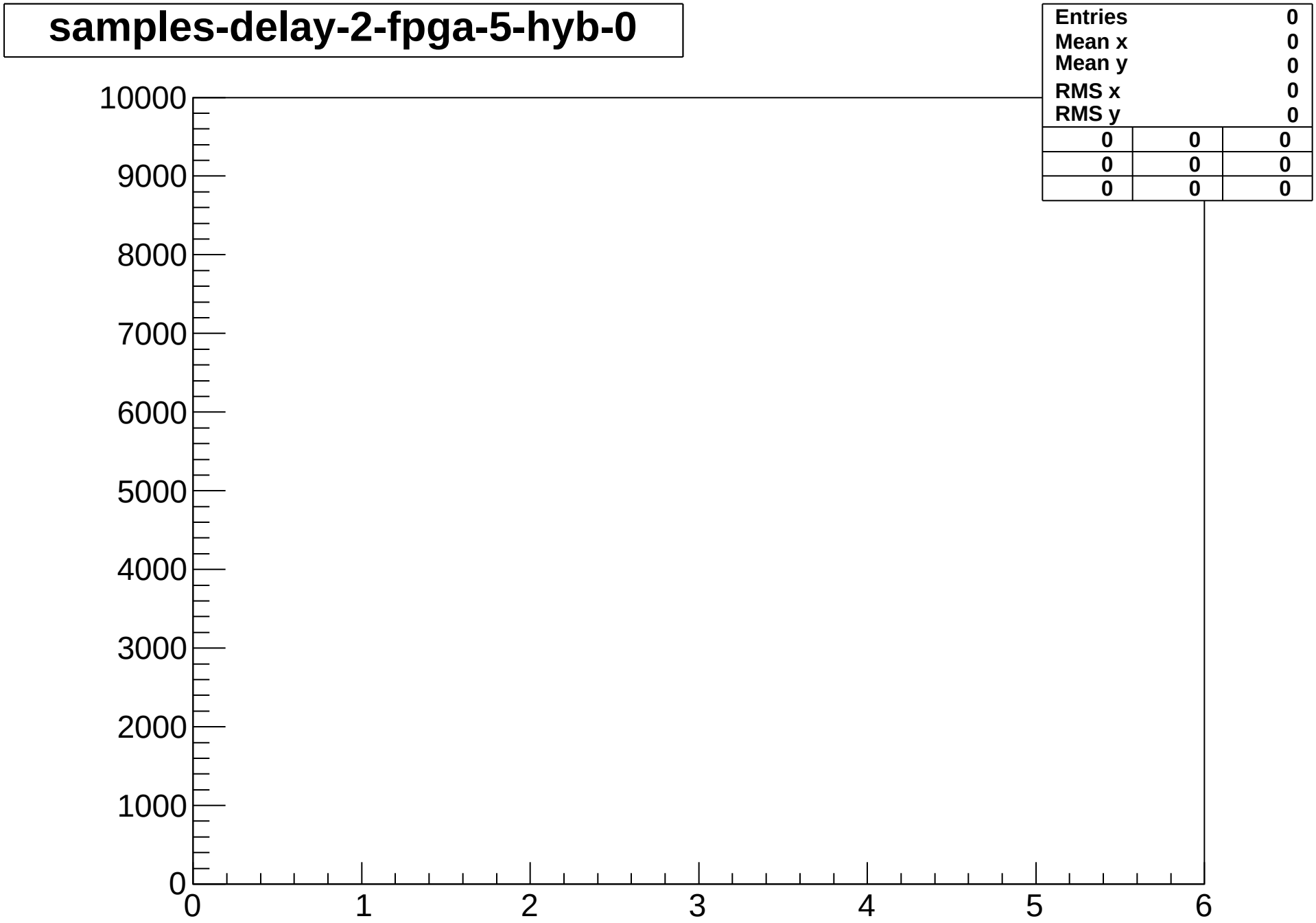
samples-delay-2-fpga-5-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
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3000
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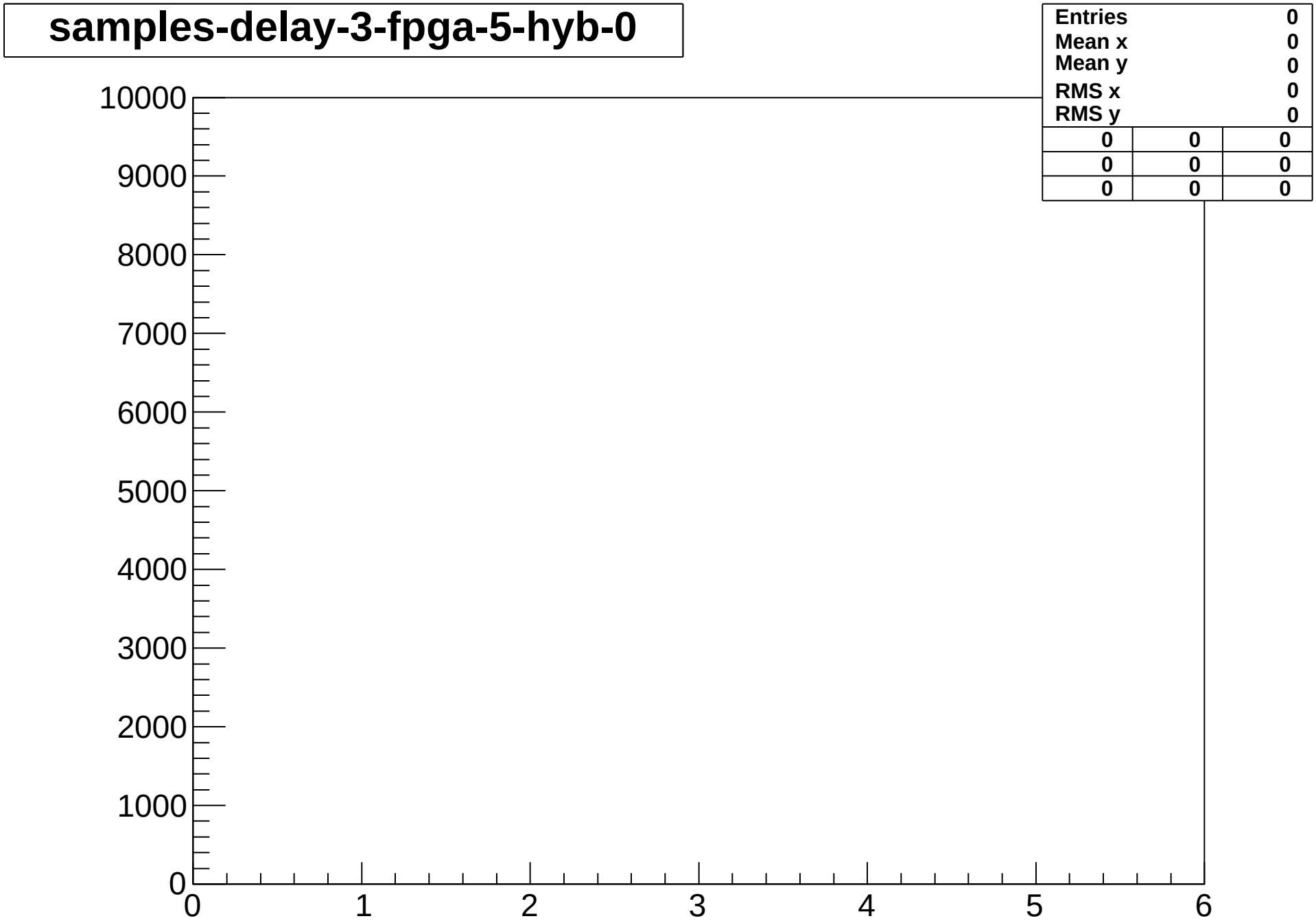
samples-delay-3-fpga-5-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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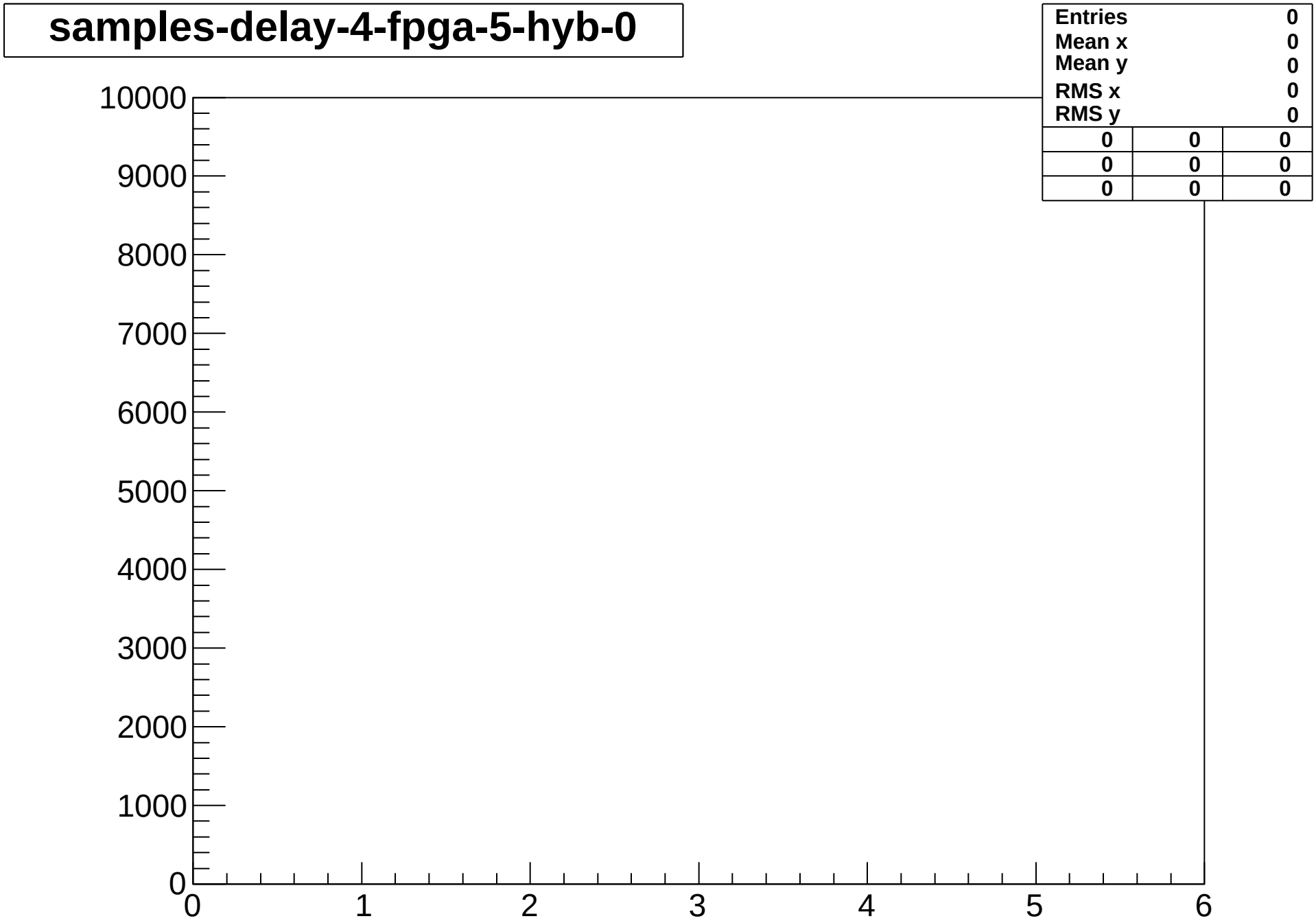
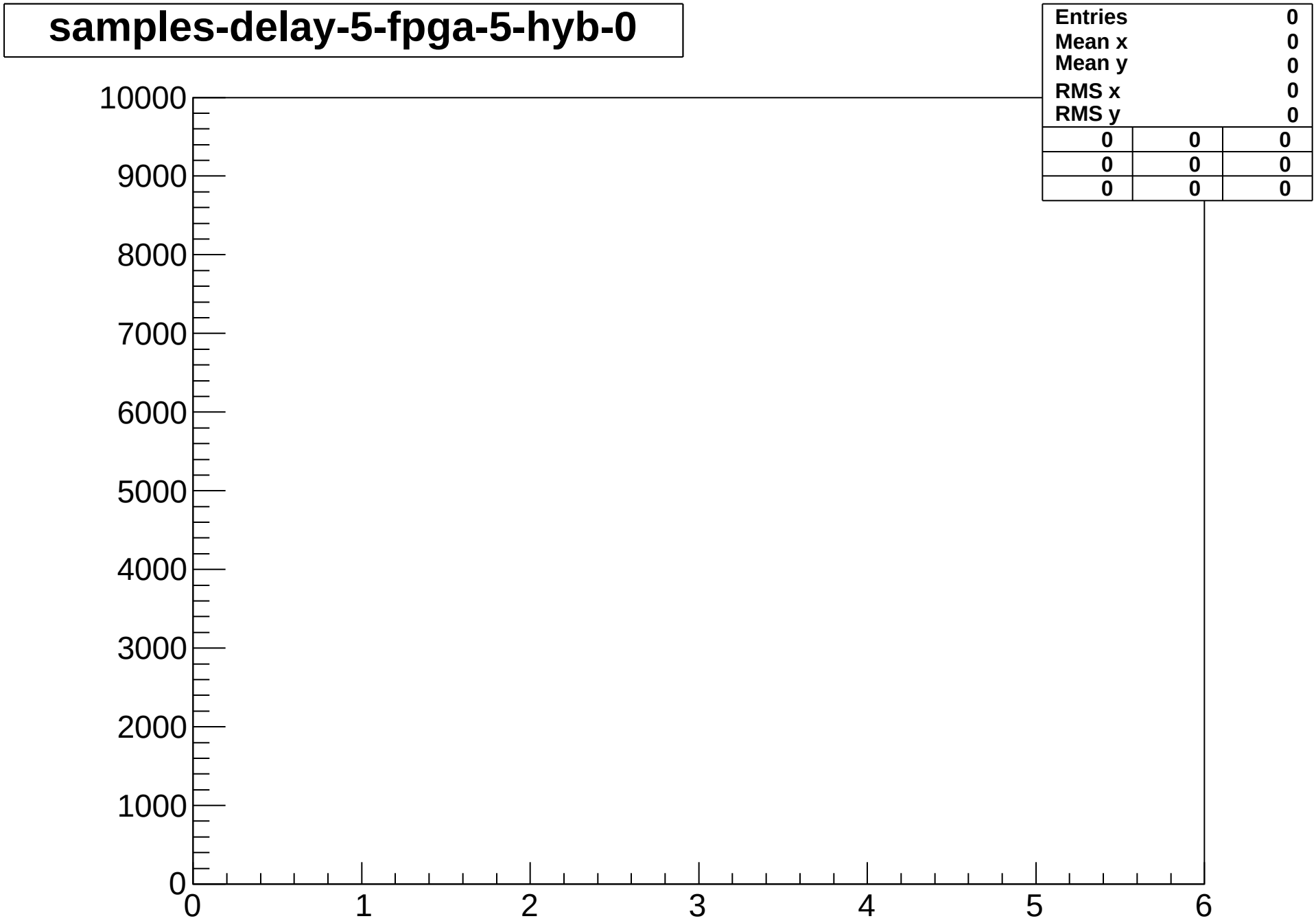
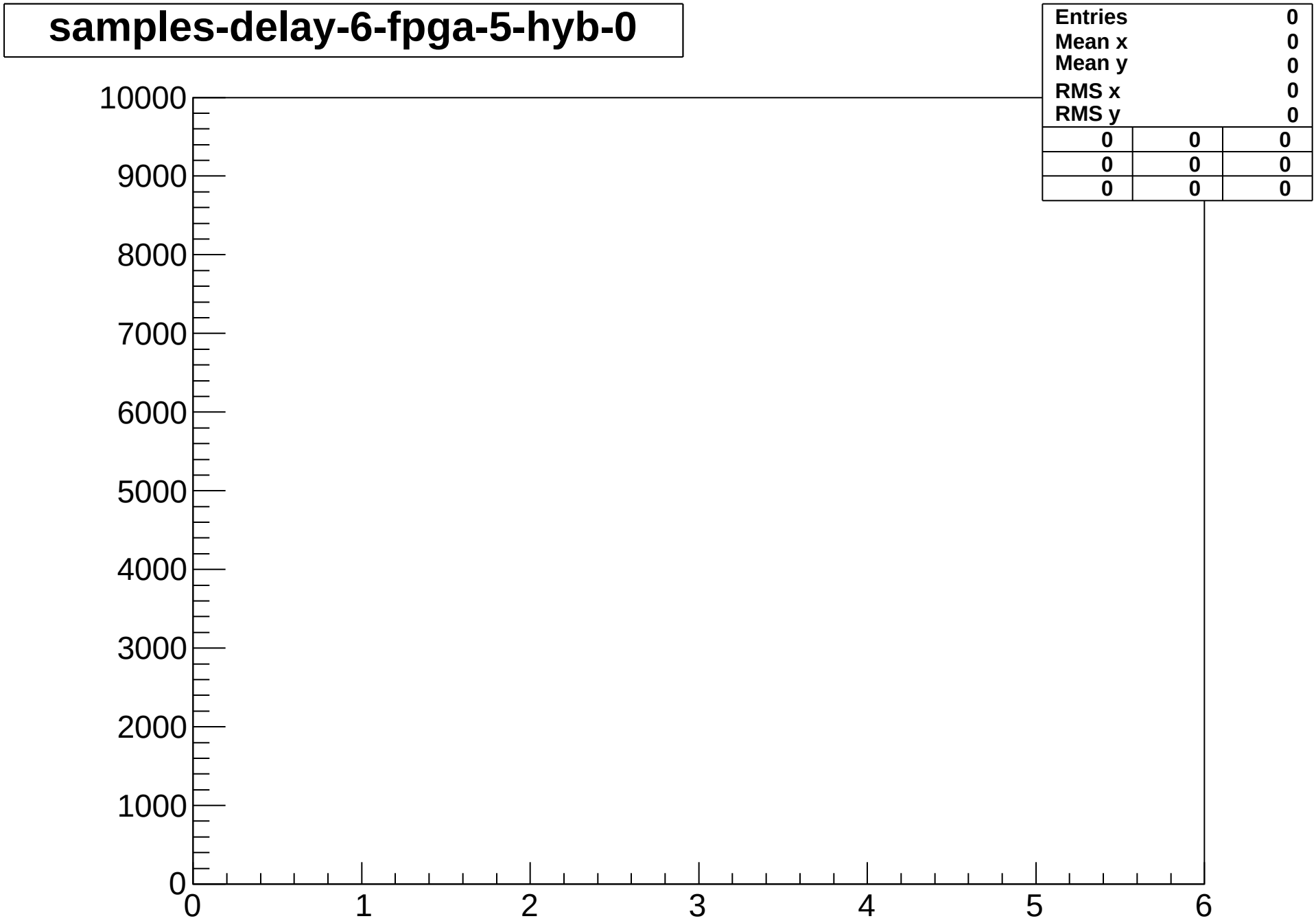
samples-delay-4-fpga-5-hyb-0



samples-delay-5-fpga-5-hyb-0




samples-delay-6-fpga-5-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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3000
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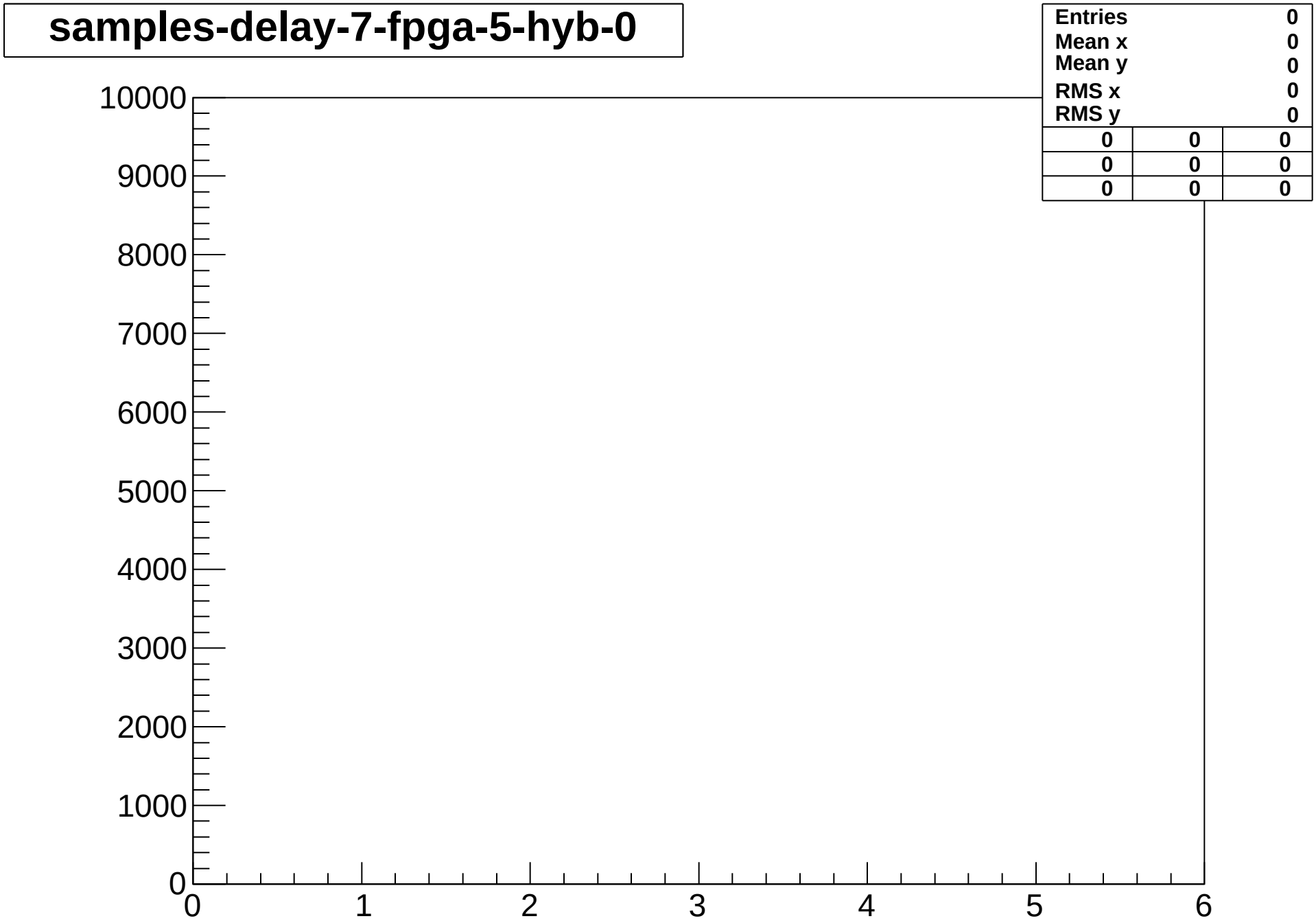
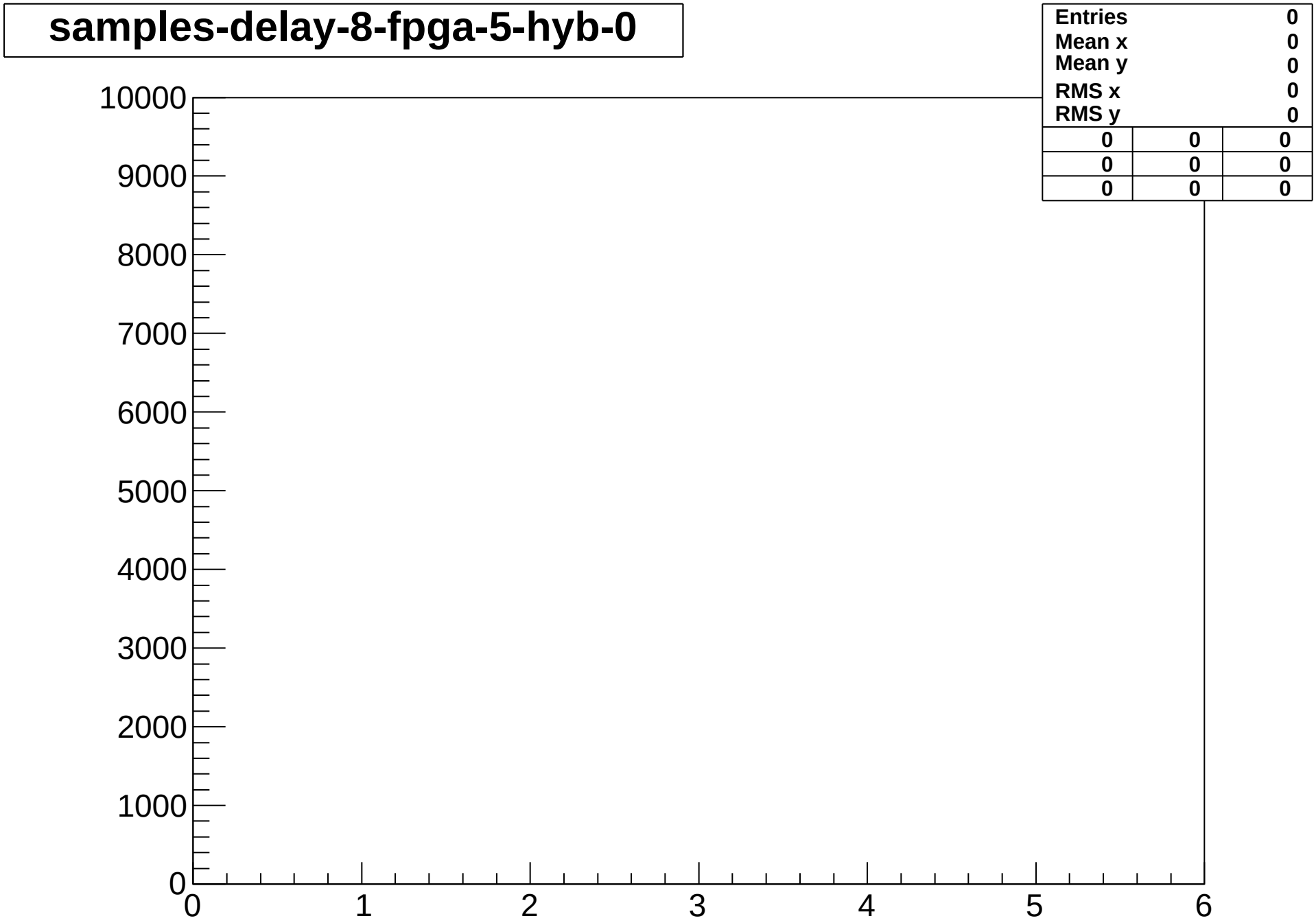
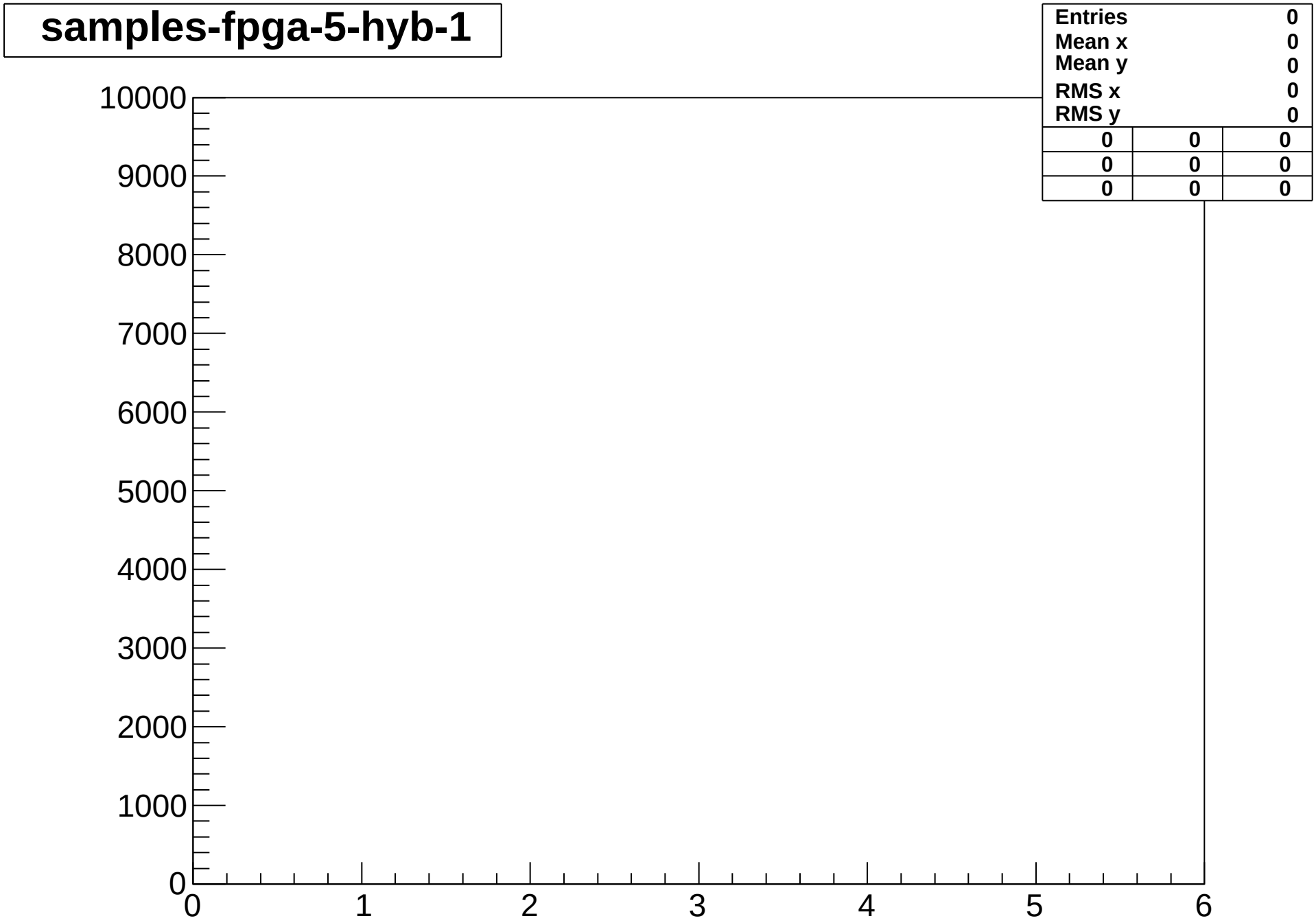
samples-delay-7-fpga-5-hyb-0



samples-delay-8-fpga-5-hyb-0




samples-fpga-5-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
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1
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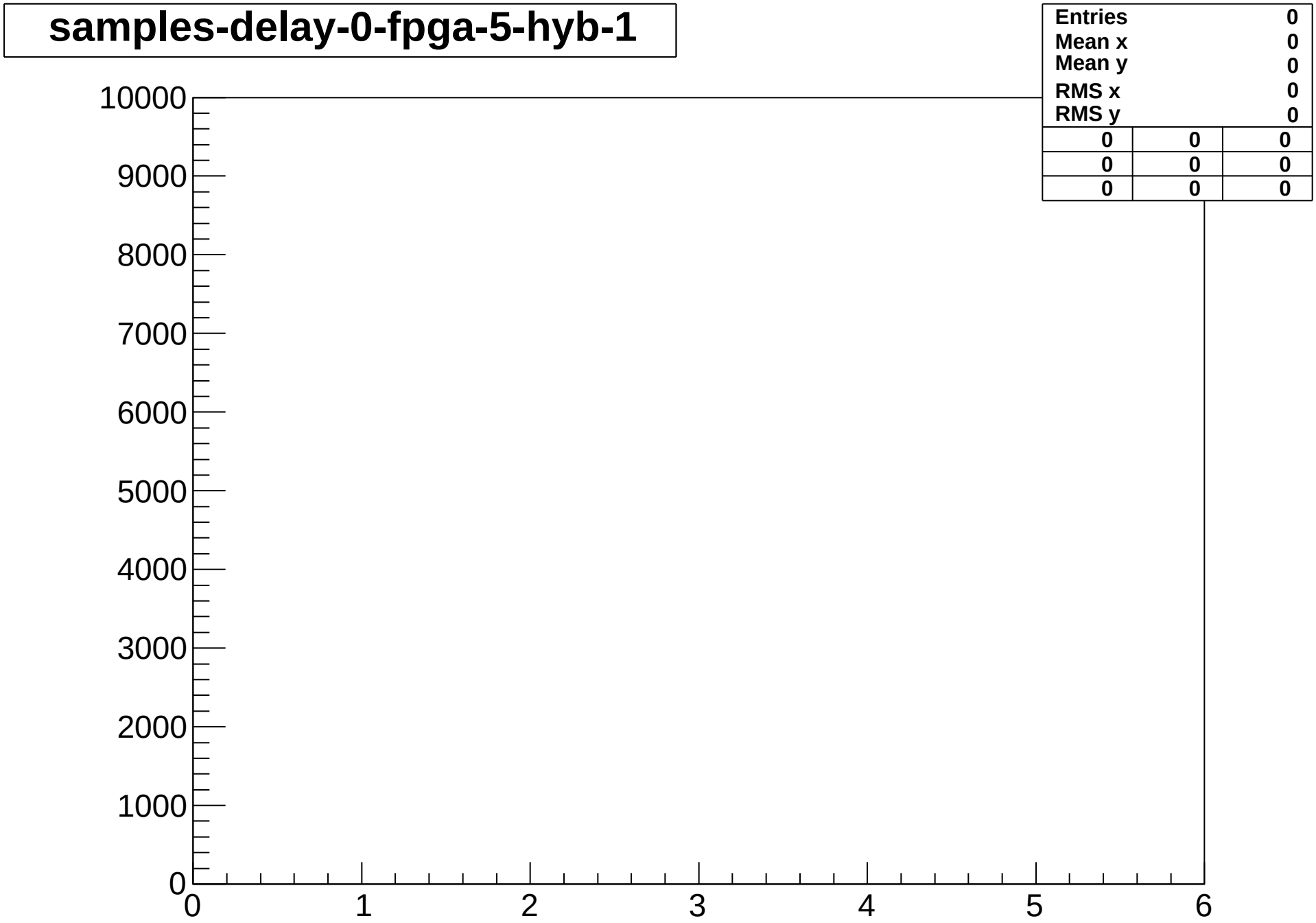
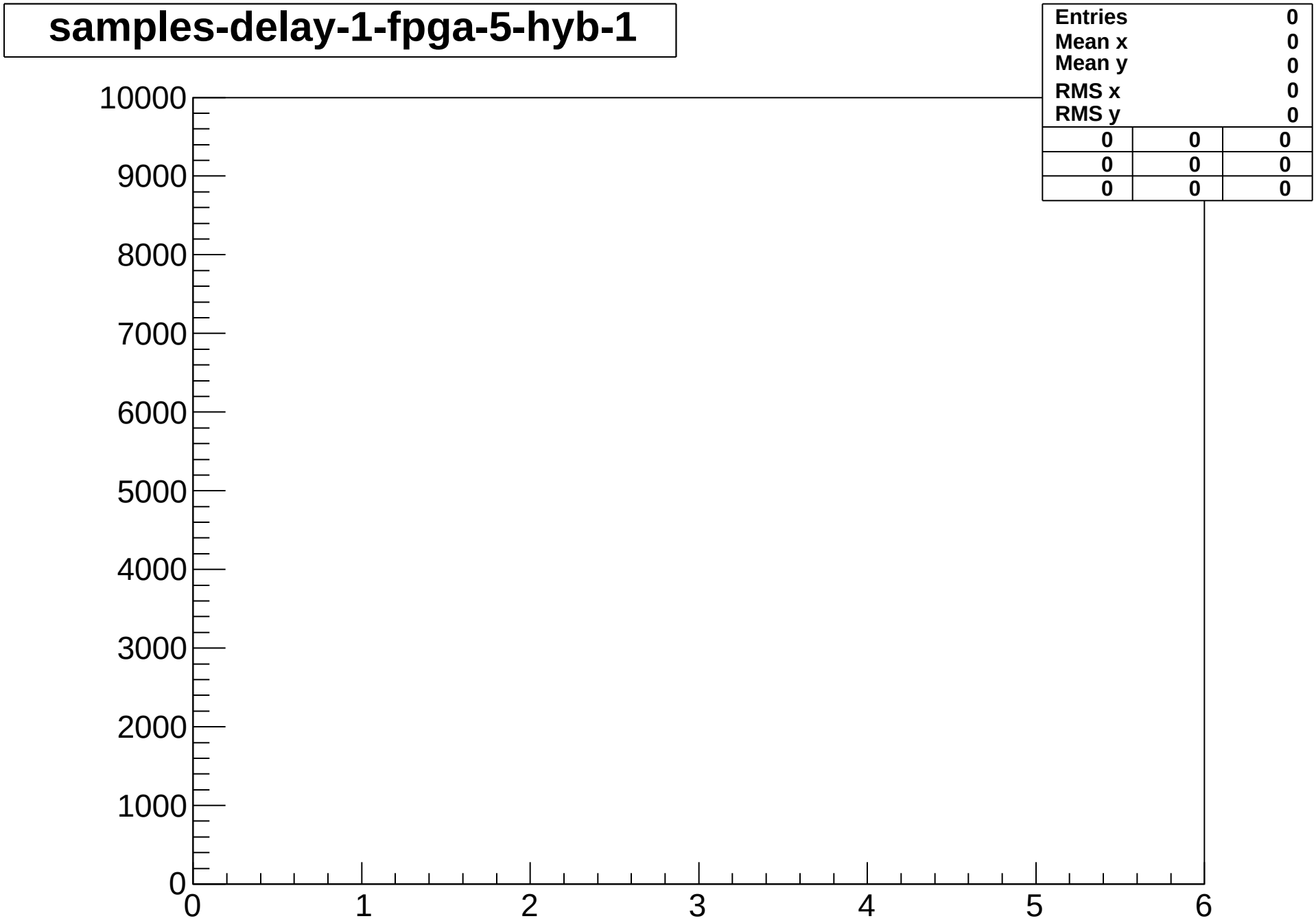
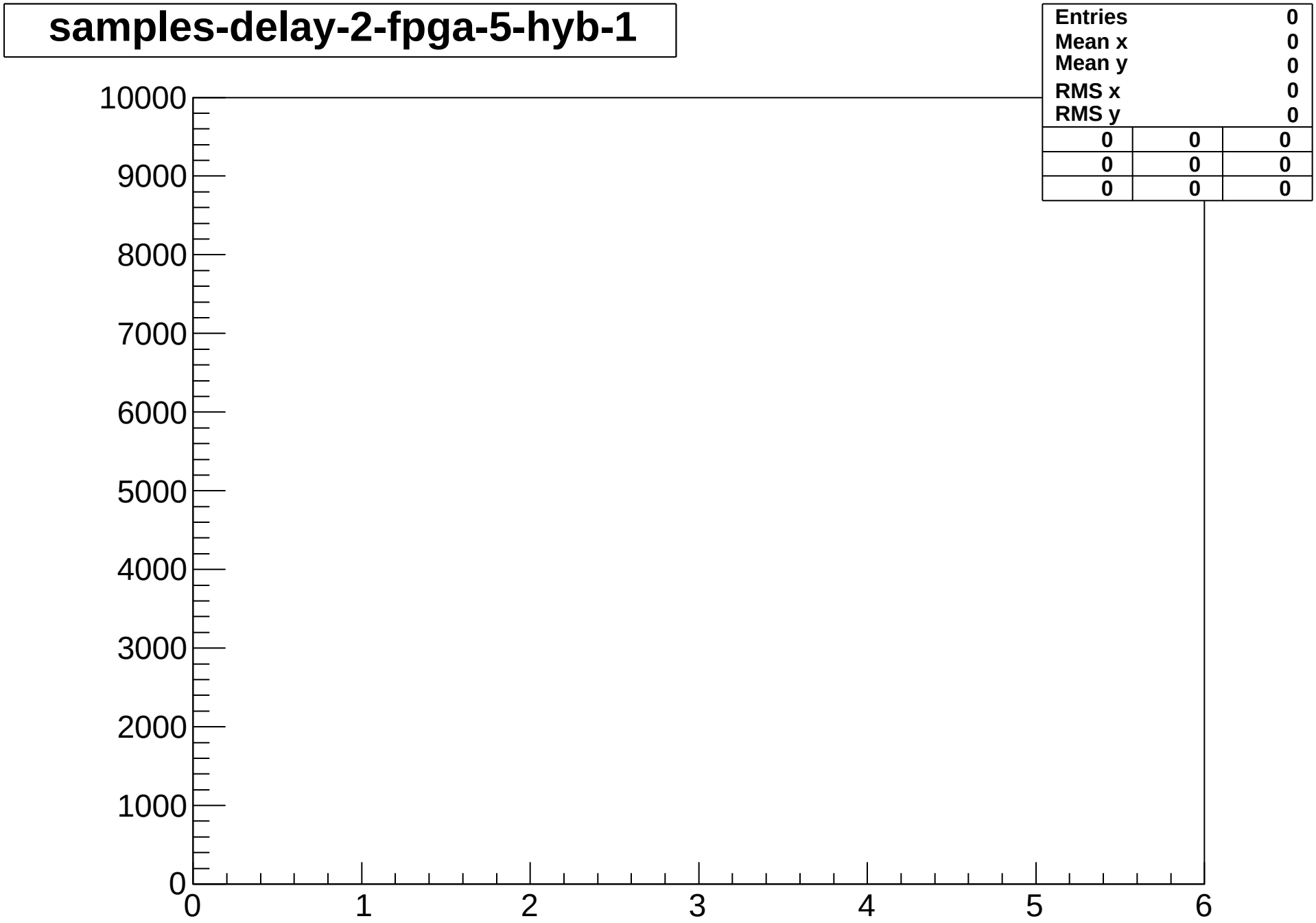
samples-delay-0-fpga-5-hyb-1



samples-delay-1-fpga-5-hyb-1




samples-delay-2-fpga-5-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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6000
5000
4000
3000
2000
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1
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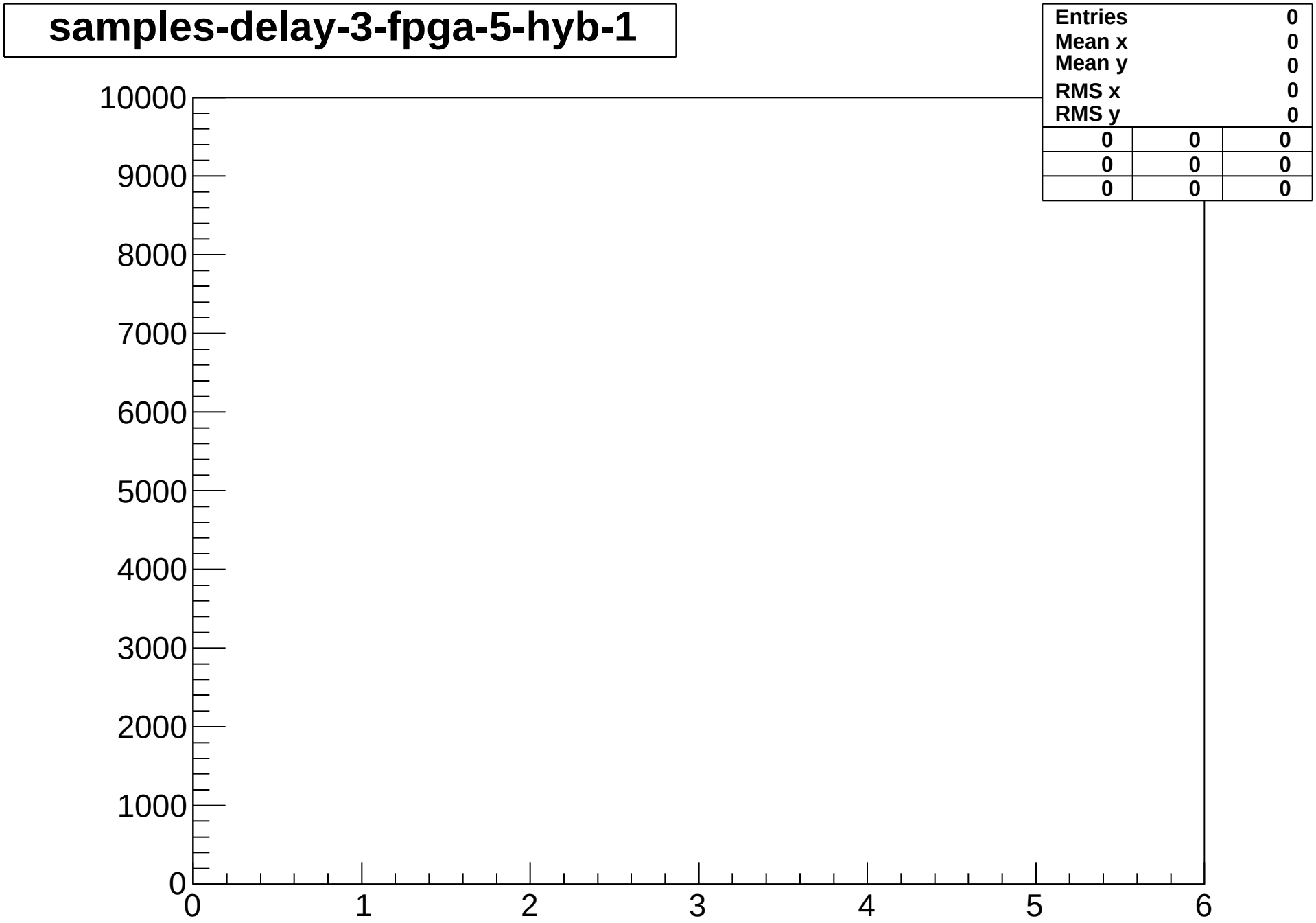
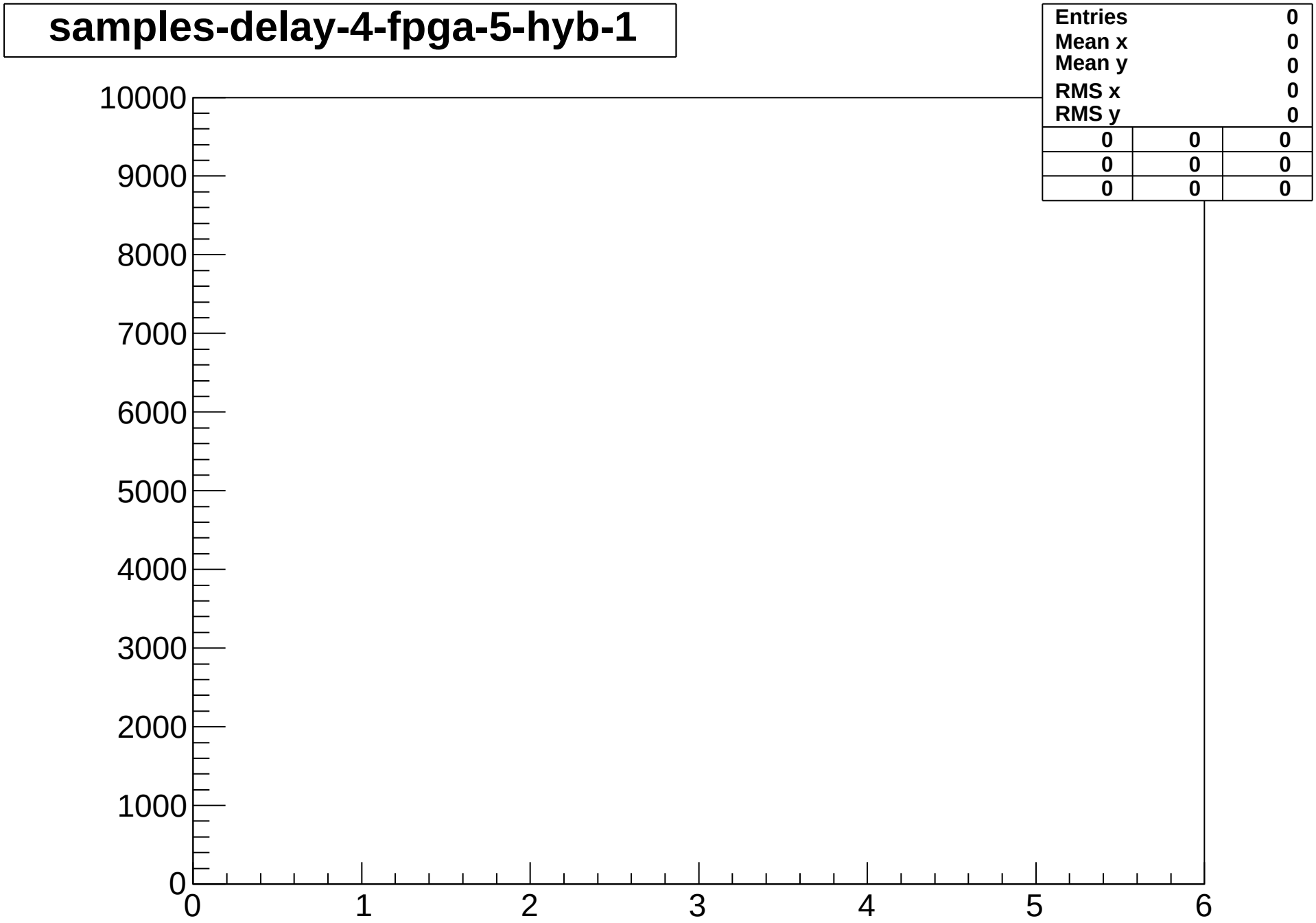
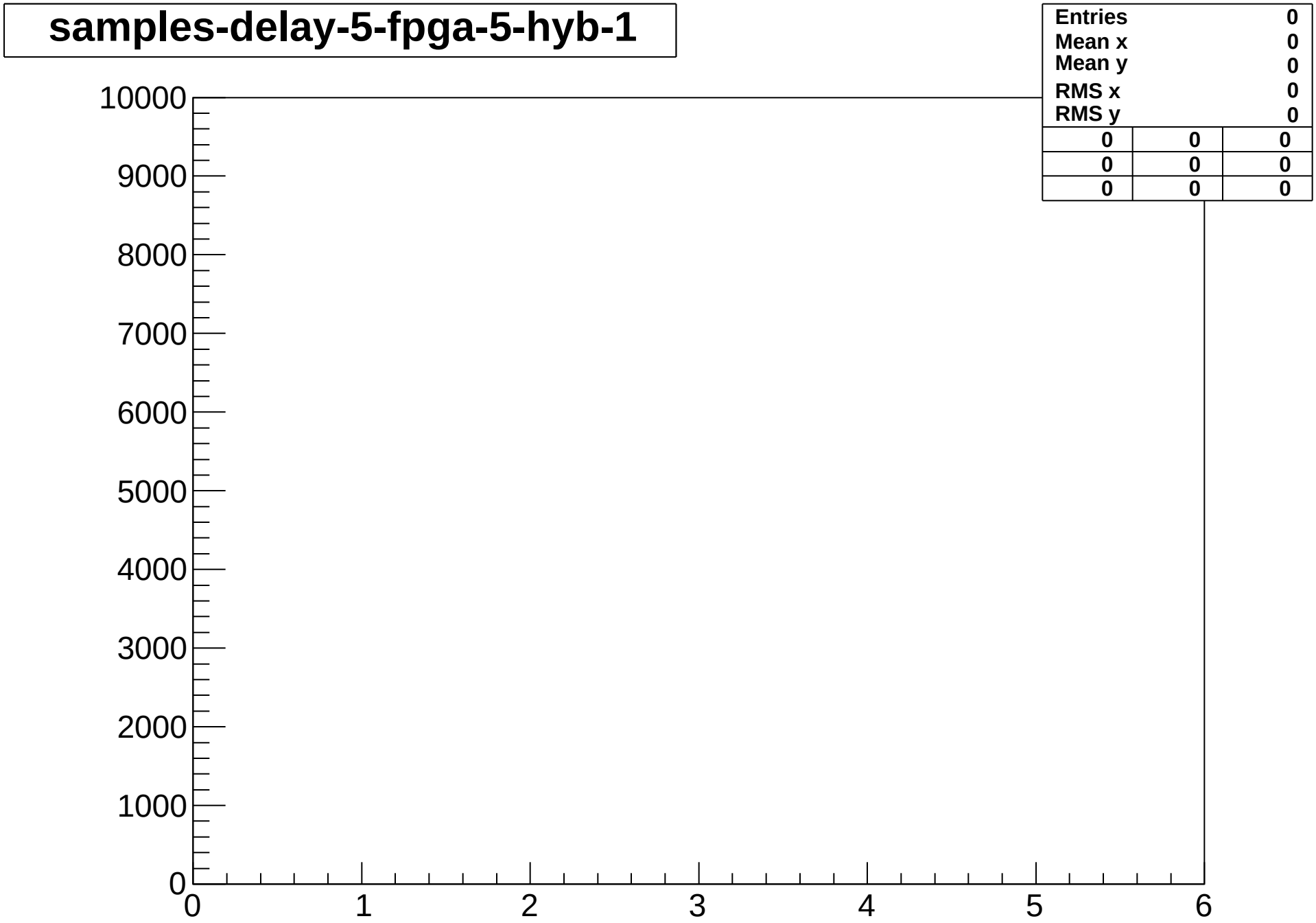
samples-delay-3-fpga-5-hyb-1



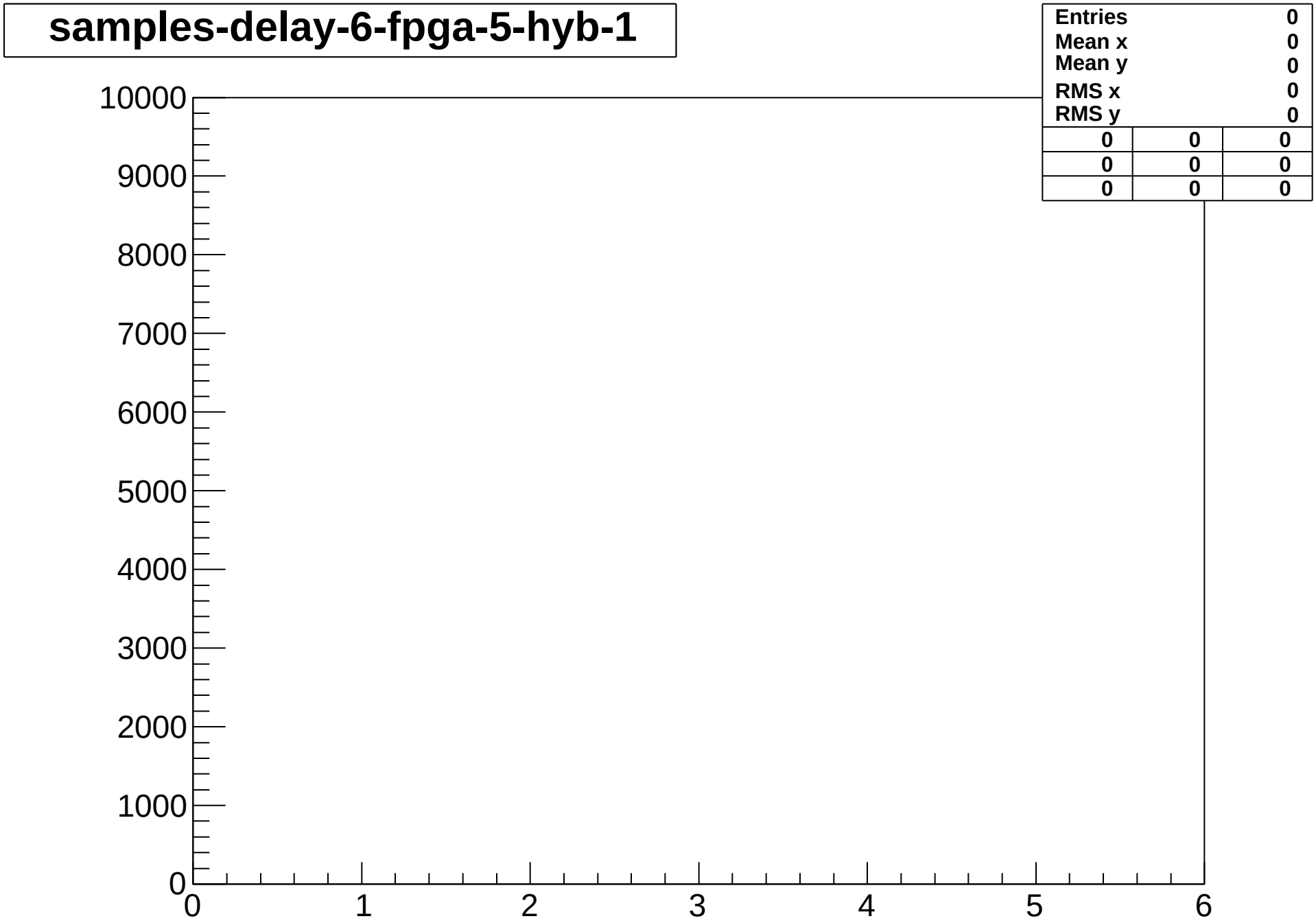
samples-delay-4-fpga-5-hyb-1

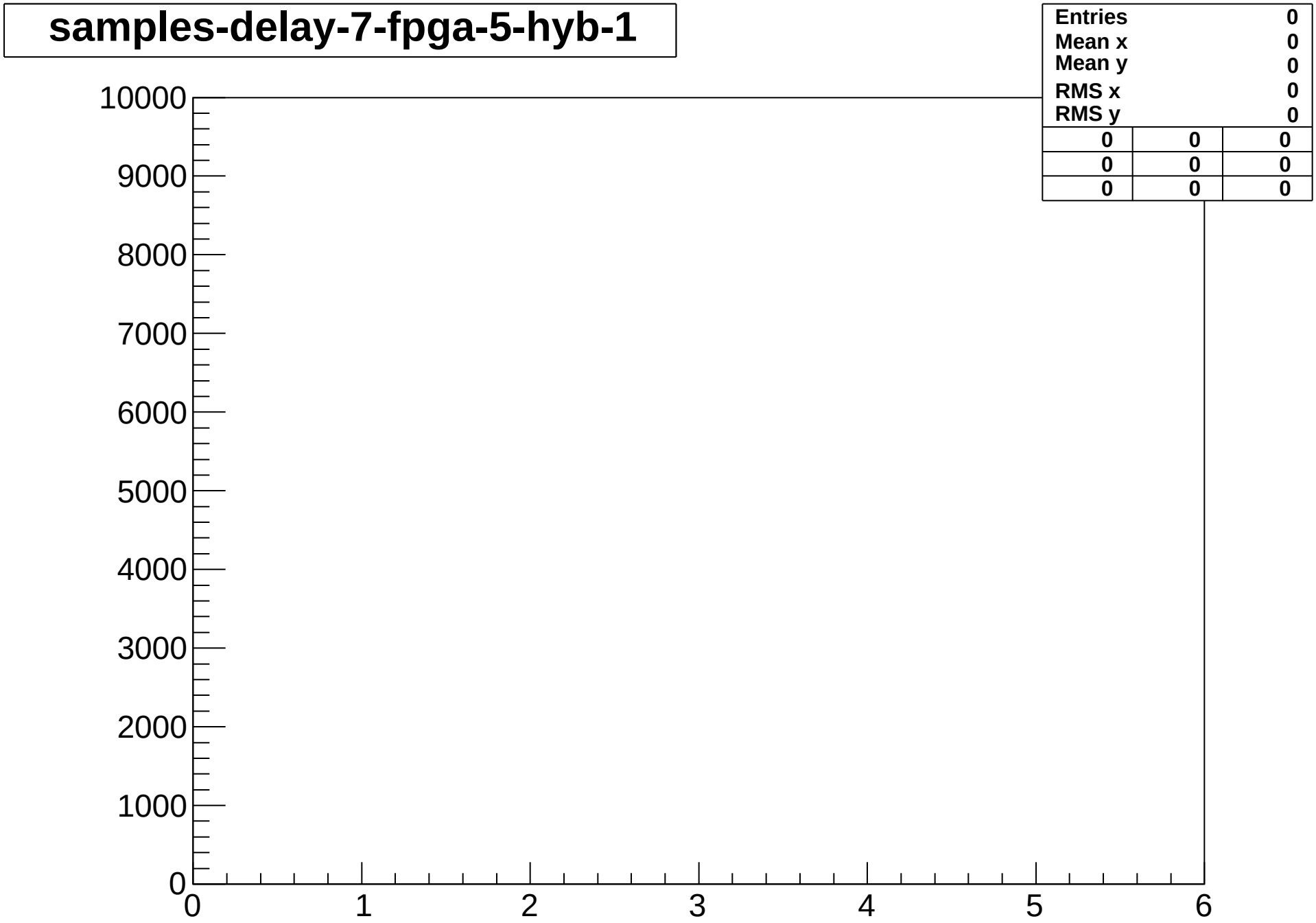


samples-delay-5-fpga-5-hyb-1



samples-delay-6-fpga-5-hyb-1




samples-delay-7-fpga-5-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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6000
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4000
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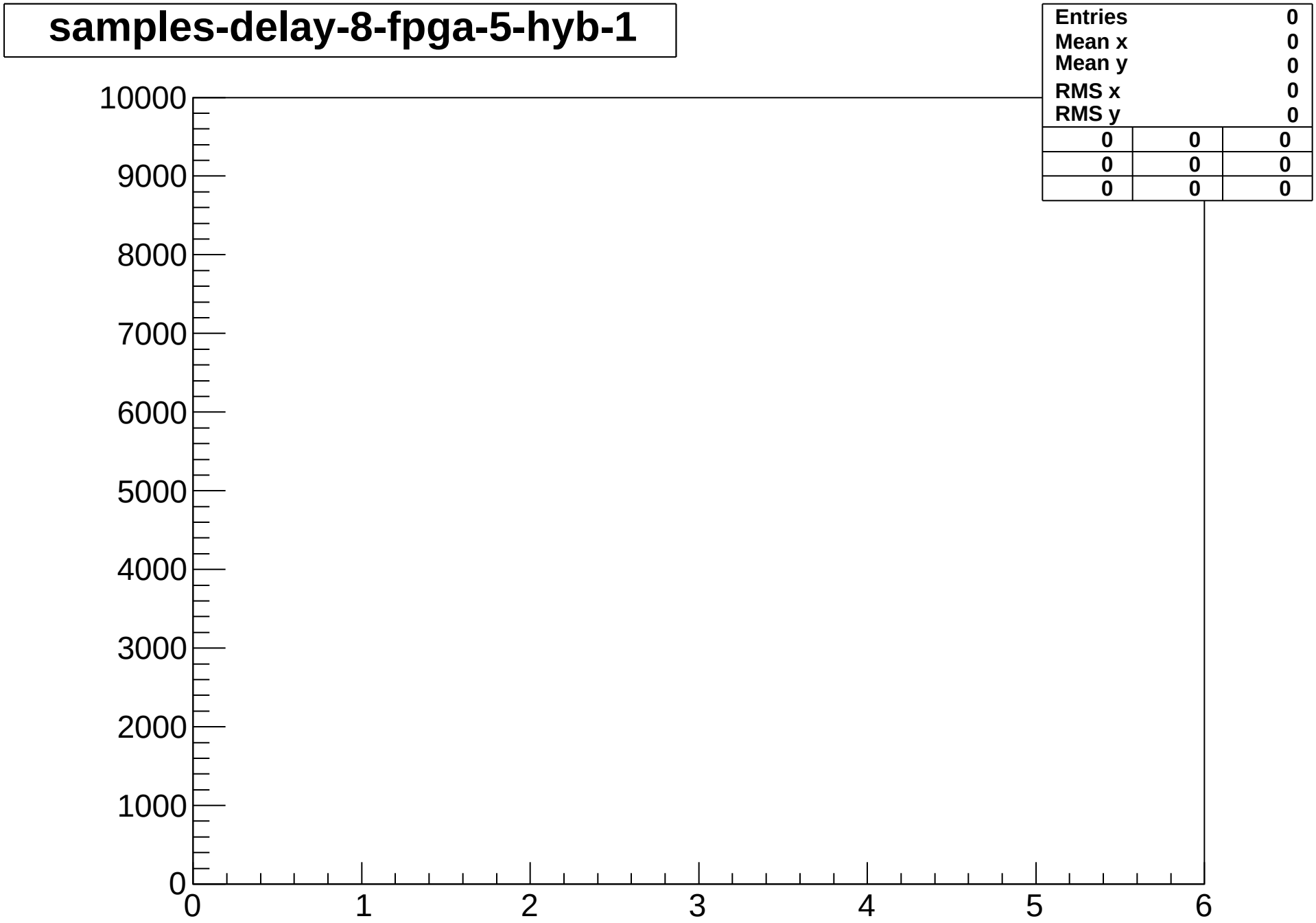
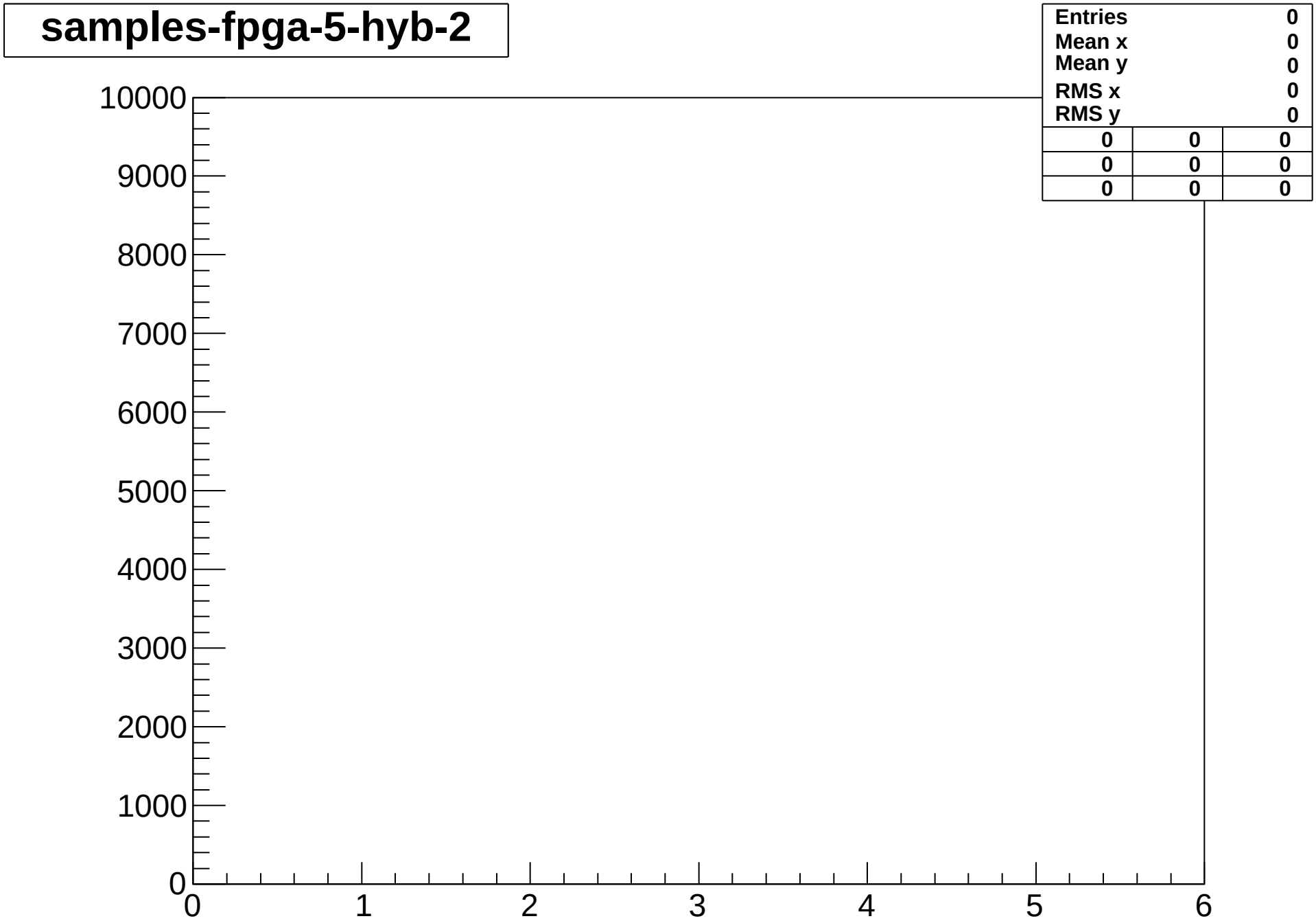
samples-delay-8-fpga-5-hyb-1




samples-fpga-5-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
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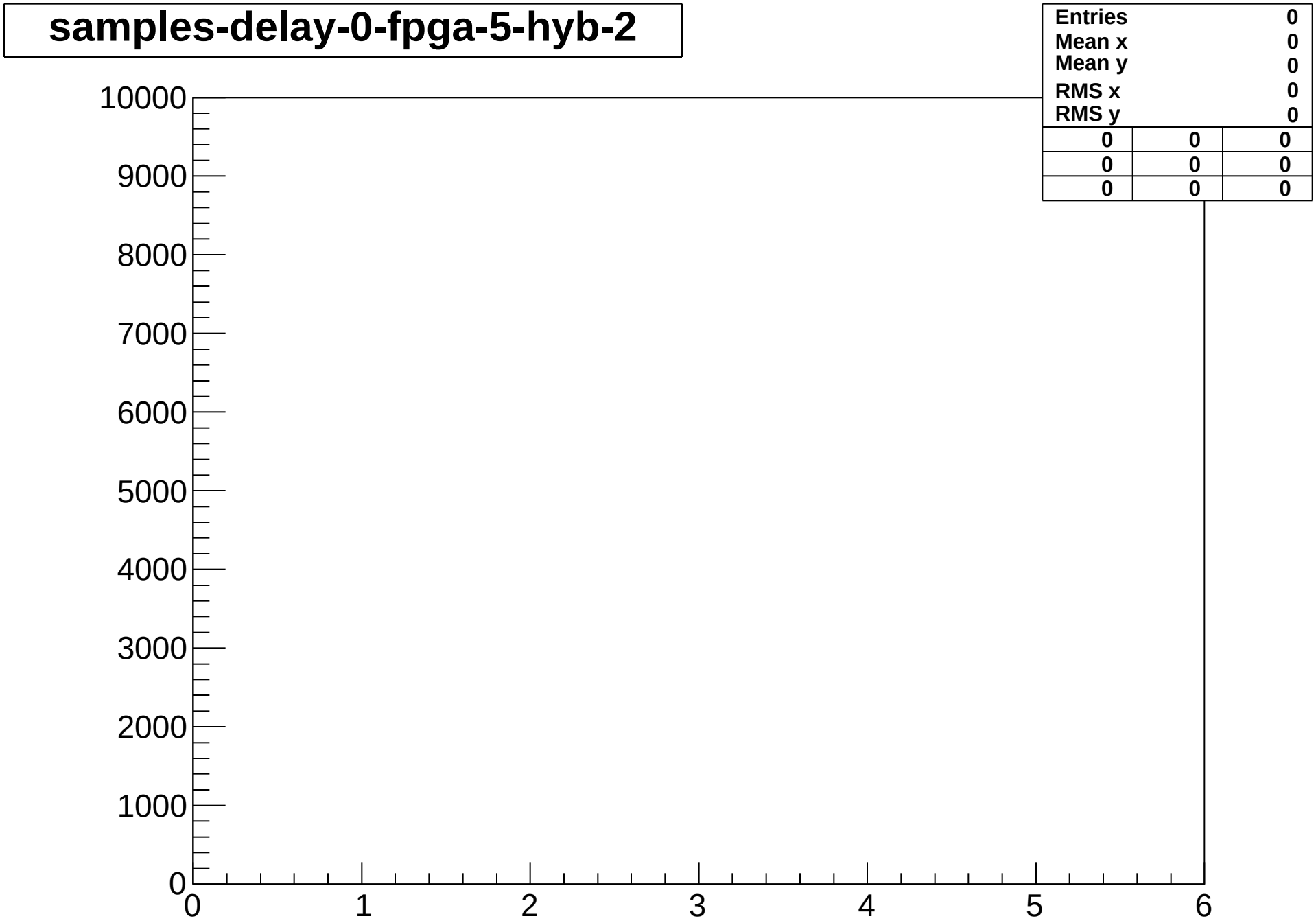
samples-delay-0-fpga-5-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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6000
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4000
3000
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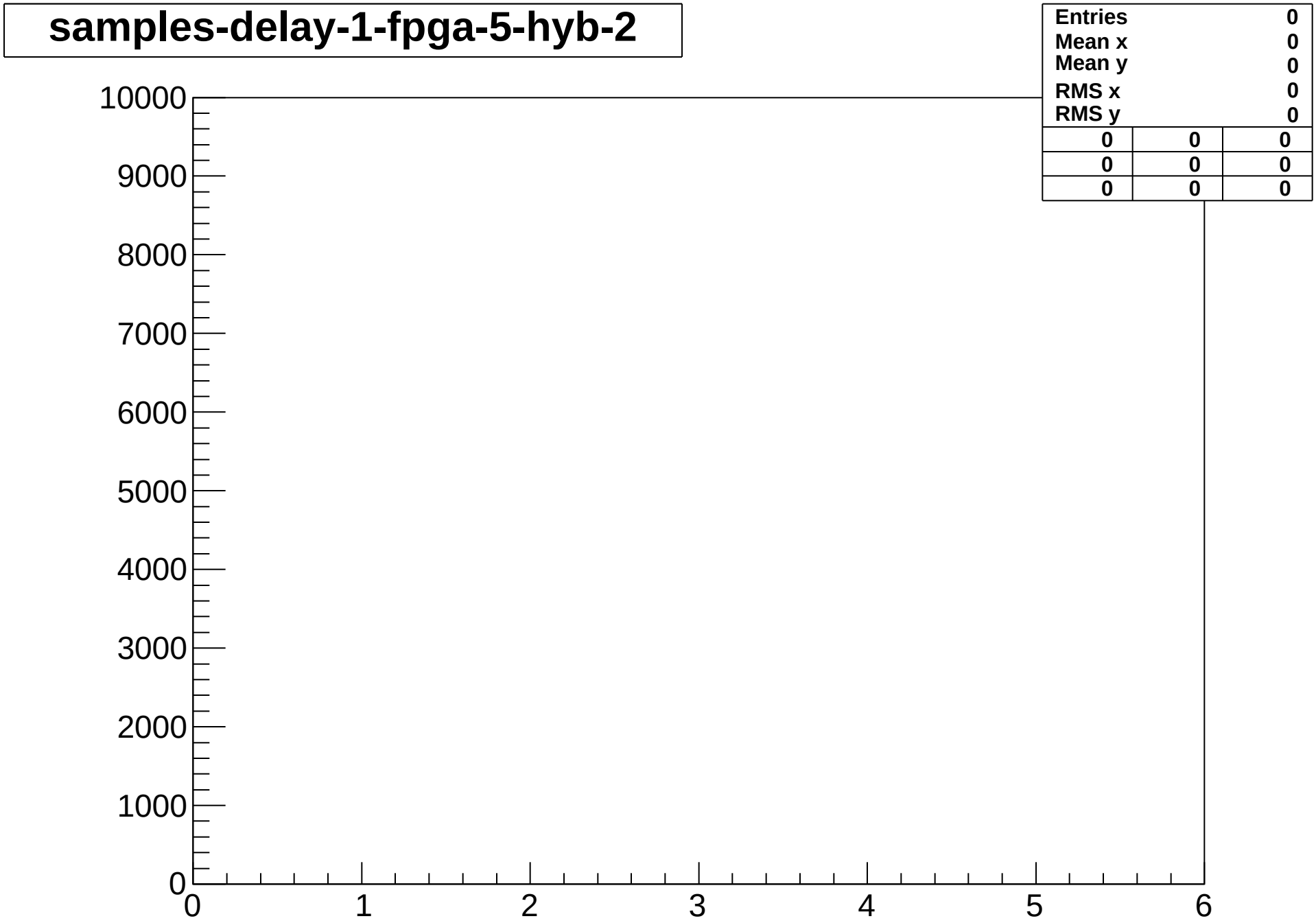
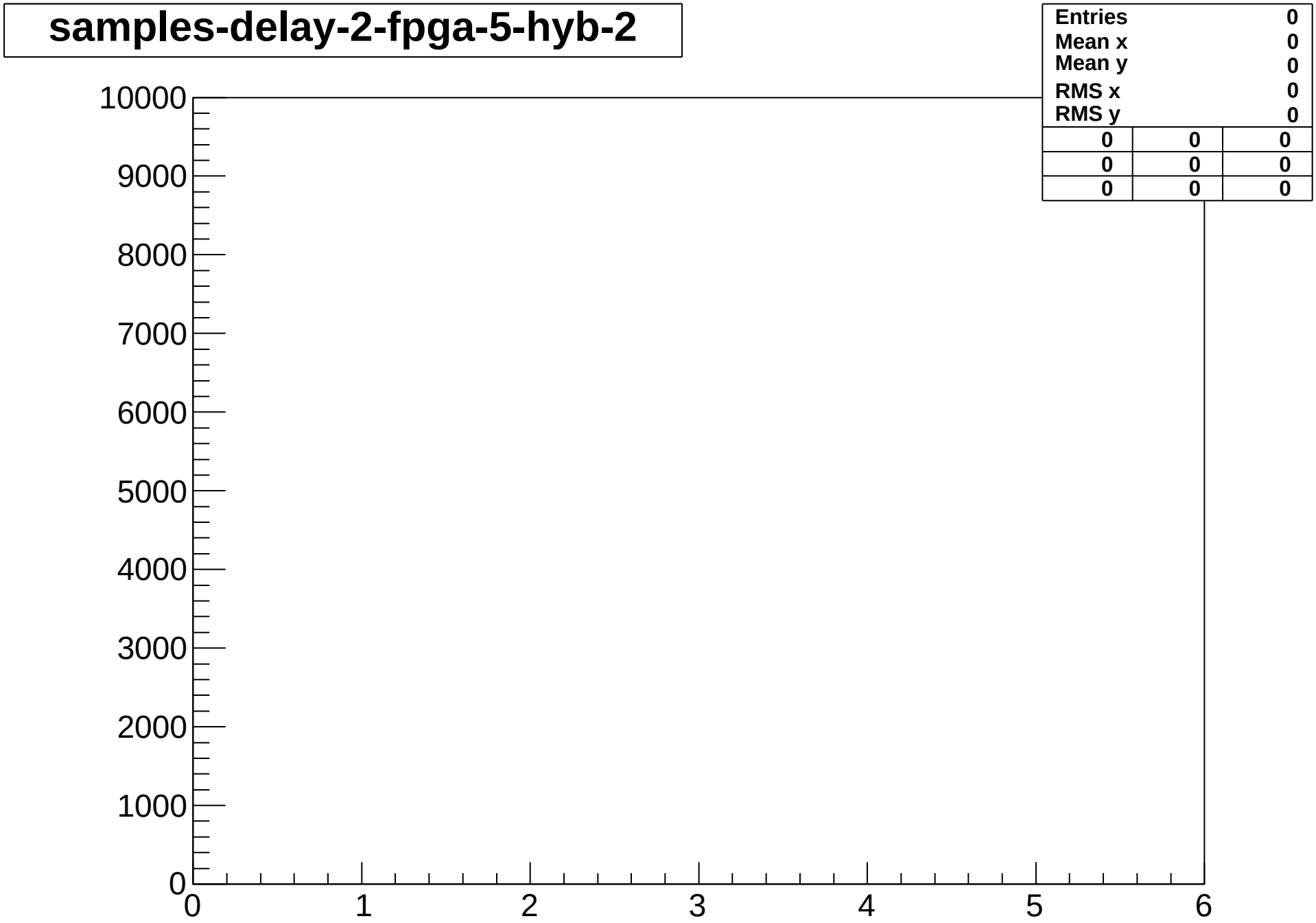
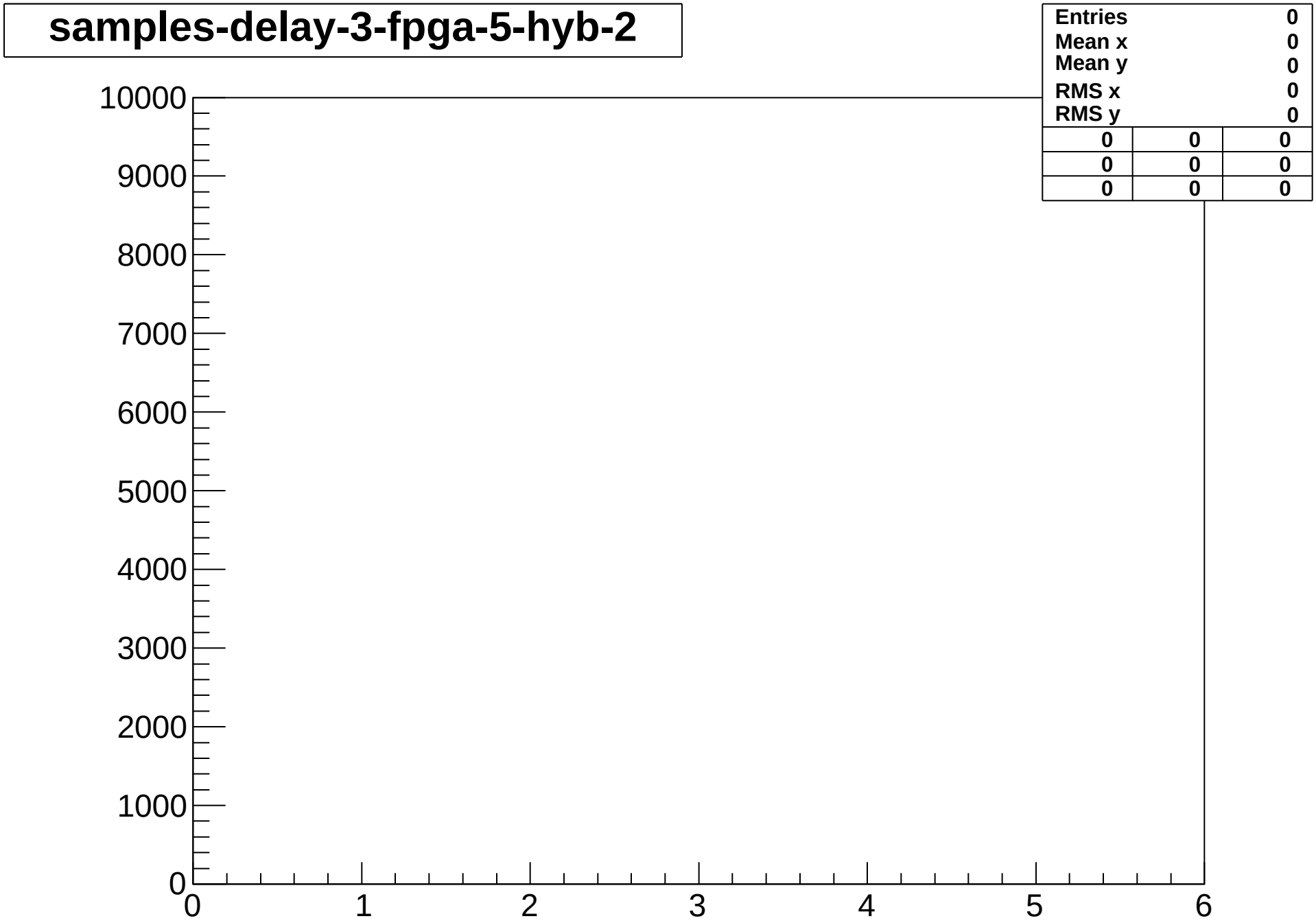
samples-delay-1-fpga-5-hyb-2



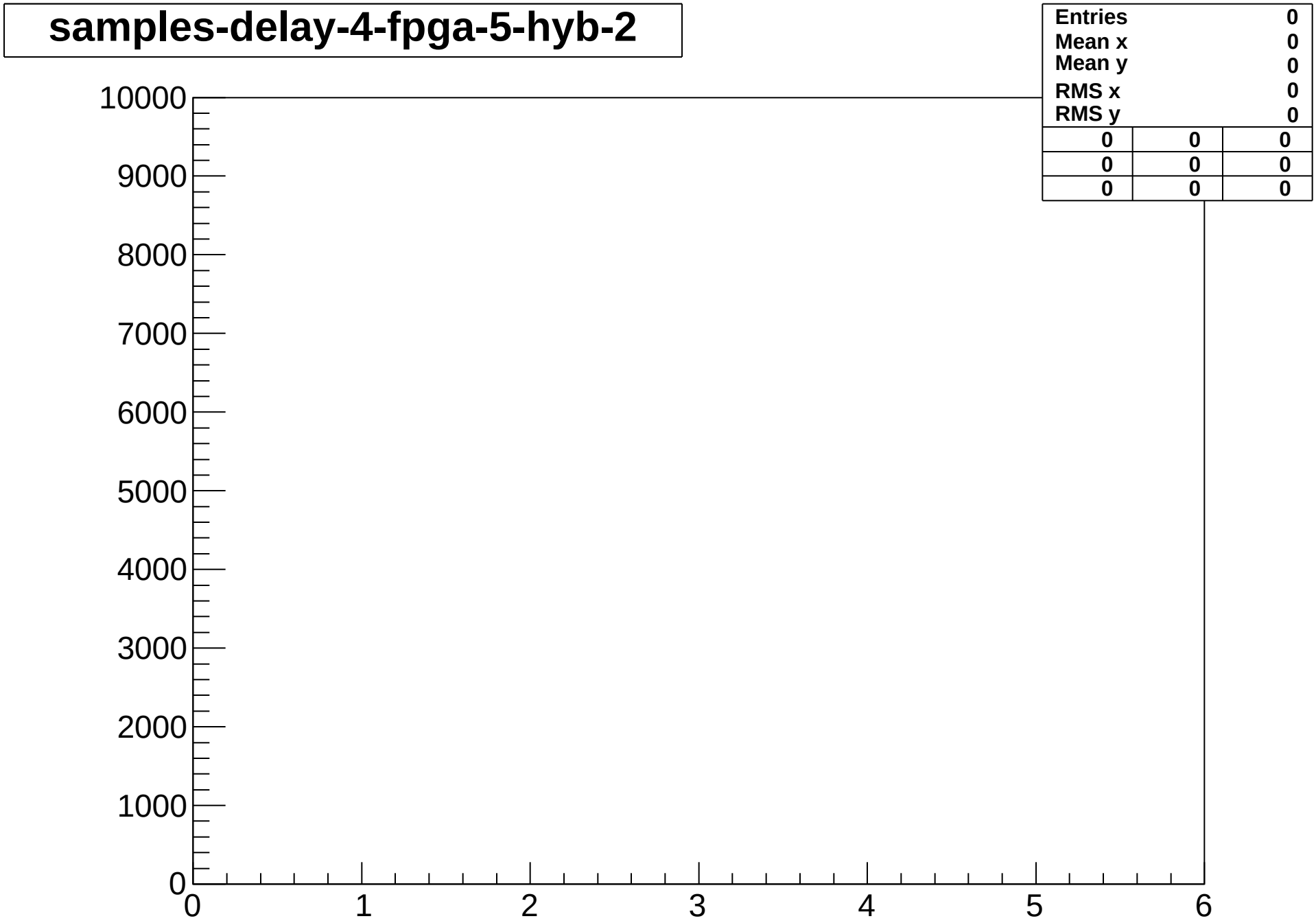
samples-delay-2-fpga-5-hyb-2



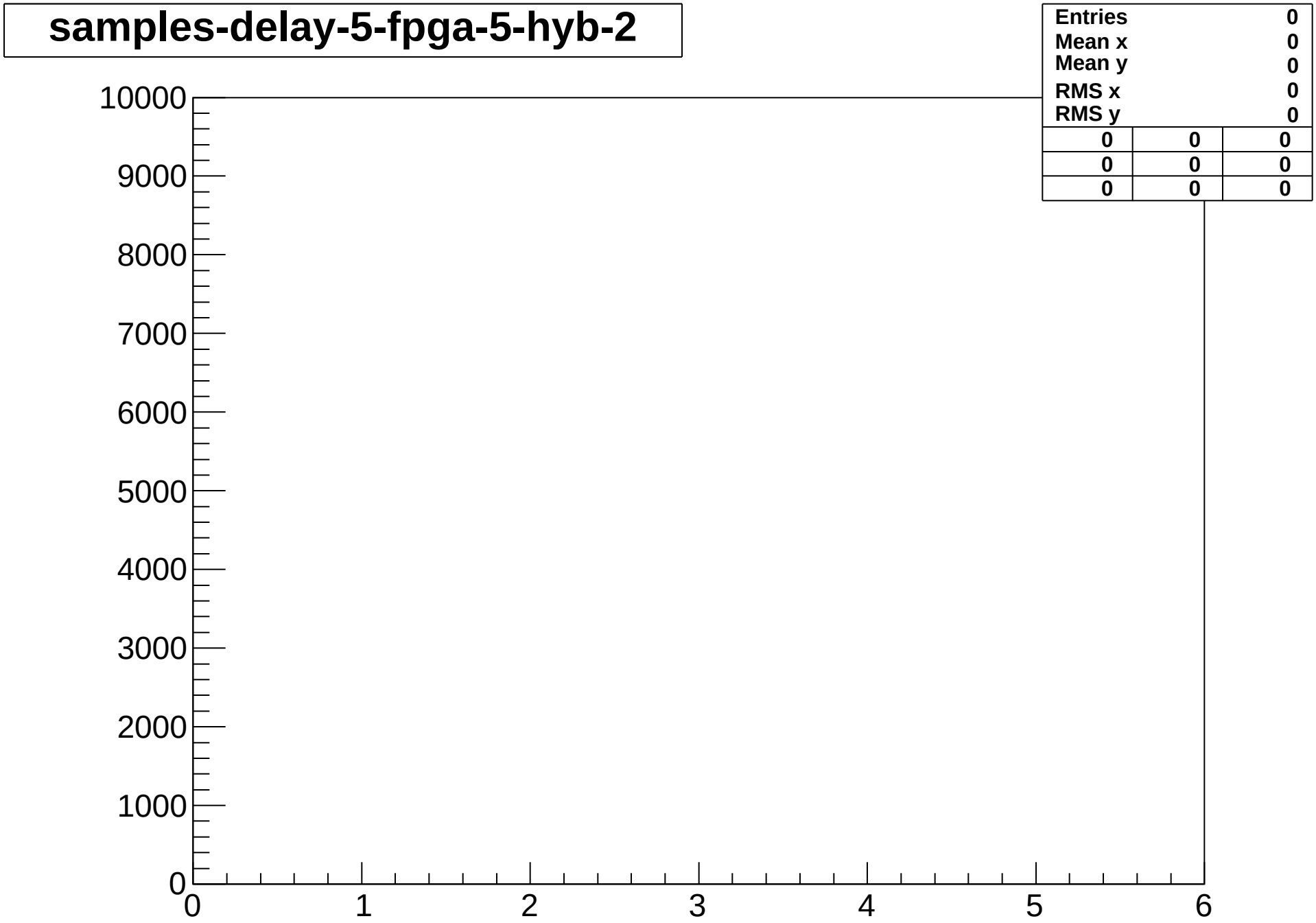
samples-delay-3-fpga-5-hyb-2



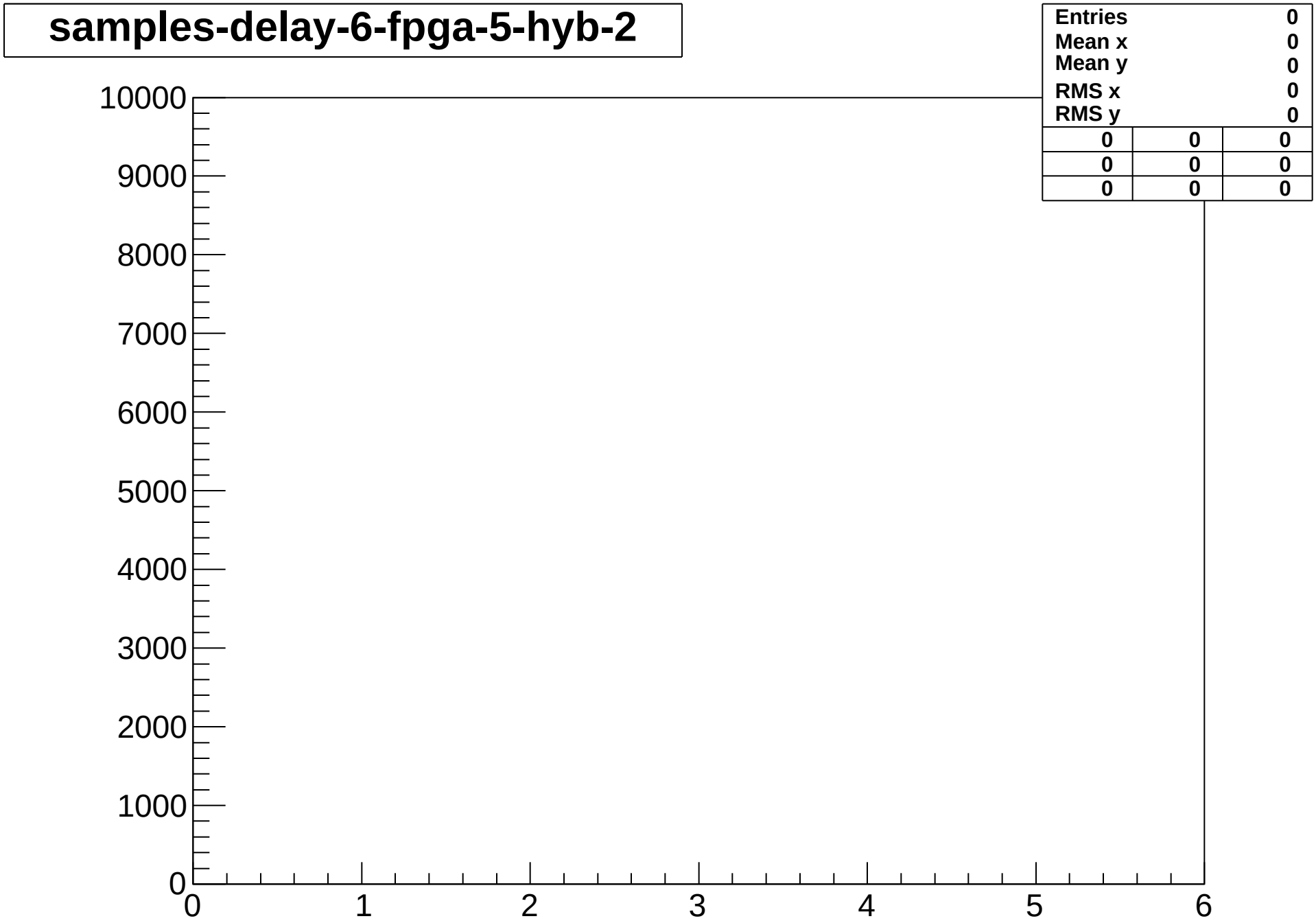
samples-delay-4-fpga-5-hyb-2



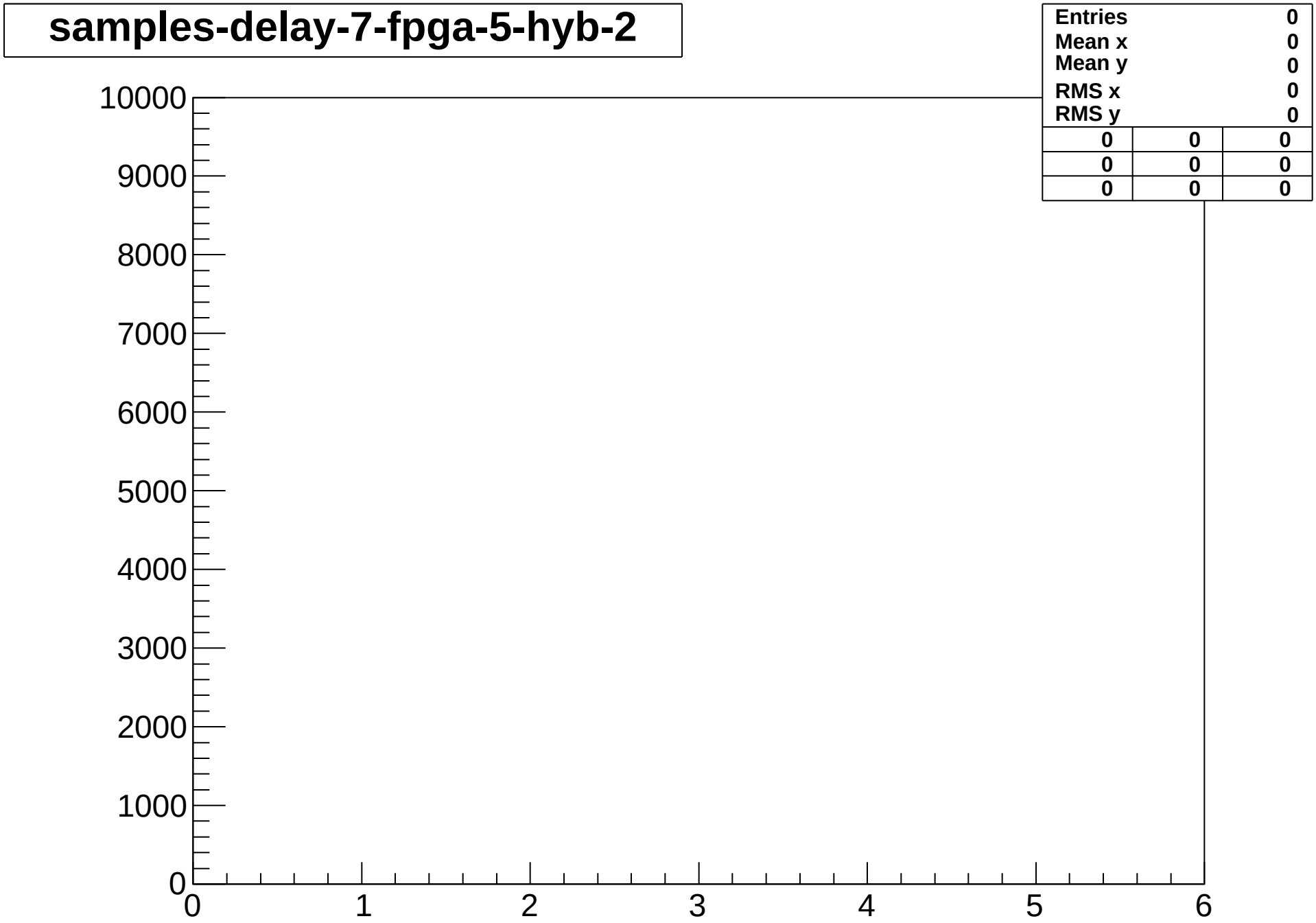
samples-delay-5-fpga-5-hyb-2



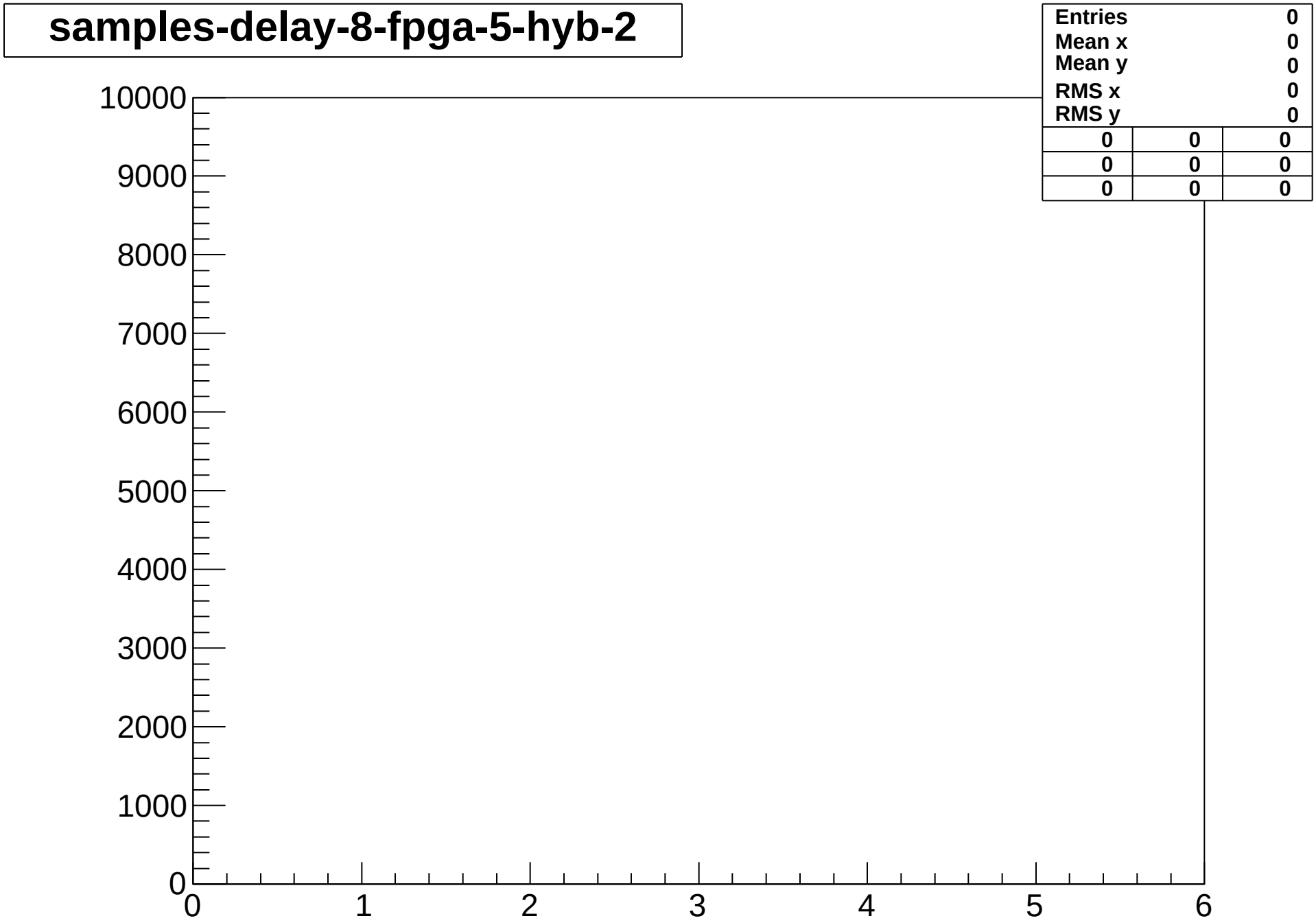
samples-delay-6-fpga-5-hyb-2

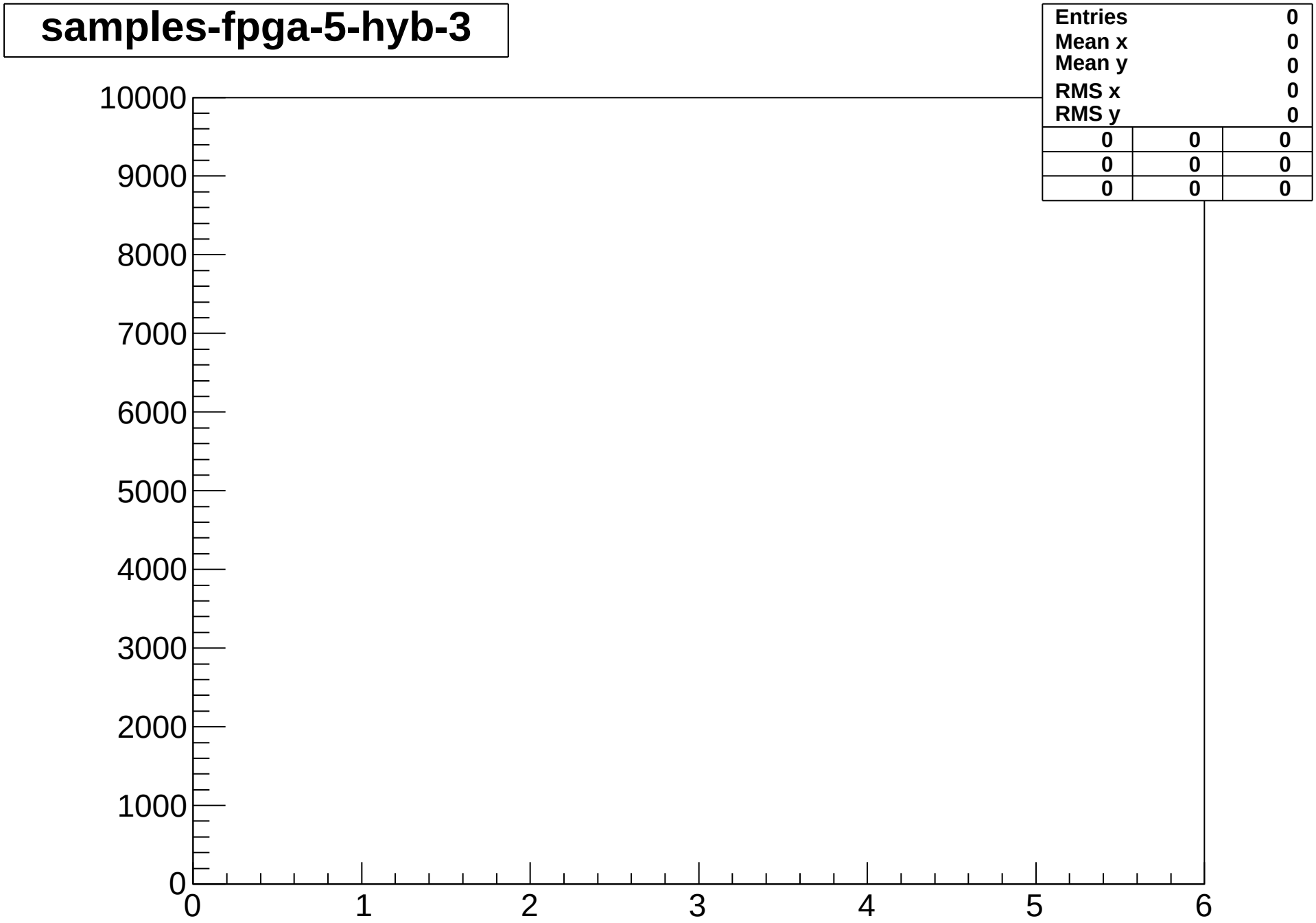


samples-delay-7-fpga-5-hyb-2



samples-delay-8-fpga-5-hyb-2




samples-fpga-5-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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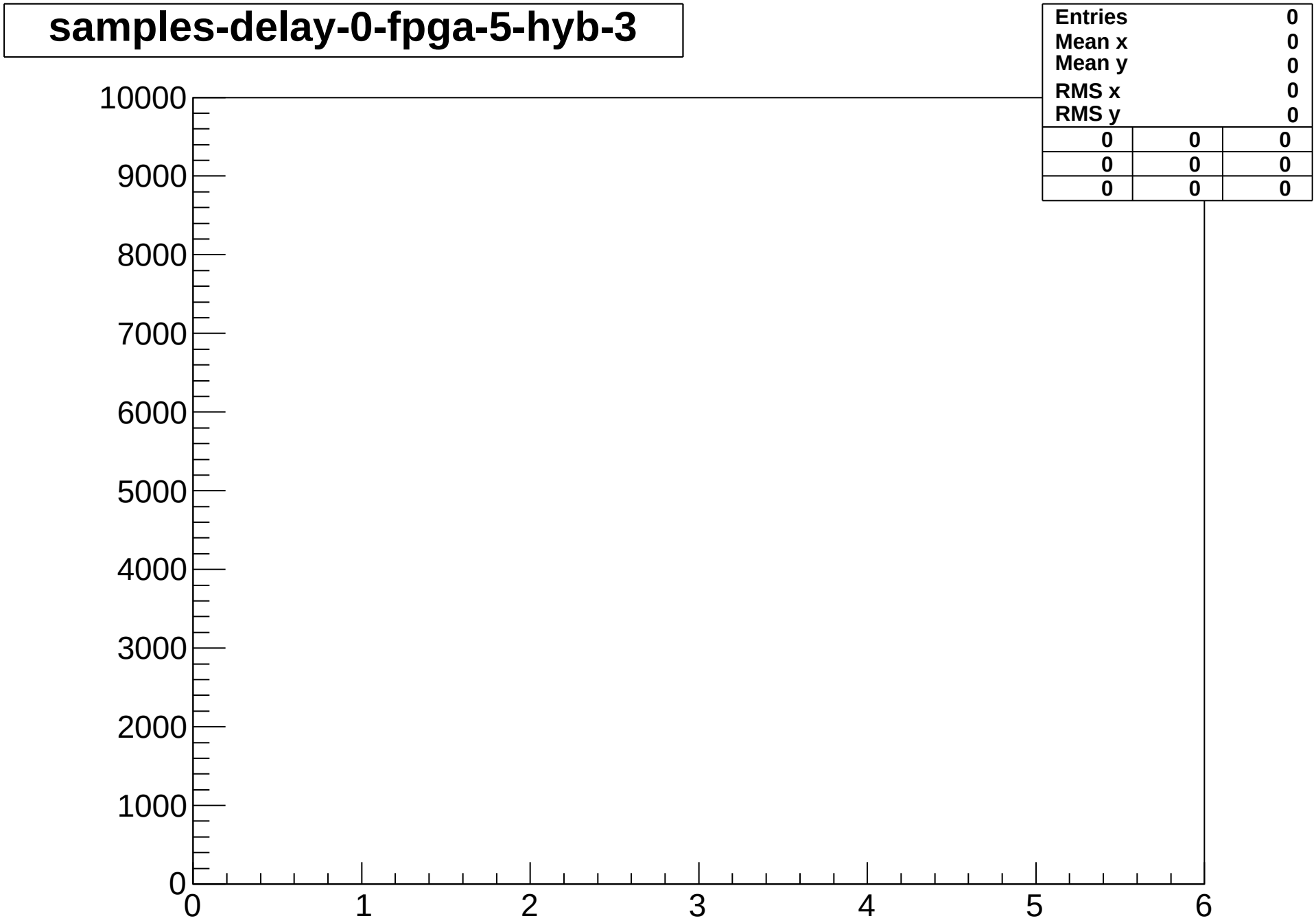
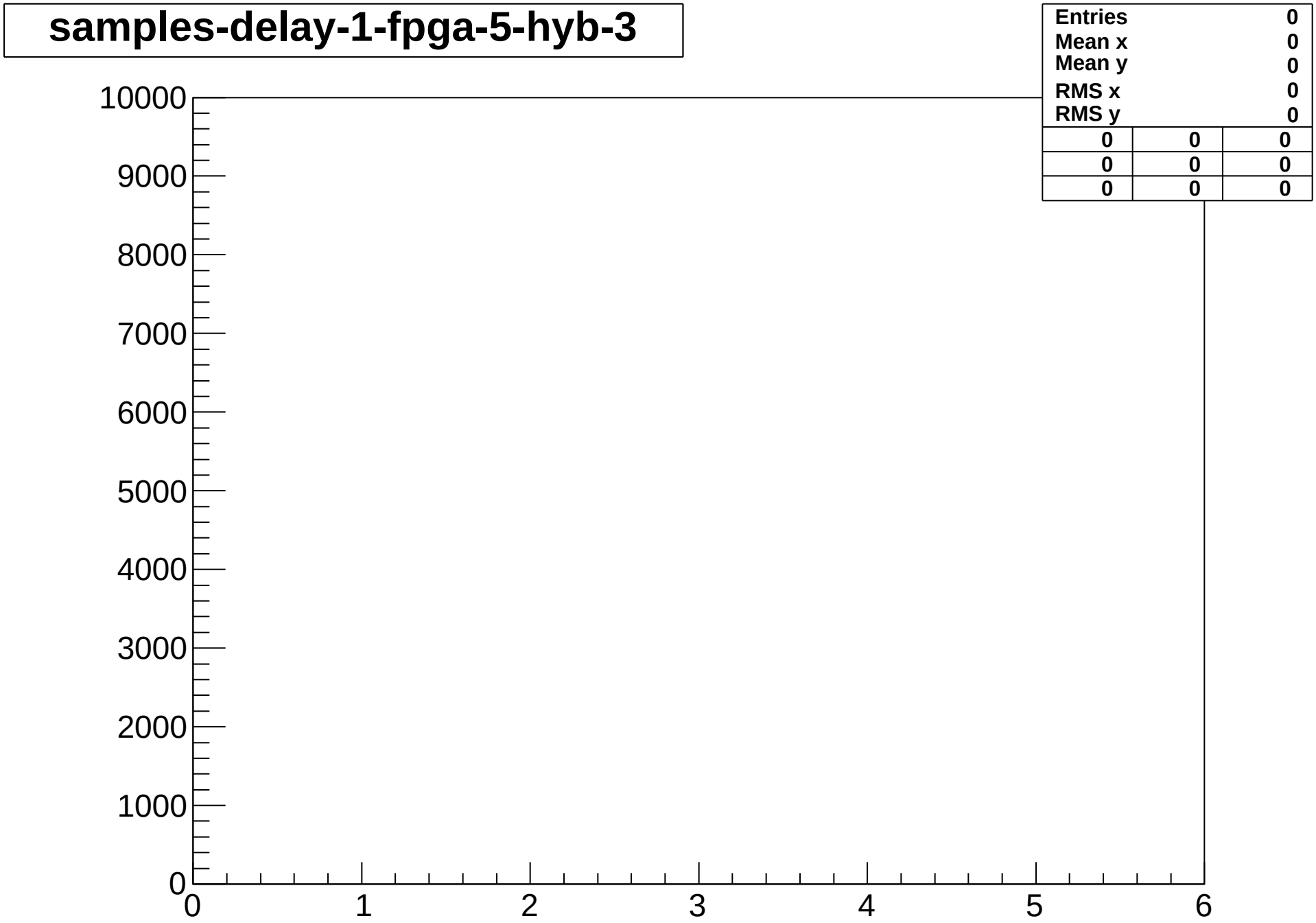
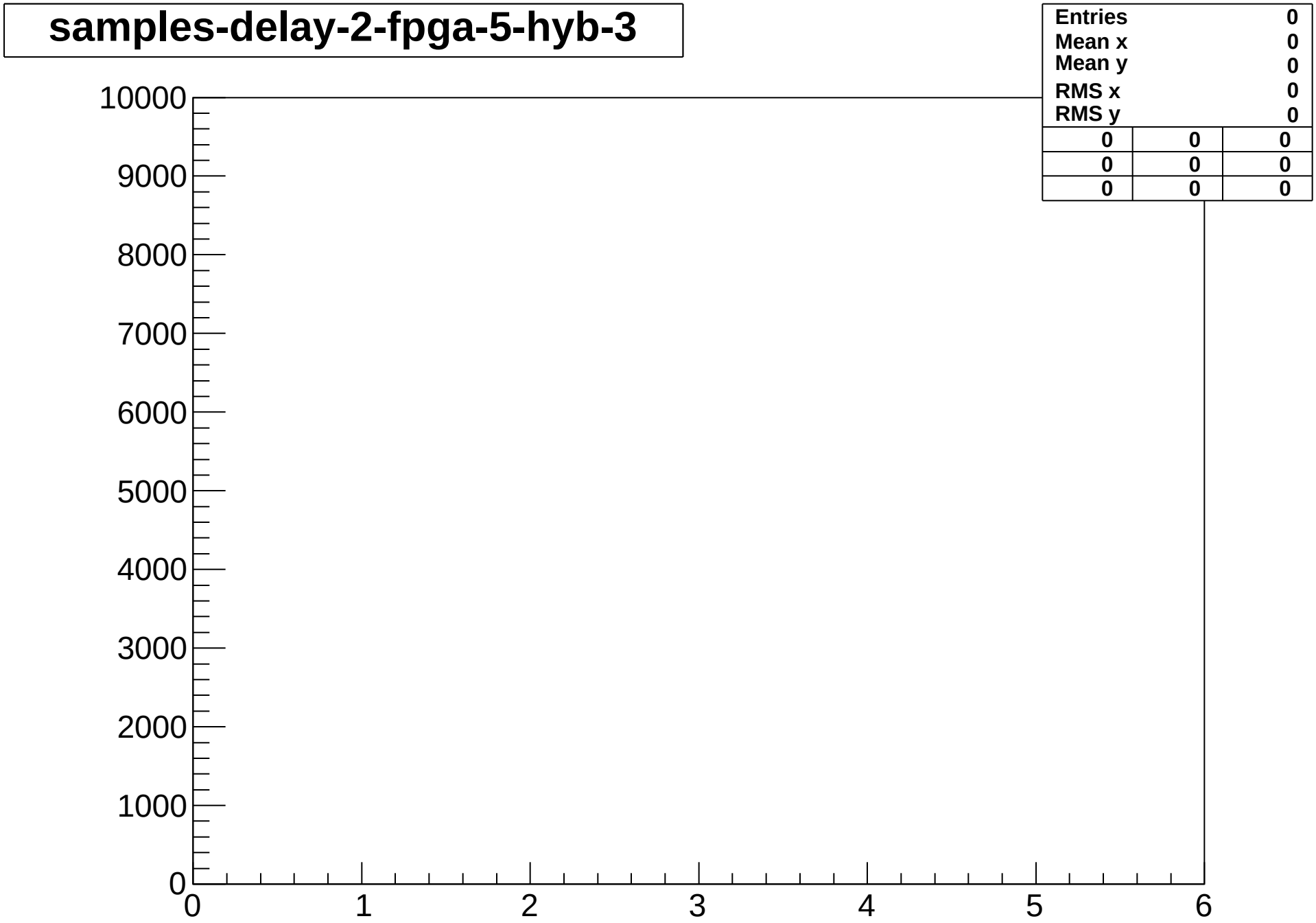
samples-delay-0-fpga-5-hyb-3



samples-delay-1-fpga-5-hyb-3




samples-delay-2-fpga-5-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
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0
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1
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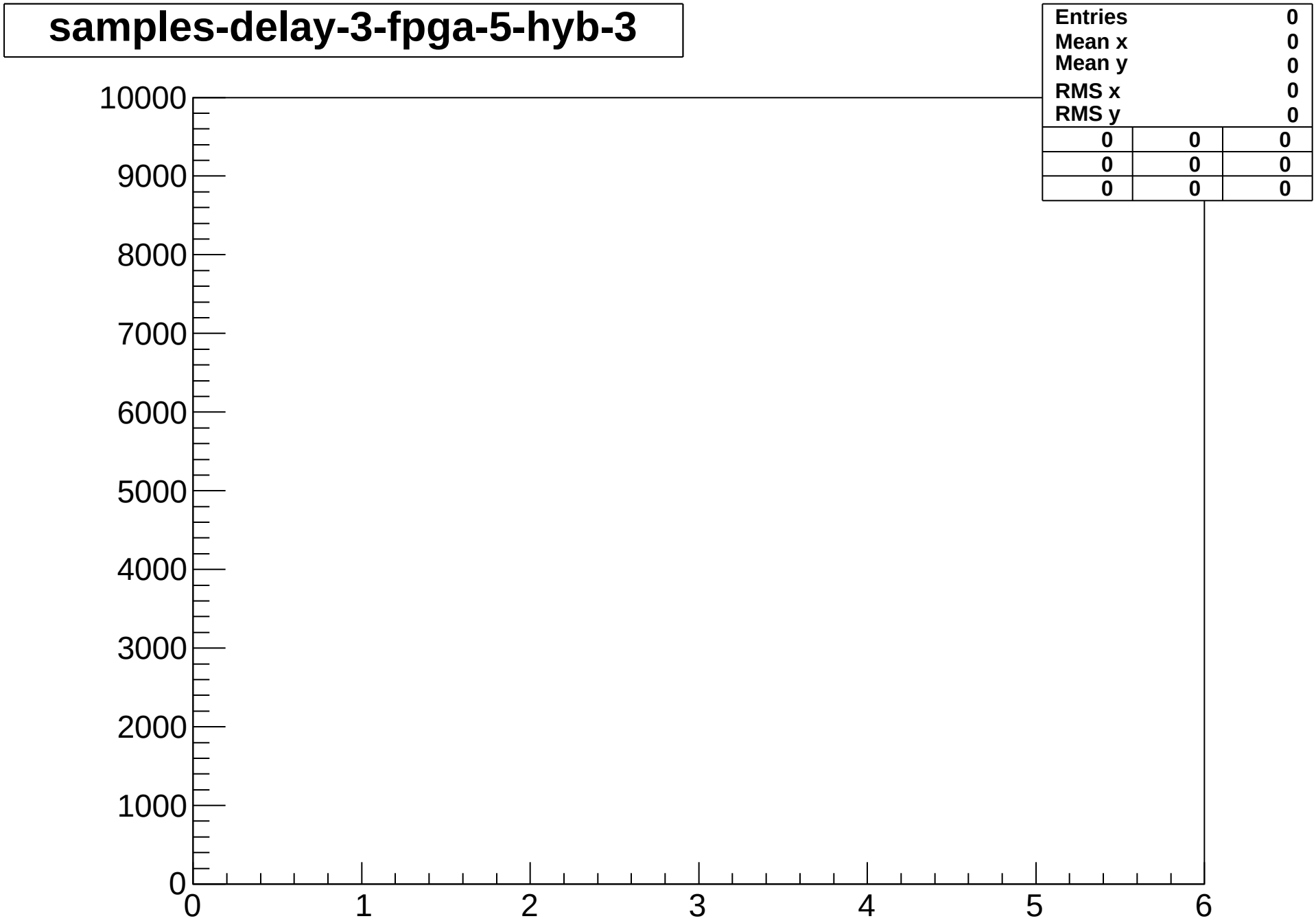
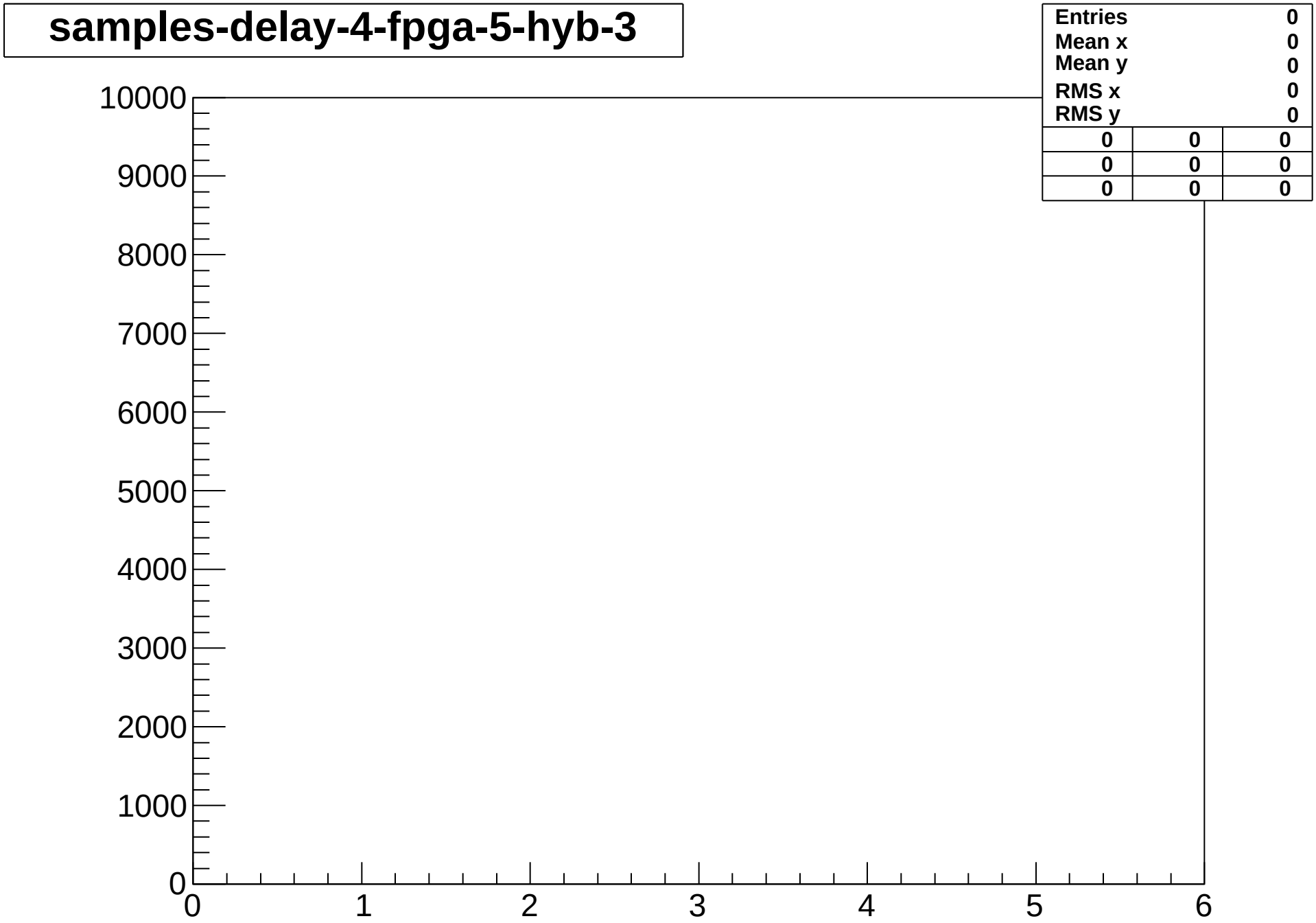
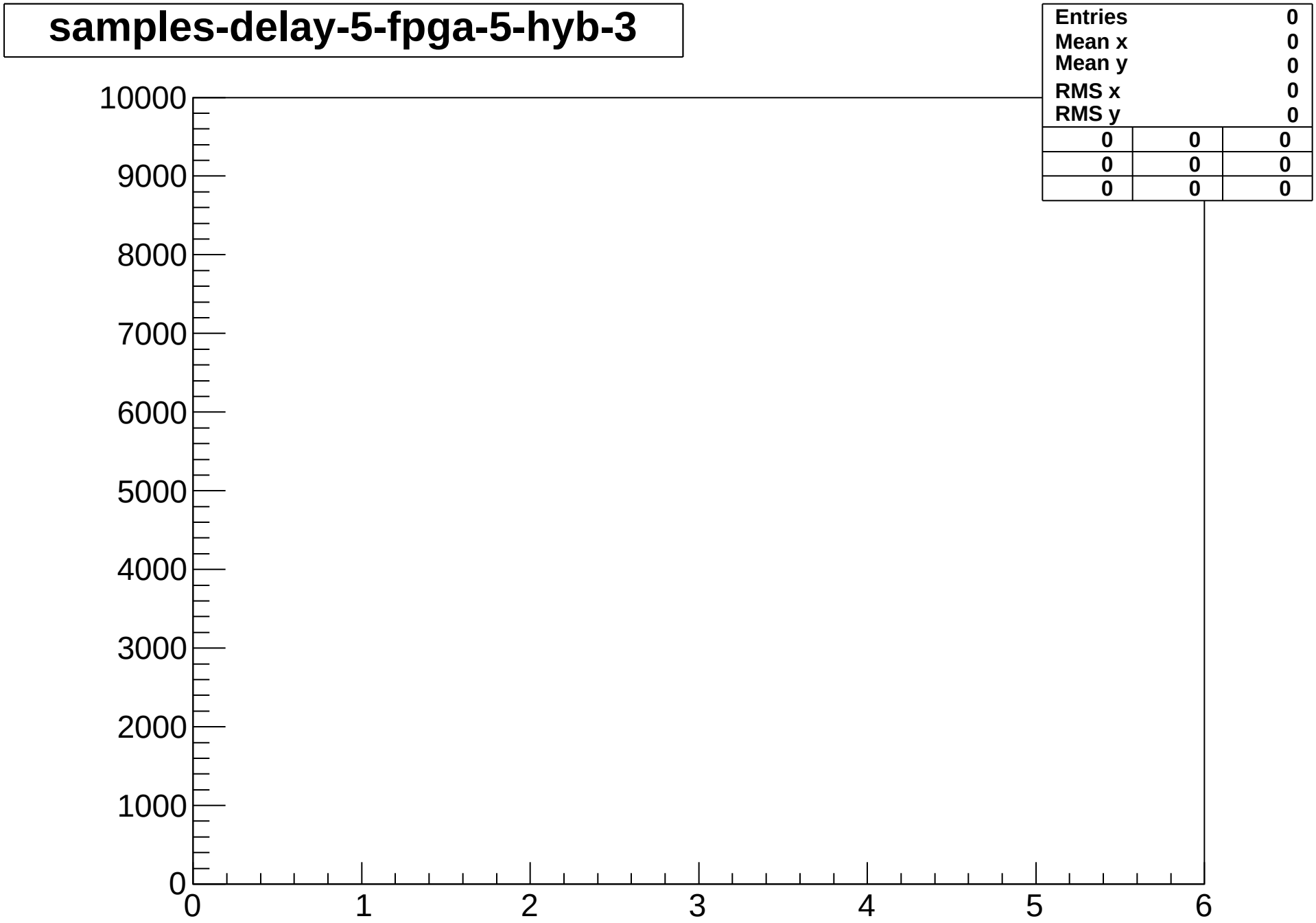
samples-delay-3-fpga-5-hyb-3



samples-delay-4-fpga-5-hyb-3




samples-delay-5-fpga-5-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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8000
7000
6000
5000
4000
3000
2000
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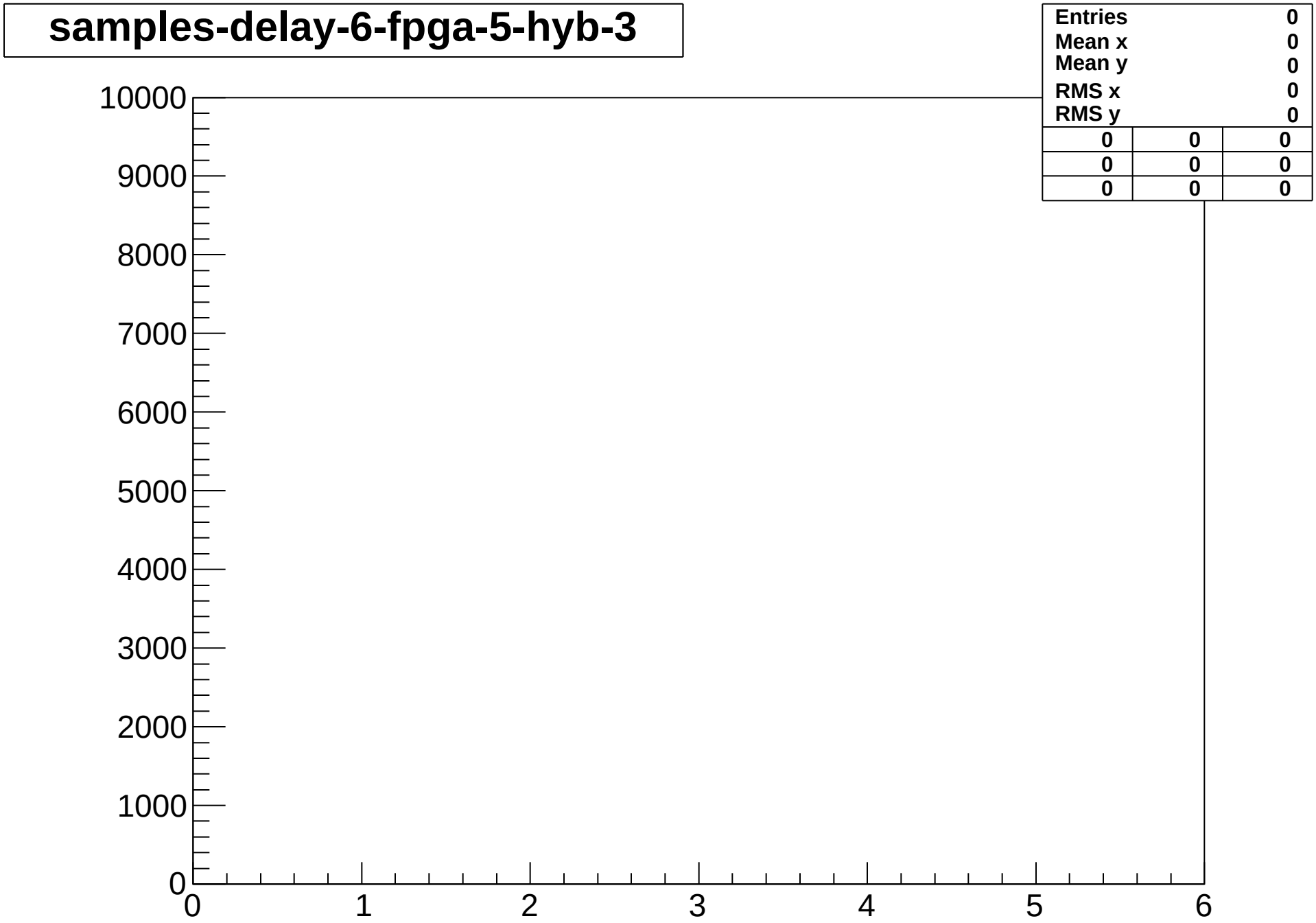
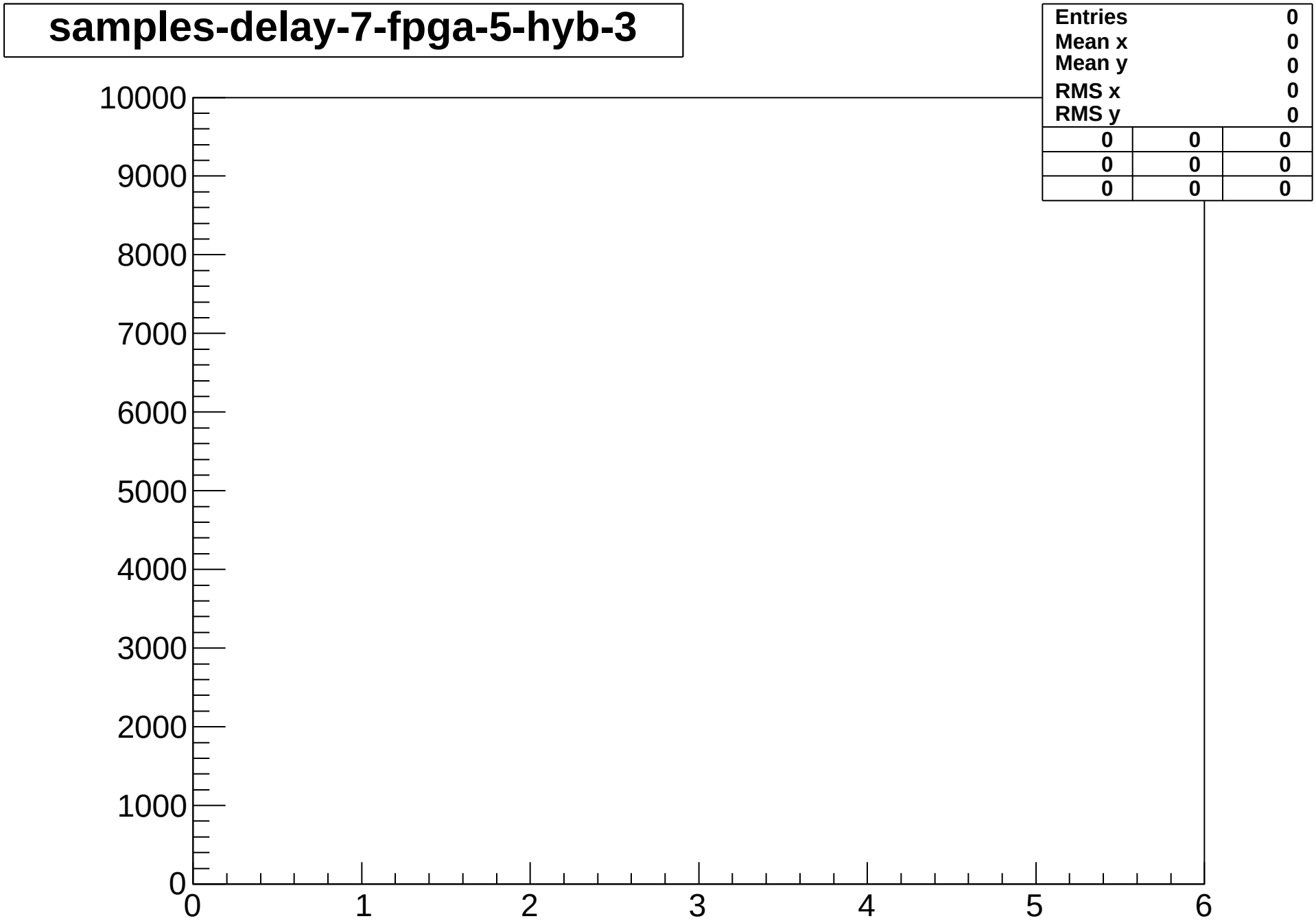
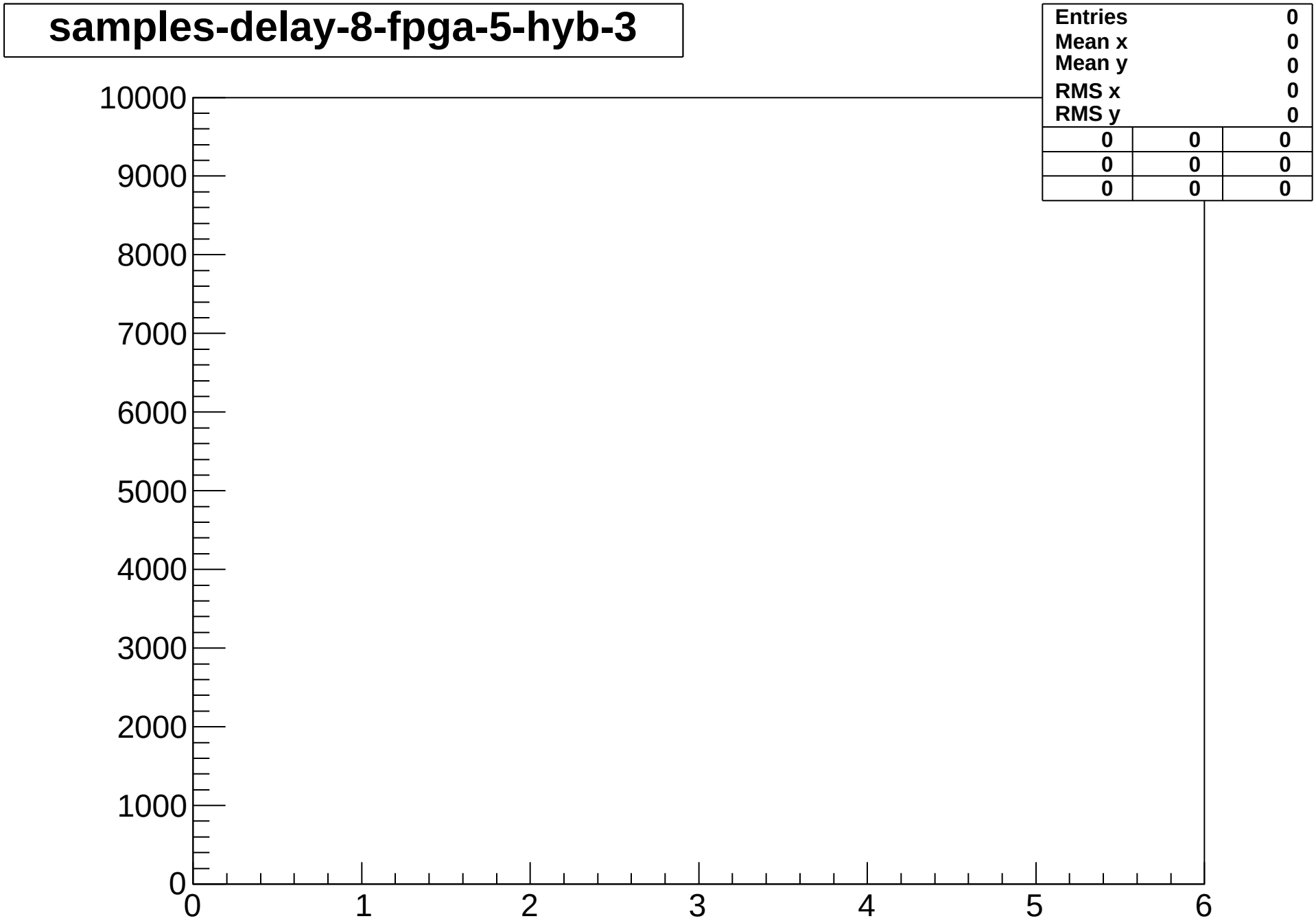
samples-delay-6-fpga-5-hyb-3

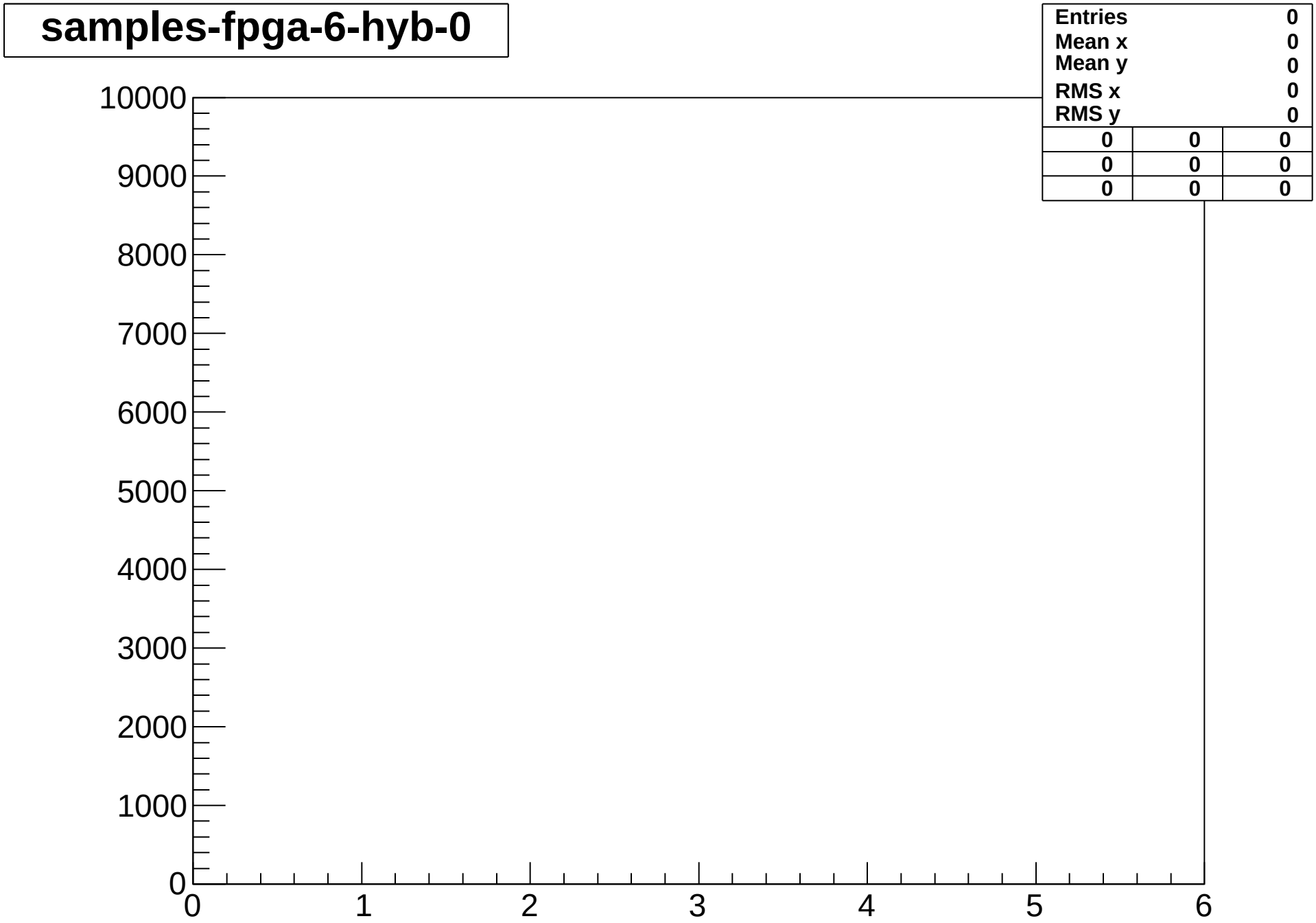


samples-delay-7-fpga-5-hyb-3



samples-delay-8-fpga-5-hyb-3




samples-fpga-6-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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4
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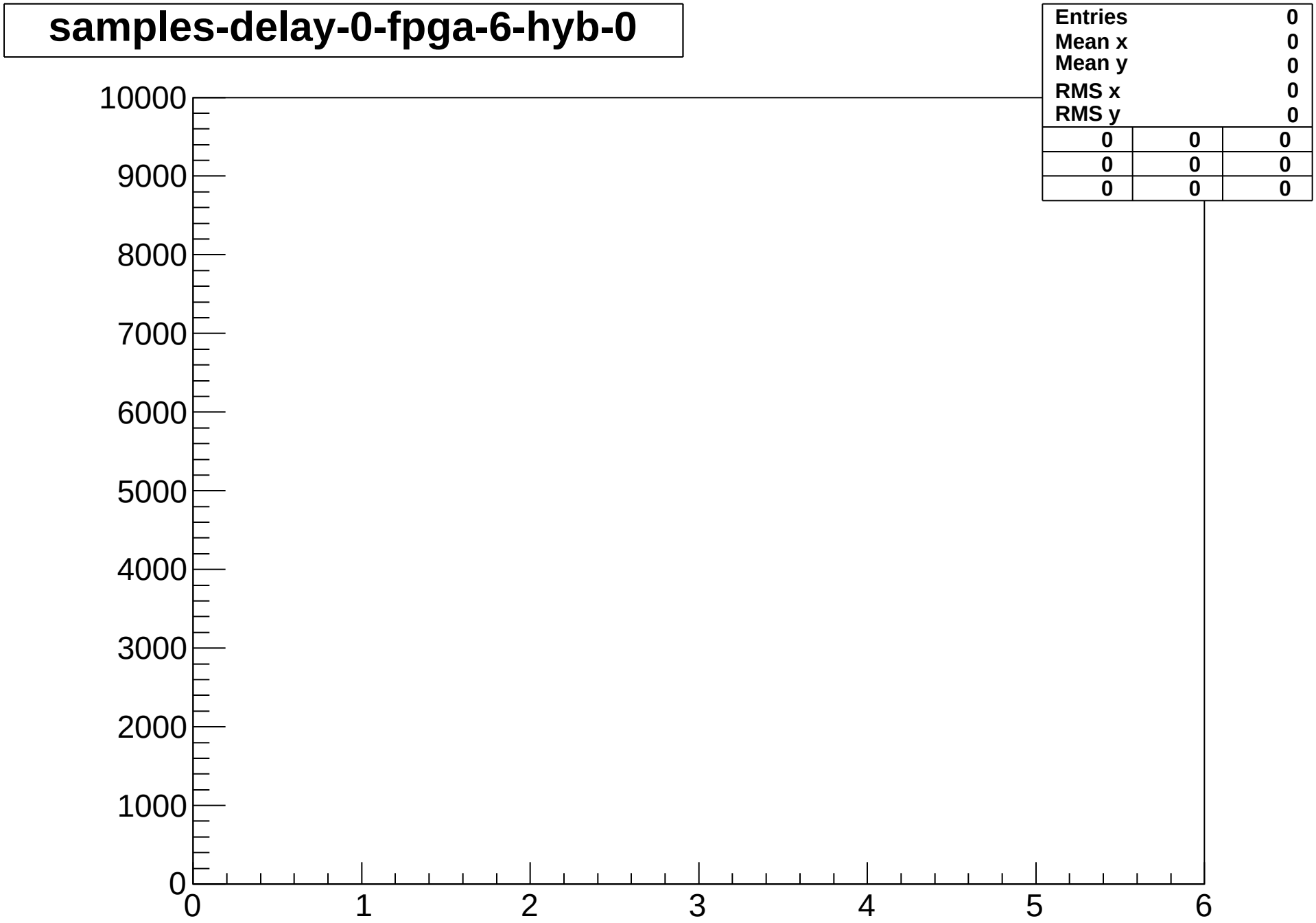
6


samples-delay-0-fpga-6-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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8000
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6000
5000
4000
3000
2000
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0
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1
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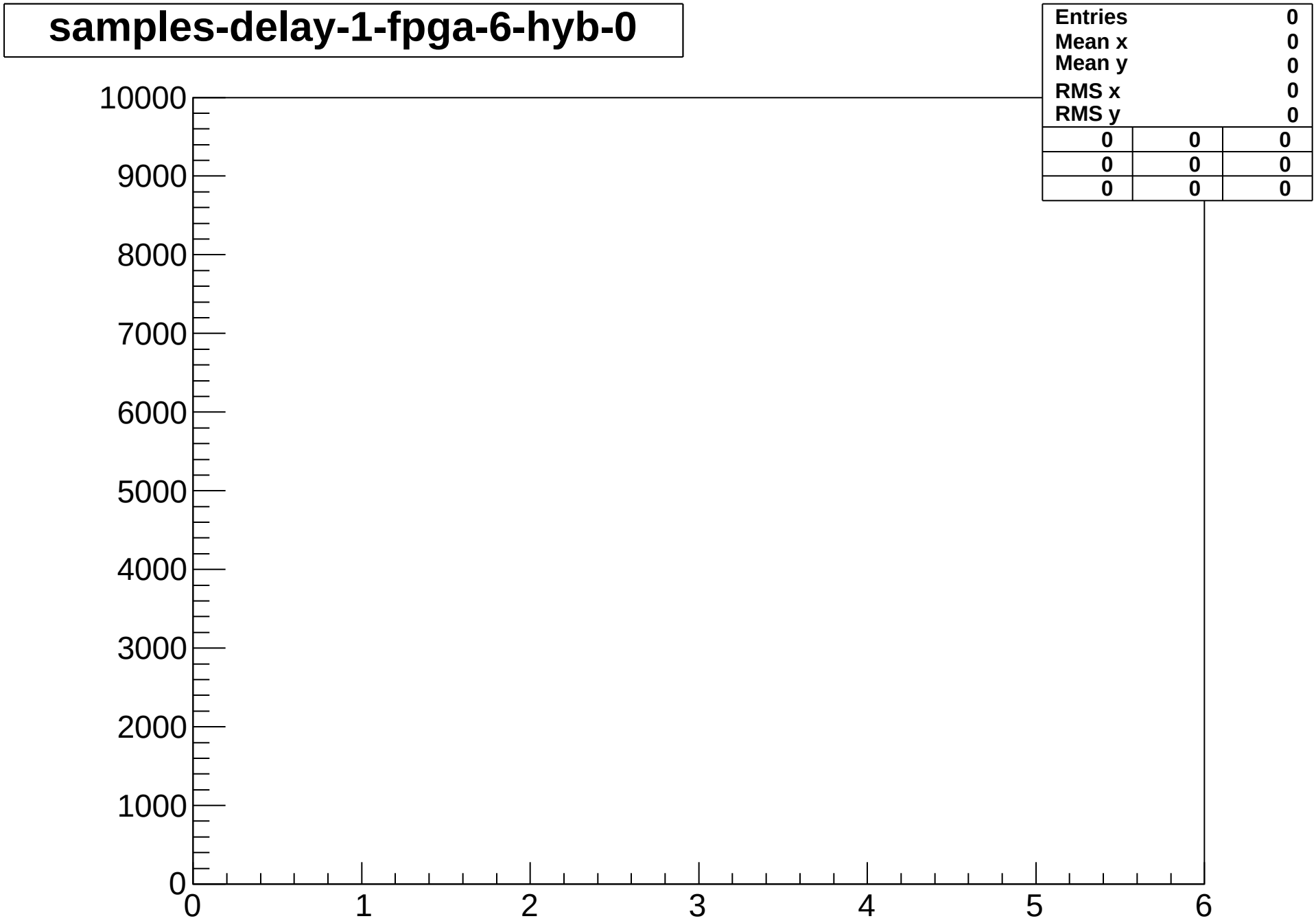
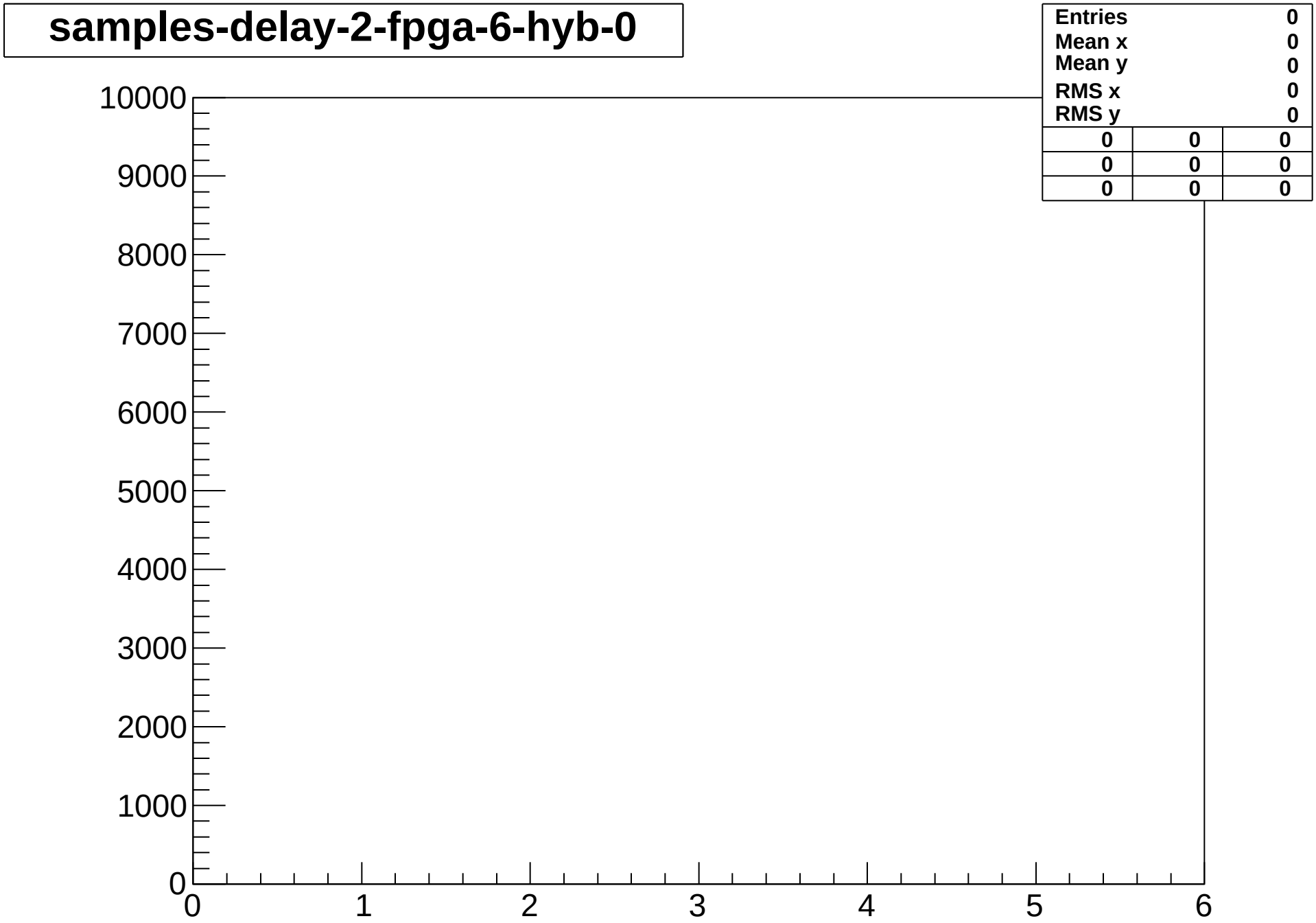
samples-delay-1-fpga-6-hyb-0




samples-delay-2-fpga-6-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
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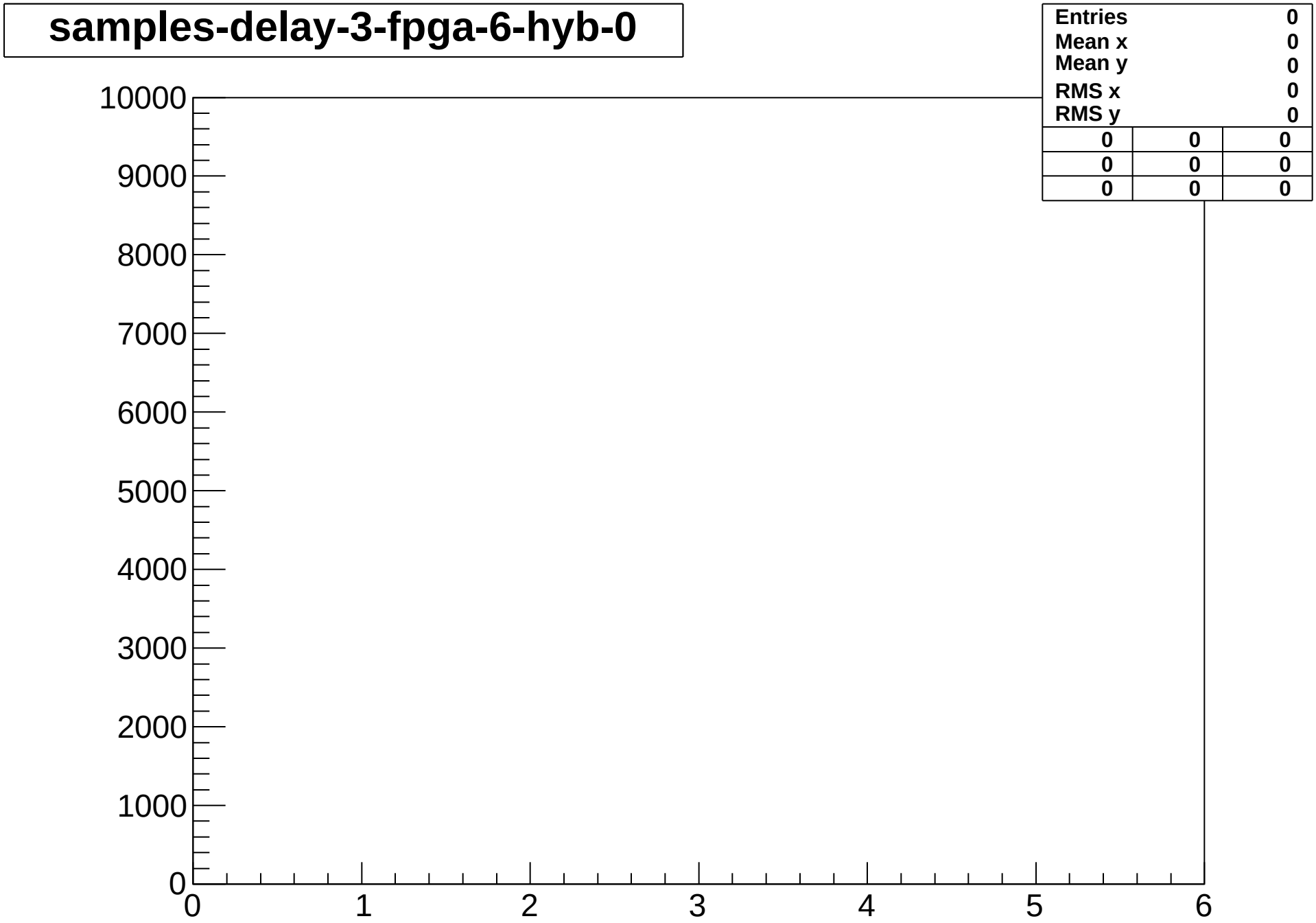
samples-delay-3-fpga-6-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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8000
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6000
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4000
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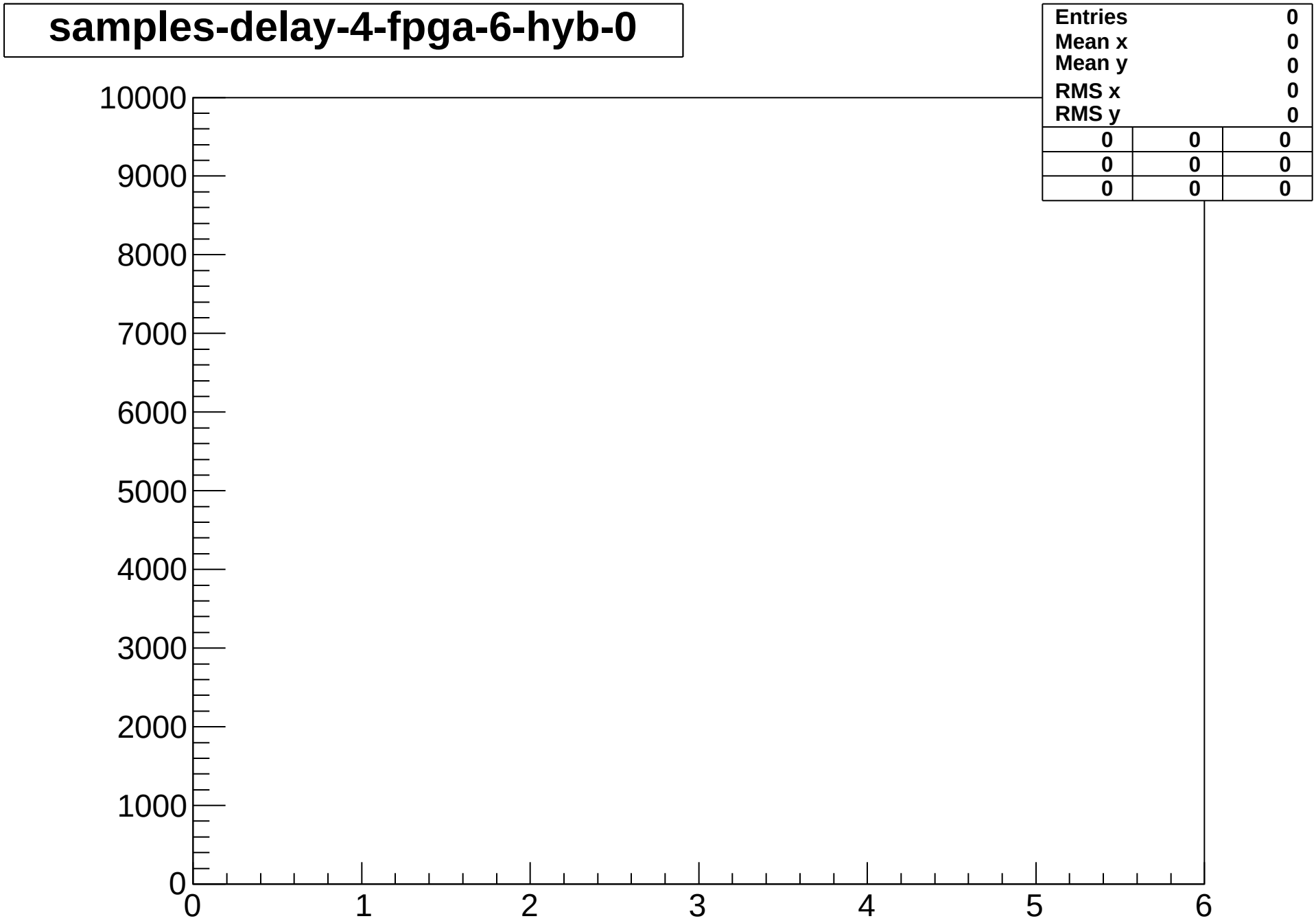
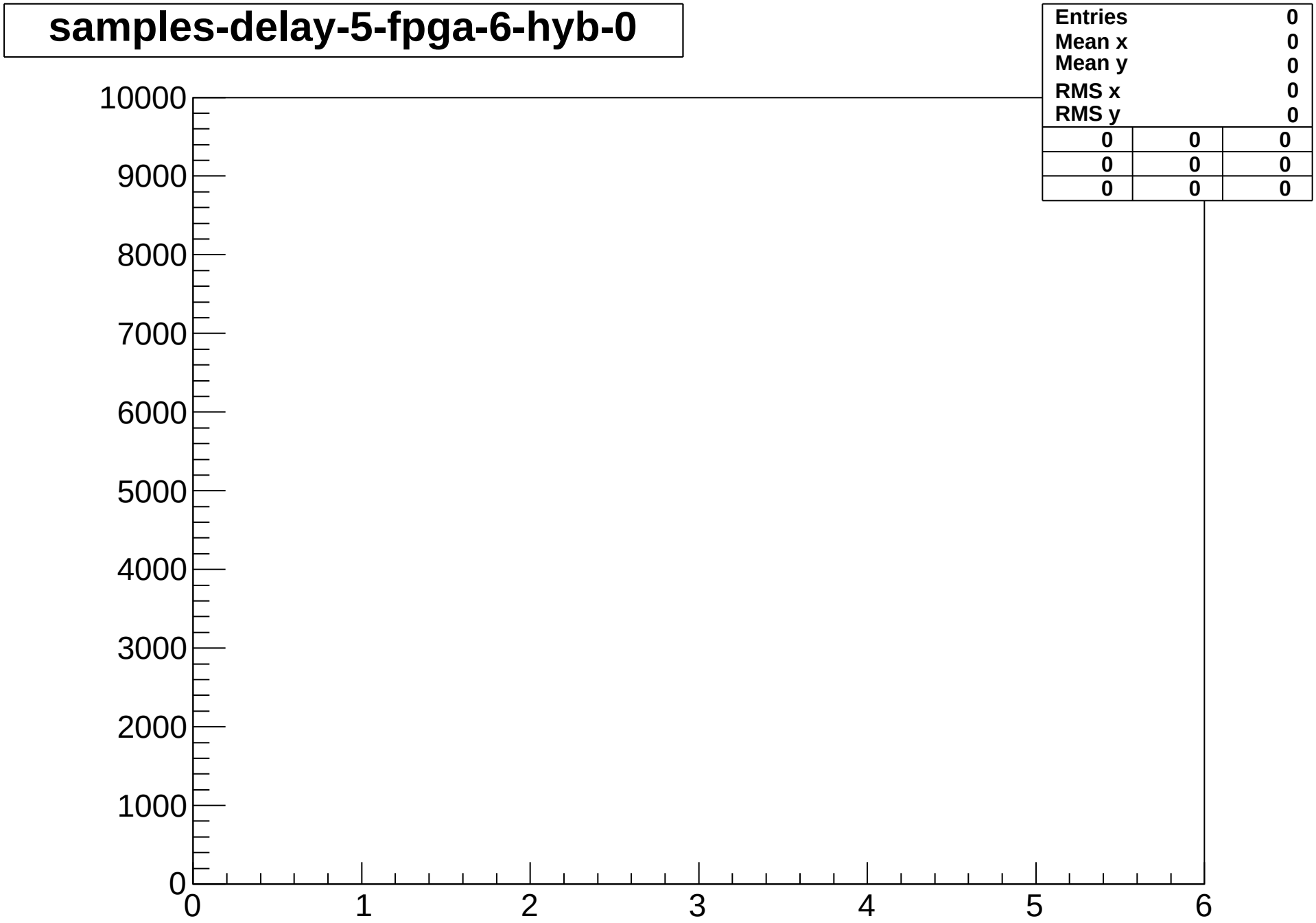
samples-delay-4-fpga-6-hyb-0




samples-delay-5-fpga-6-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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8000
7000
6000
5000
4000
3000
2000
1000
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1
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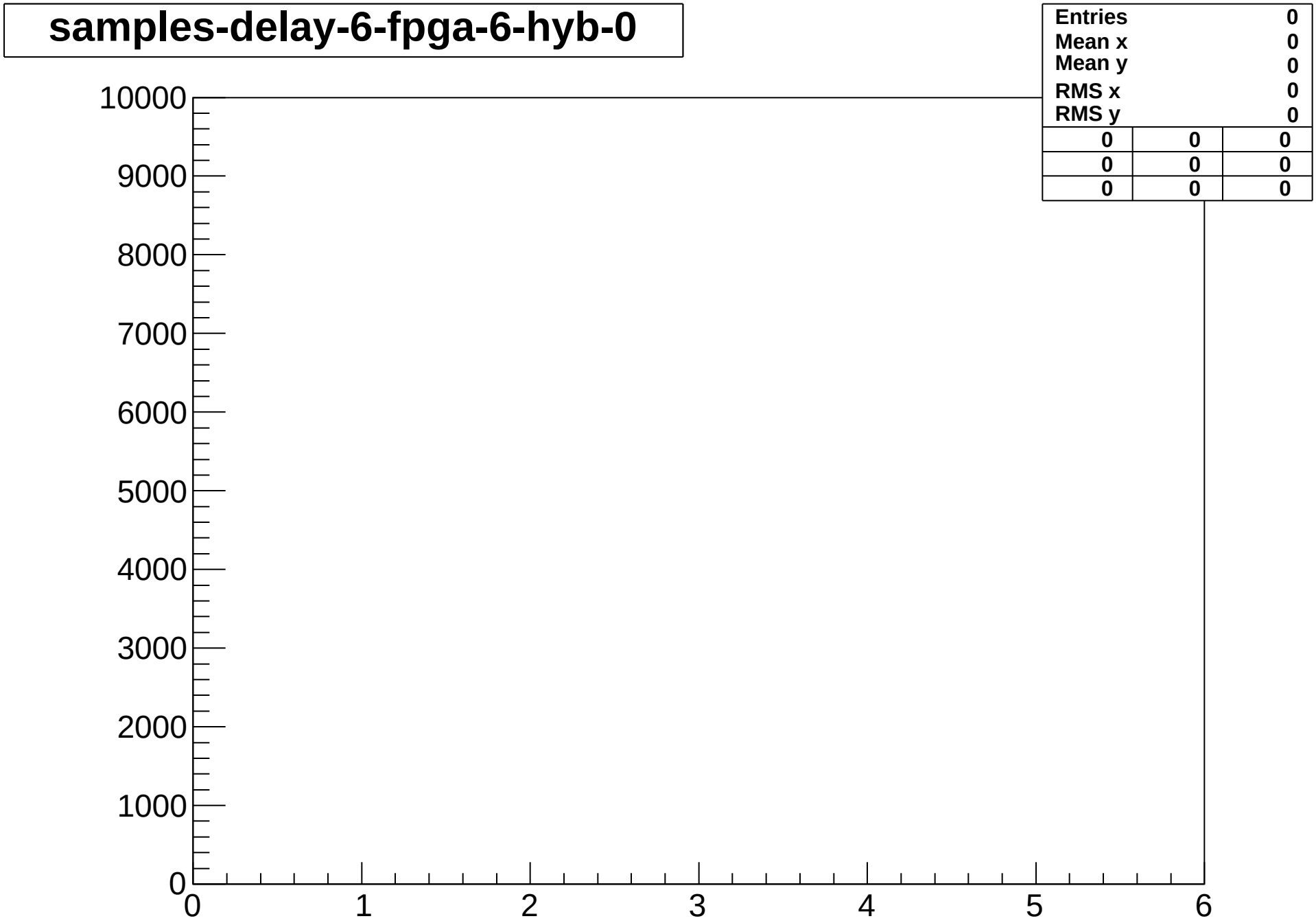
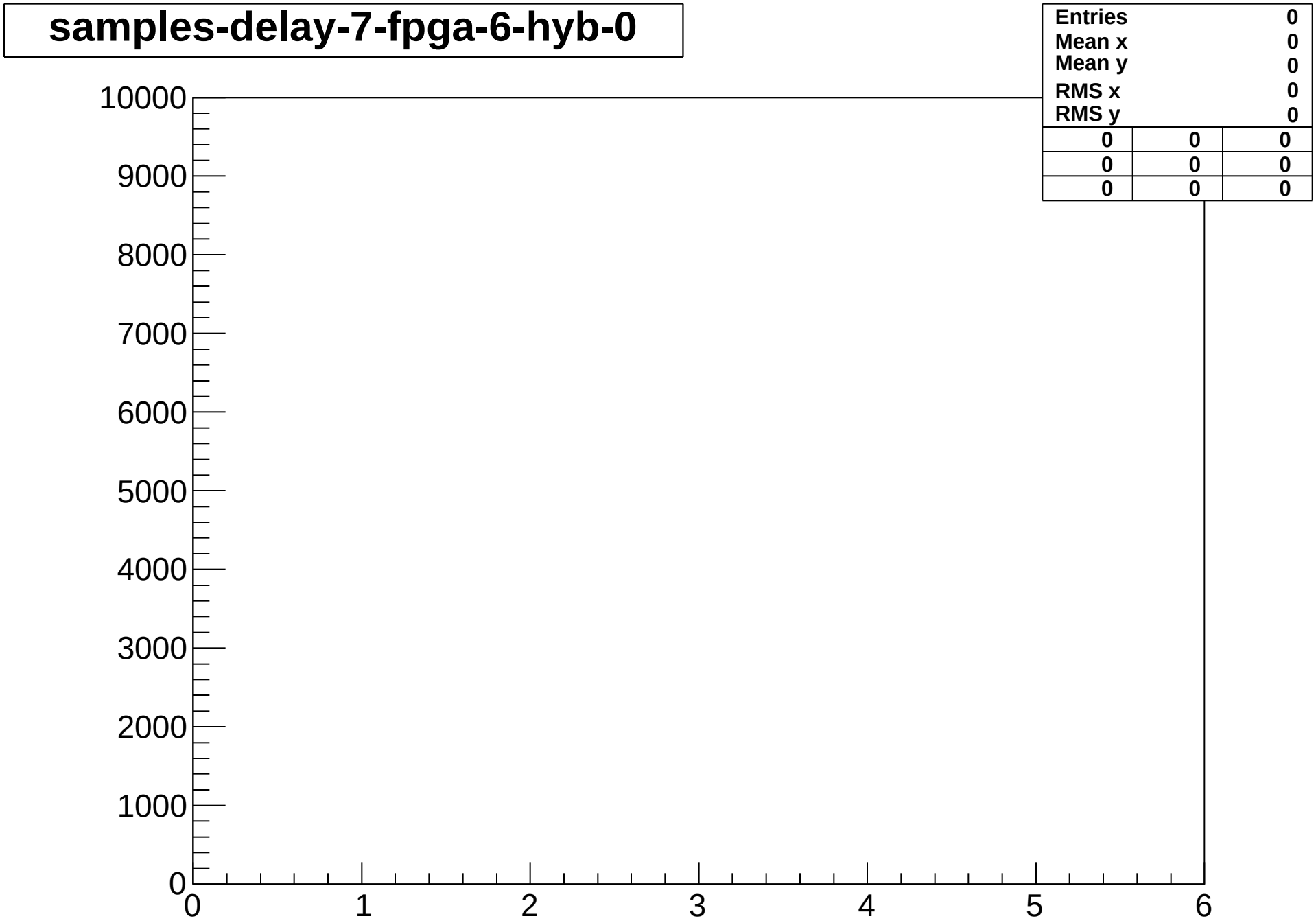
samples-delay-6-fpga-6-hyb-0




samples-delay-7-fpga-6-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
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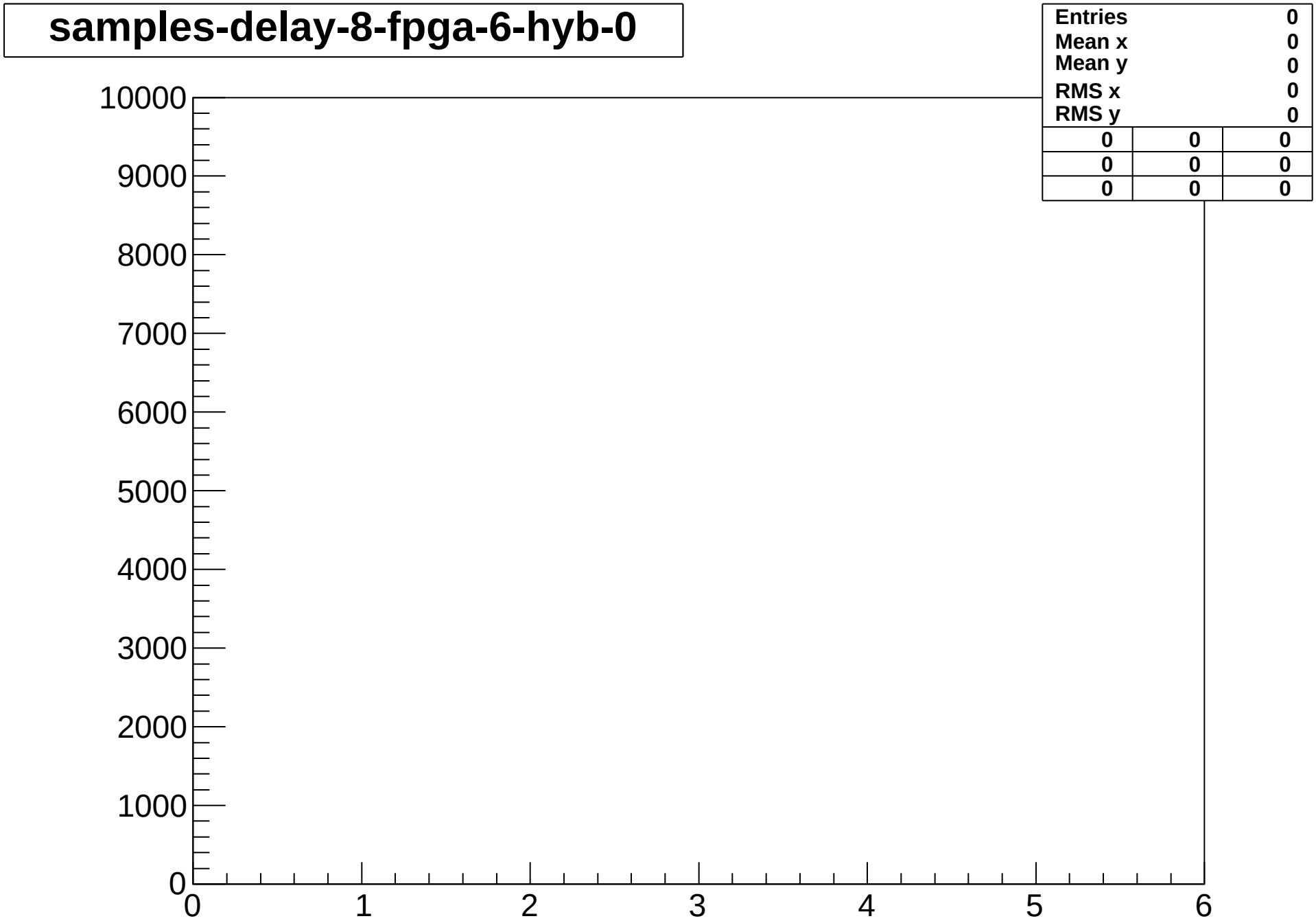
samples-delay-8-fpga-6-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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4
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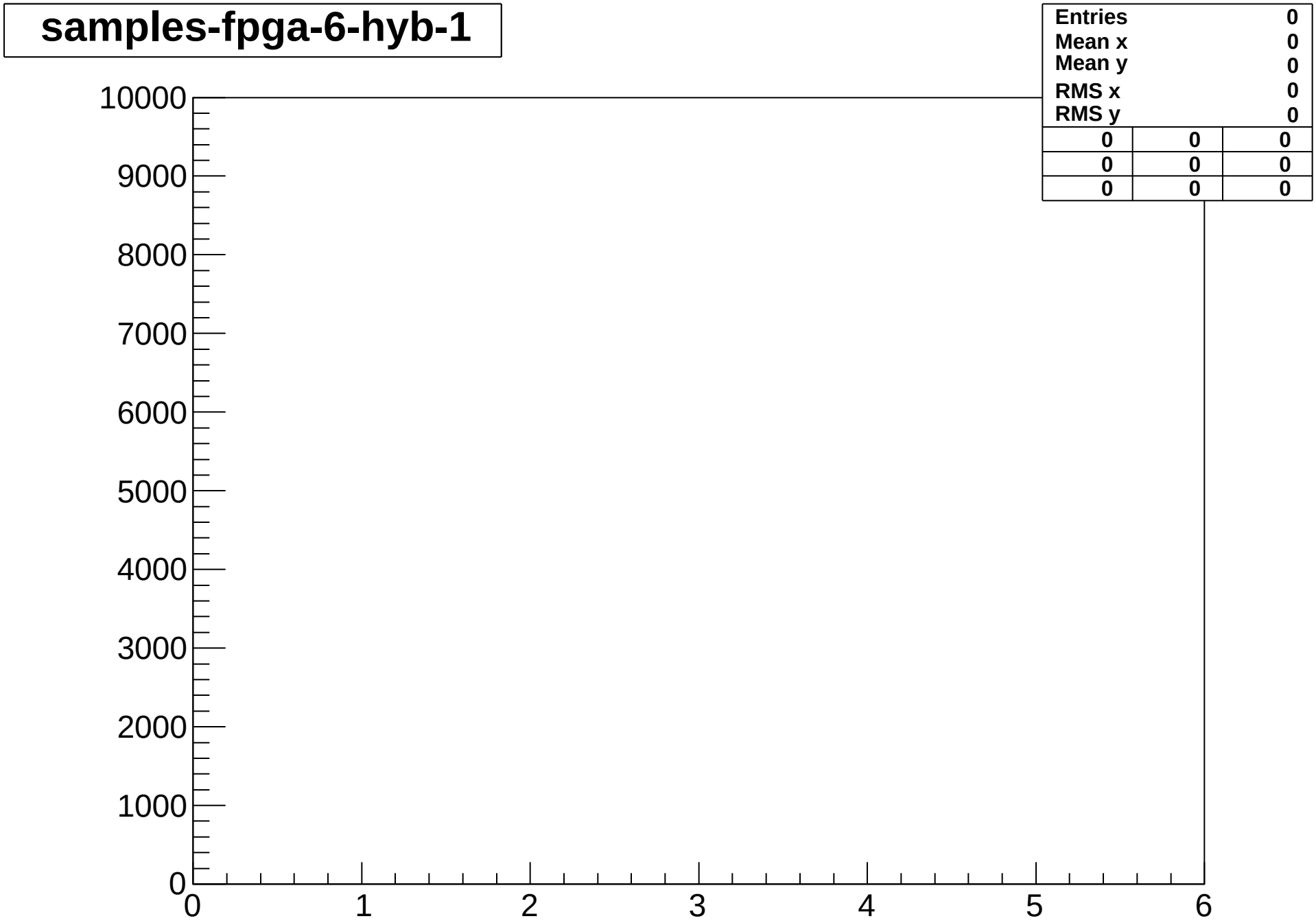
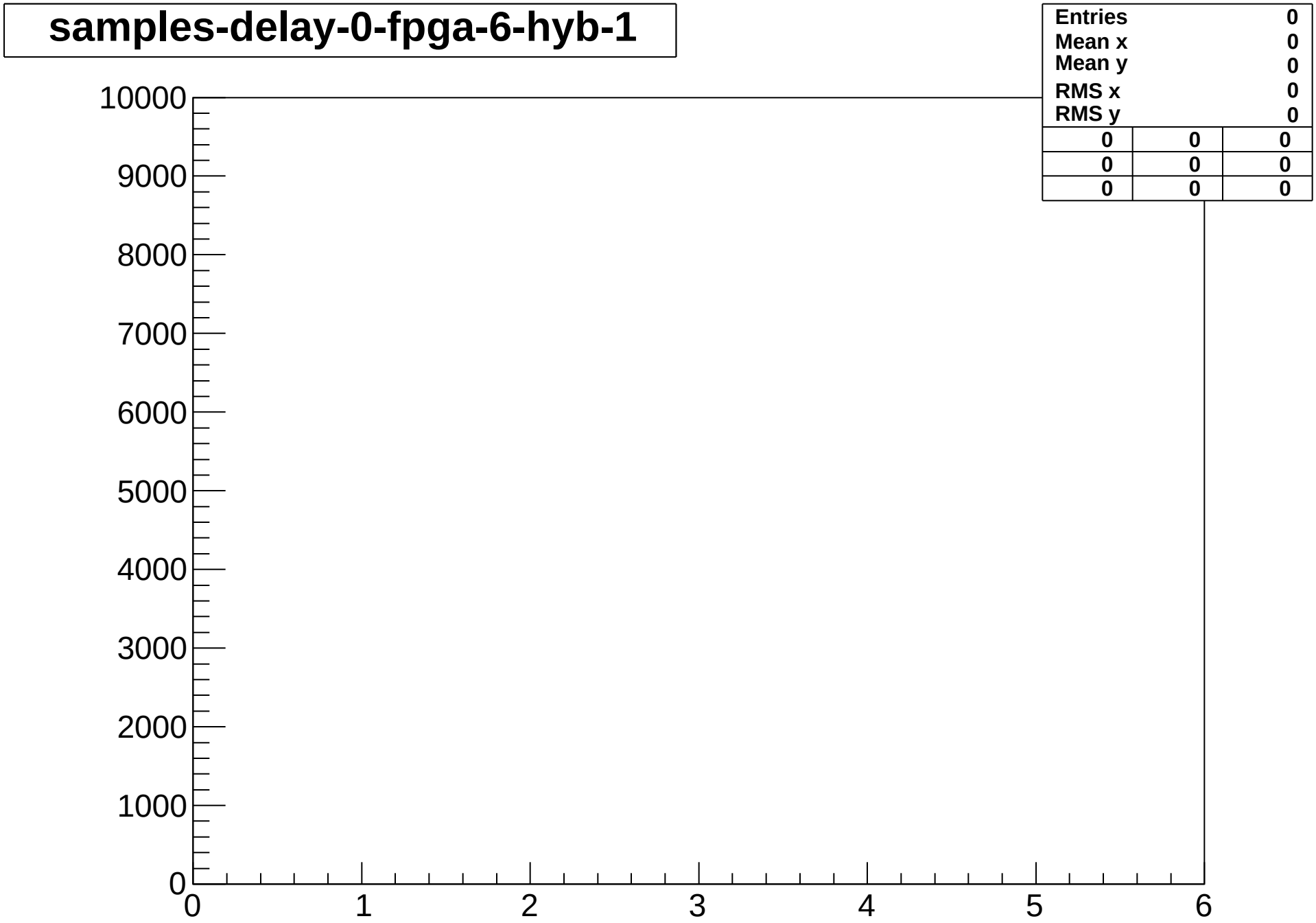
6


samples-fpga-6-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6


samples-delay-0-fpga-6-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
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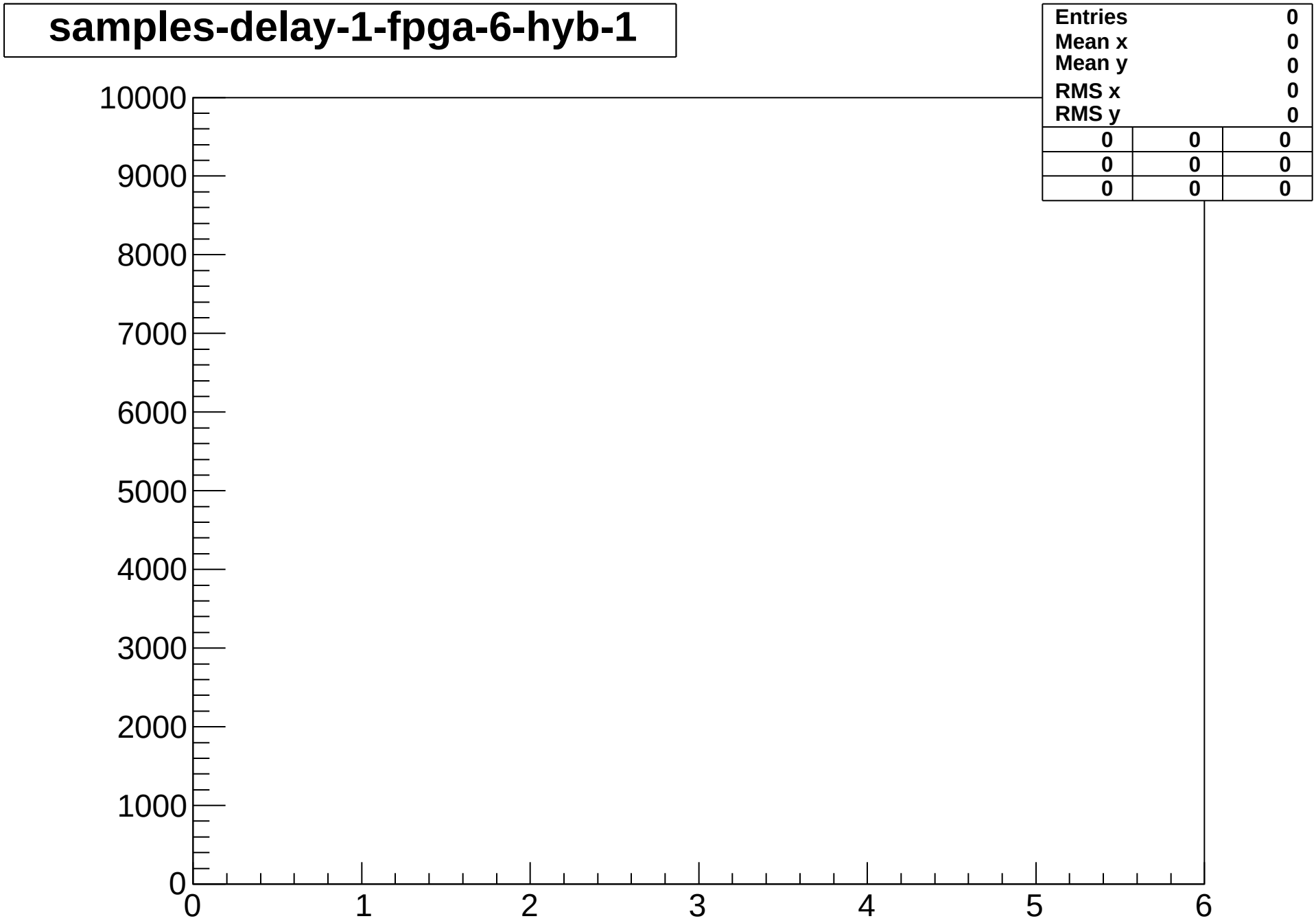
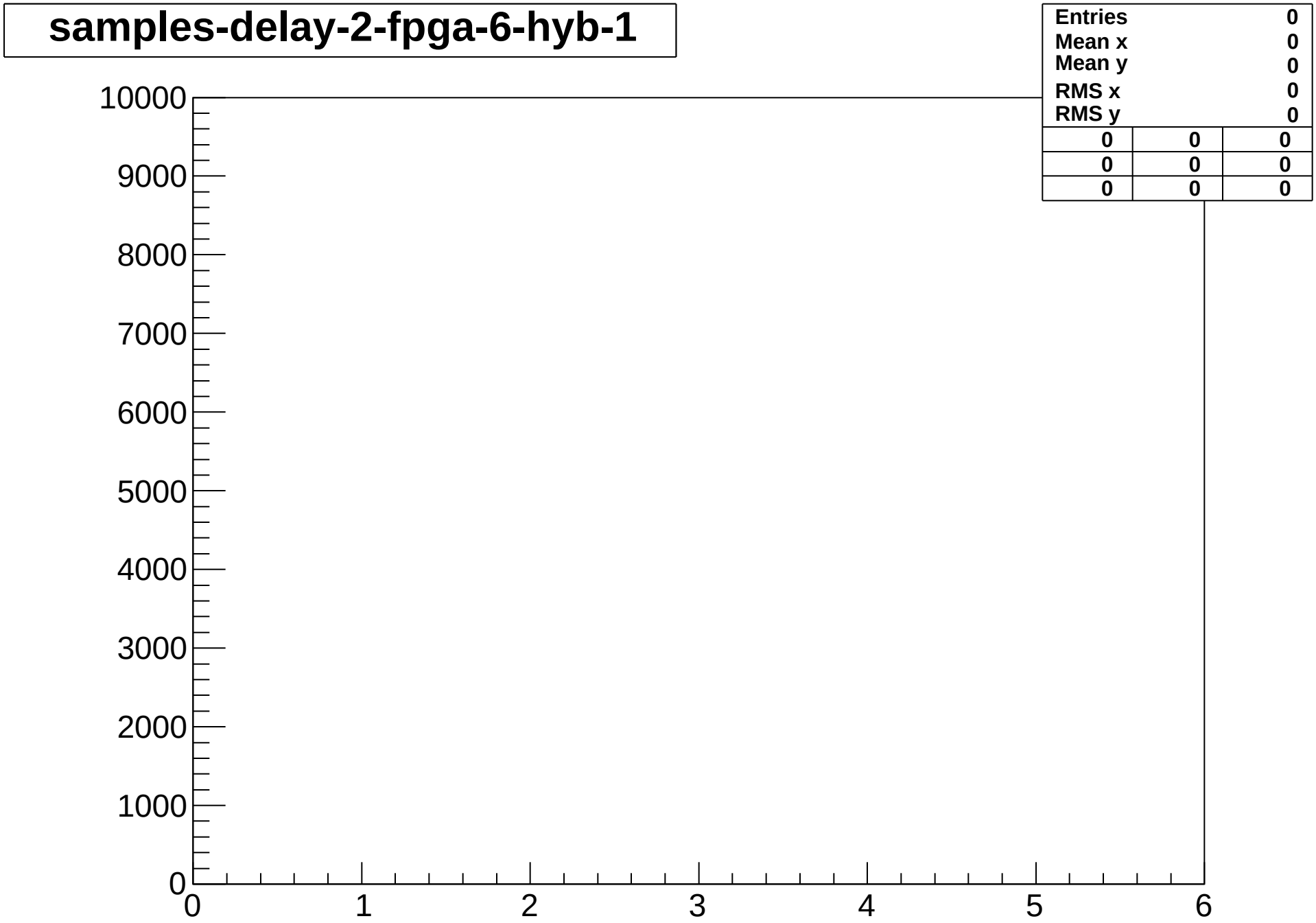
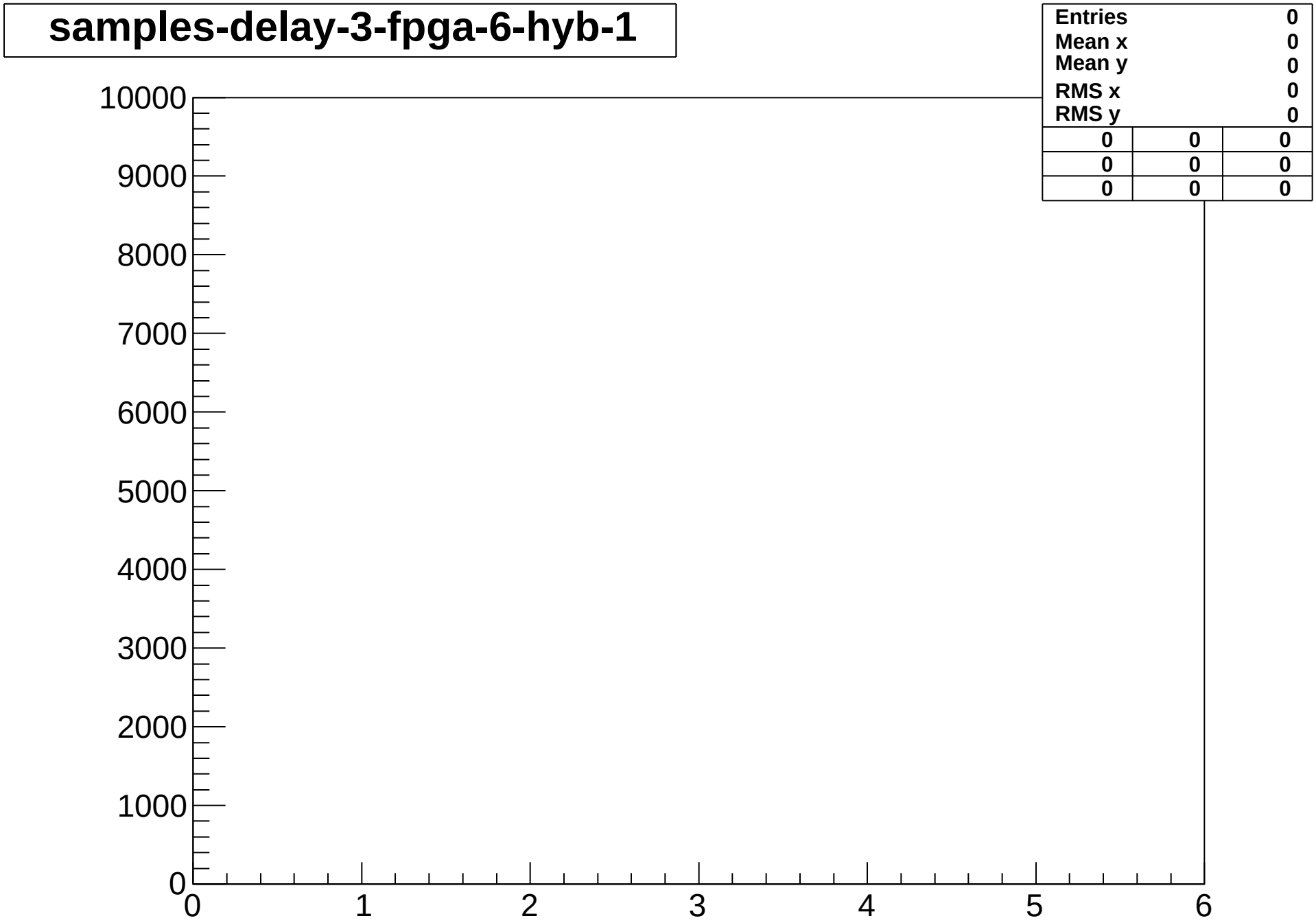
samples-delay-1-fpga-6-hyb-1



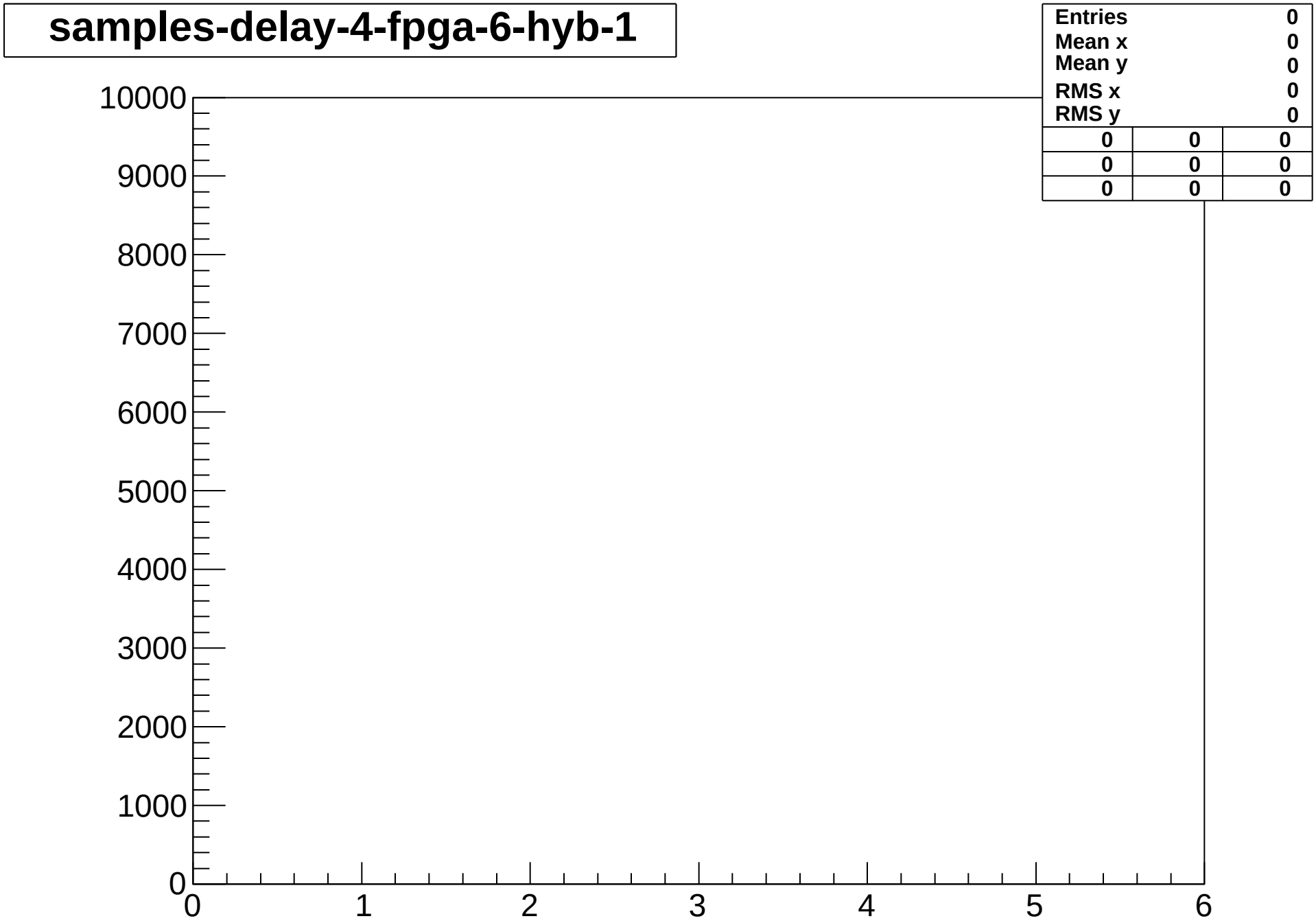
samples-delay-2-fpga-6-hyb-1



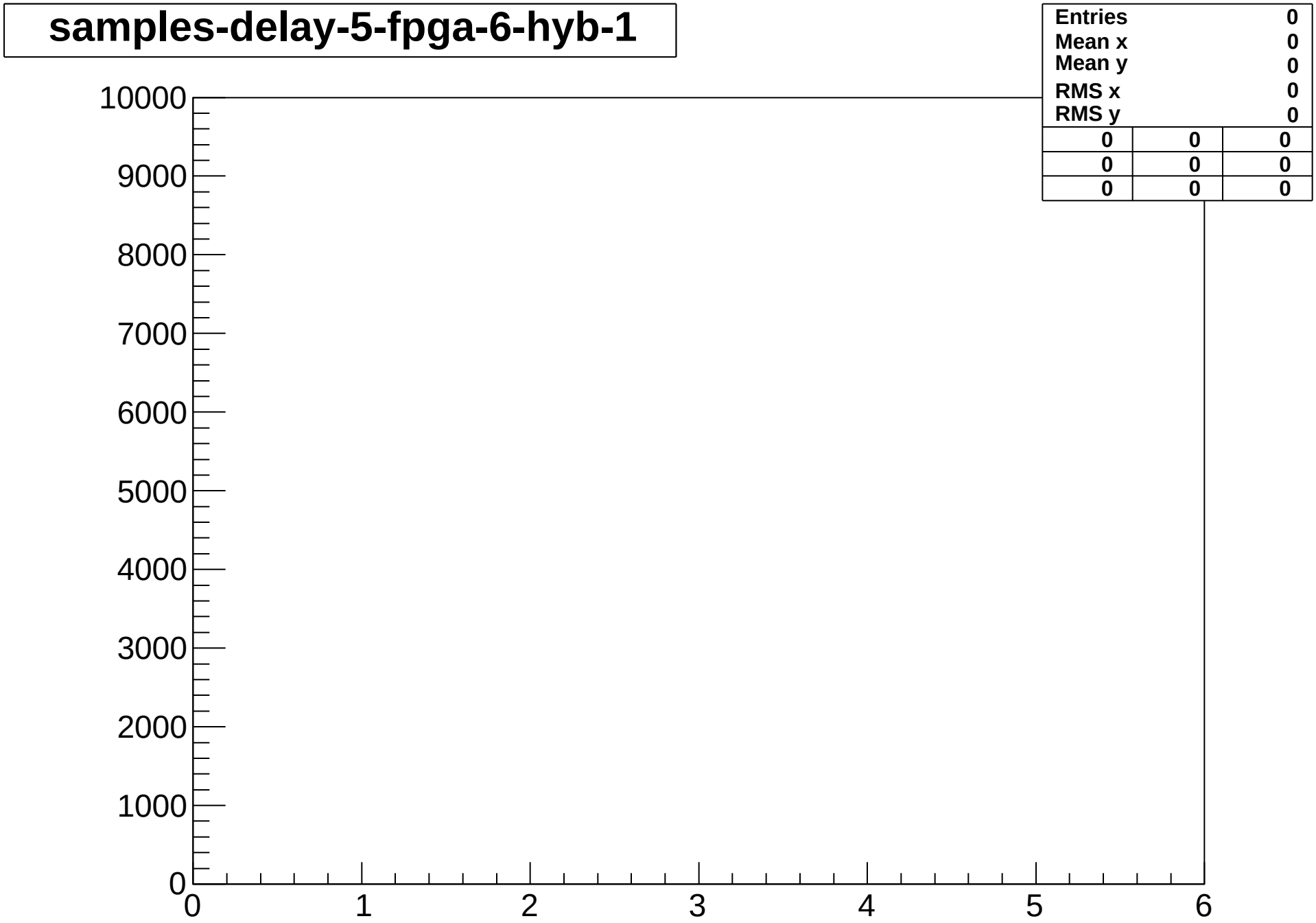
samples-delay-3-fpga-6-hyb-1

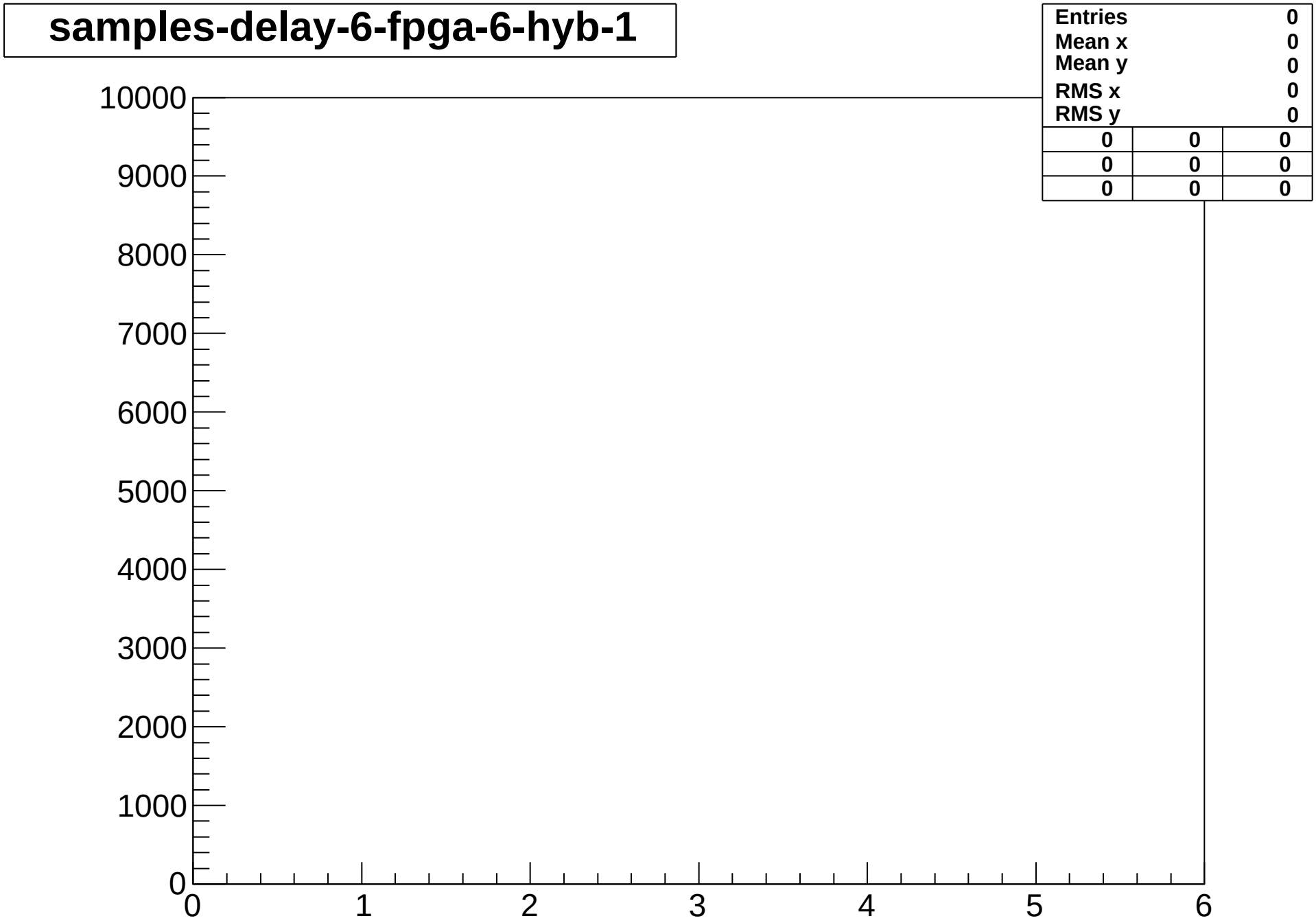


samples-delay-4-fpga-6-hyb-1



samples-delay-5-fpga-6-hyb-1




samples-delay-6-fpga-6-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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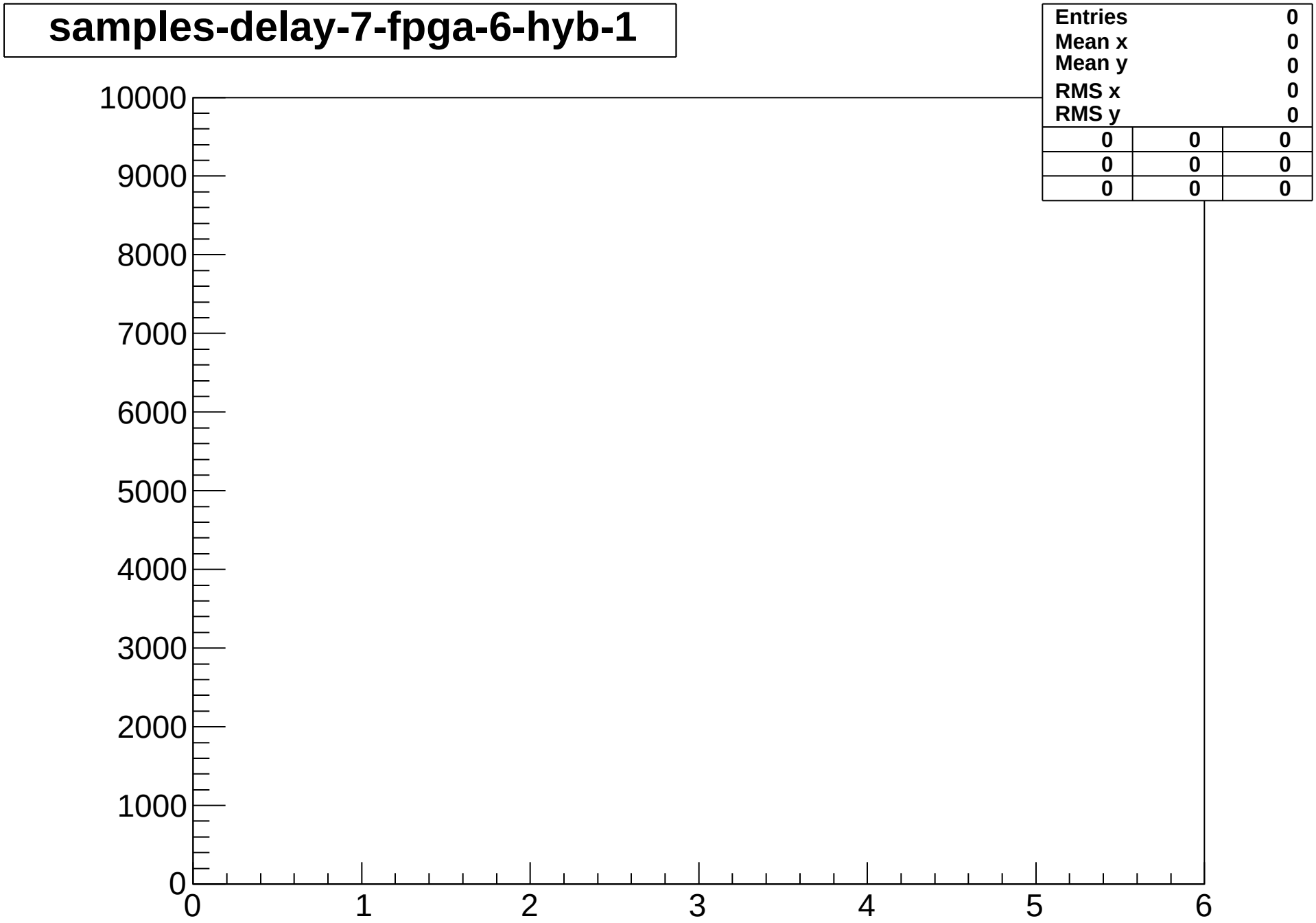
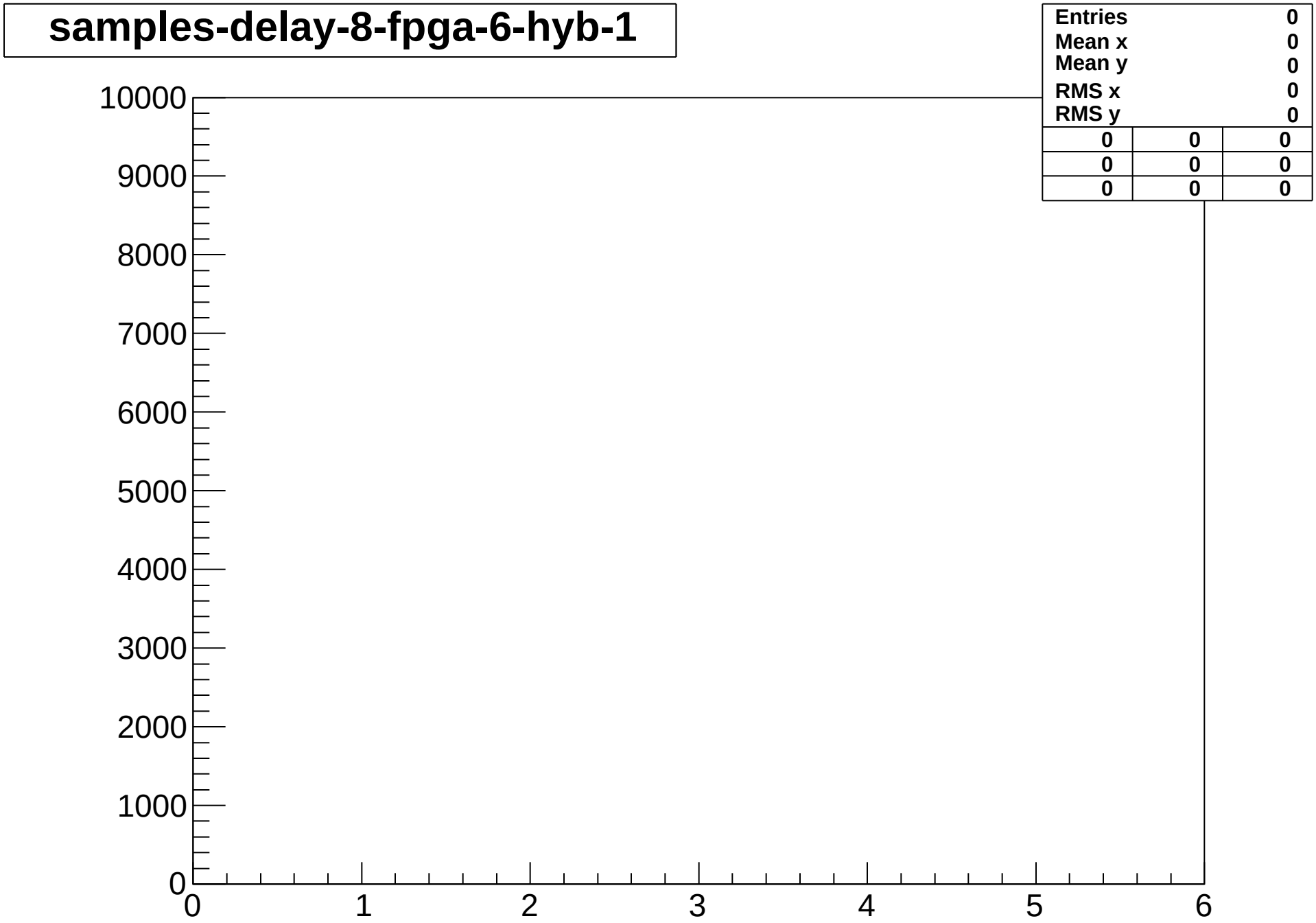
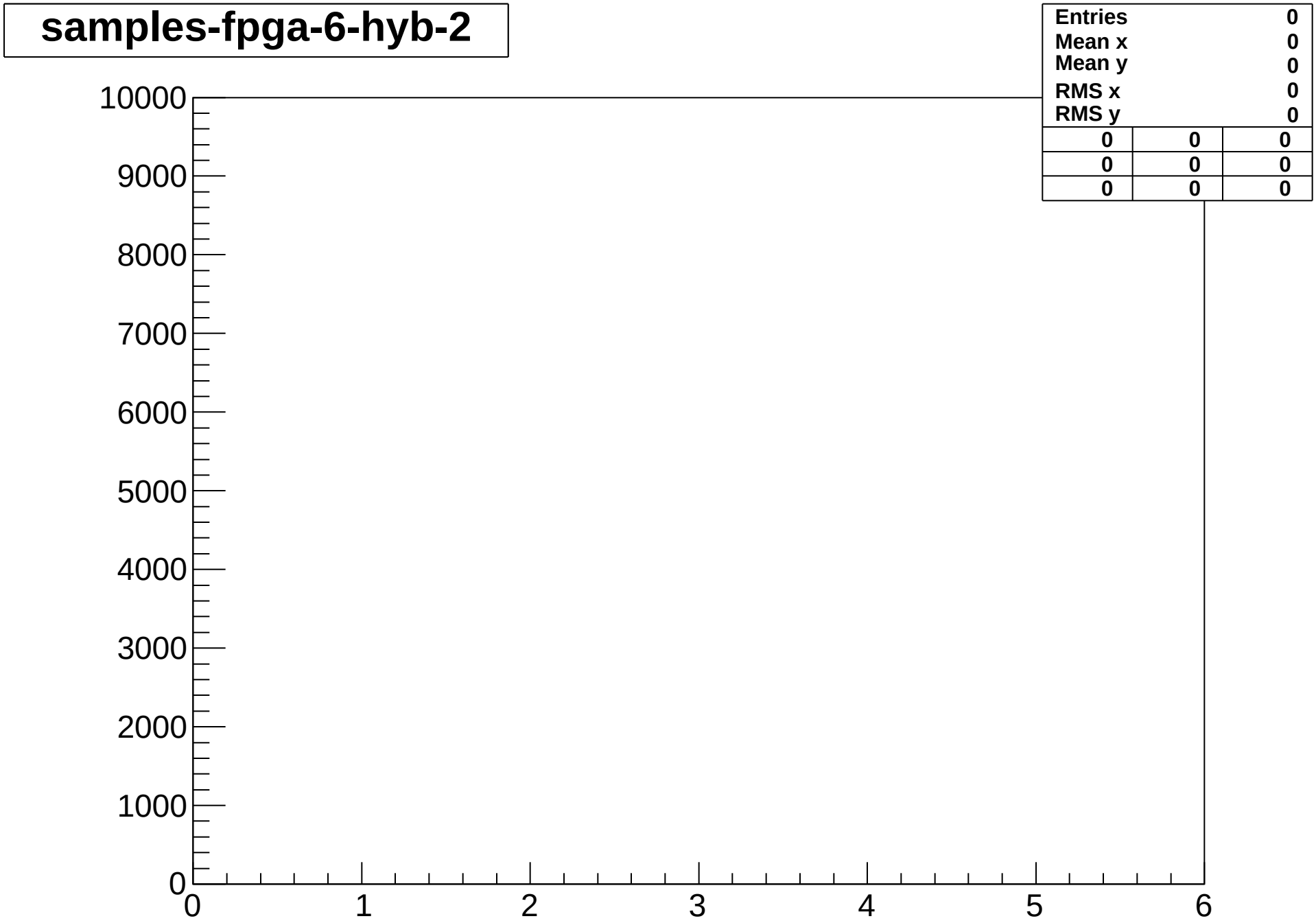
samples-delay-7-fpga-6-hyb-1



samples-delay-8-fpga-6-hyb-1




samples-fpga-6-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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6000
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4000
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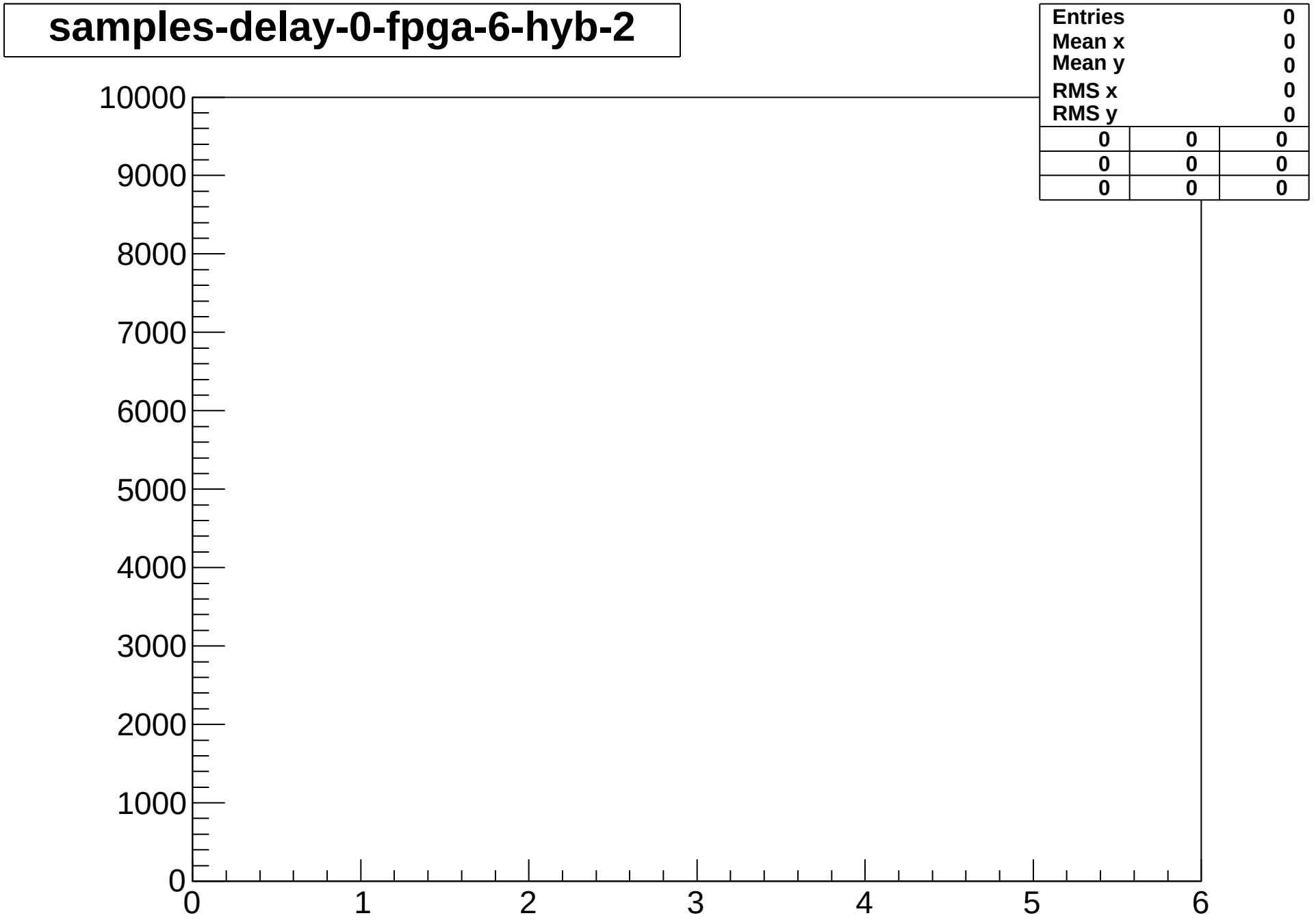
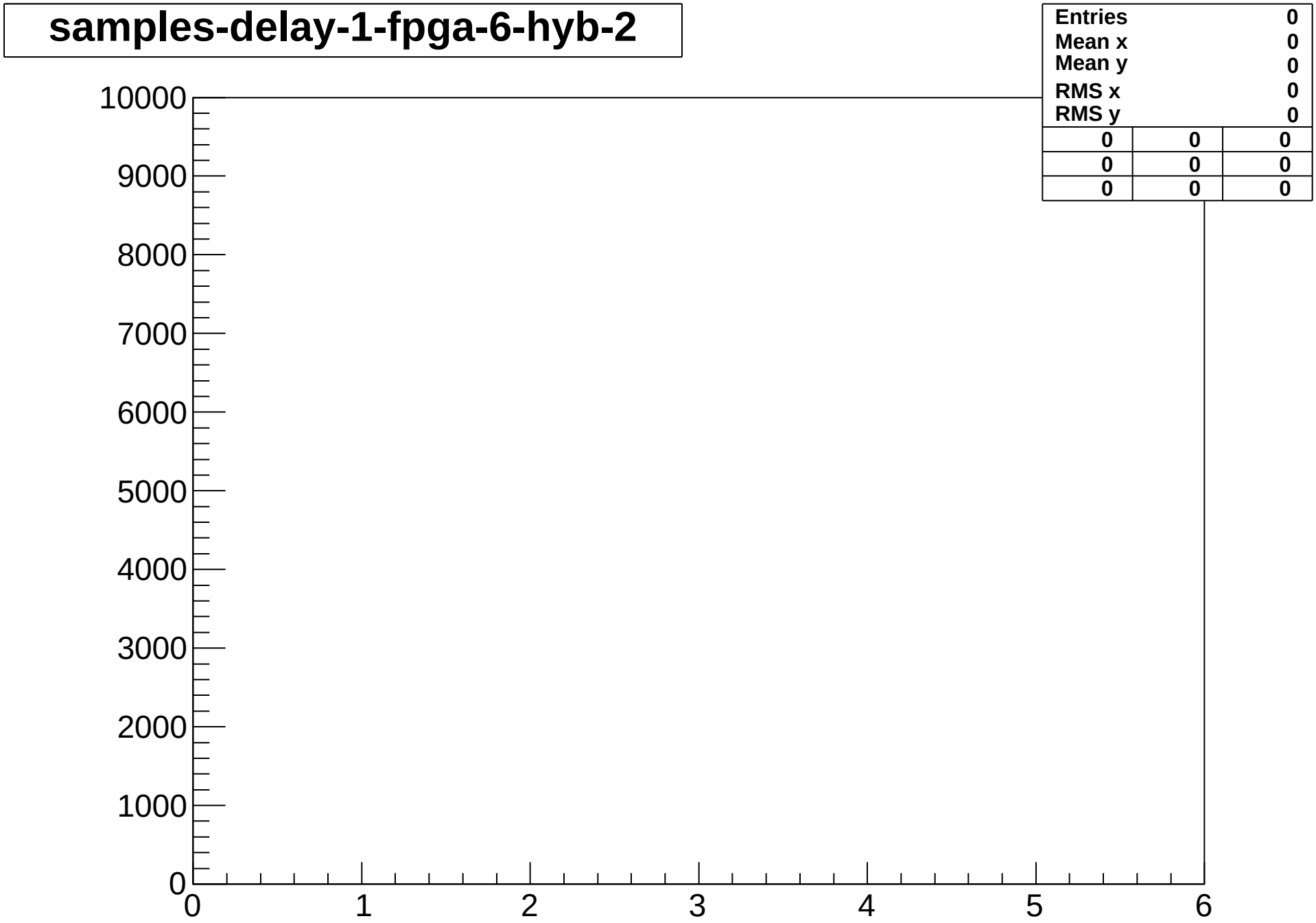
samples-delay-0-fpga-6-hyb-2




samples-delay-1-fpga-6-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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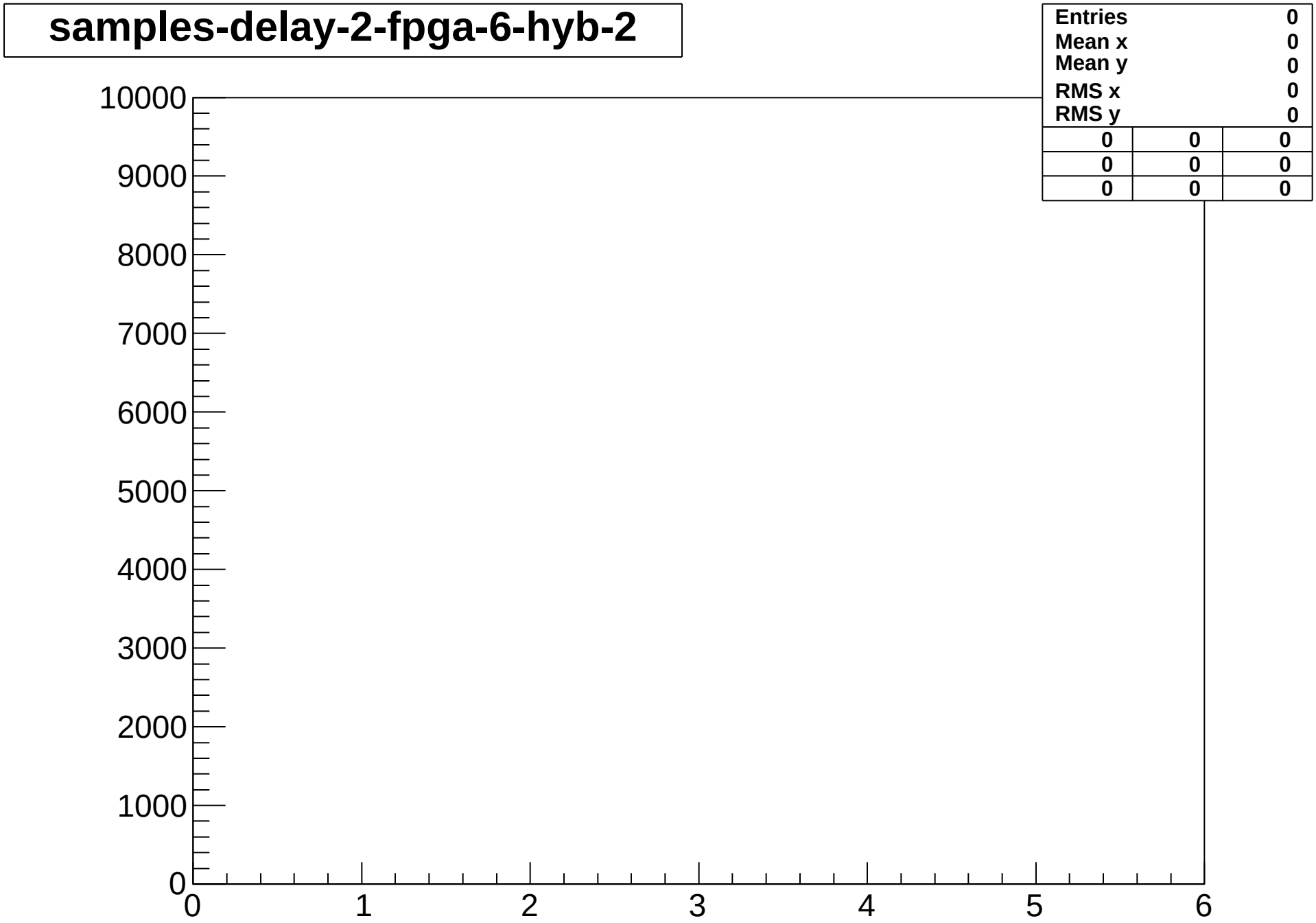
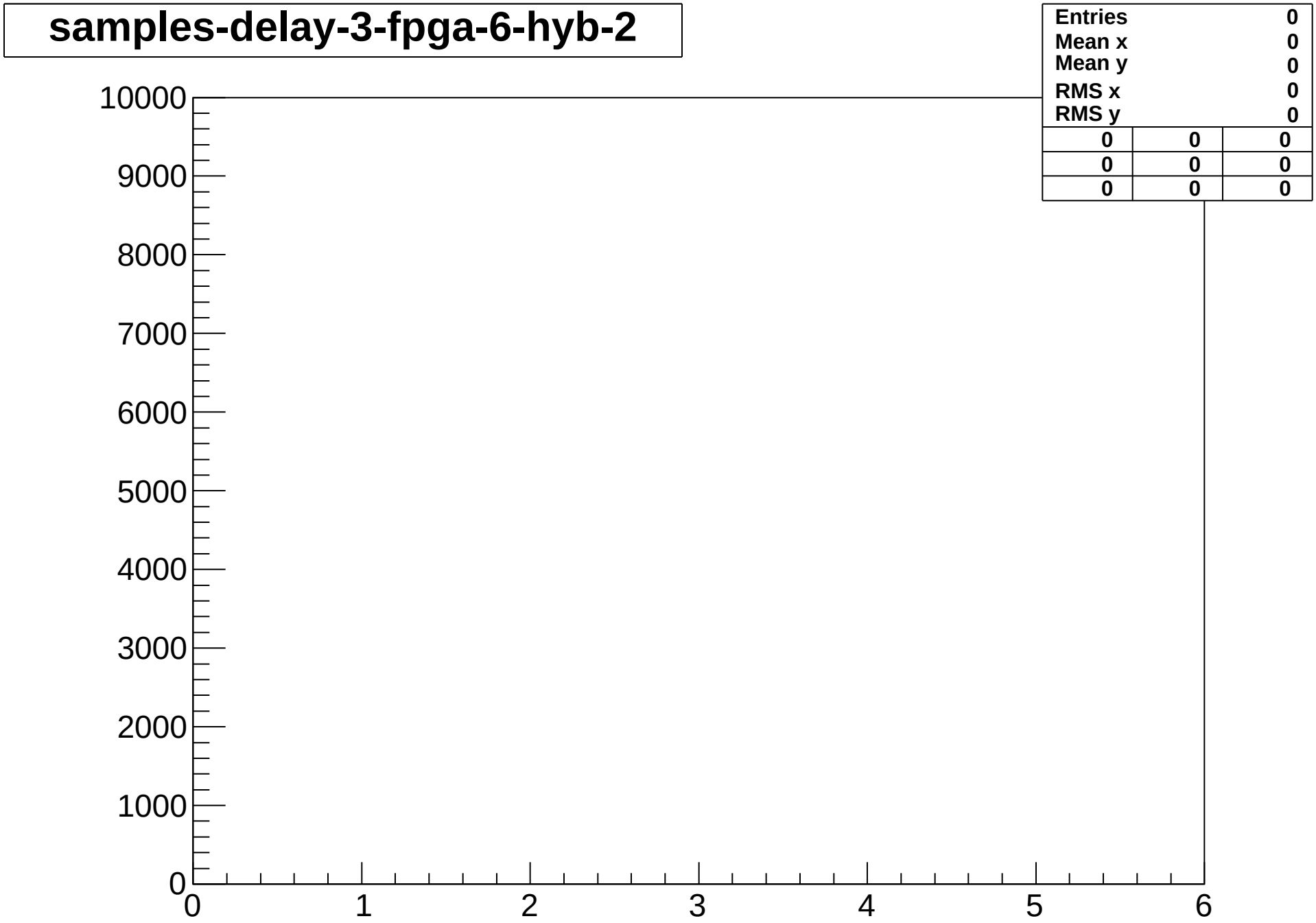
samples-delay-2-fpga-6-hyb-2




samples-delay-3-fpga-6-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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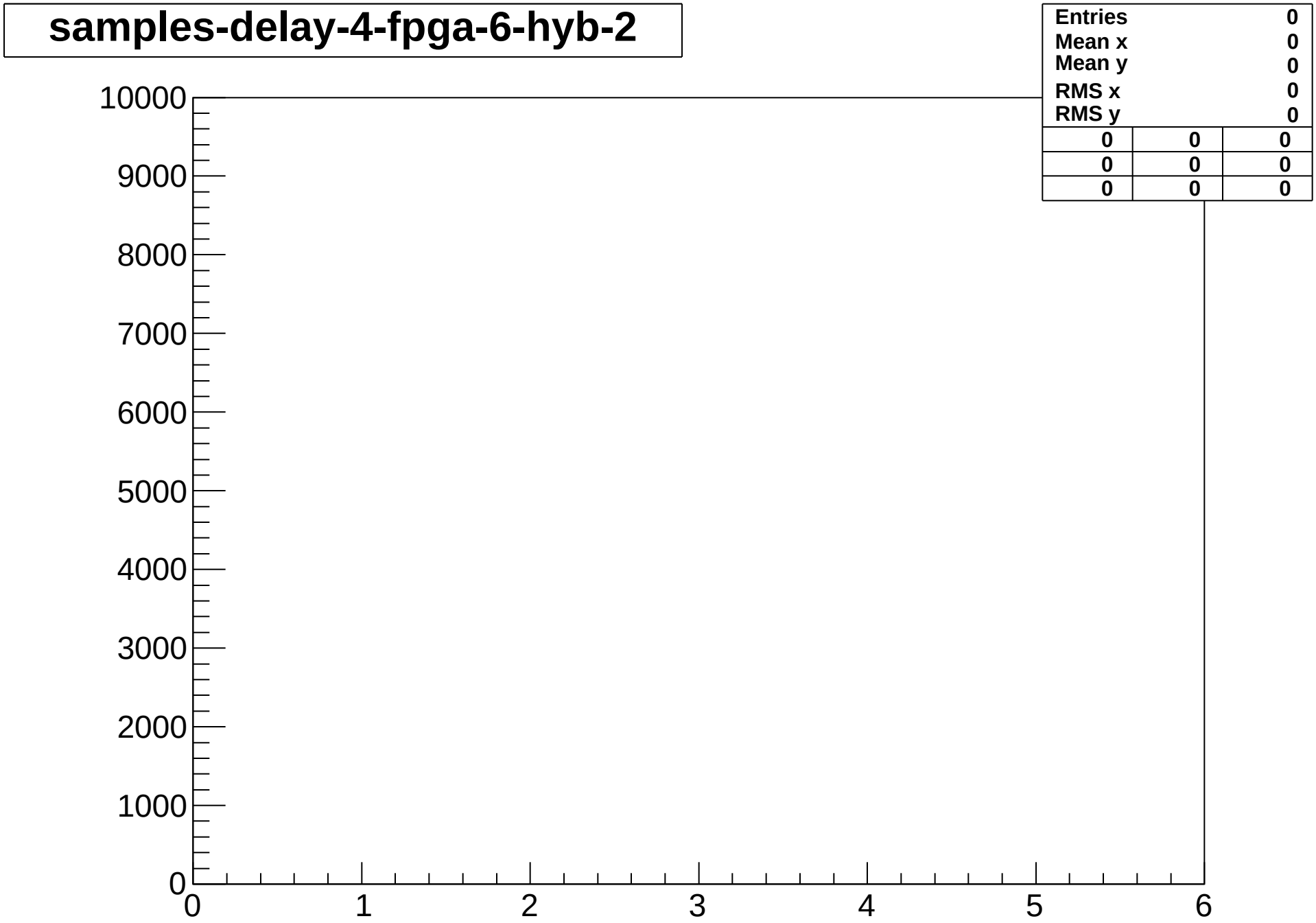
samples-delay-4-fpga-6-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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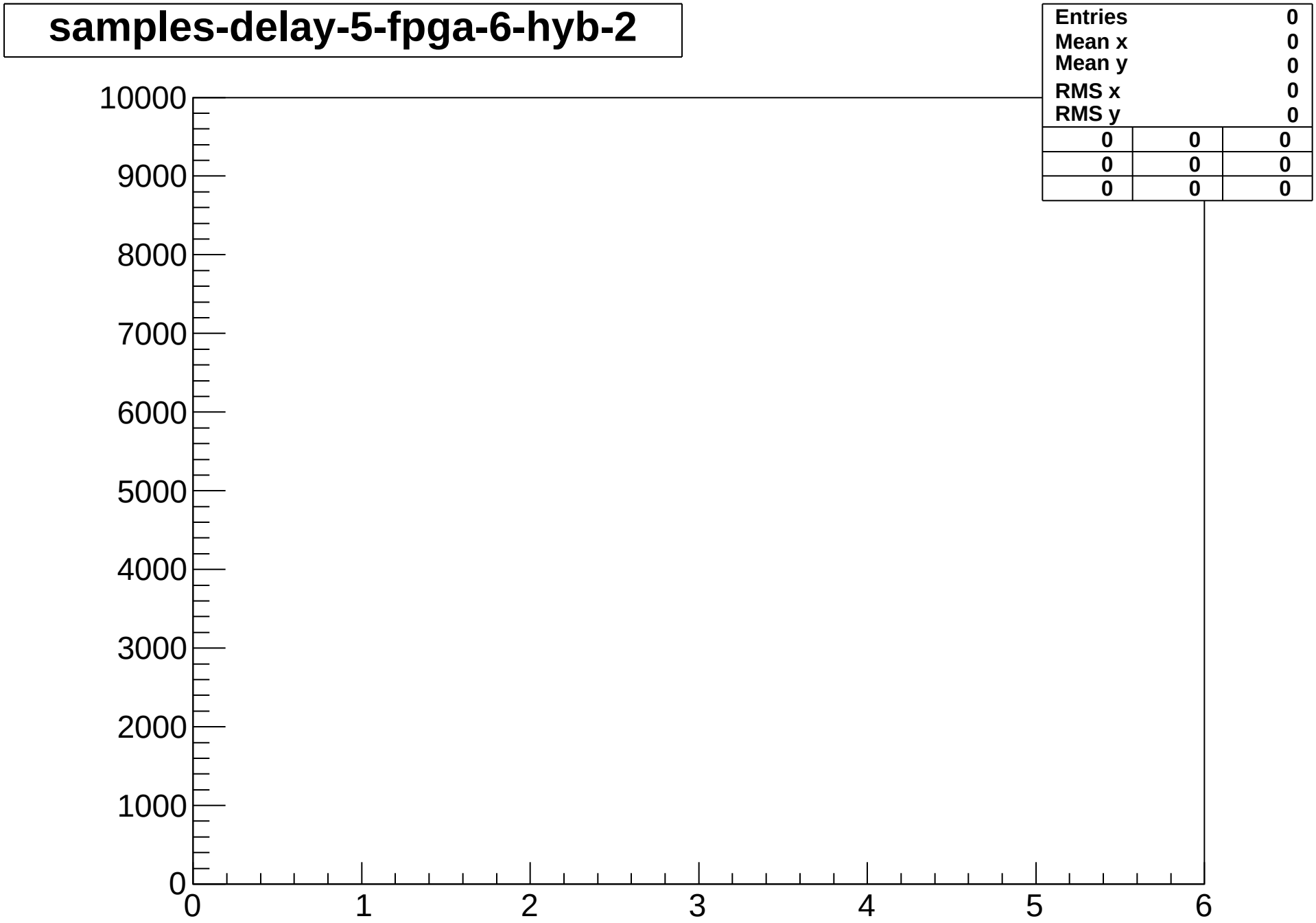
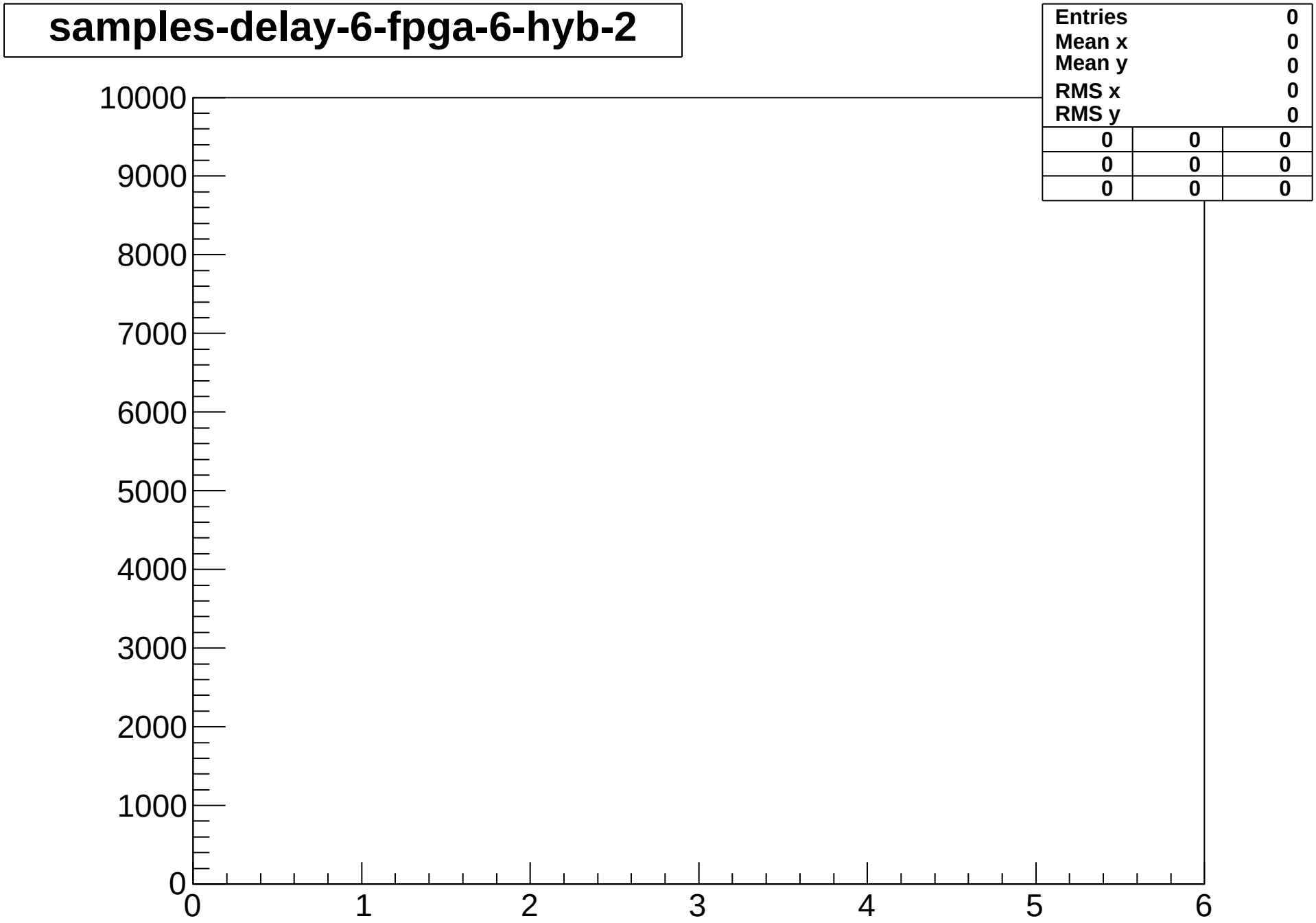
samples-delay-5-fpga-6-hyb-2




samples-delay-6-fpga-6-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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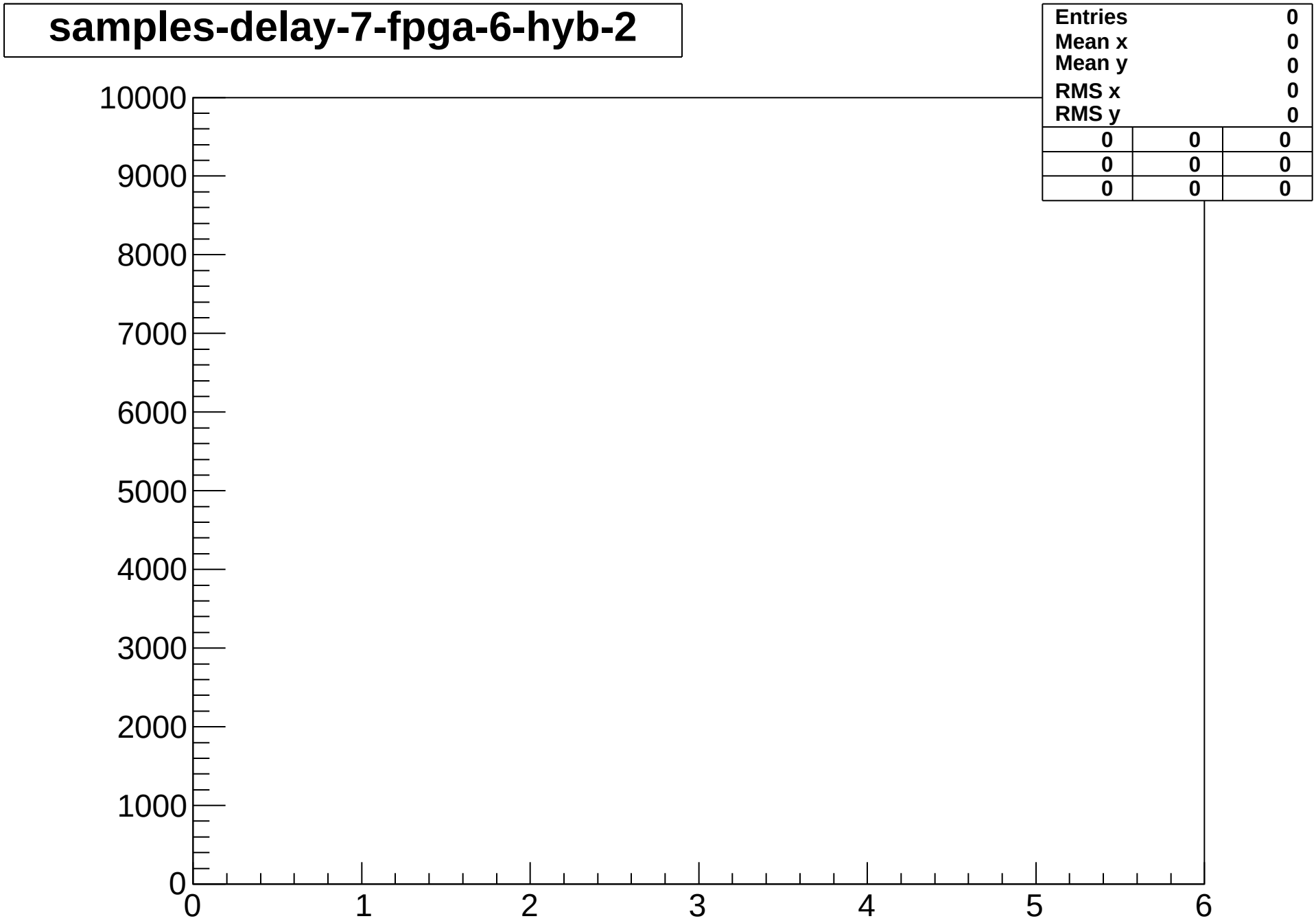
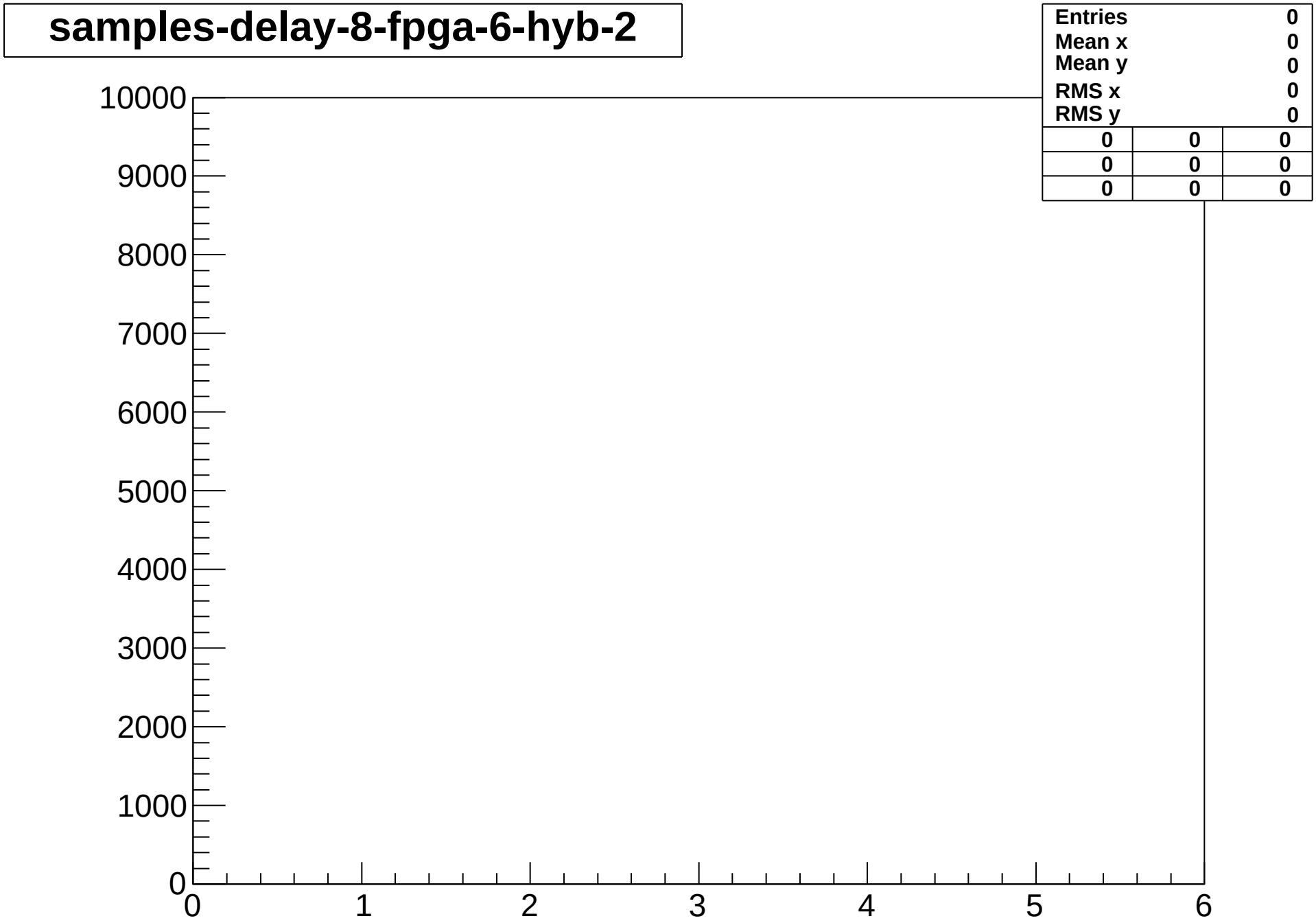
samples-delay-7-fpga-6-hyb-2




samples-delay-8-fpga-6-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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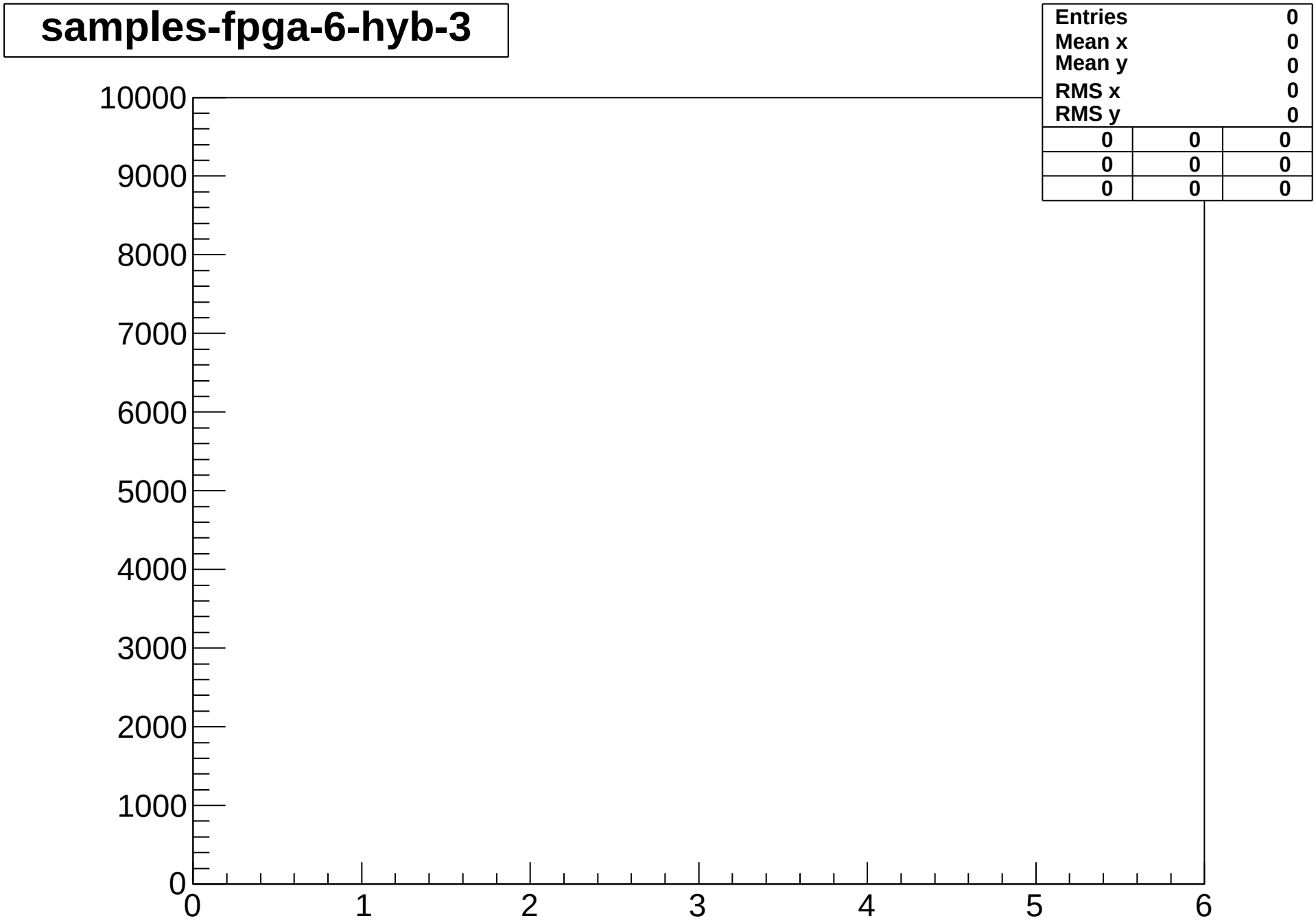
samples-fpga-6-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
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0
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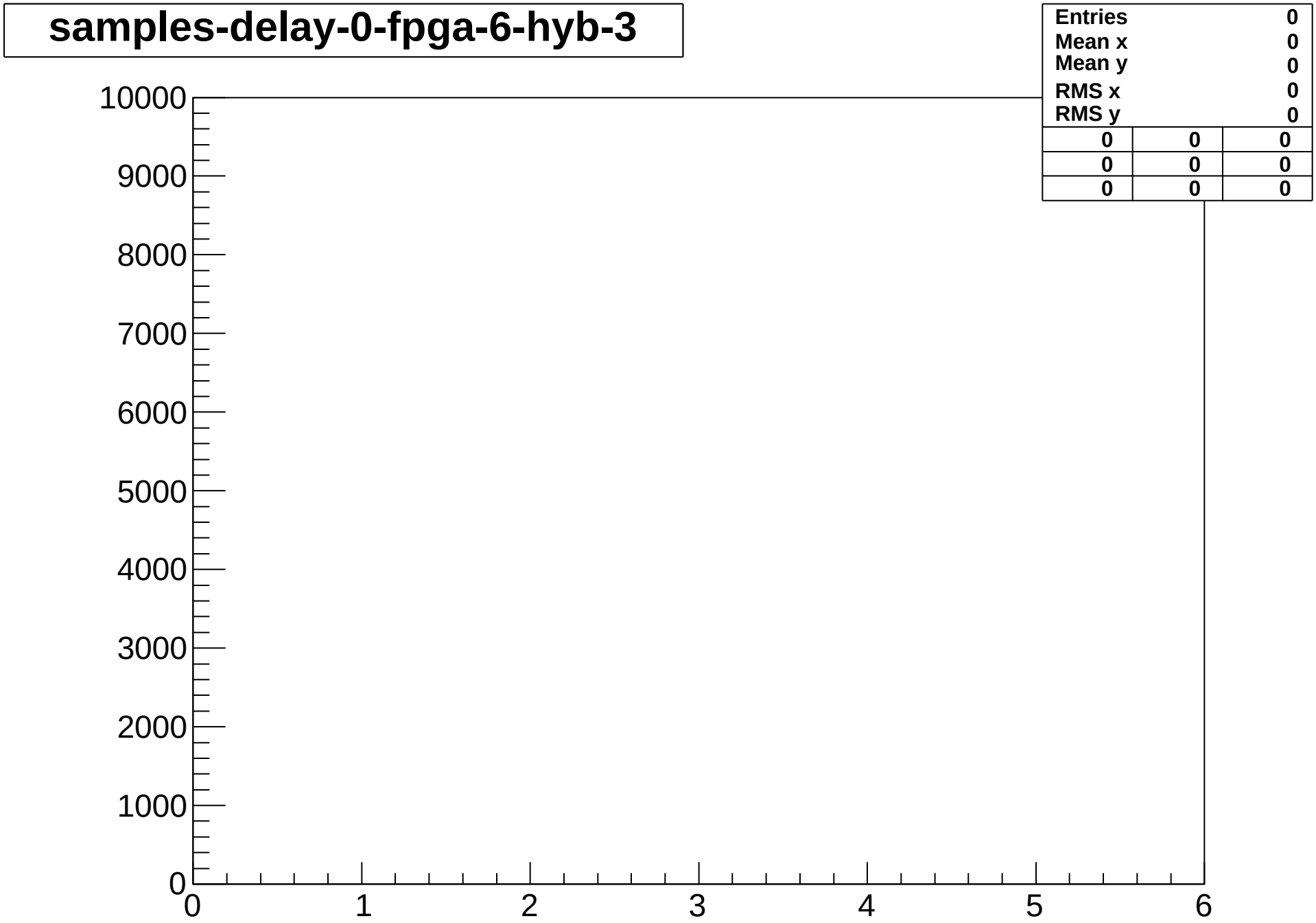
samples-delay-0-fpga-6-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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6000
5000
4000
3000
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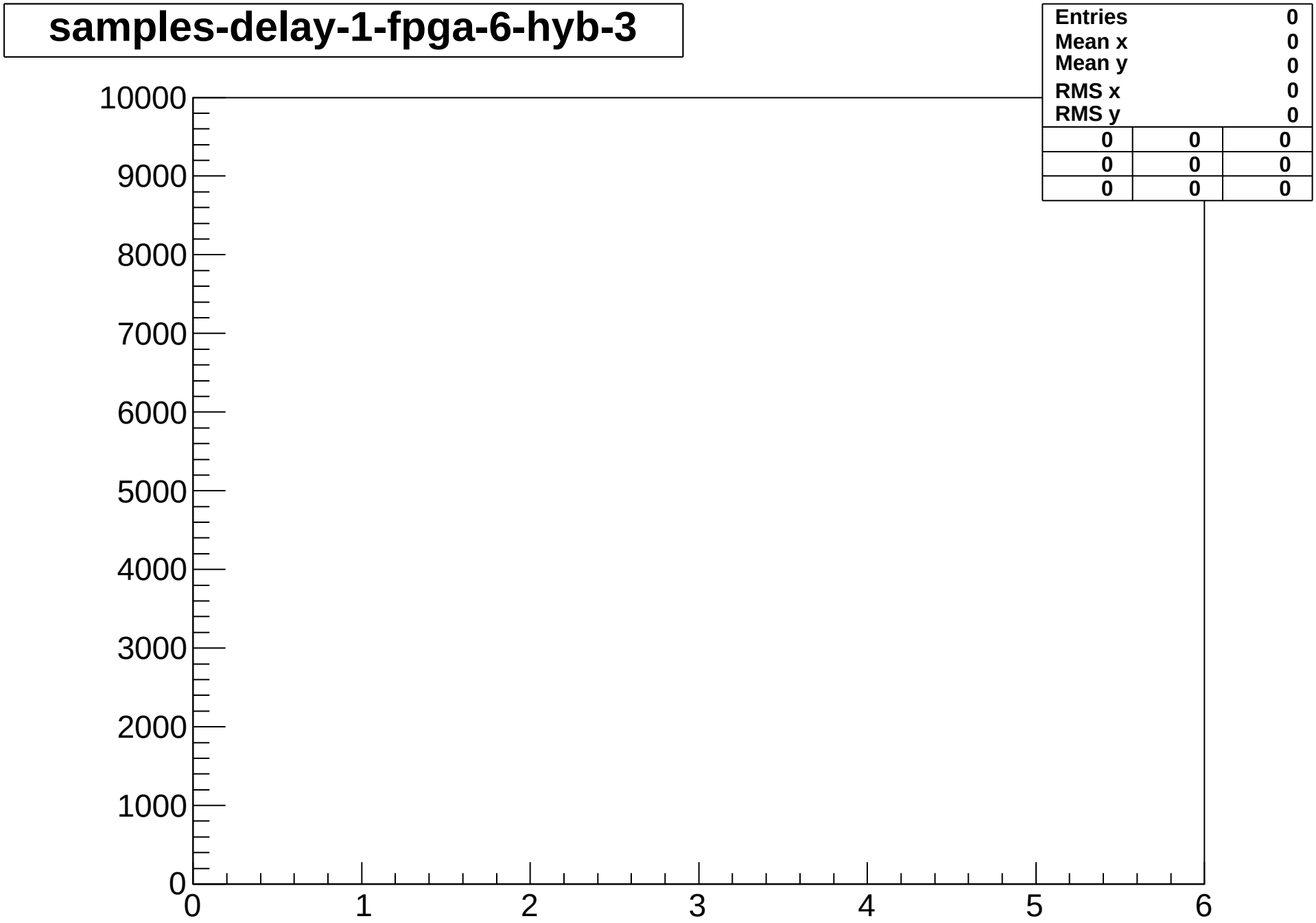
samples-delay-1-fpga-6-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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6000
5000
4000
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1
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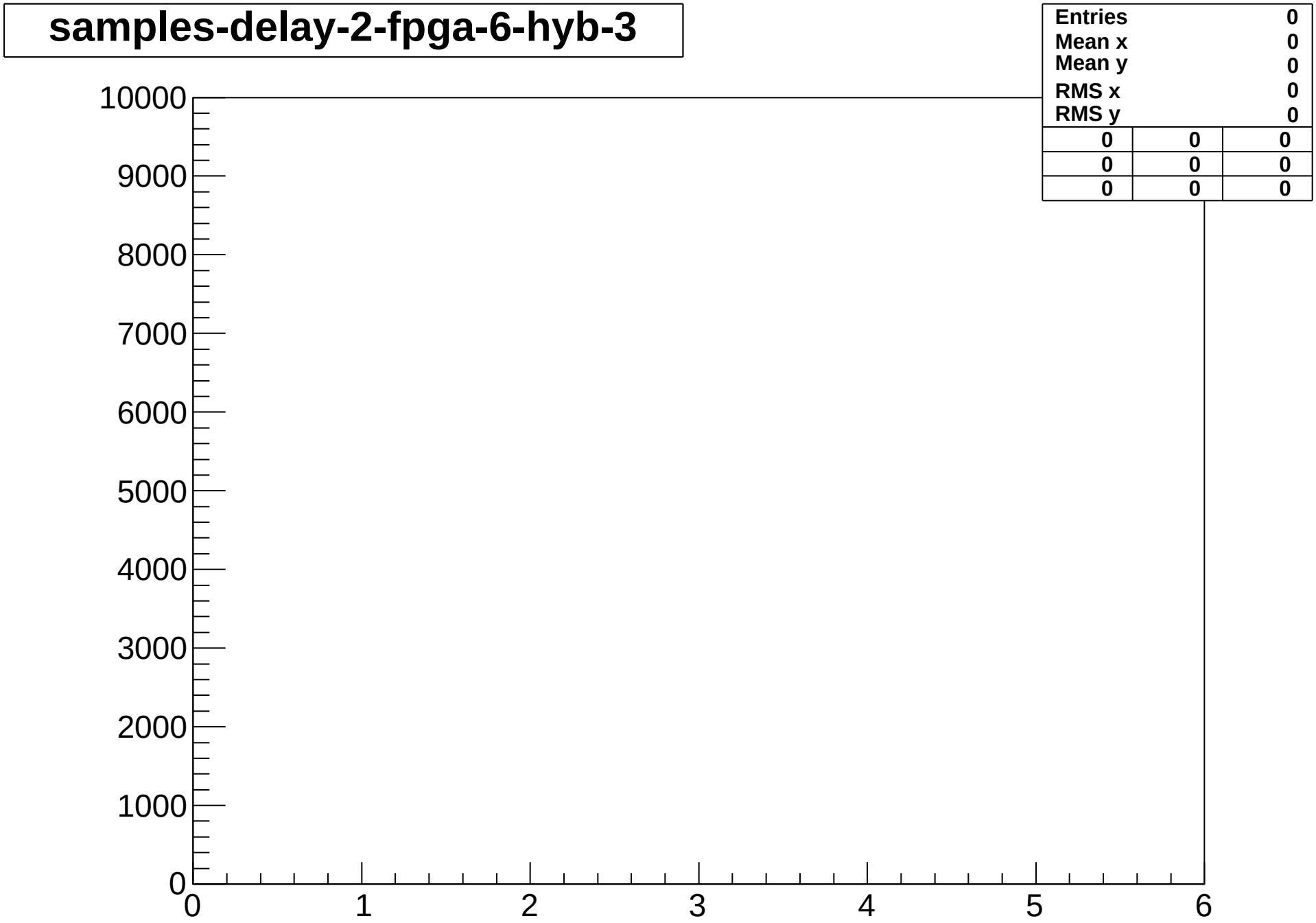
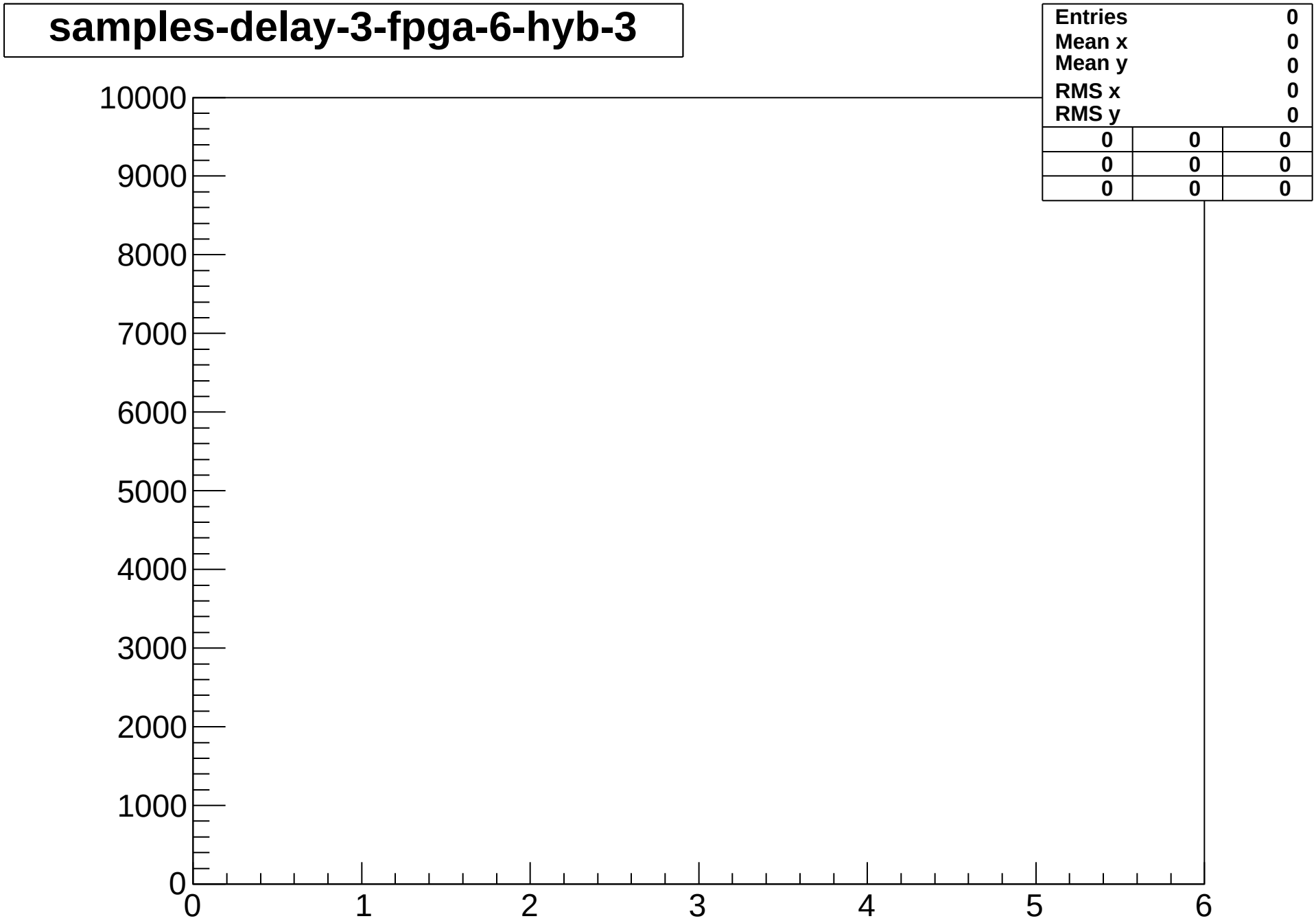
samples-delay-2-fpga-6-hyb-3




samples-delay-3-fpga-6-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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6000
5000
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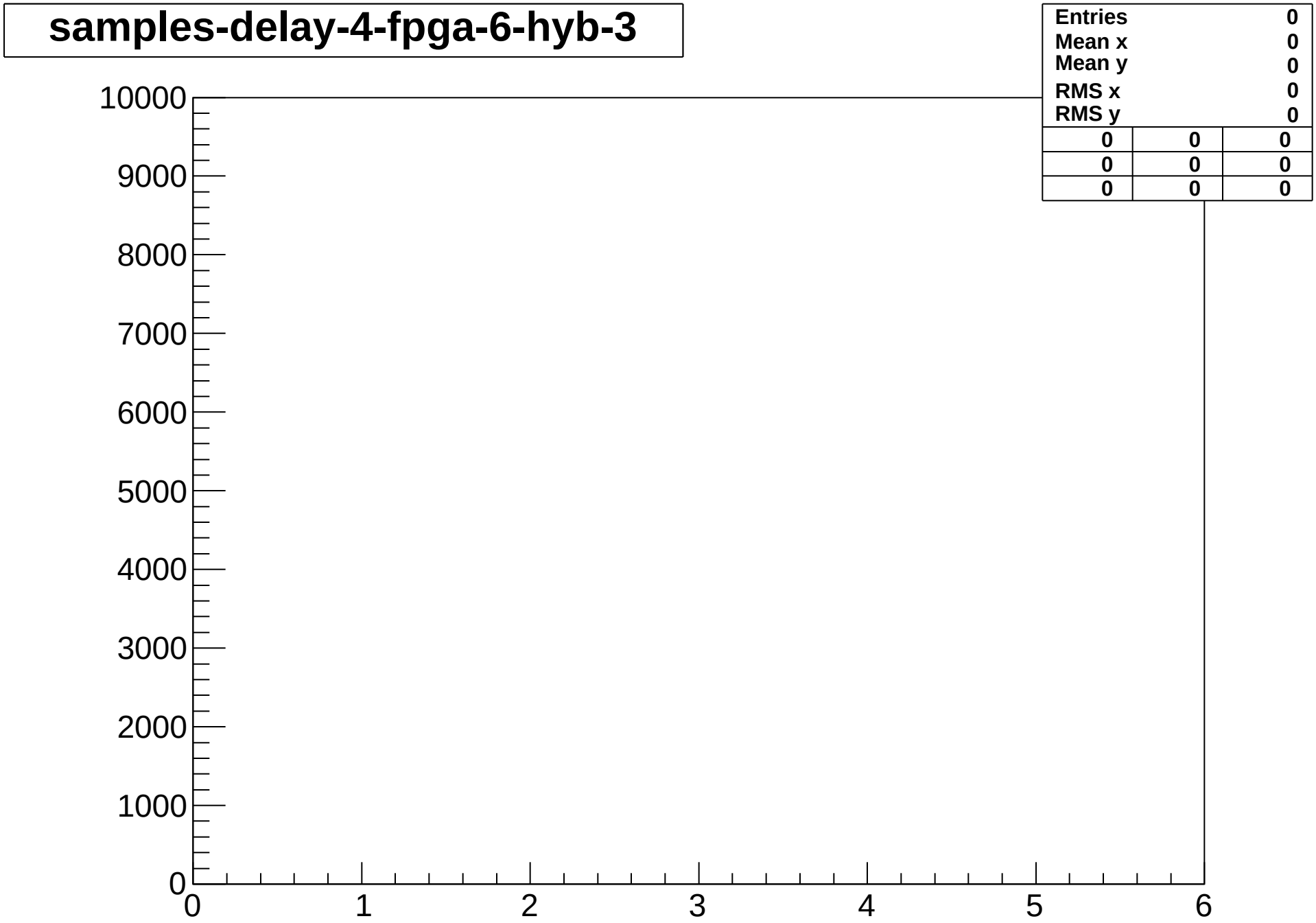
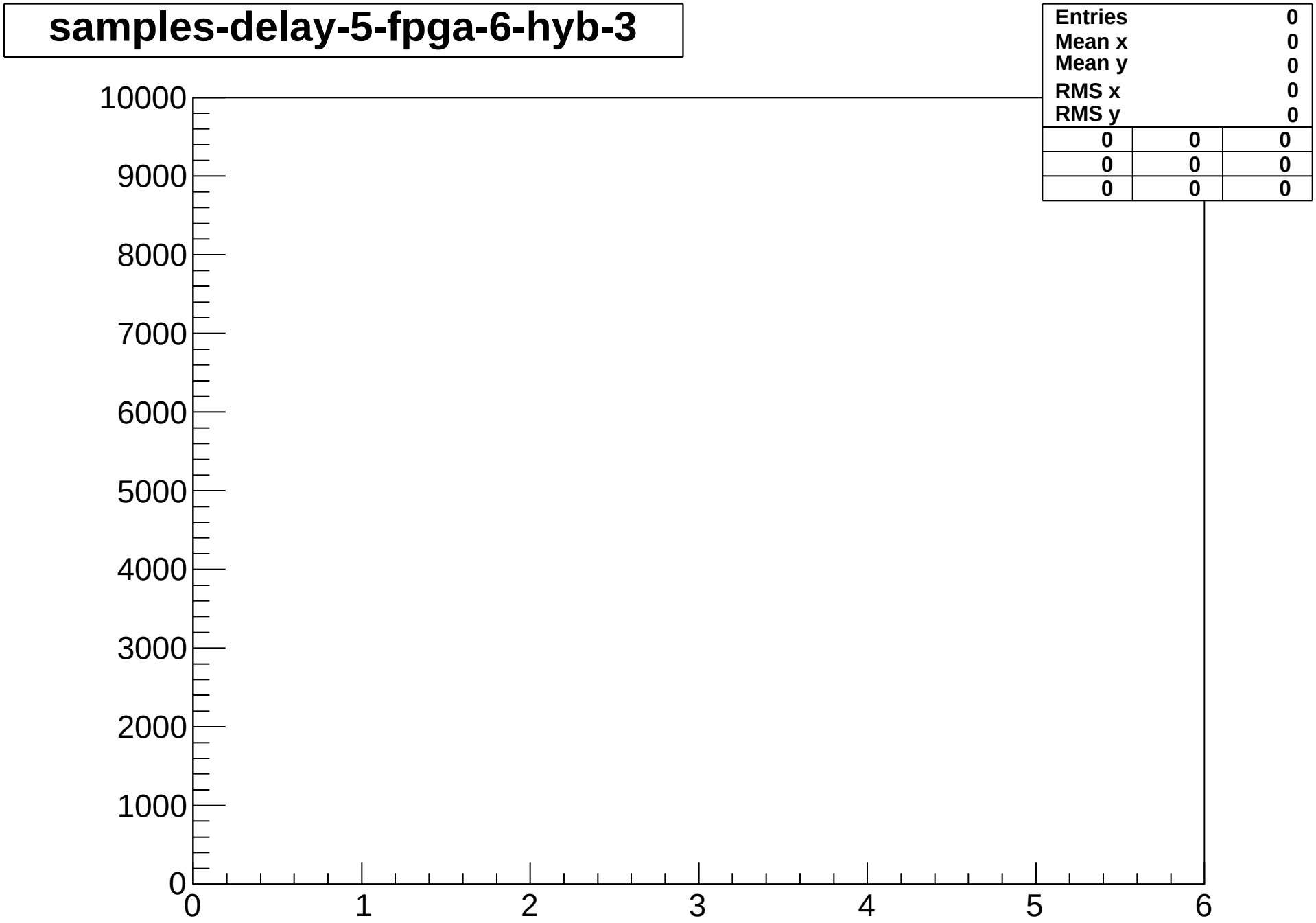
samples-delay-4-fpga-6-hyb-3




samples-delay-5-fpga-6-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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7000
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3000
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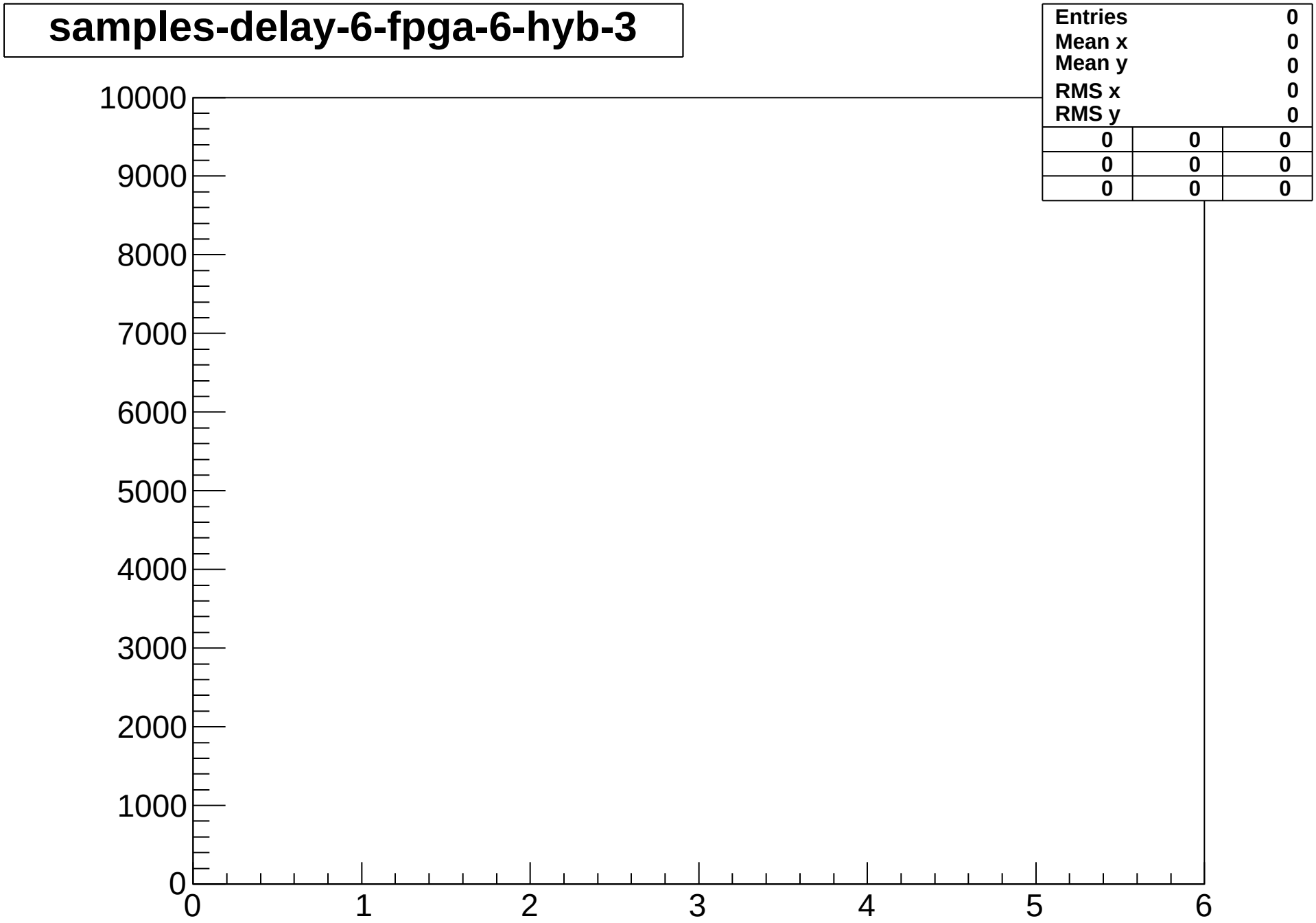
samples-delay-6-fpga-6-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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6000
5000
4000
3000
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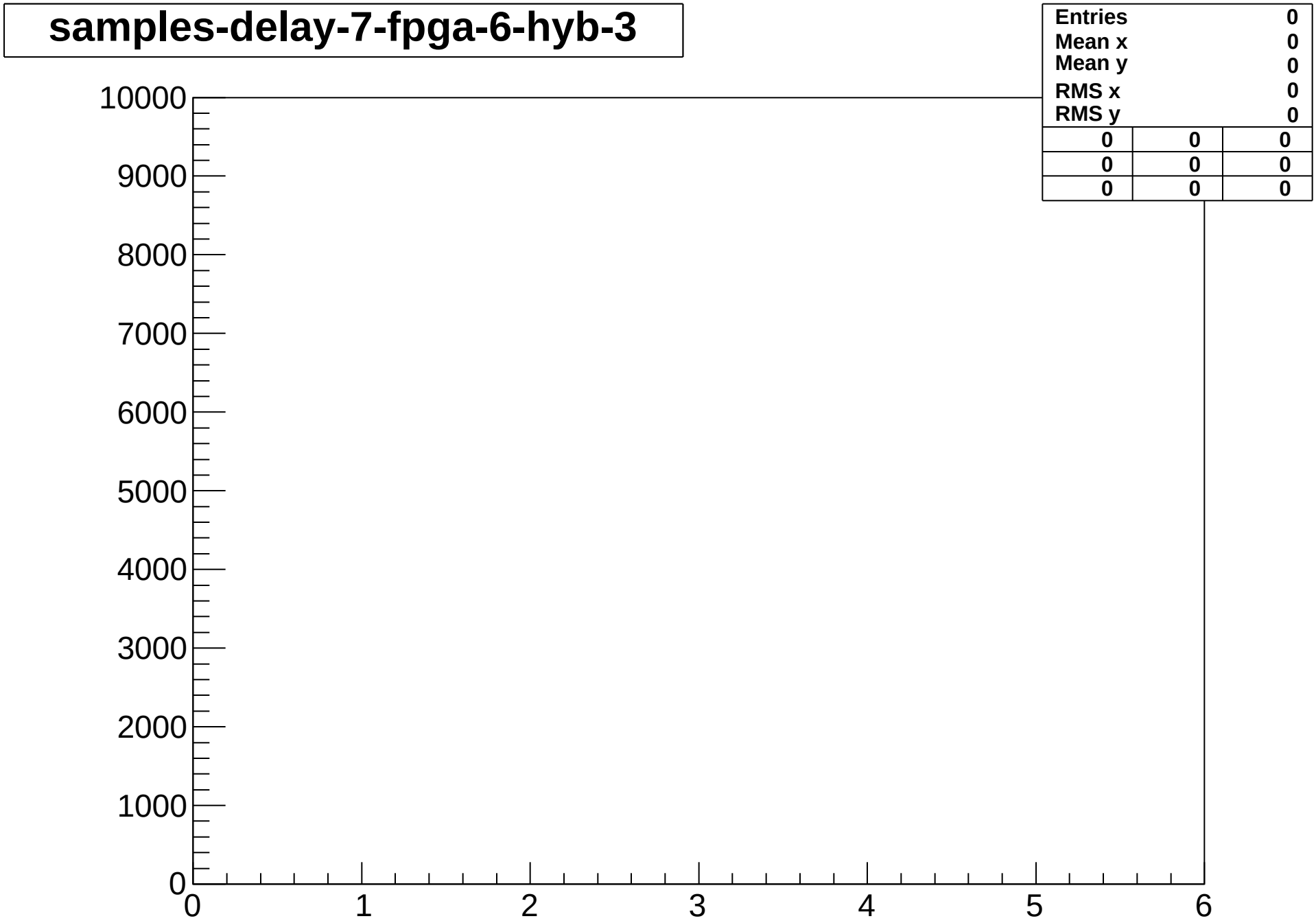
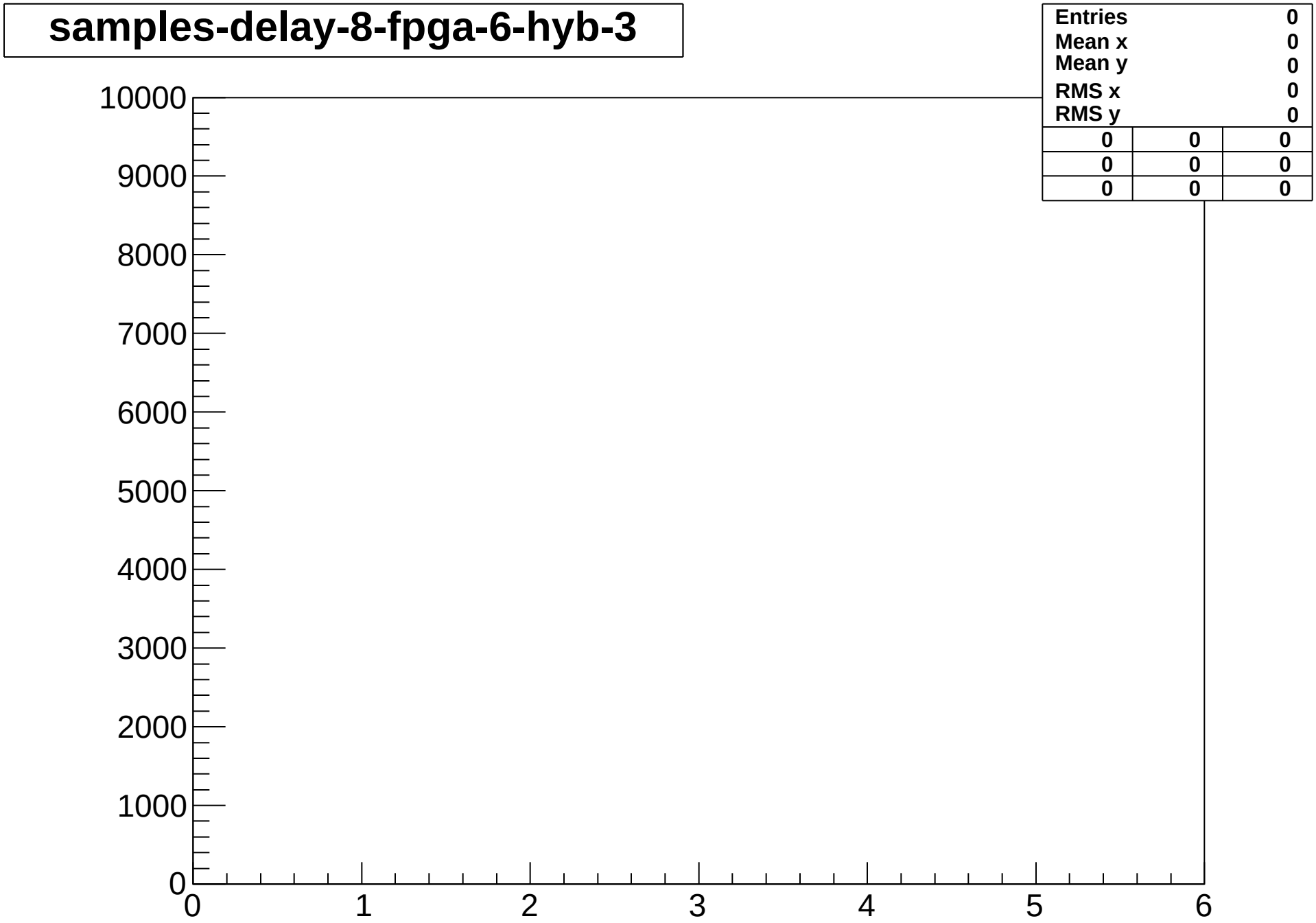
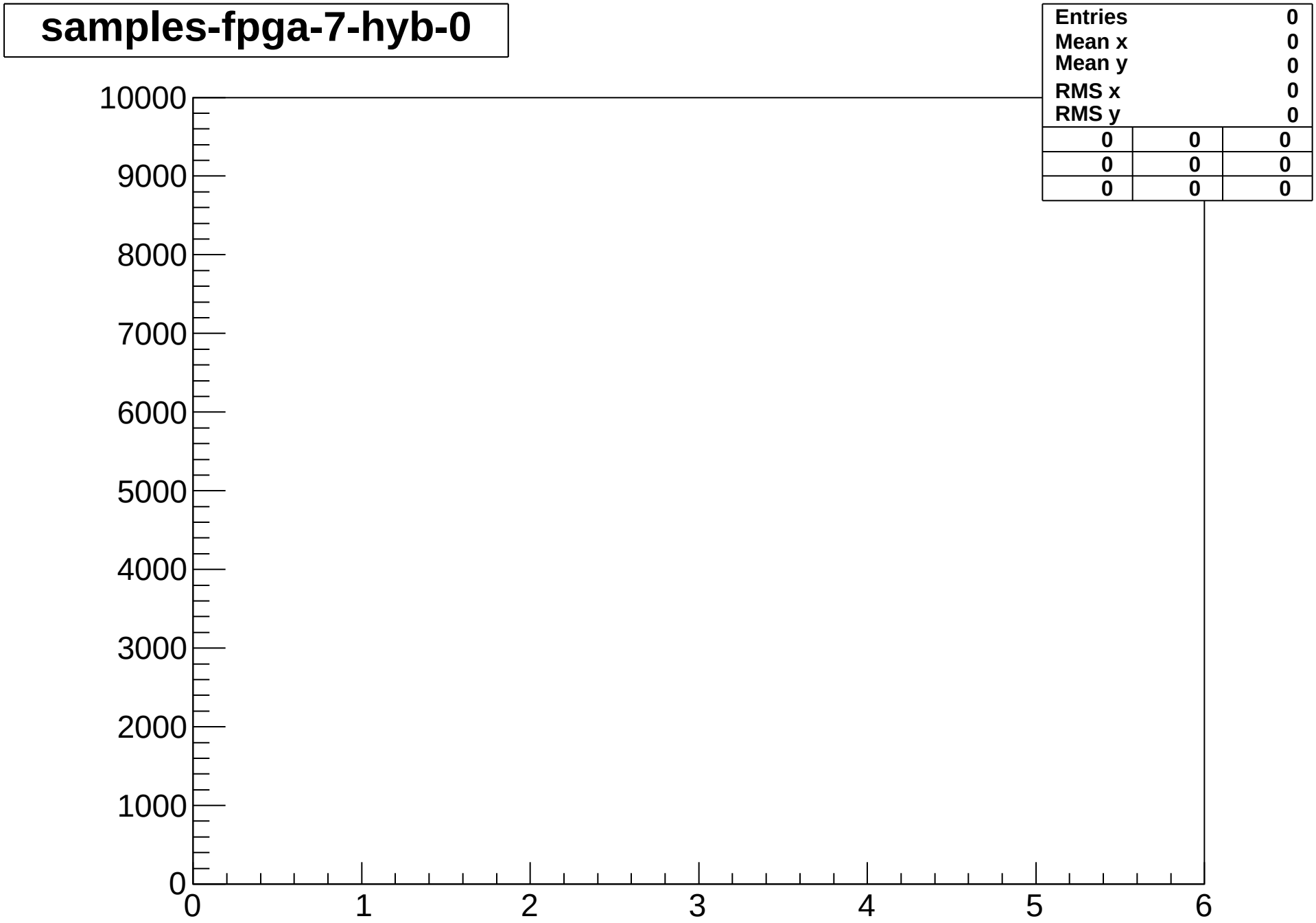
samples-delay-7-fpga-6-hyb-3



samples-delay-8-fpga-6-hyb-3




samples-fpga-7-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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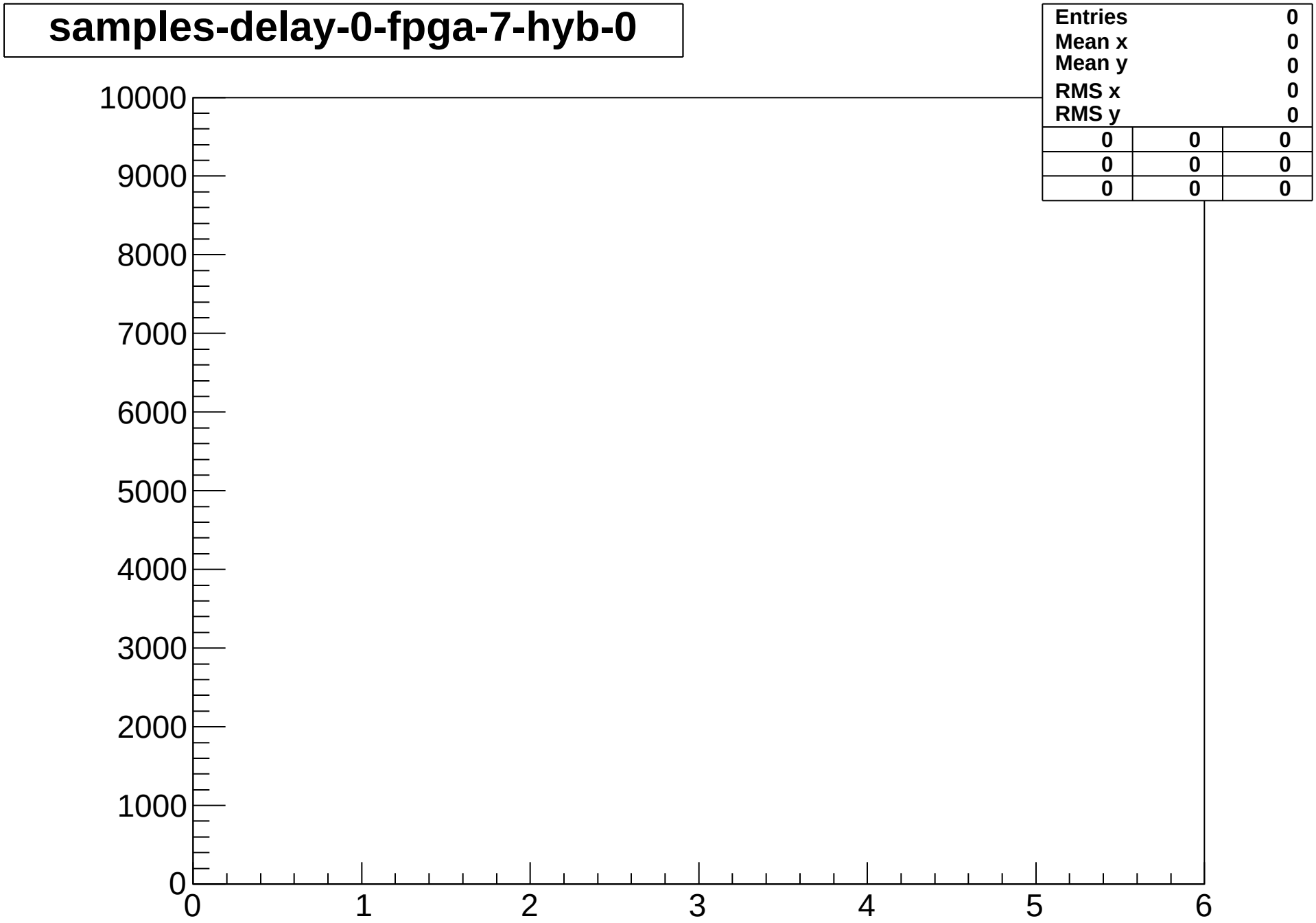
samples-delay-0-fpga-7-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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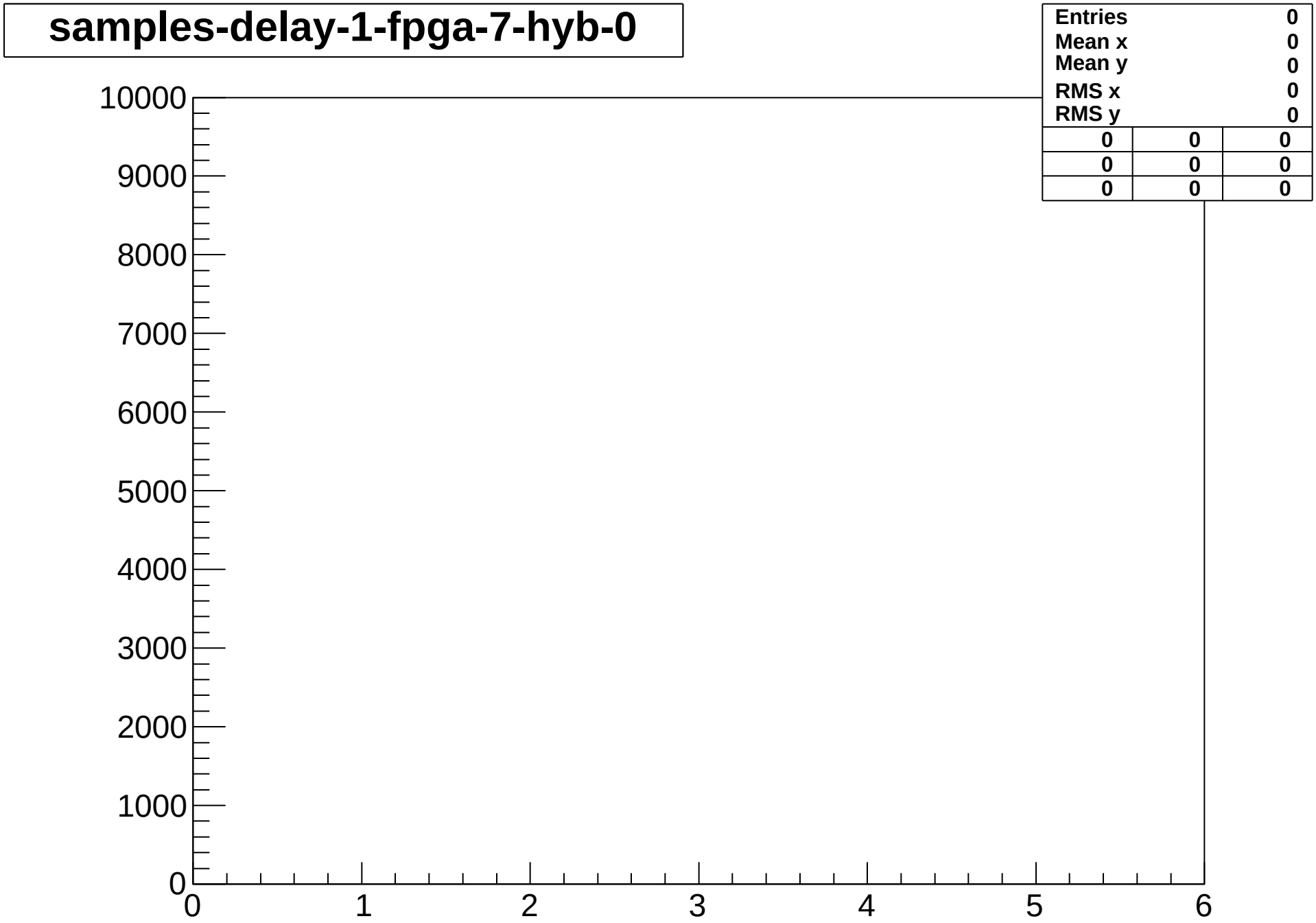
samples-delay-1-fpga-7-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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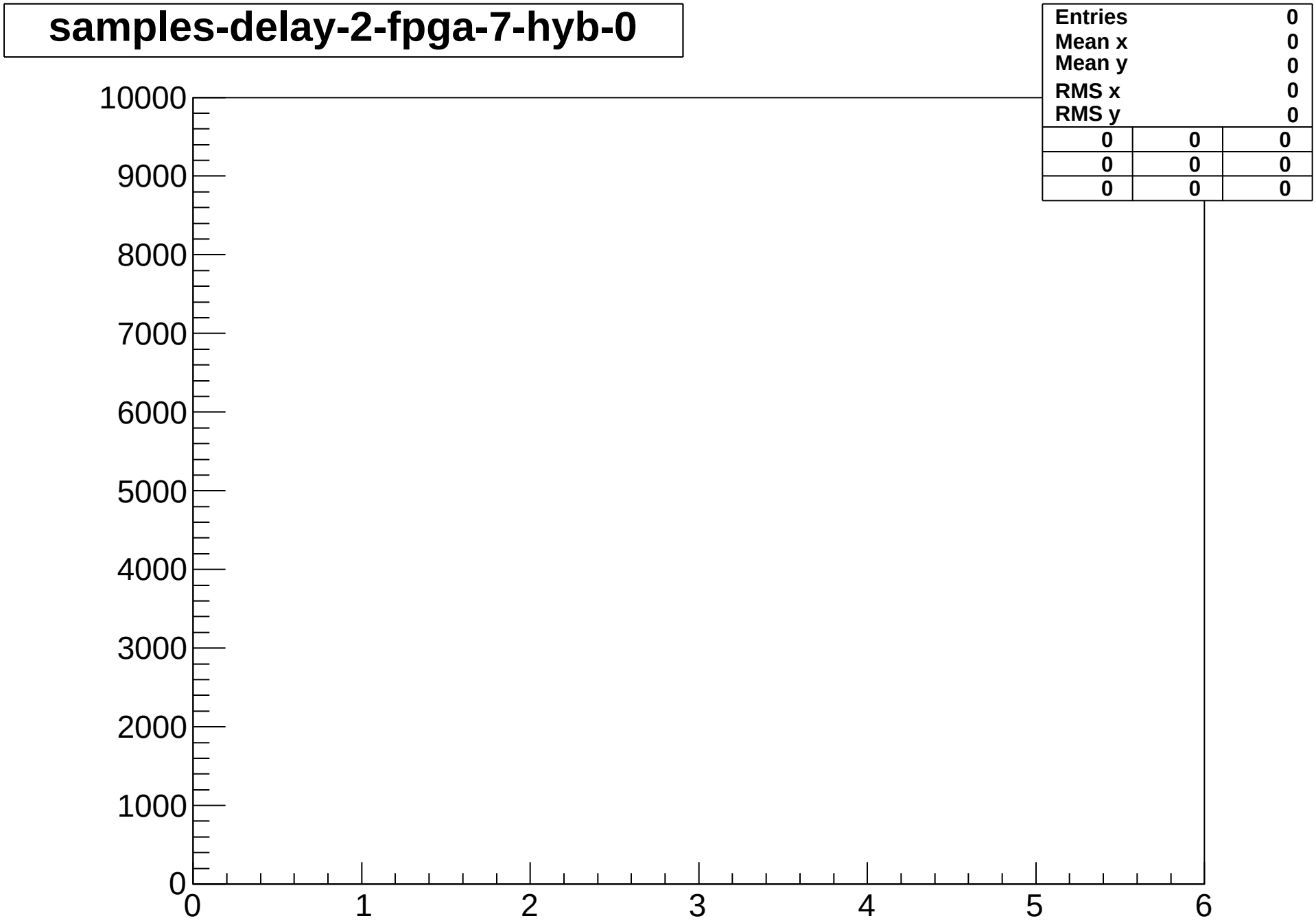
samples-delay-2-fpga-7-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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6000
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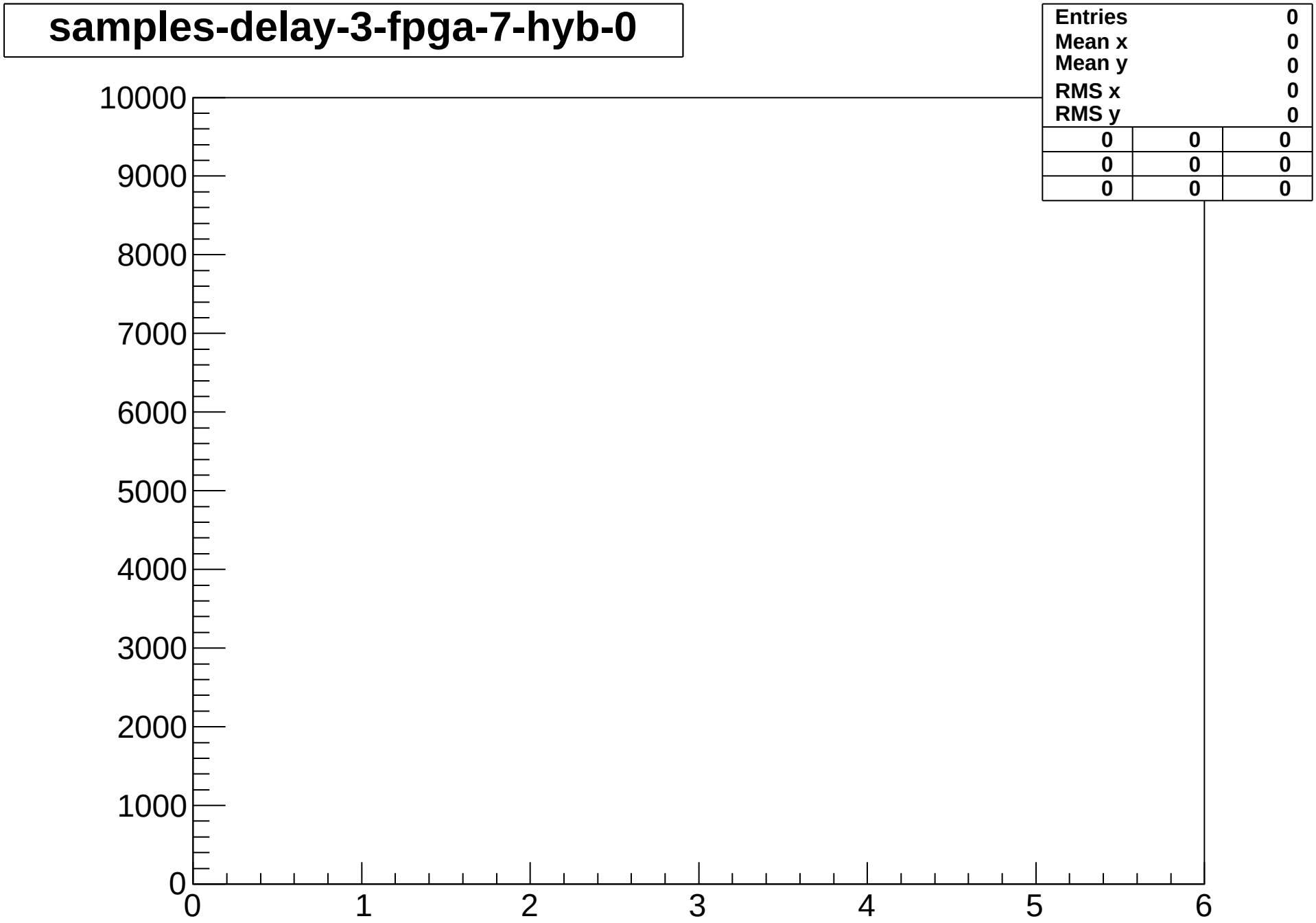
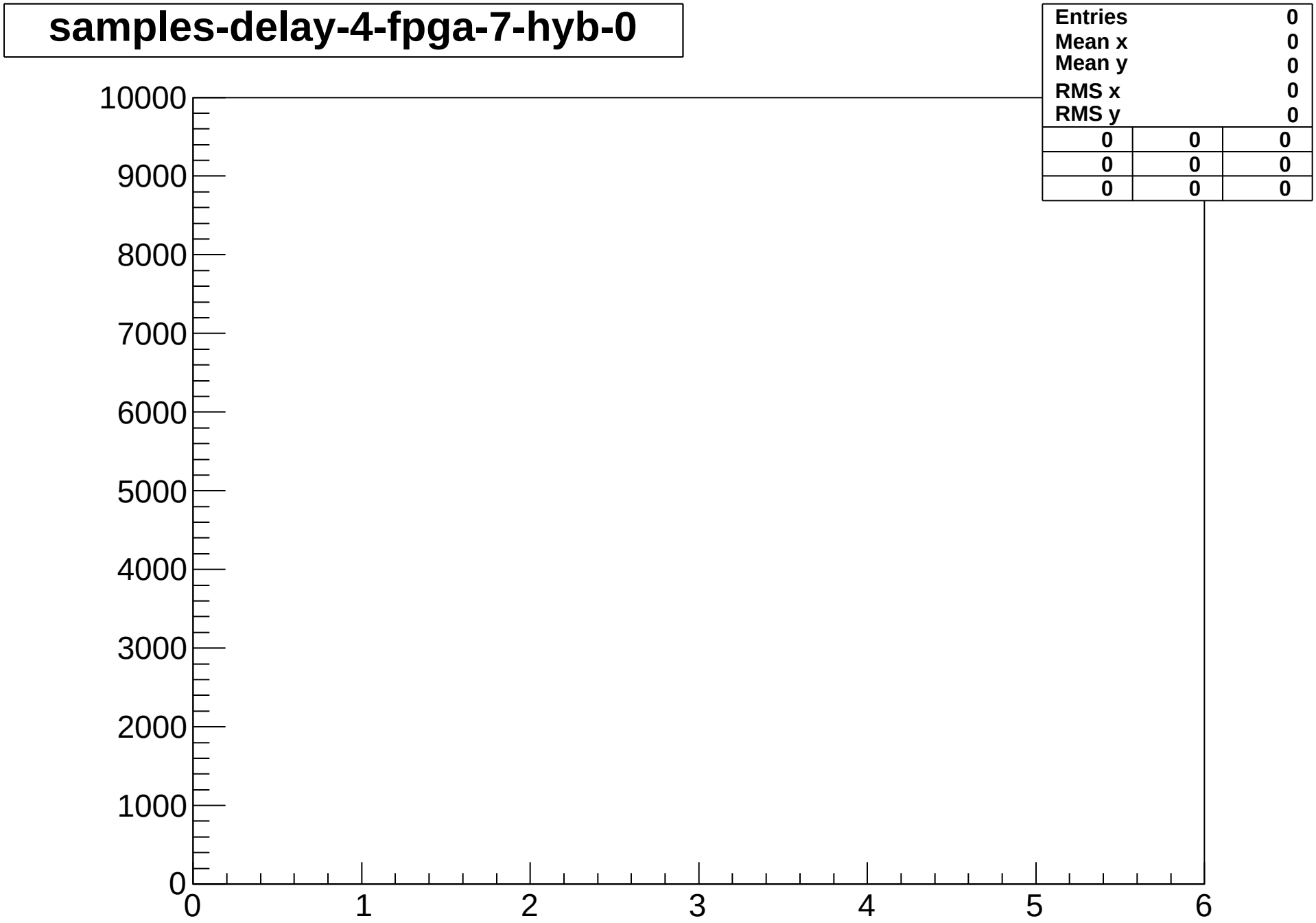
samples-delay-3-fpga-7-hyb-0




samples-delay-4-fpga-7-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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3000
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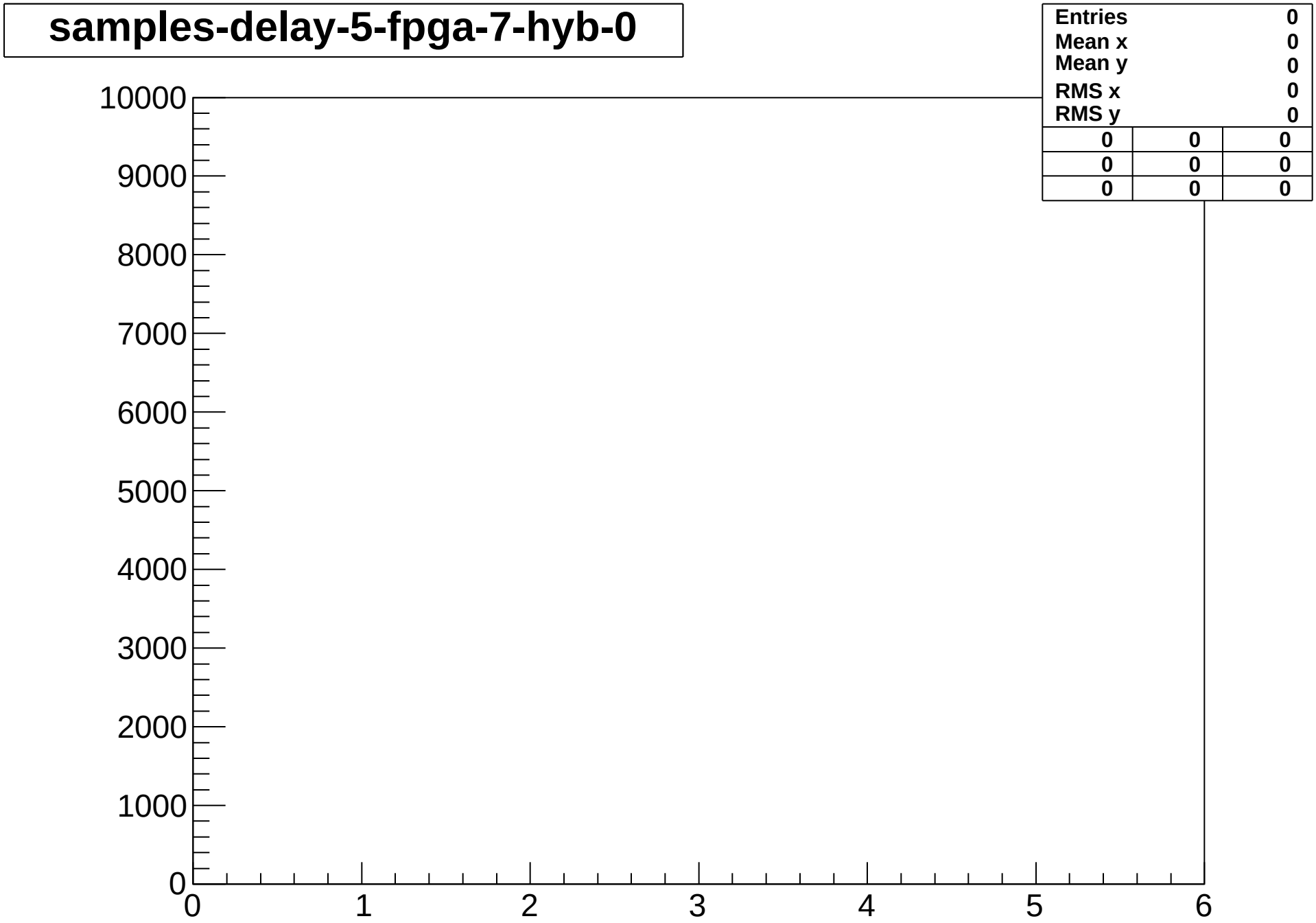
samples-delay-5-fpga-7-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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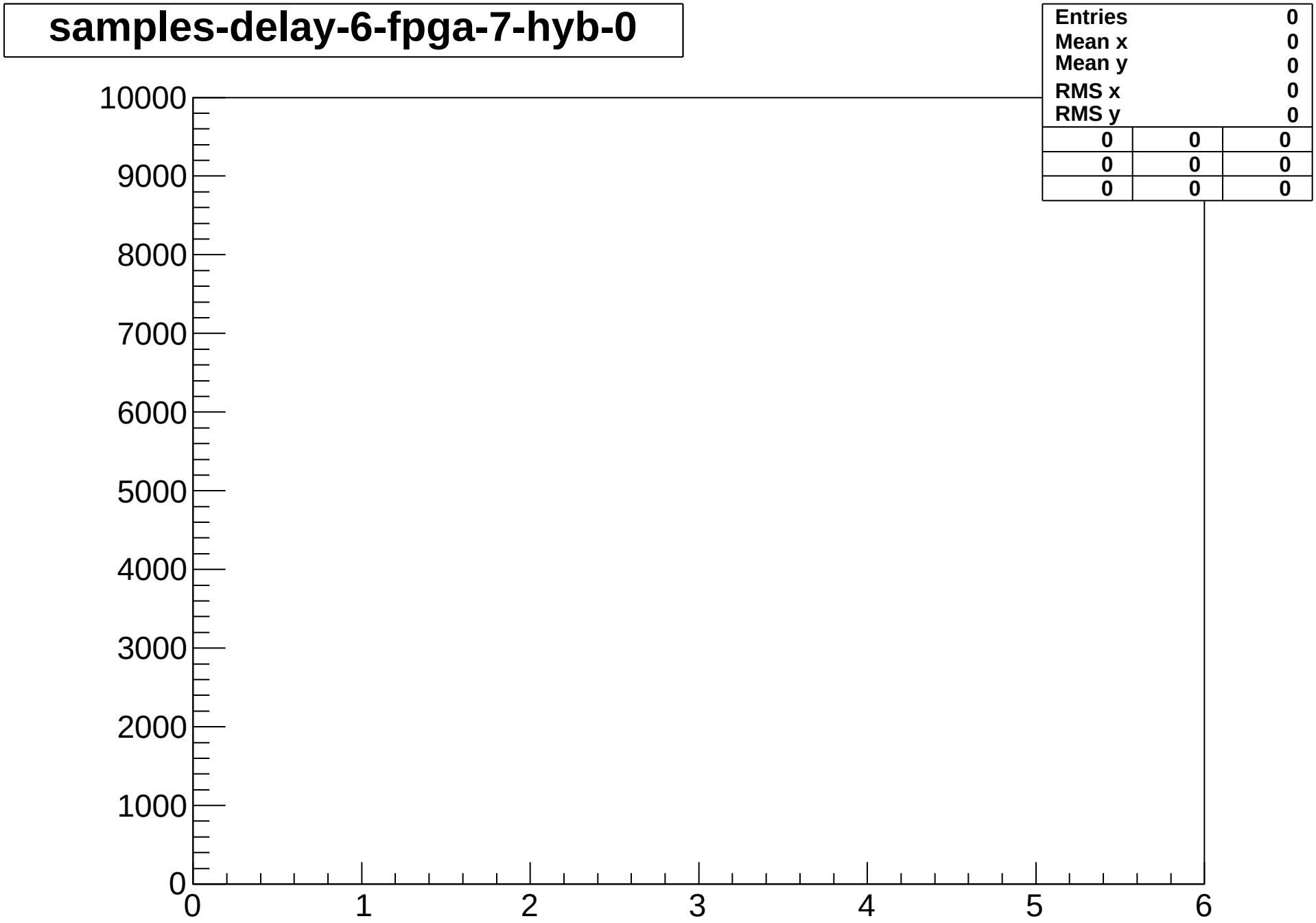
6


samples-delay-6-fpga-7-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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4
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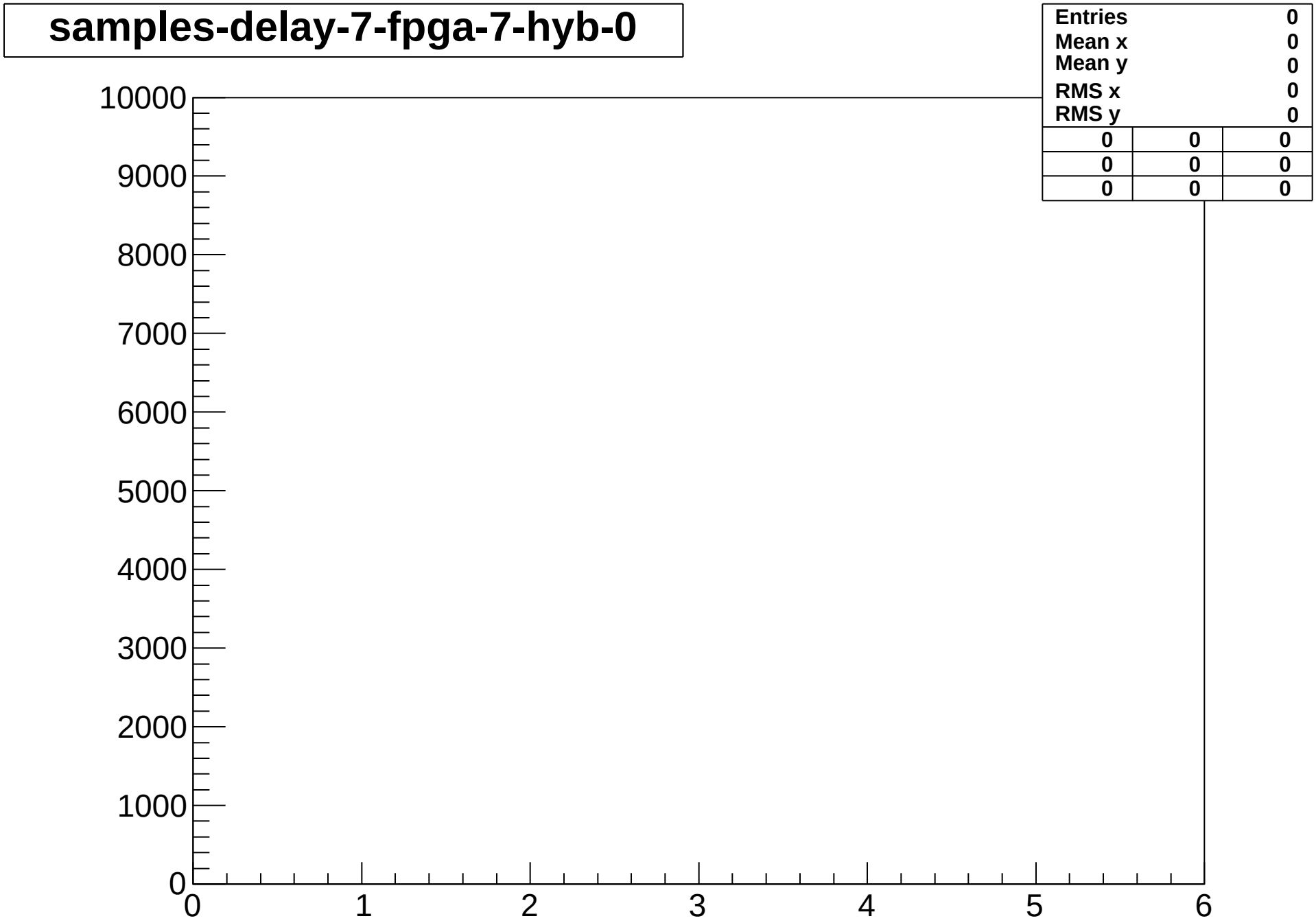
6


samples-delay-7-fpga-7-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
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5000
4000
3000
2000
1000
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0
1
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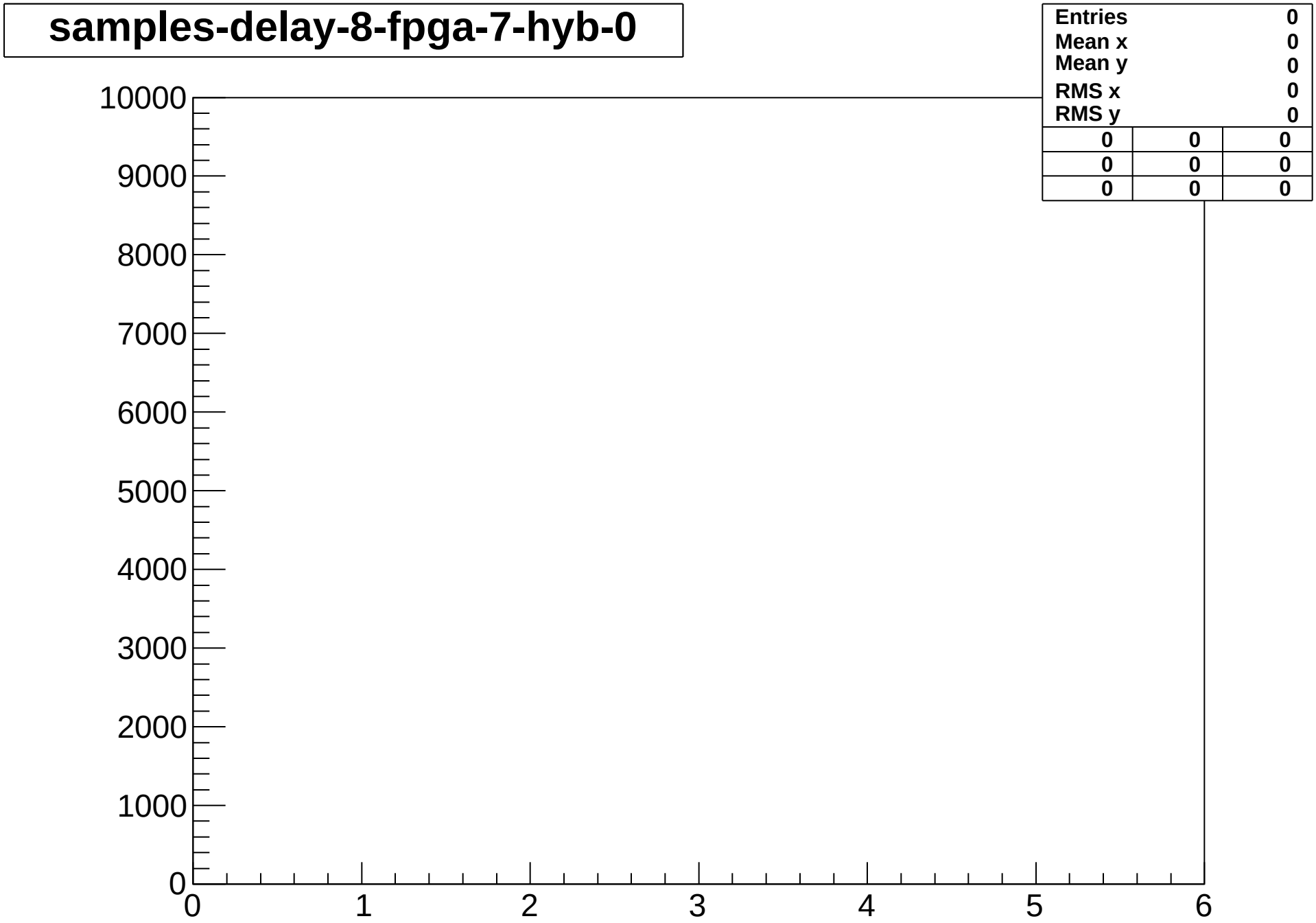
samples-delay-8-fpga-7-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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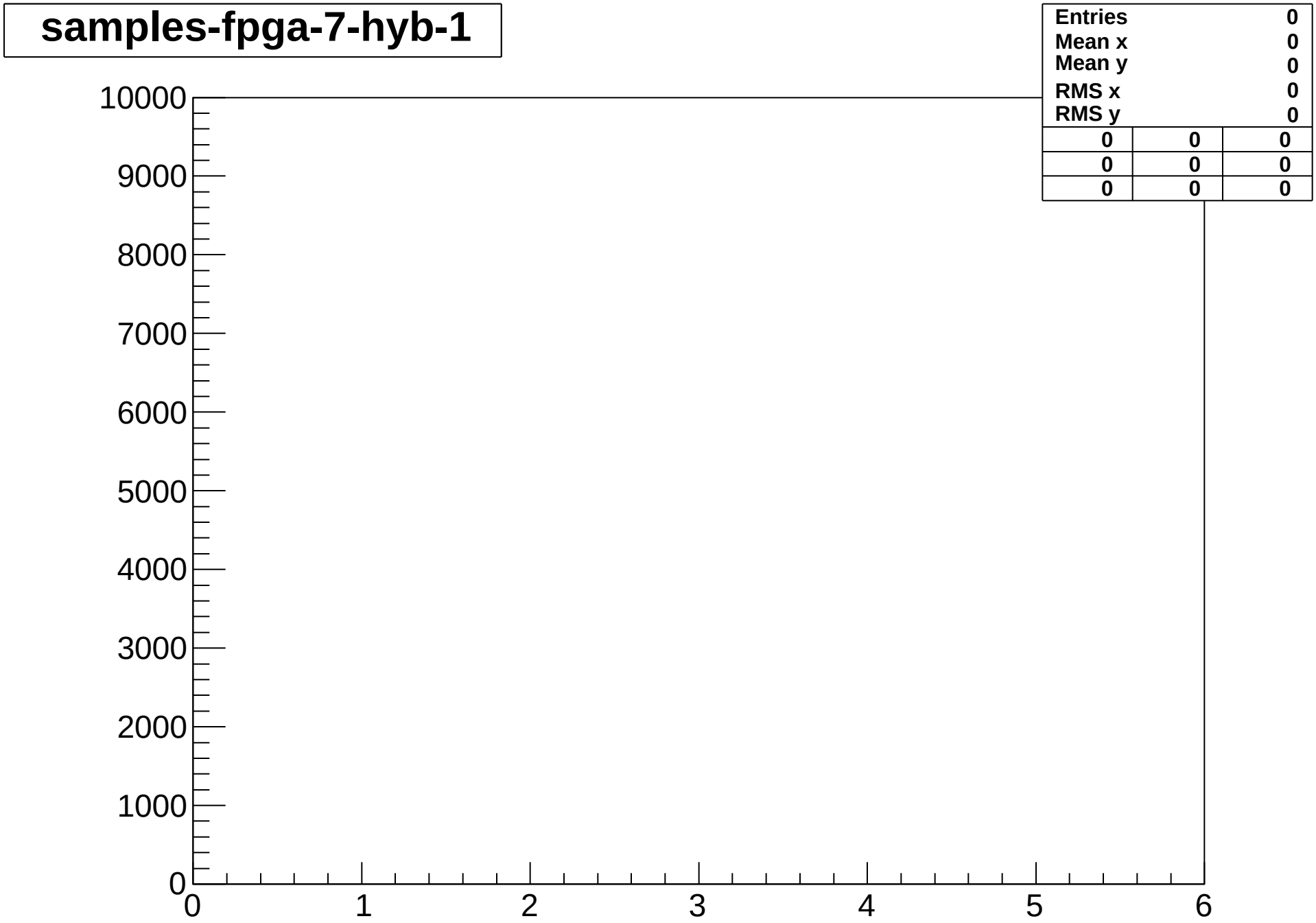
4
5
6


samples-fpga-7-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
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1
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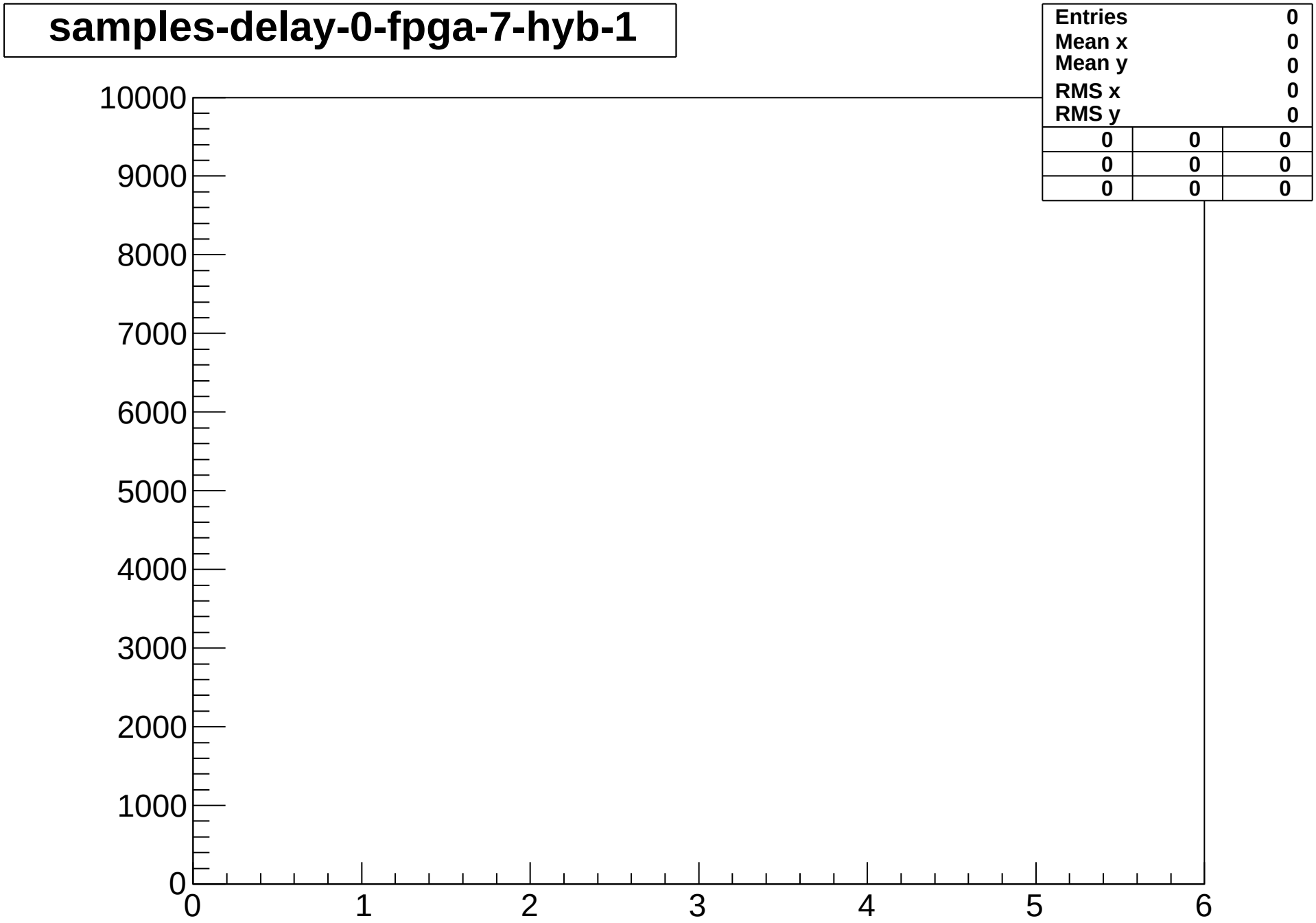
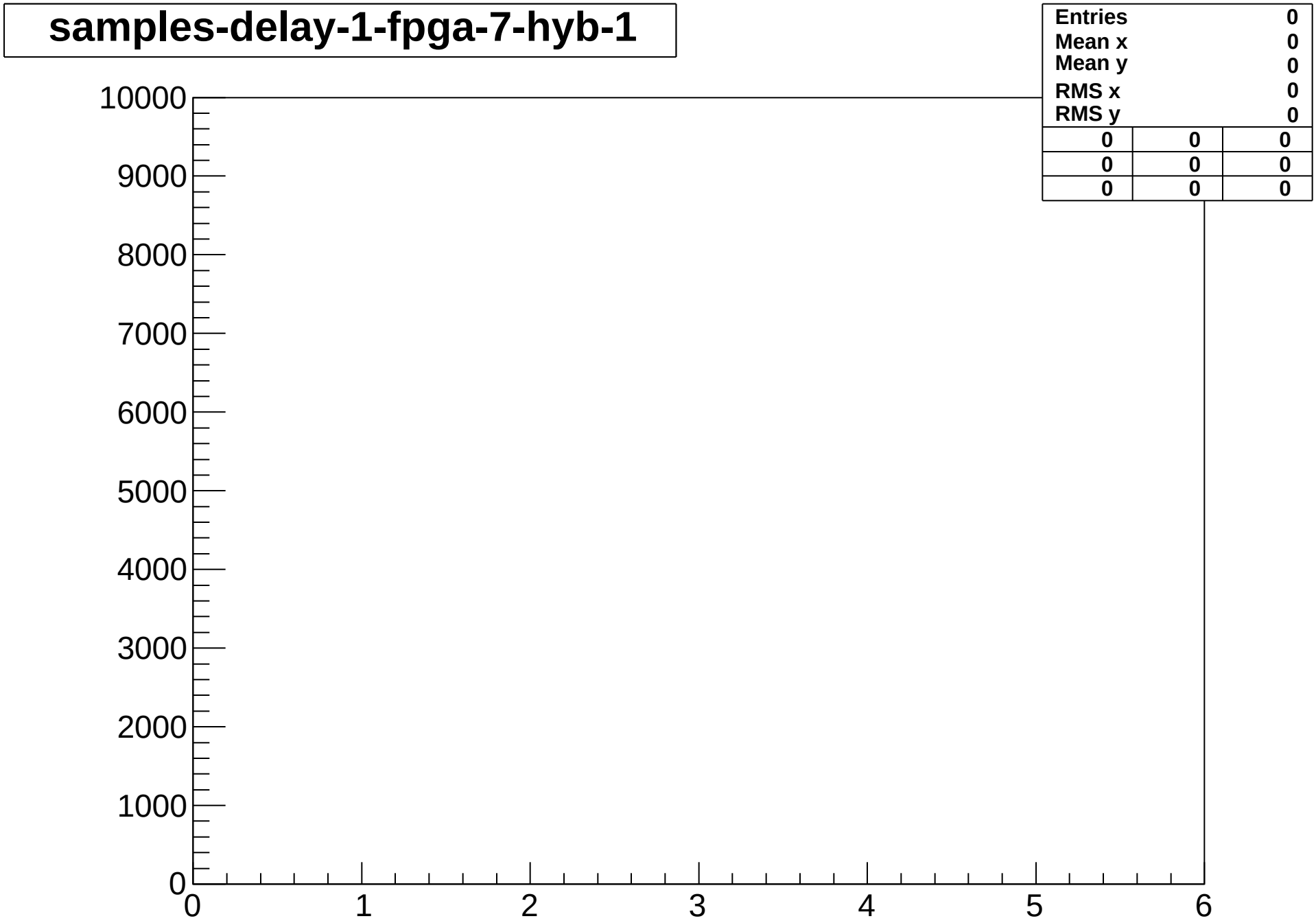
samples-delay-0-fpga-7-hyb-1




samples-delay-1-fpga-7-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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4000
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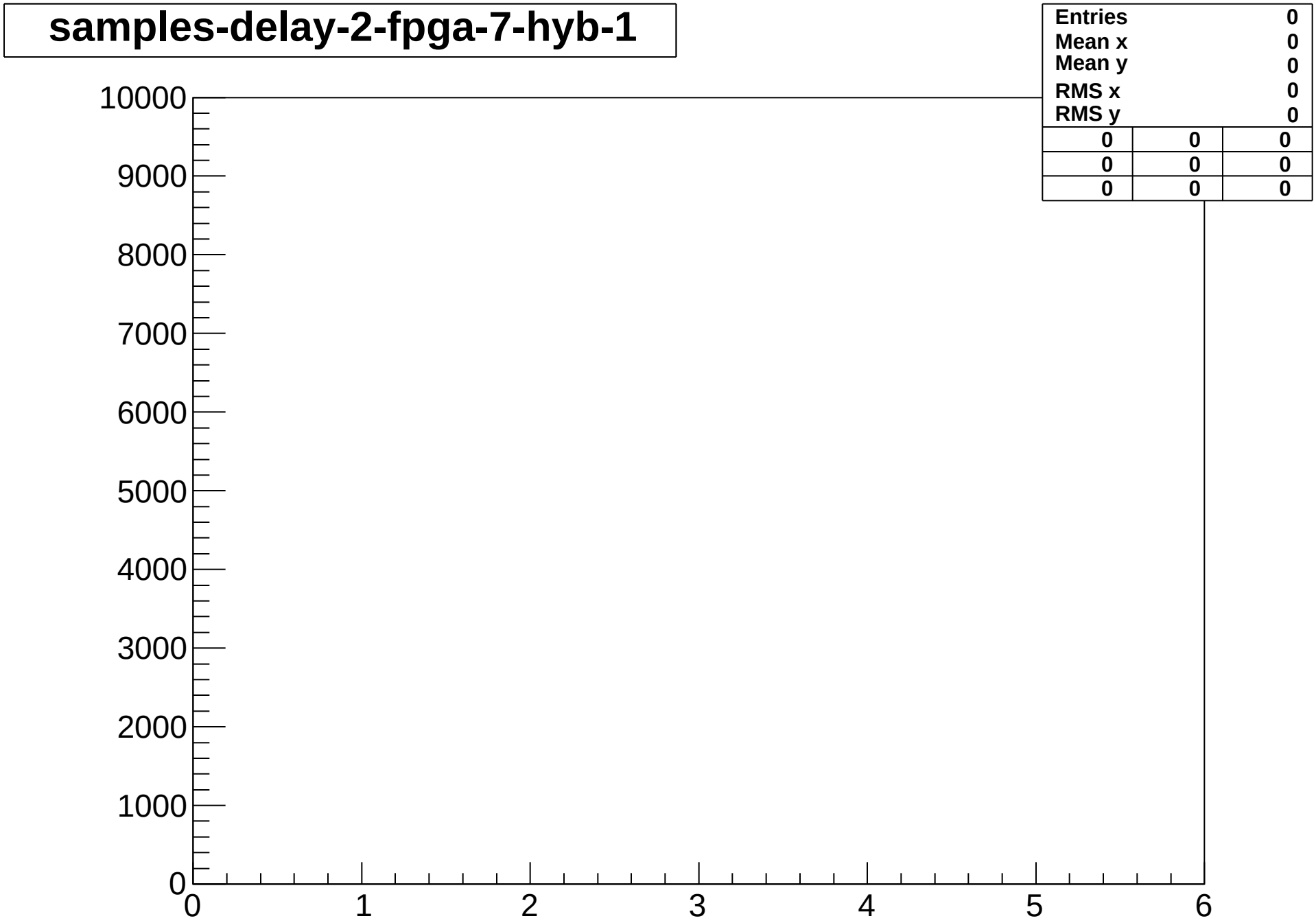
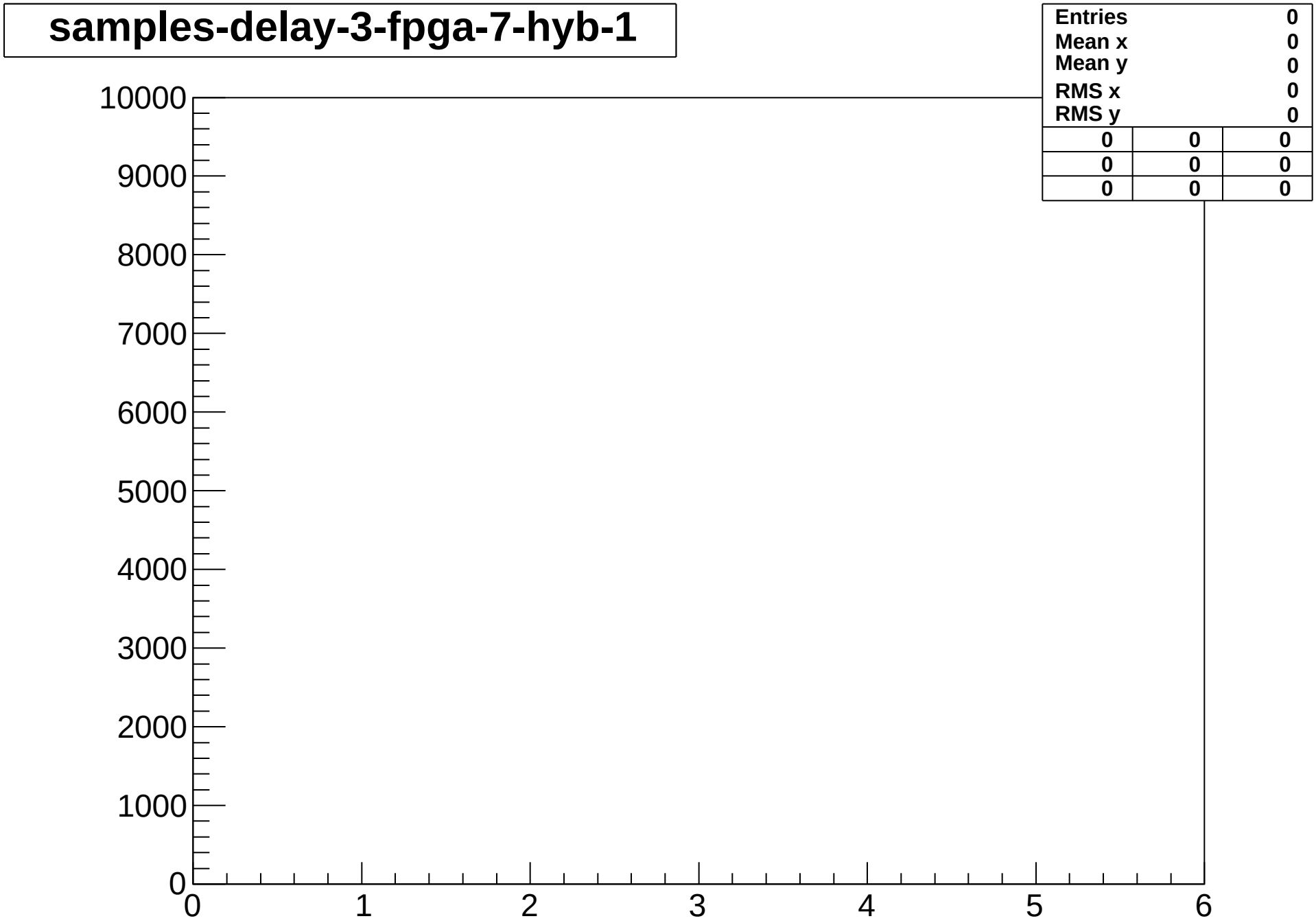
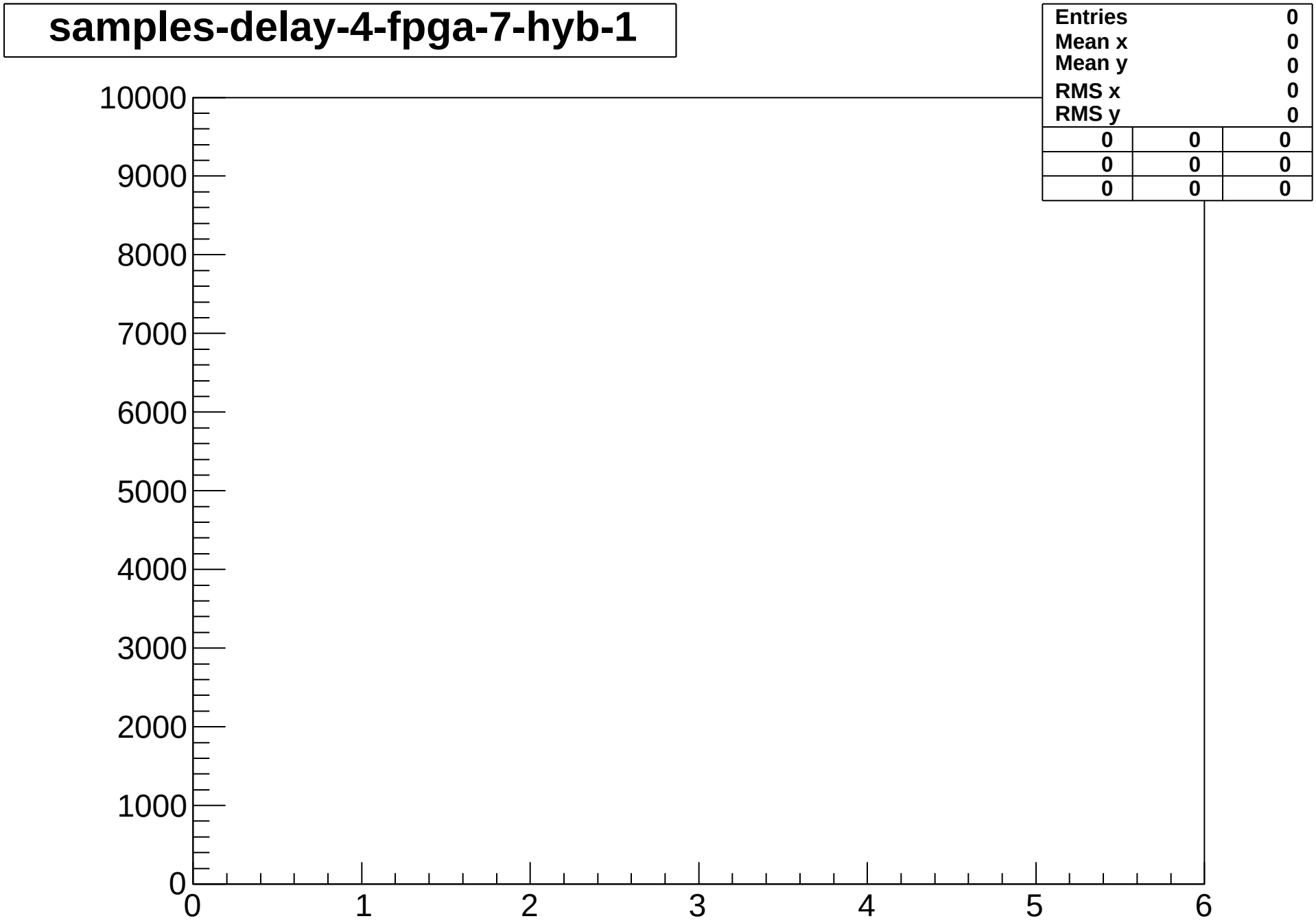
samples-delay-2-fpga-7-hyb-1



samples-delay-3-fpga-7-hyb-1




samples-delay-4-fpga-7-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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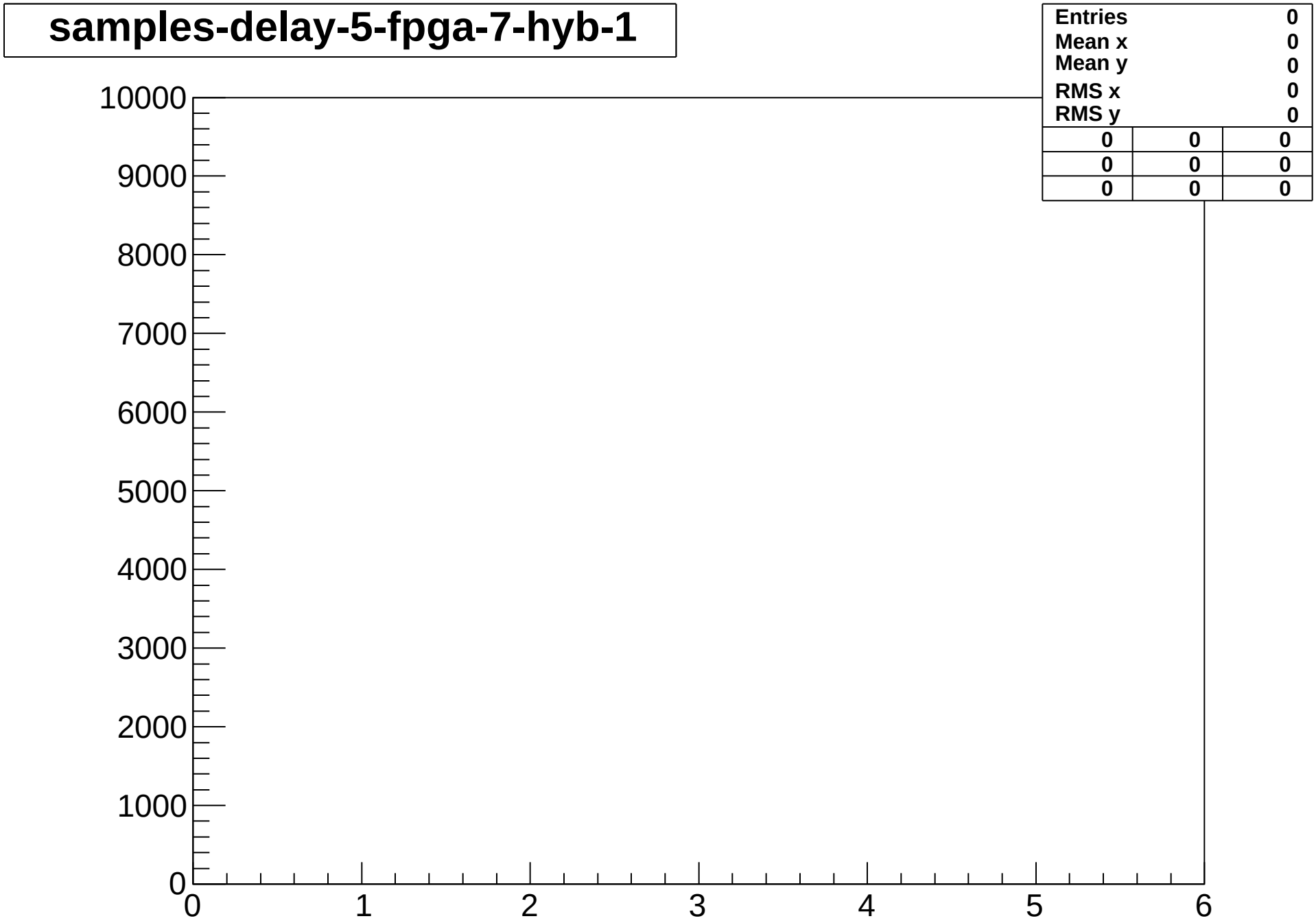
samples-delay-5-fpga-7-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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0 0 0
10000
9000
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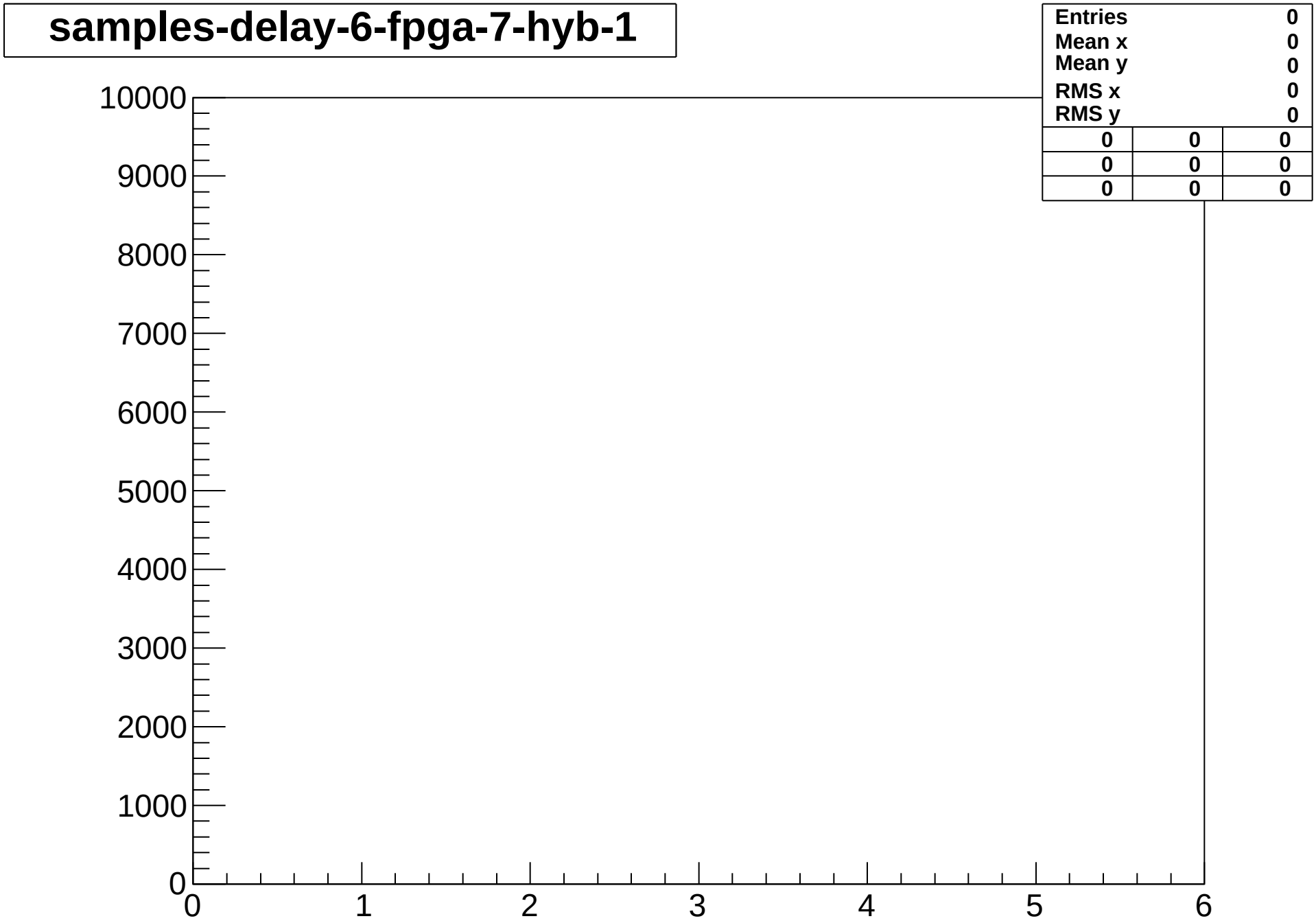
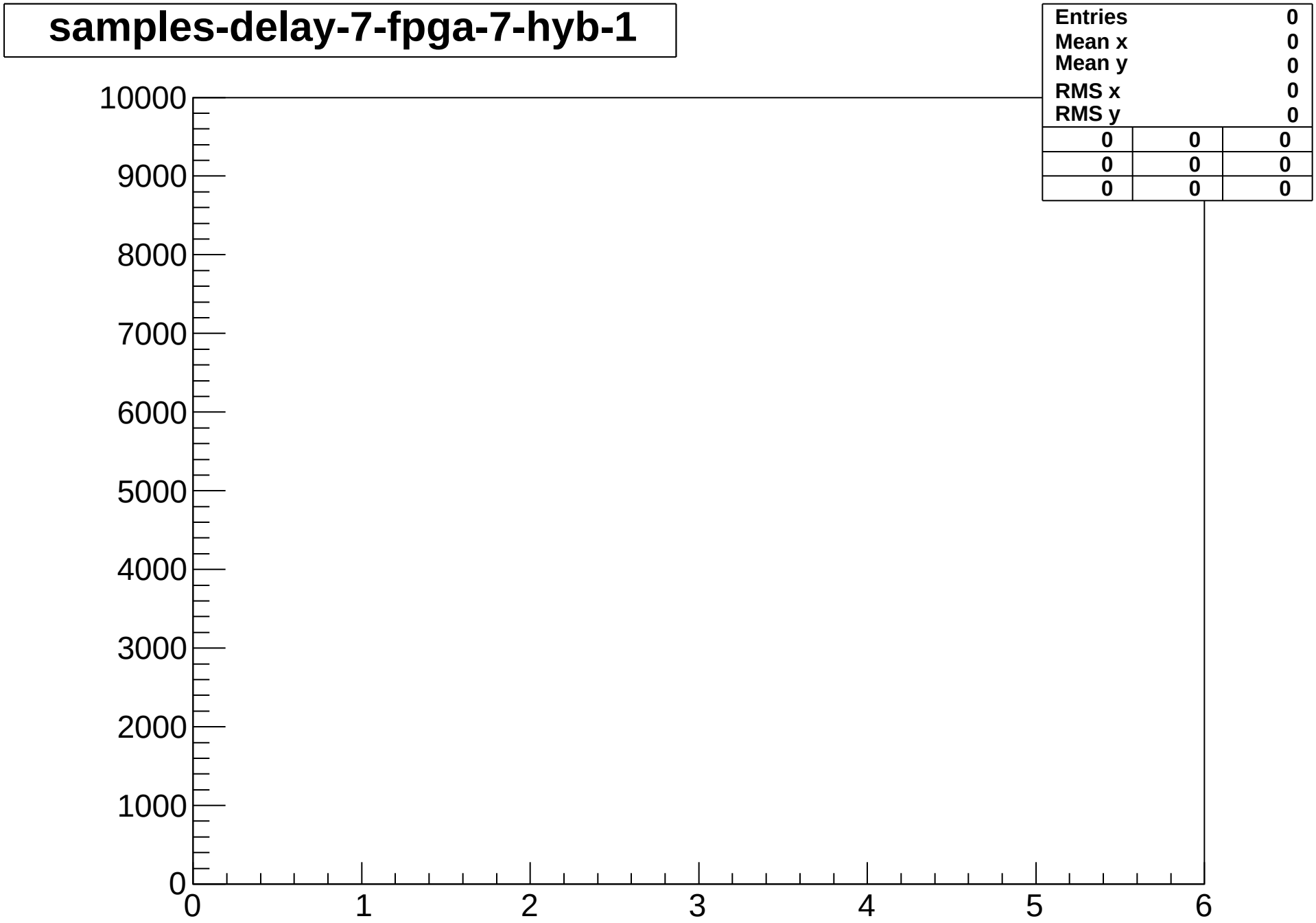

samples-delay-6-fpga-7-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6


samples-delay-7-fpga-7-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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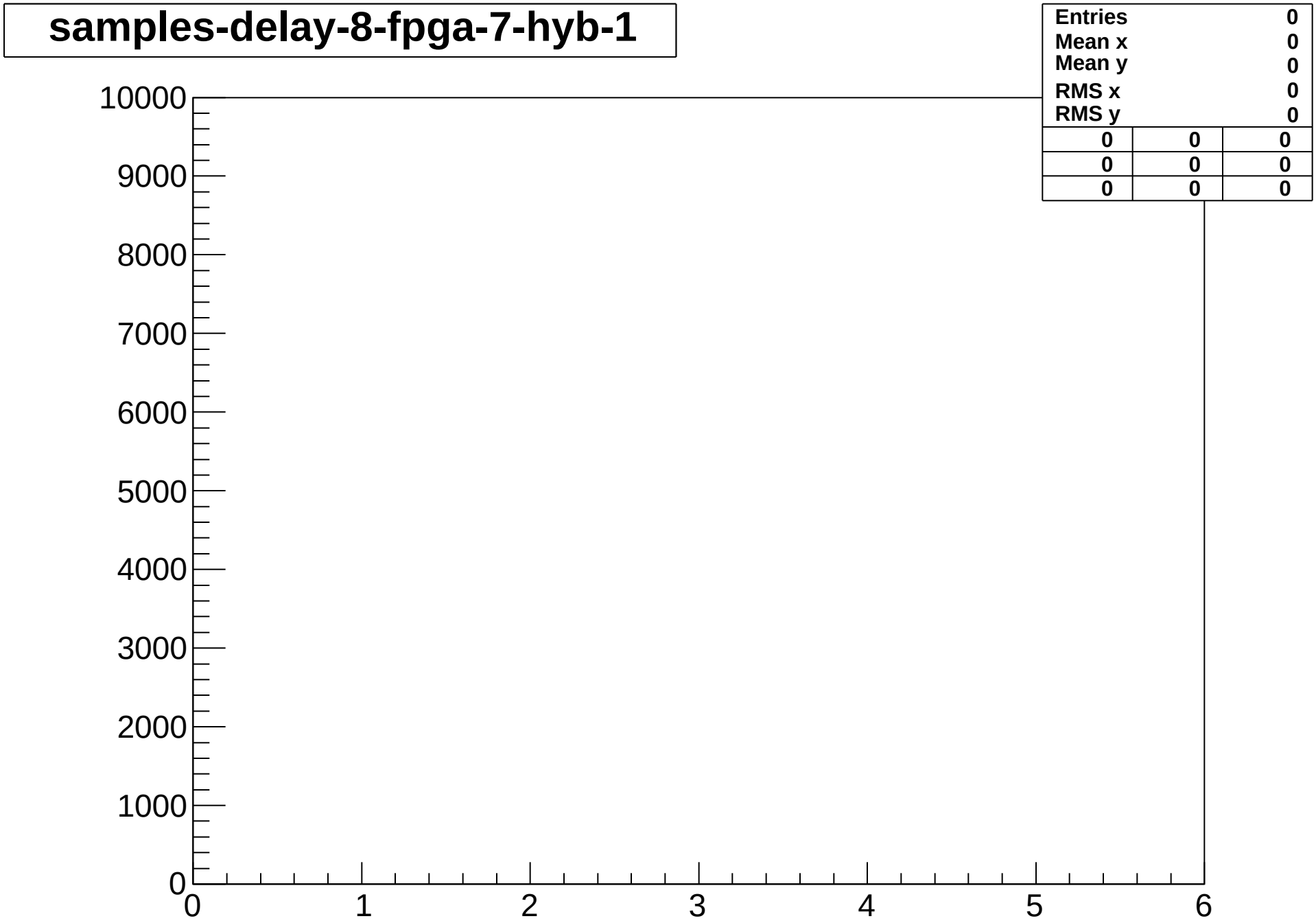
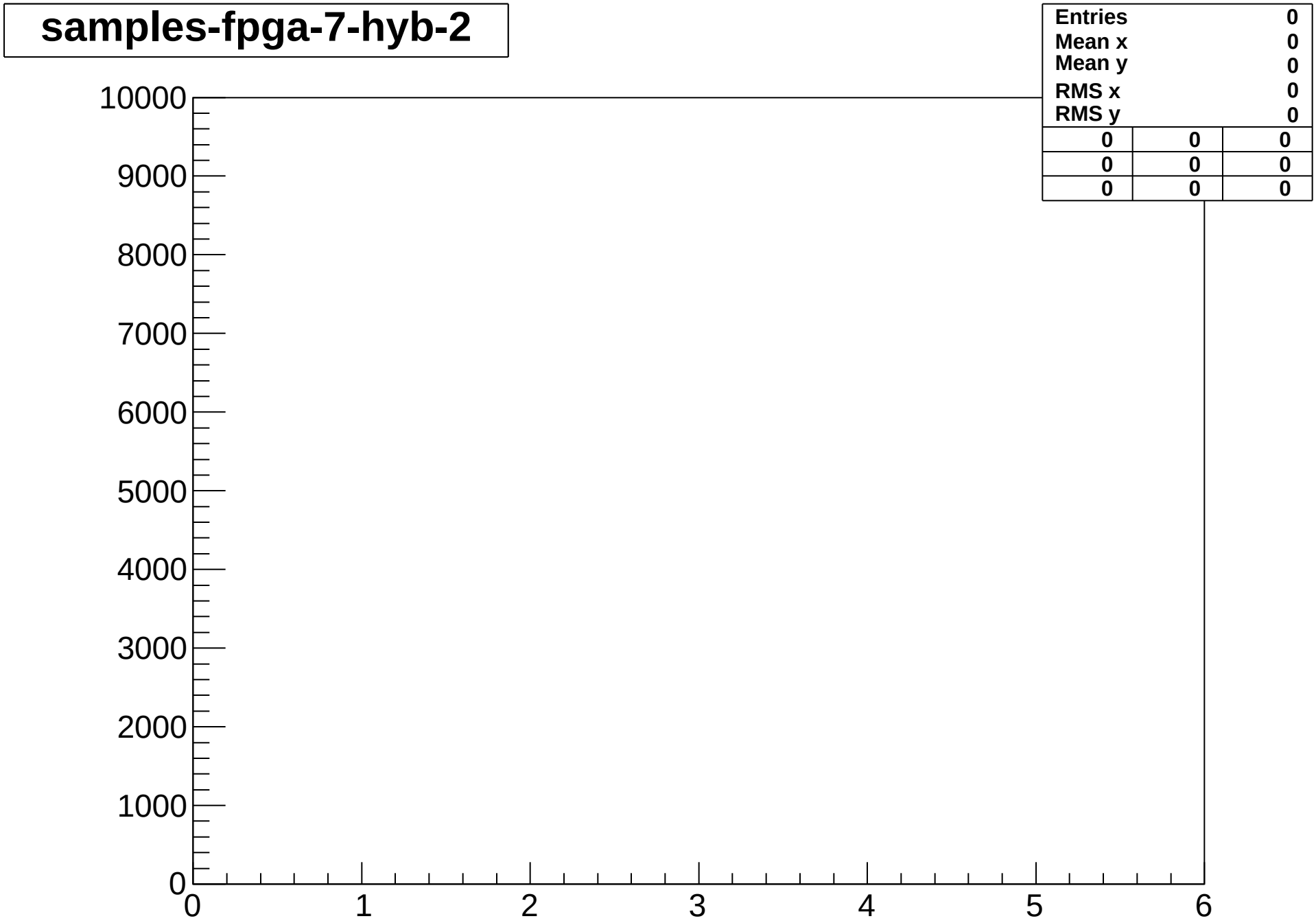
samples-delay-8-fpga-7-hyb-1




samples-fpga-7-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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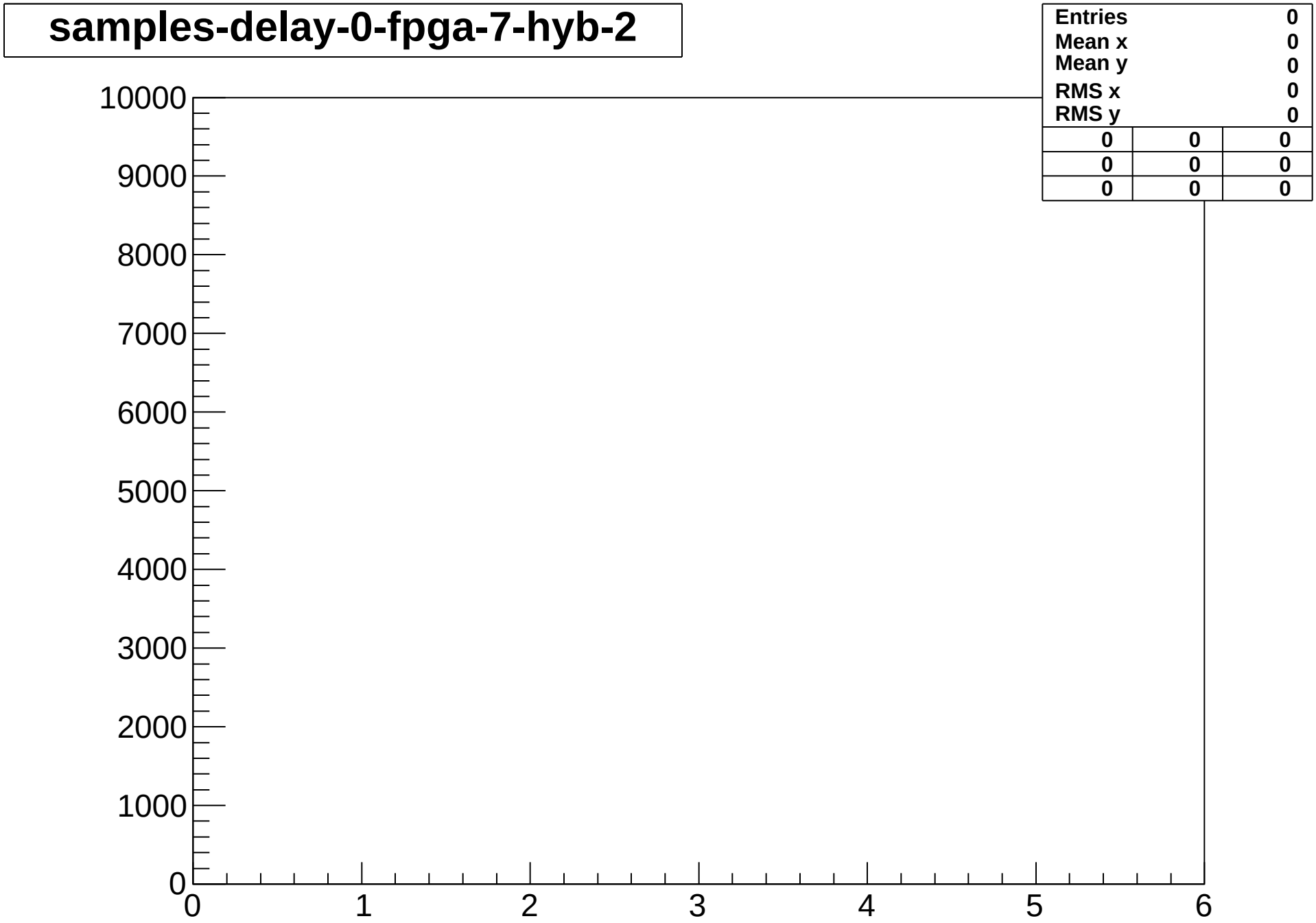
samples-delay-0-fpga-7-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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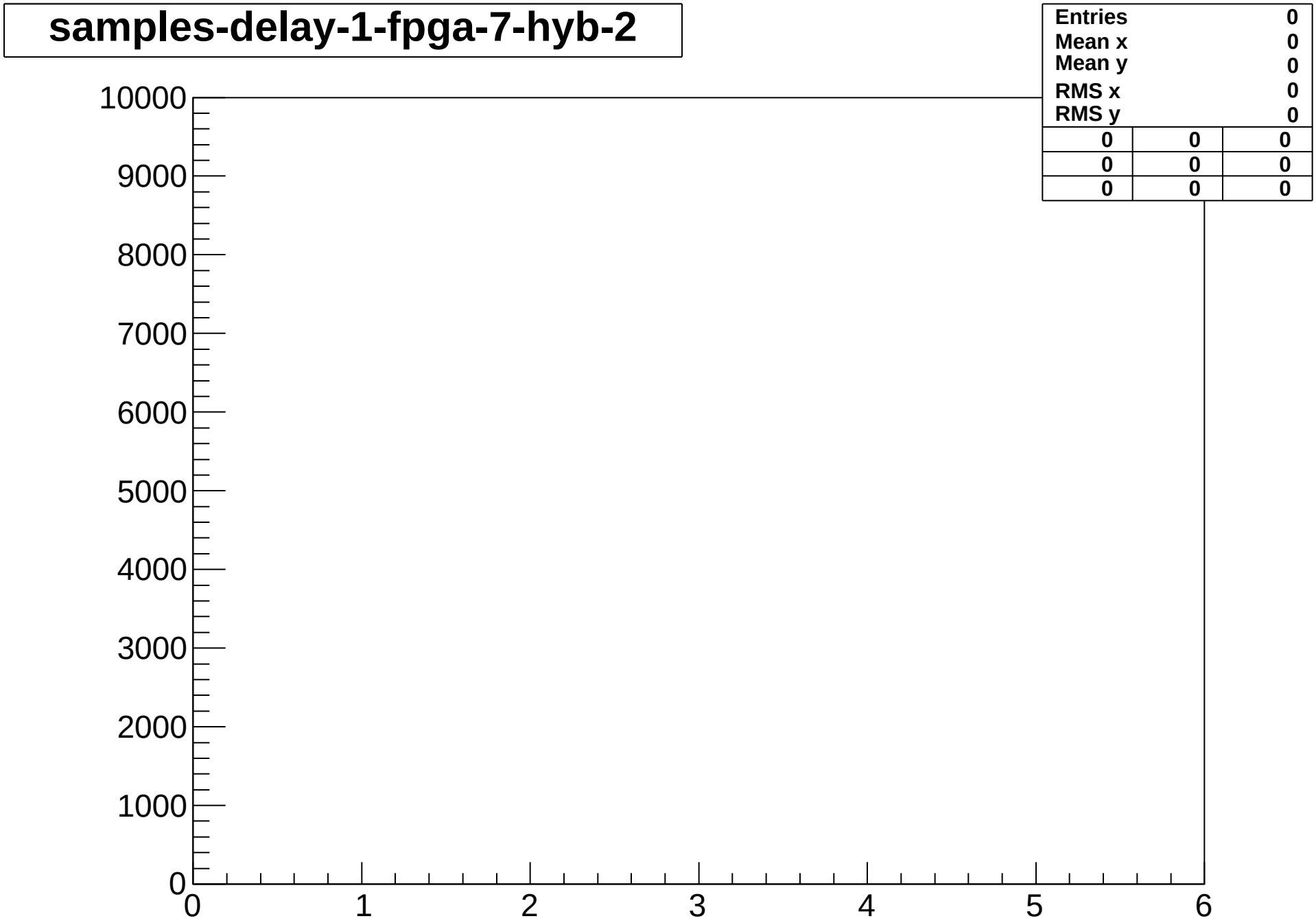
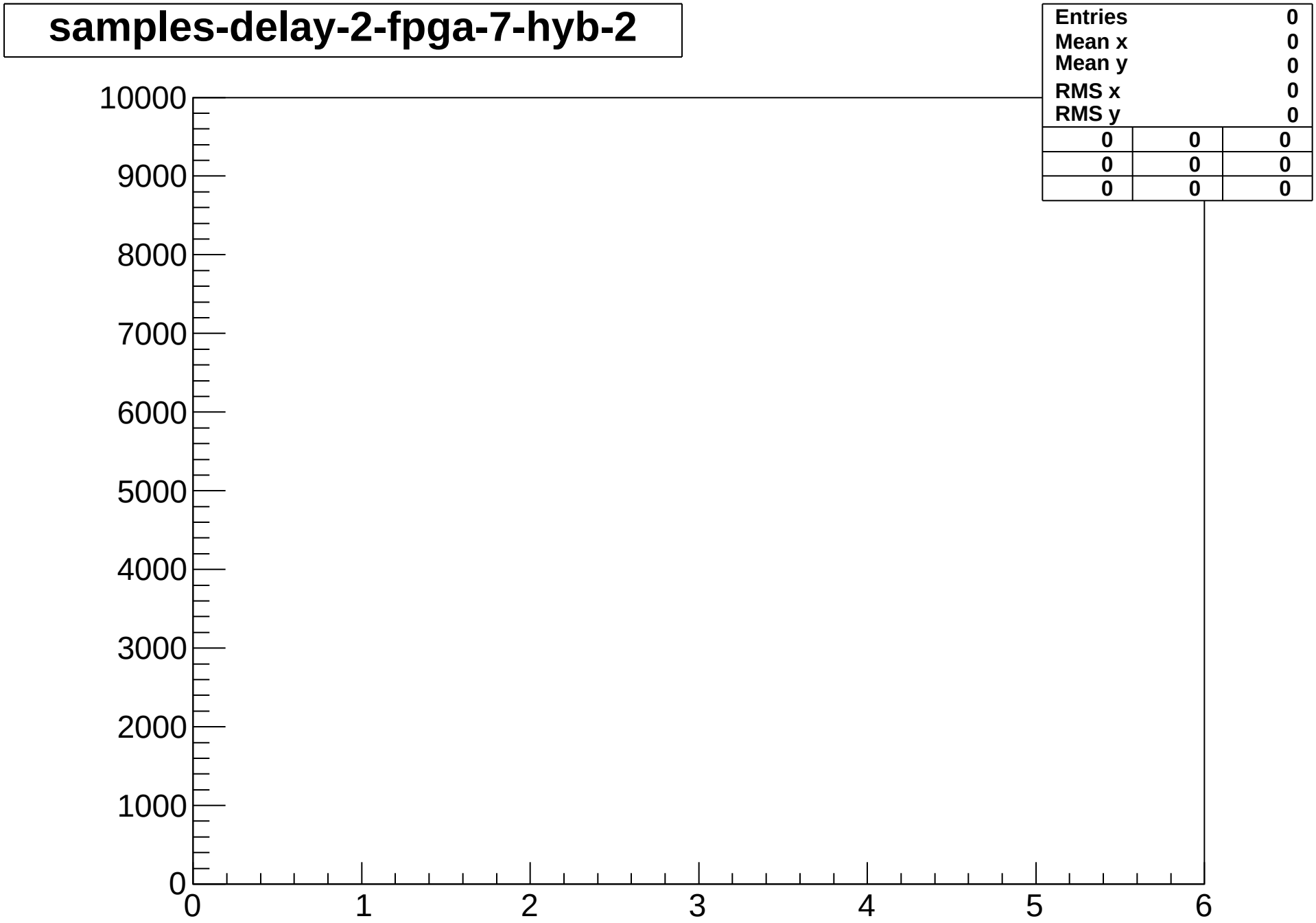
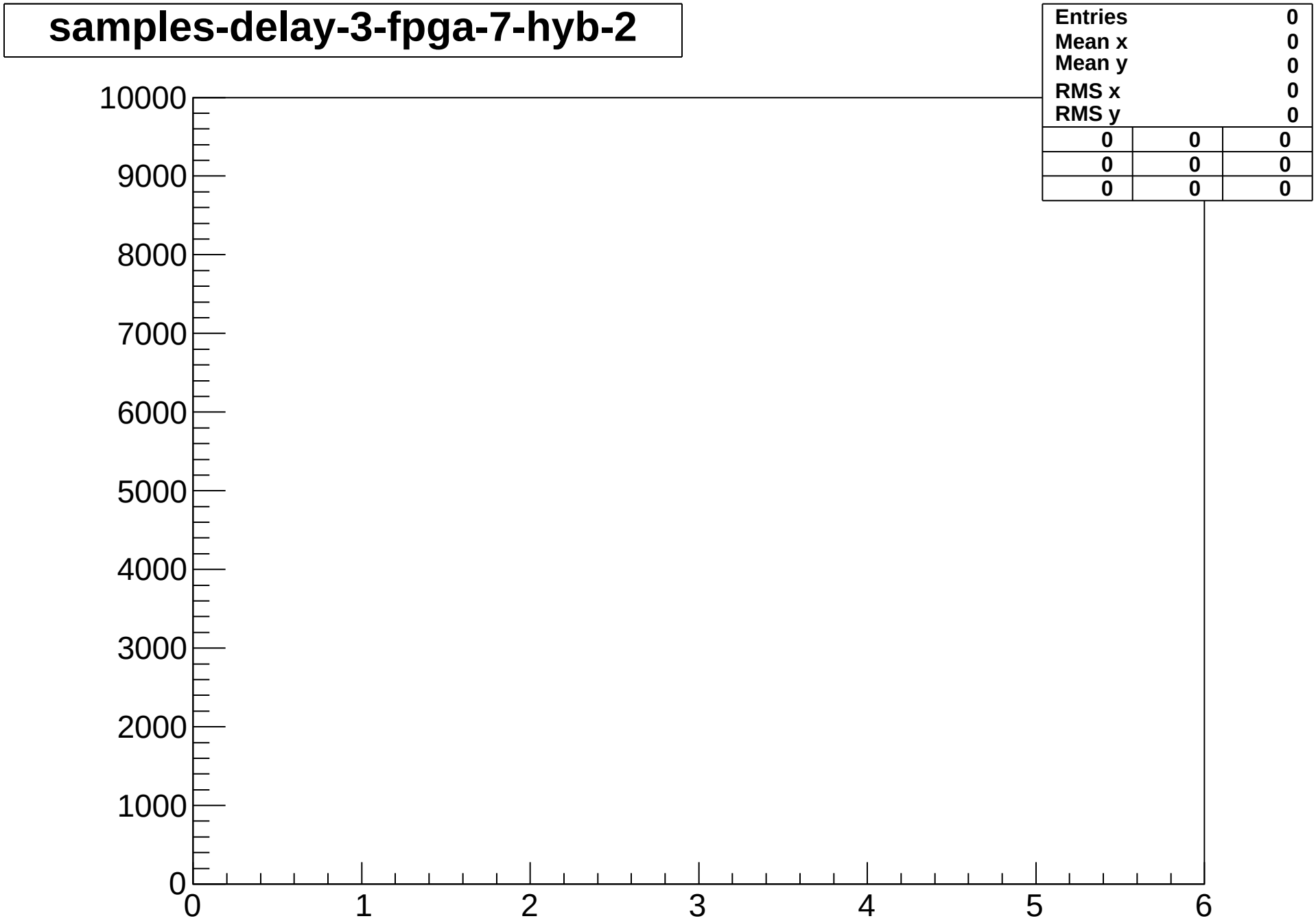
samples-delay-1-fpga-7-hyb-2



samples-delay-2-fpga-7-hyb-2




samples-delay-3-fpga-7-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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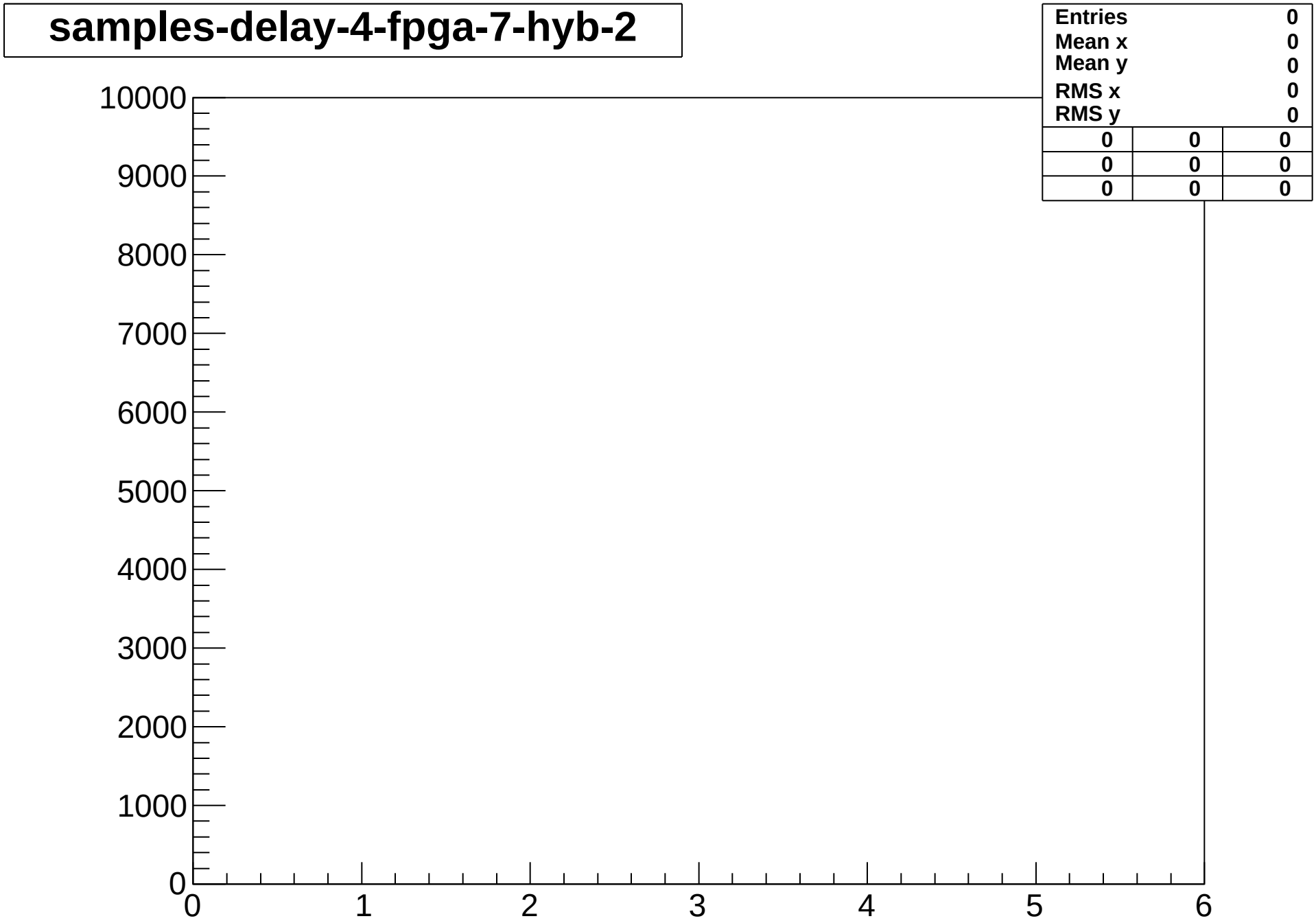
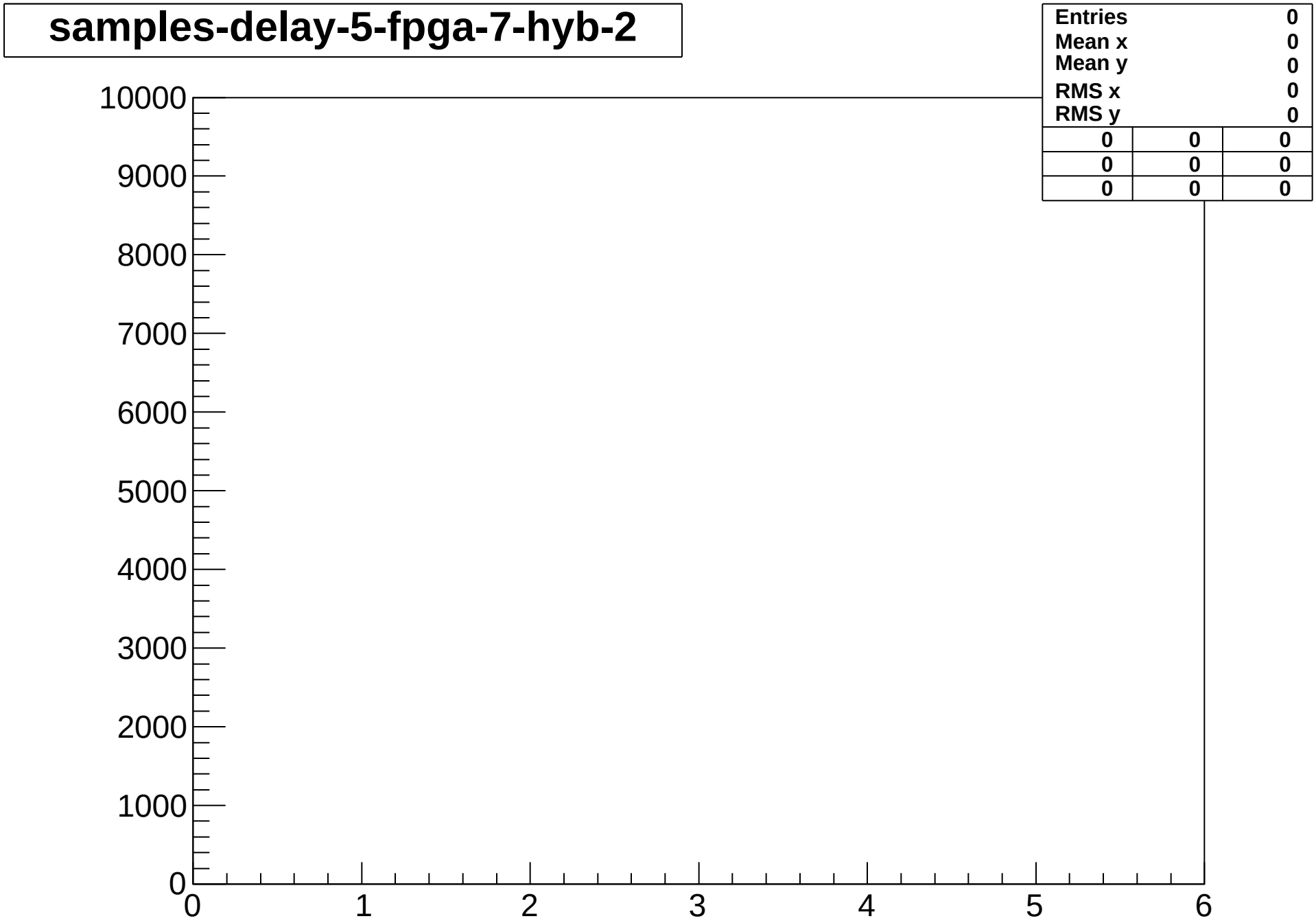
samples-delay-4-fpga-7-hyb-2




samples-delay-5-fpga-7-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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6000
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4000
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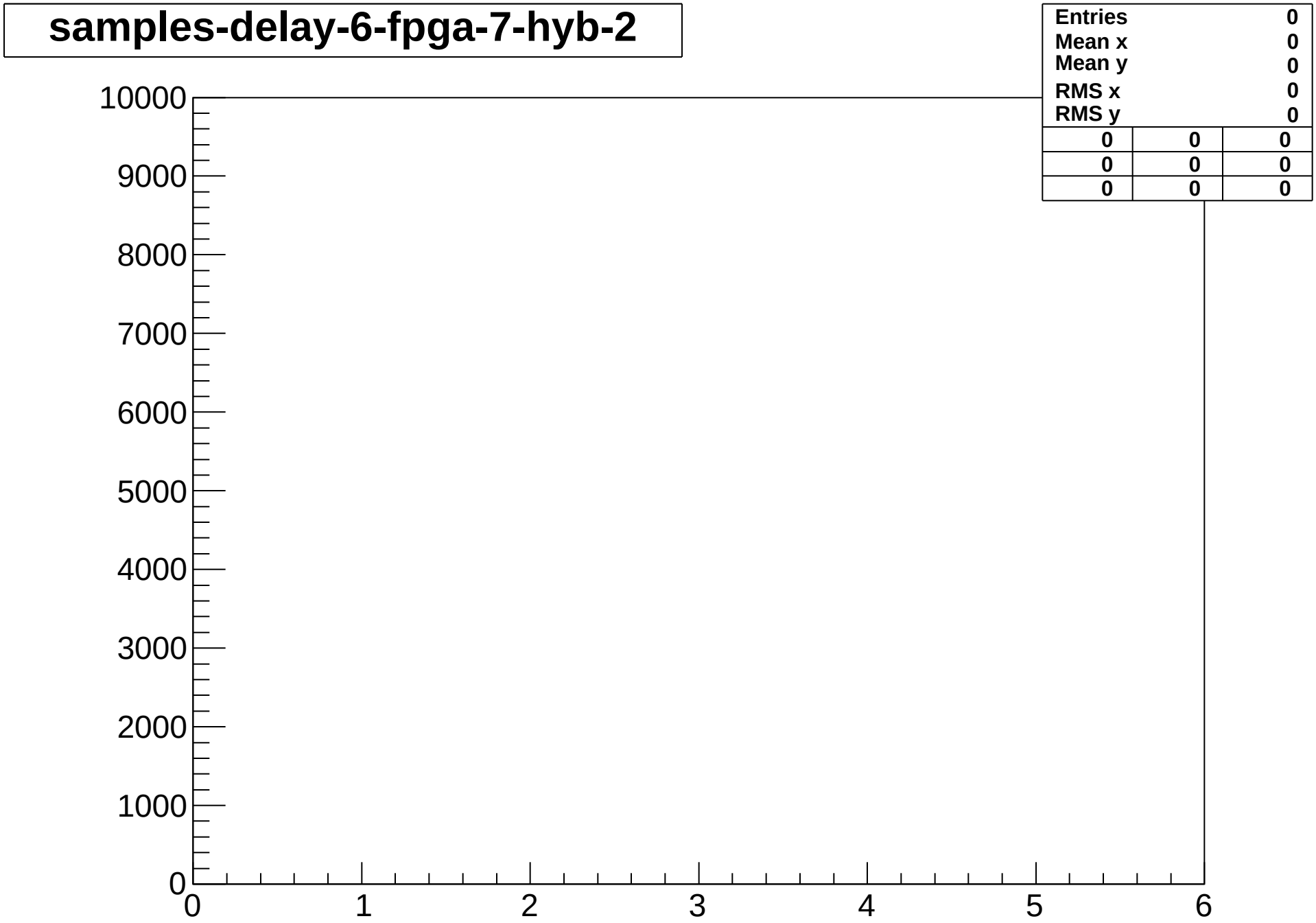
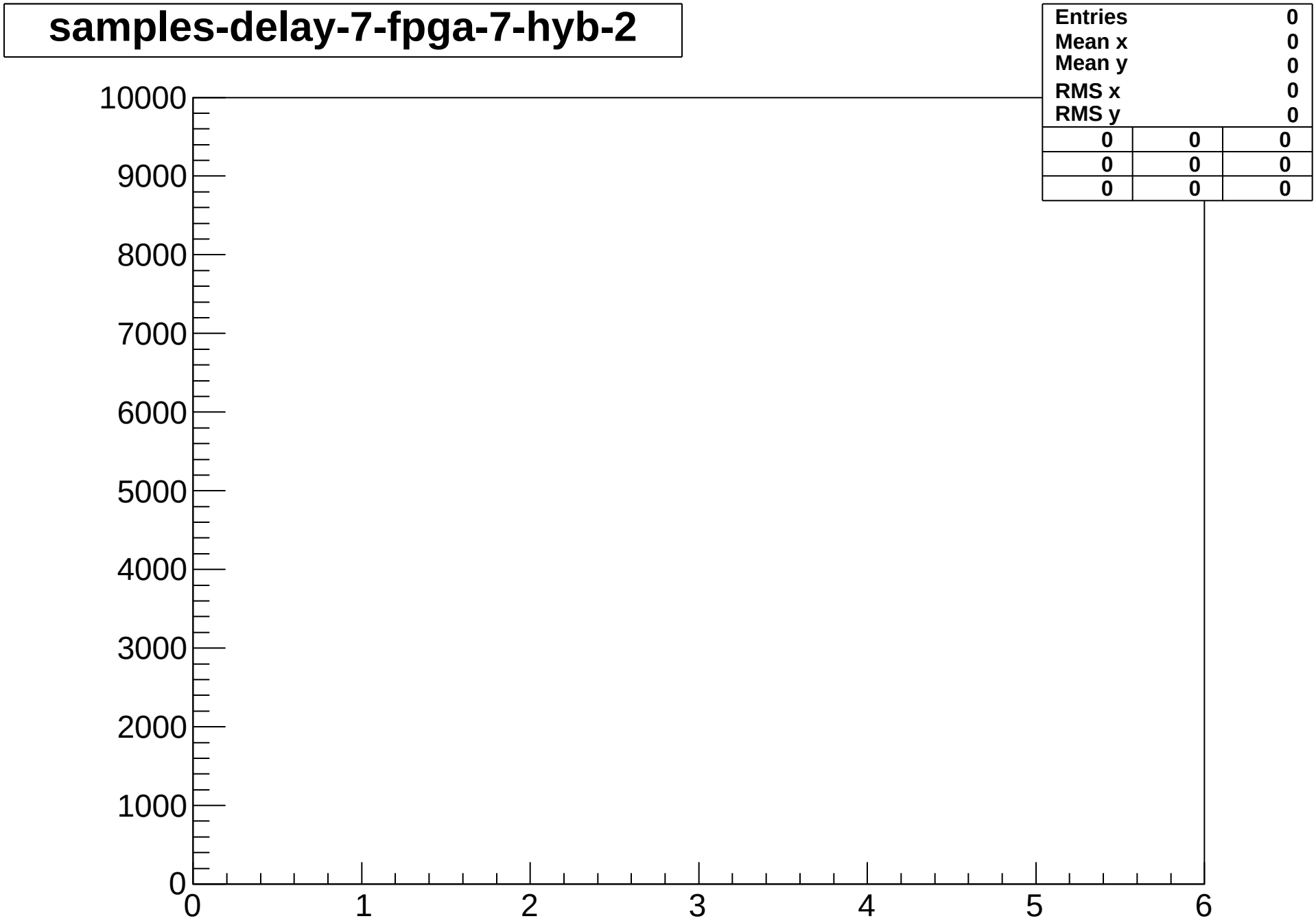
samples-delay-6-fpga-7-hyb-2




samples-delay-7-fpga-7-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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6000
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4000
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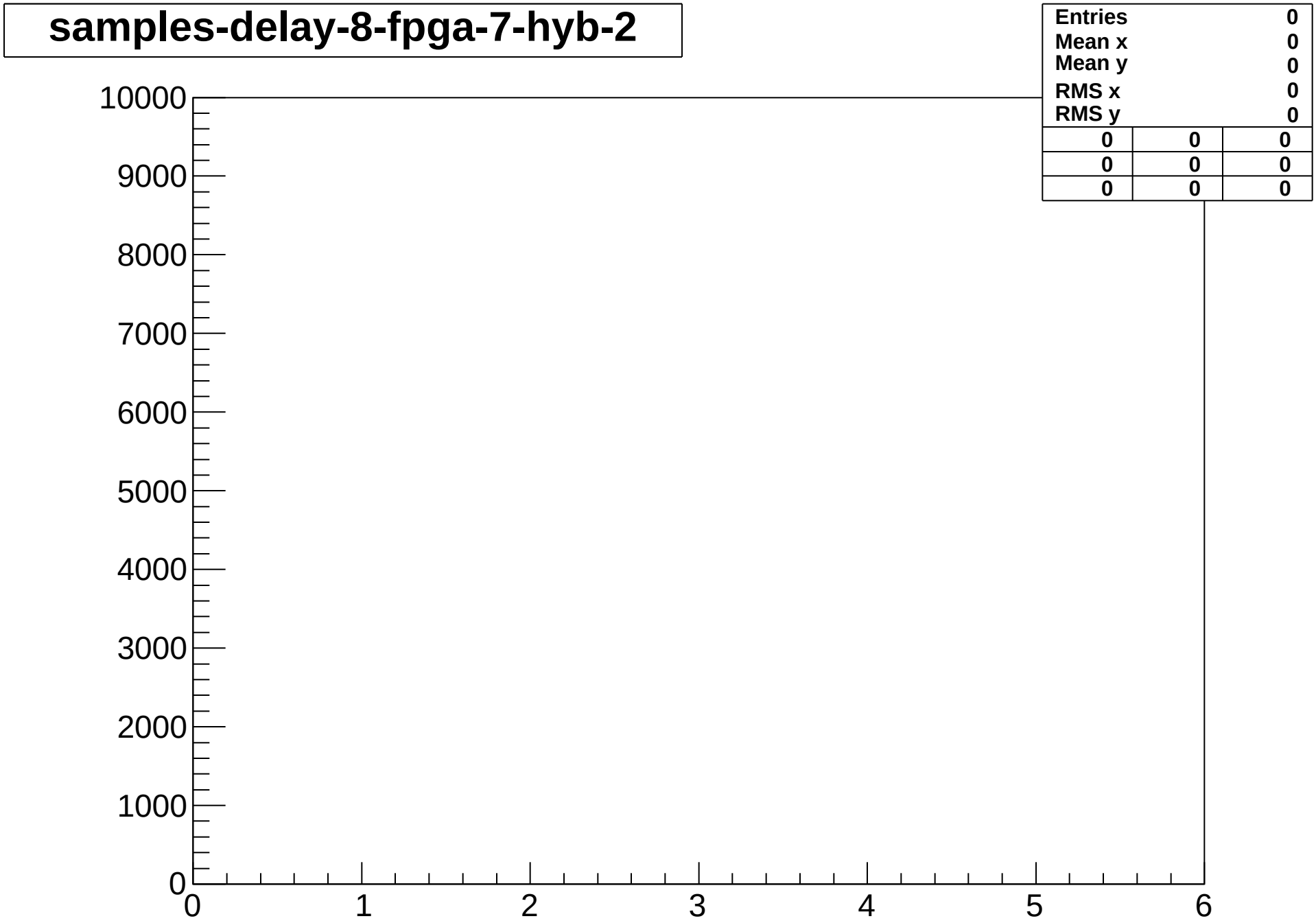
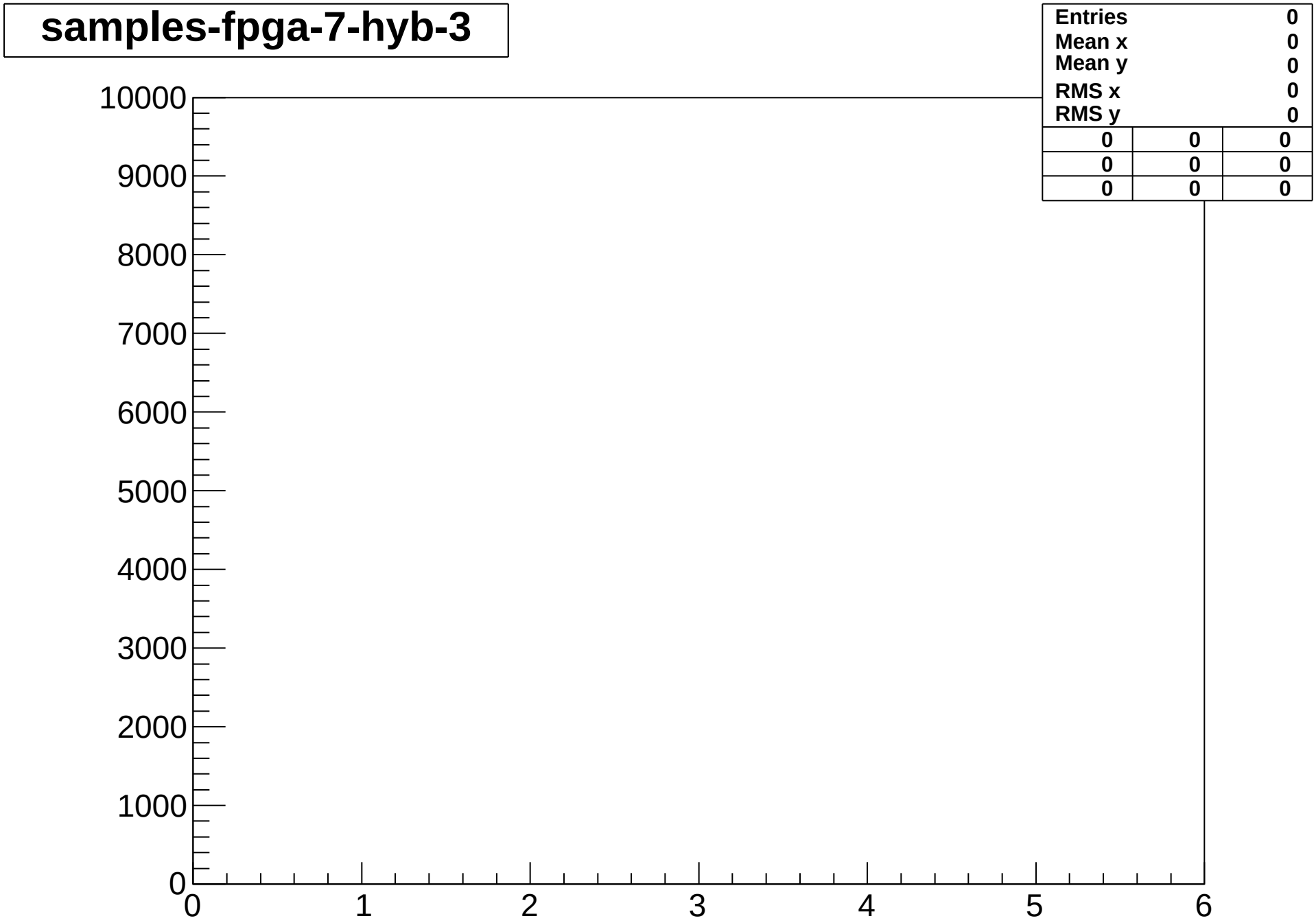
samples-delay-8-fpga-7-hyb-2




samples-fpga-7-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
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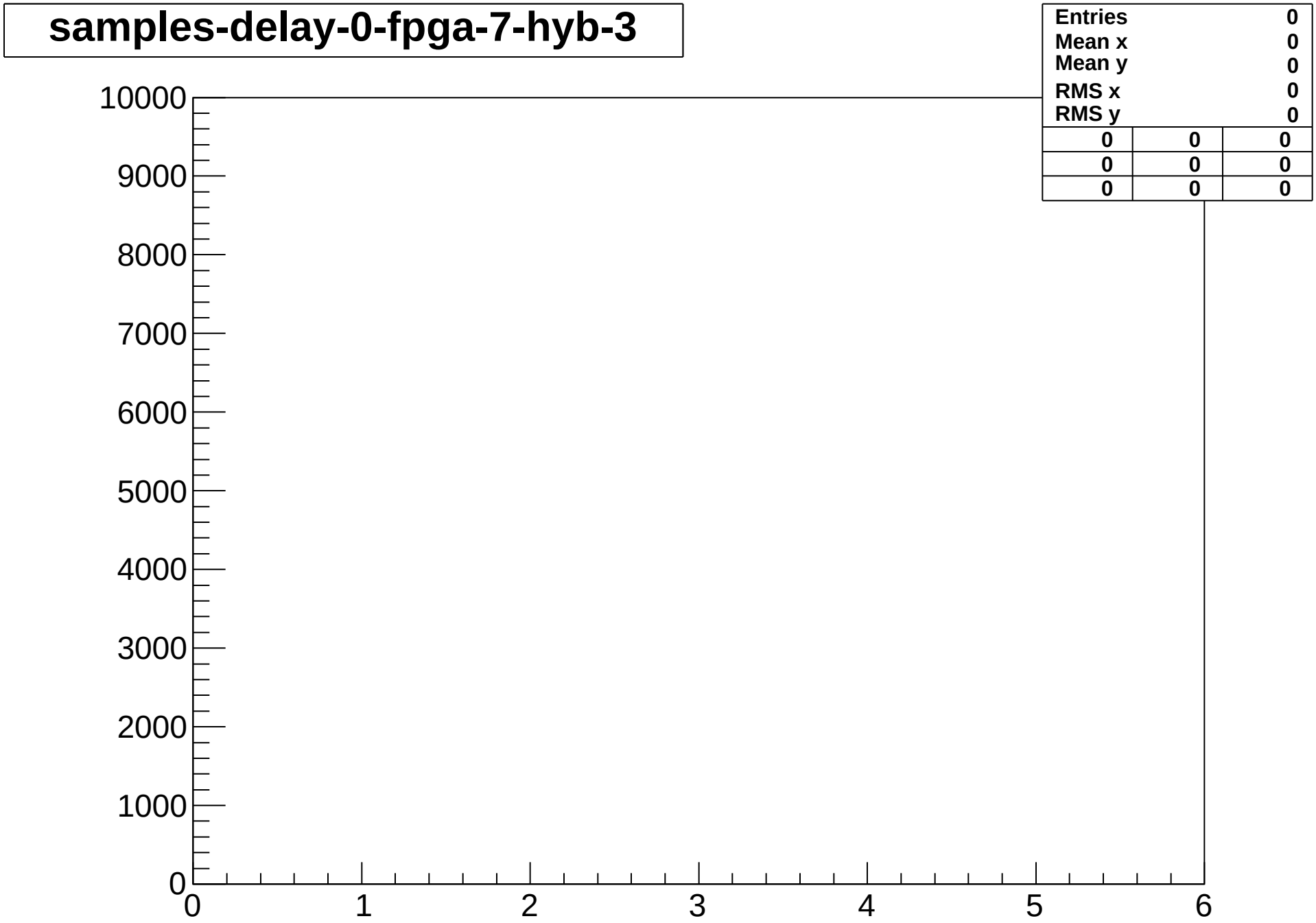
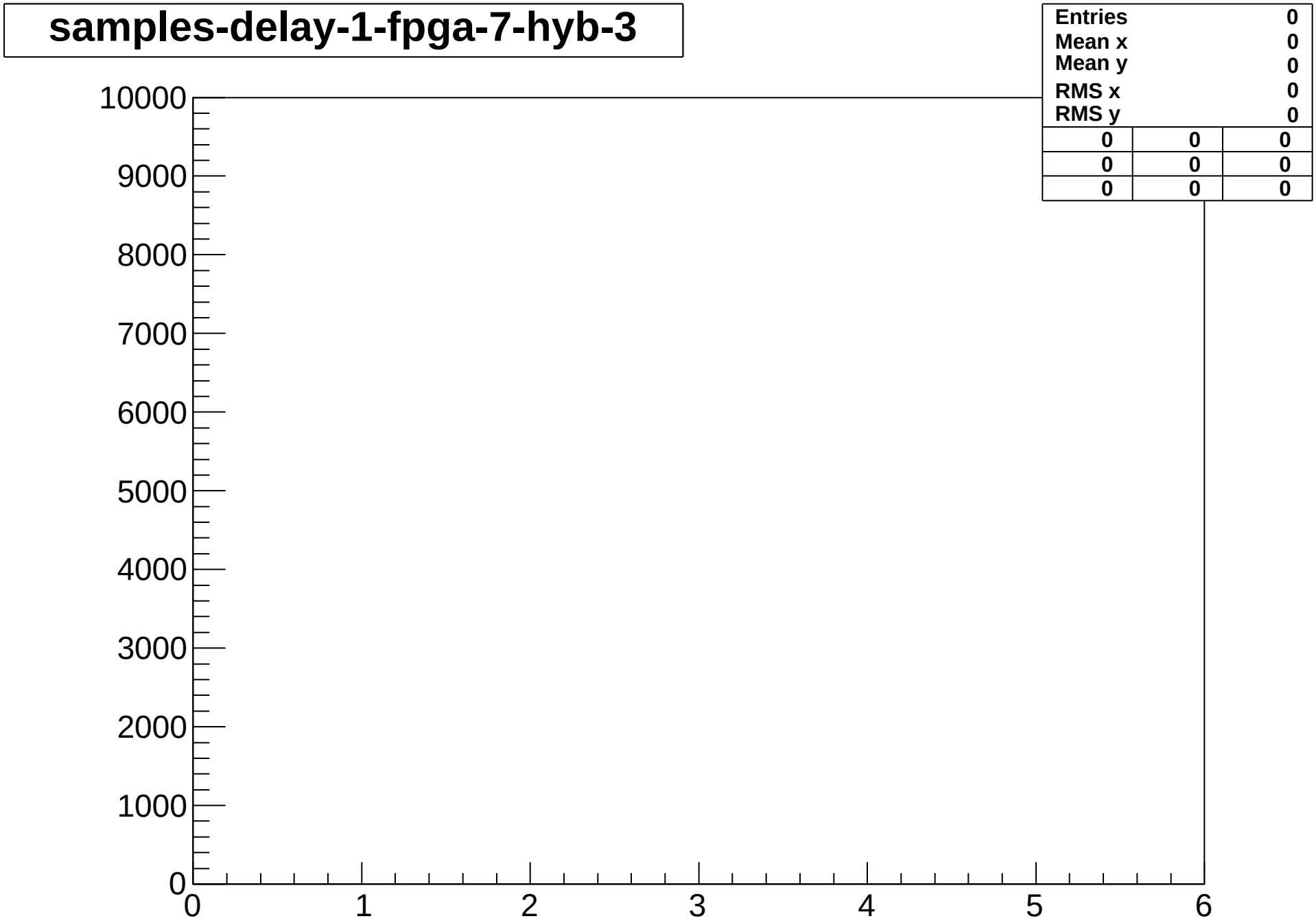
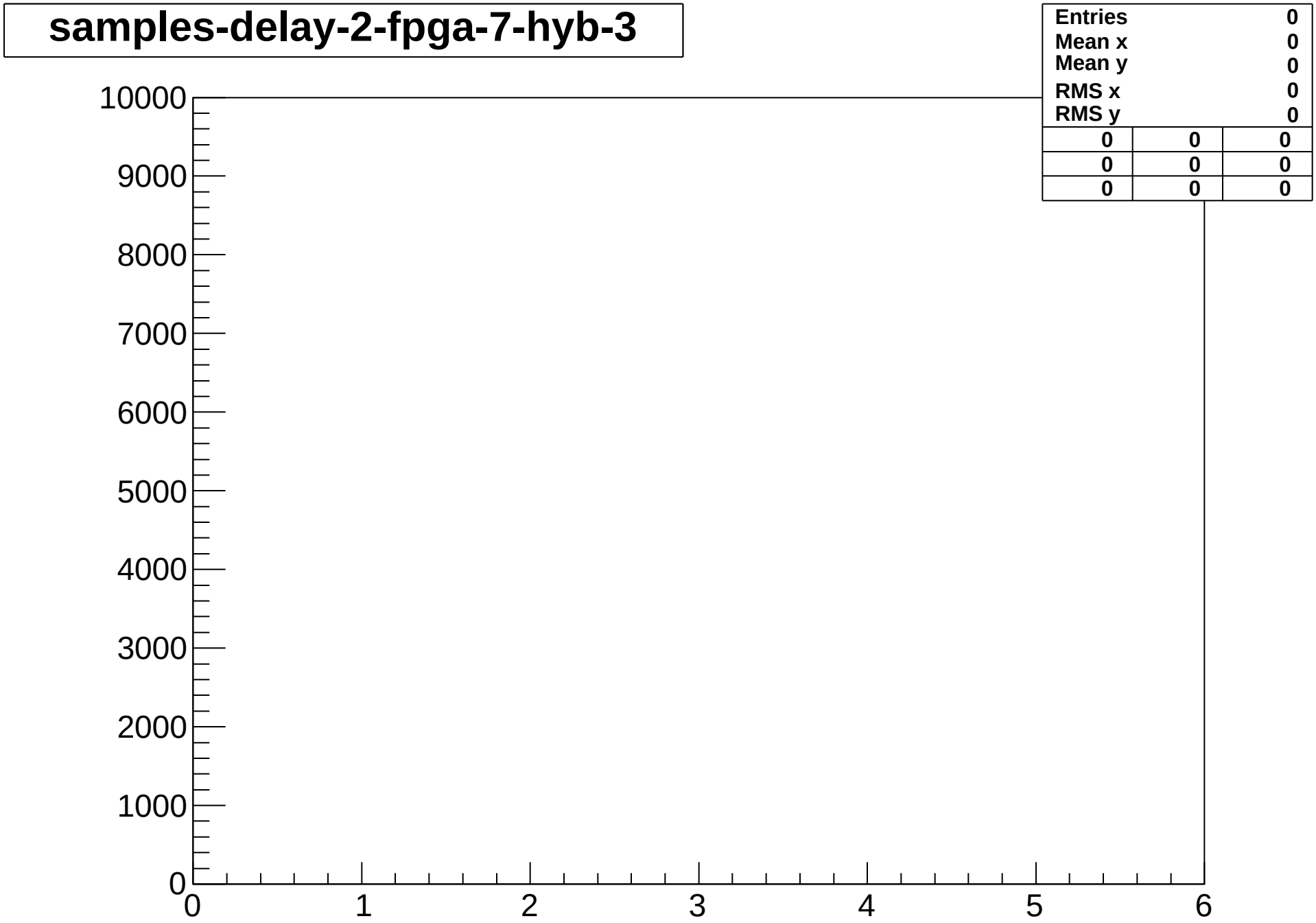
samples-delay-0-fpga-7-hyb-3



samples-delay-1-fpga-7-hyb-3




samples-delay-2-fpga-7-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
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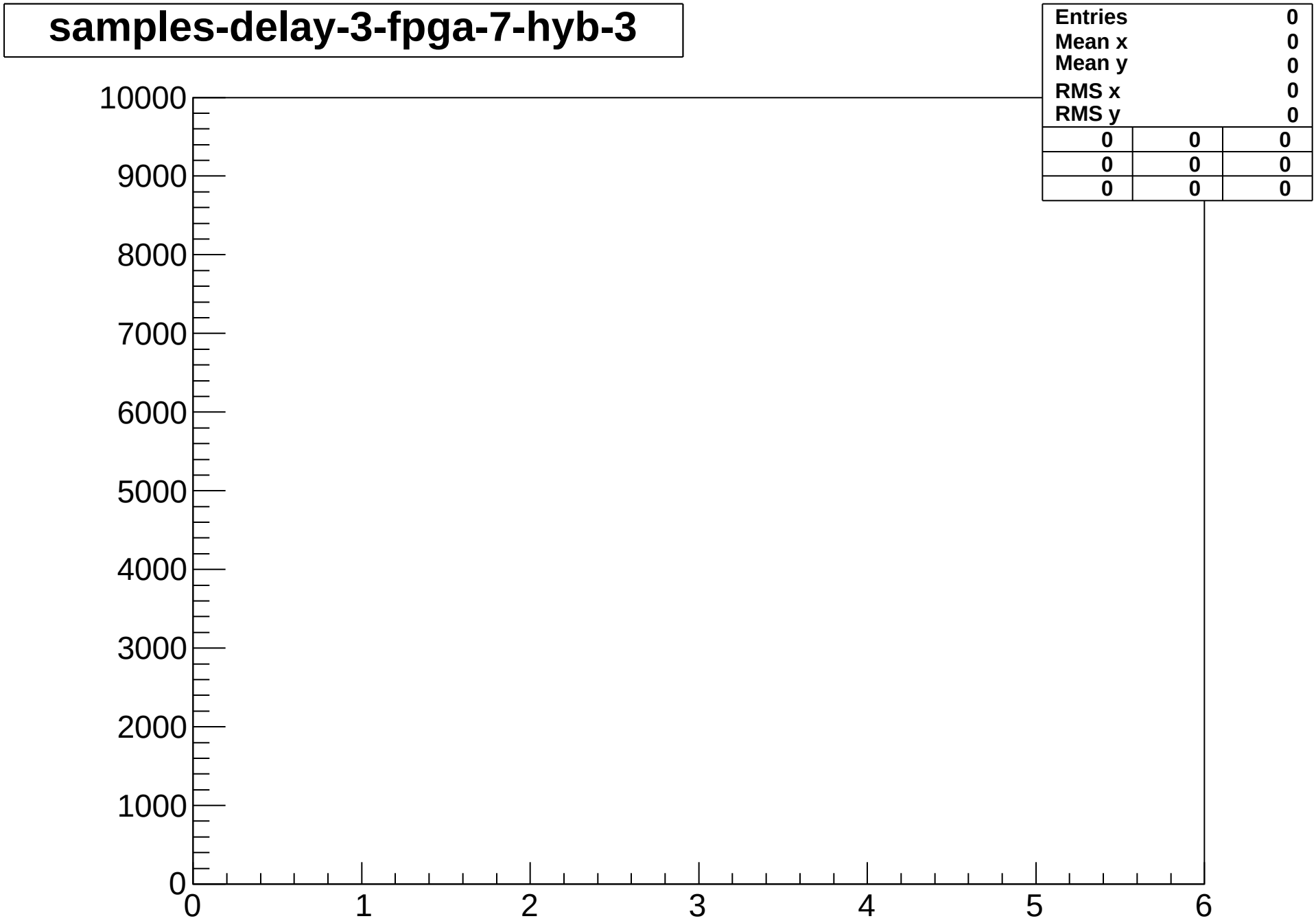
samples-delay-3-fpga-7-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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6000
5000
4000
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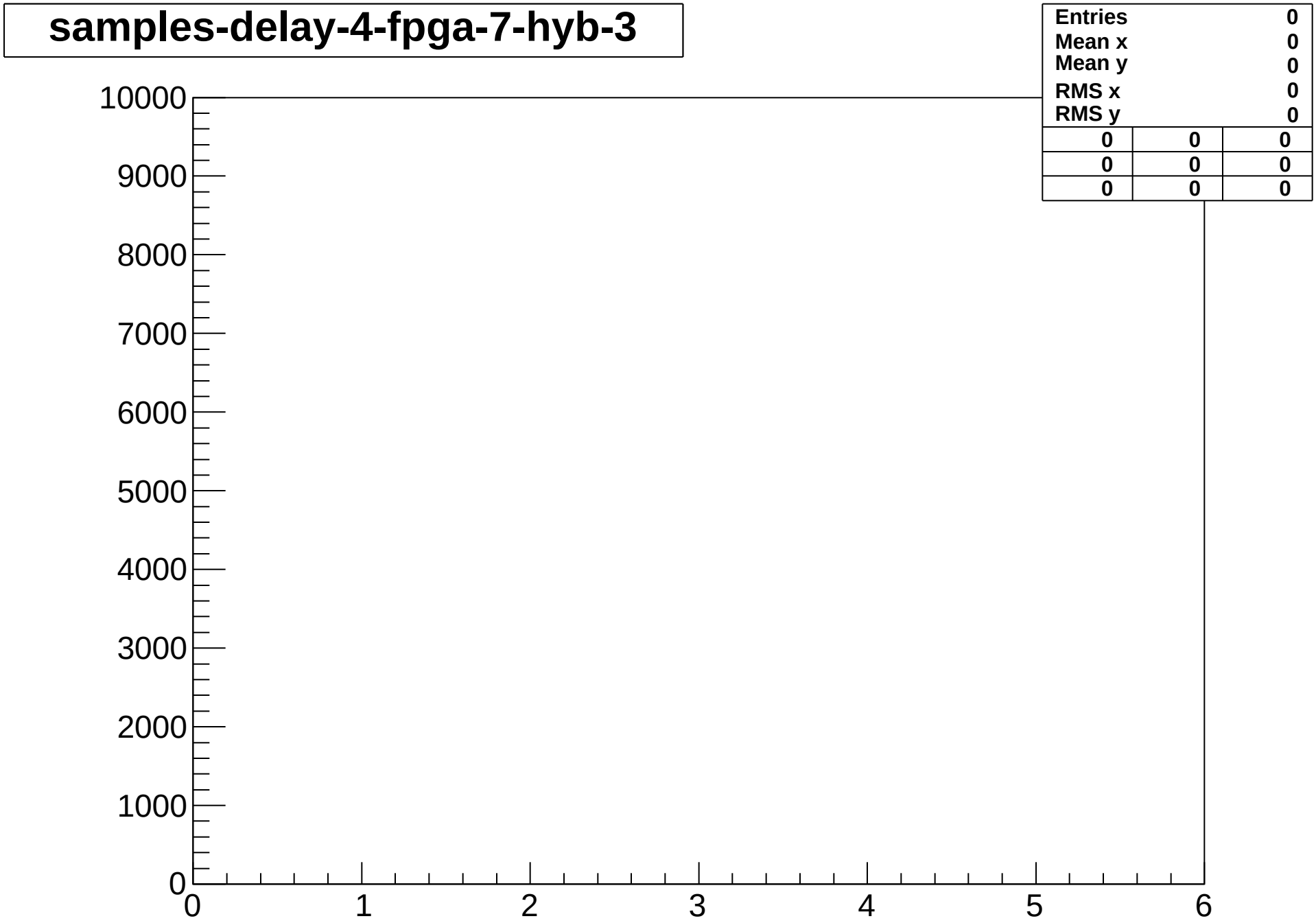
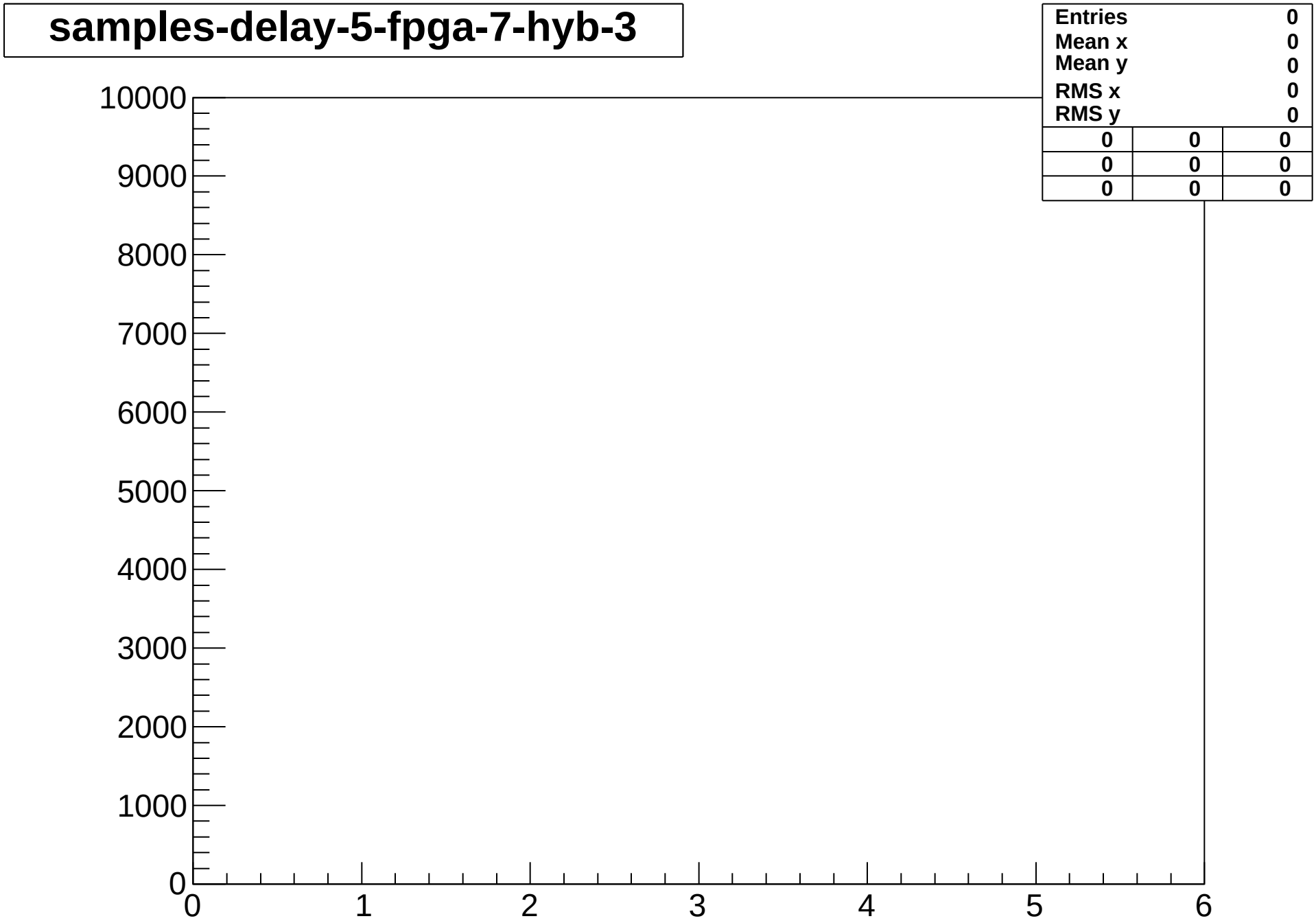
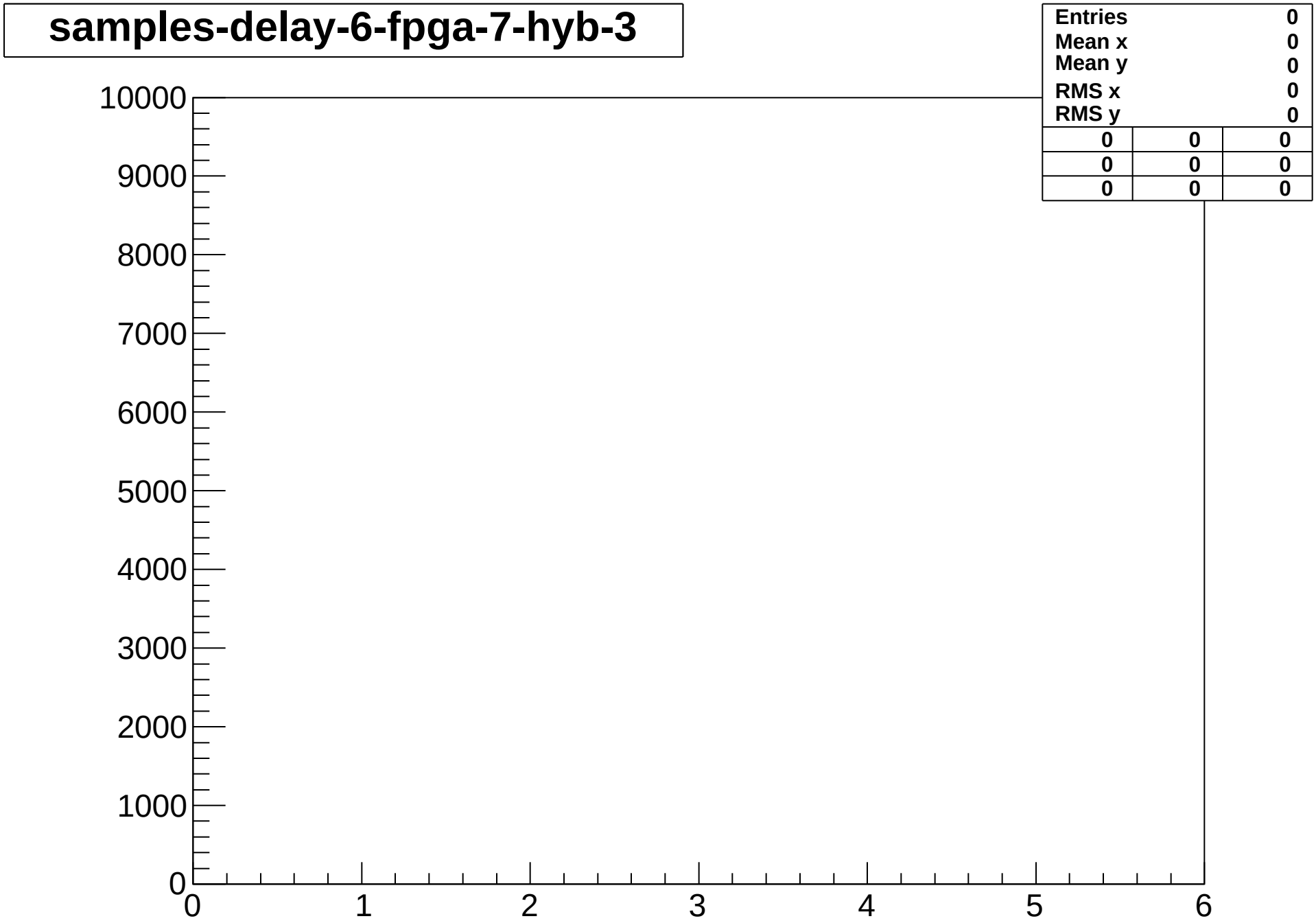
samples-delay-4-fpga-7-hyb-3



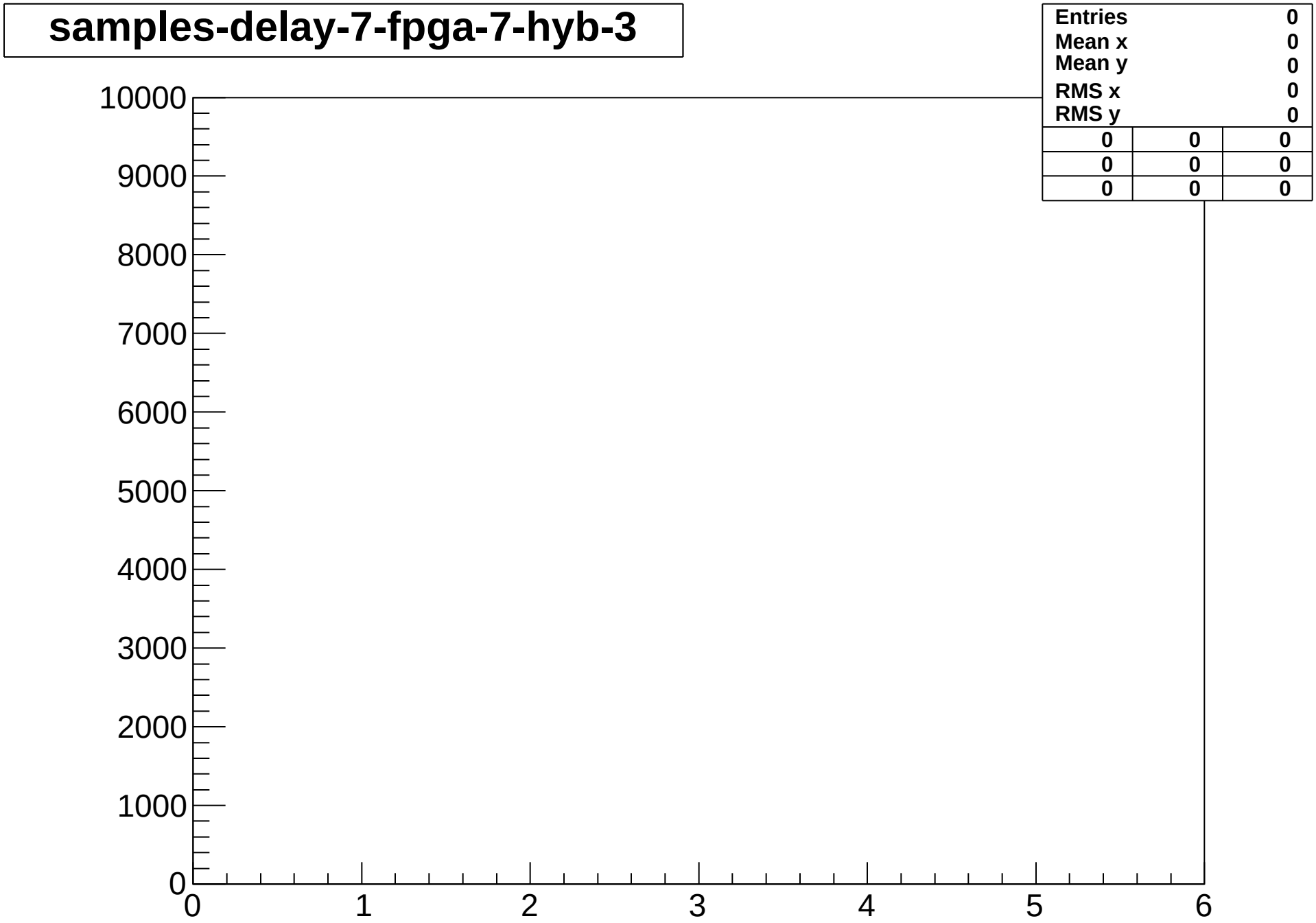
samples-delay-5-fpga-7-hyb-3

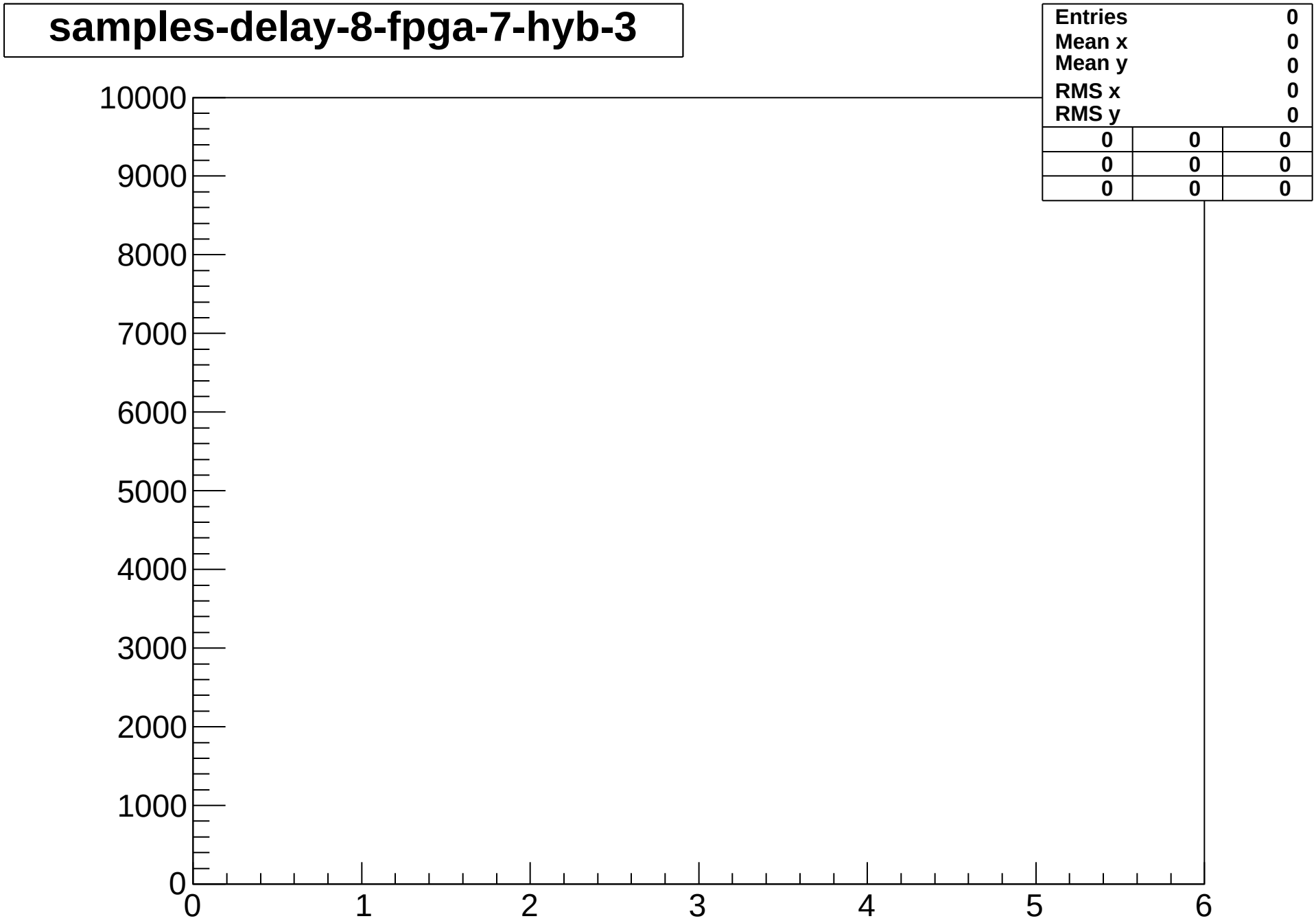


samples-delay-6-fpga-7-hyb-3



samples-delay-7-fpga-7-hyb-3




samples-delay-8-fpga-7-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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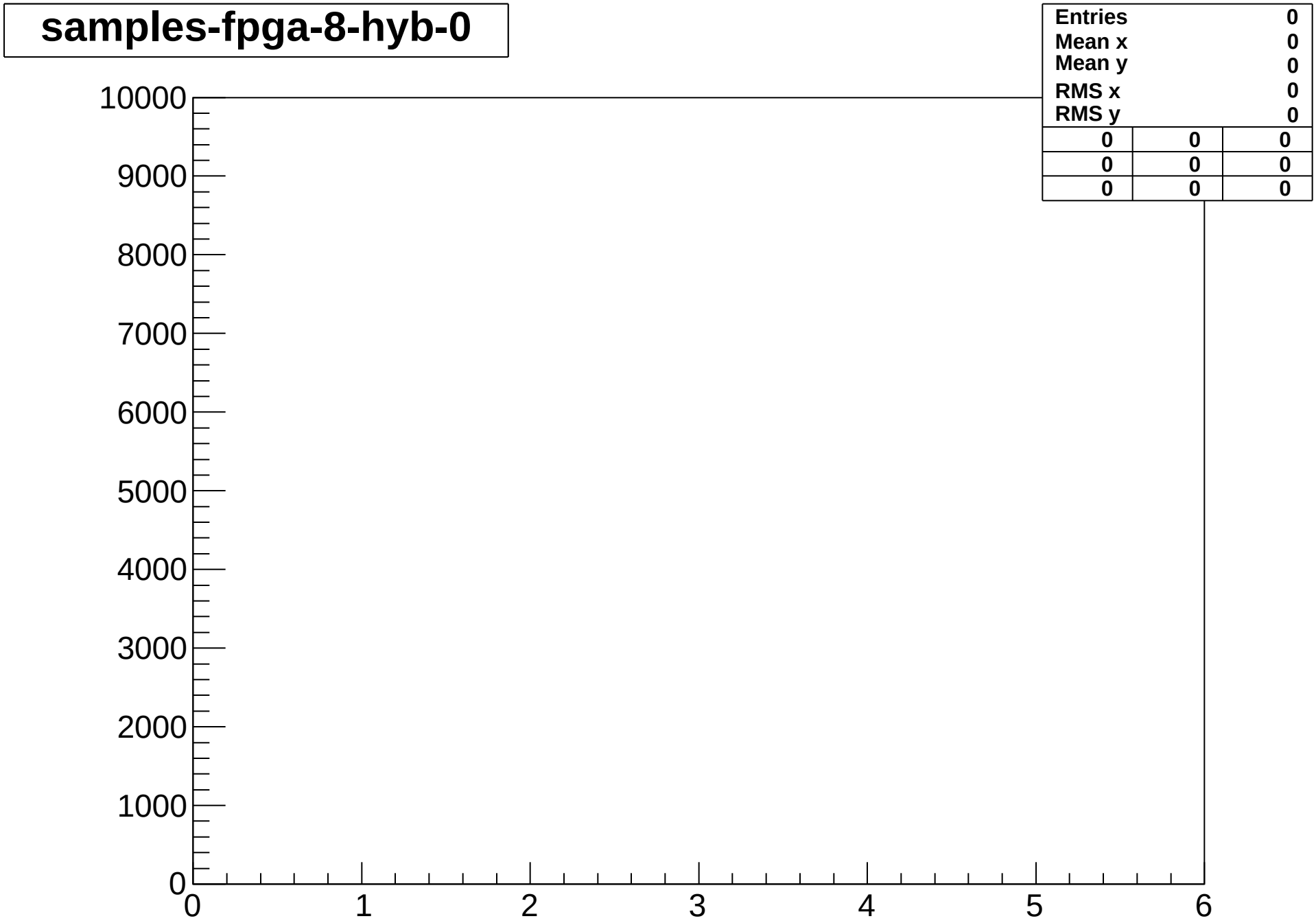
samples-fpga-8-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
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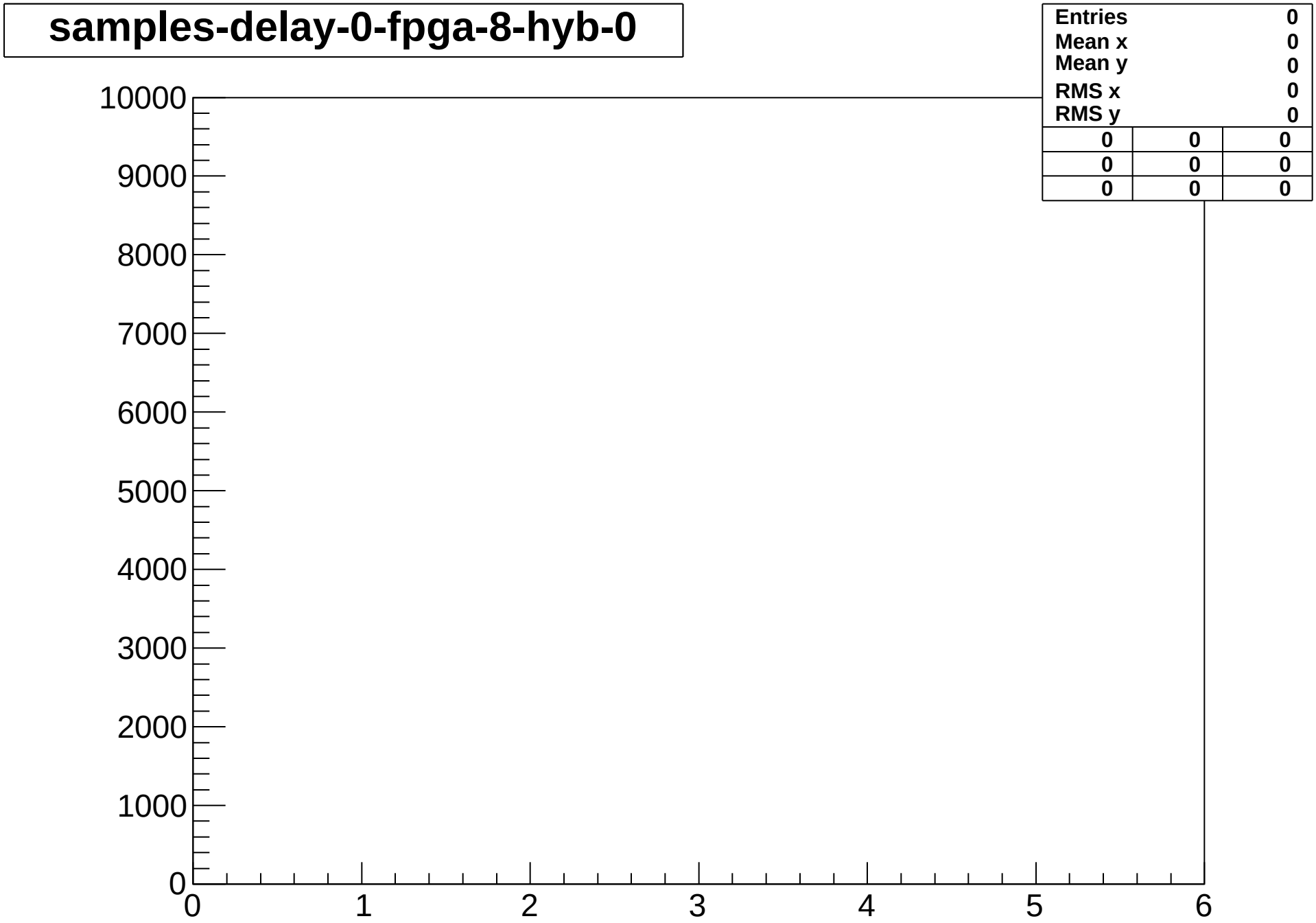
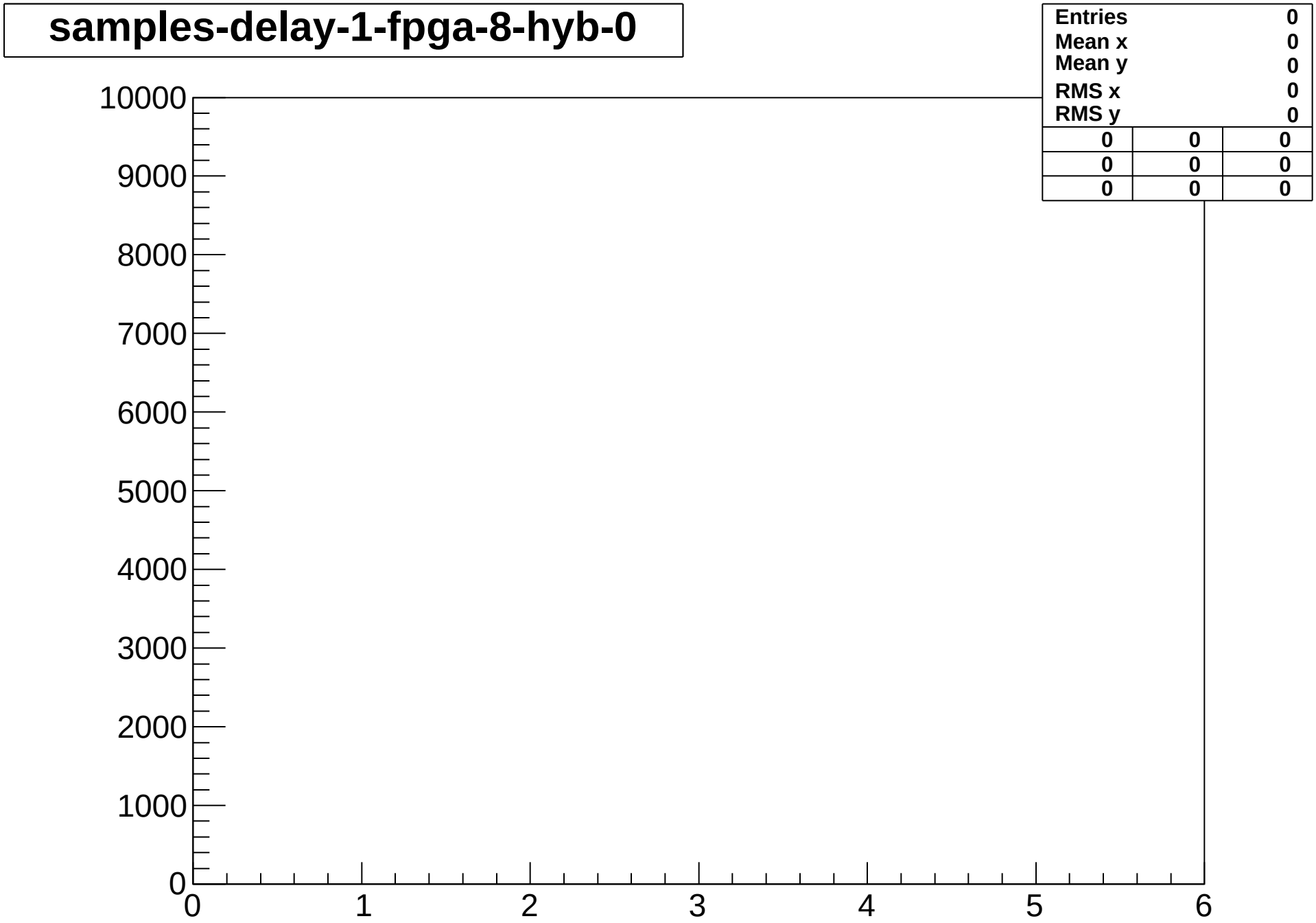

samples-delay-0-fpga-8-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
5
6


samples-delay-1-fpga-8-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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8000
7000
6000
5000
4000
3000
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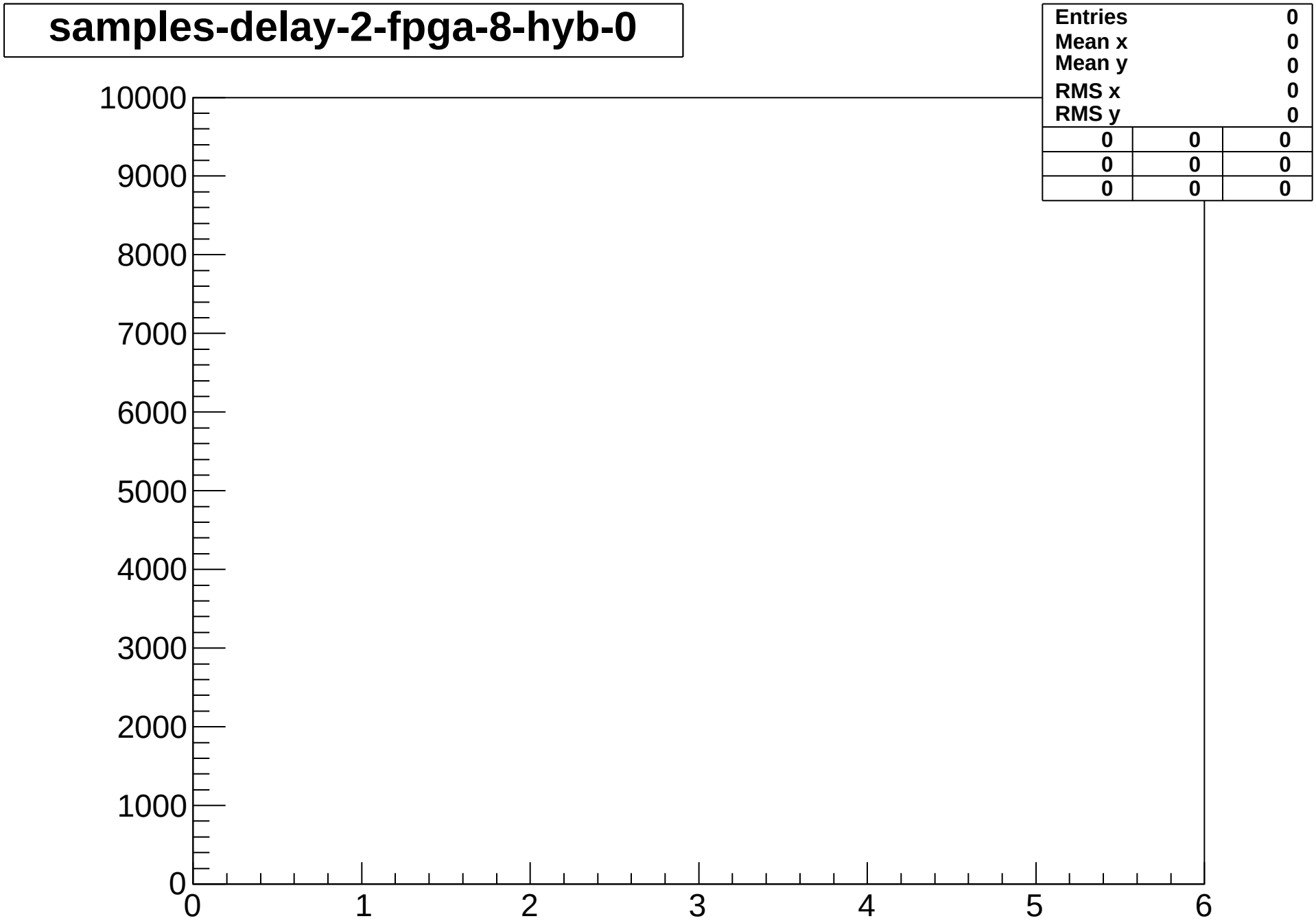
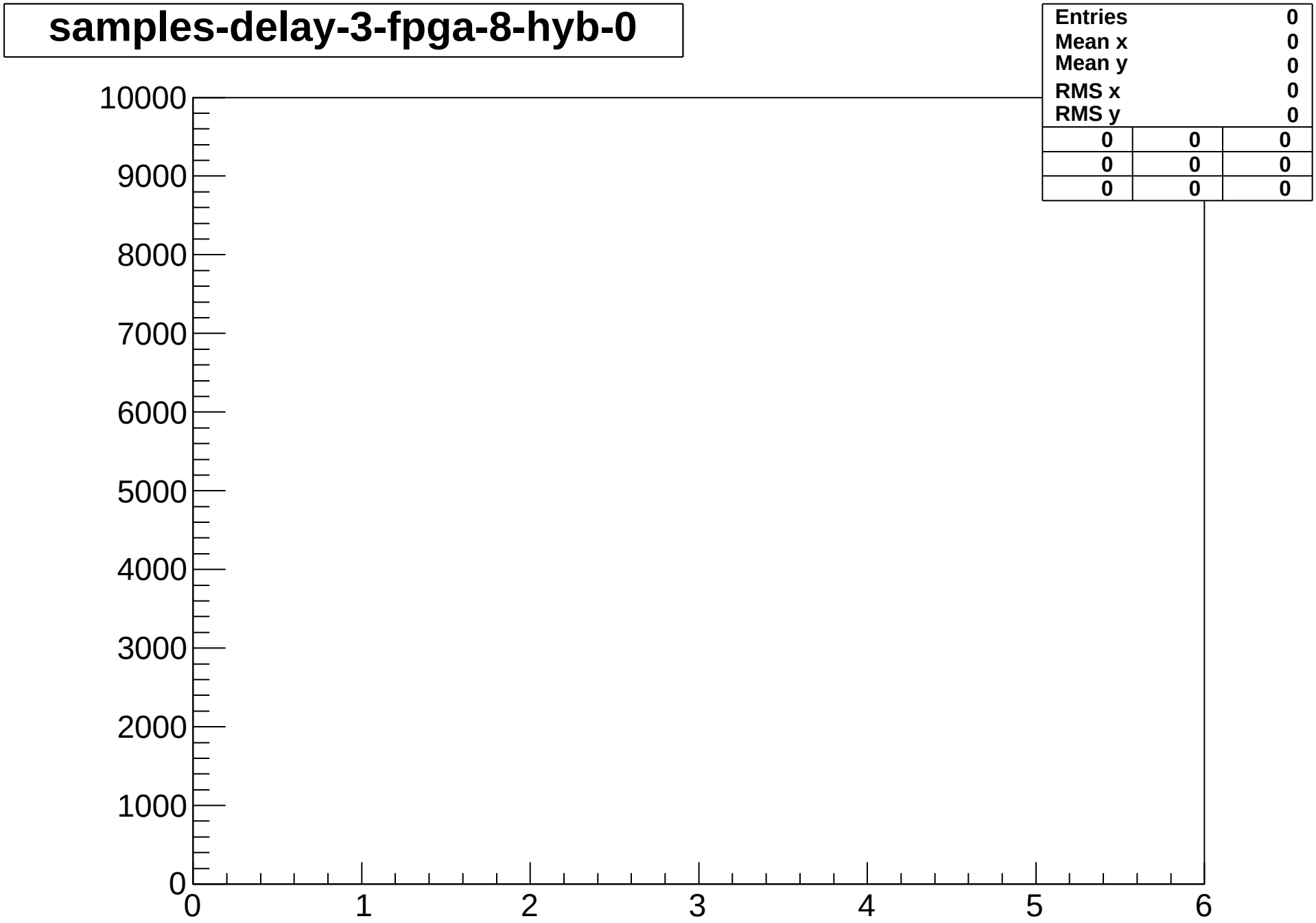
samples-delay-2-fpga-8-hyb-0




samples-delay-3-fpga-8-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
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4
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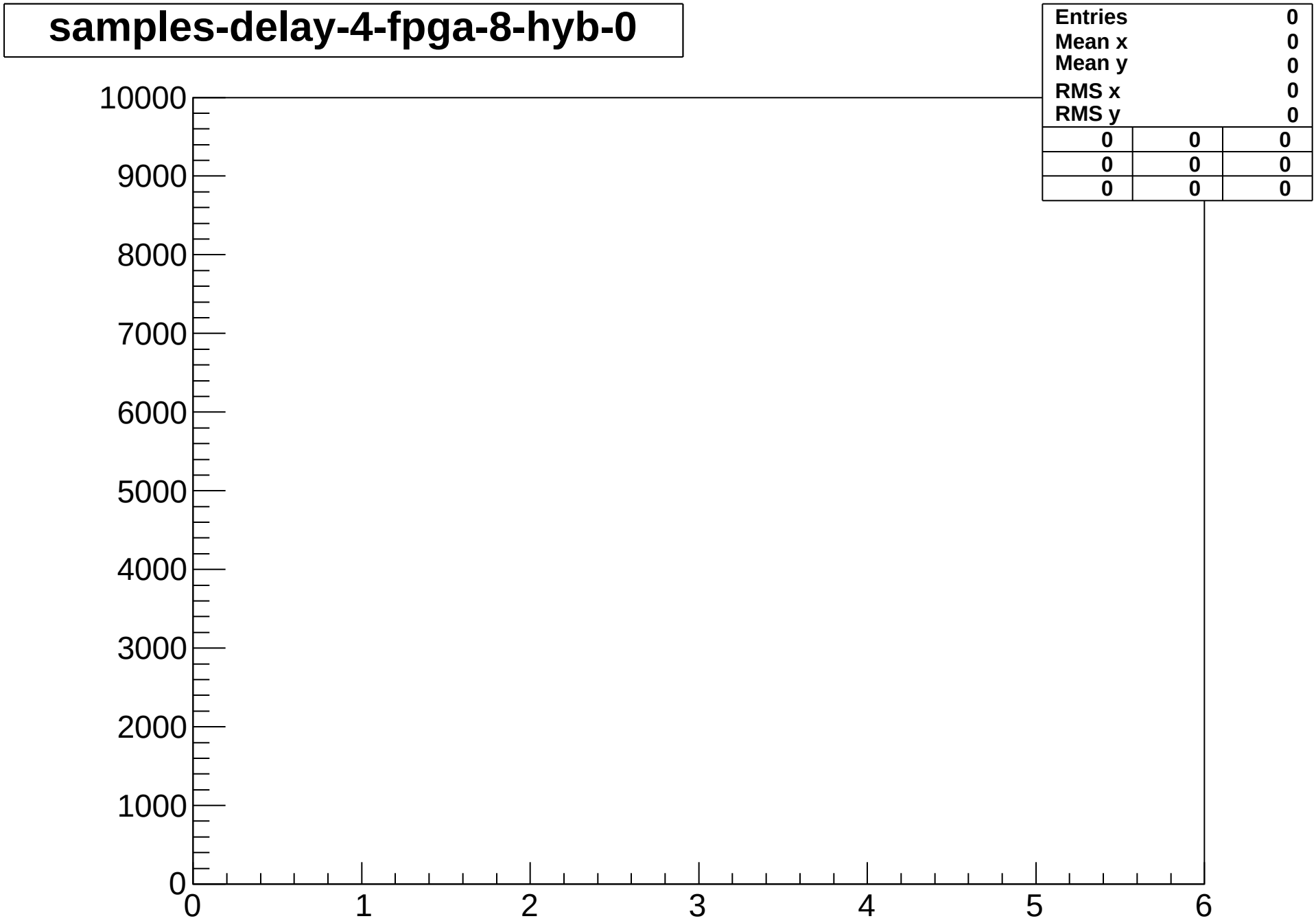
samples-delay-4-fpga-8-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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7000
6000
5000
4000
3000
2000
1000
0
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1
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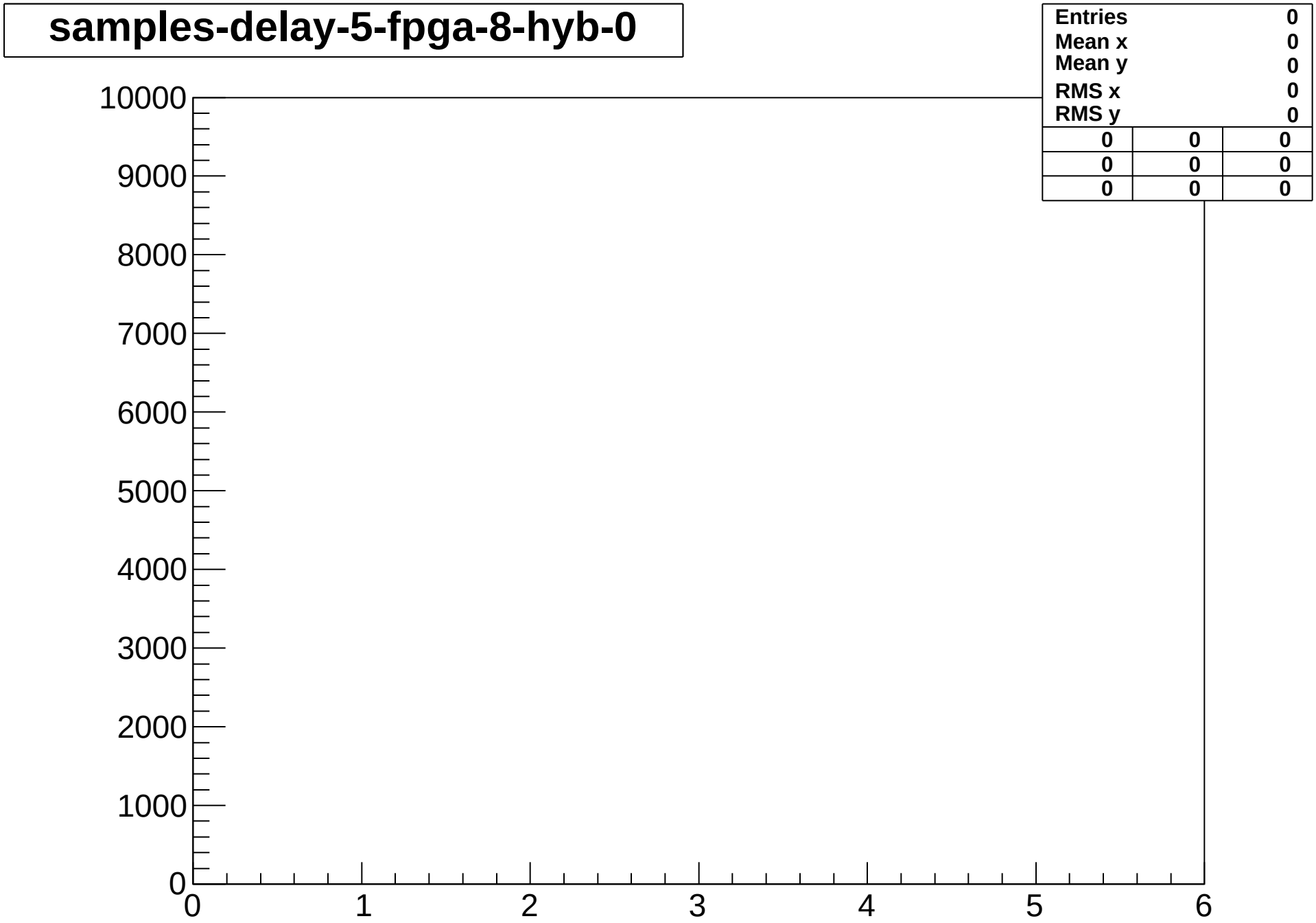
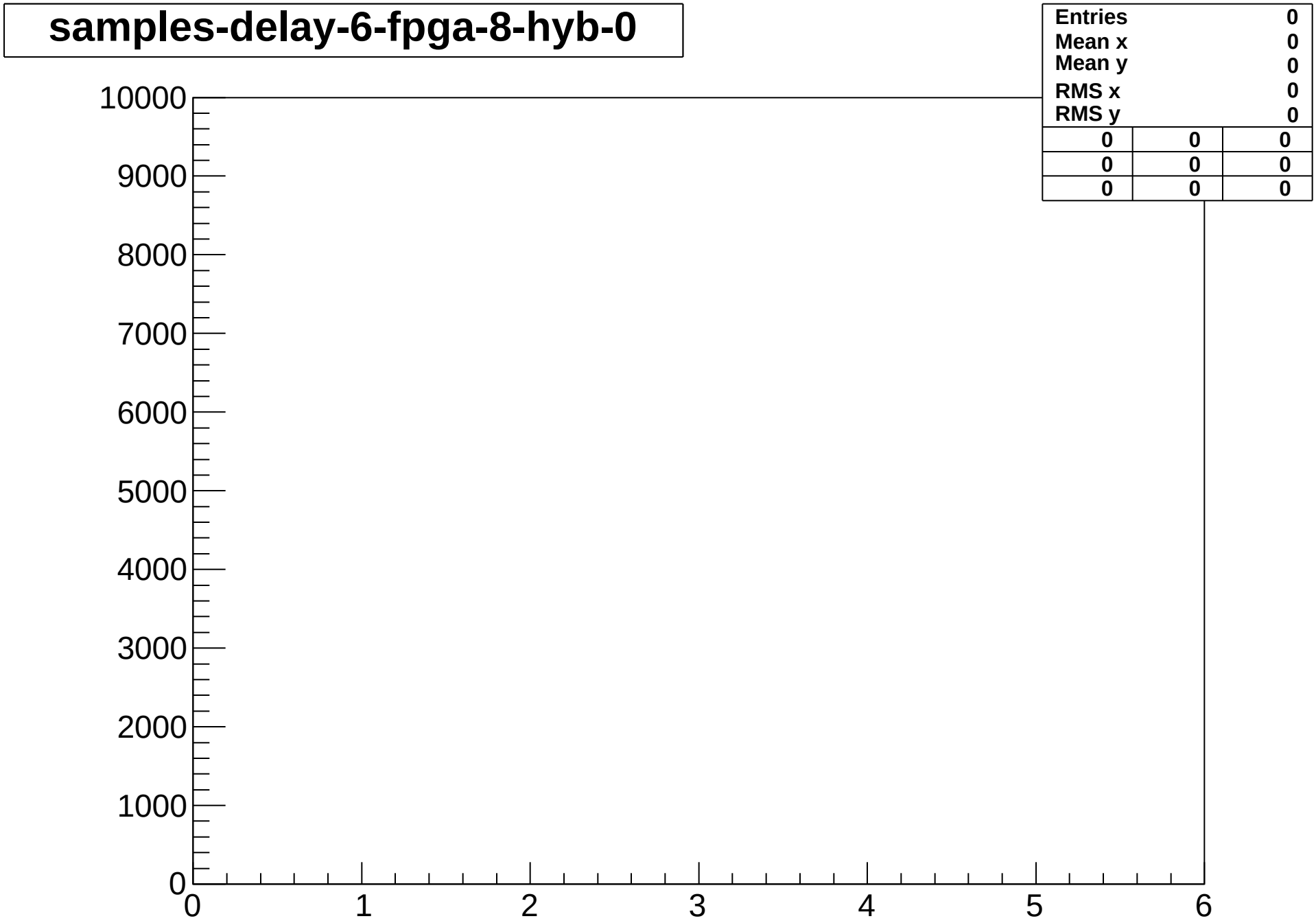
samples-delay-5-fpga-8-hyb-0




samples-delay-6-fpga-8-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
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0
1
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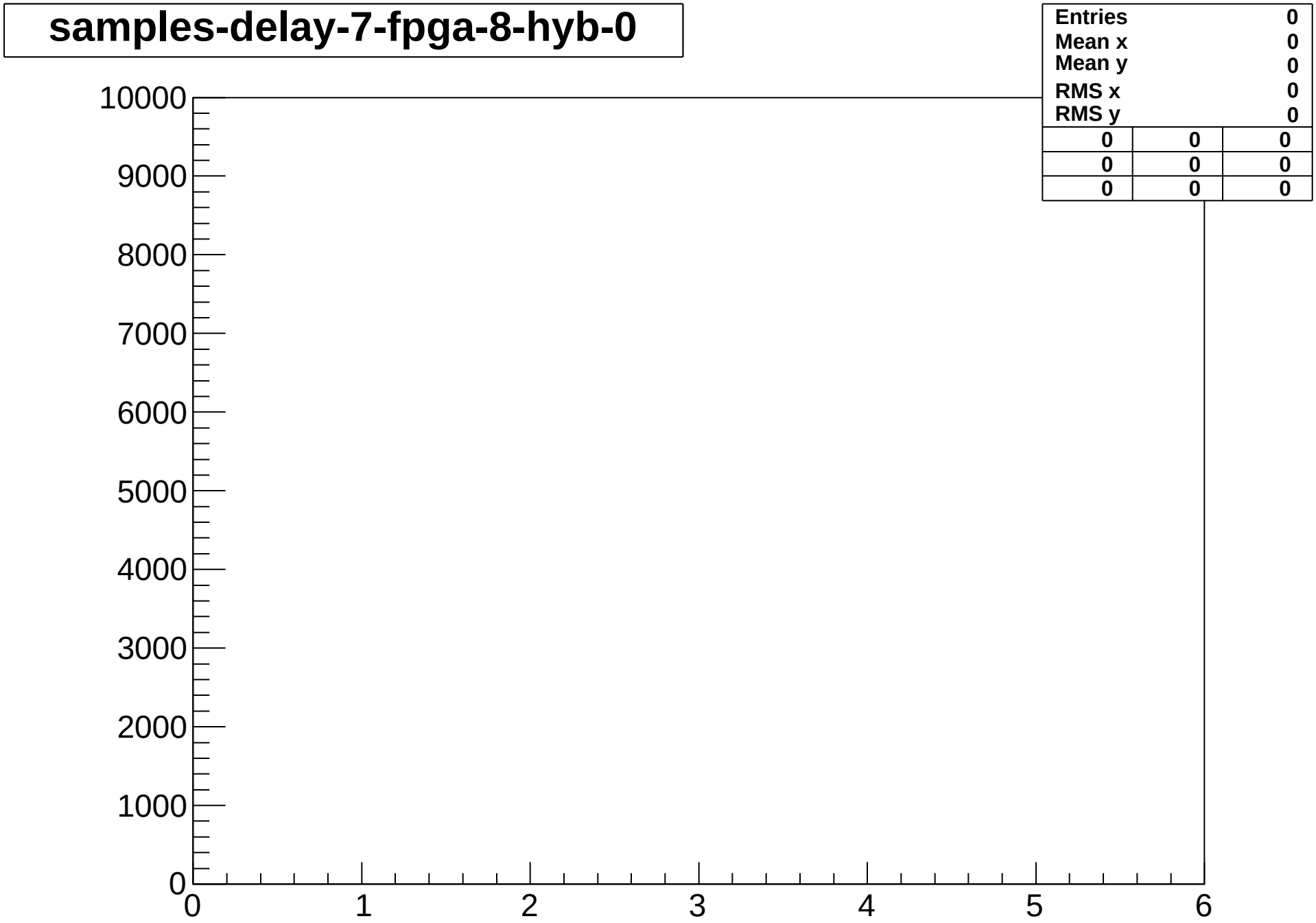
samples-delay-7-fpga-8-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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5000
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3000
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0
1
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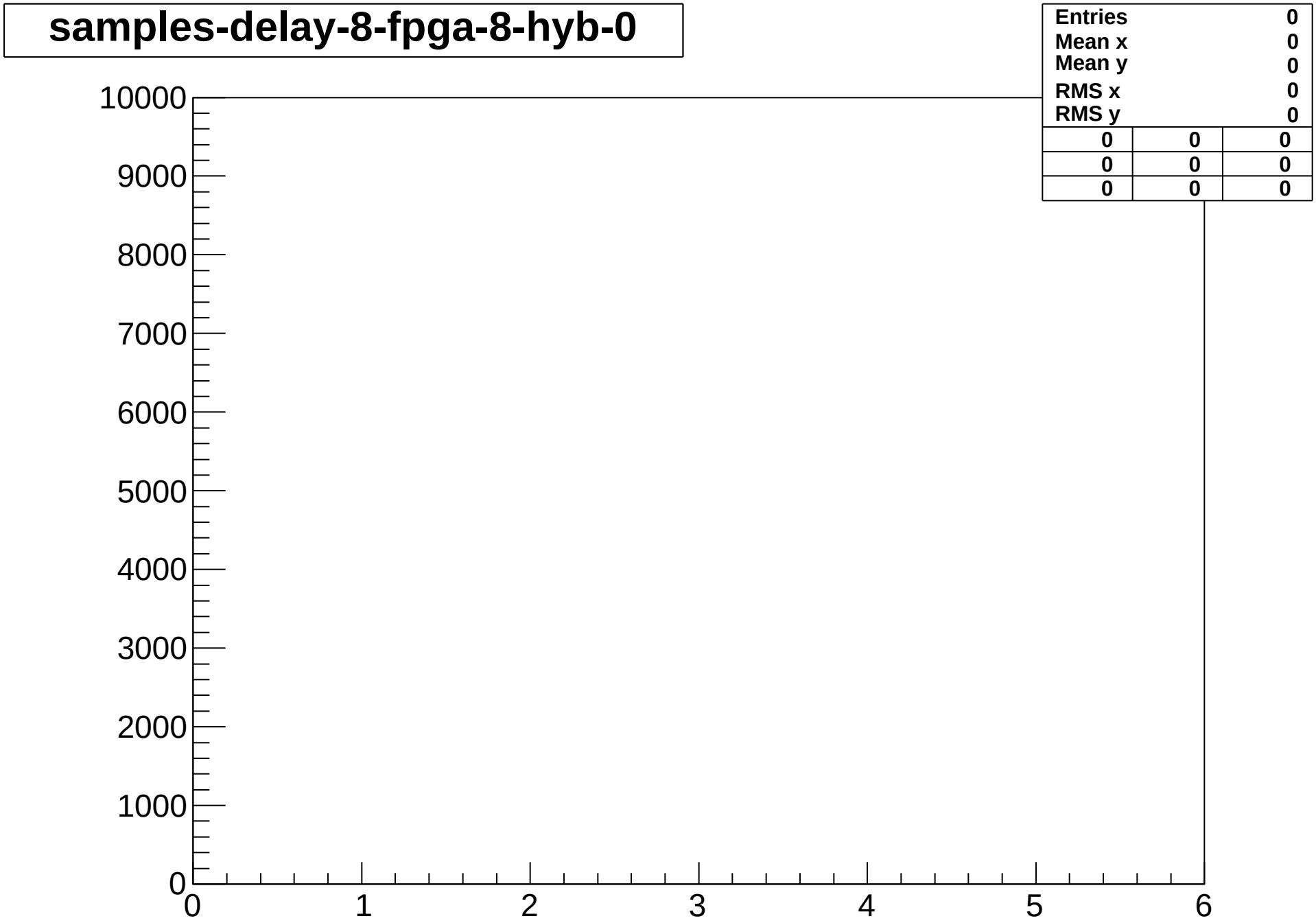
samples-delay-8-fpga-8-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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3000
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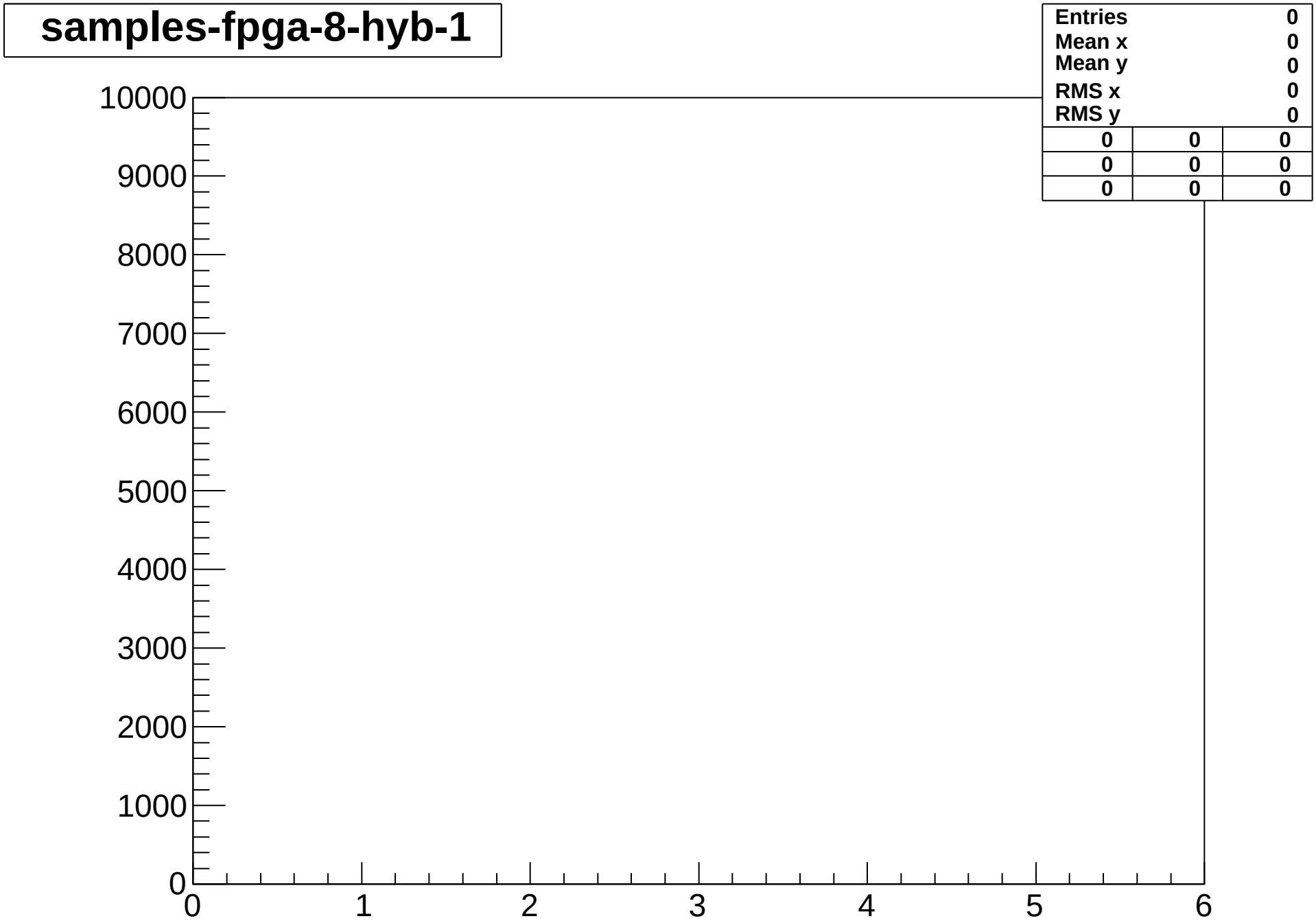
samples-fpga-8-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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3000
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1
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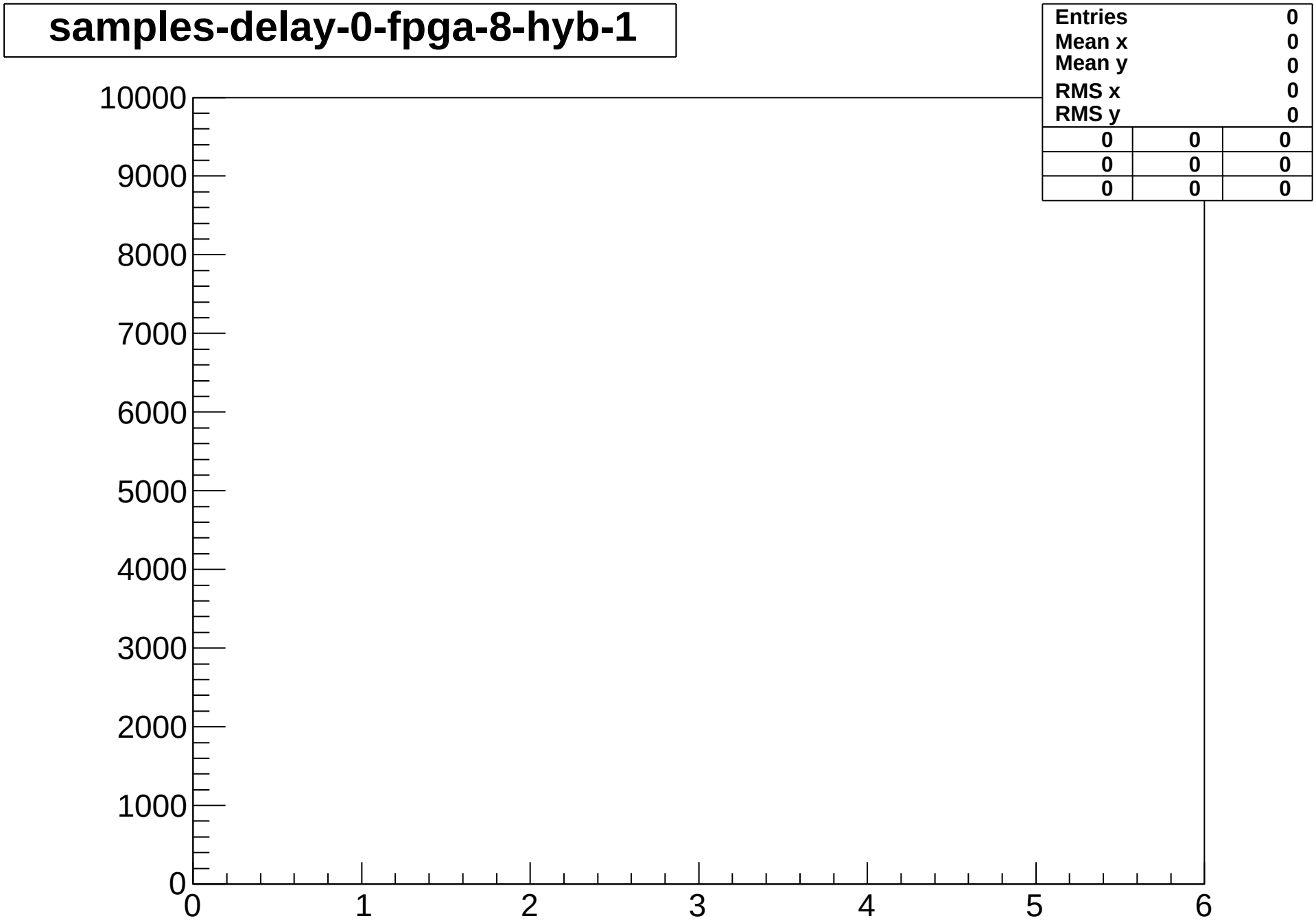
samples-delay-0-fpga-8-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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6000
5000
4000
3000
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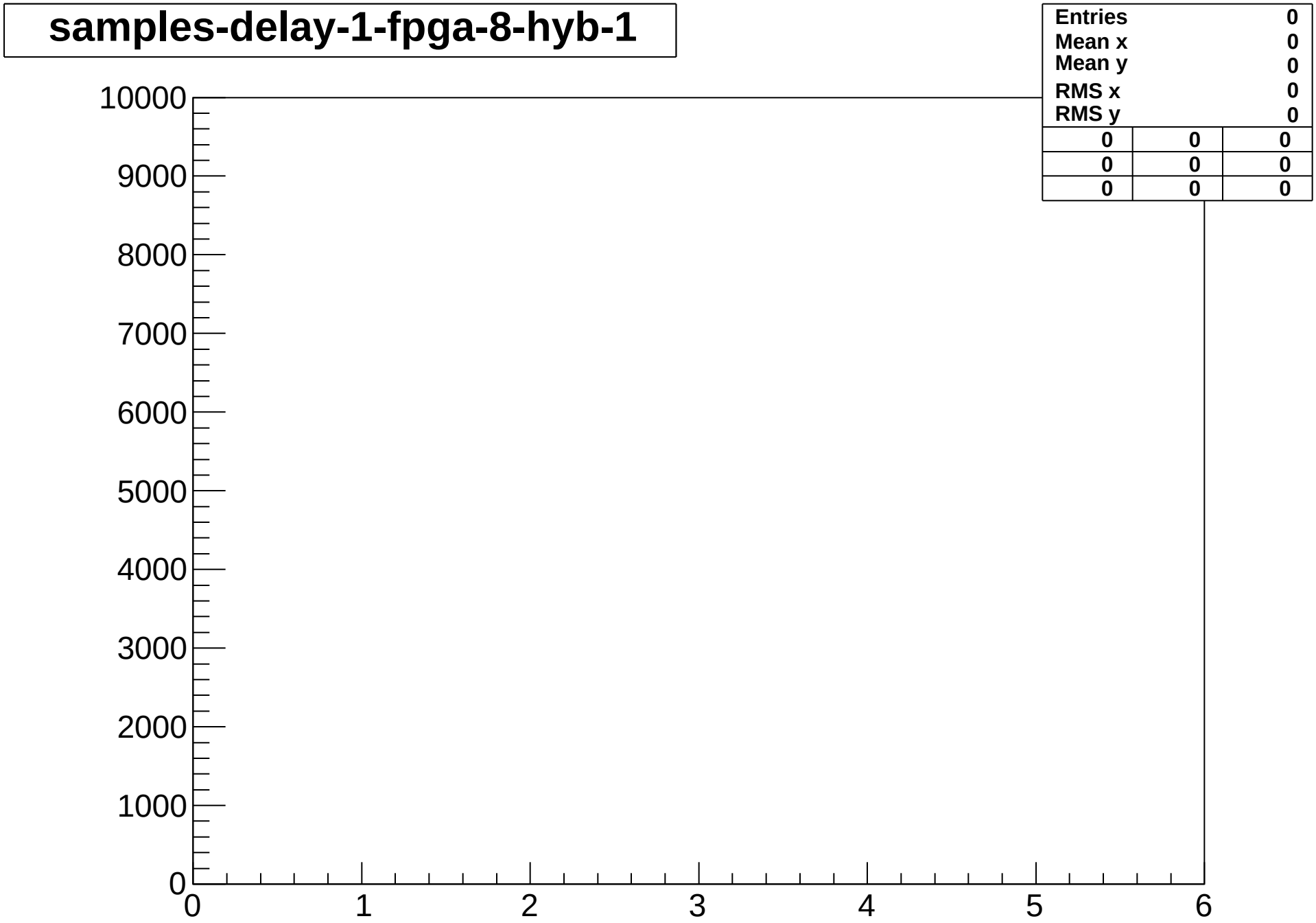
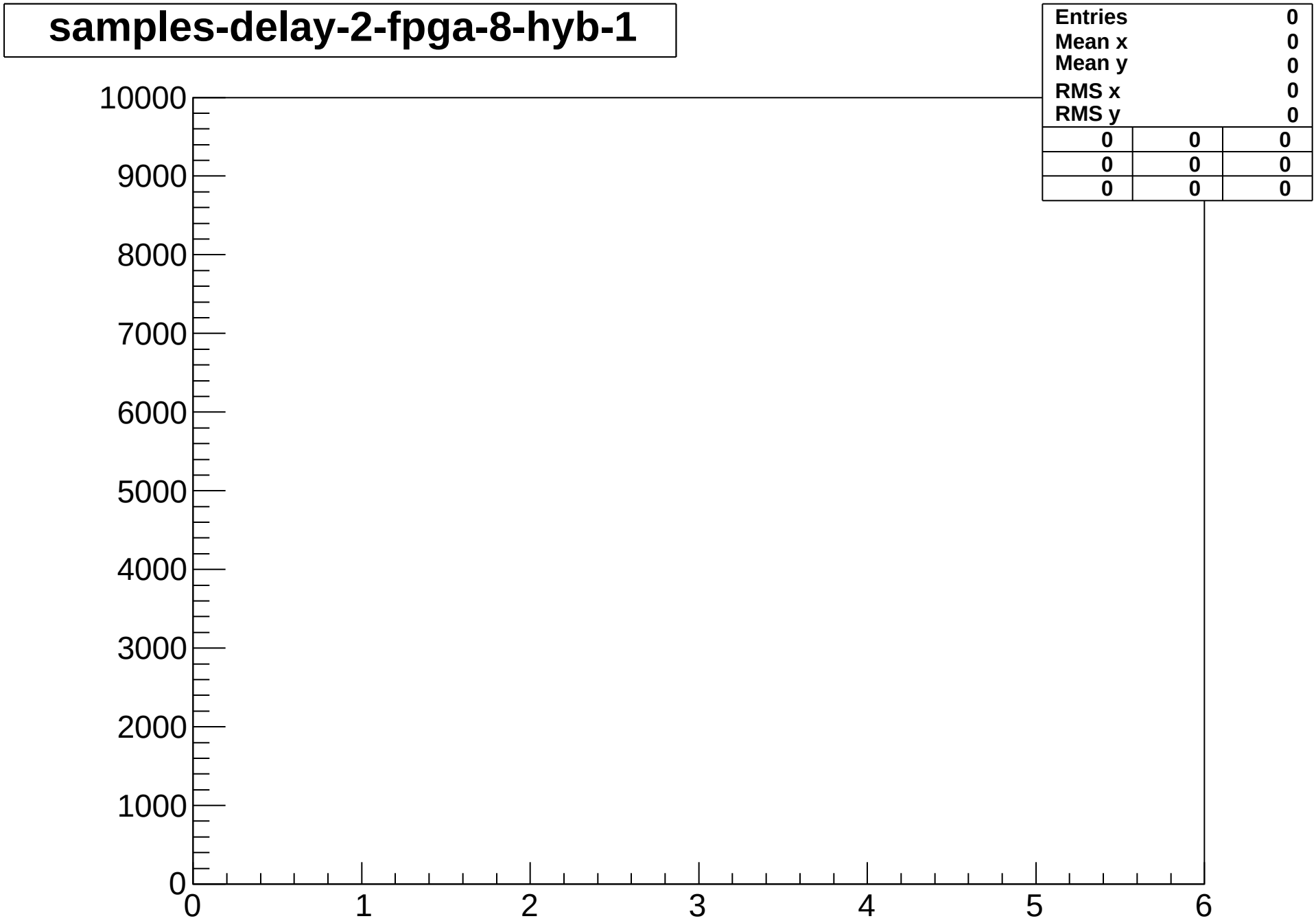
samples-delay-1-fpga-8-hyb-1




samples-delay-2-fpga-8-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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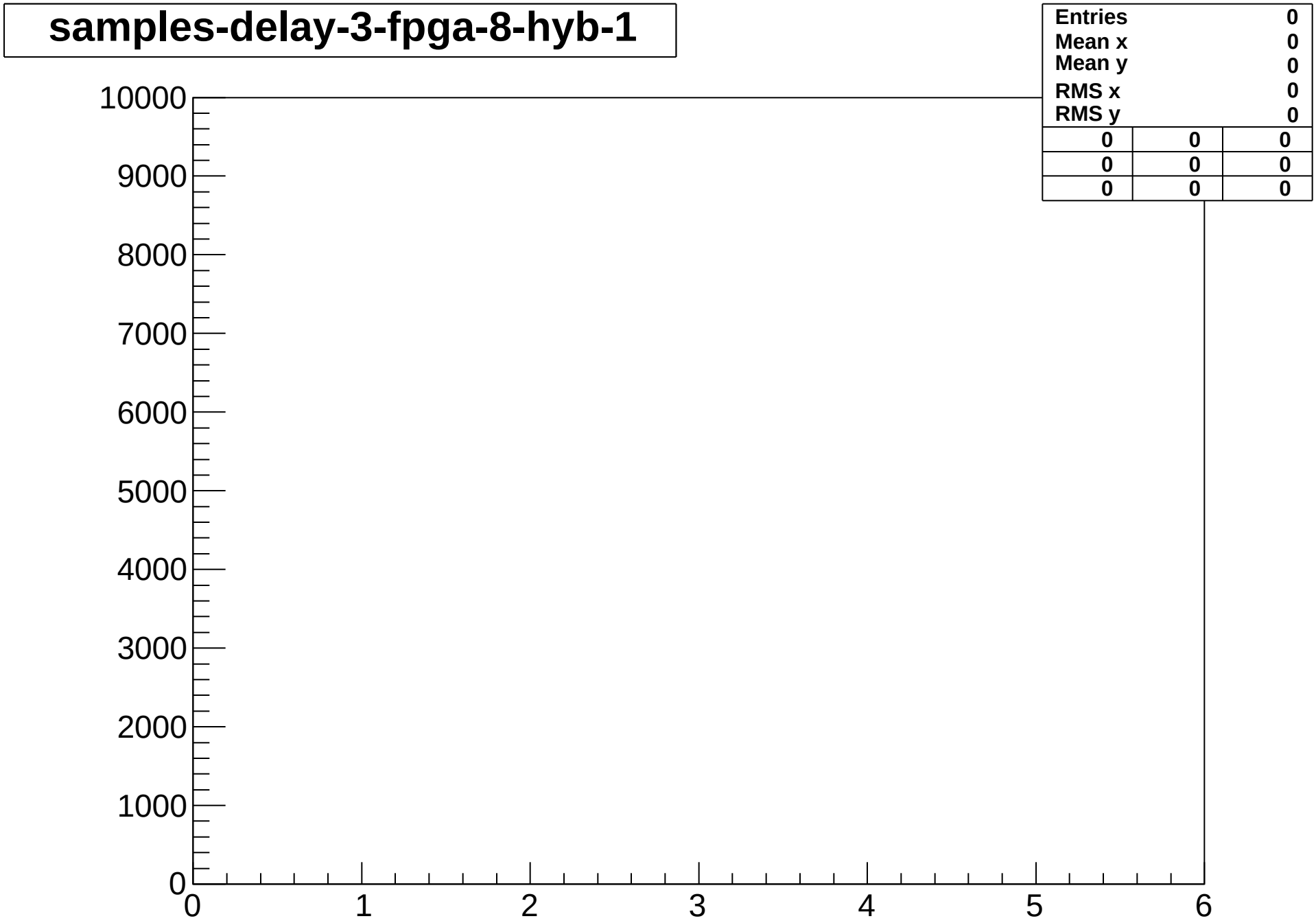
samples-delay-3-fpga-8-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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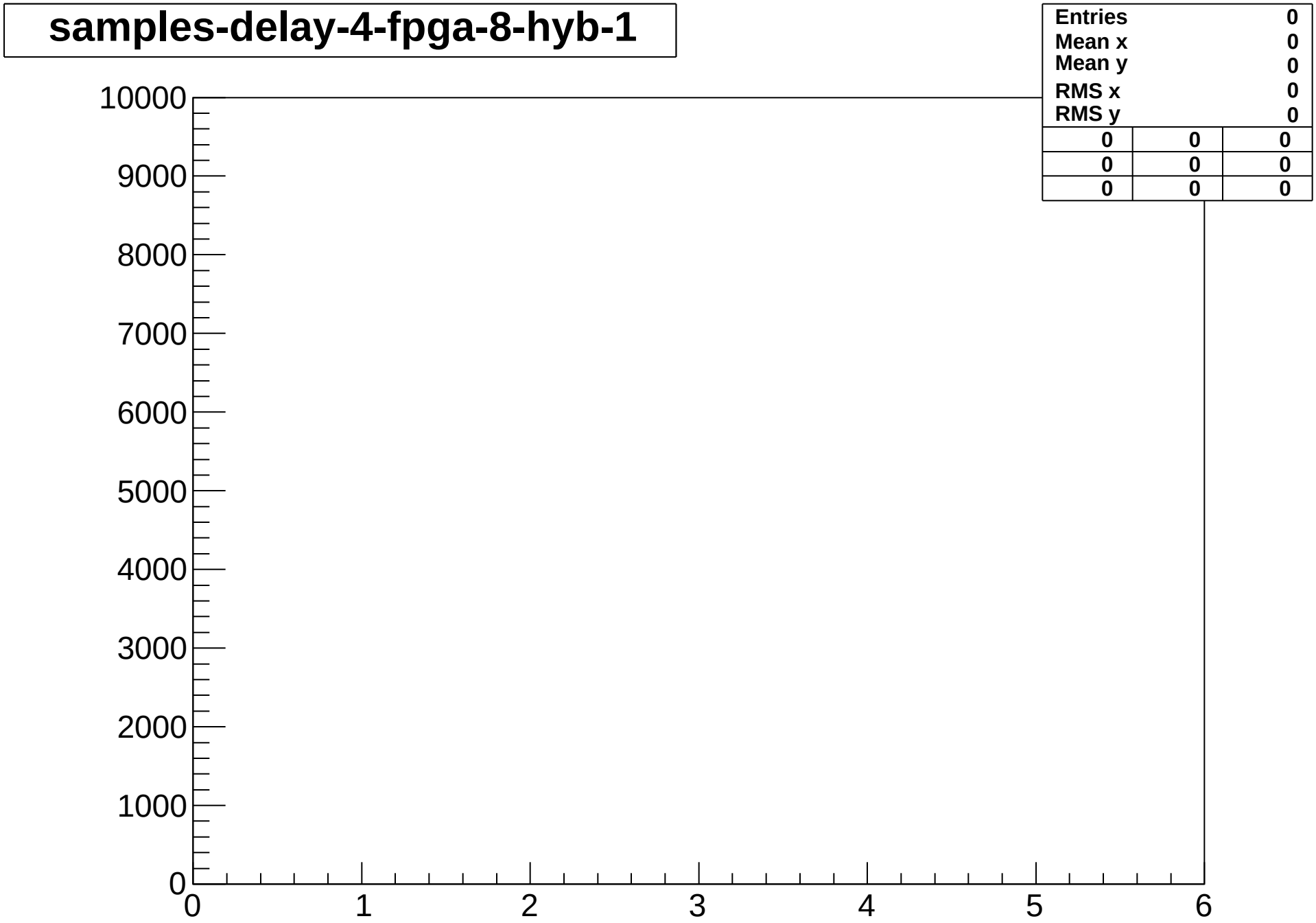
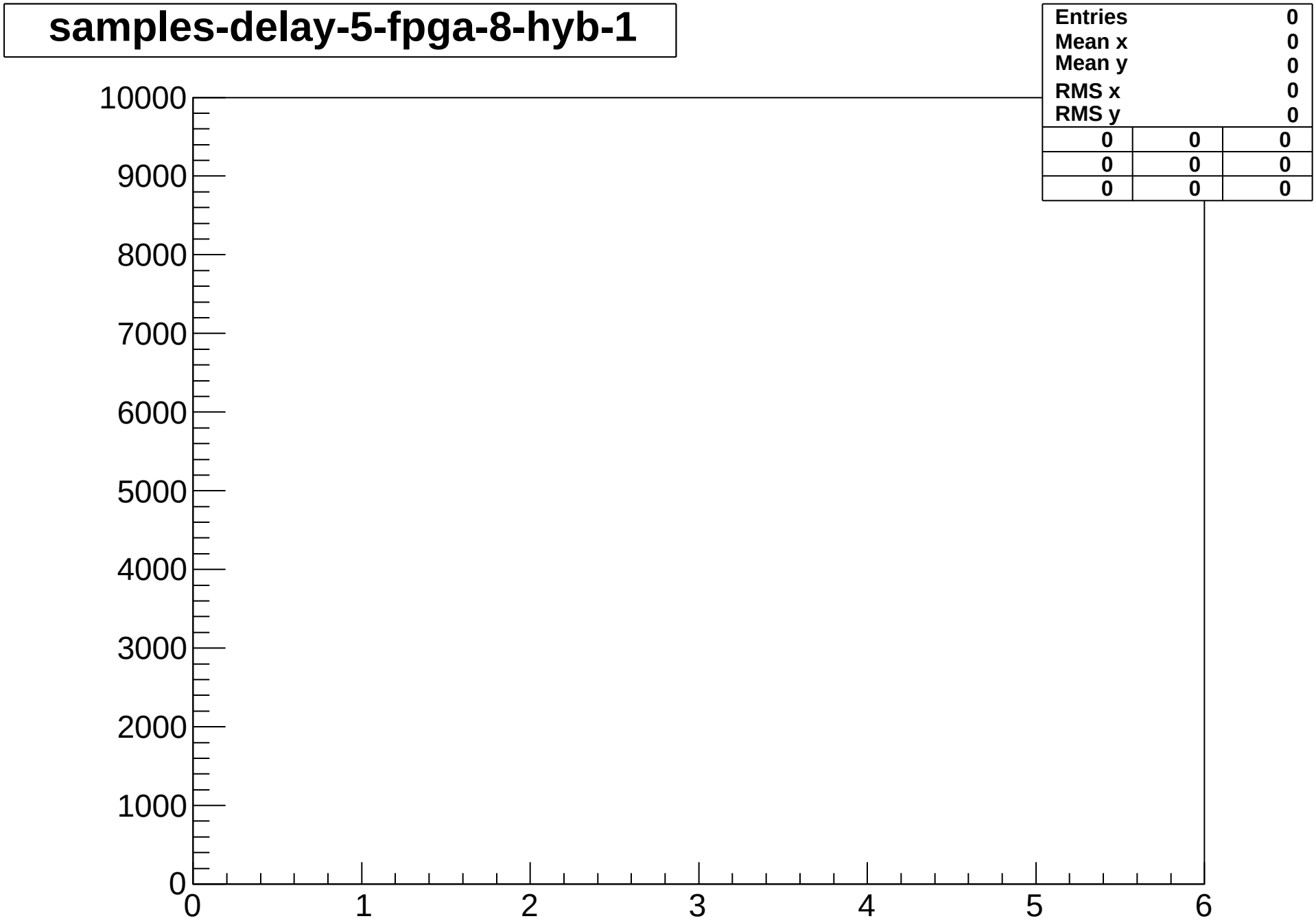
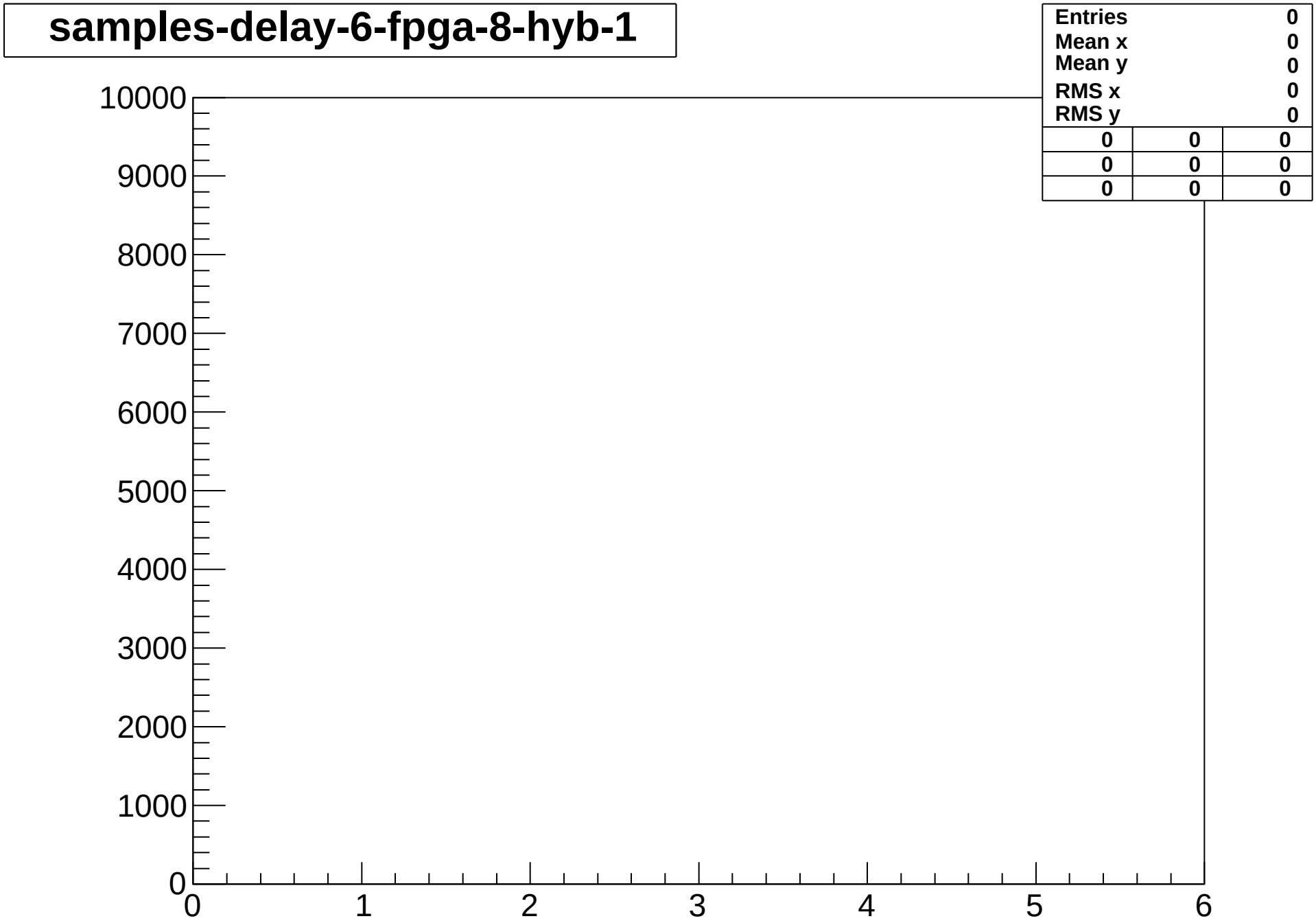
samples-delay-4-fpga-8-hyb-1

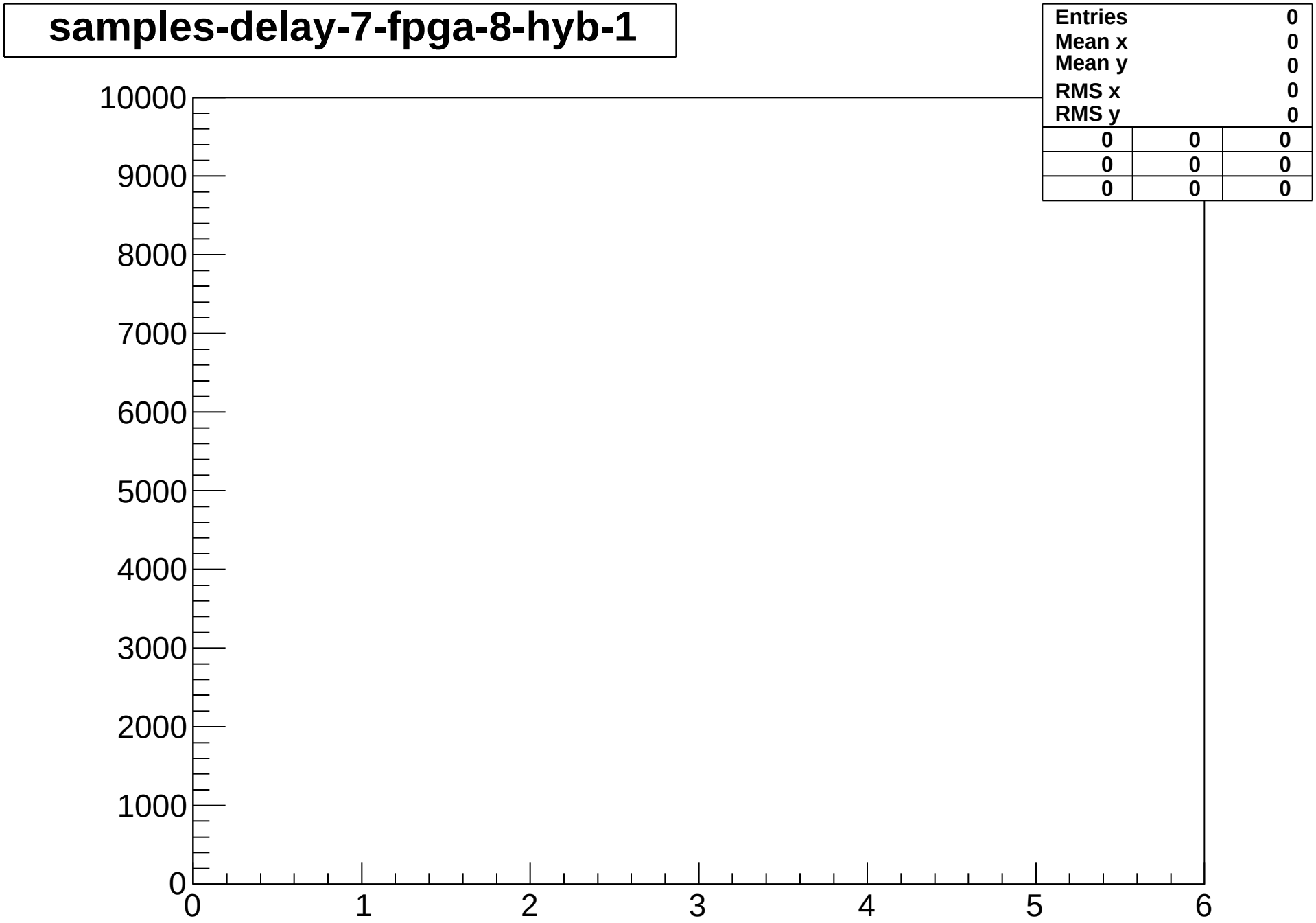


samples-delay-5-fpga-8-hyb-1



samples-delay-6-fpga-8-hyb-1




samples-delay-7-fpga-8-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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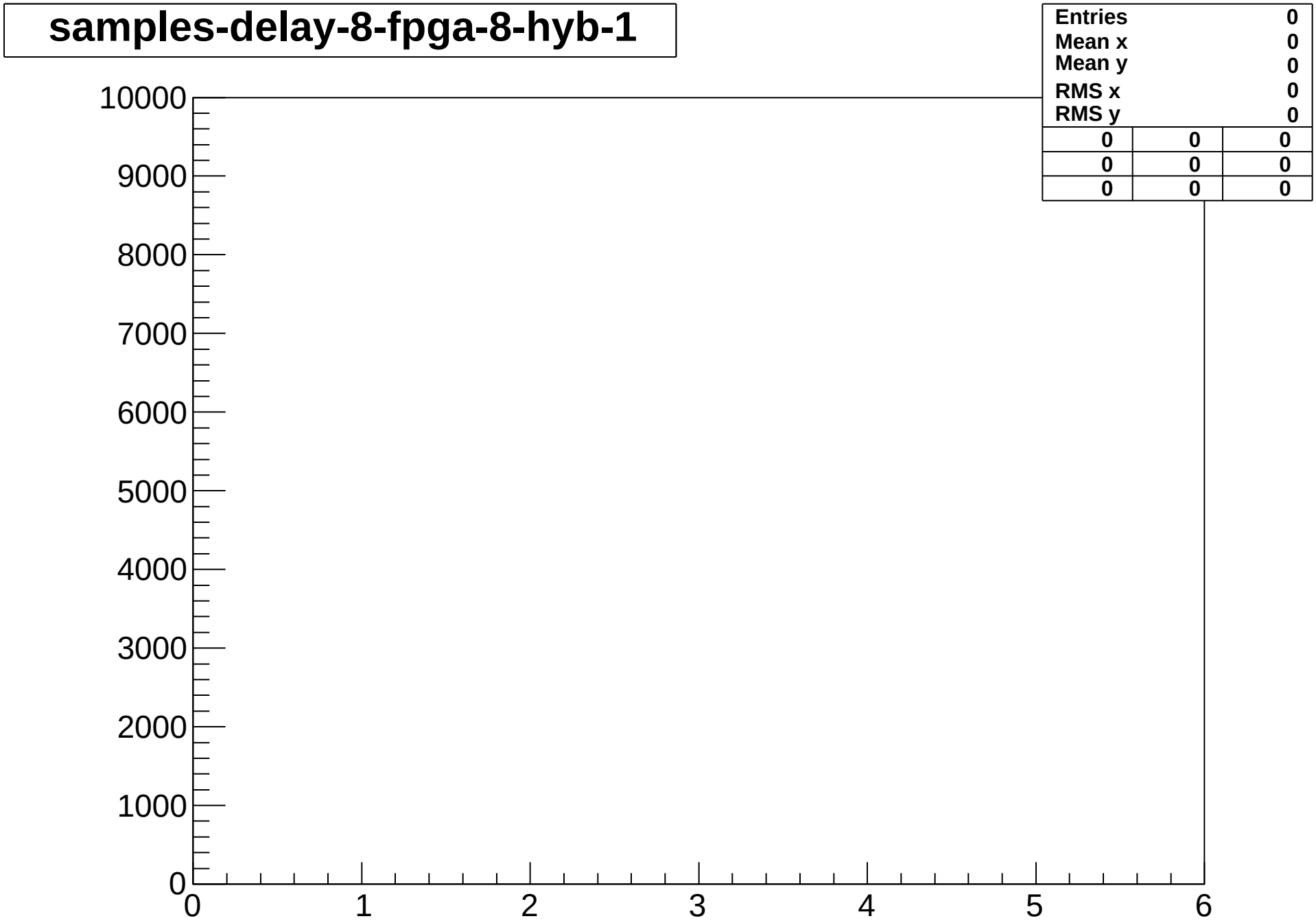
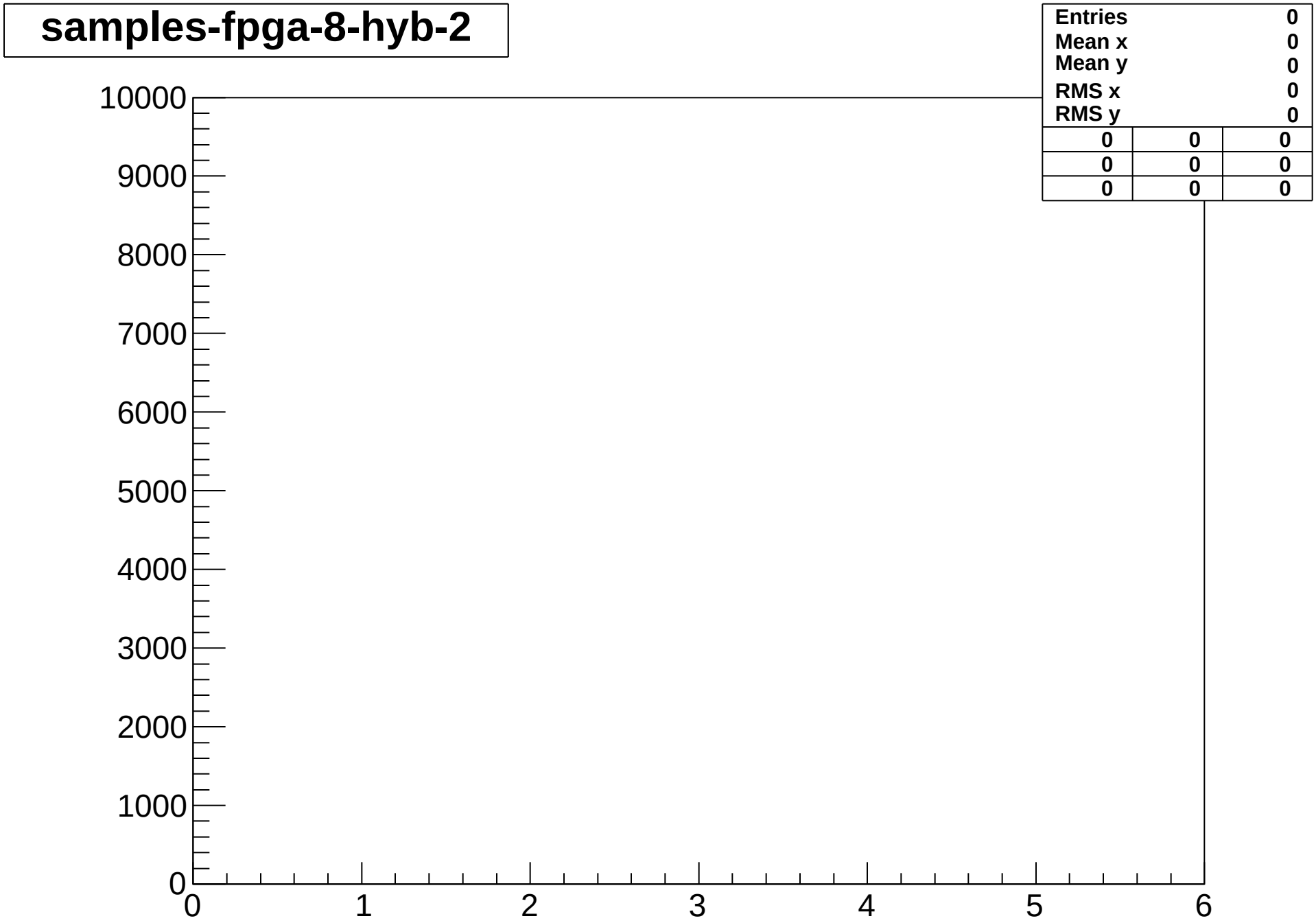
samples-delay-8-fpga-8-hyb-1




samples-fpga-8-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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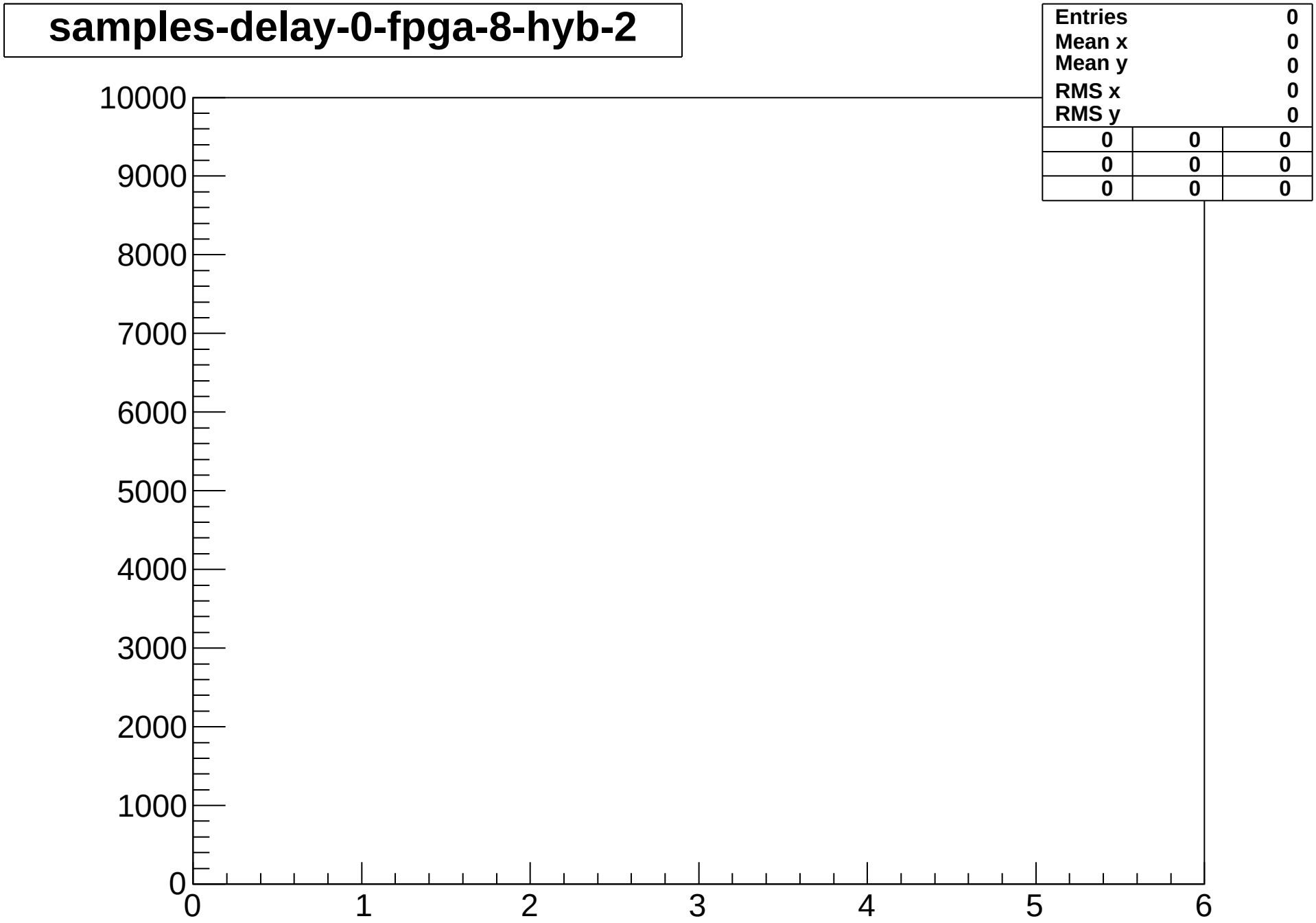
samples-delay-0-fpga-8-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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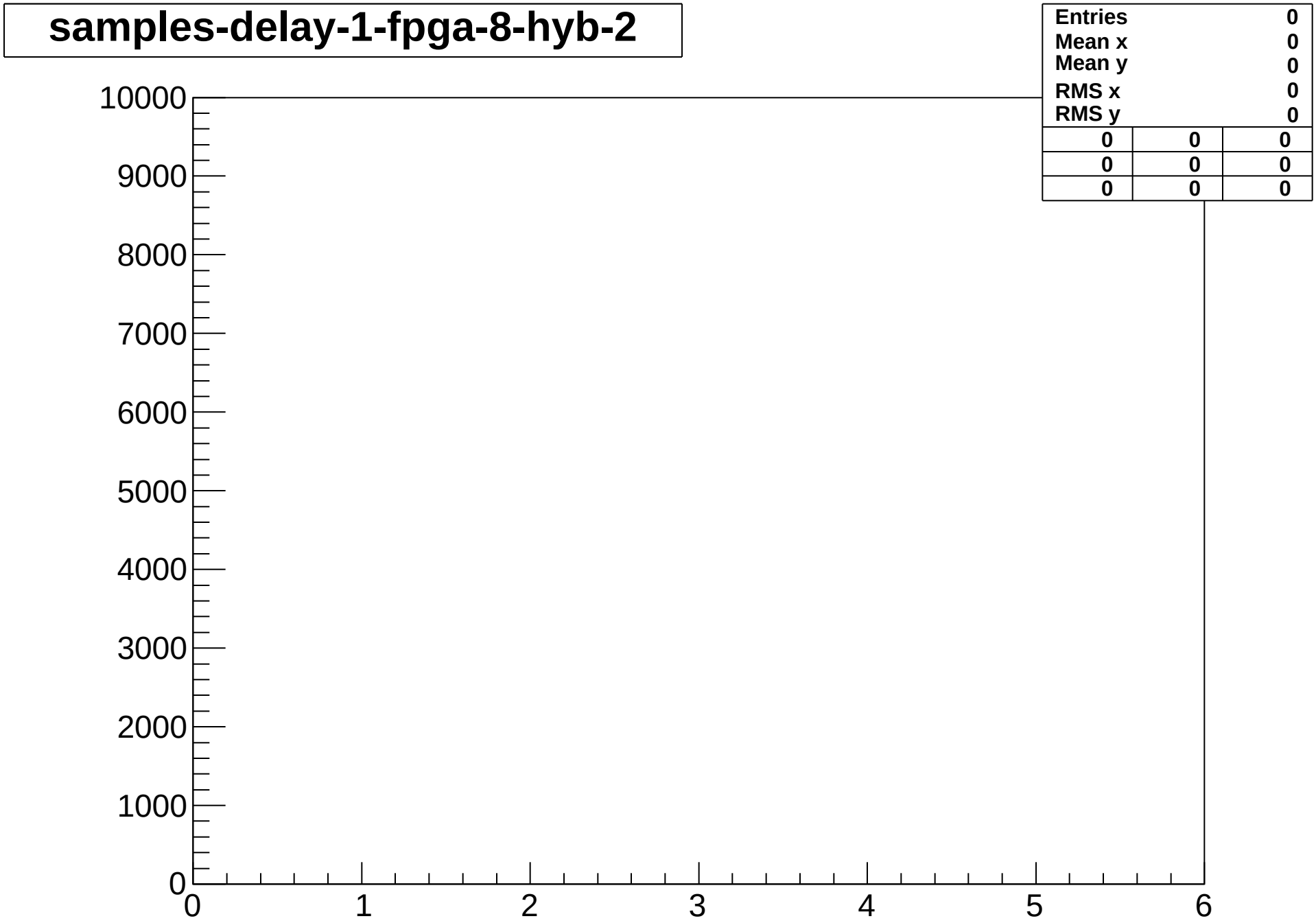
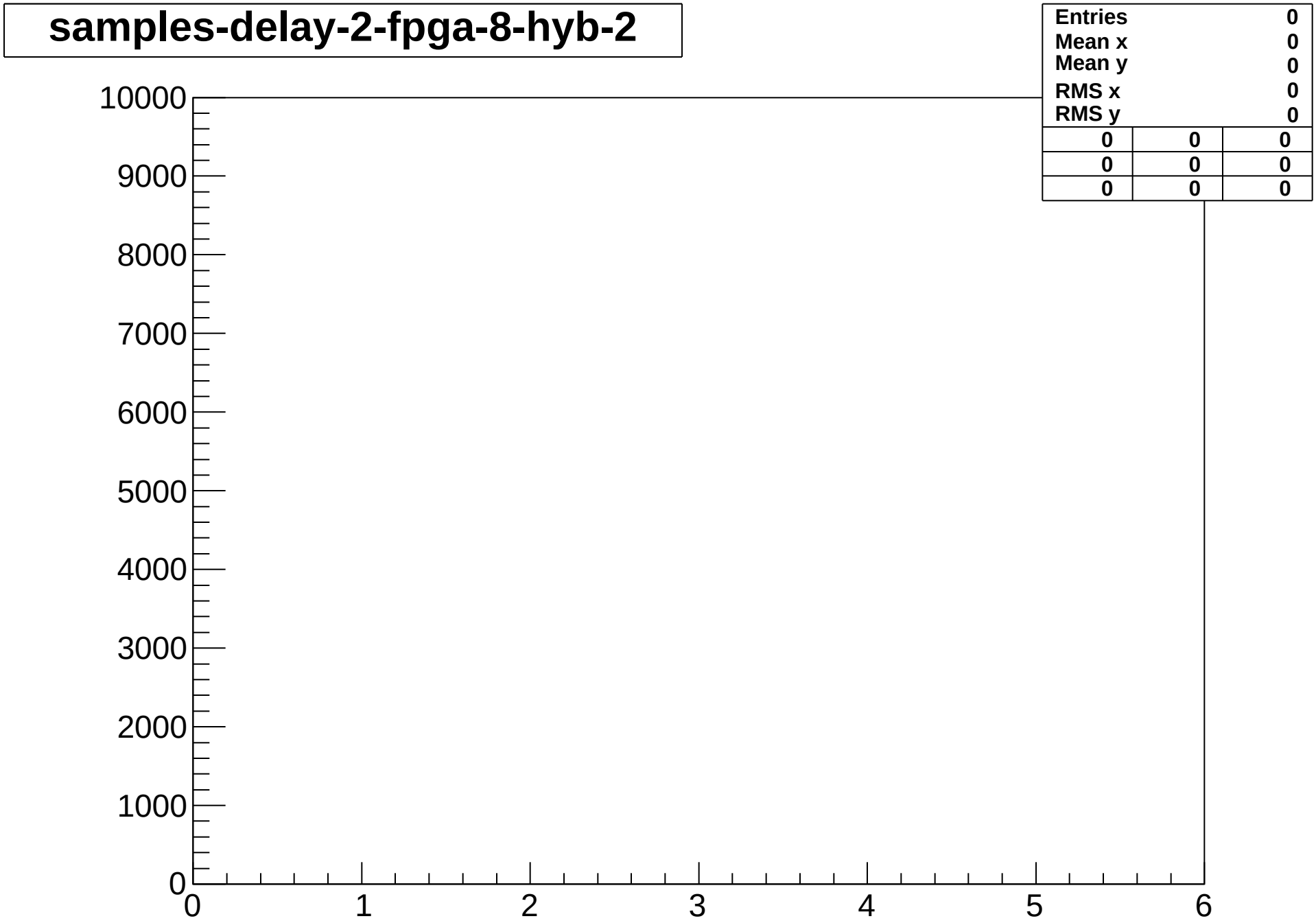
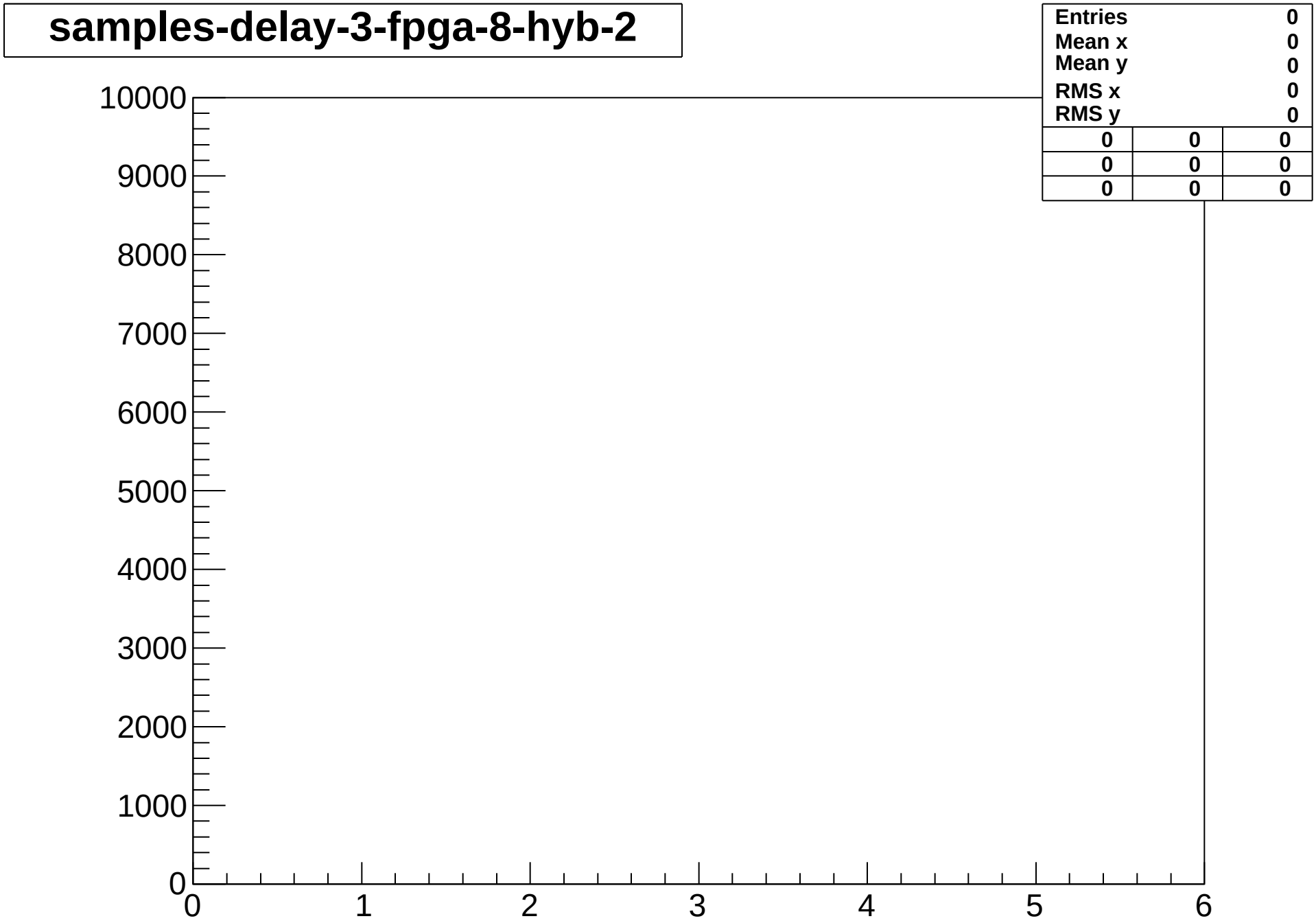
samples-delay-1-fpga-8-hyb-2



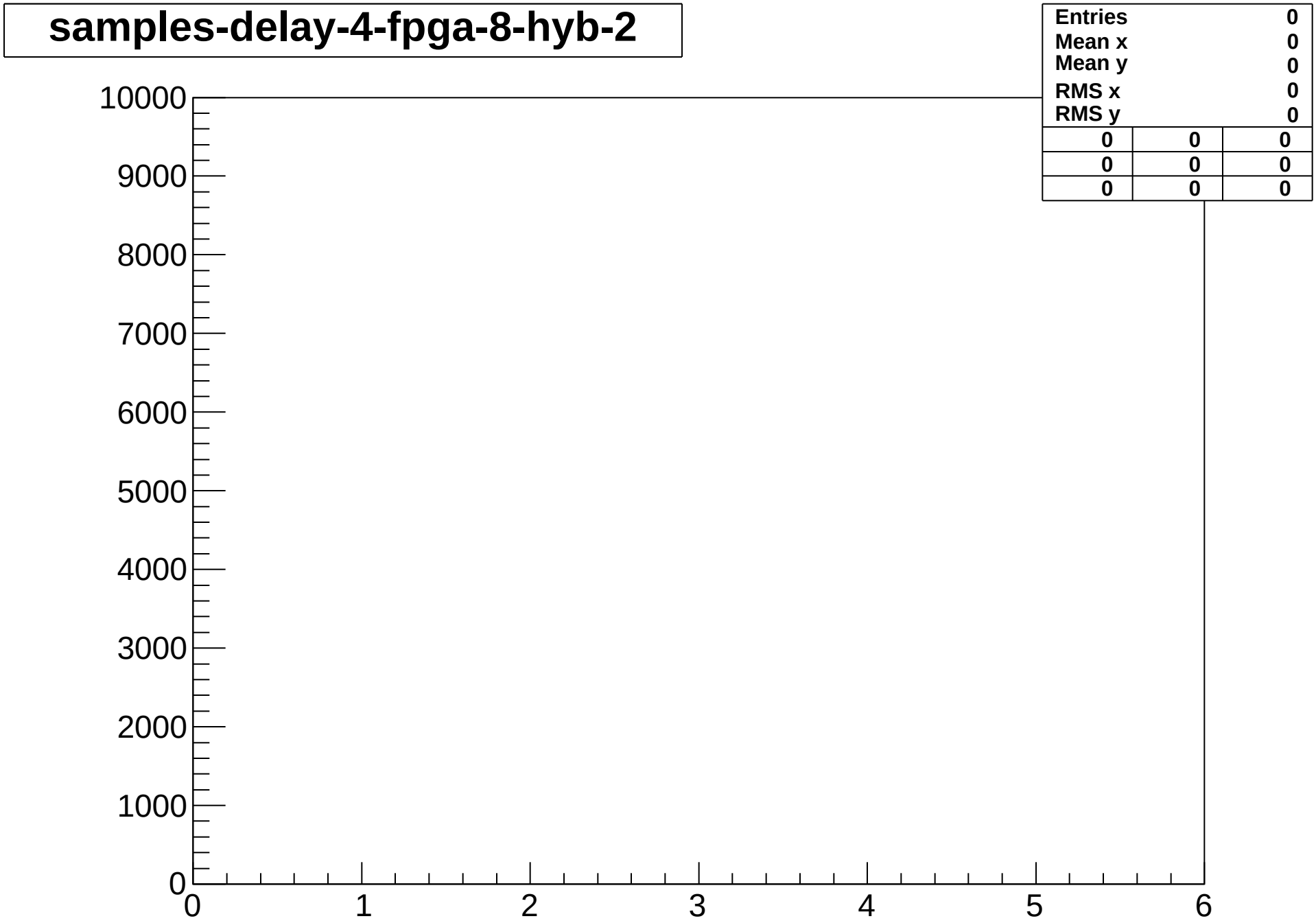
samples-delay-2-fpga-8-hyb-2



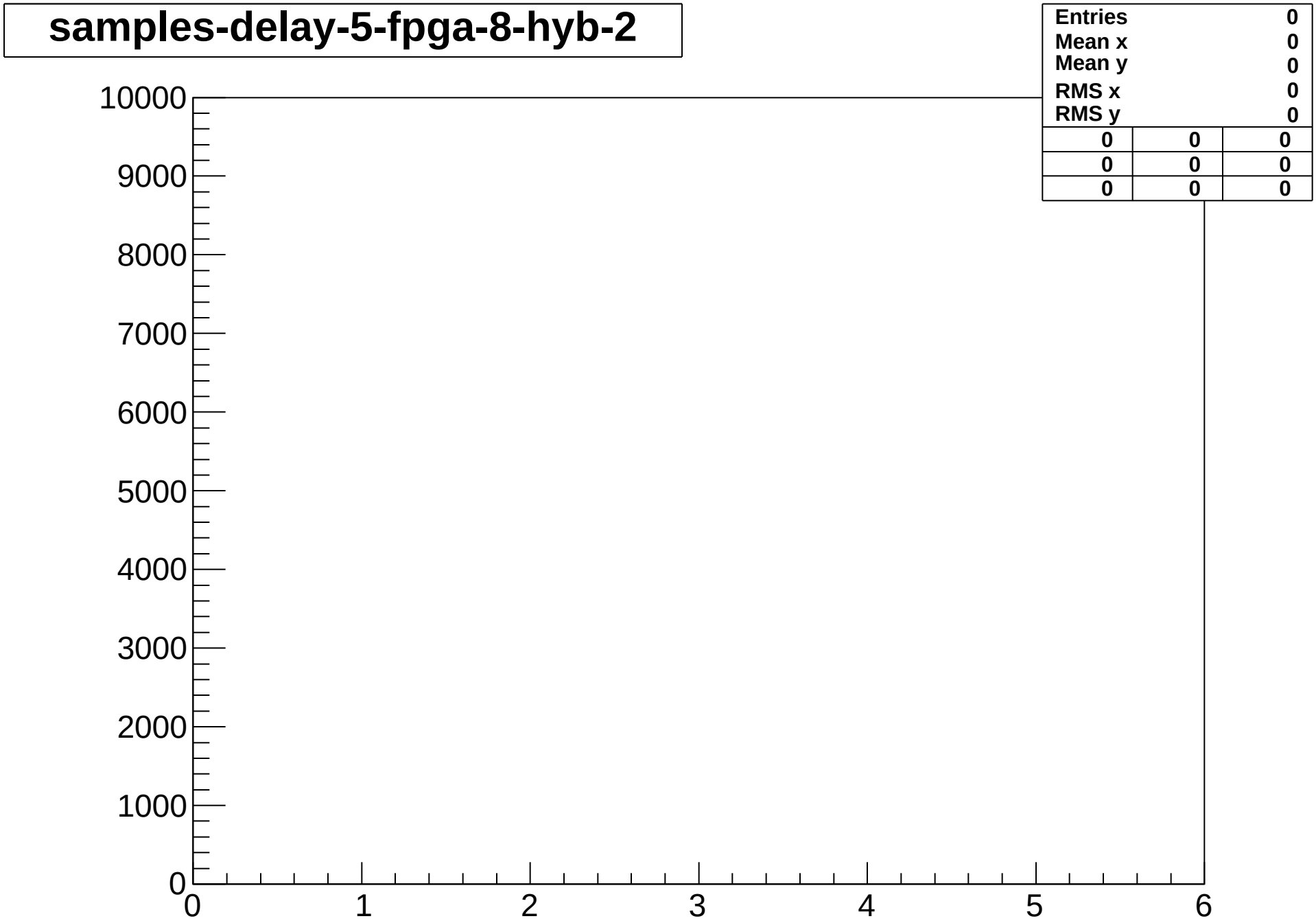
samples-delay-3-fpga-8-hyb-2



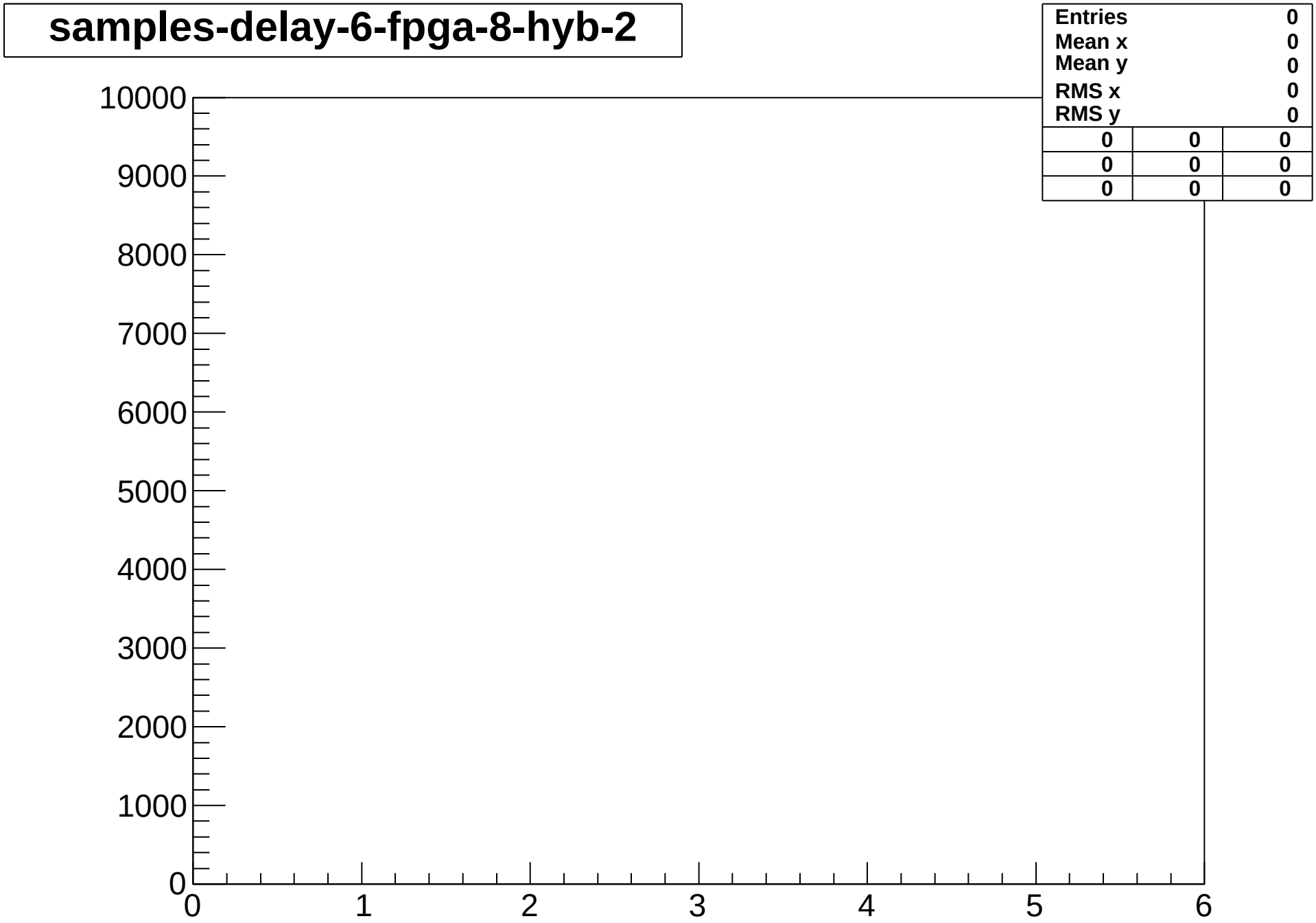
samples-delay-4-fpga-8-hyb-2



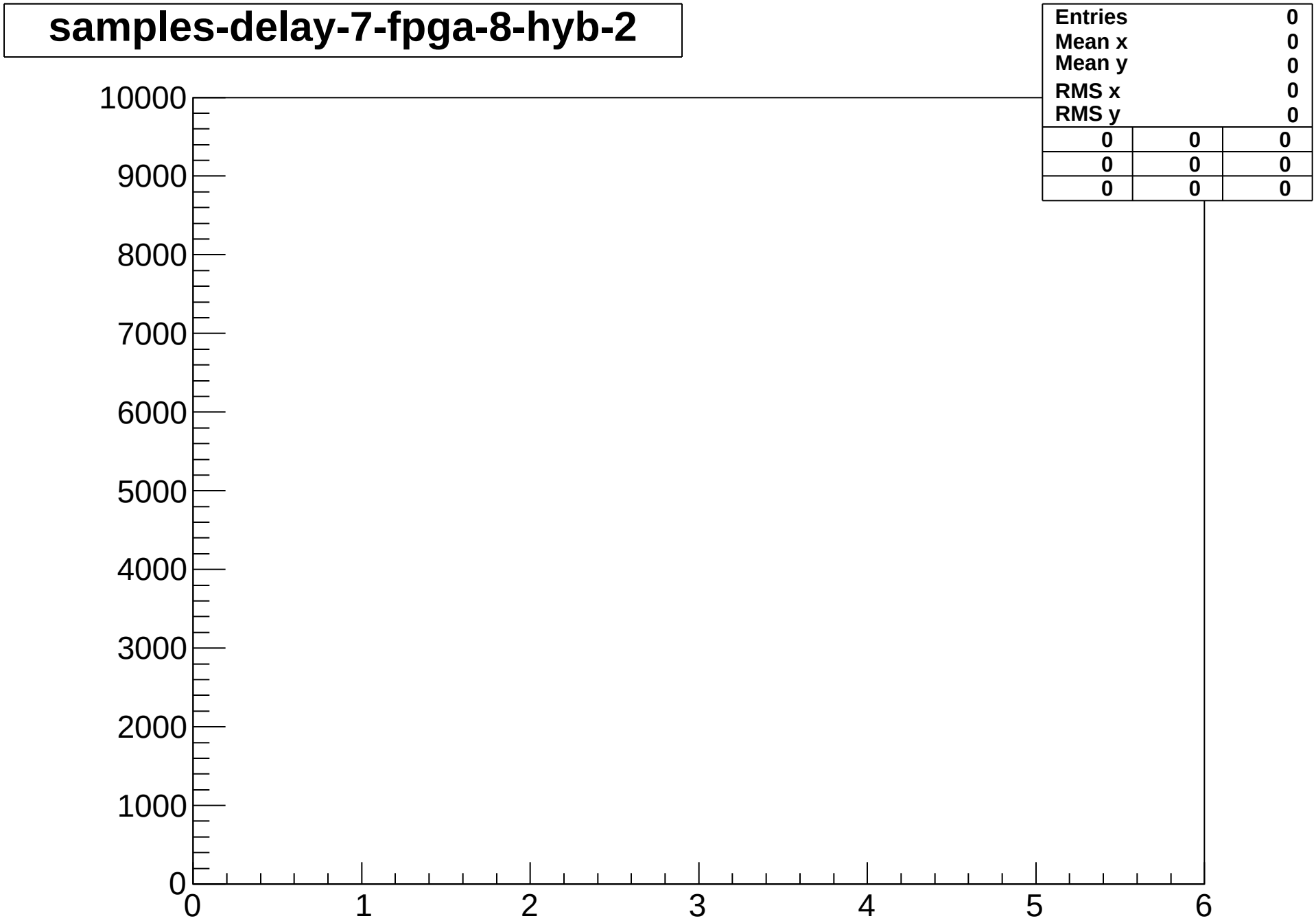
samples-delay-5-fpga-8-hyb-2

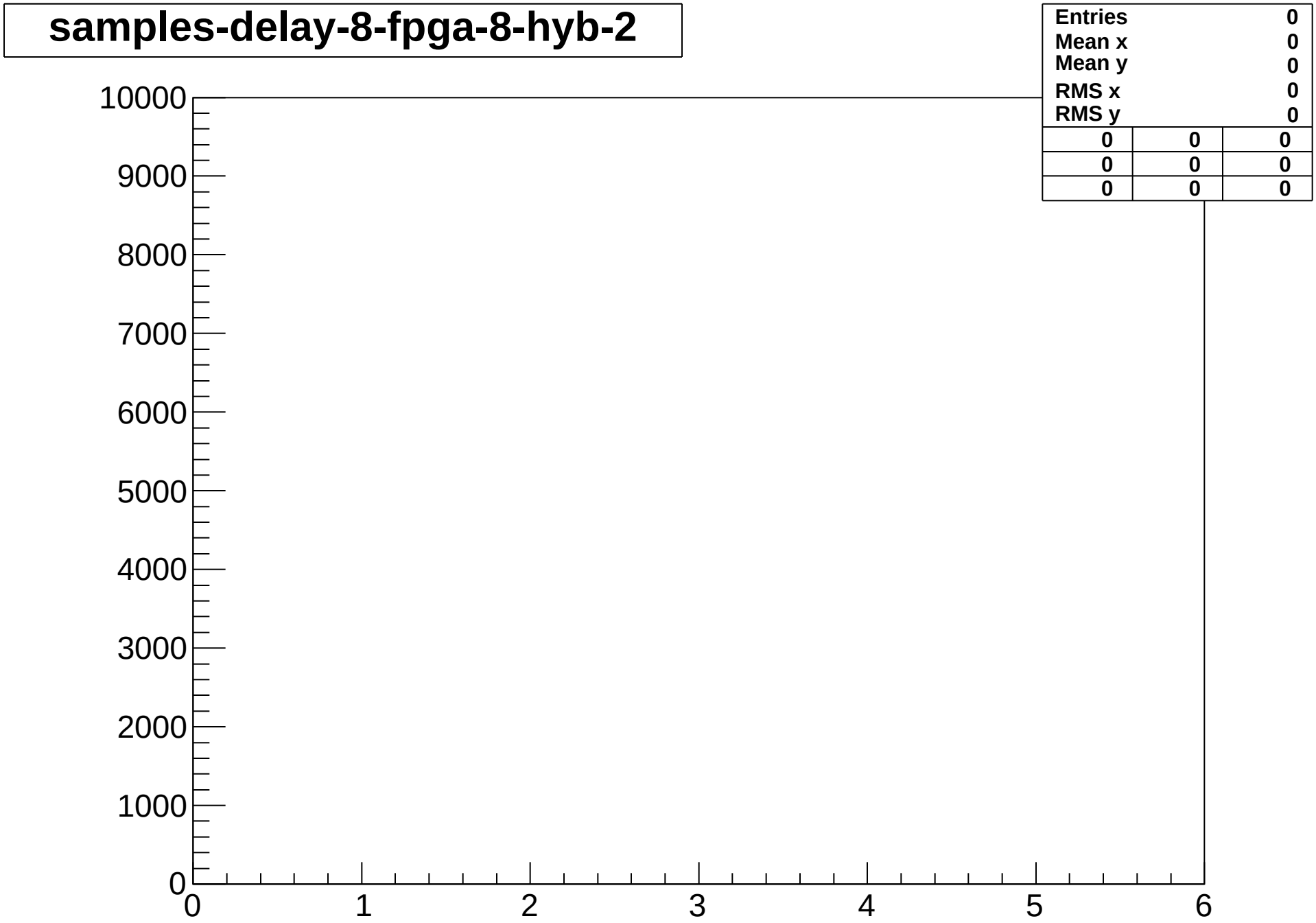


samples-delay-6-fpga-8-hyb-2



samples-delay-7-fpga-8-hyb-2




samples-delay-8-fpga-8-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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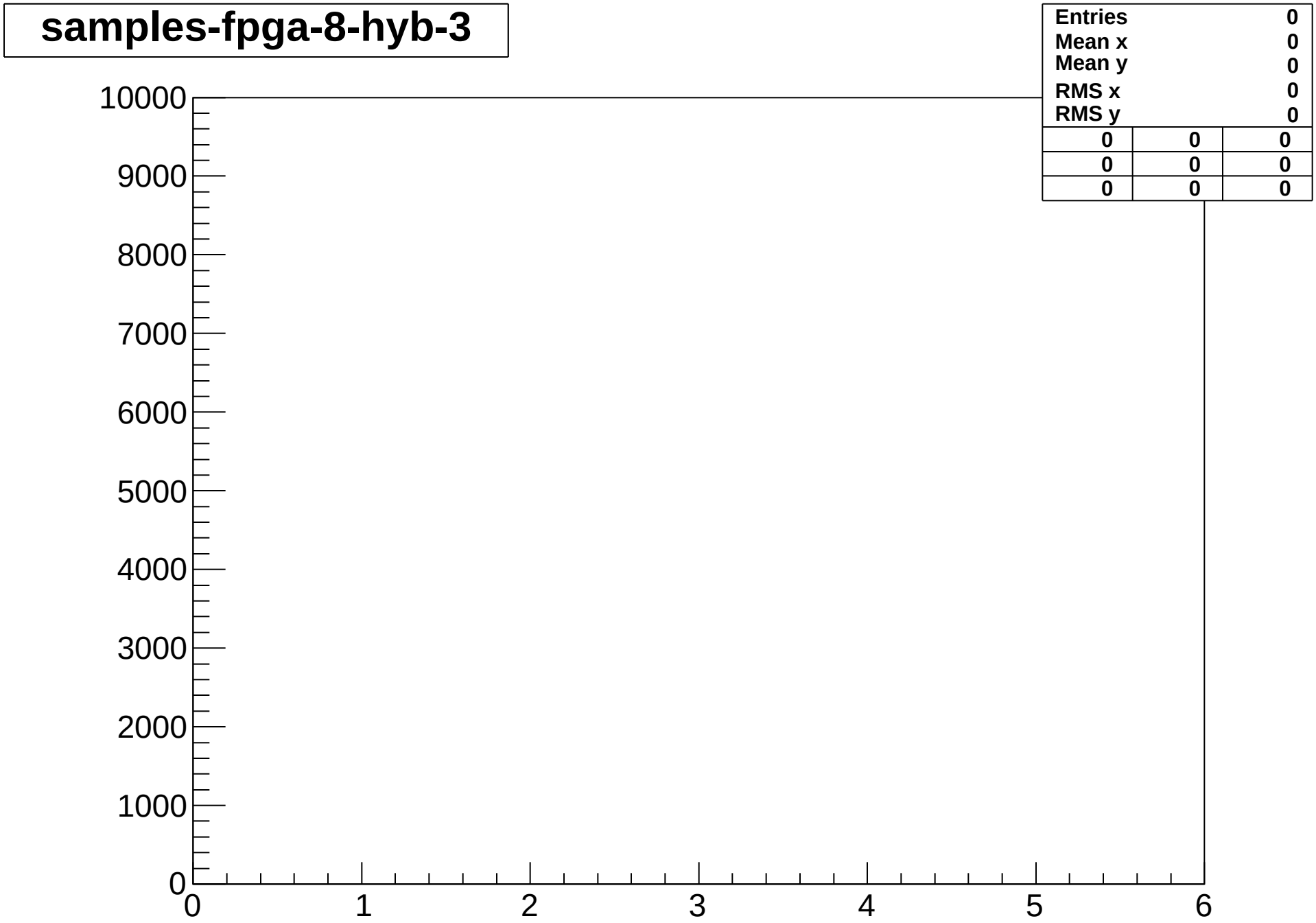
samples-fpga-8-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
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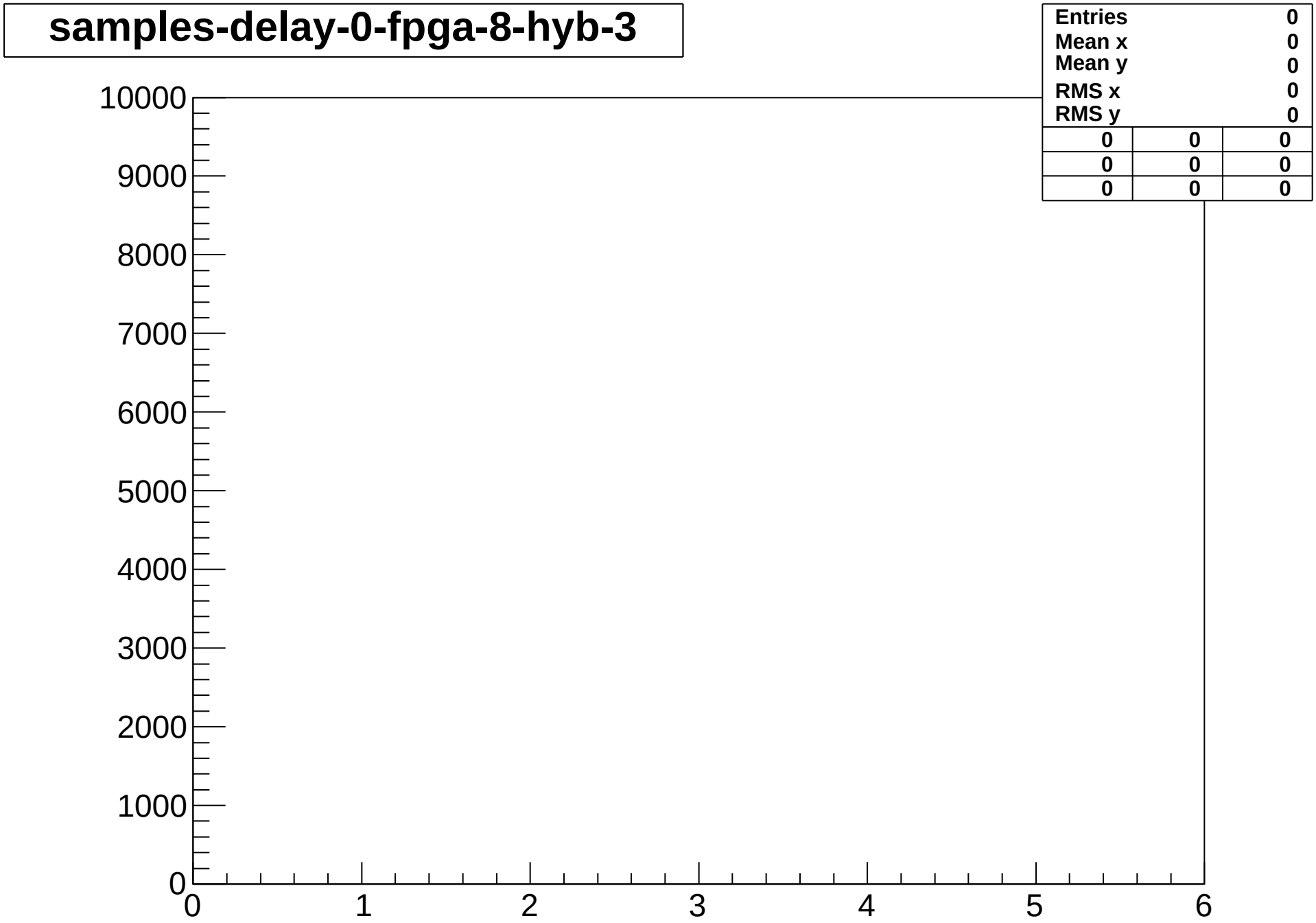
samples-delay-0-fpga-8-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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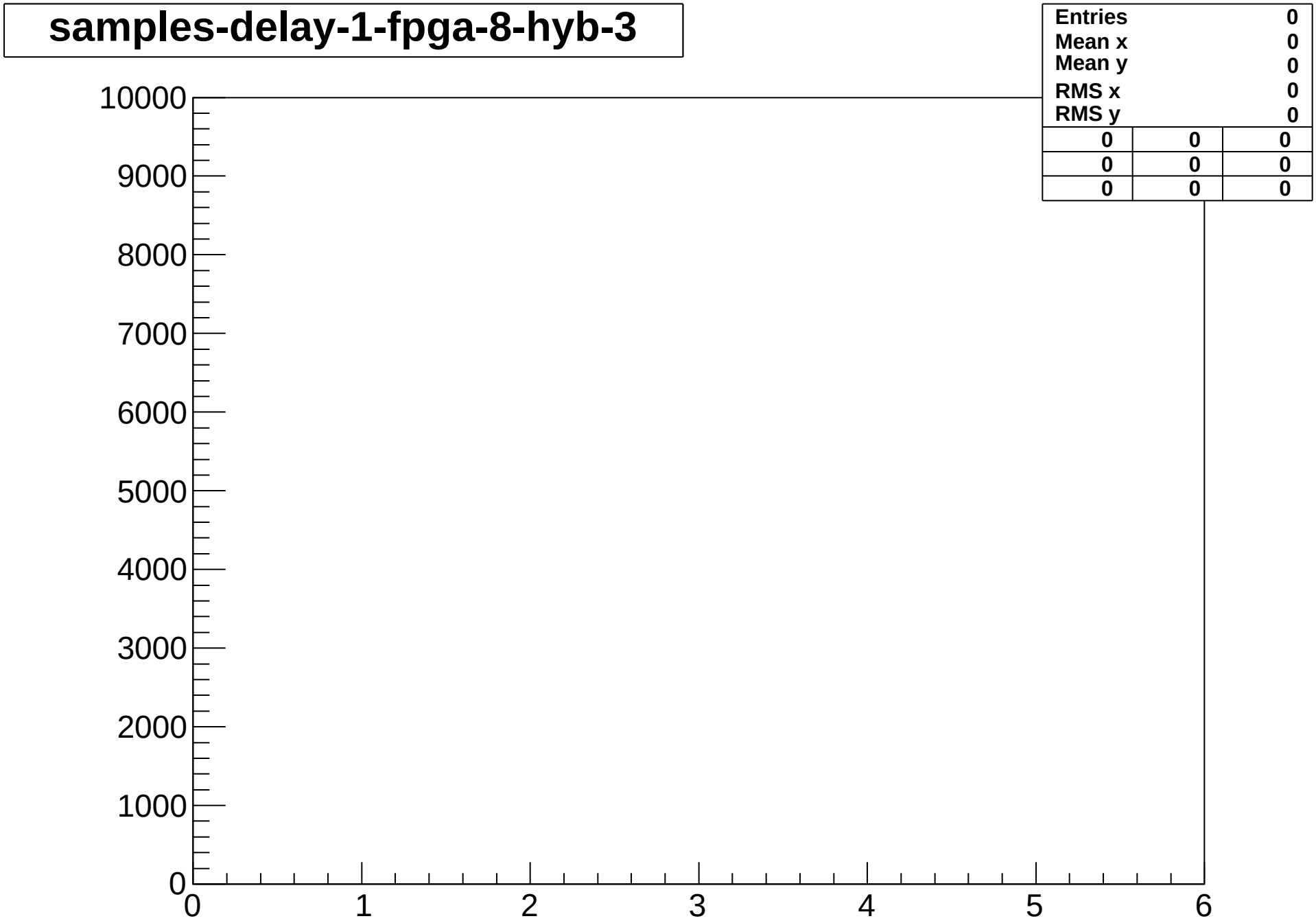
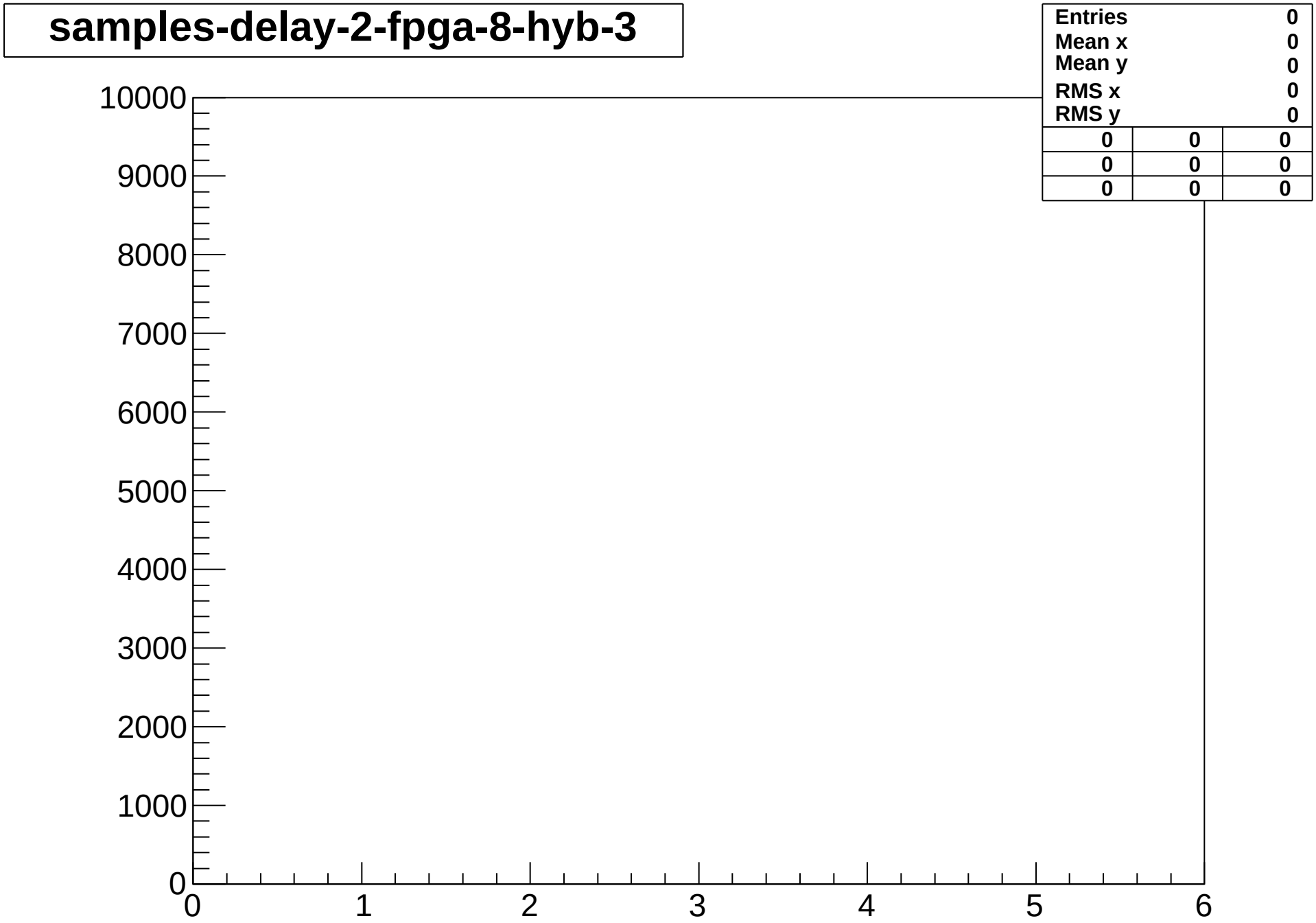
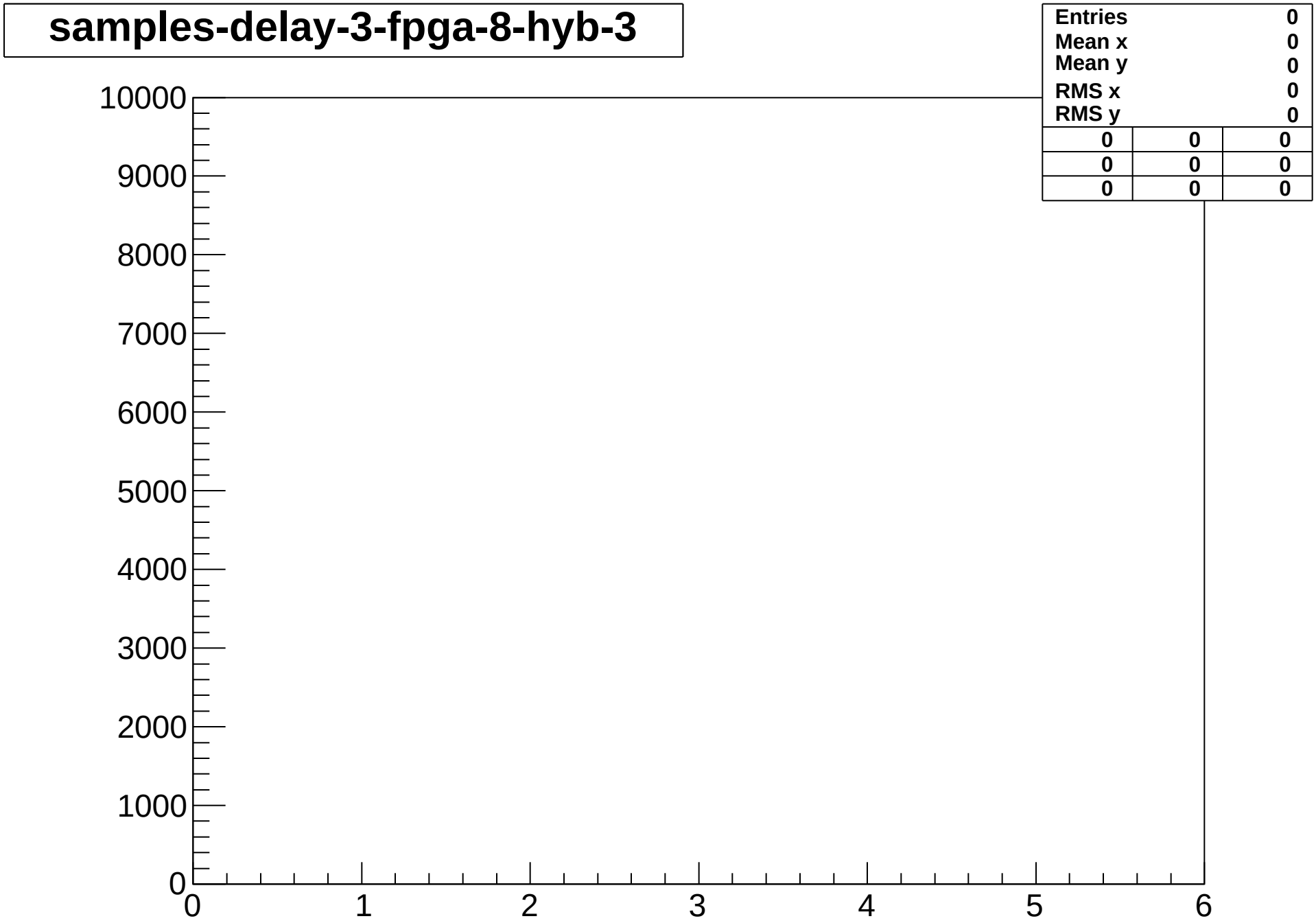
samples-delay-1-fpga-8-hyb-3

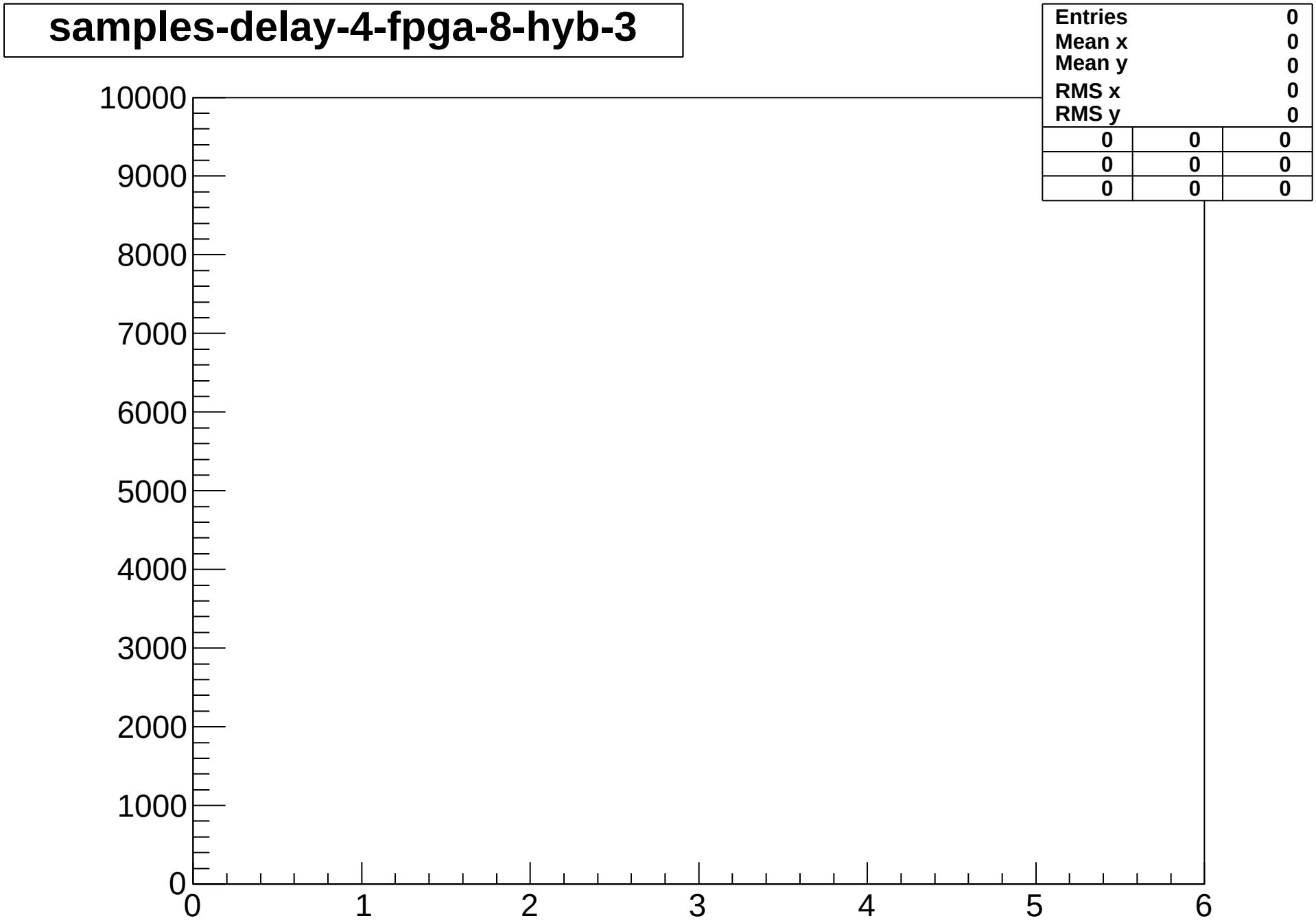


samples-delay-2-fpga-8-hyb-3



samples-delay-3-fpga-8-hyb-3




samples-delay-4-fpga-8-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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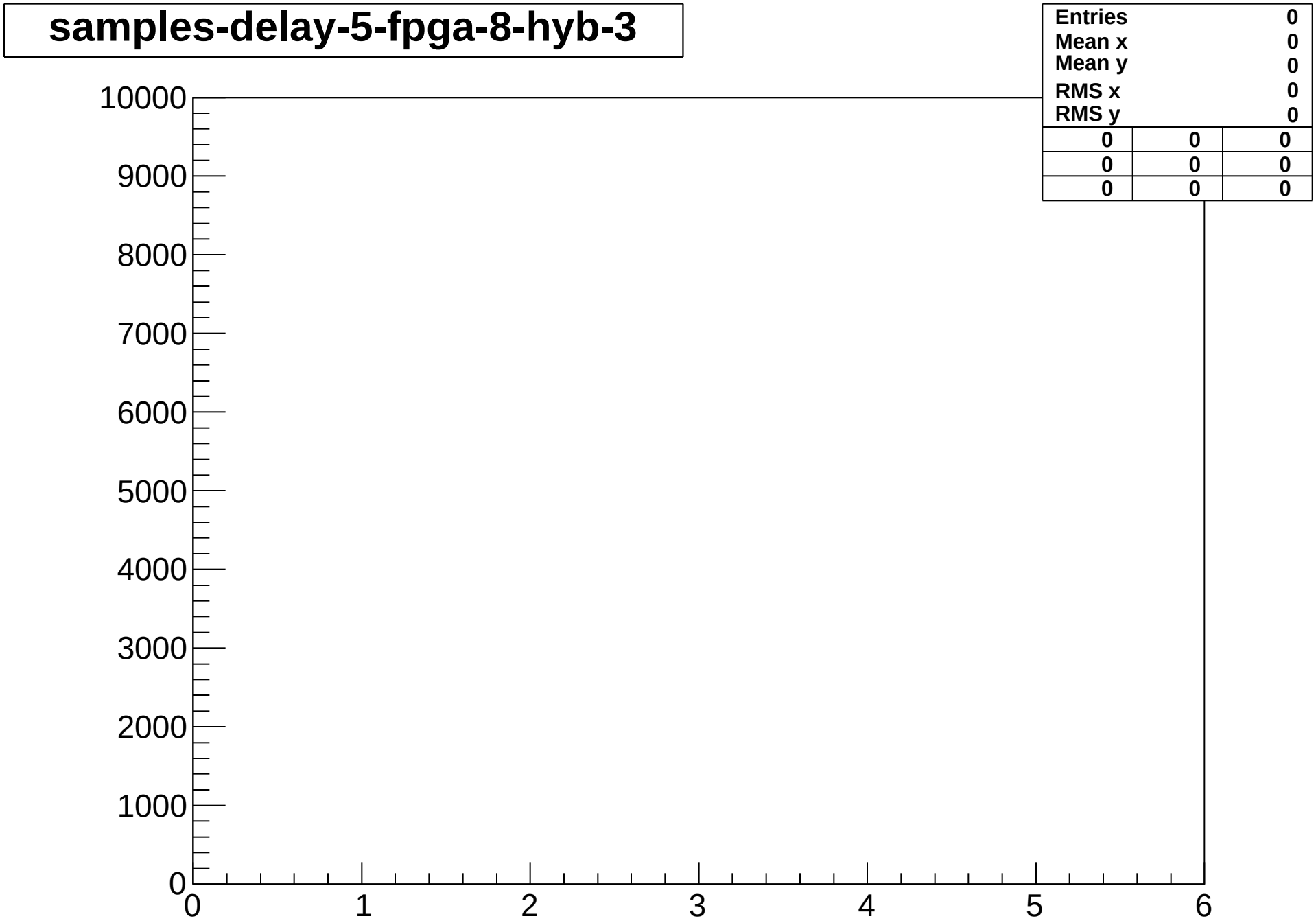
samples-delay-5-fpga-8-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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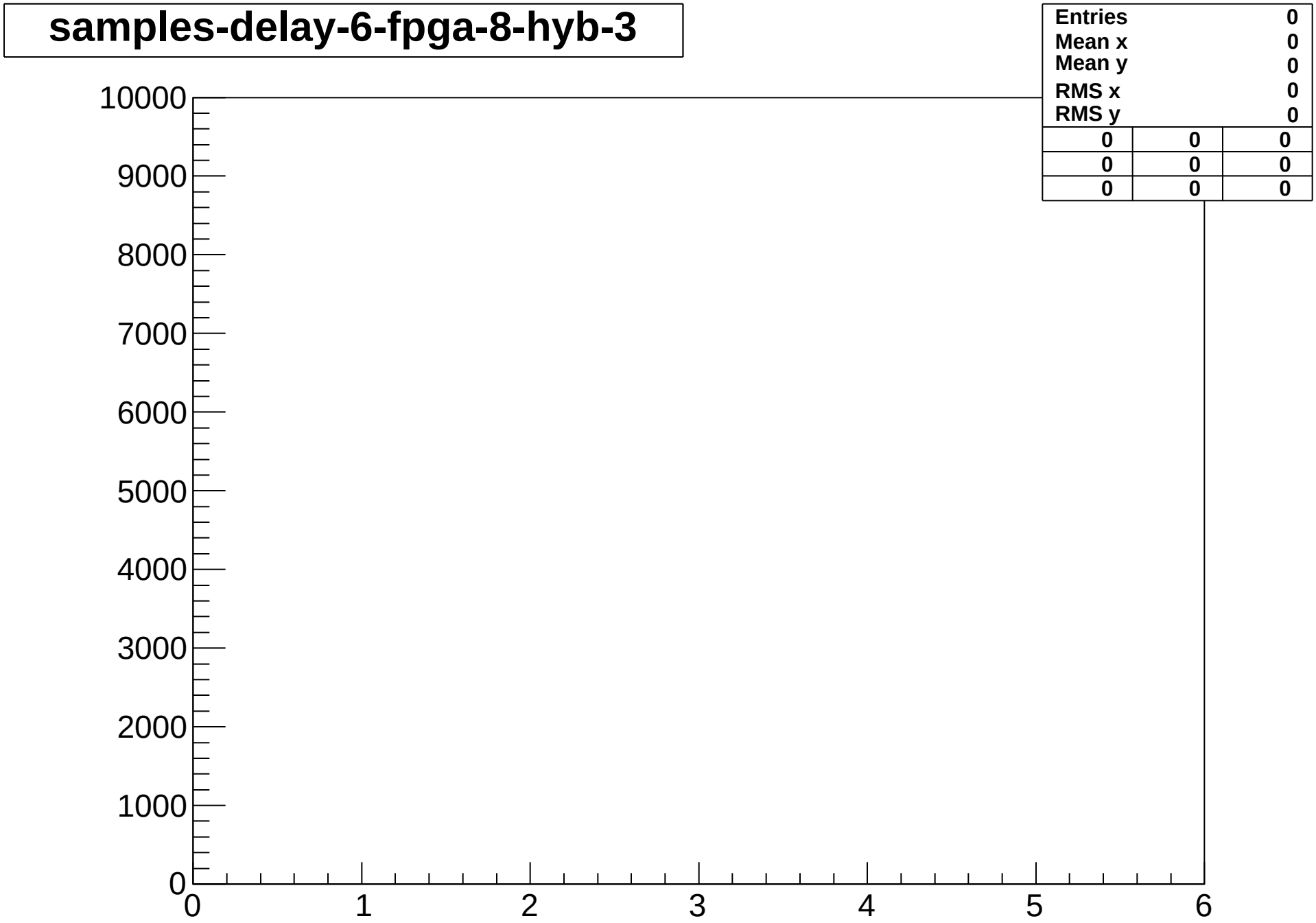
samples-delay-6-fpga-8-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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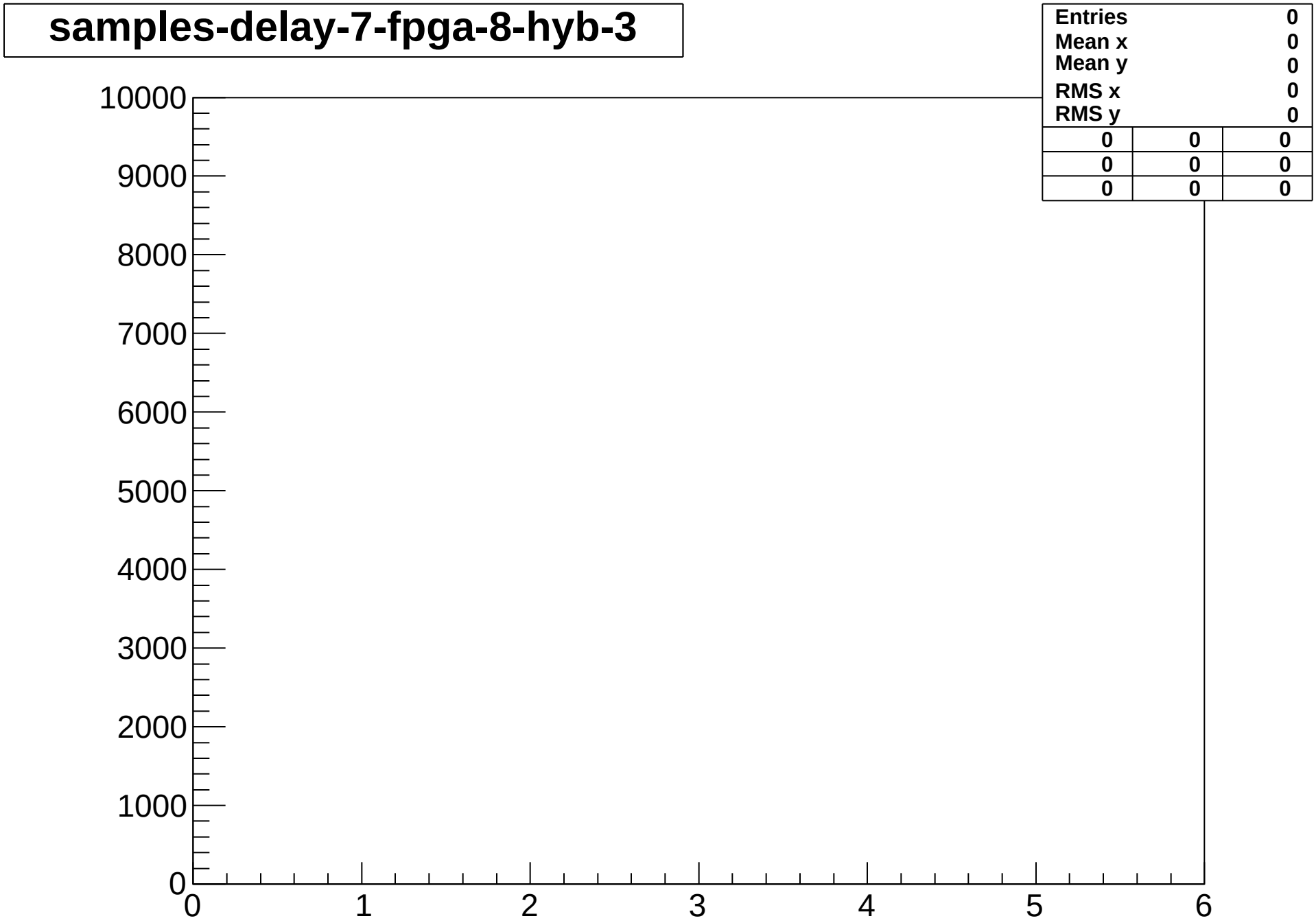
samples-delay-7-fpga-8-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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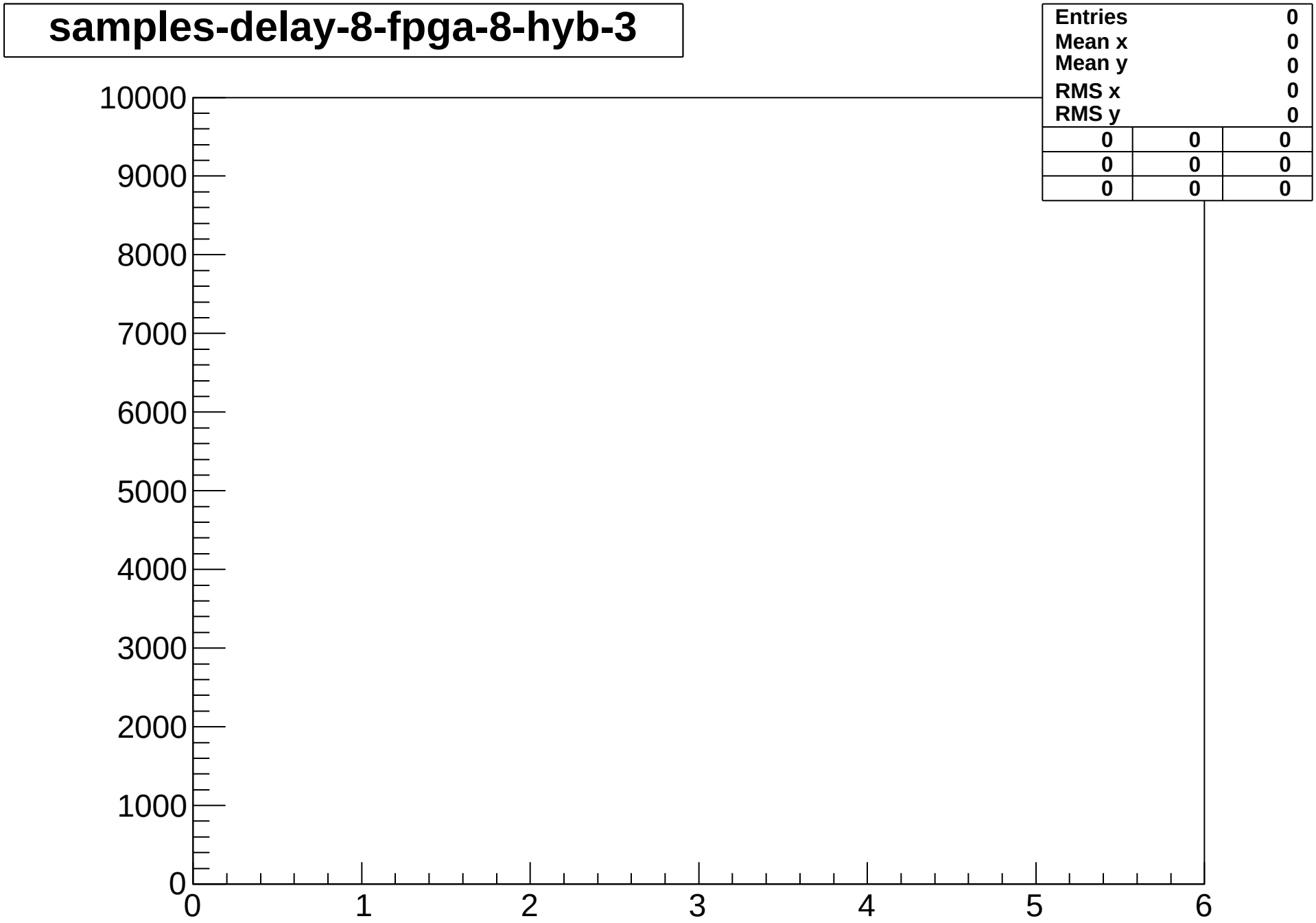
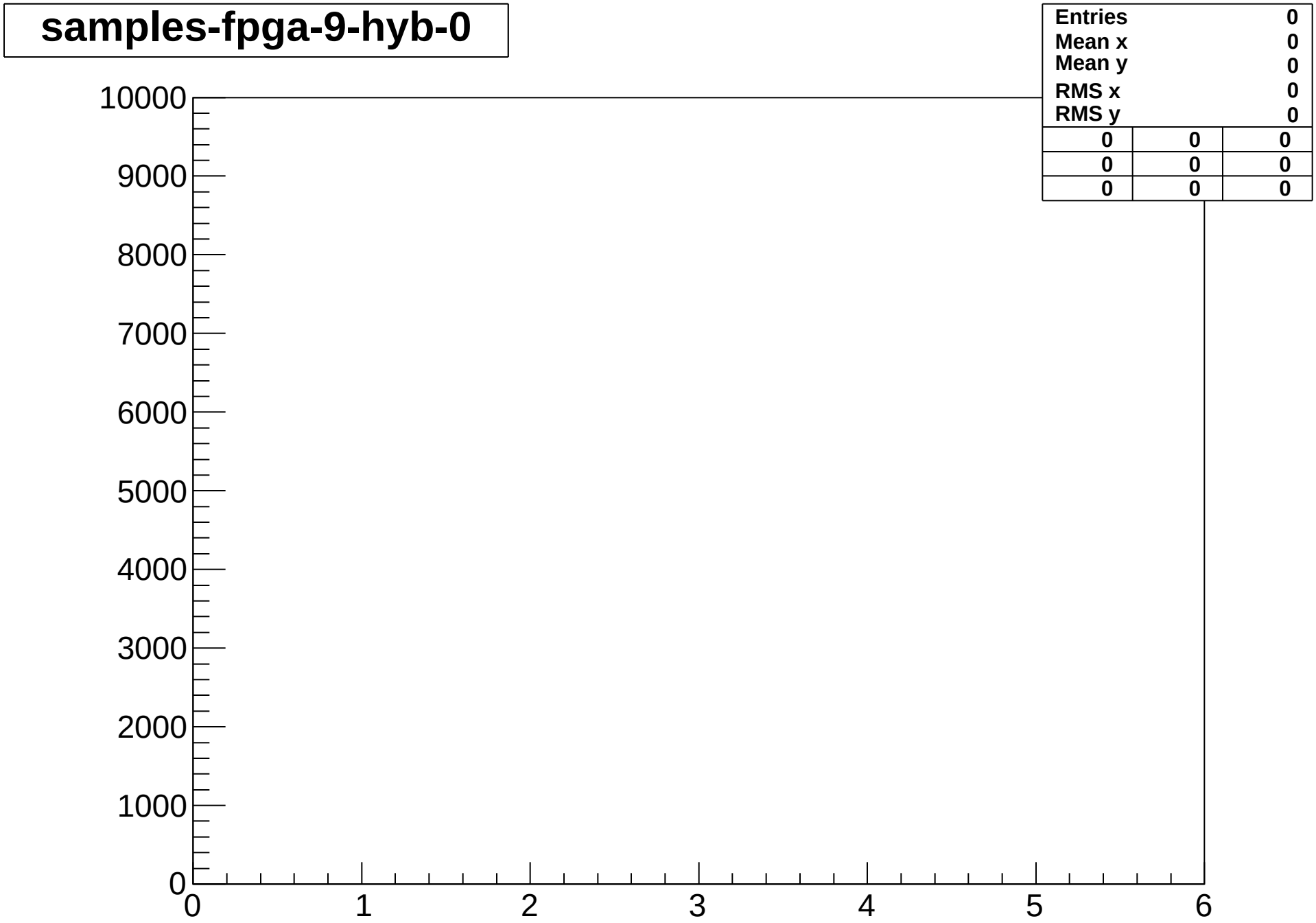
samples-delay-8-fpga-8-hyb-3




samples-fpga-9-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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6000
5000
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3000
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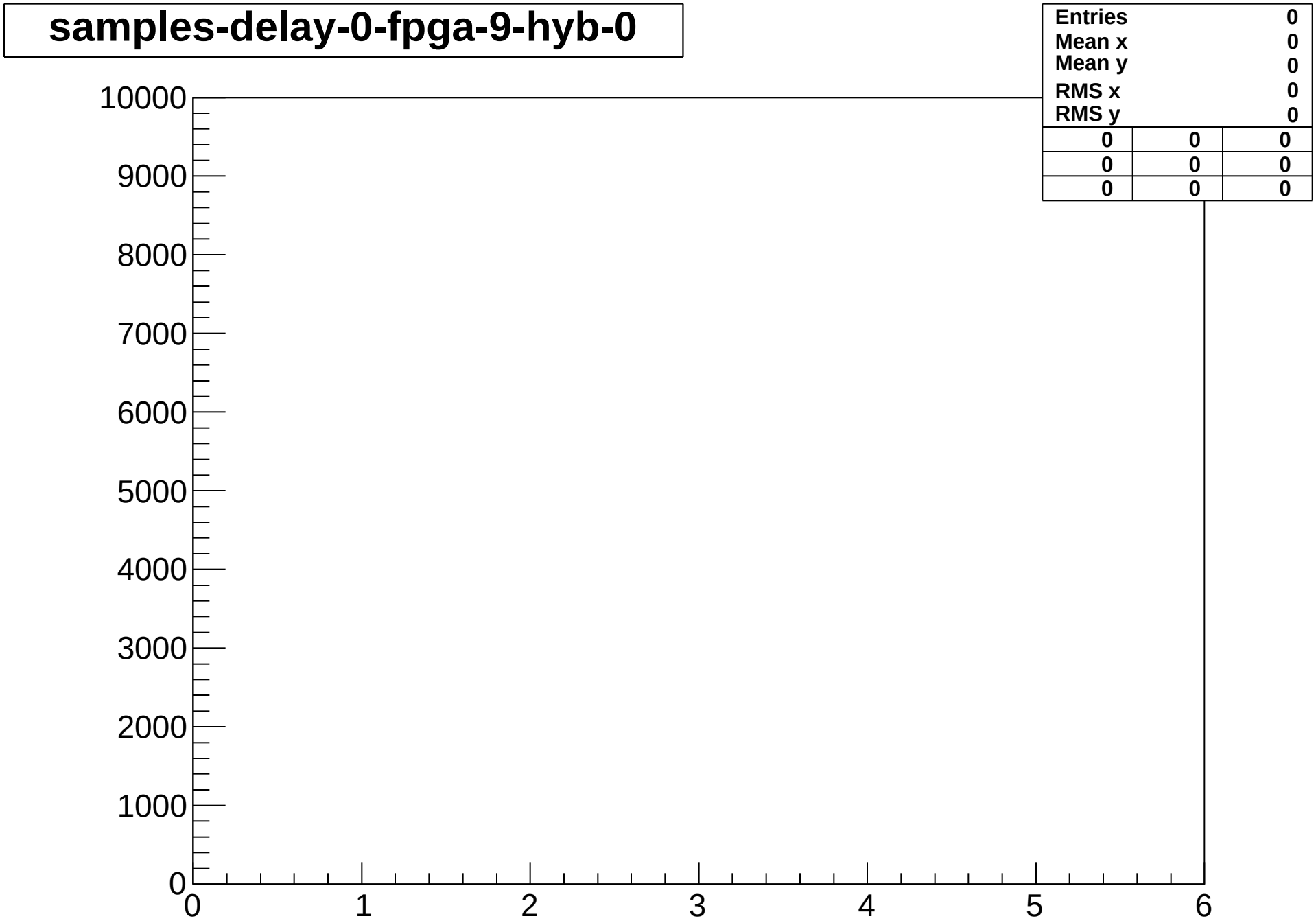
samples-delay-0-fpga-9-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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5000
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3000
2000
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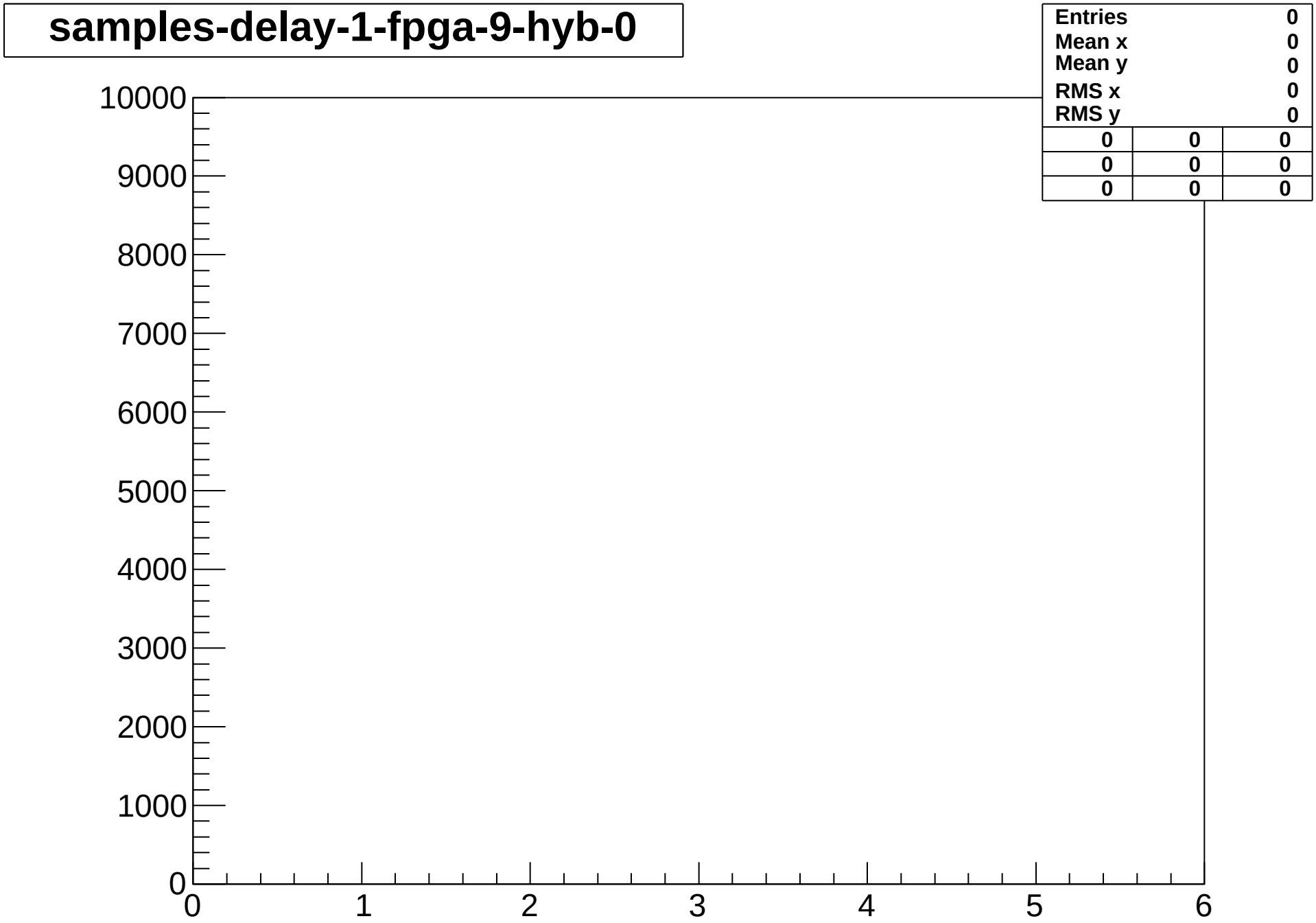
samples-delay-1-fpga-9-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
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0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
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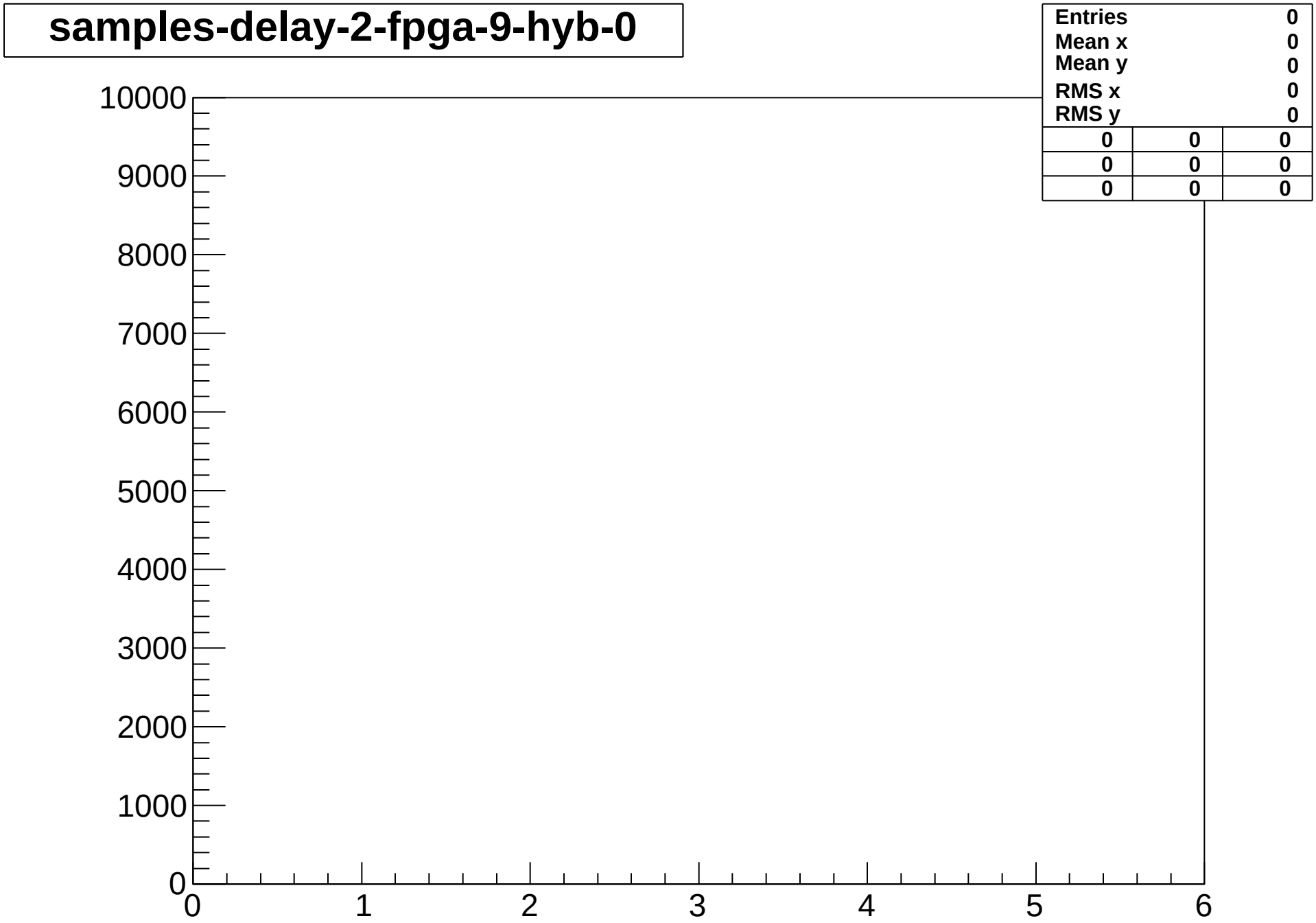
samples-delay-2-fpga-9-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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6000
5000
4000
3000
2000
1000
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1
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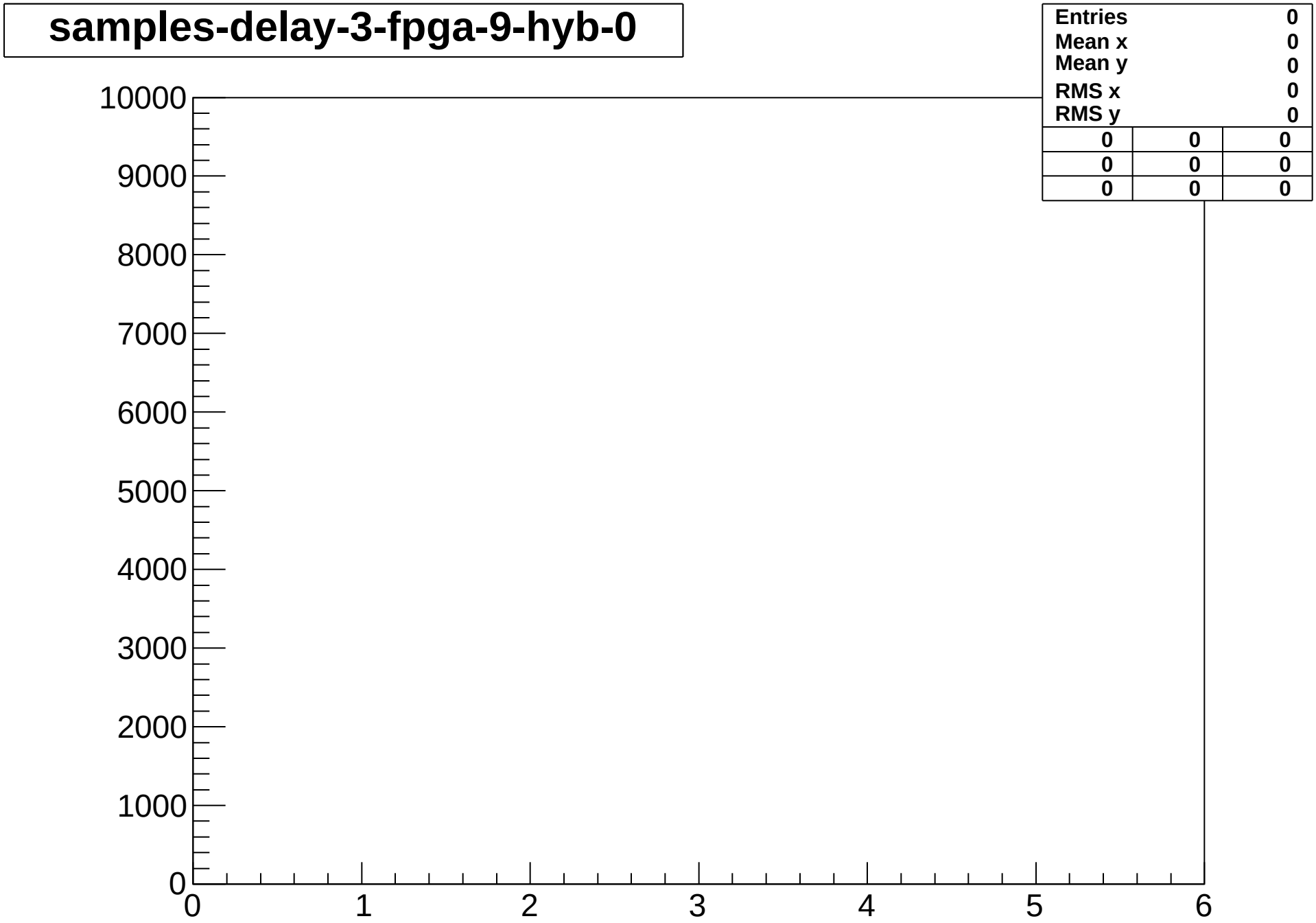
samples-delay-3-fpga-9-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
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6000
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4000
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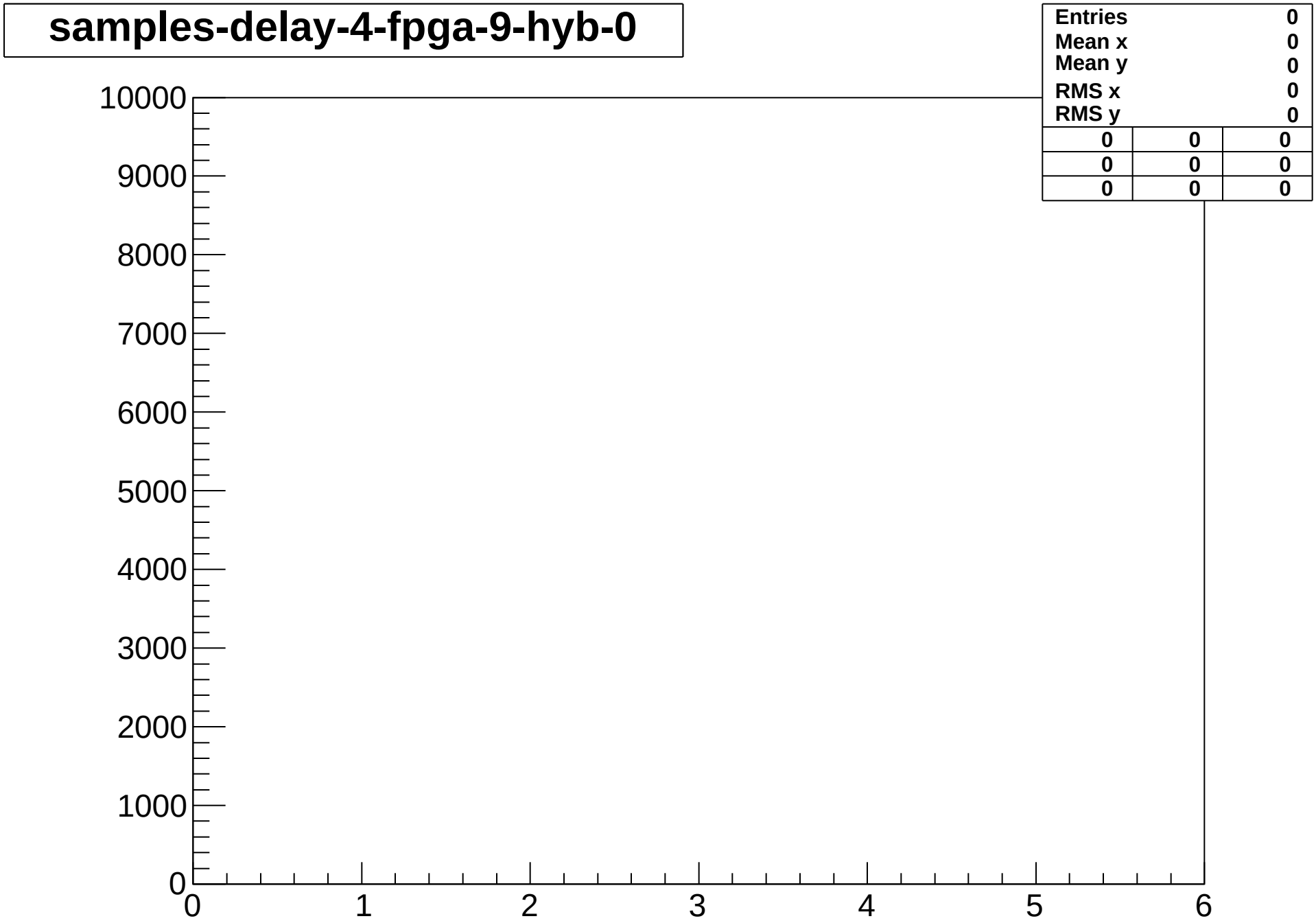
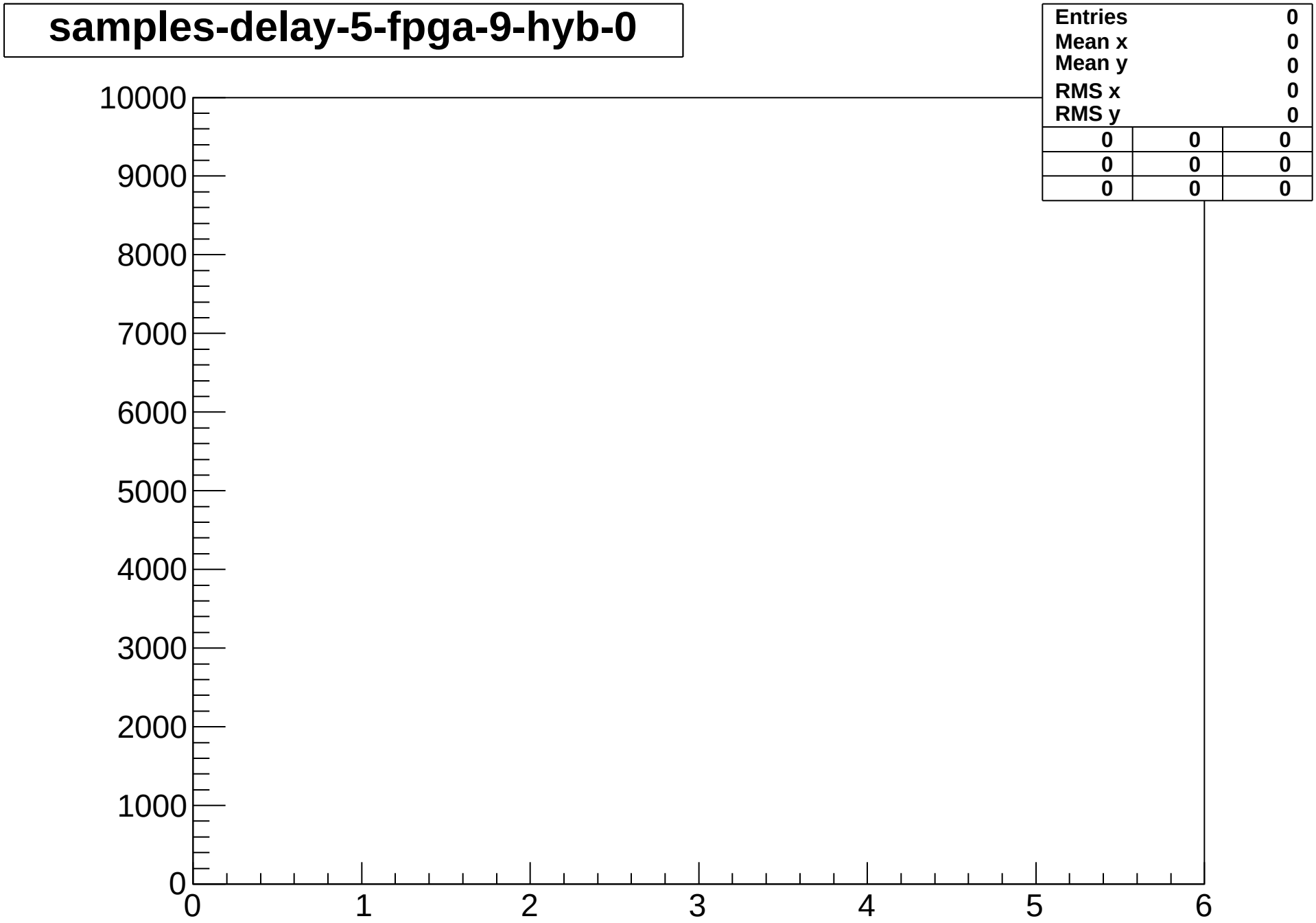
samples-delay-4-fpga-9-hyb-0




samples-delay-5-fpga-9-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
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3
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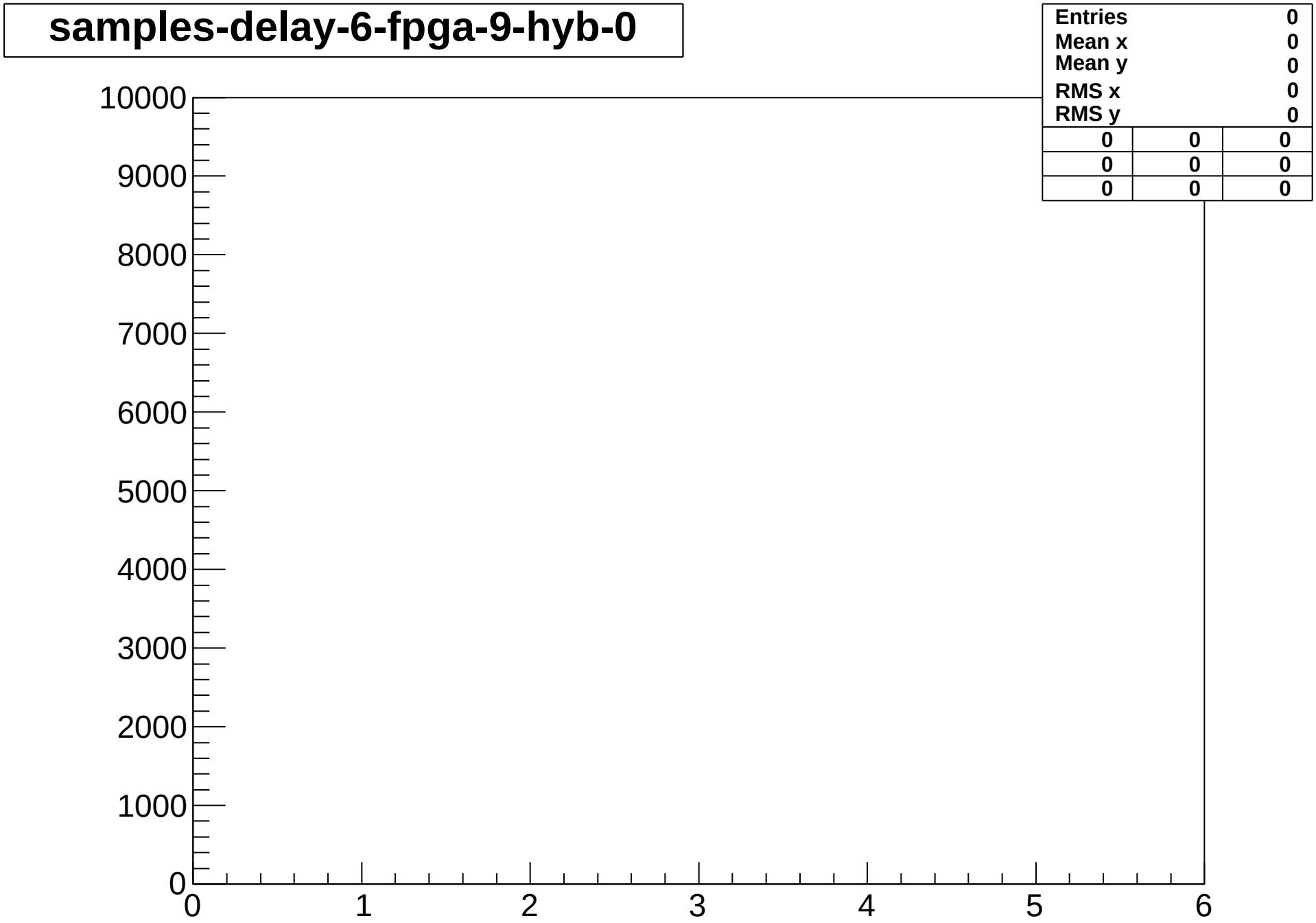
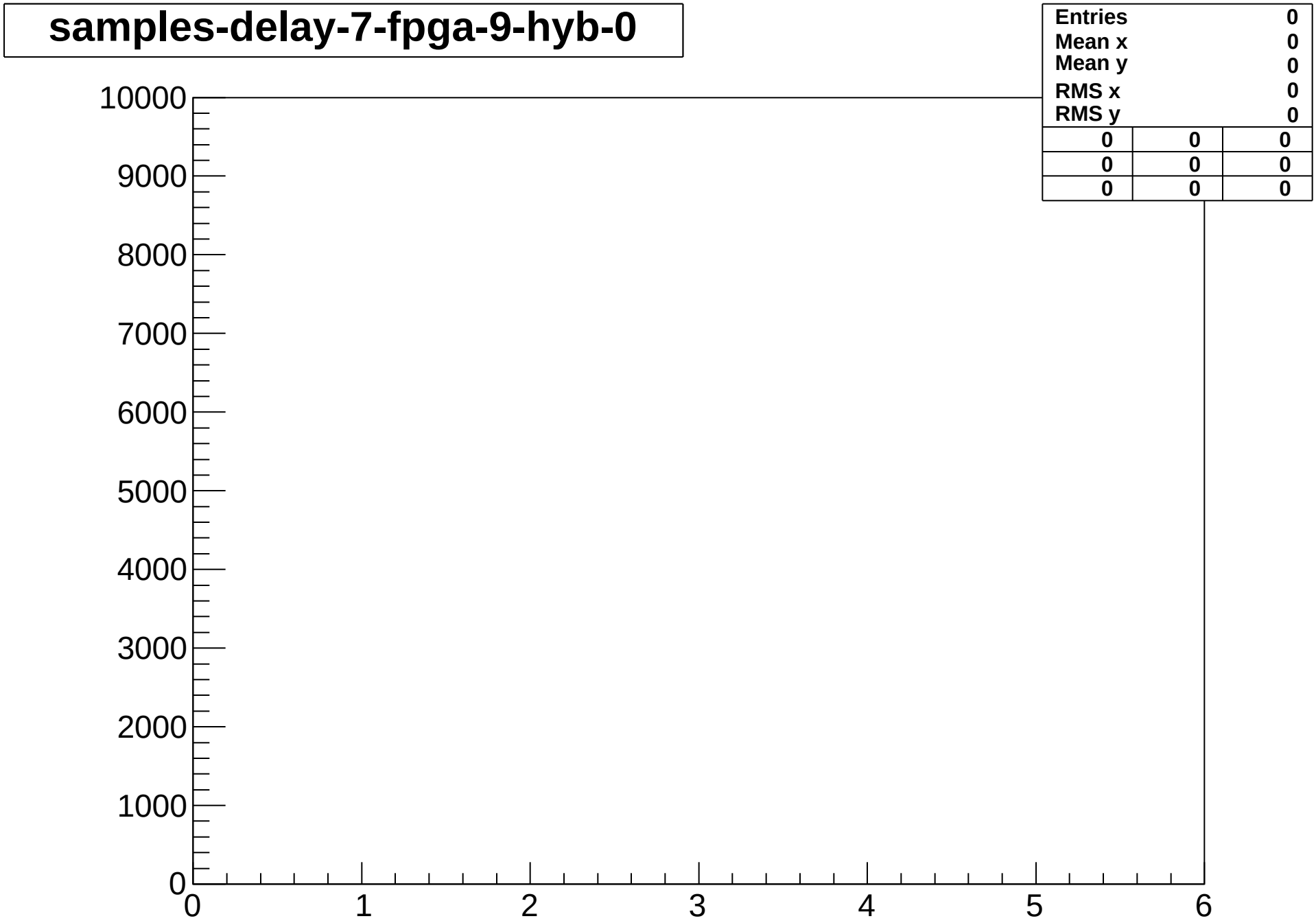
samples-delay-6-fpga-9-hyb-0




samples-delay-7-fpga-9-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
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7000
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5000
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3000
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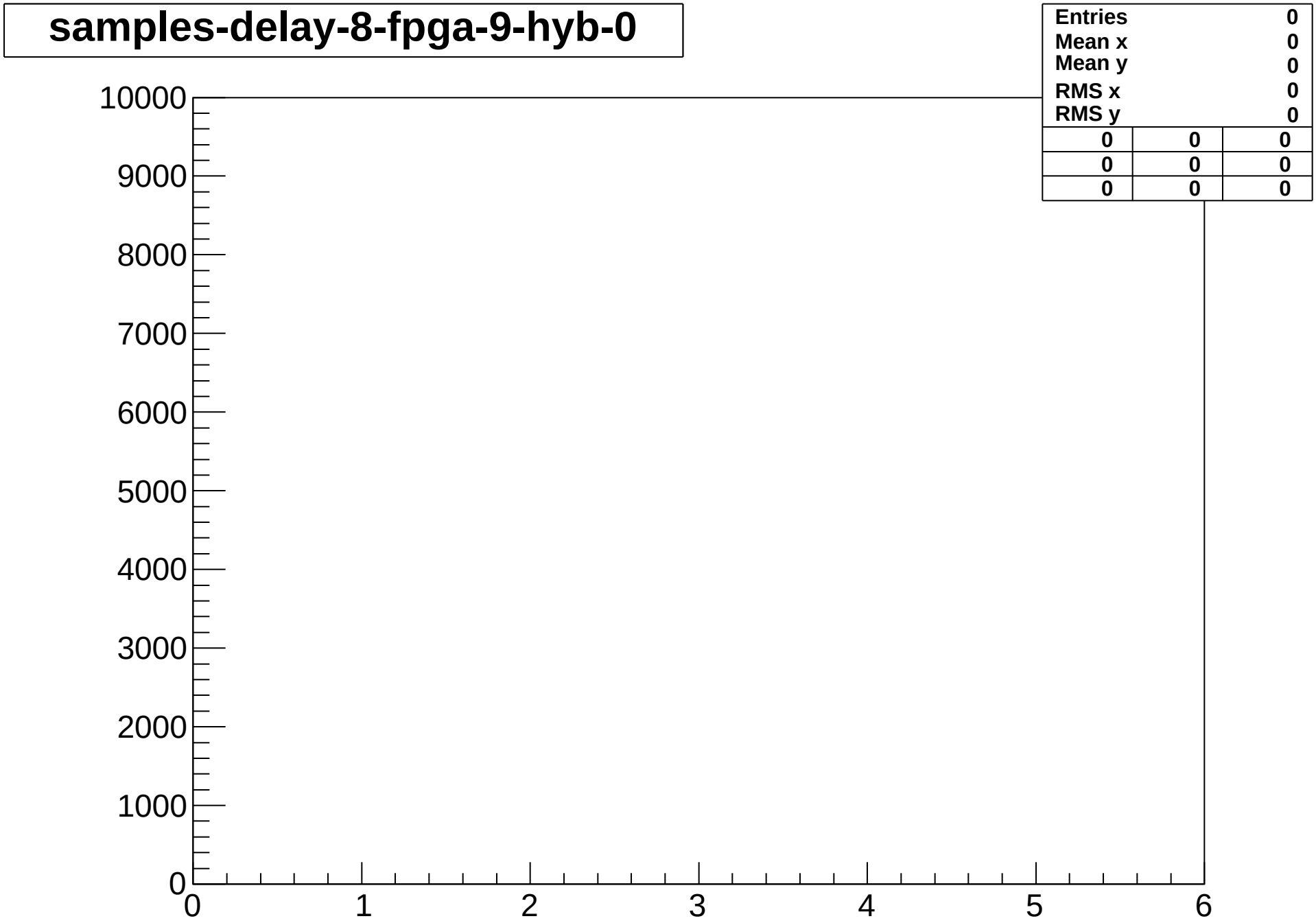
samples-delay-8-fpga-9-hyb-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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0
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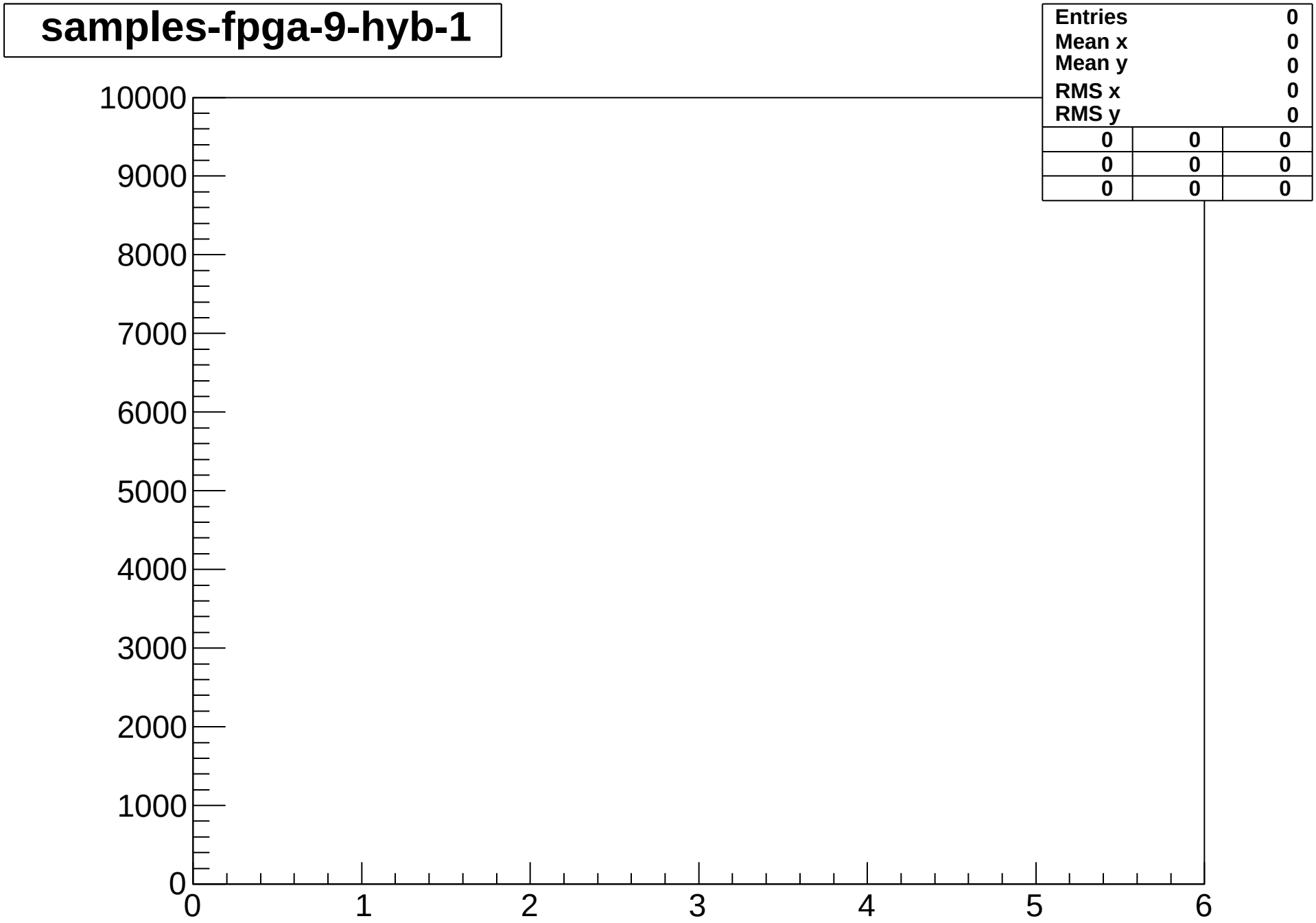
6


samples-fpga-9-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
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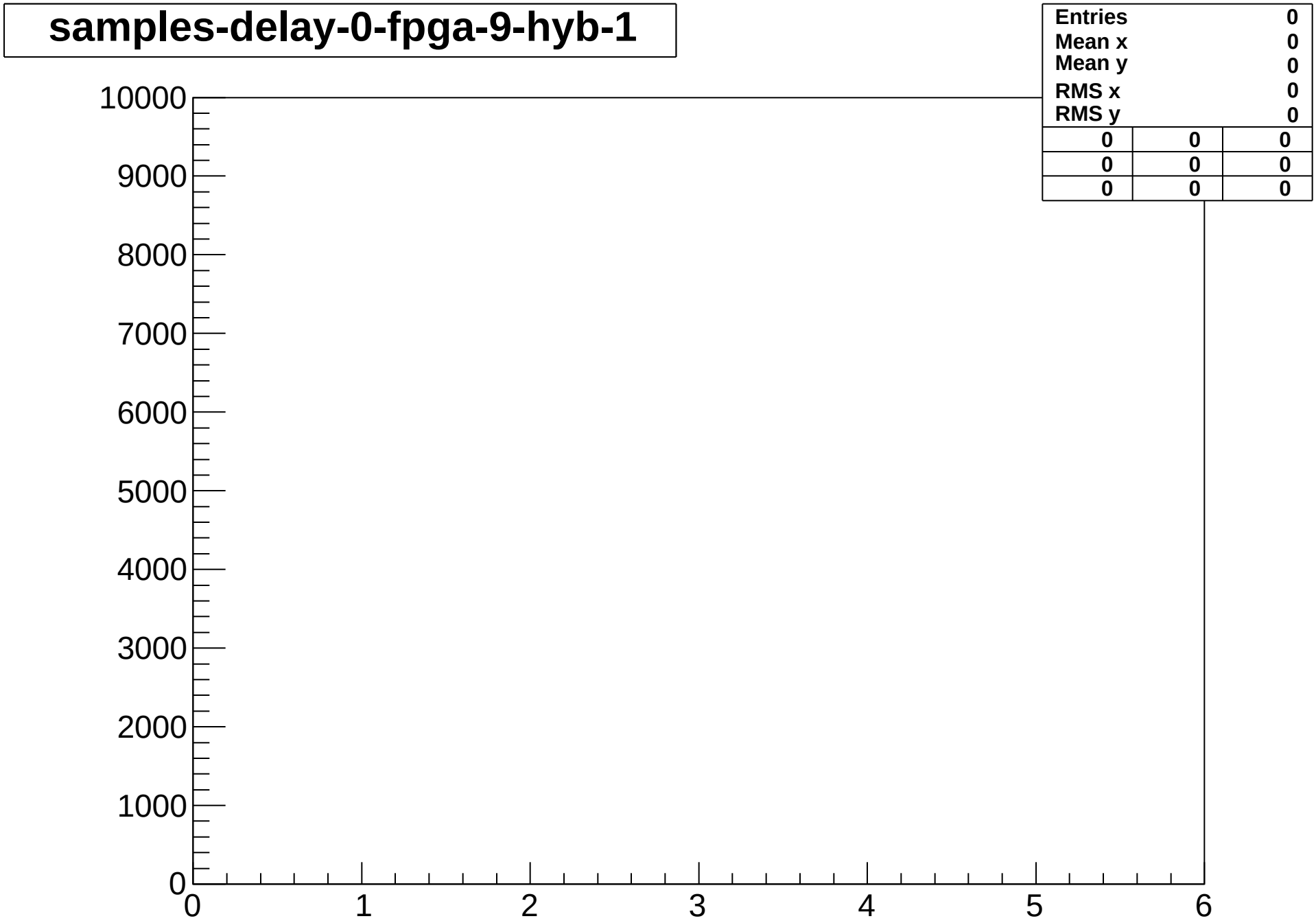
samples-delay-0-fpga-9-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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6000
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4000
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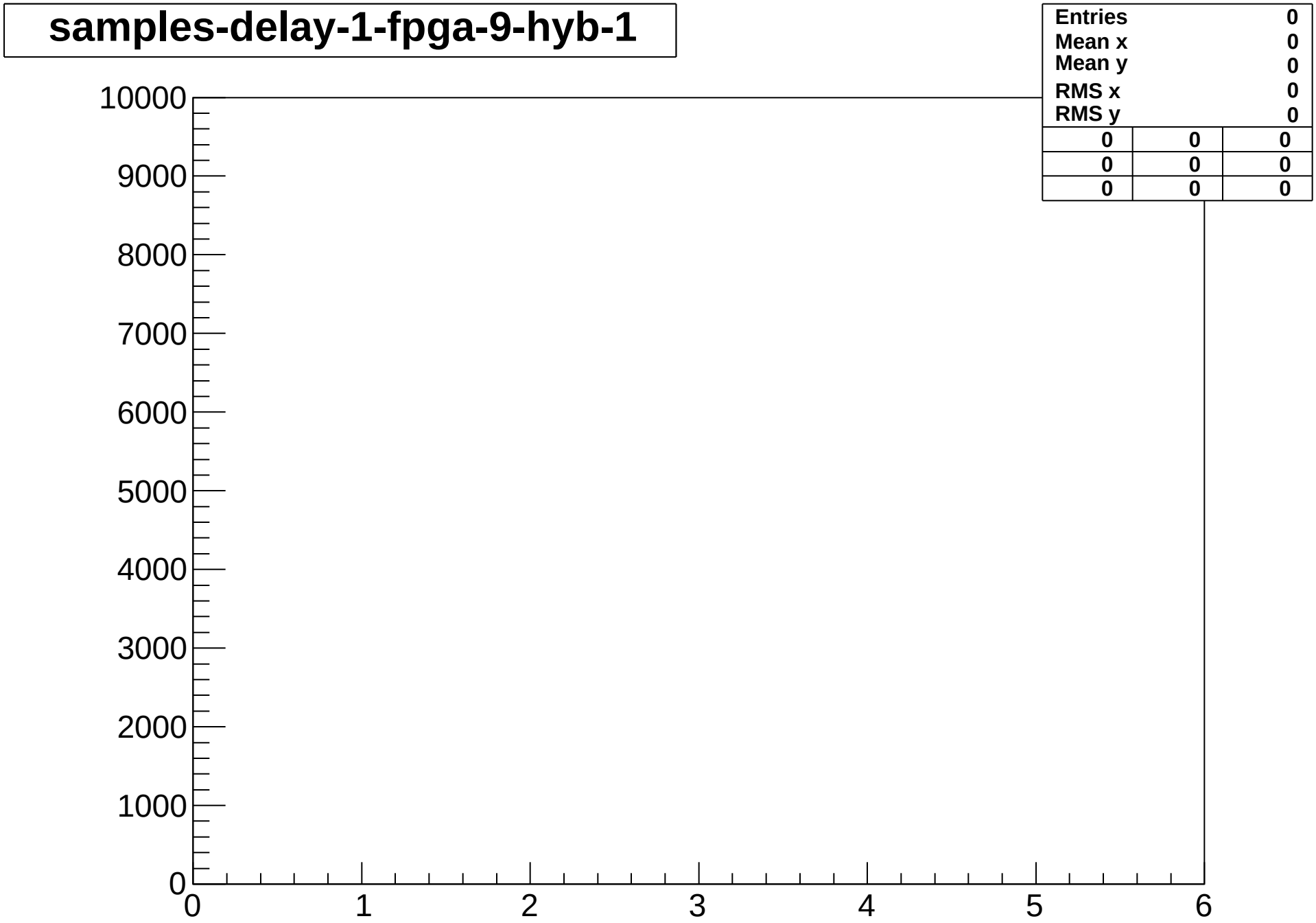
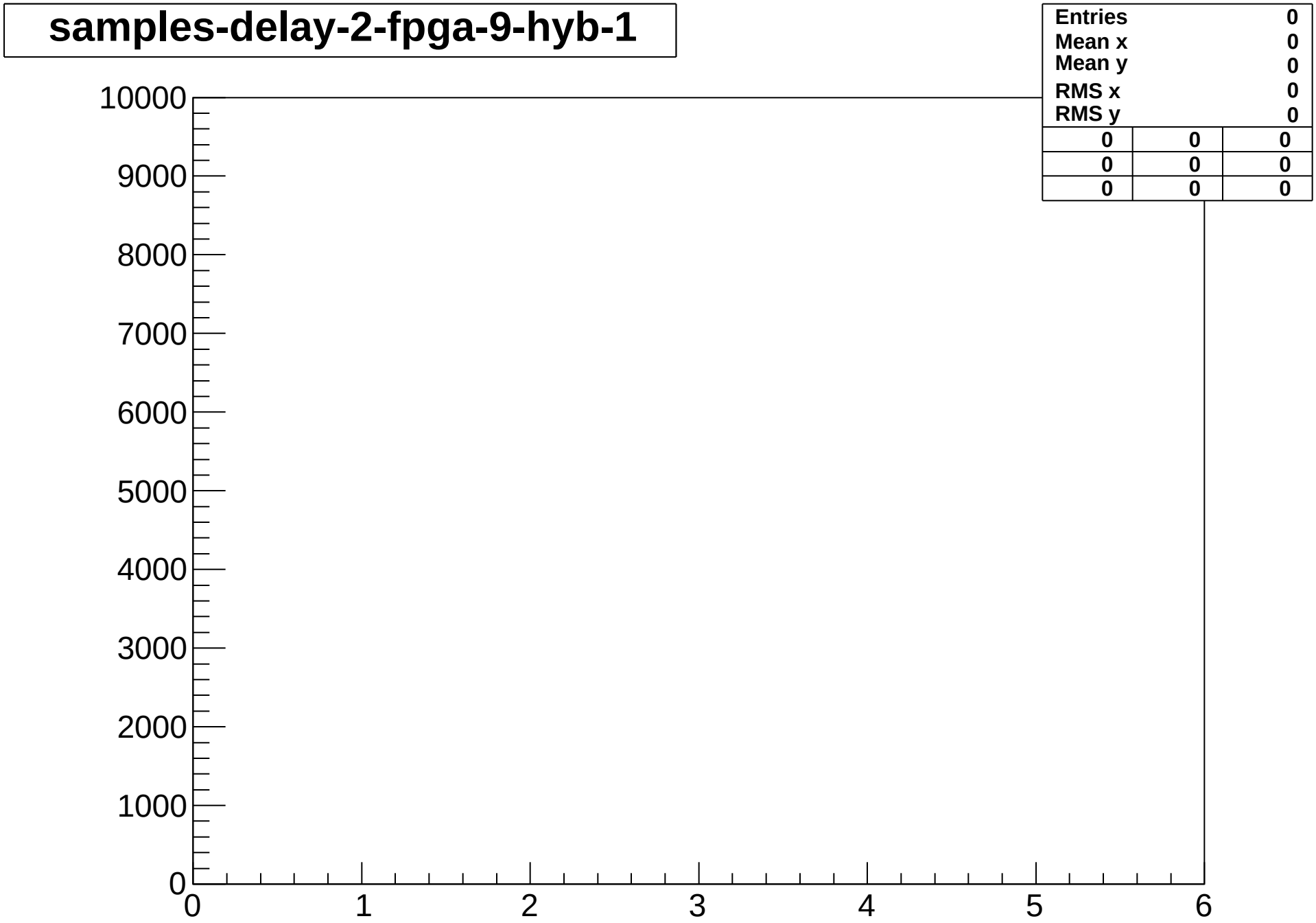
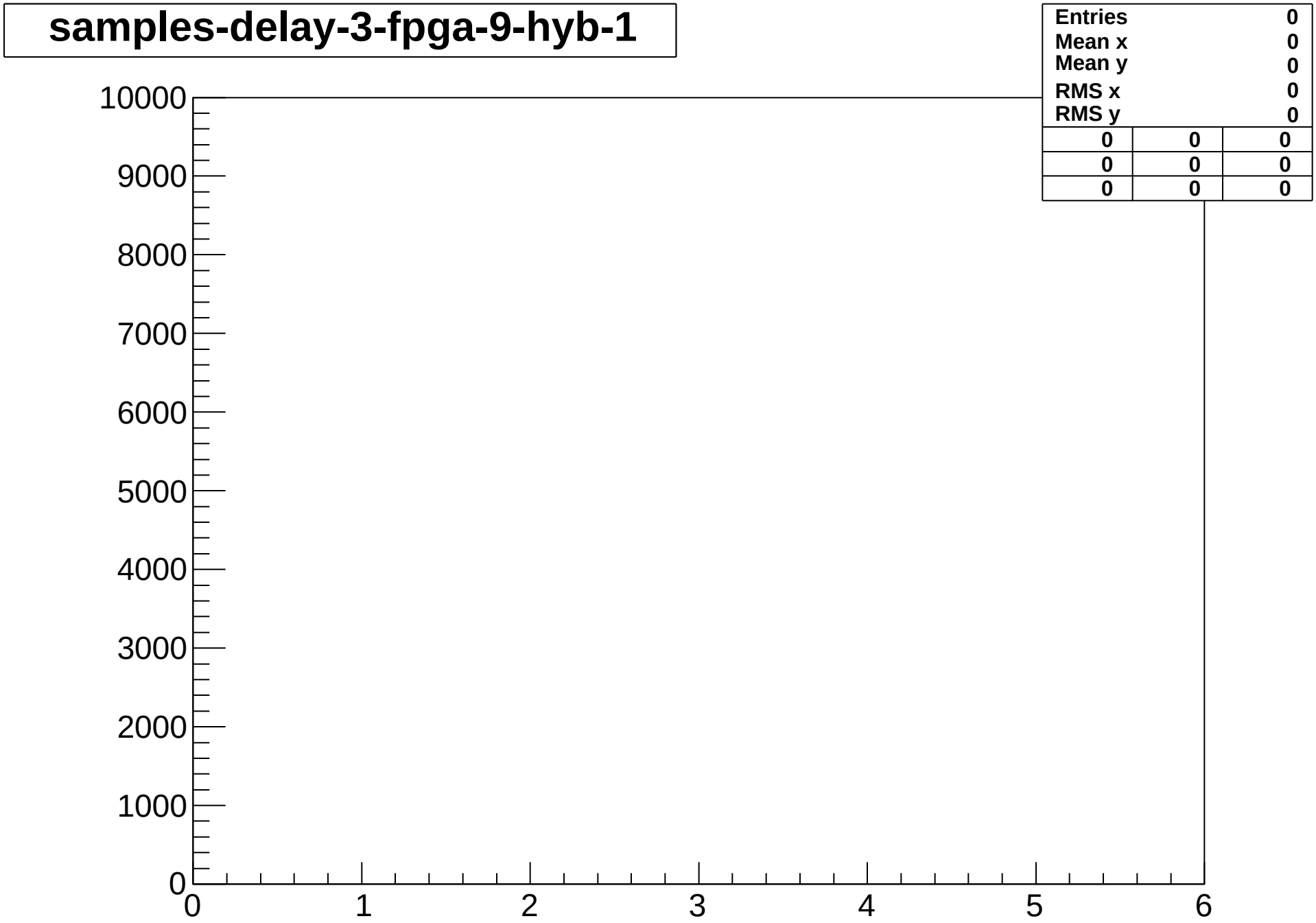
samples-delay-1-fpga-9-hyb-1



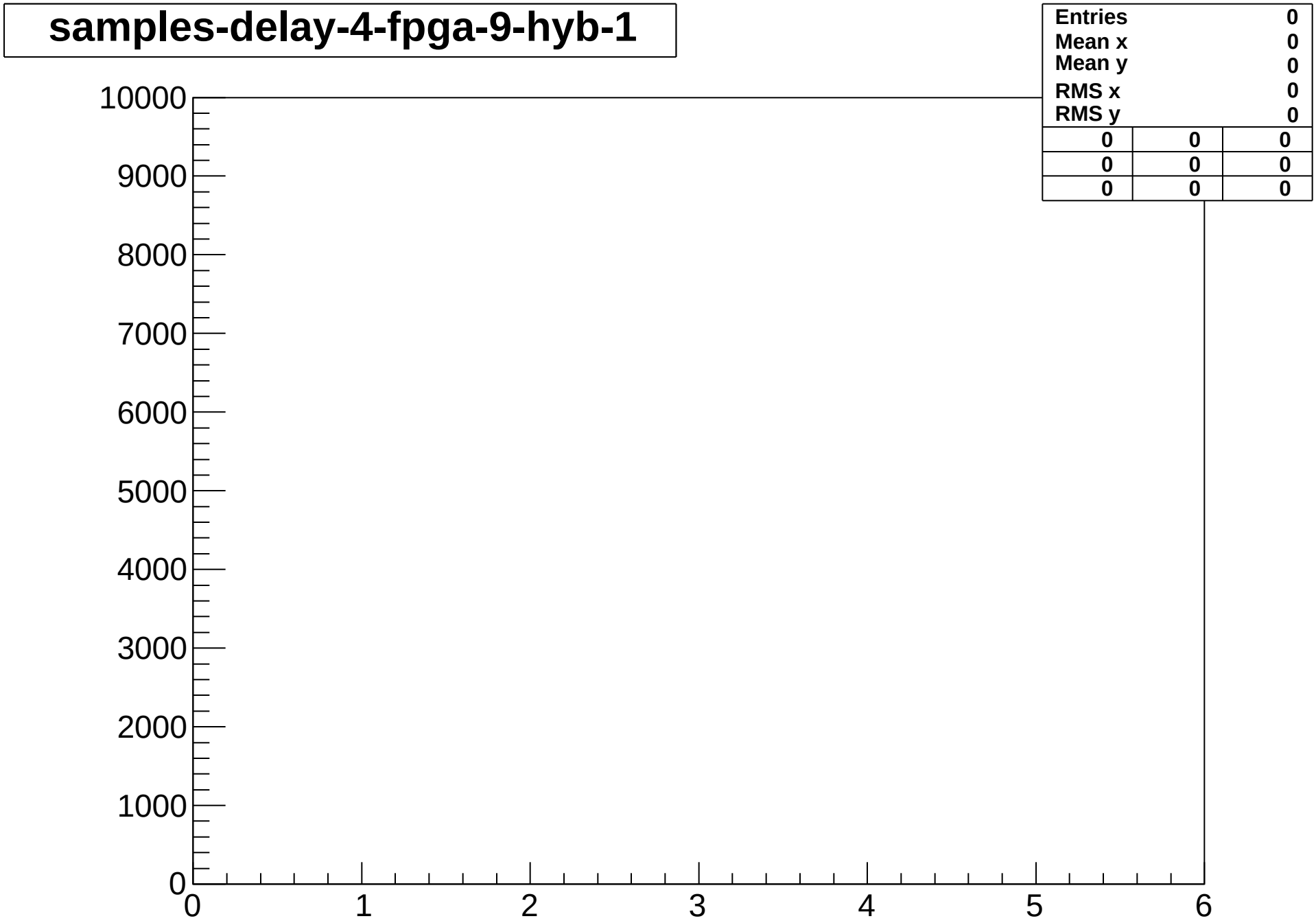
samples-delay-2-fpga-9-hyb-1

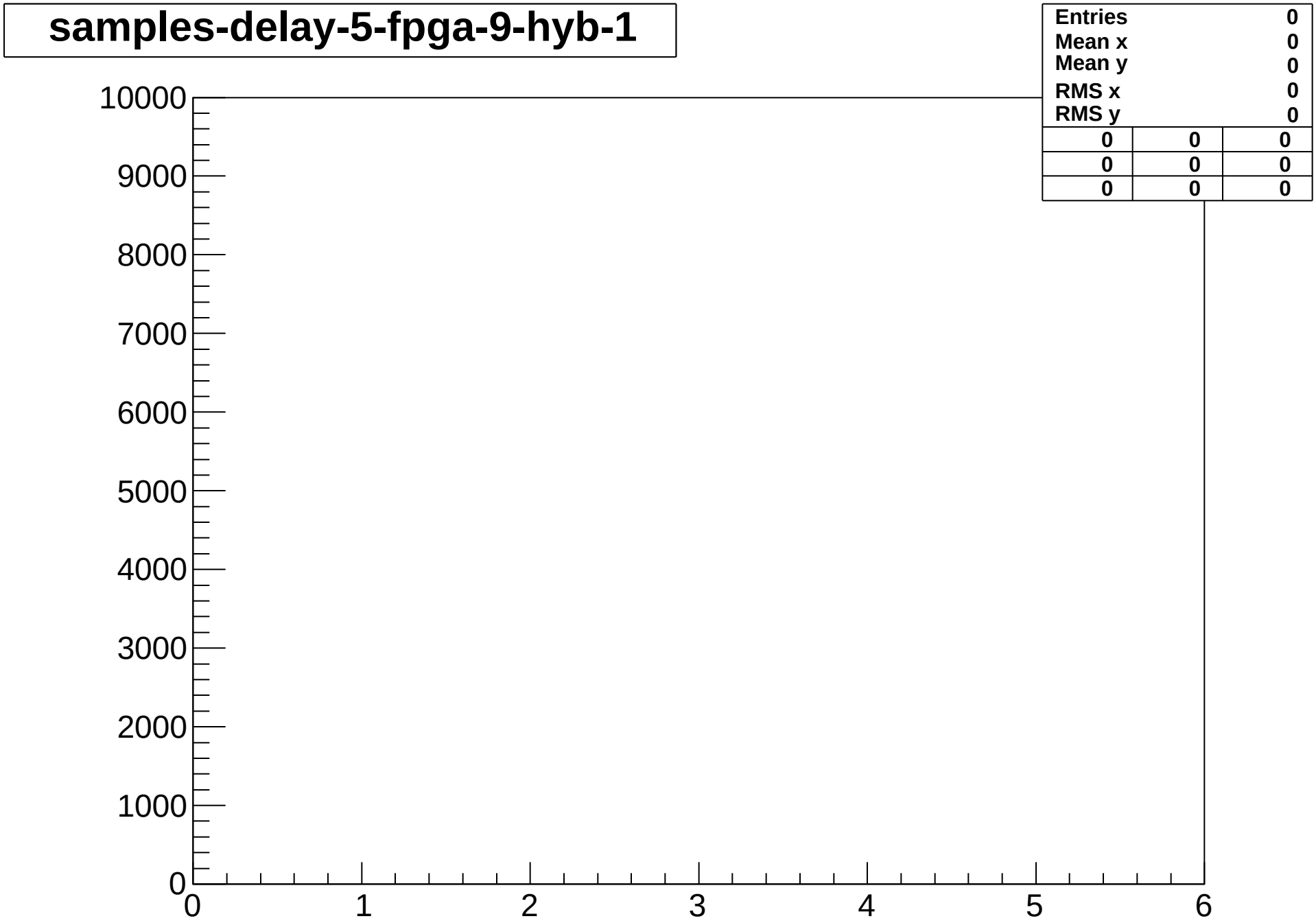


samples-delay-3-fpga-9-hyb-1



samples-delay-4-fpga-9-hyb-1




samples-delay-5-fpga-9-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
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9000
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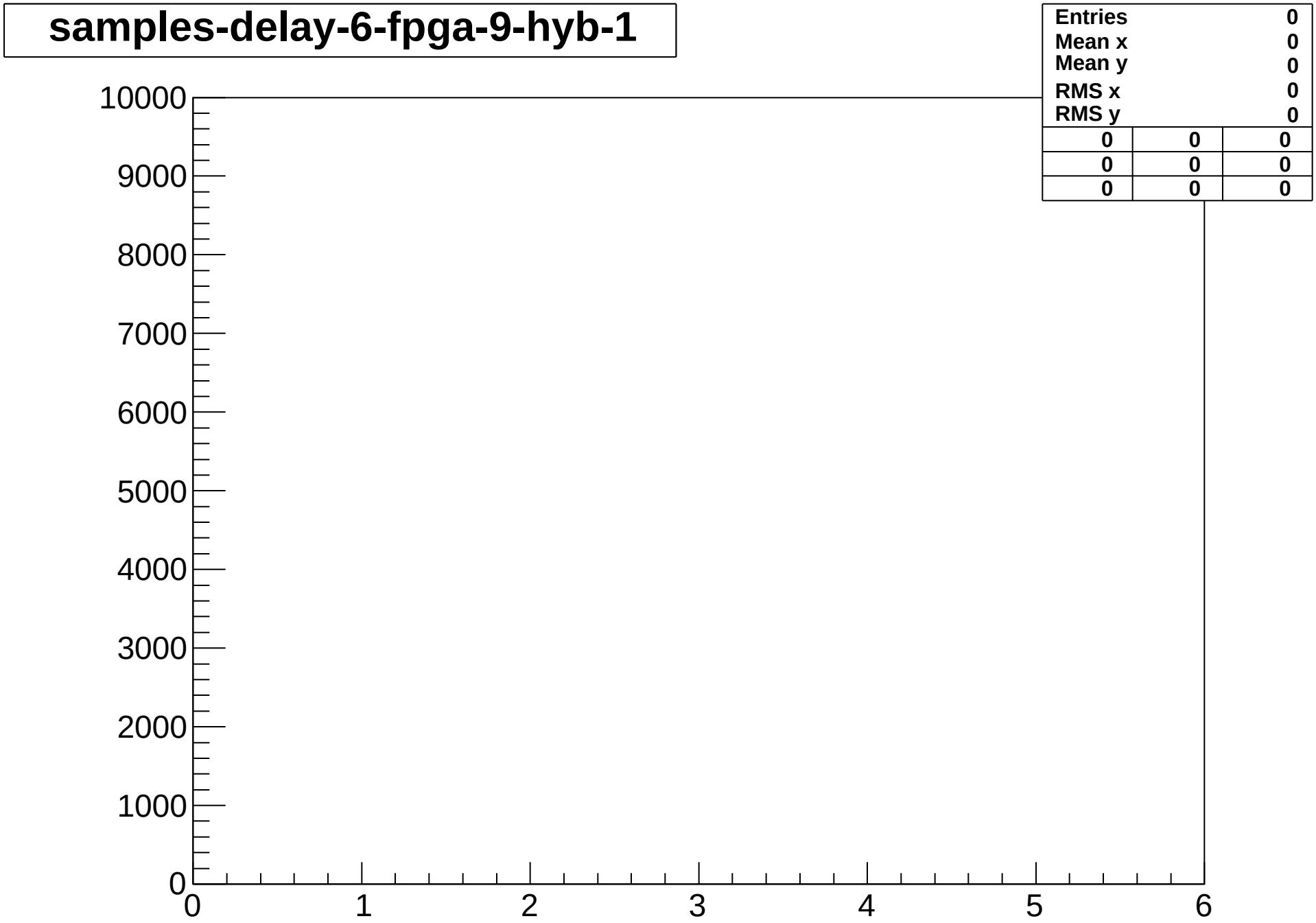
samples-delay-6-fpga-9-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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4000
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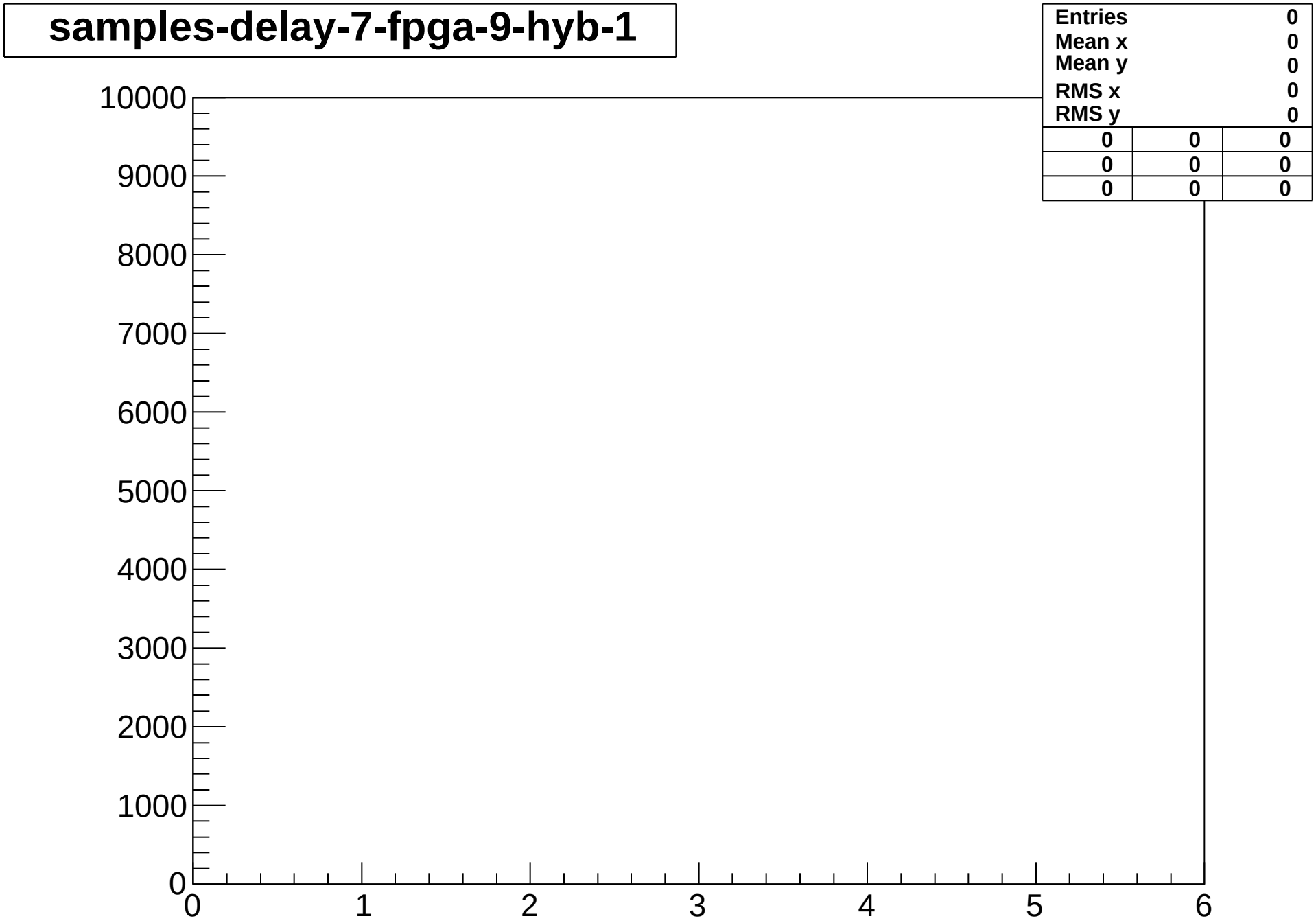
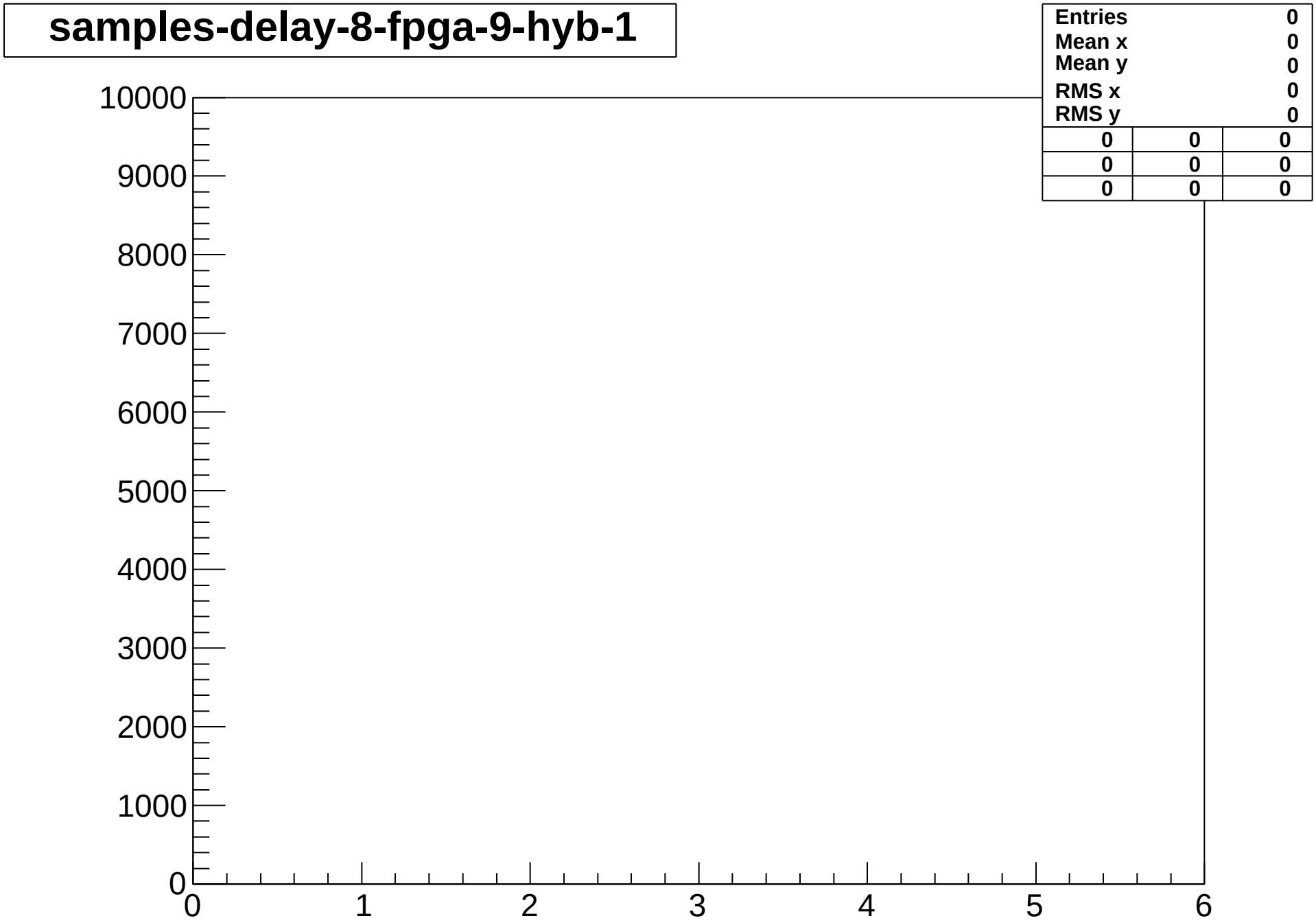
samples-delay-7-fpga-9-hyb-1




samples-delay-8-fpga-9-hyb-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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10000
9000
8000
7000
6000
5000
4000
3000
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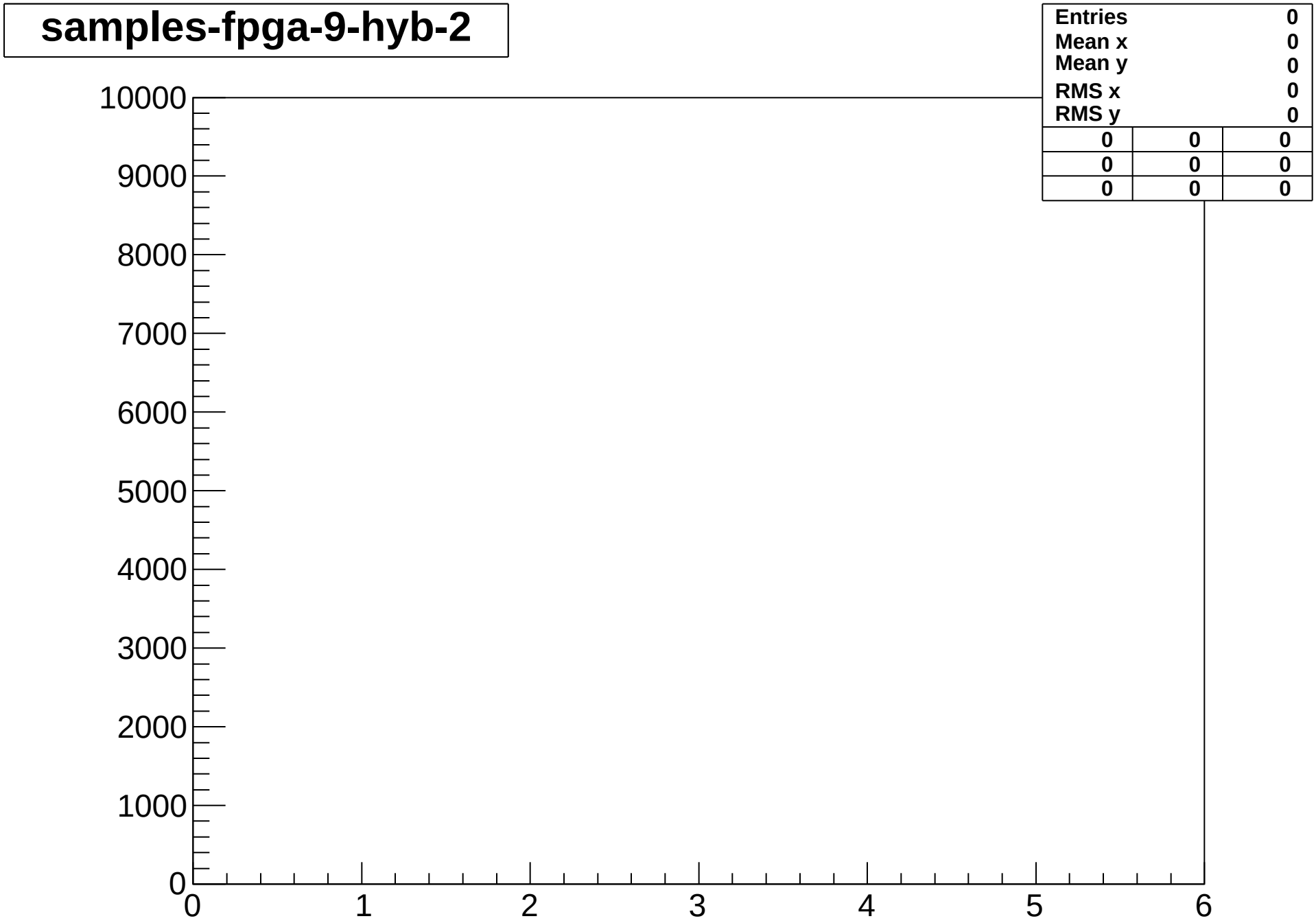
samples-fpga-9-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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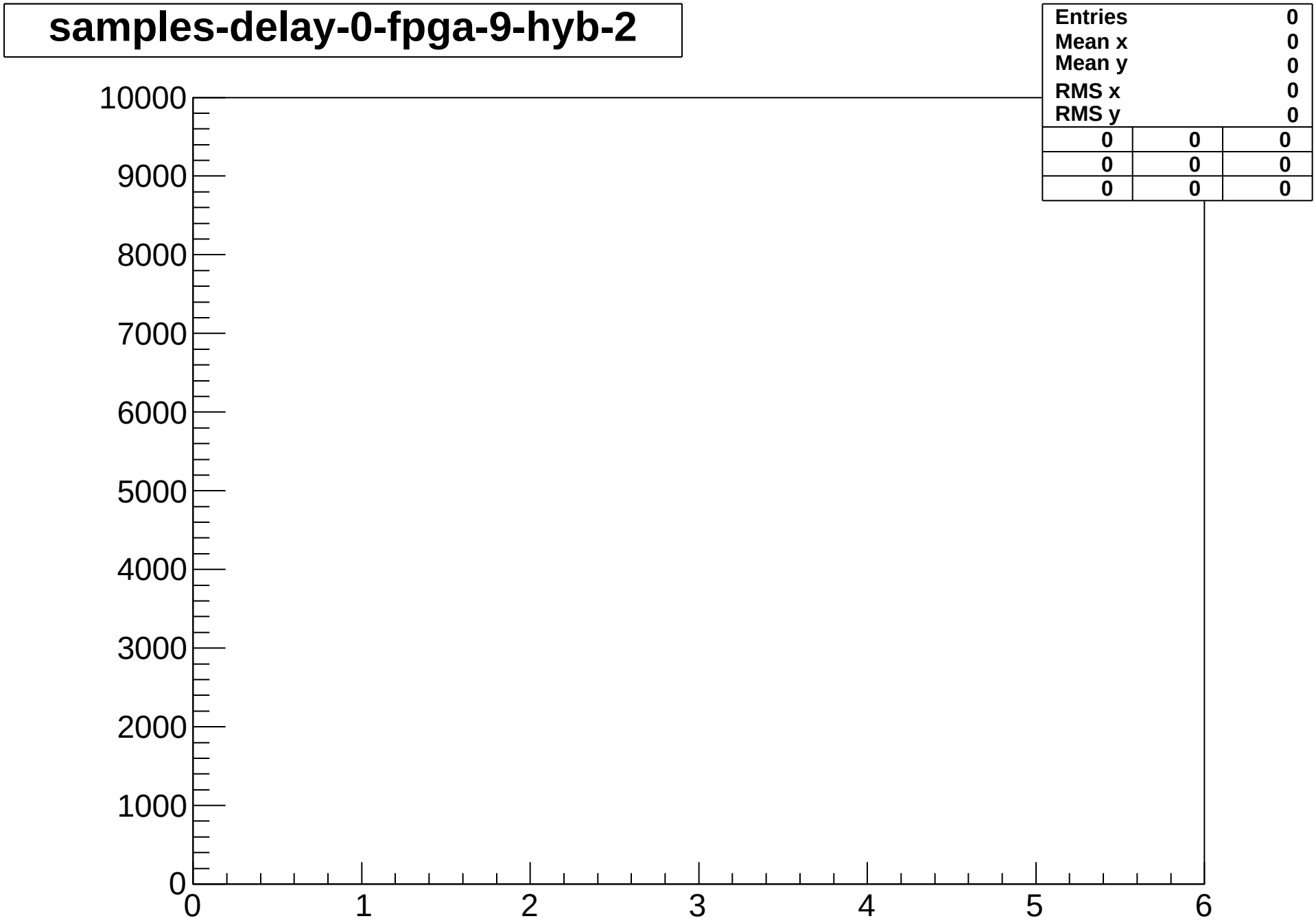
samples-delay-0-fpga-9-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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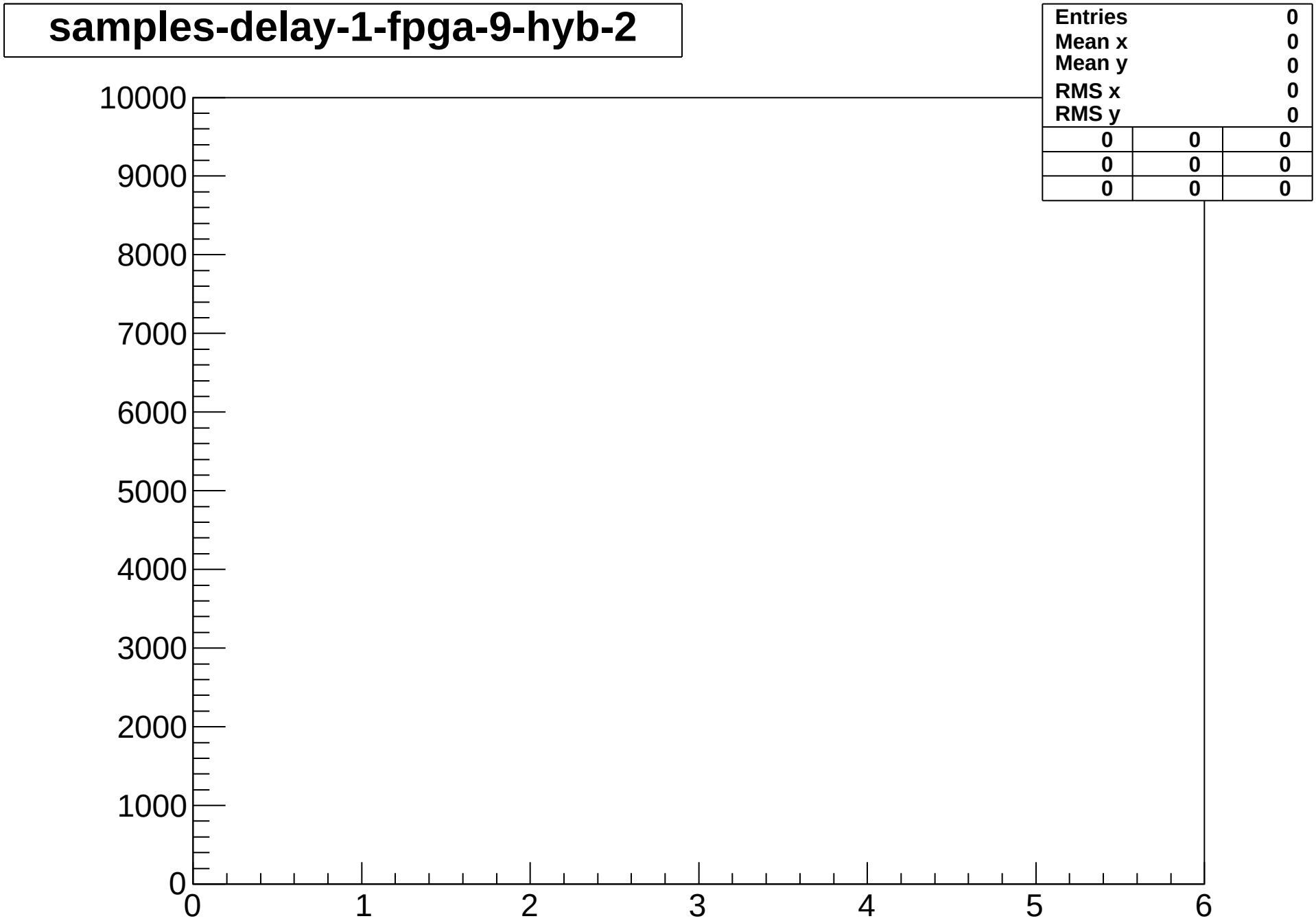
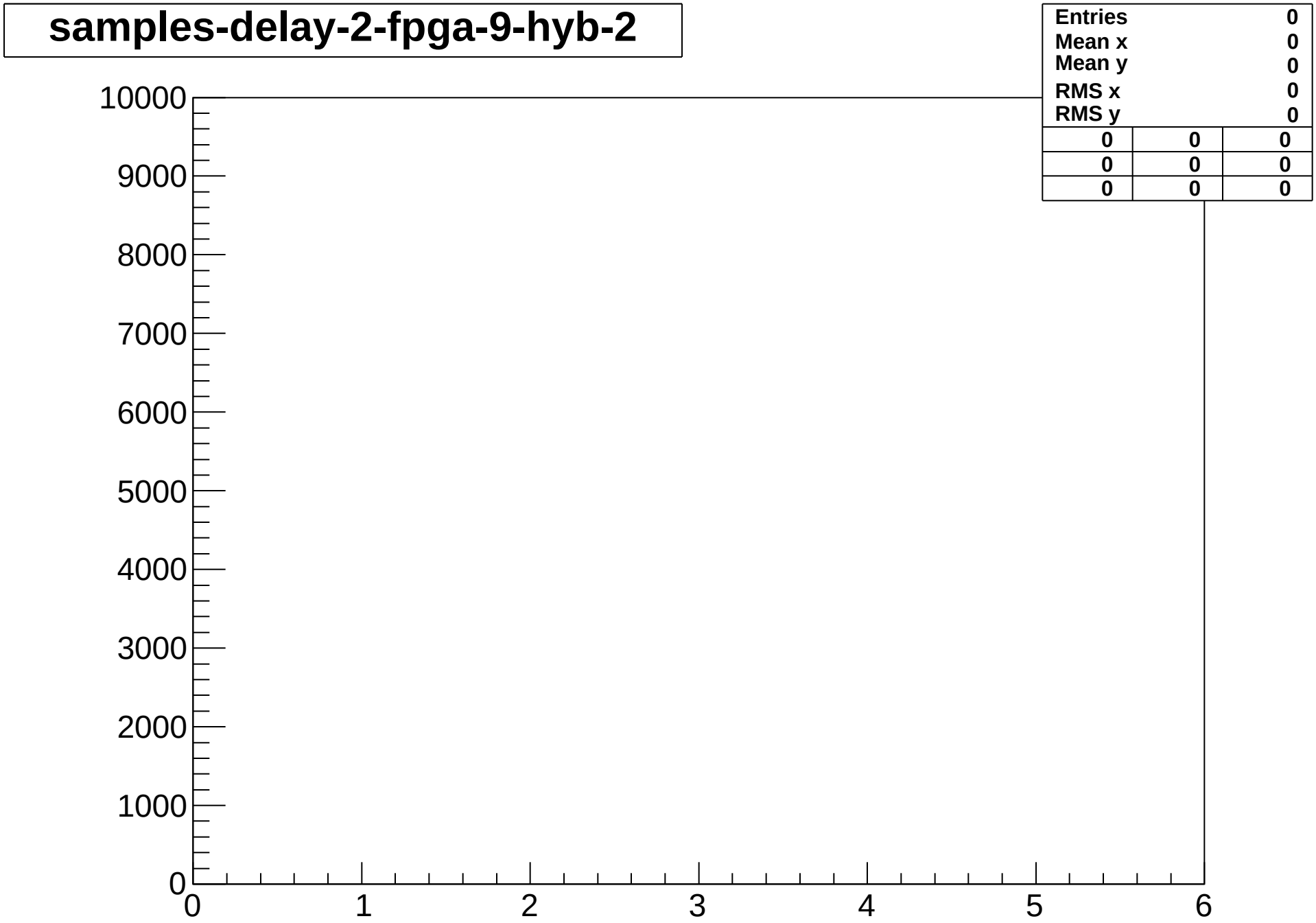
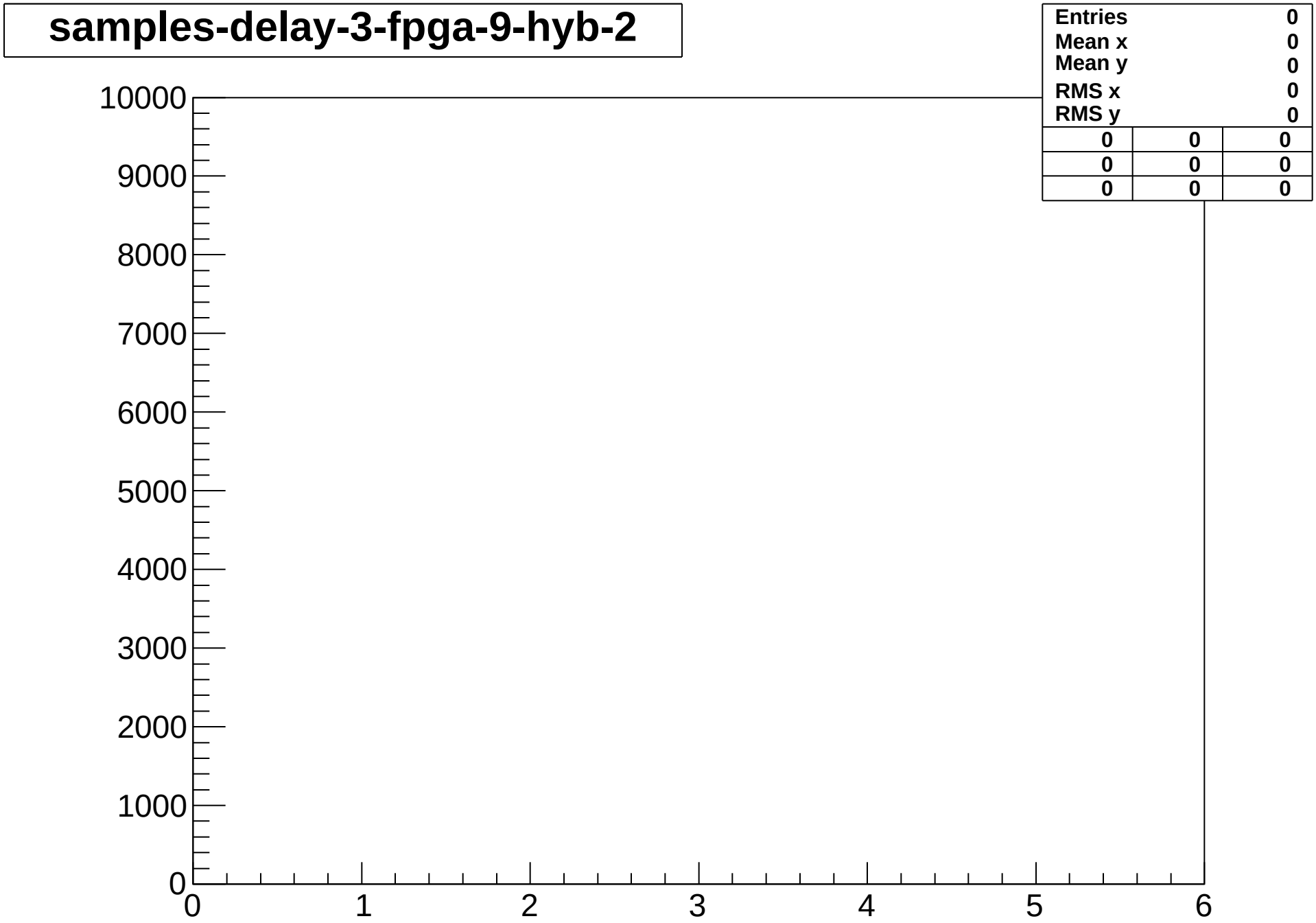
samples-delay-1-fpga-9-hyb-2



samples-delay-2-fpga-9-hyb-2




samples-delay-3-fpga-9-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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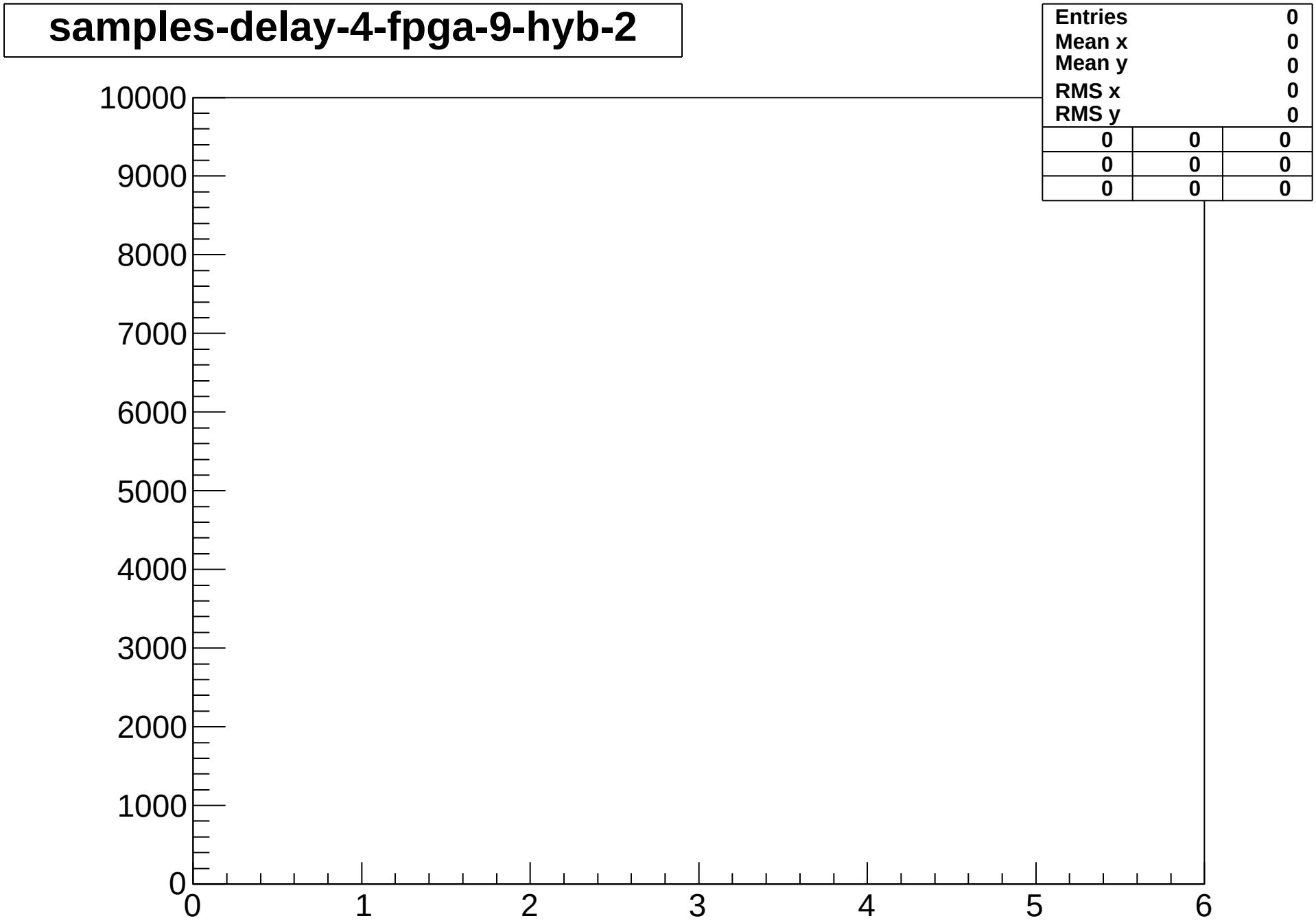
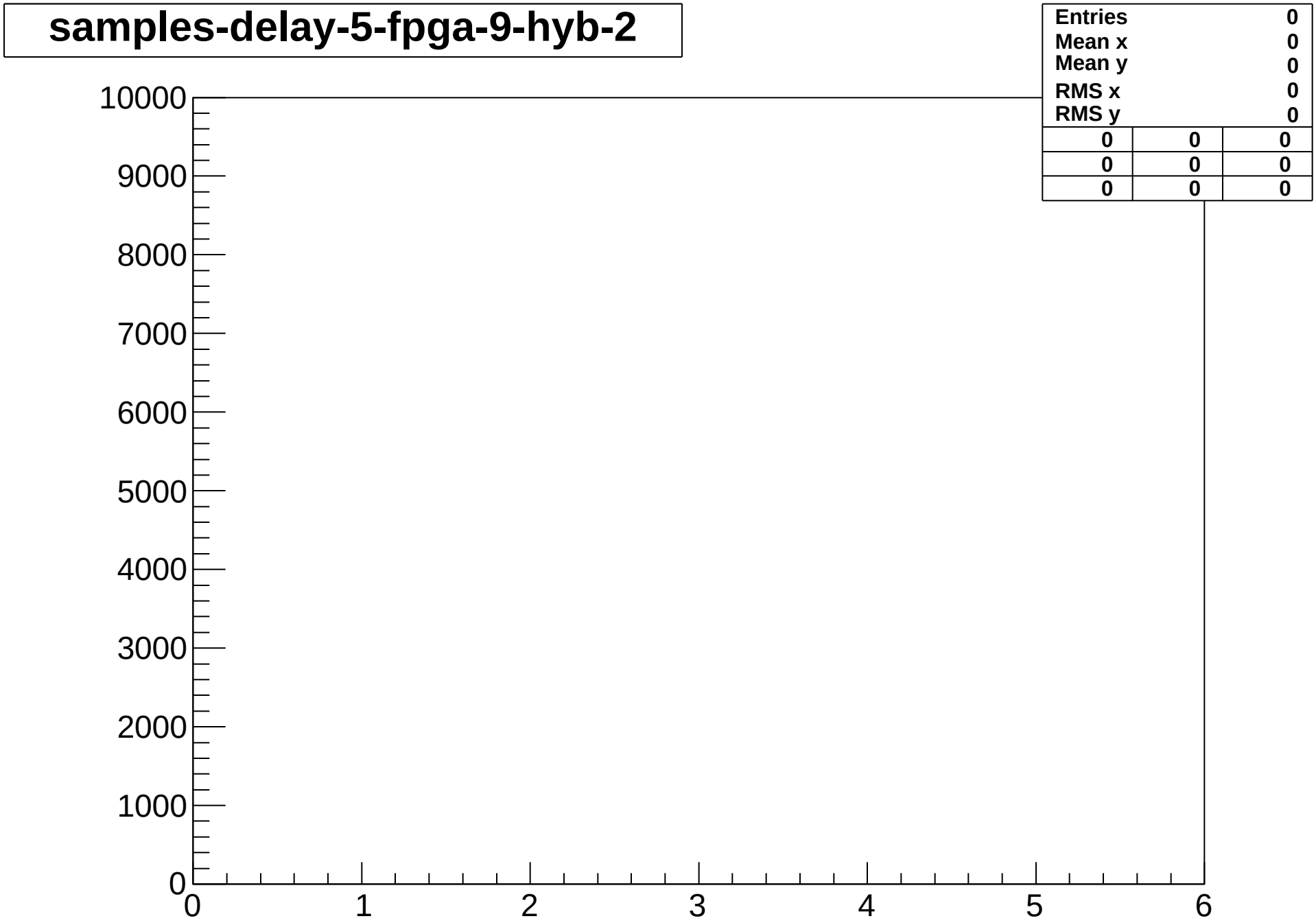
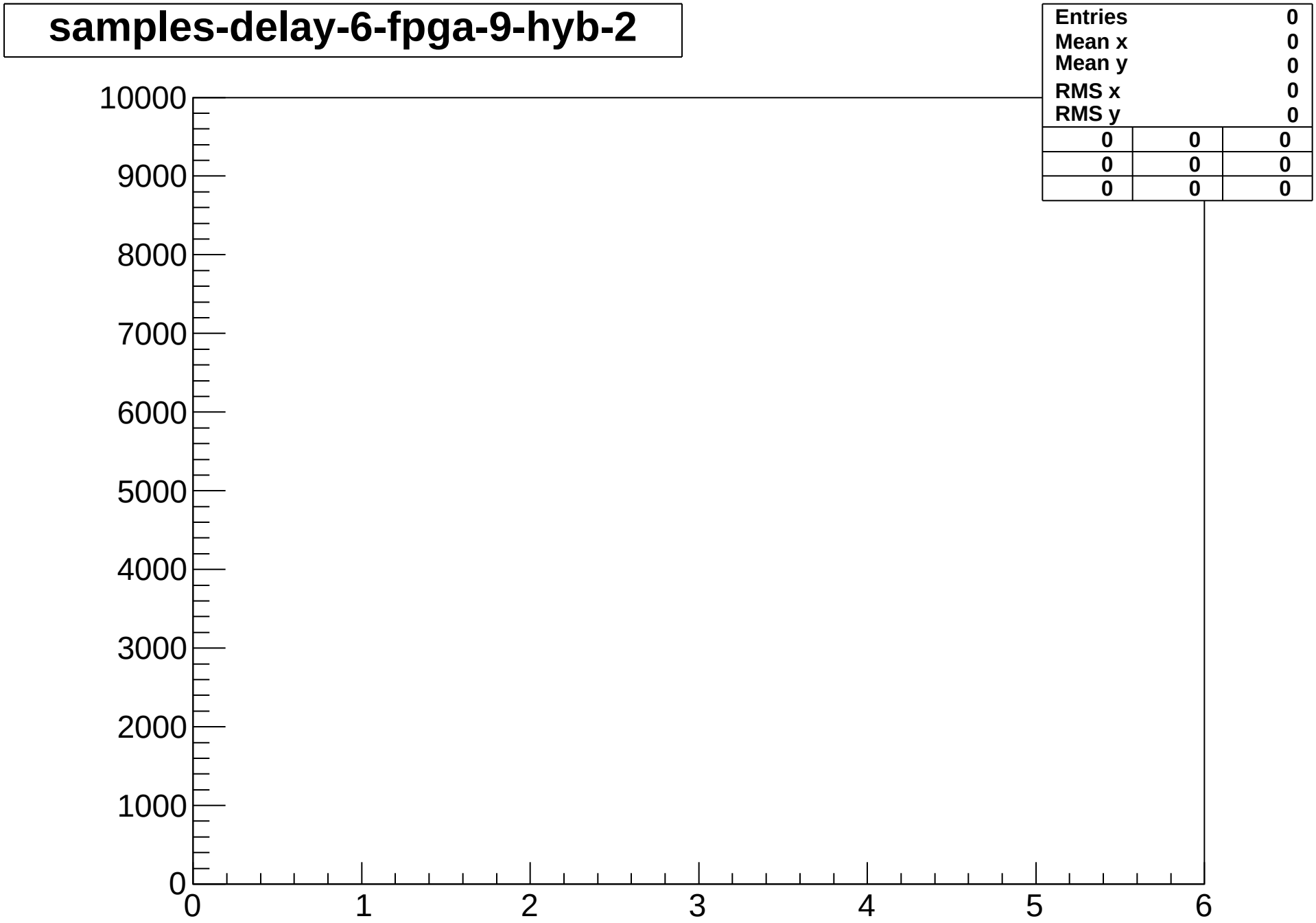
samples-delay-4-fpga-9-hyb-2

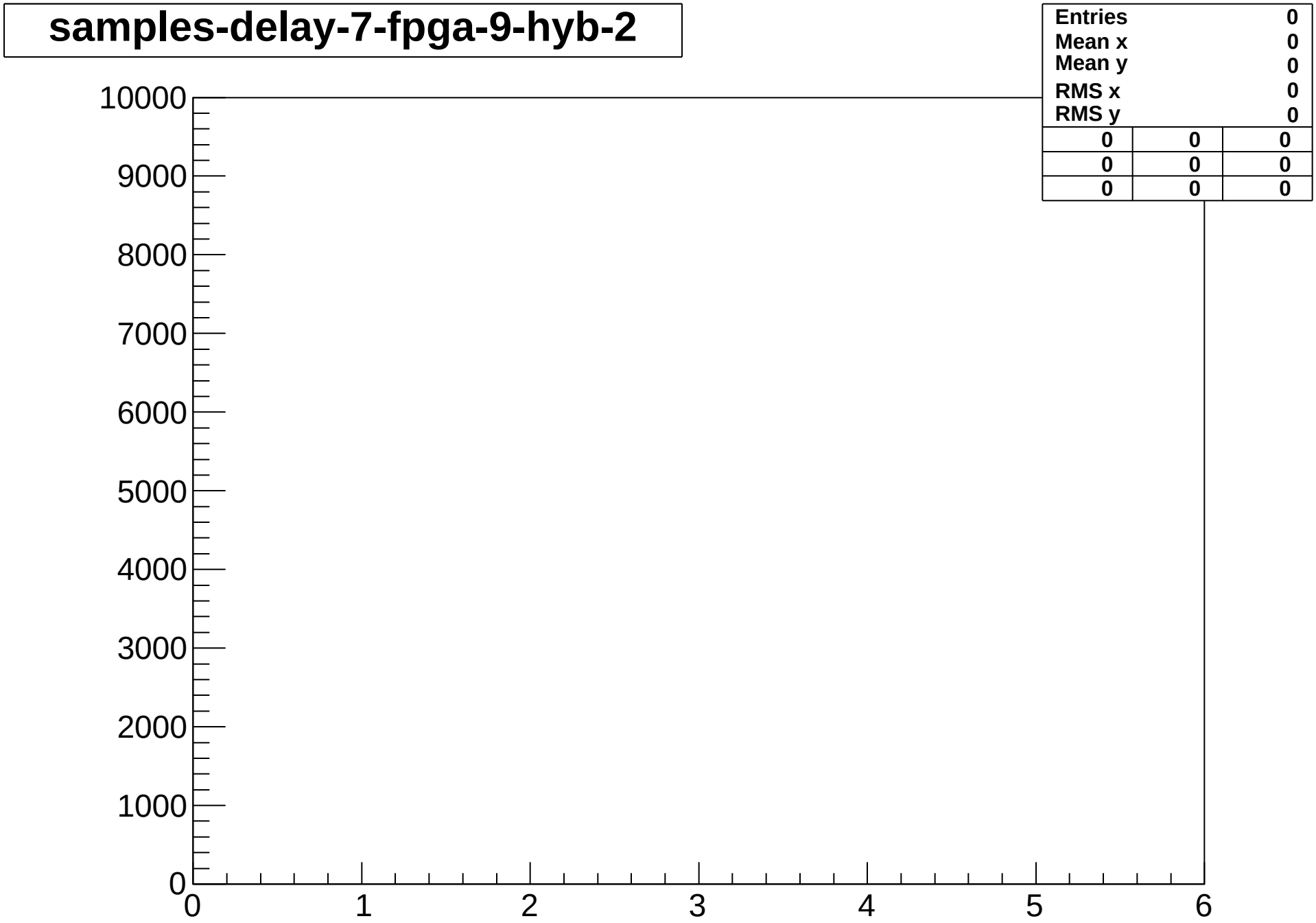


samples-delay-5-fpga-9-hyb-2



samples-delay-6-fpga-9-hyb-2




samples-delay-7-fpga-9-hyb-2
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
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4000
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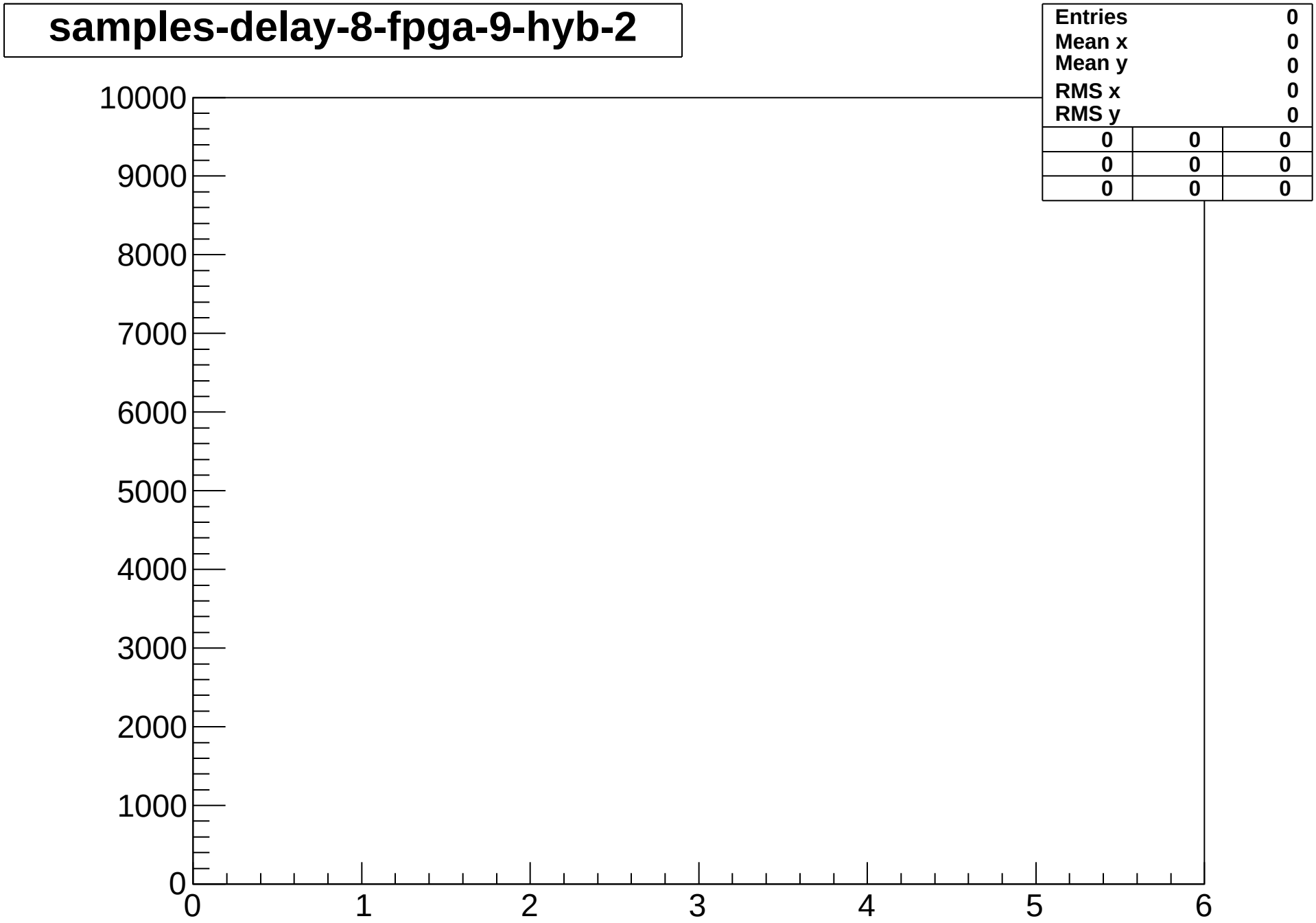
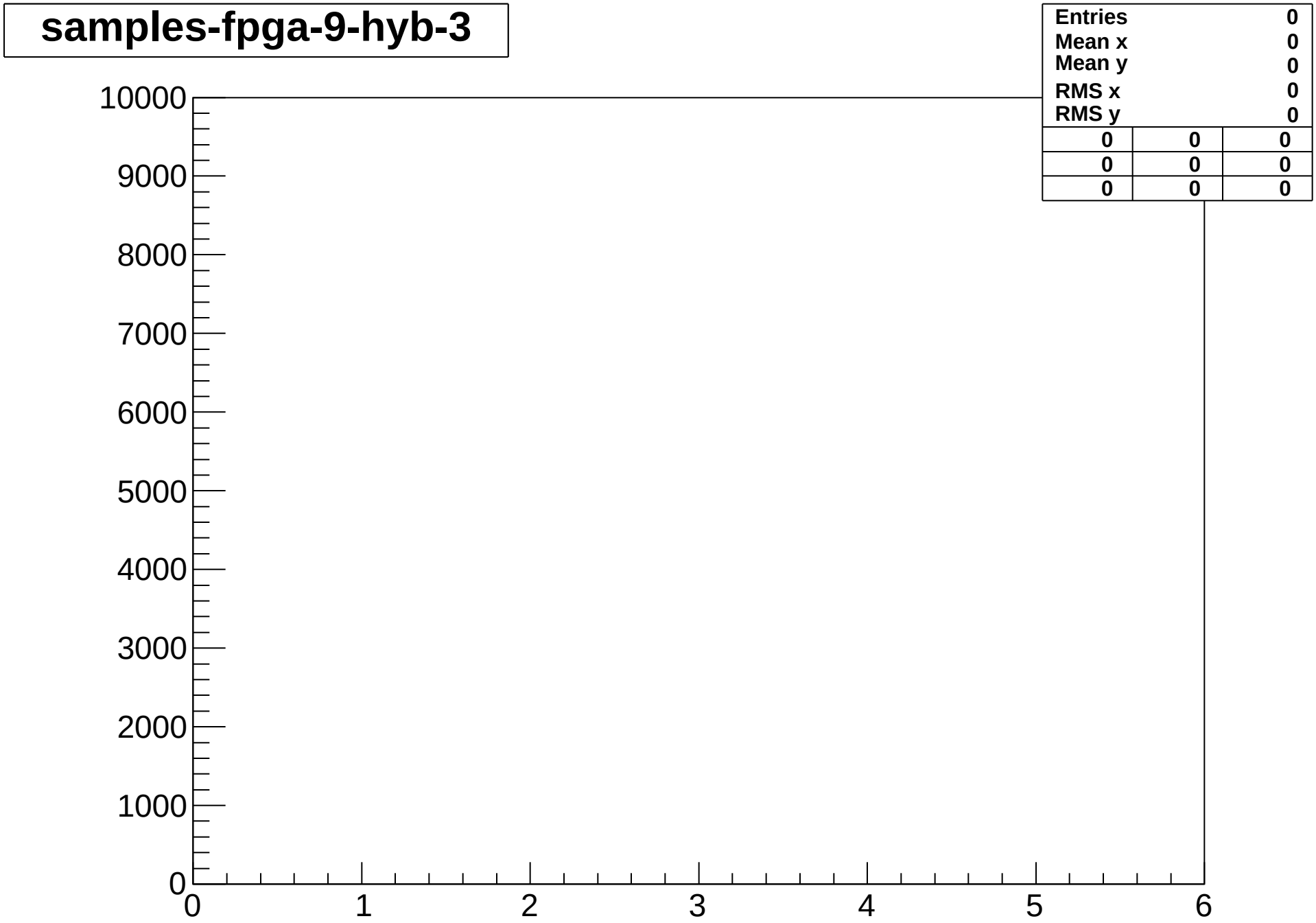
samples-delay-8-fpga-9-hyb-2




samples-fpga-9-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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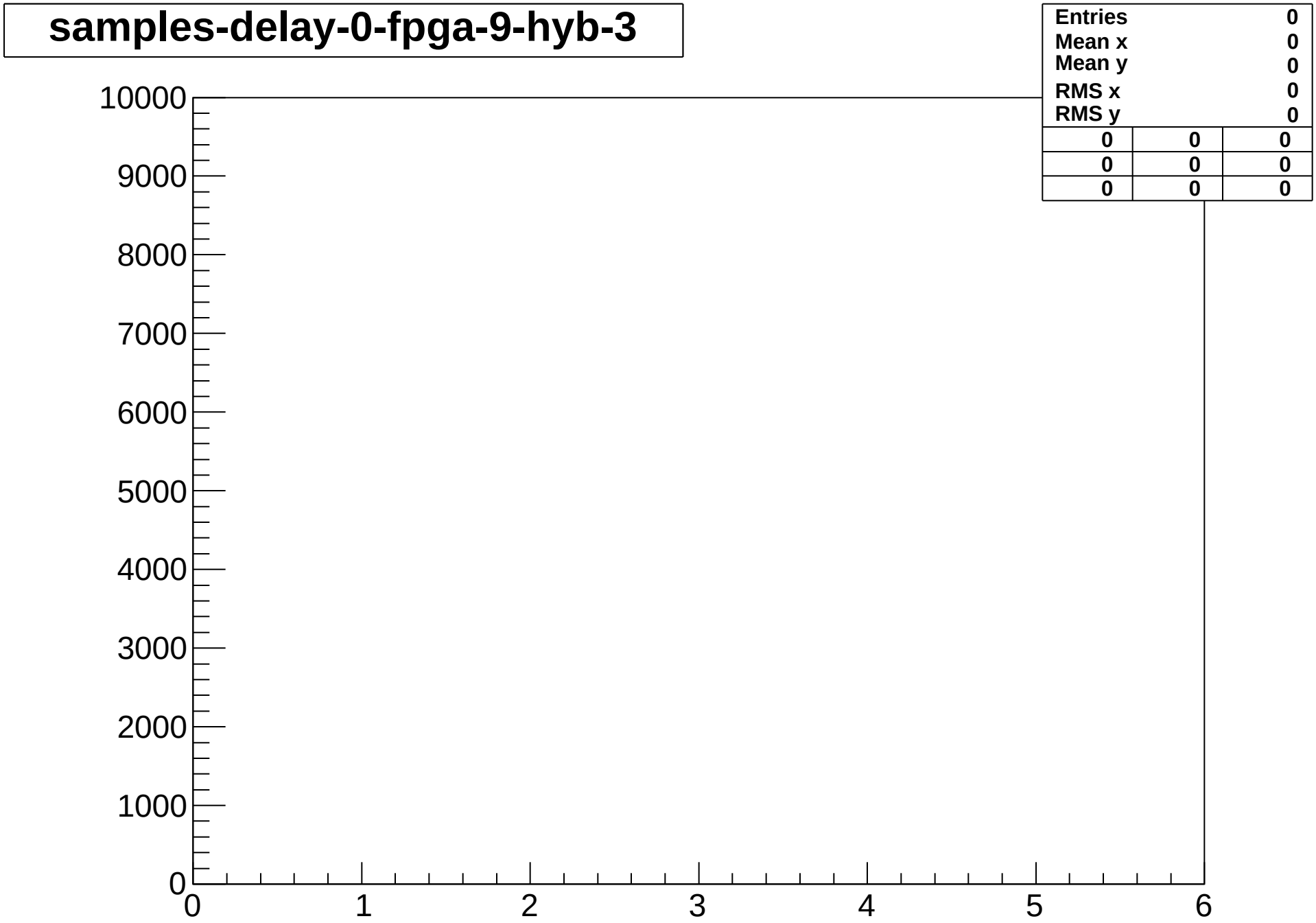
samples-delay-0-fpga-9-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
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1000
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0
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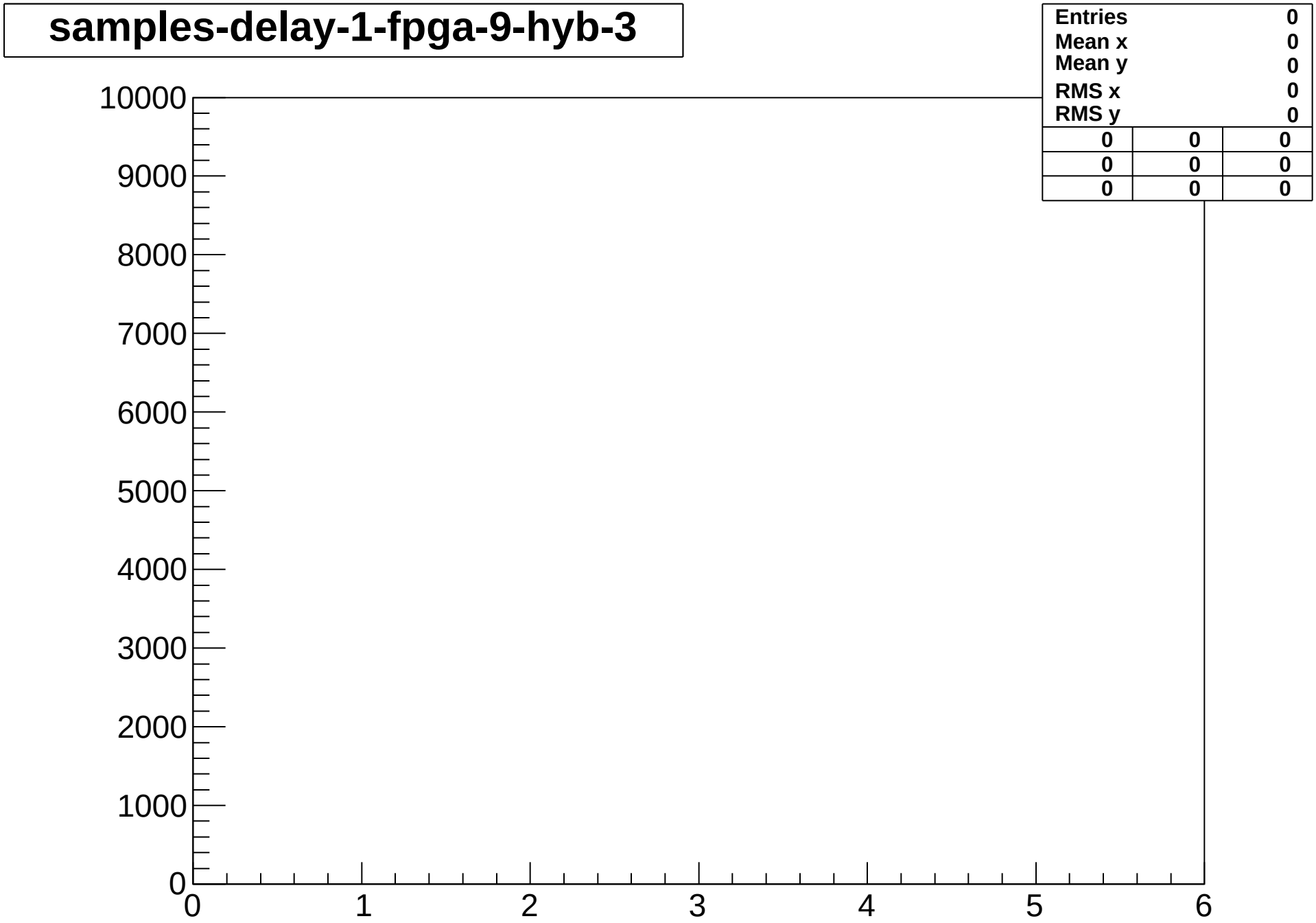
samples-delay-1-fpga-9-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
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6000
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4000
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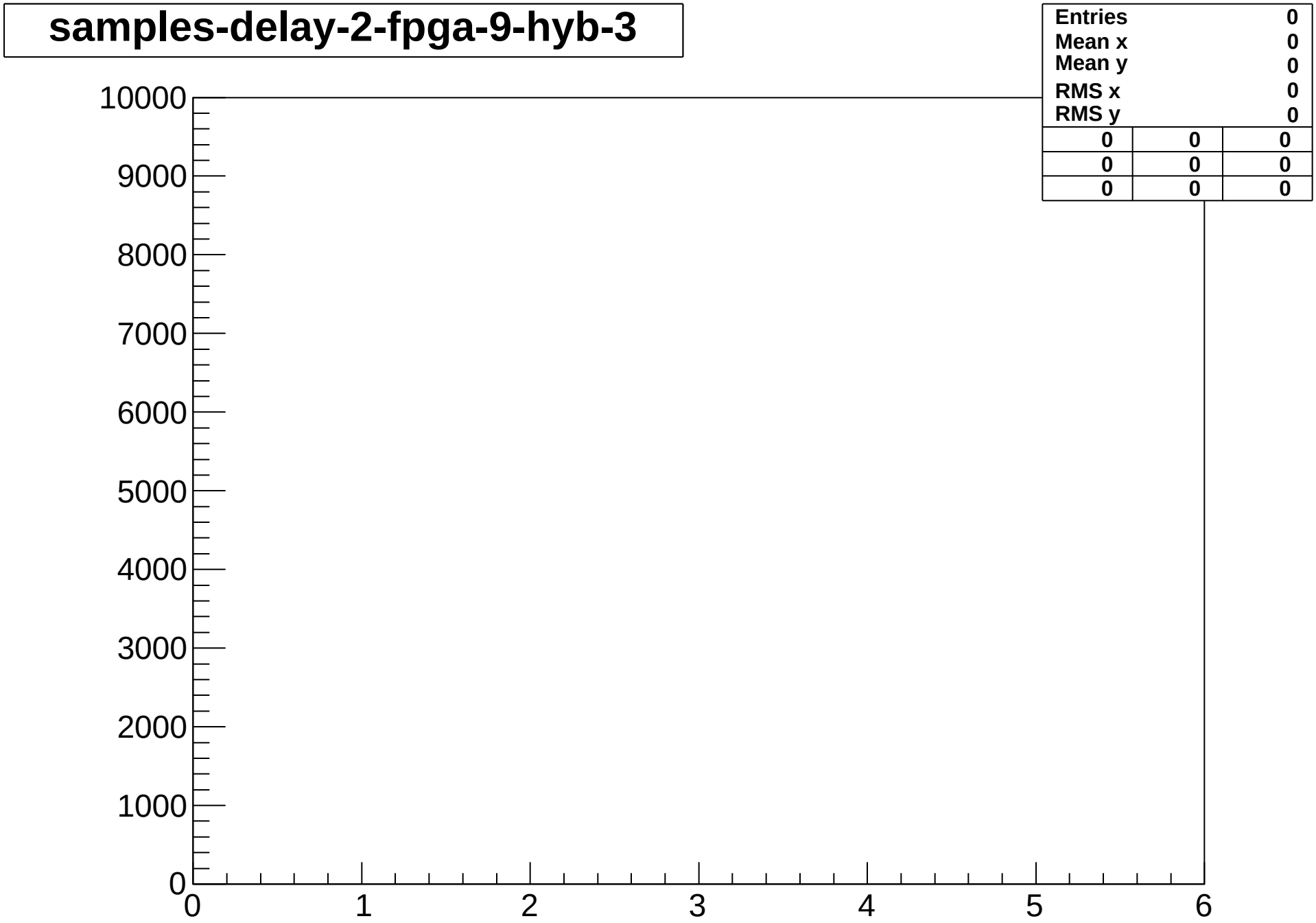
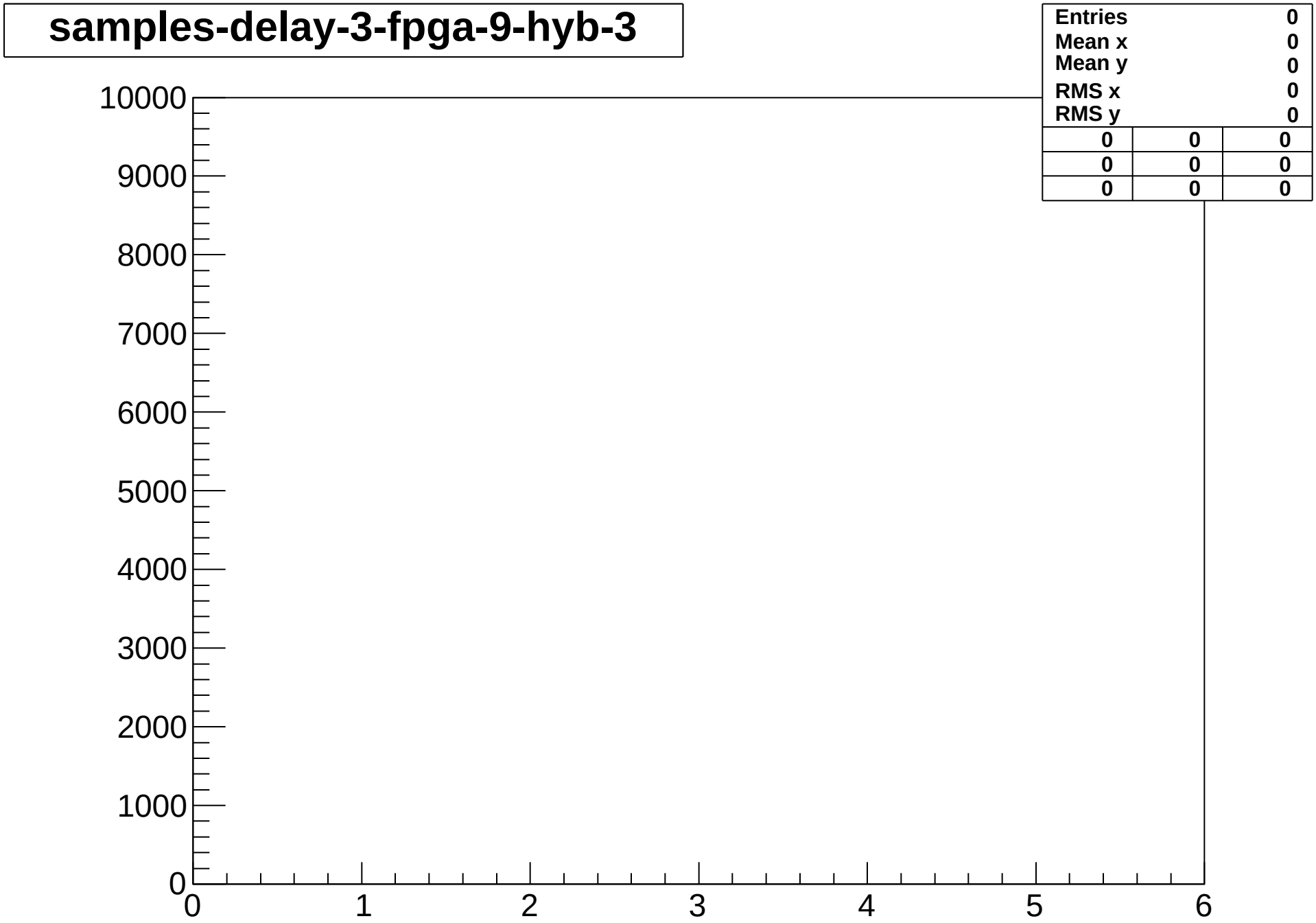
samples-delay-2-fpga-9-hyb-3




samples-delay-3-fpga-9-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
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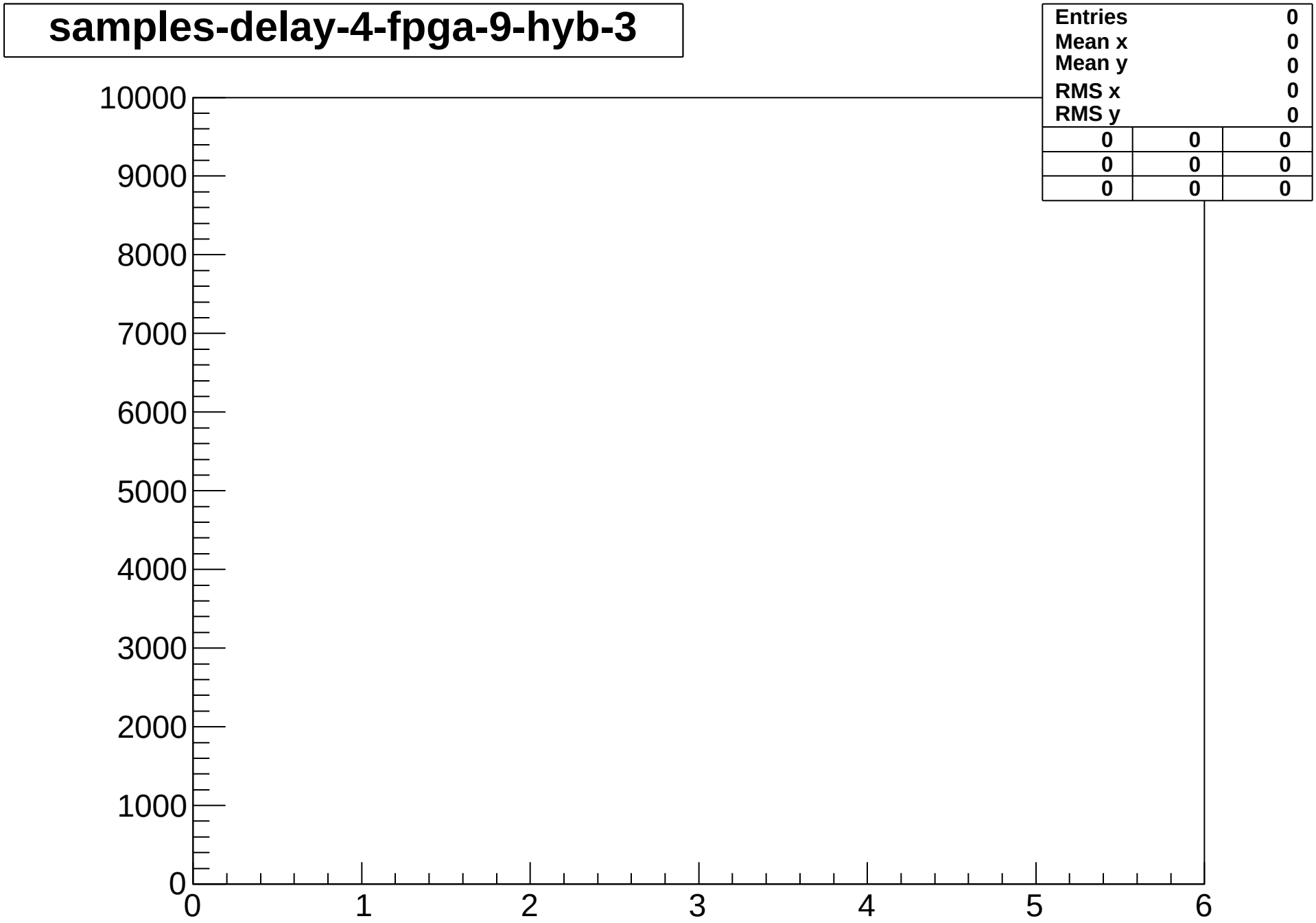
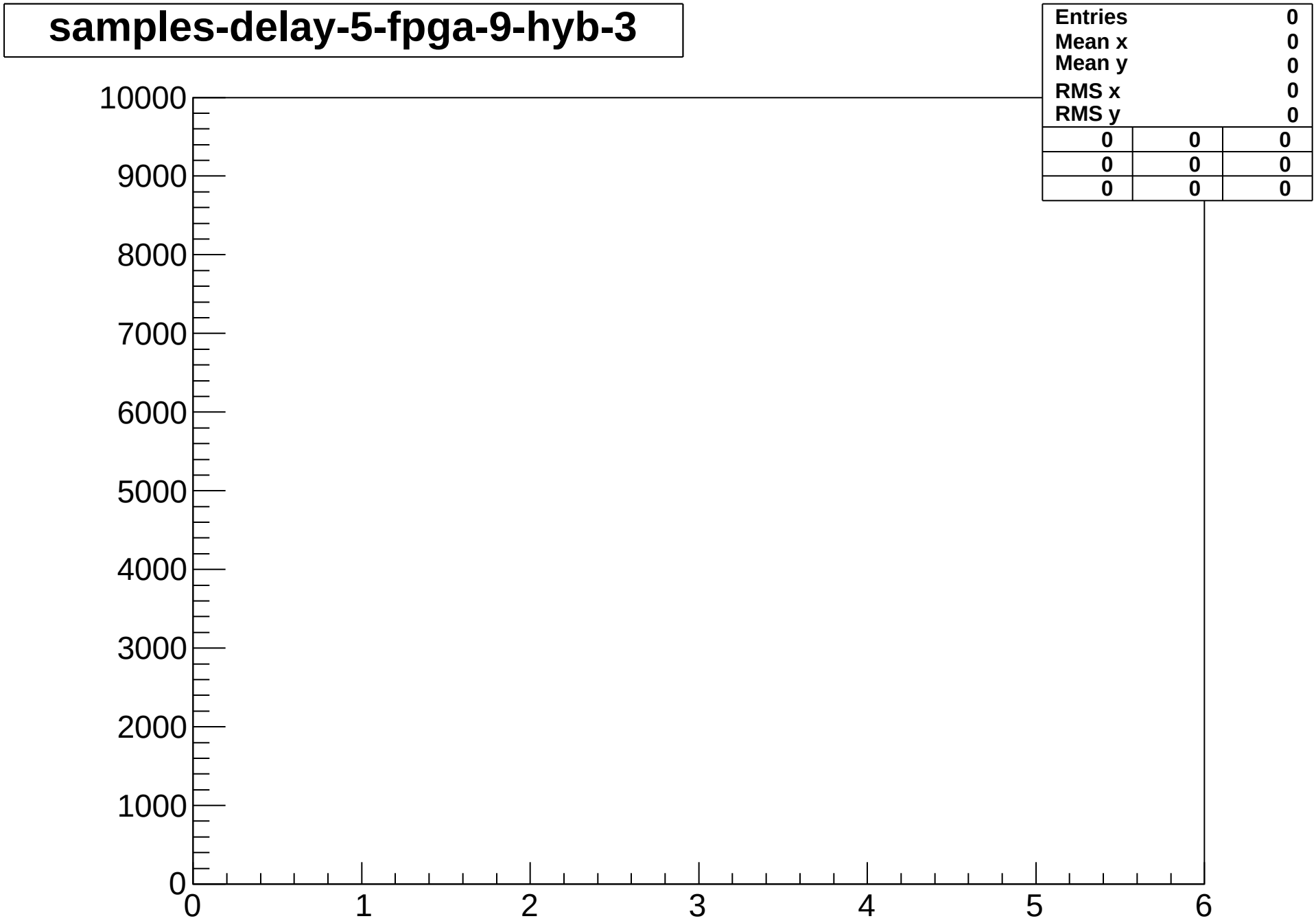
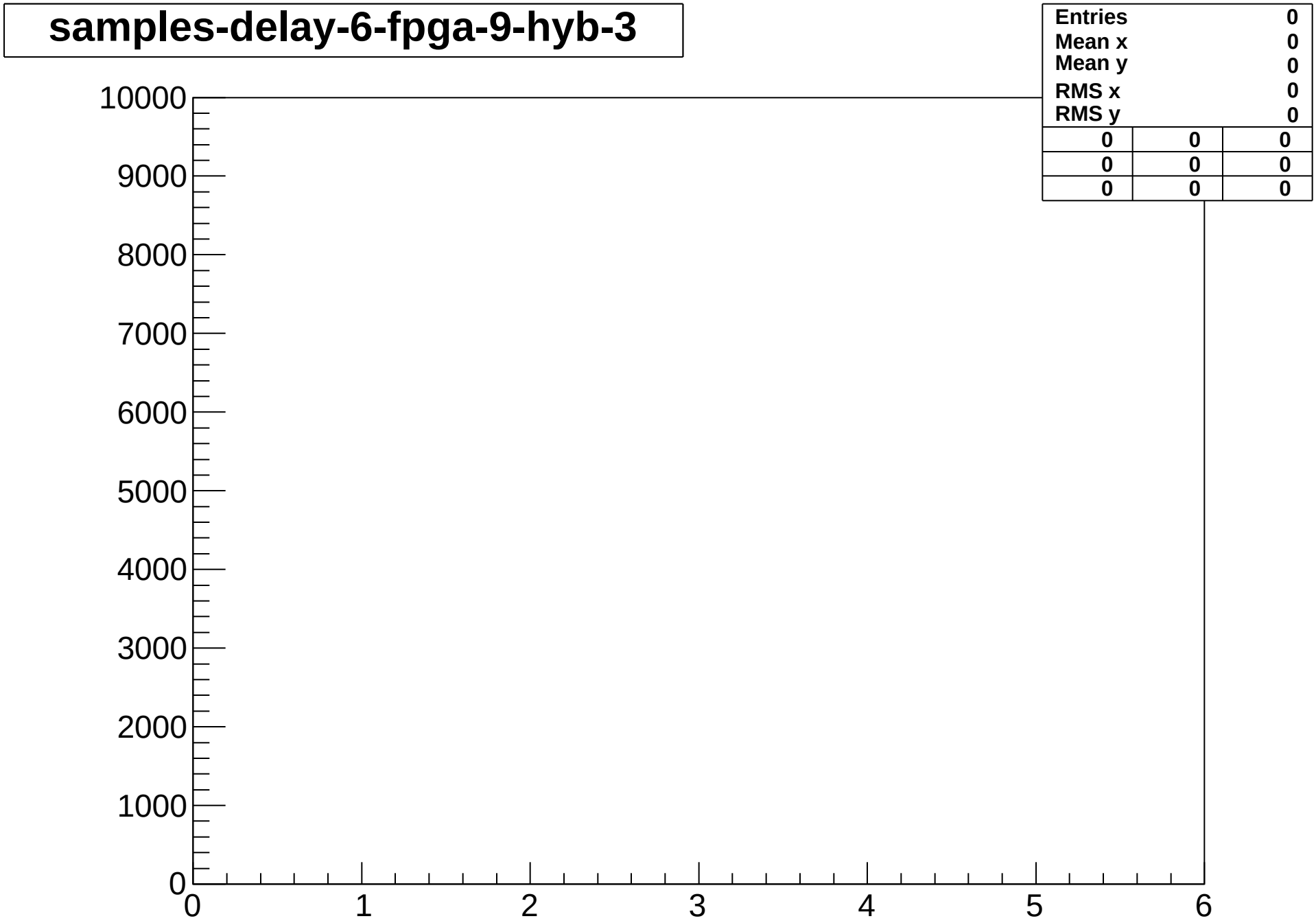
samples-delay-4-fpga-9-hyb-3

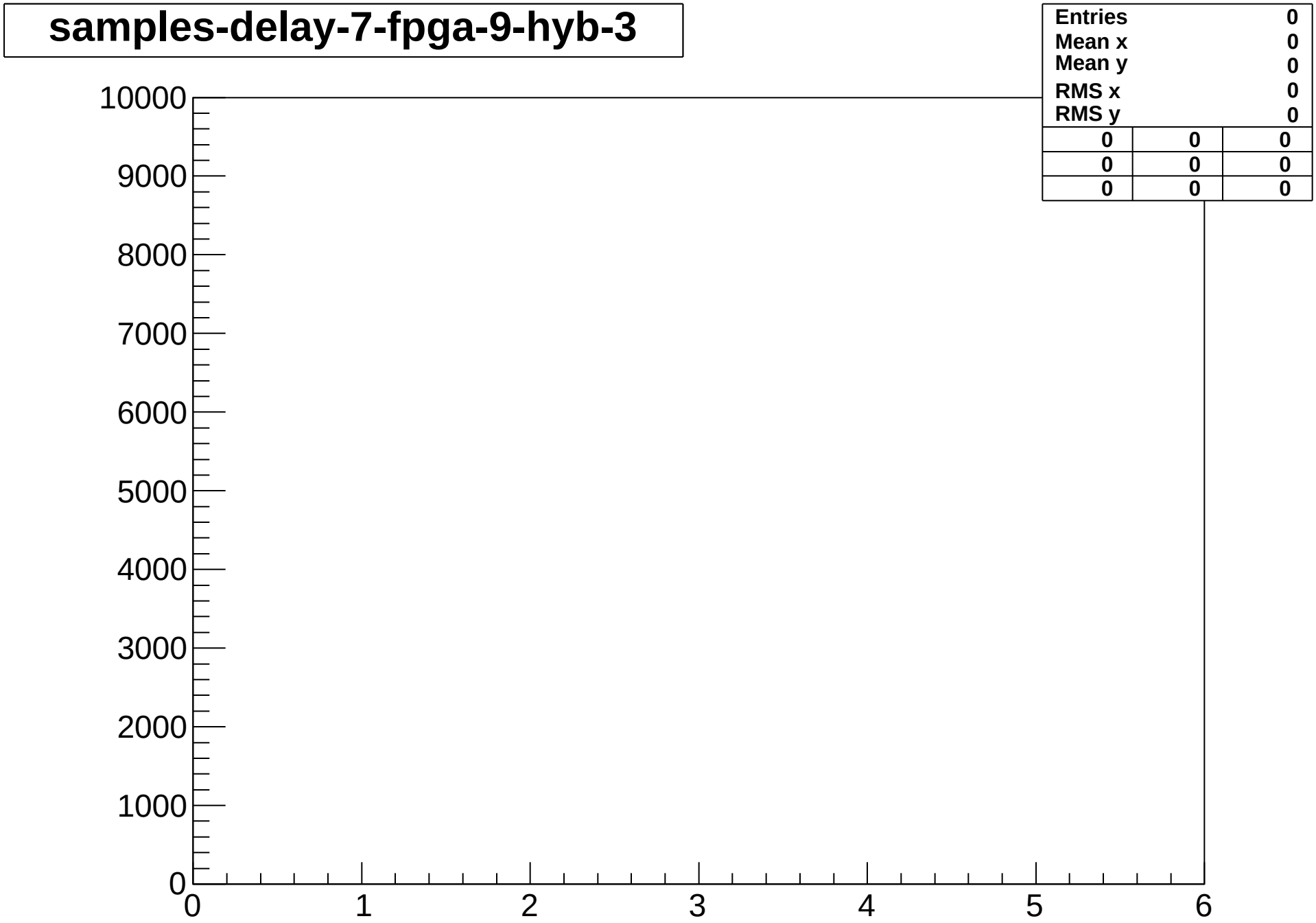


samples-delay-5-fpga-9-hyb-3



samples-delay-6-fpga-9-hyb-3




samples-delay-7-fpga-9-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
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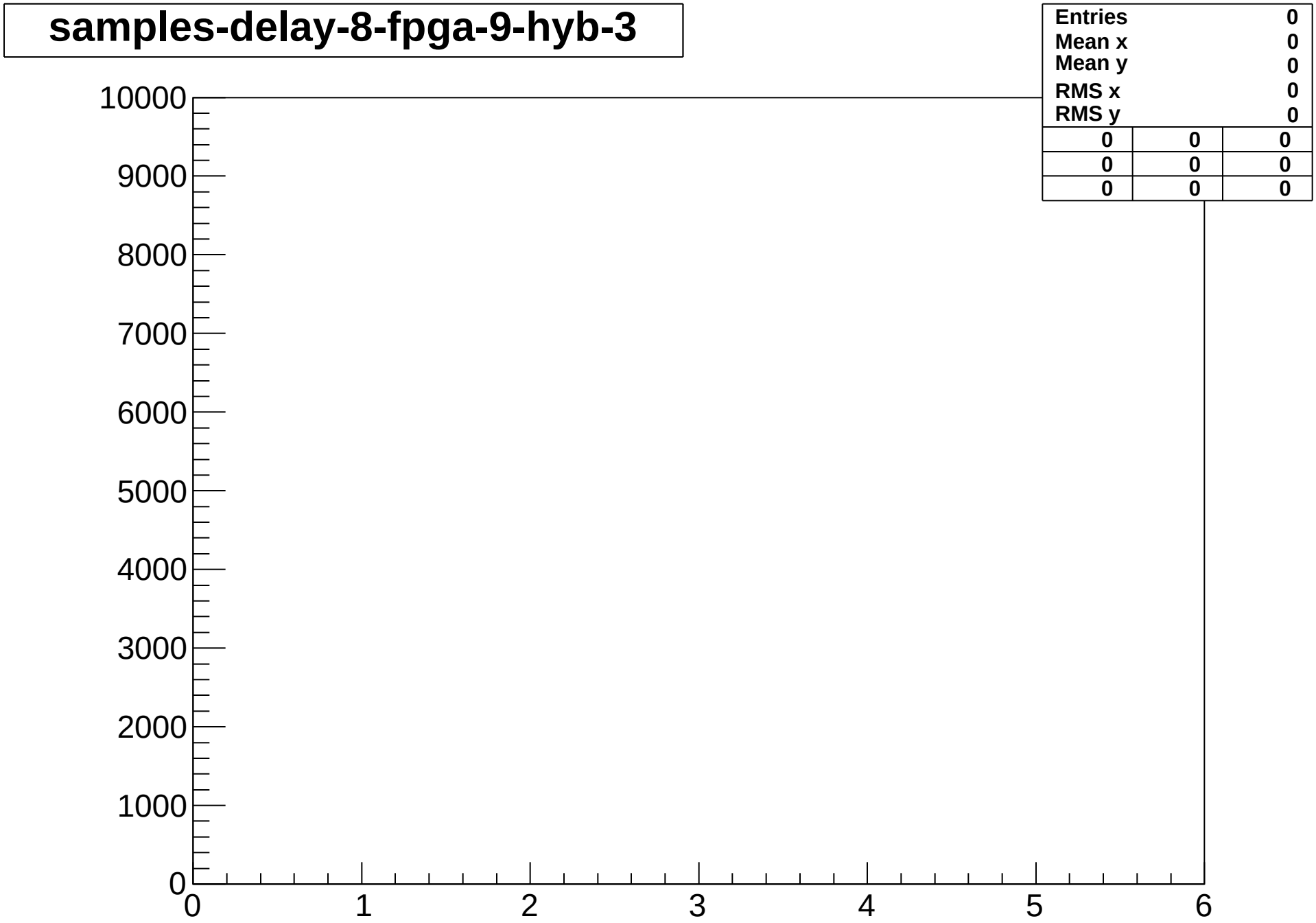
samples-delay-8-fpga-9-hyb-3
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
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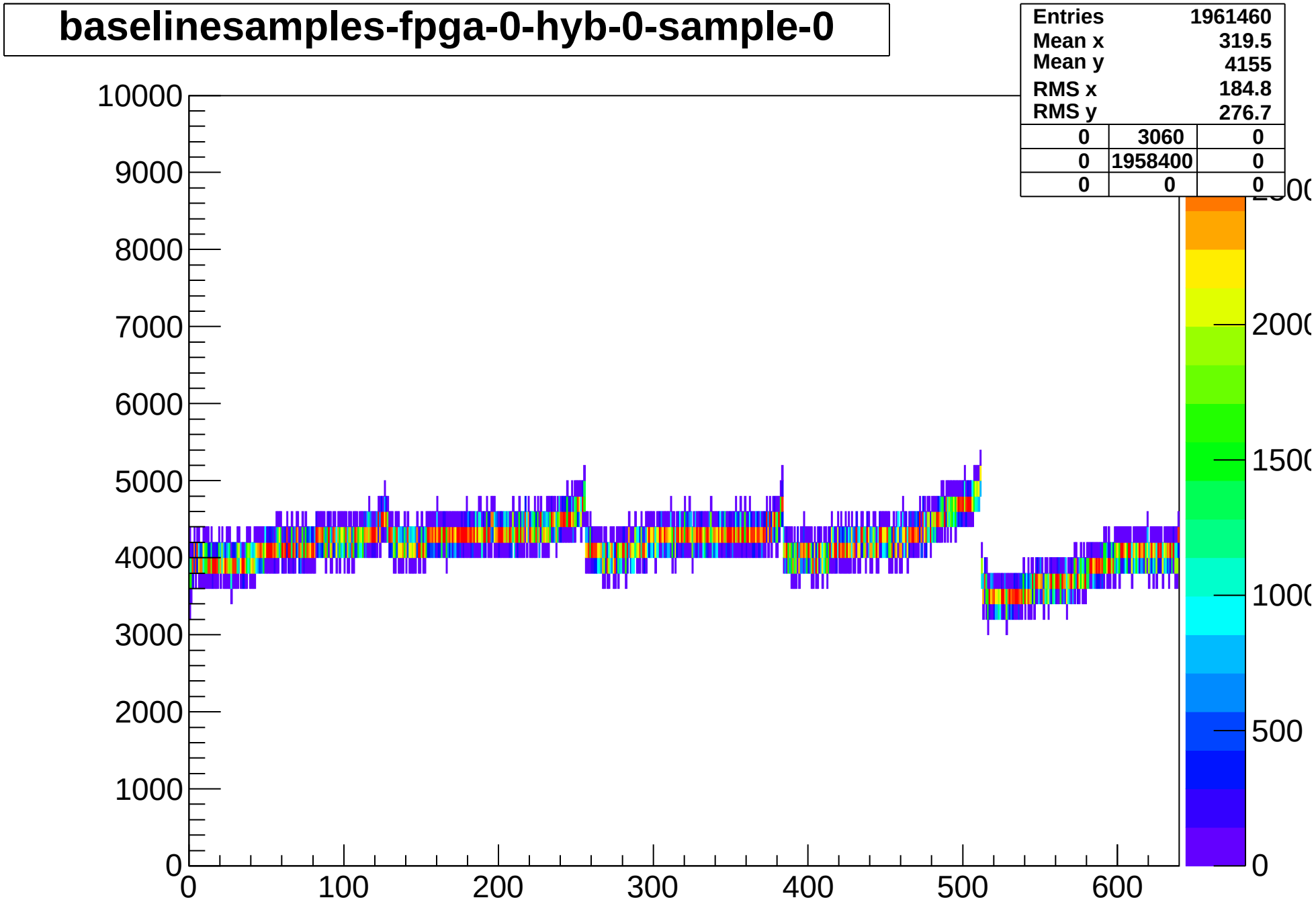
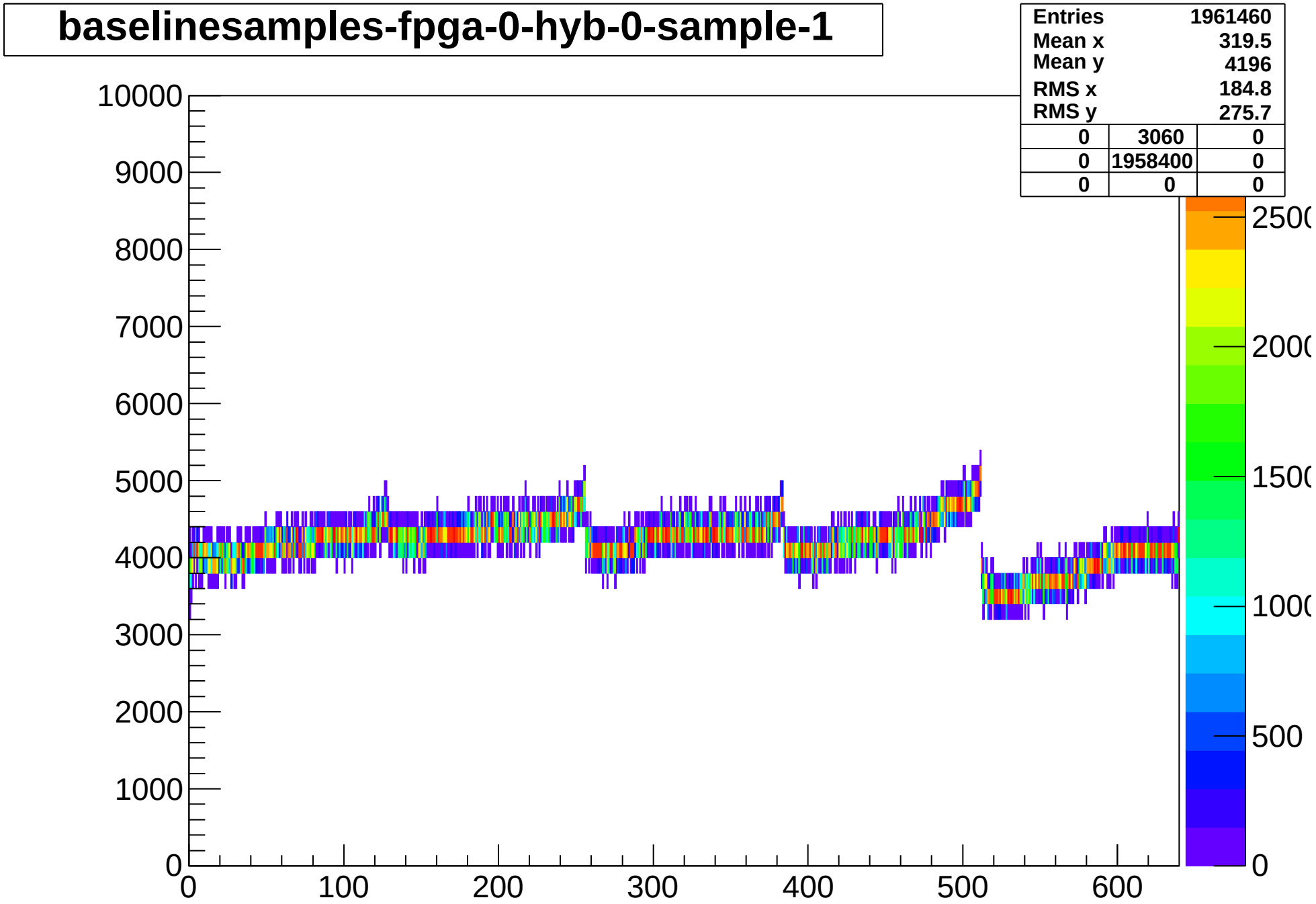
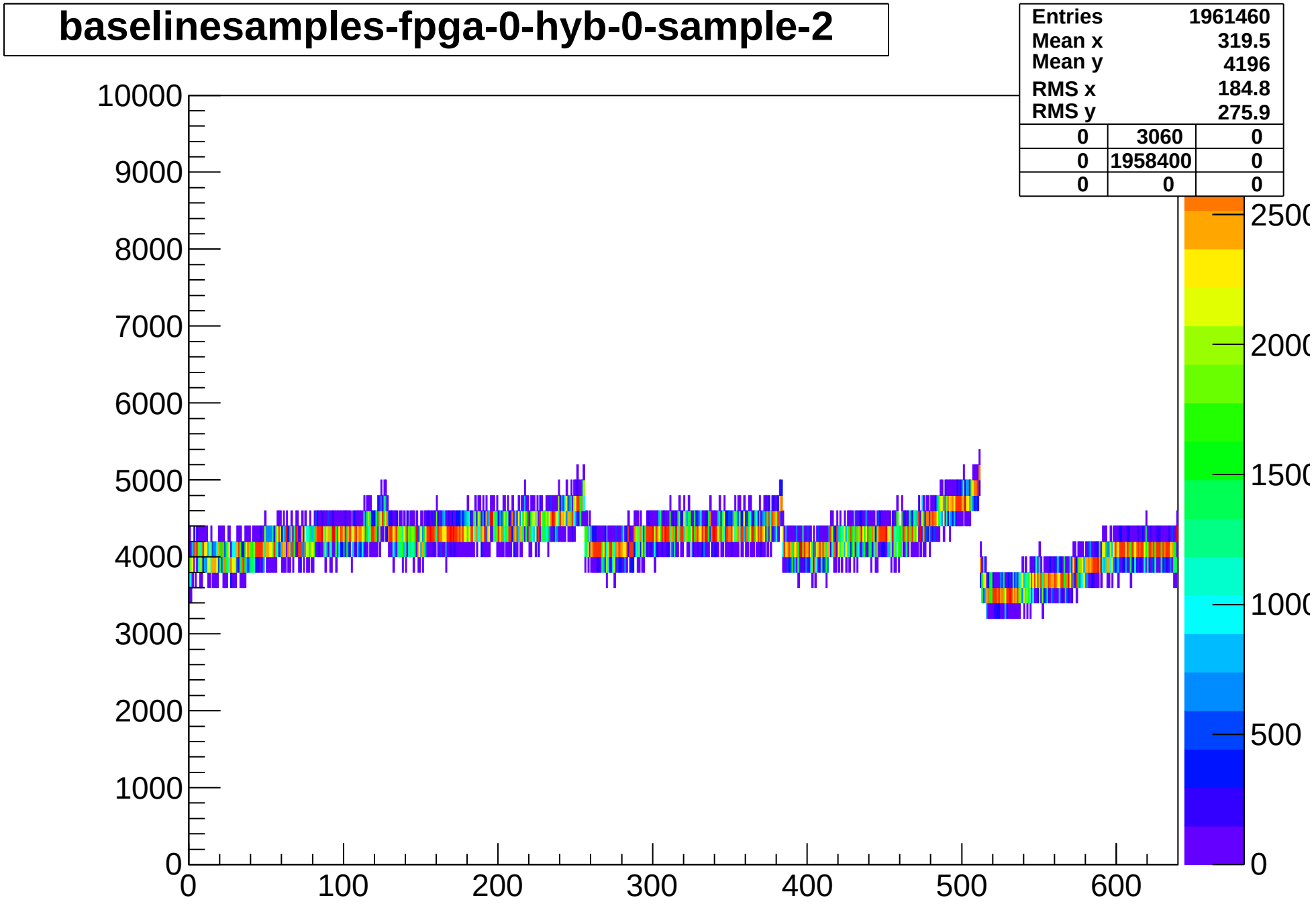
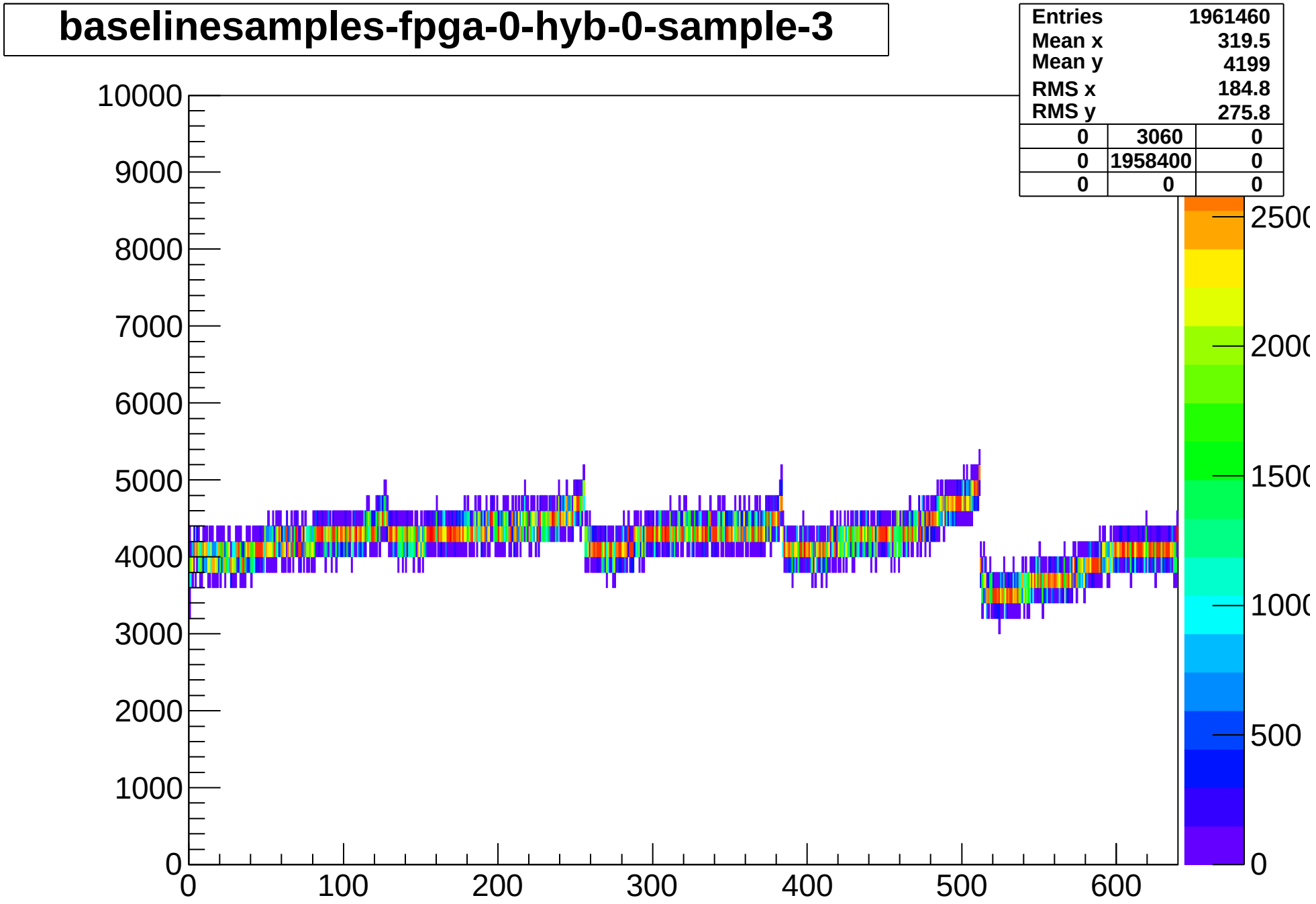
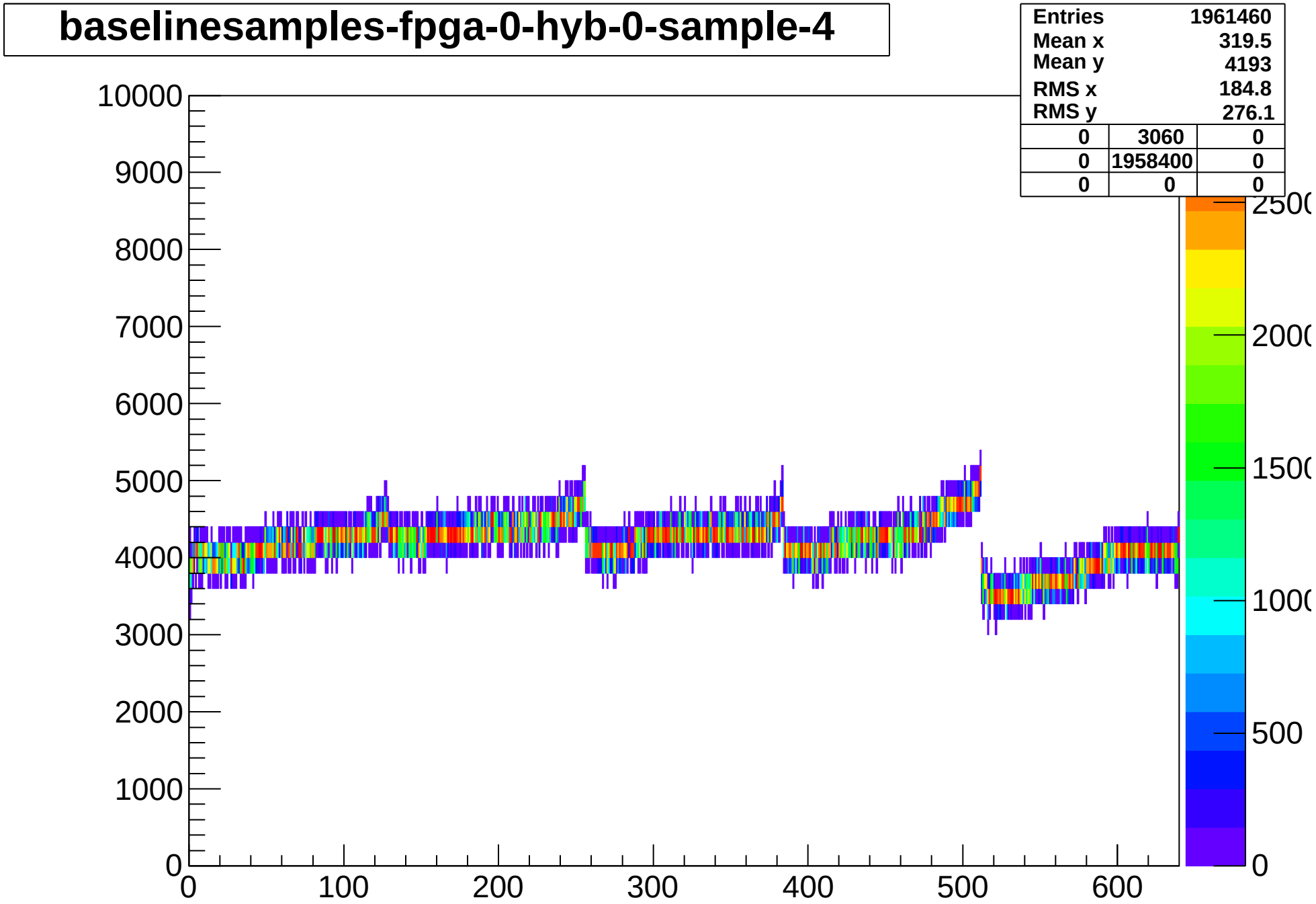
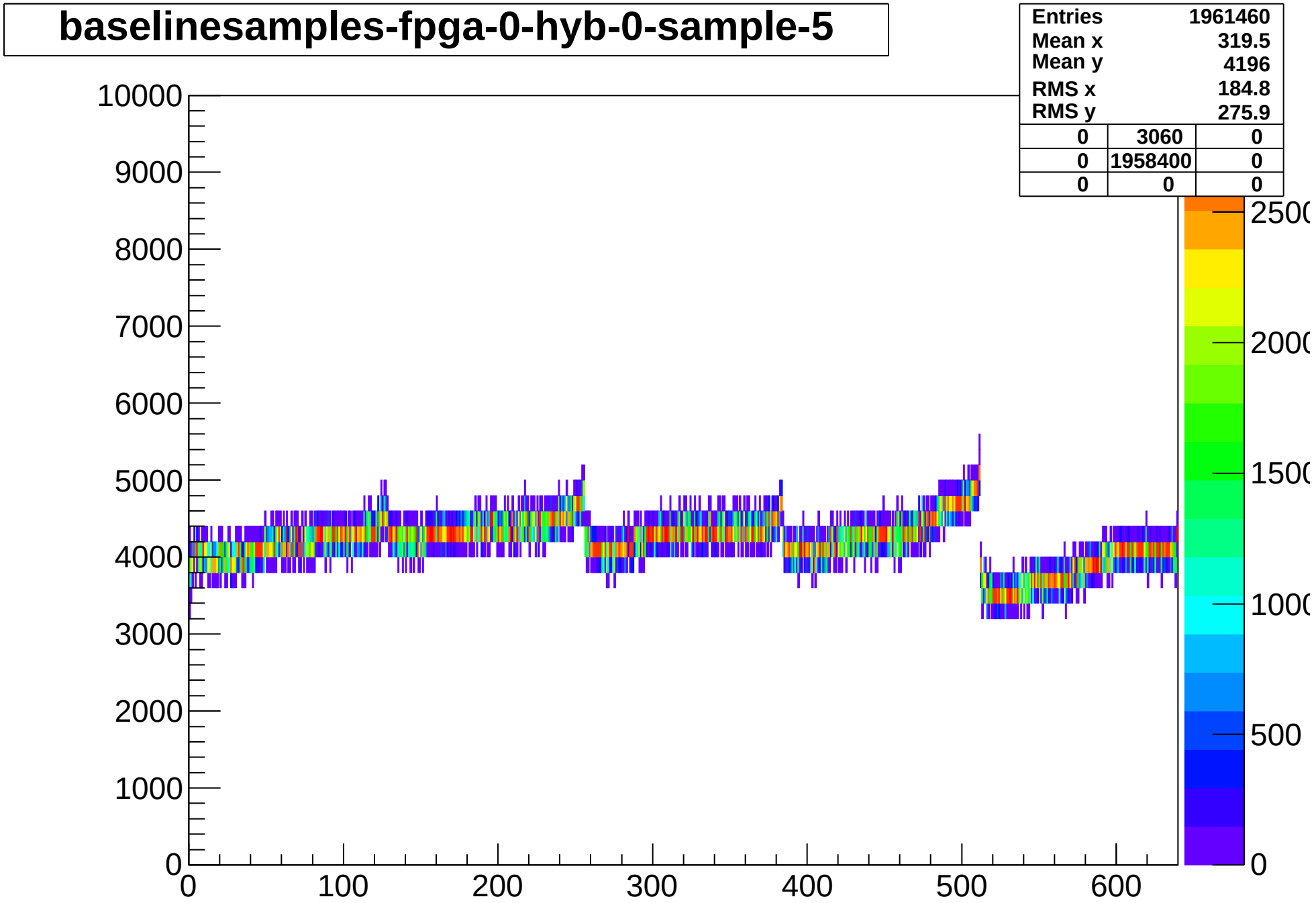

baselinesamples-fpga-0-hyb-0-sample-0
Entries 1961460
Mean x 319.5
Mean y 4155
RMS x 184.8
RMS y 276.7
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

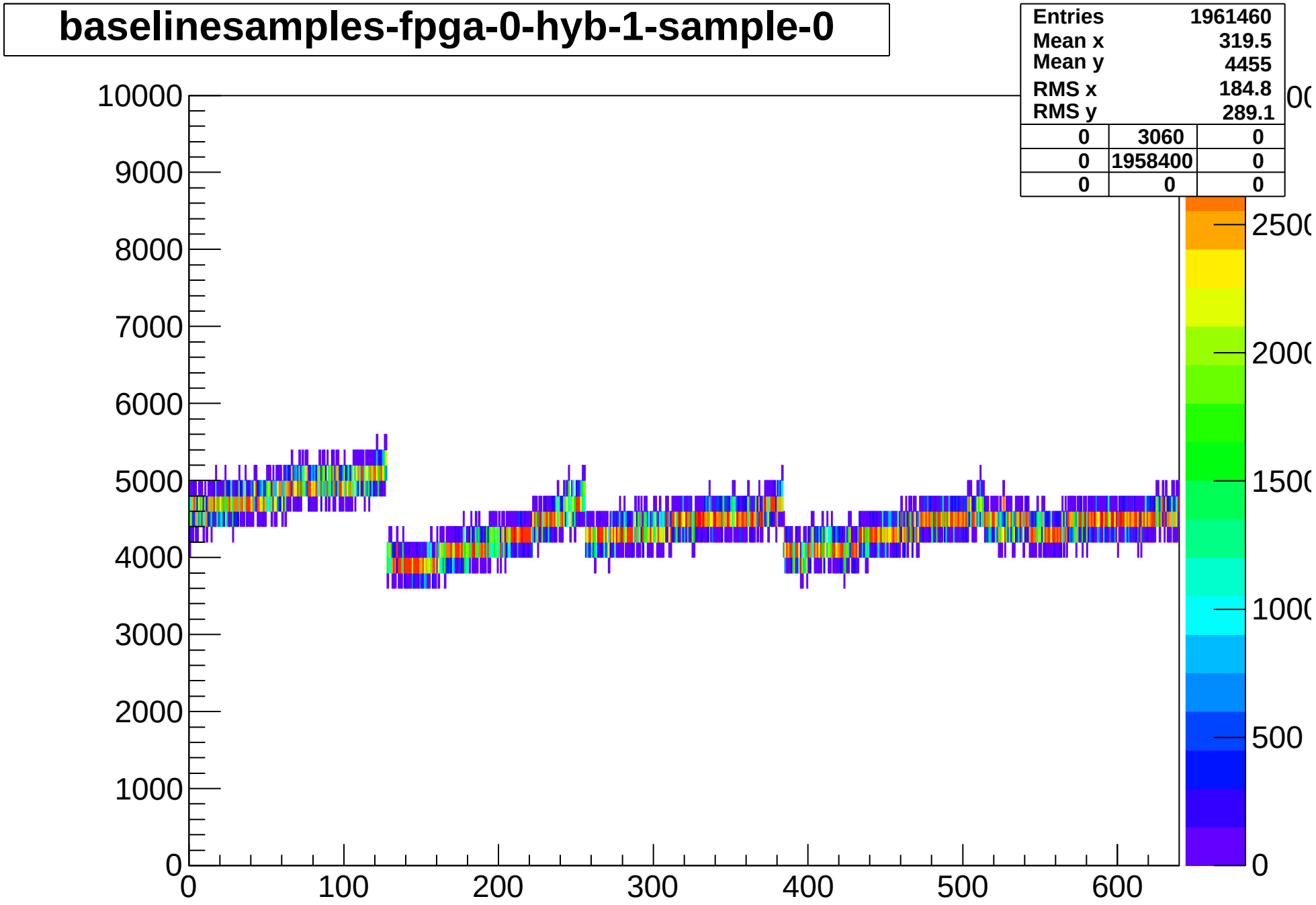

baselinesamples-fpga-0-hyb-0-sample-1
Entries 1961460
Mean x 319.5
Mean y 4196
RMS x 184.8
RMS y 275.7
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

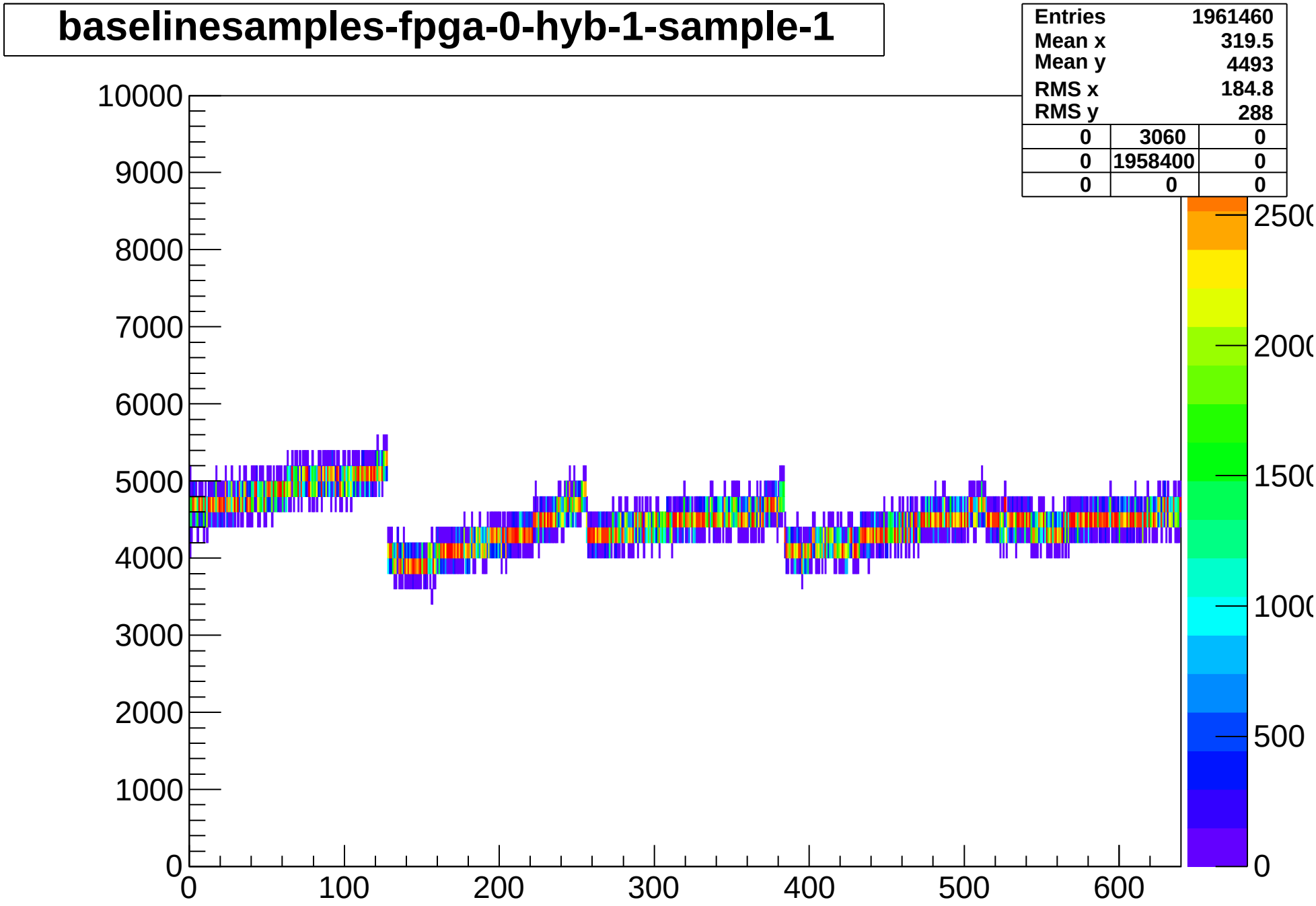

baselinesamples-fpga-0-hyb-0-sample-2
Entries 1961460
Mean x 319.5
Mean y 4196
RMS x 184.8
RMS y 275.9
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

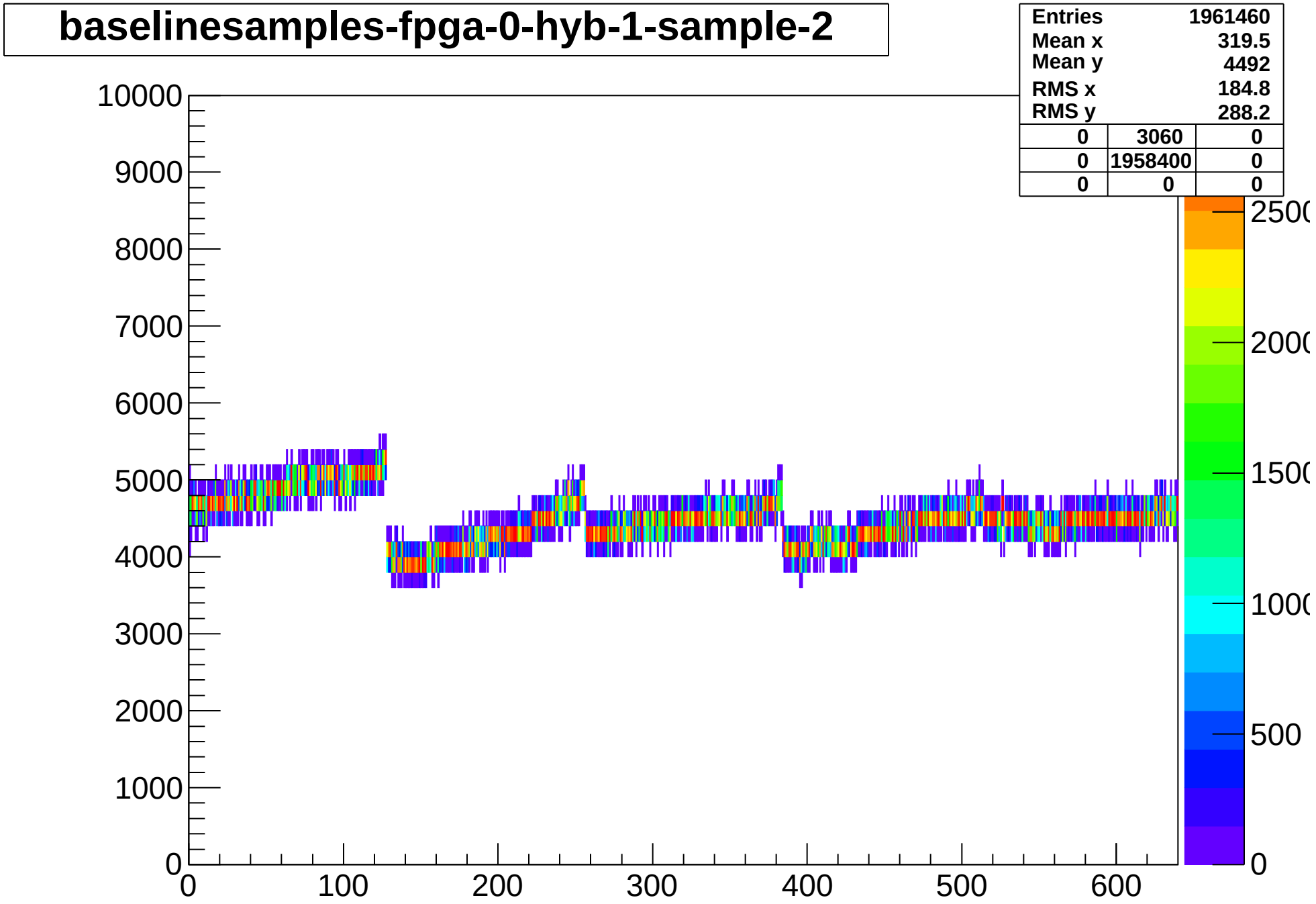

baselinesamples-fpga-0-hyb-0-sample-3
Entries 1961460
Mean x 319.5
Mean y 4199
RMS x 184.8
RMS y 275.8
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

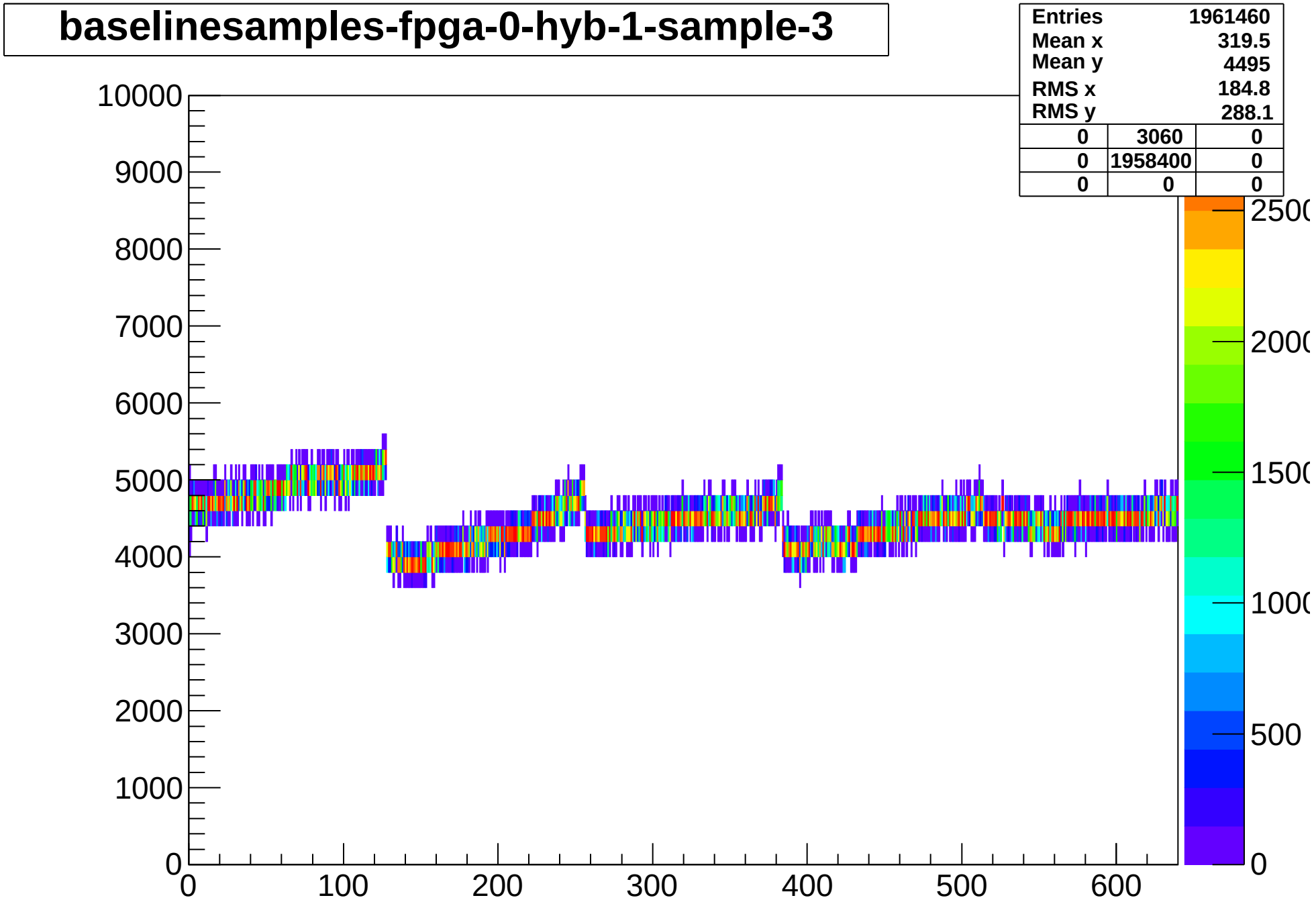

baselinesamples-fpga-0-hyb-0-sample-4
Entries 1961460
Mean x 319.5
Mean y 4193
RMS x 184.8
RMS y 276.1
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

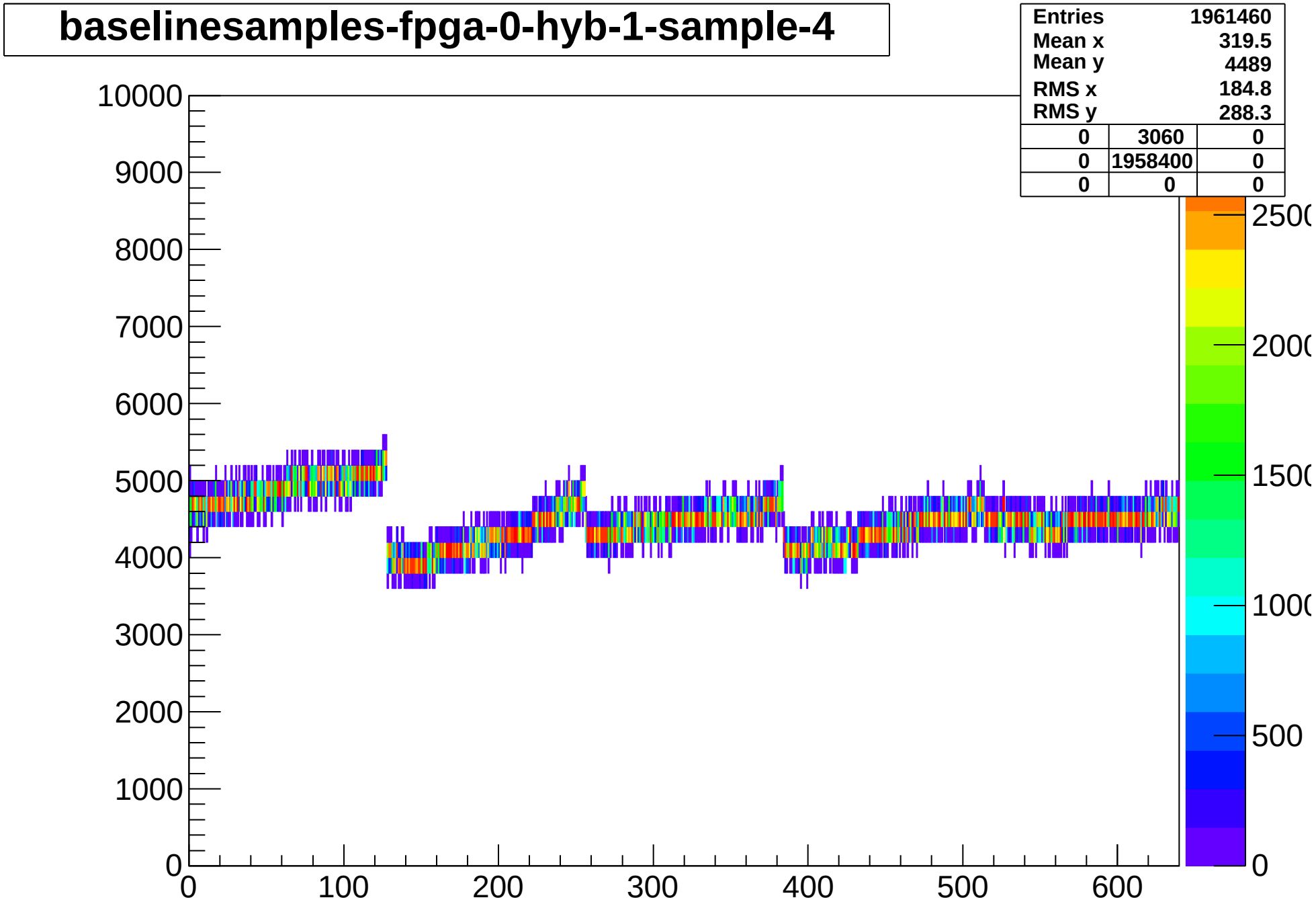

baselinesamples-fpga-0-hyb-0-sample-5
Entries 1961460
Mean x 319.5
Mean y 4196
RMS x 184.8
RMS y 275.9
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

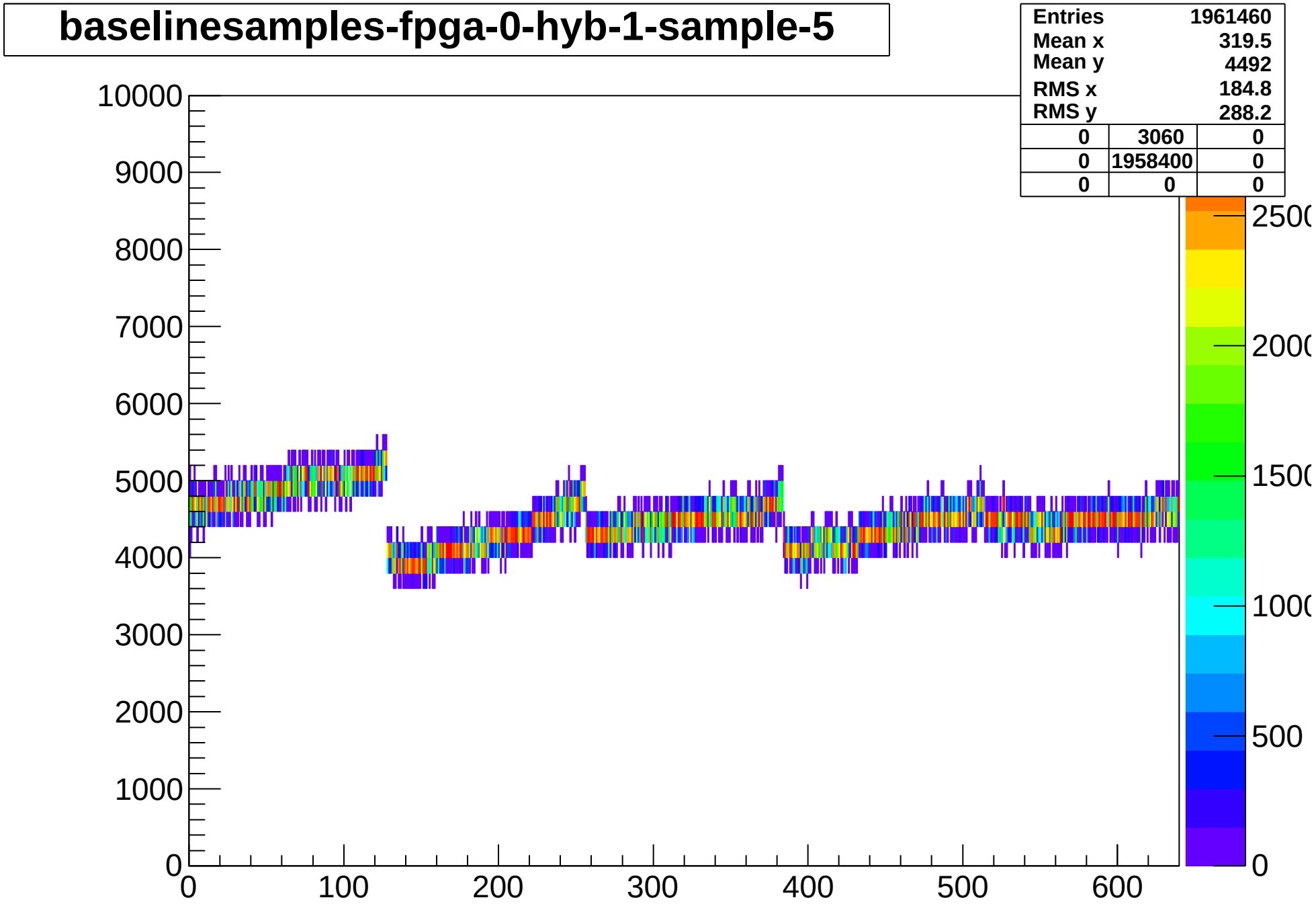

baselinesamples-fpga-0-hyb-1-sample-0
Entries 1961460
Mean x 319.5
Mean y 4455
RMS x 184.8
RMS y 289.1
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

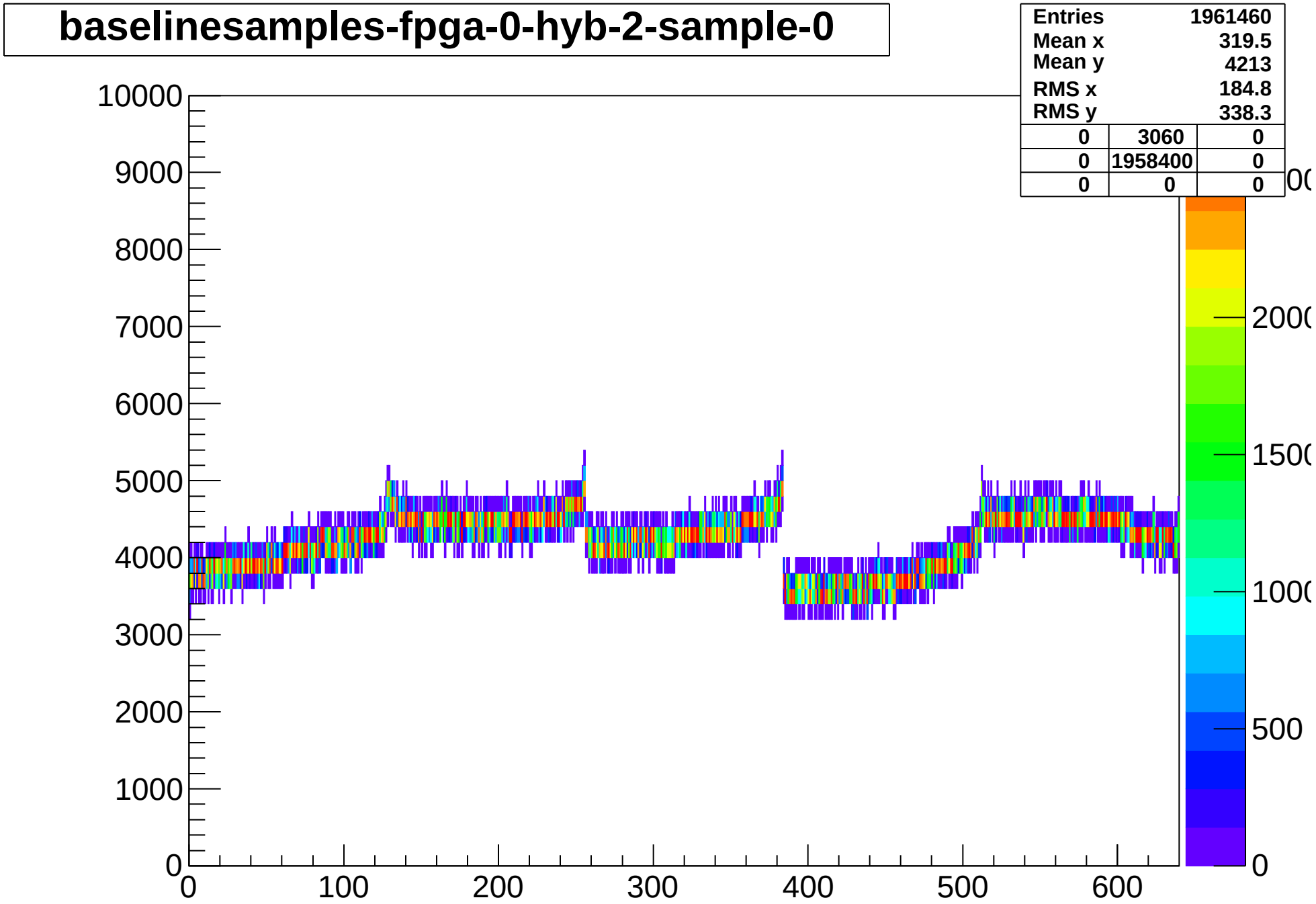

baselinesamples-fpga-0-hyb-1-sample-1
Entries 1961460
Mean x 319.5
Mean y 4493
RMS x 184.8
RMS y 288
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

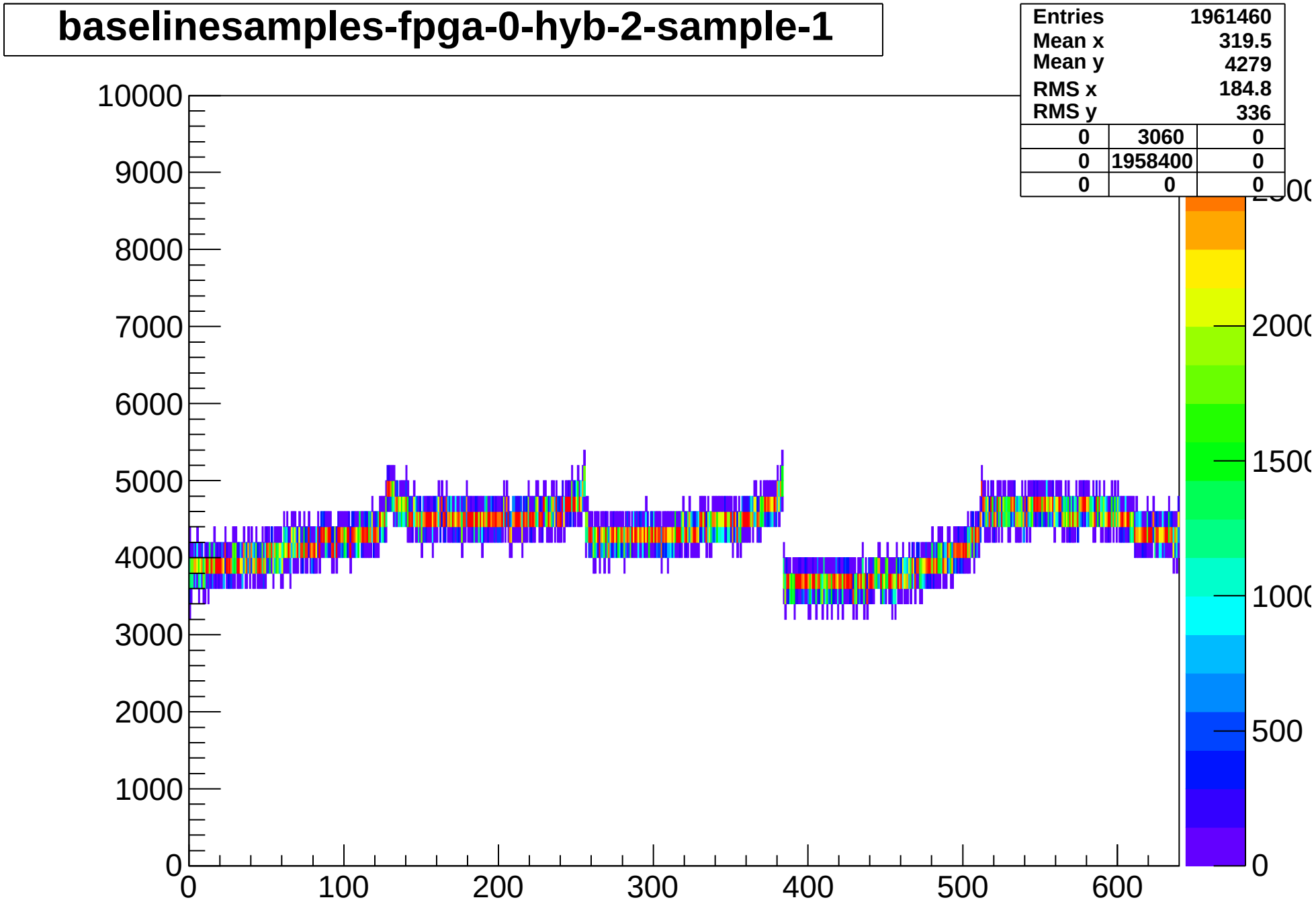

baselinesamples-fpga-0-hyb-1-sample-2
Entries 1961460
Mean x 319.5
Mean y 4492
RMS x 184.8
RMS y 288.2
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

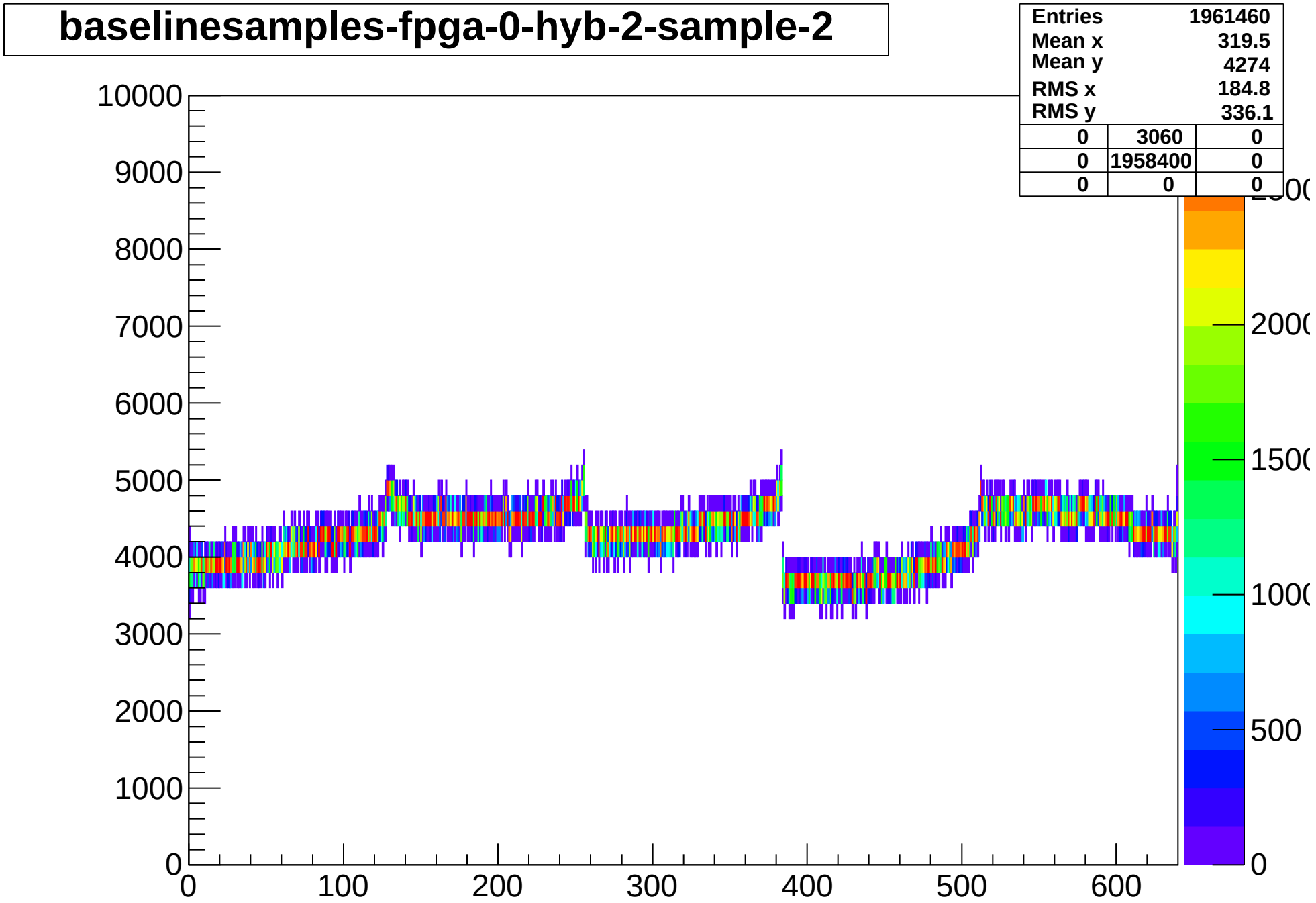

baselinesamples-fpga-0-hyb-1-sample-3
Entries 1961460
Mean x 319.5
Mean y 4495
RMS x 184.8
RMS y 288.1
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

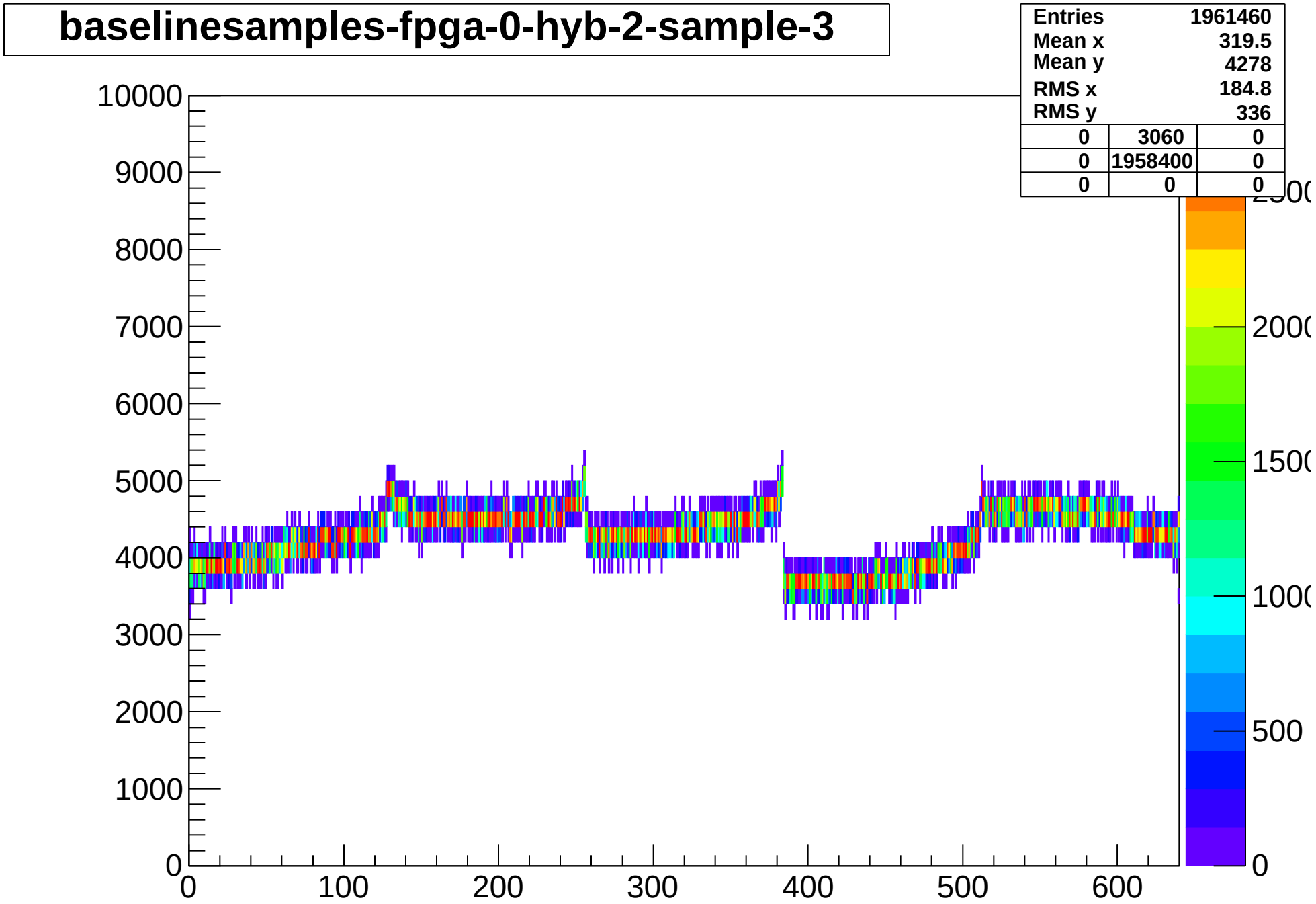

baselinesamples-fpga-0-hyb-1-sample-4
Entries 1961460
Mean x 319.5
Mean y 4489
RMS x 184.8
RMS y 288.3
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

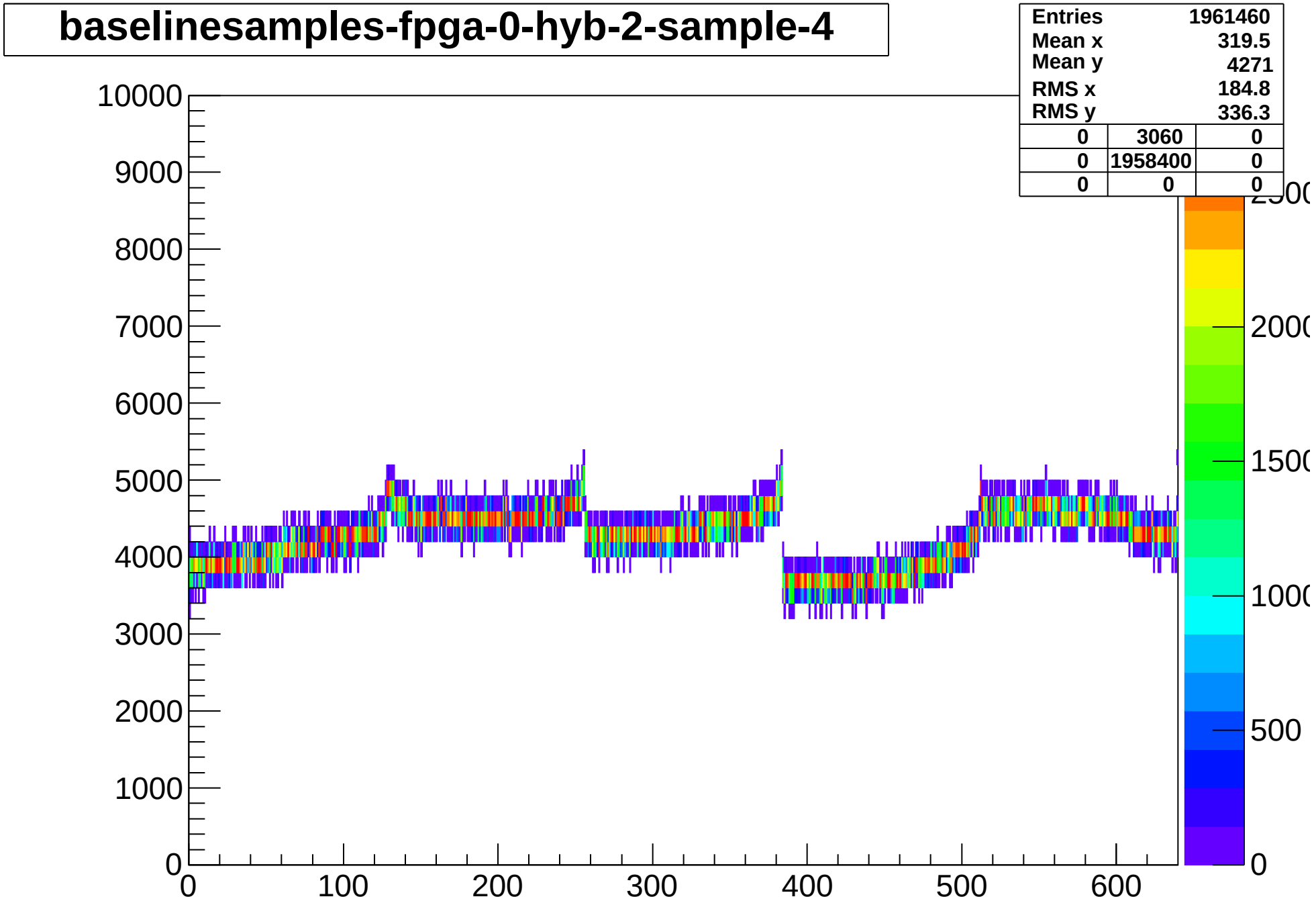

baselinesamples-fpga-0-hyb-1-sample-5
Entries 1961460
Mean x 319.5
Mean y 4492
RMS x 184.8
RMS y 288.2
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2500
2000
1500
1000
500
0

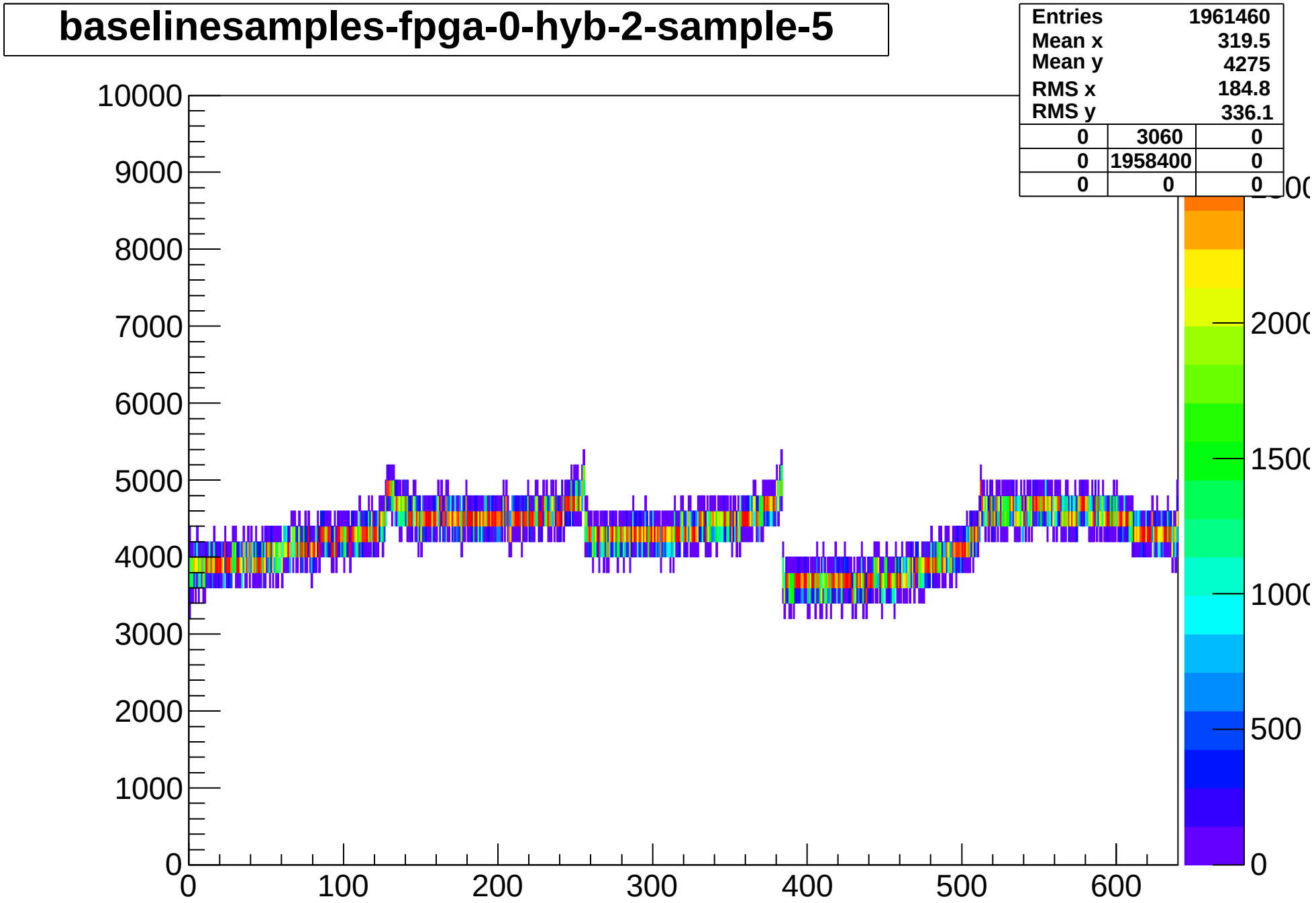

baselinesamples-fpga-0-hyb-2-sample-0
Entries 1961460
Mean x 319.5
Mean y 4213
RMS x 184.8
RMS y 338.3
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

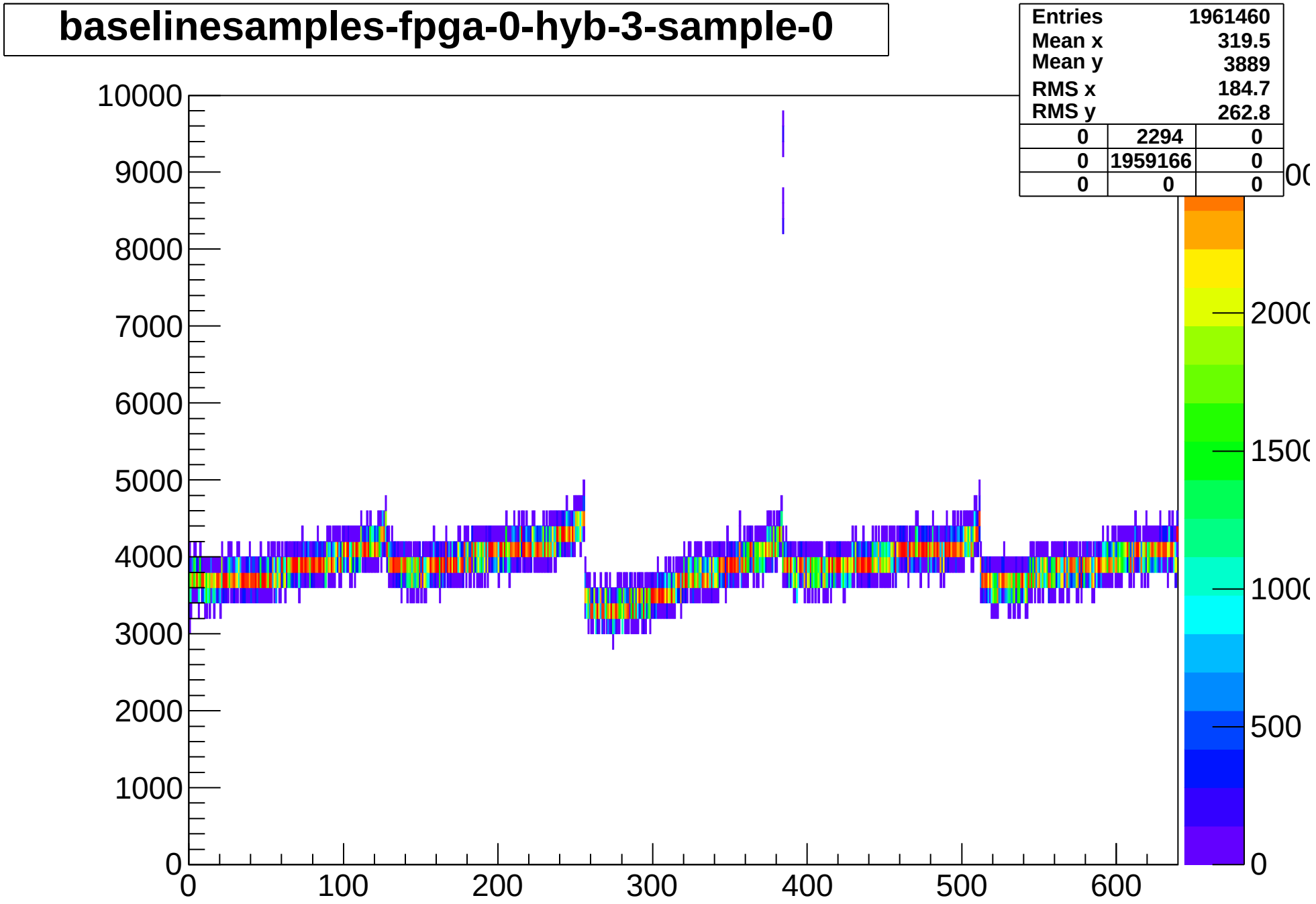

baselinesamples-fpga-0-hyb-2-sample-1
Entries 1961460
Mean x 319.5
Mean y 4279
RMS x 184.8
RMS y 336
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

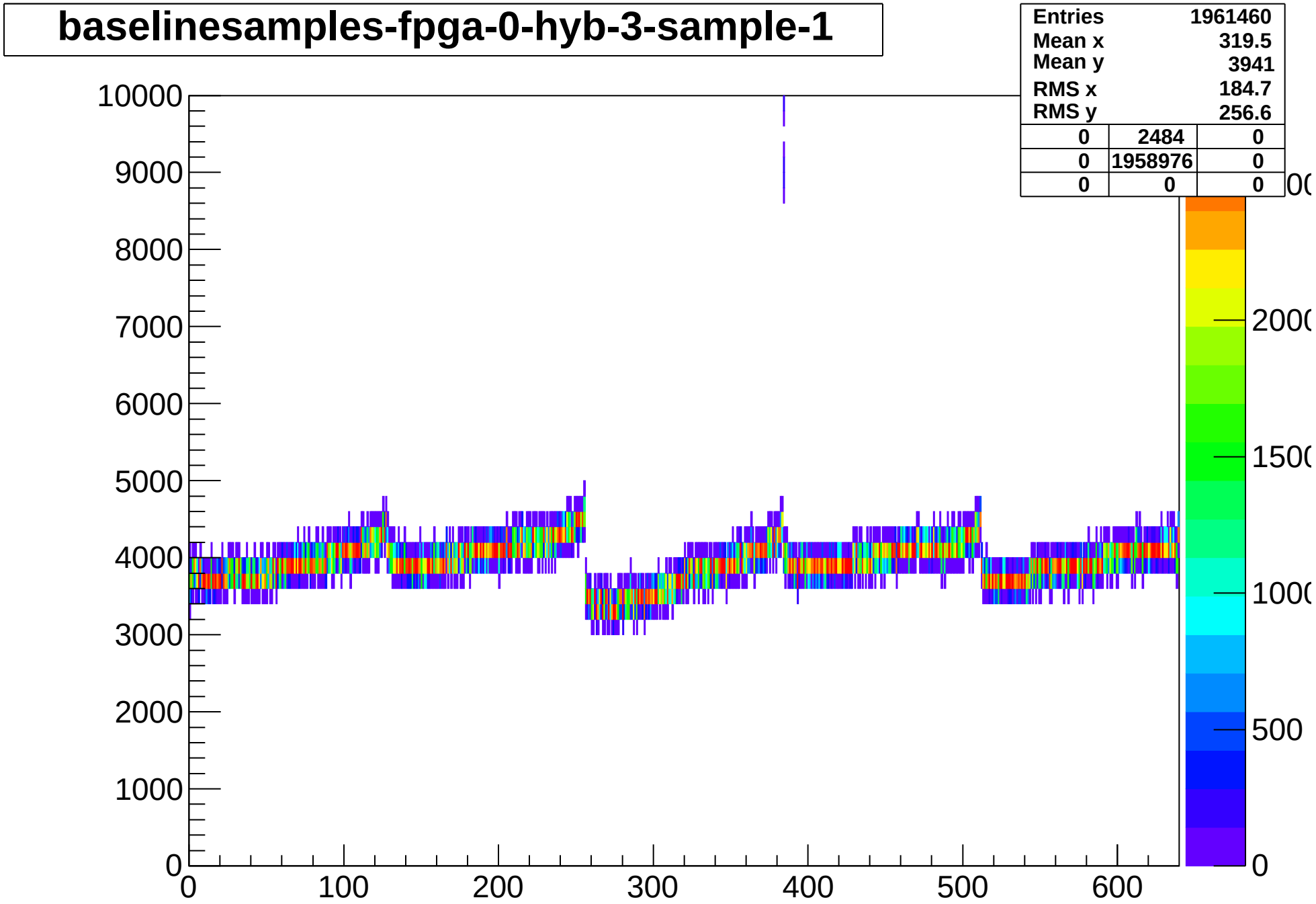

baselinesamples-fpga-0-hyb-2-sample-2
Entries 1961460
Mean x 319.5
Mean y 4274
RMS x 184.8
RMS y 336.1
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

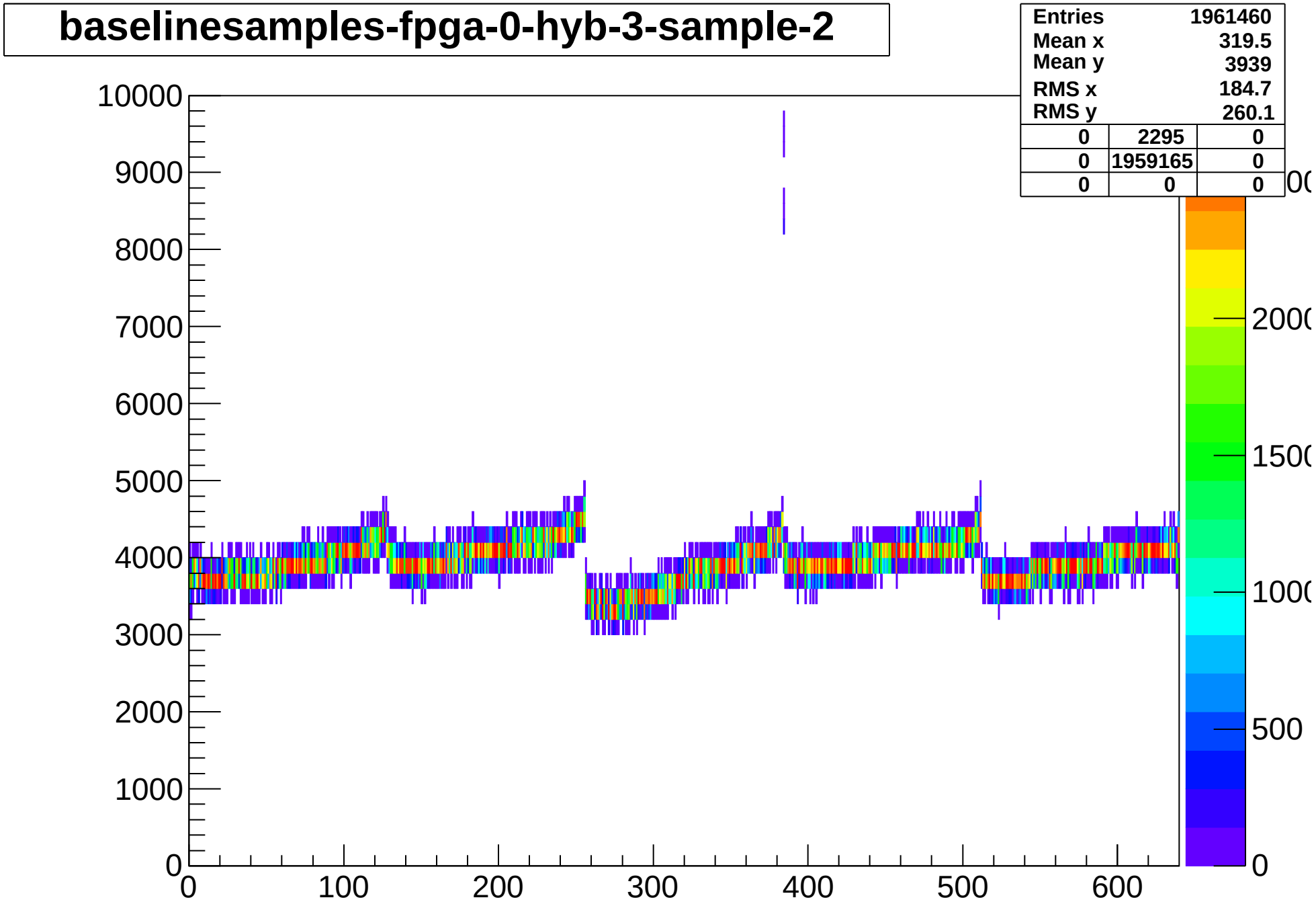

baselinesamples-fpga-0-hyb-2-sample-3
Entries 1961460
Mean x 319.5
Mean y 4278
RMS x 184.8
RMS y 336
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

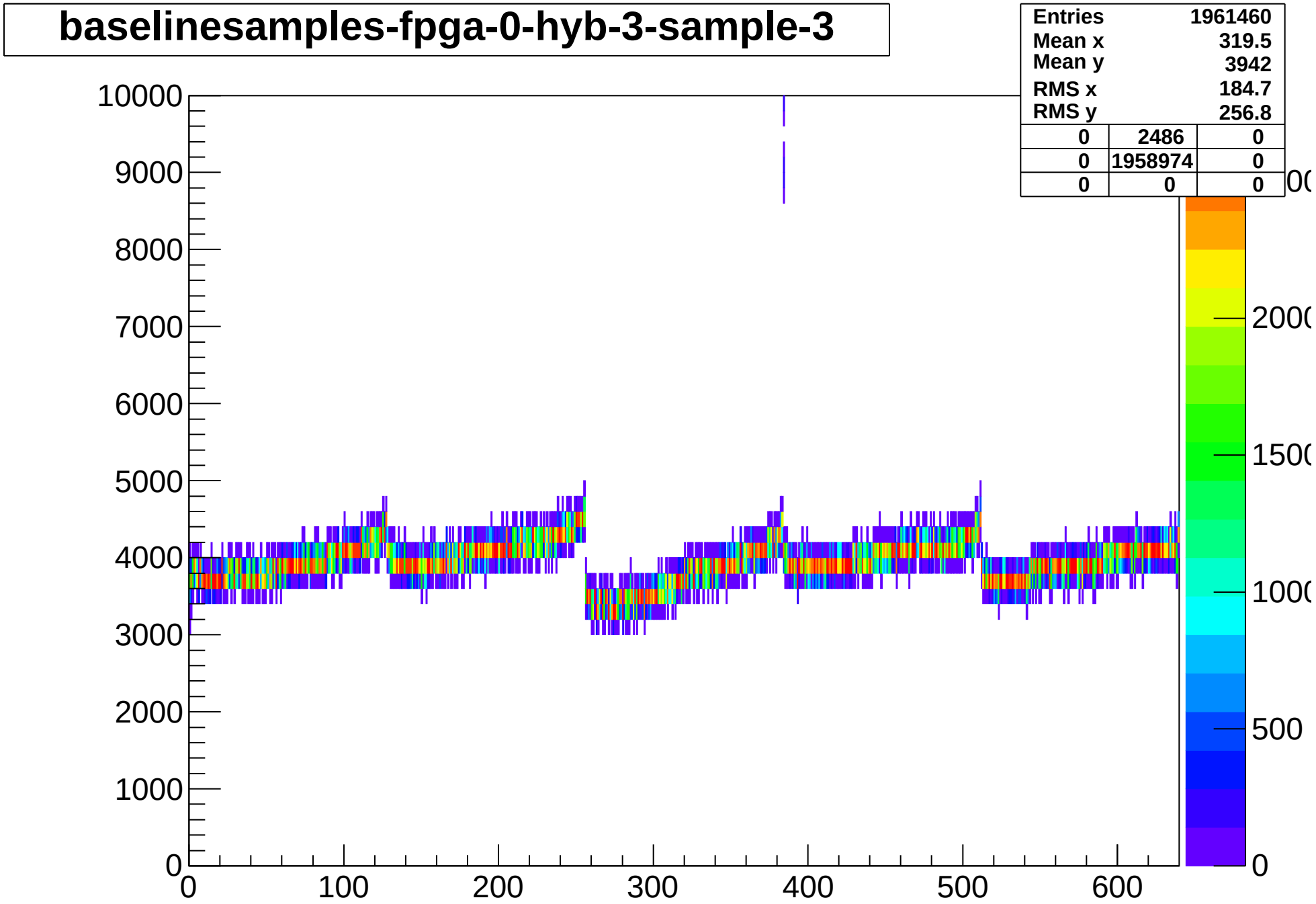

baselinesamples-fpga-0-hyb-2-sample-4
Entries 1961460
Mean x 319.5
Mean y 4271
RMS x 184.8
RMS y 336.3
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

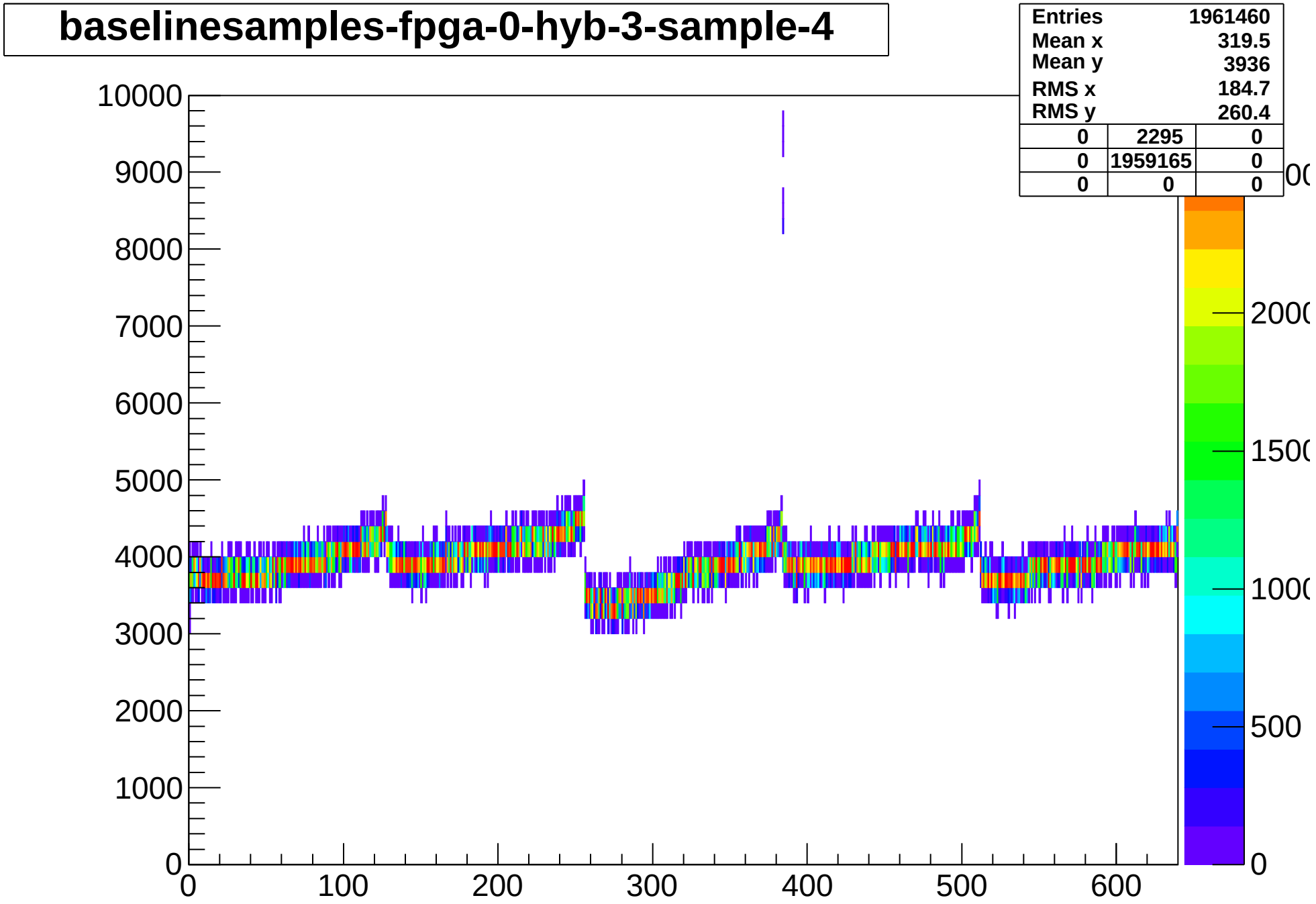

baselinesamples-fpga-0-hyb-2-sample-5
Entries 1961460
Mean x 319.5
Mean y 4275
RMS x 184.8
RMS y 336.1
0 3060 0
0 1958400 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

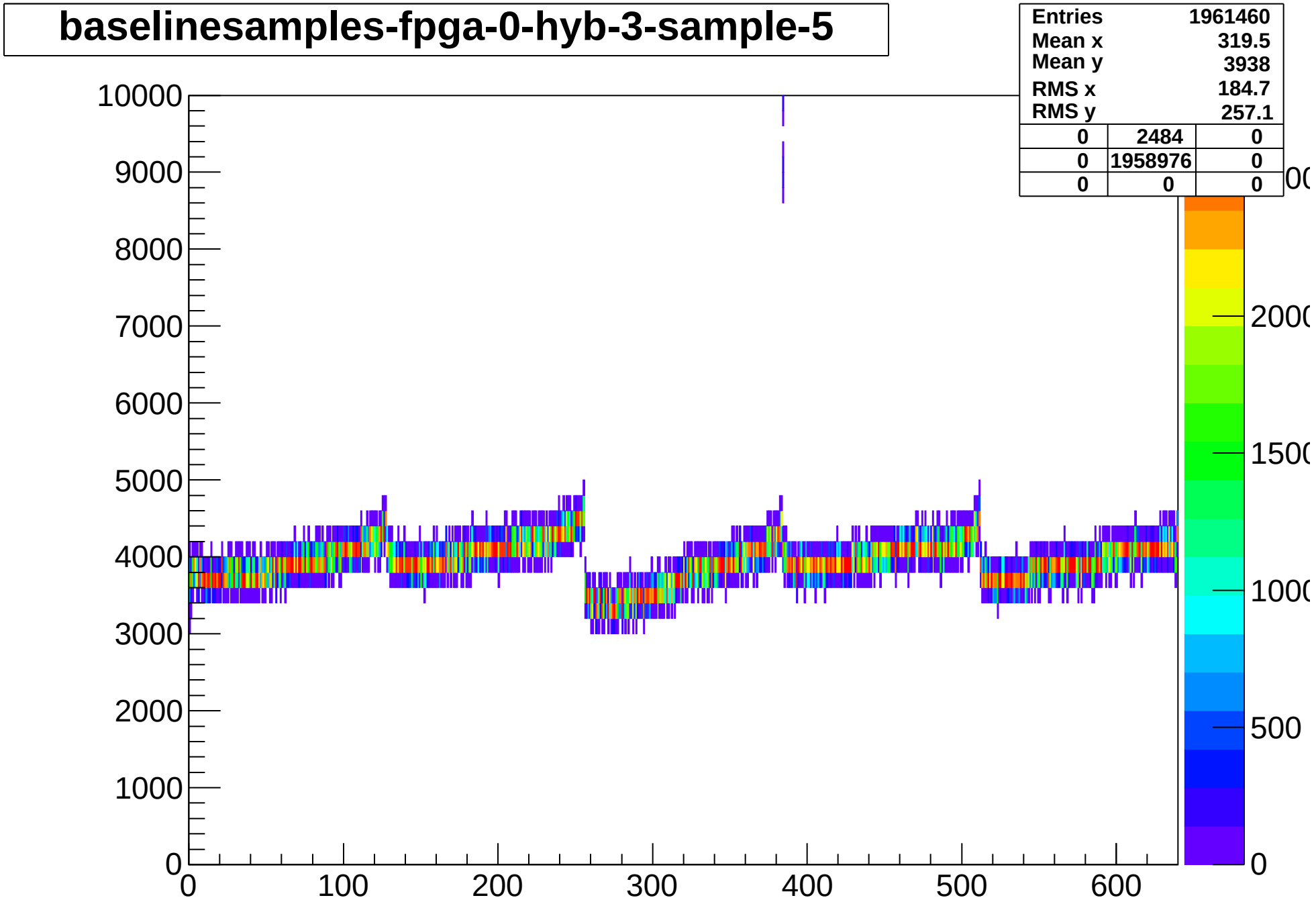

baselinesamples-fpga-0-hyb-3-sample-0
Entries 1961460
Mean x 319.5
Mean y 3889
RMS x 184.7
RMS y 262.8
0 2294 0
0 1959166 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

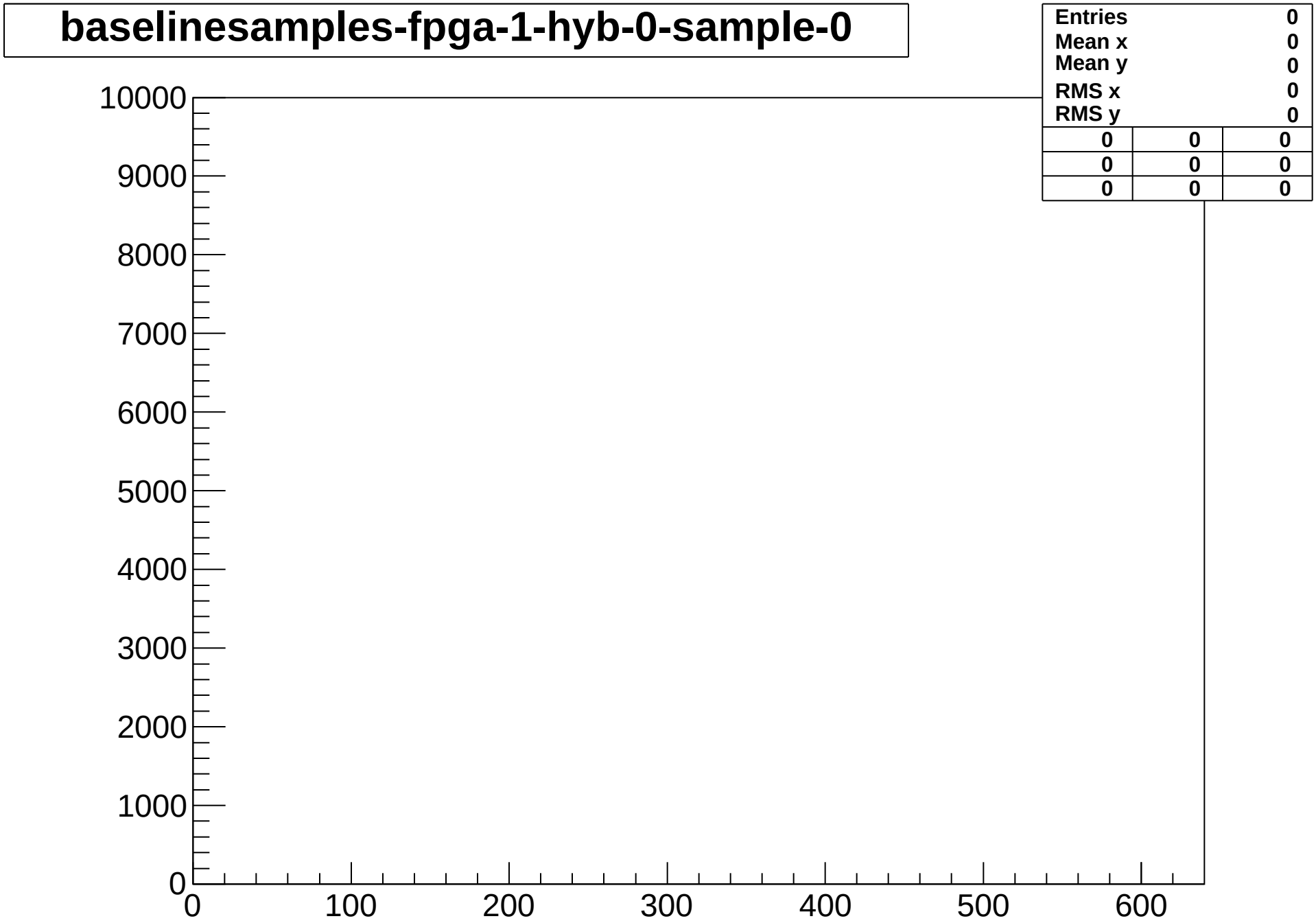

baselinesamples-fpga-0-hyb-3-sample-1
Entries 1961460
Mean x 319.5
Mean y 3941
RMS x 184.7
RMS y 256.6
0 2484 0
0 1958976 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0


baselinesamples-fpga-0-hyb-3-sample-2
Entries 1961460
Mean x 319.5
Mean y 3939
RMS x 184.7
RMS y 260.1
0 2295 0
0 1959165 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

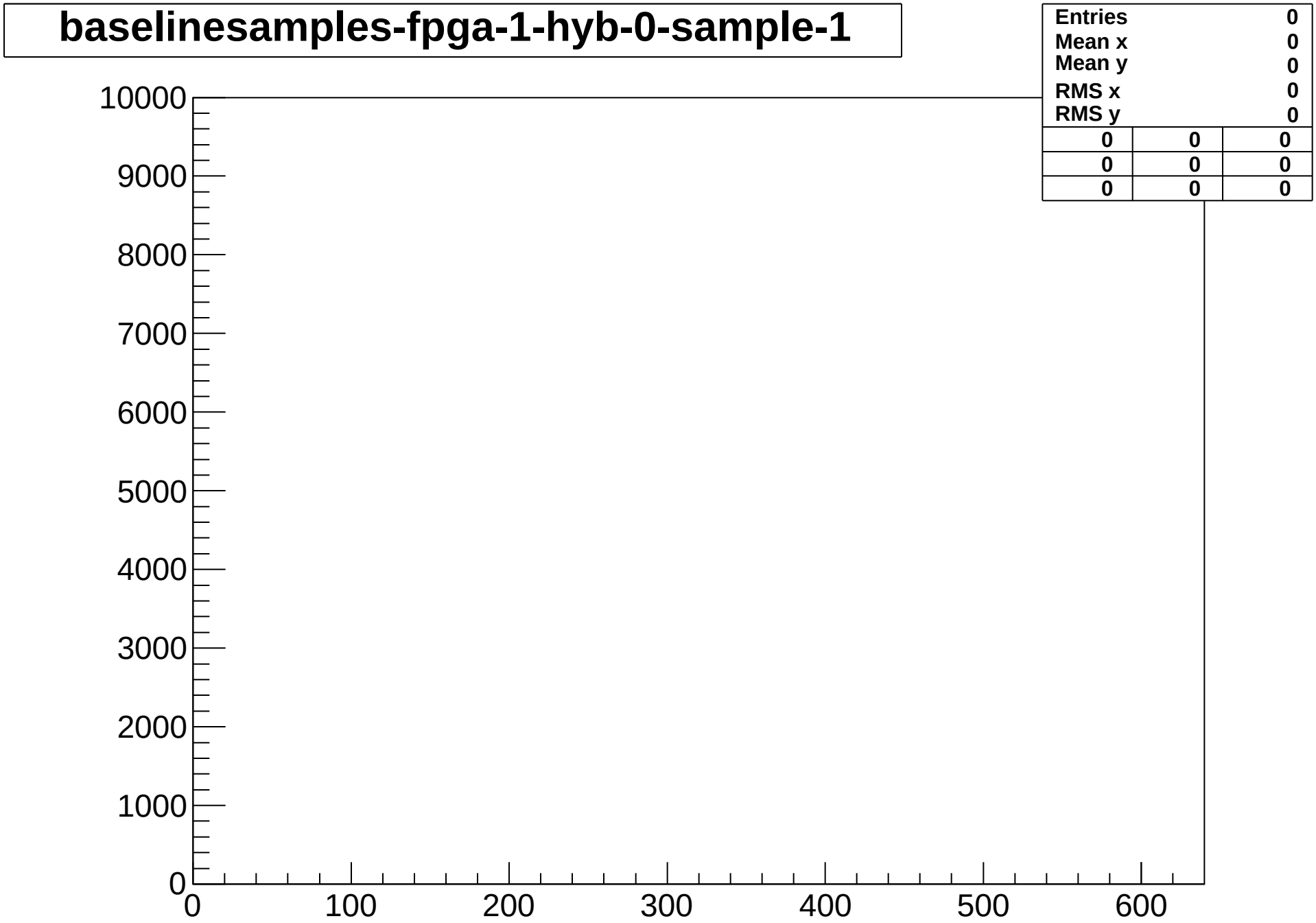

baselinesamples-fpga-0-hyb-3-sample-3
Entries 1961460
Mean x 319.5
Mean y 3942
RMS x 184.7
RMS y 256.8
0 2486 0
0 1958974 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0


baselinesamples-fpga-0-hyb-3-sample-4
Entries 1961460
Mean x 319.5
Mean y 3936
RMS x 184.7
RMS y 260.4
0 2295 0
0 1959165 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0

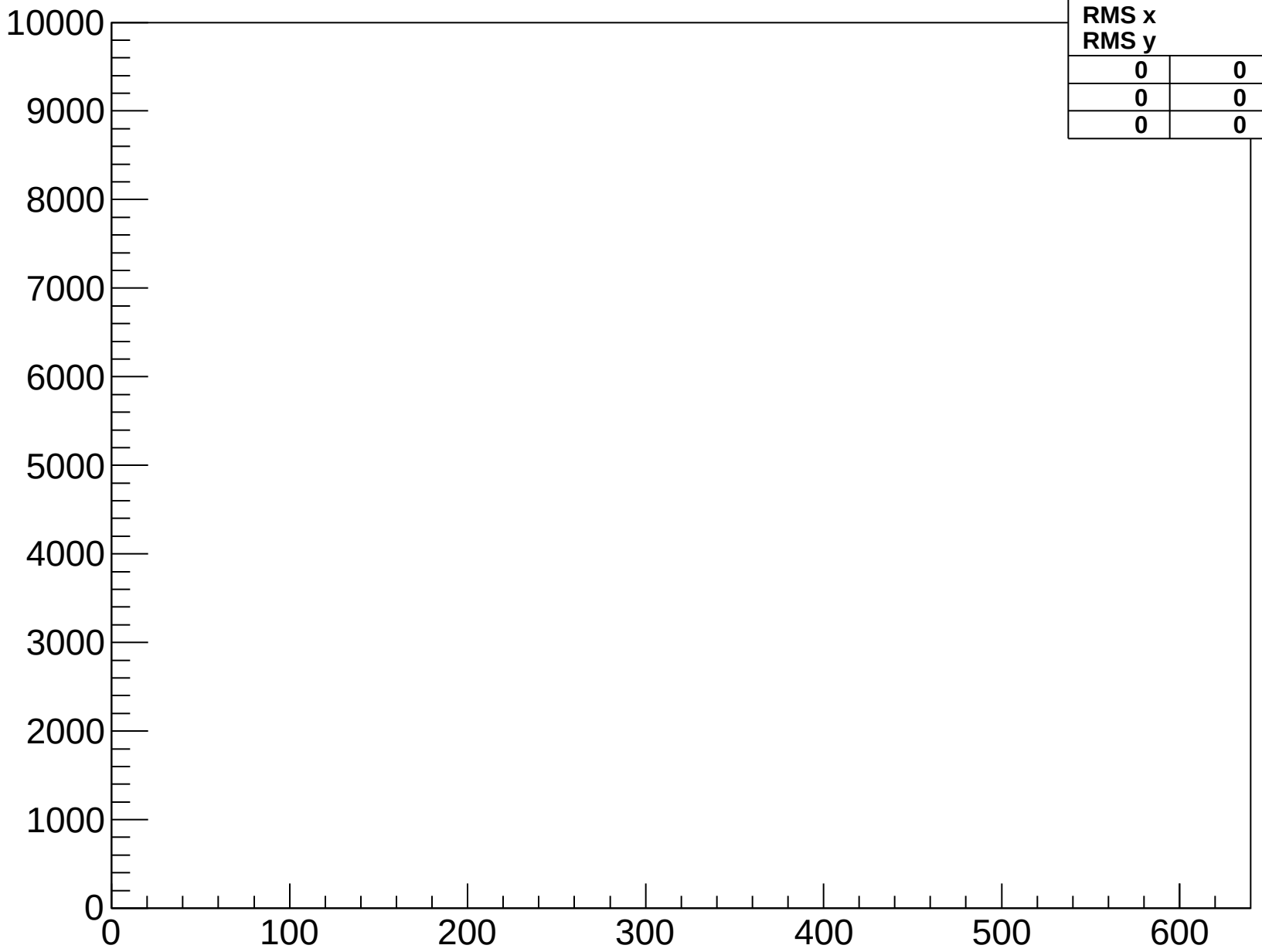

baselinesamples-fpga-0-hyb-3-sample-5
Entries 1961460
Mean x 319.5
Mean y 3938
RMS x 184.7
RMS y 257.1
0 2484 0
0 1958976 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
2000
1500
1000
500
0


baselinesamples-fpga-1-hyb-0-sample-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

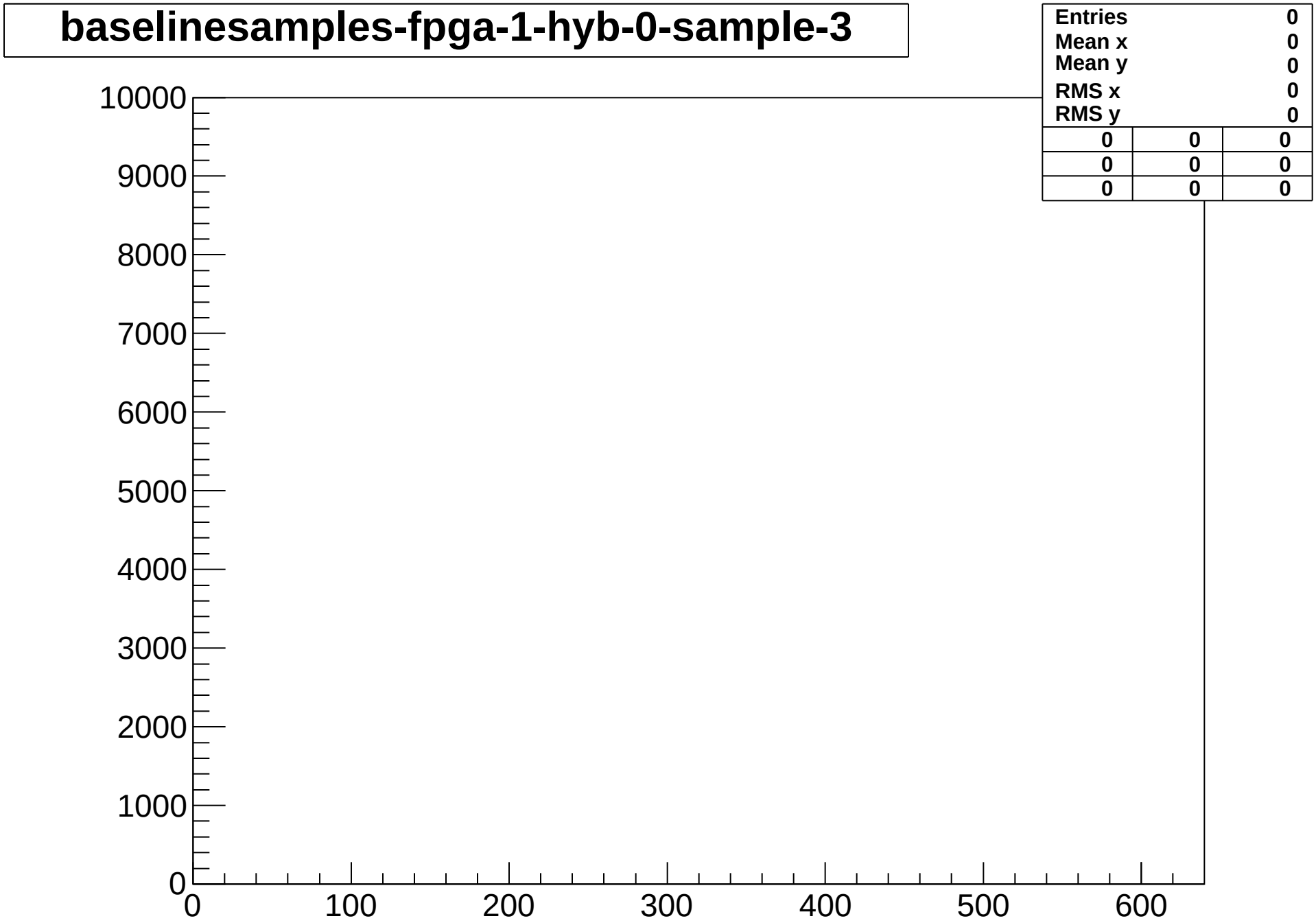
baselinesamples-fpga-1-hyb-0-sample-1



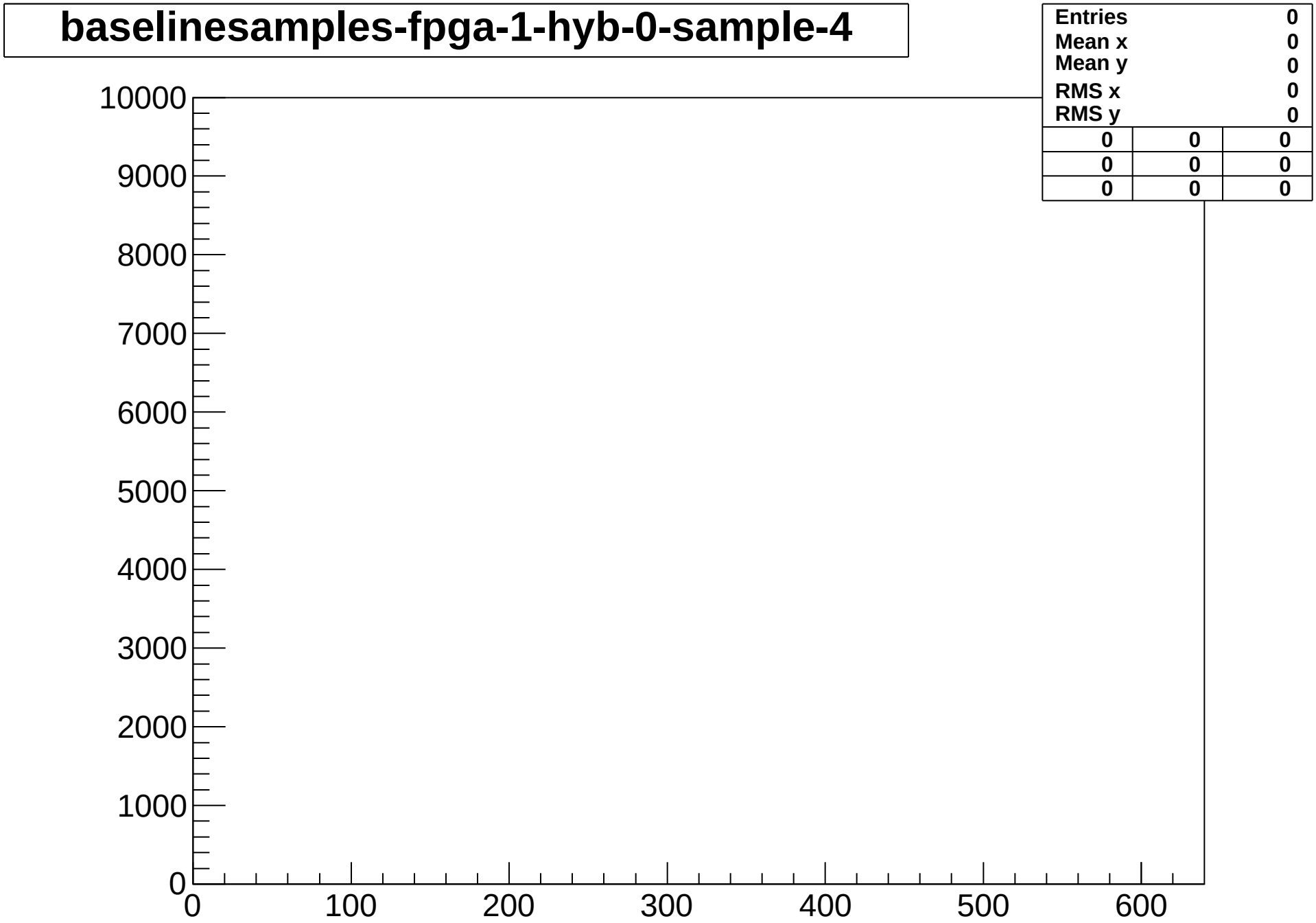
baselinesamples-fpga-1-hyb-0-sample-2



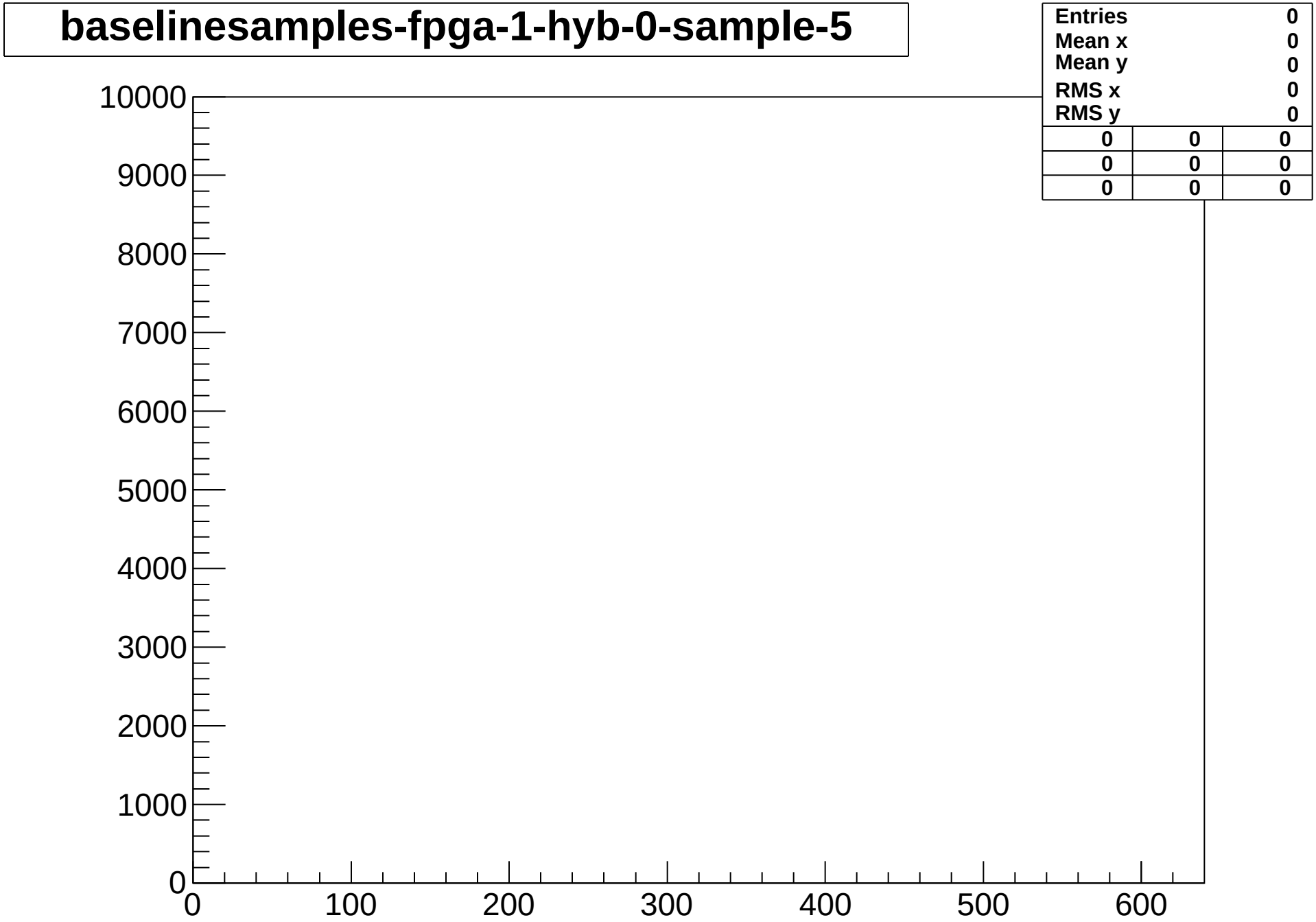
baselinesamples-fpga-1-hyb-0-sample-3

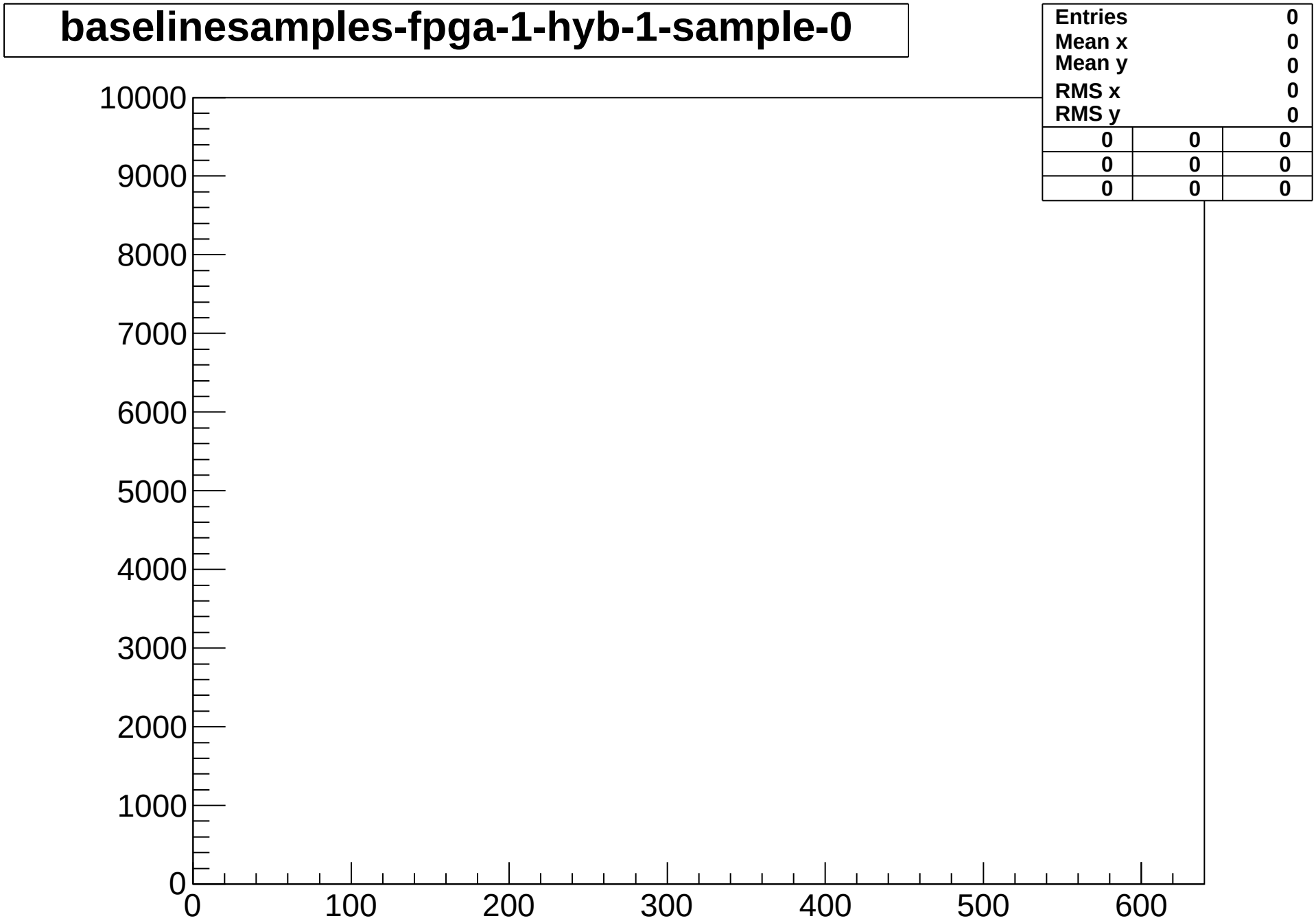


baselinesamples-fpga-1-hyb-0-sample-4

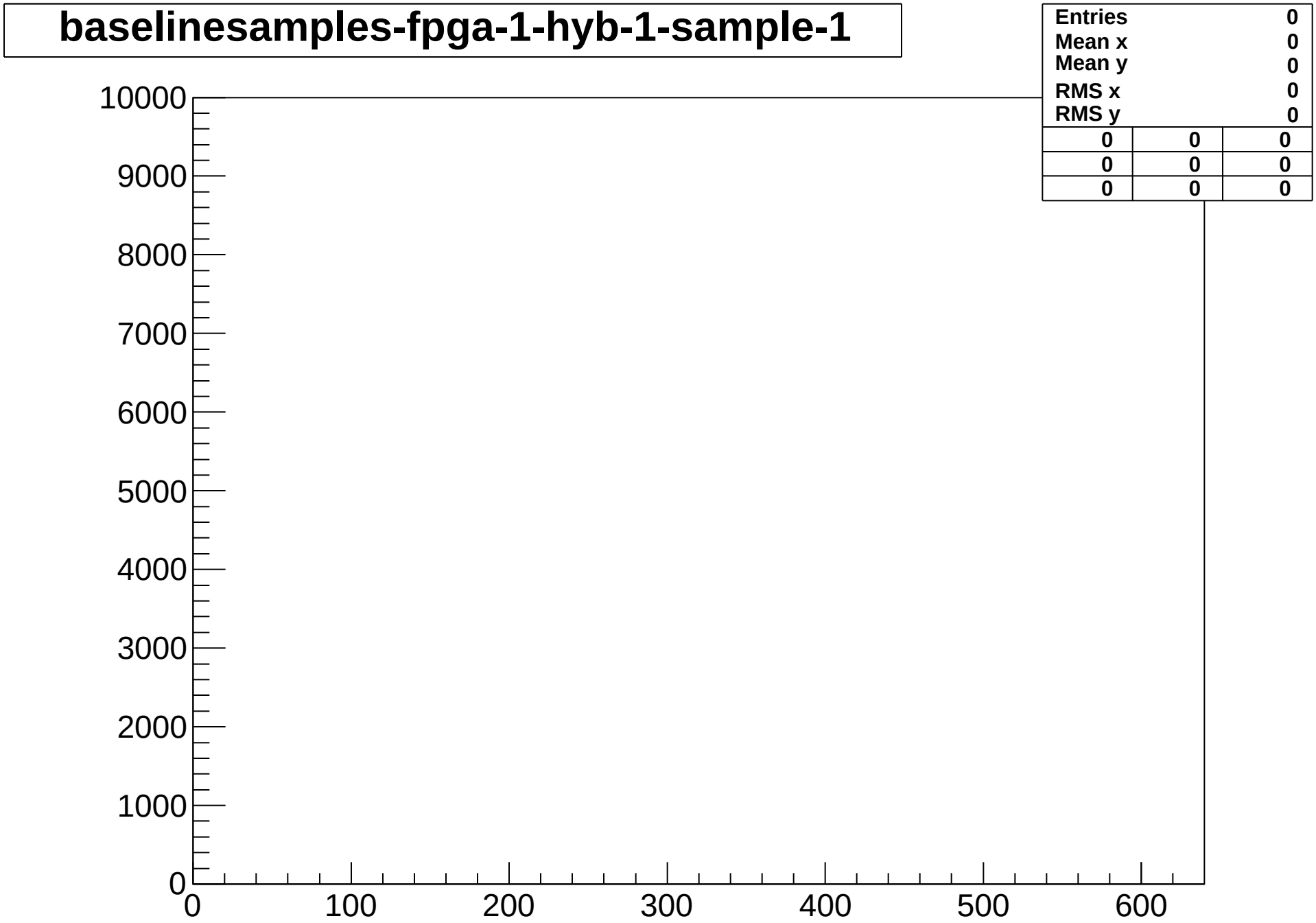


baselinesamples-fpga-1-hyb-0-sample-5

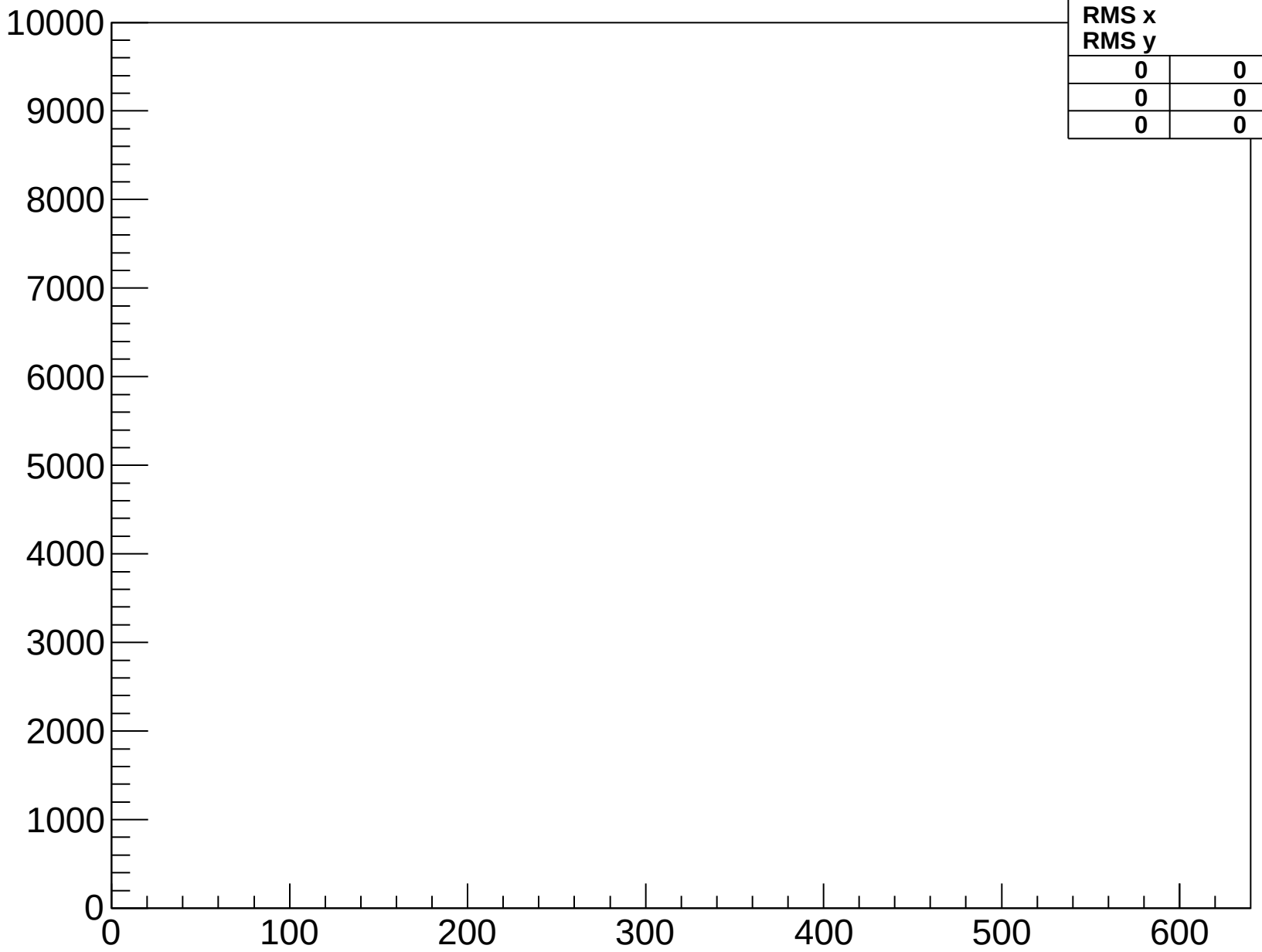



baselinesamples-fpga-1-hyb-1-sample-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

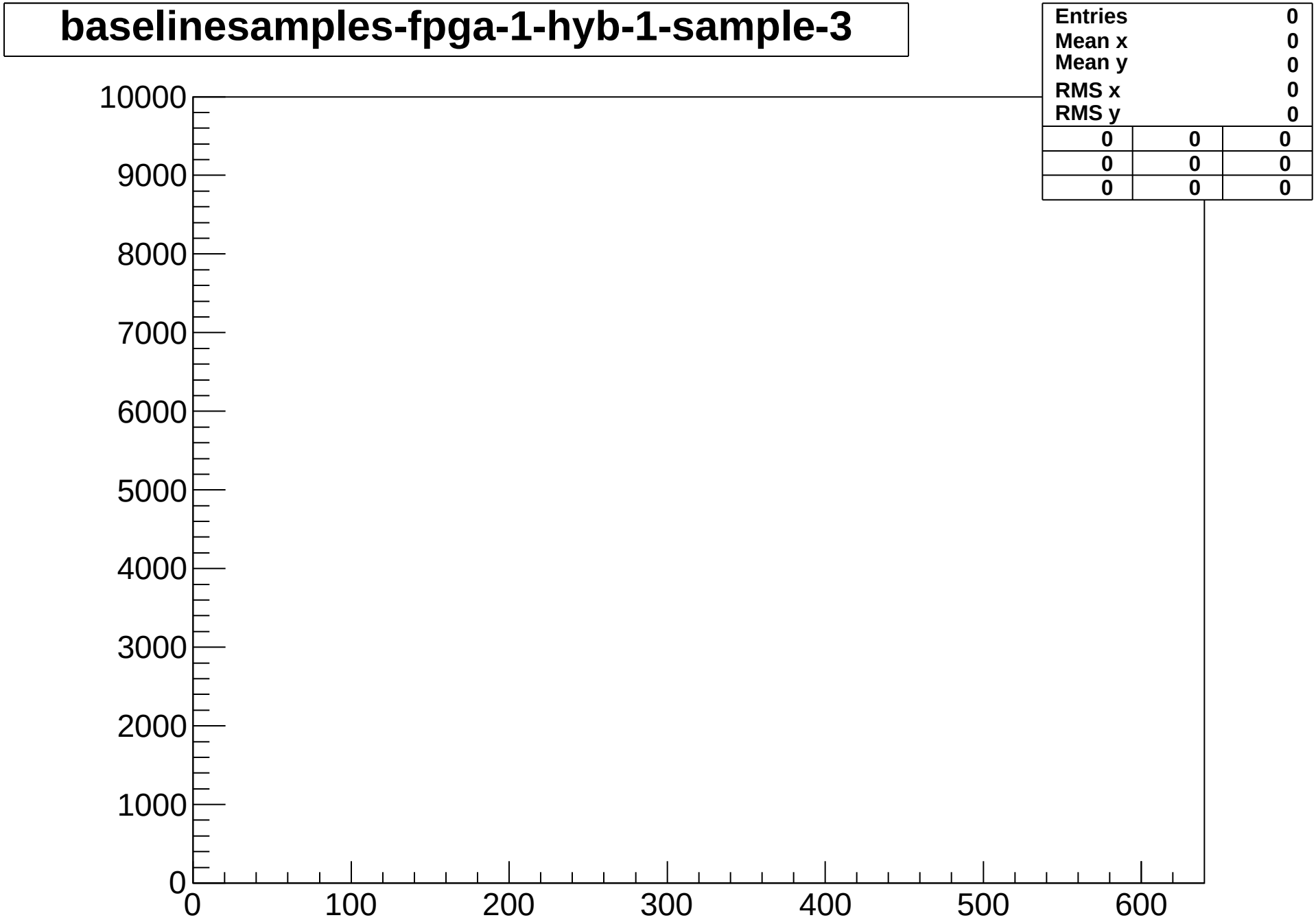
baselinesamples-fpga-1-hyb-1-sample-1



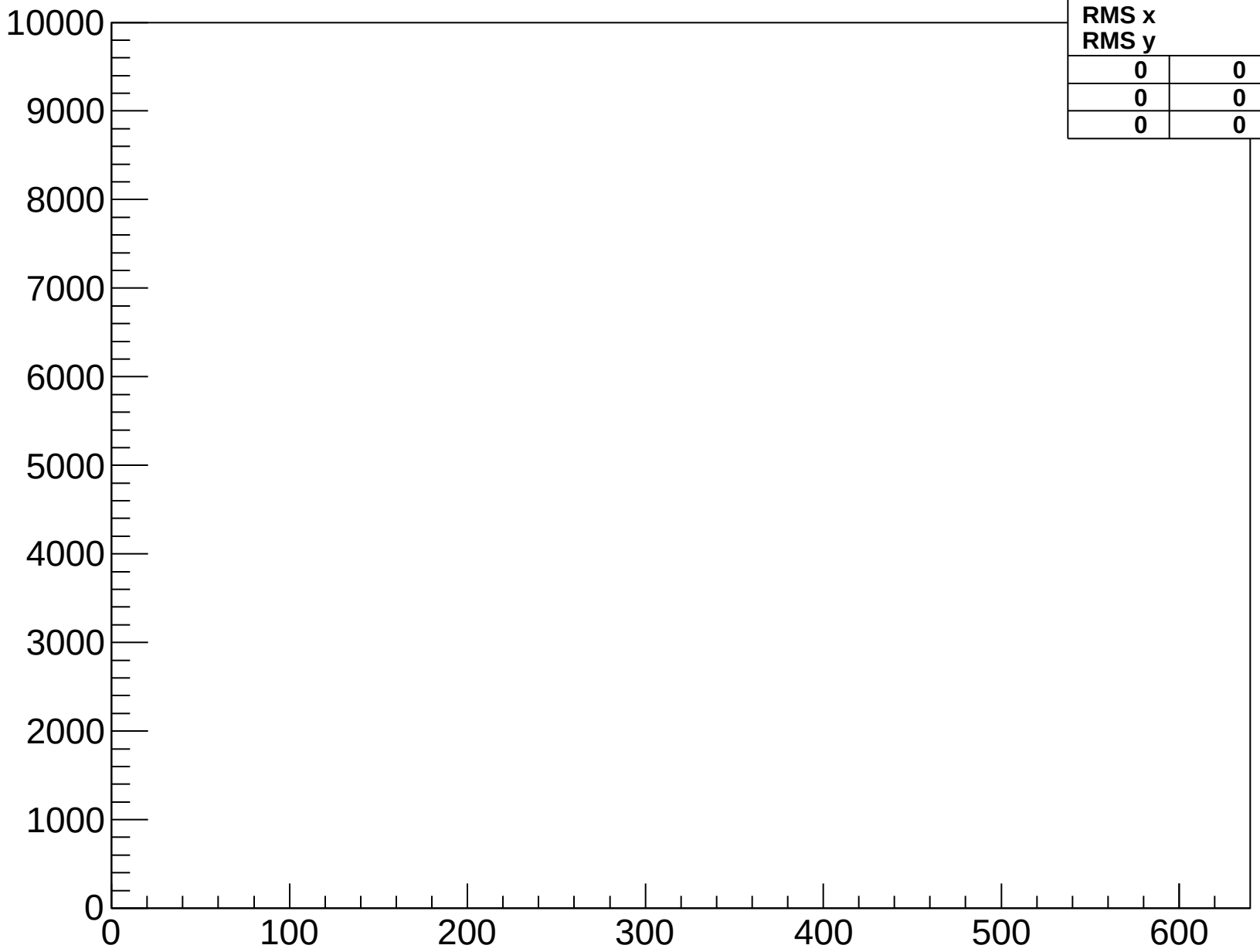
baselinesamples-fpga-1-hyb-1-sample-2



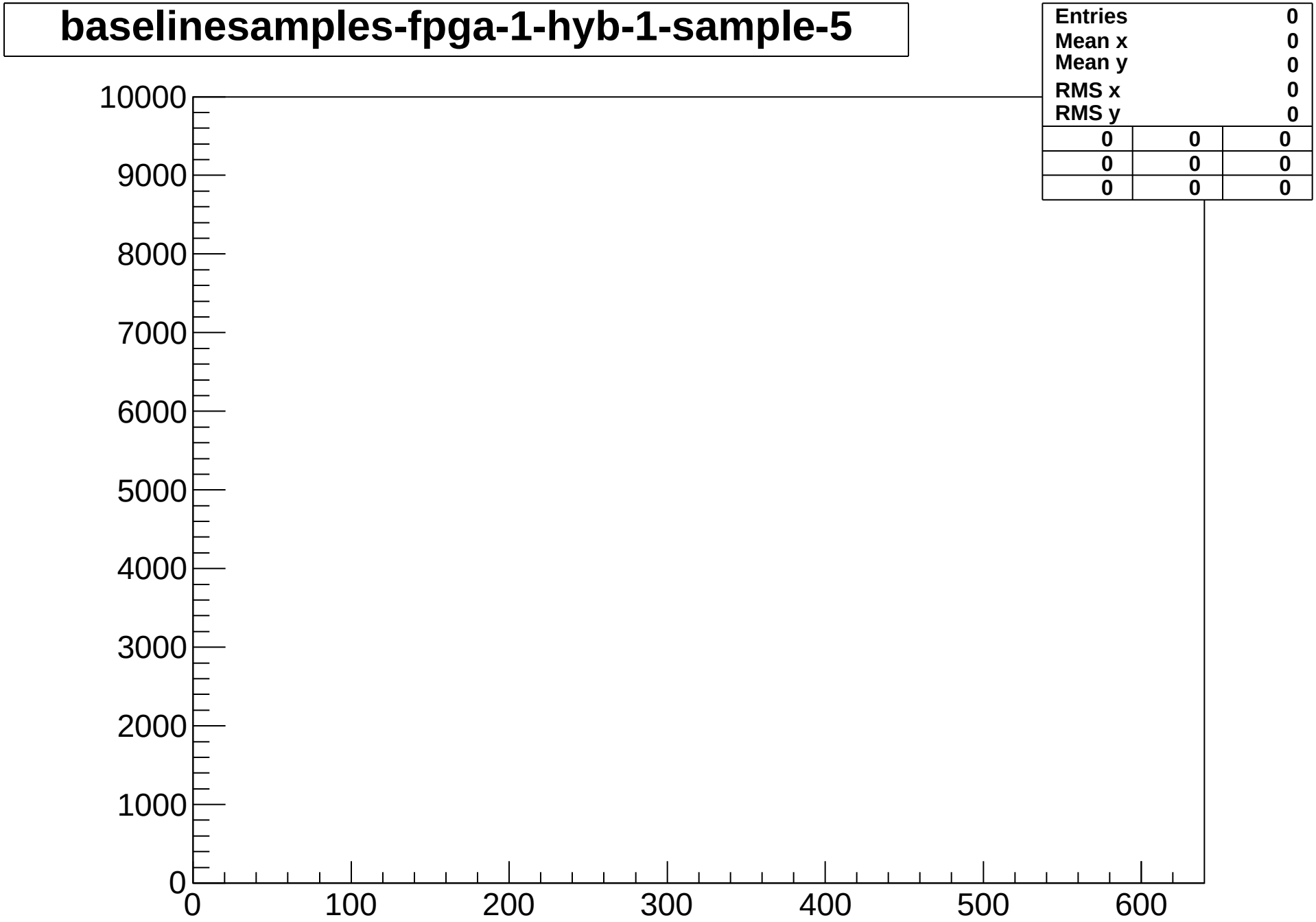
baselinesamples-fpga-1-hyb-1-sample-3



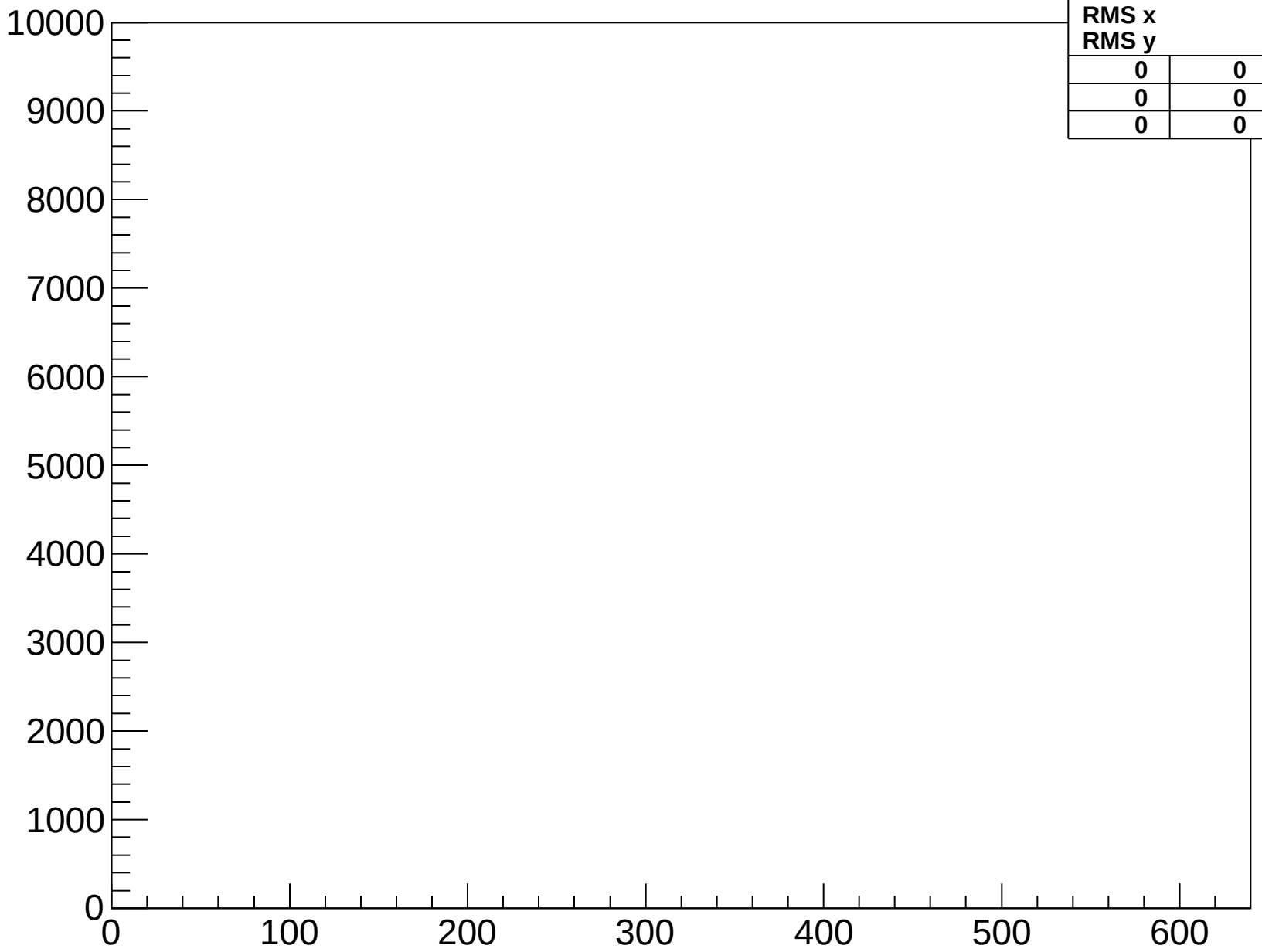
baselinesamples-fpga-1-hyb-1-sample-4



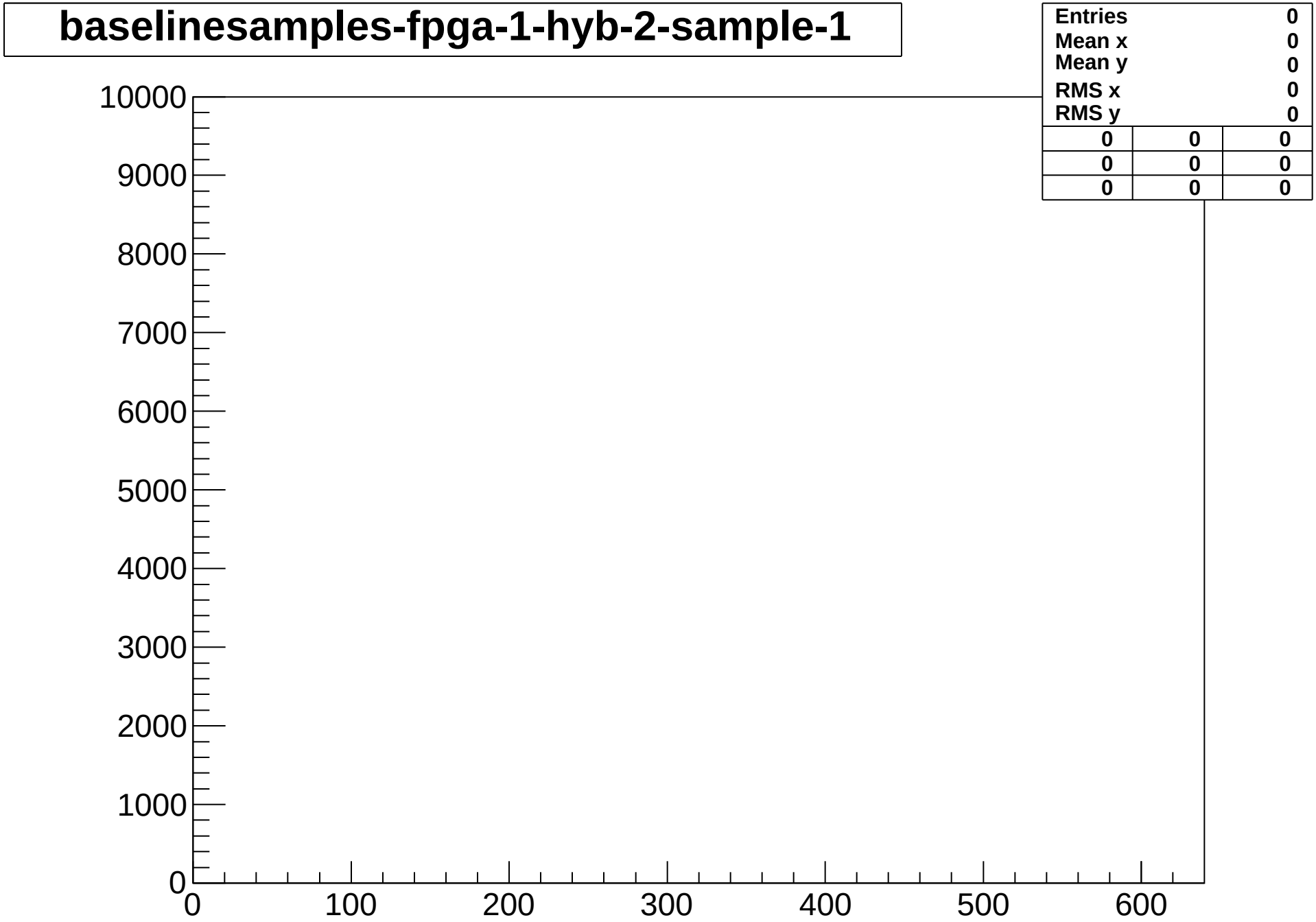
baselinesamples-fpga-1-hyb-1-sample-5



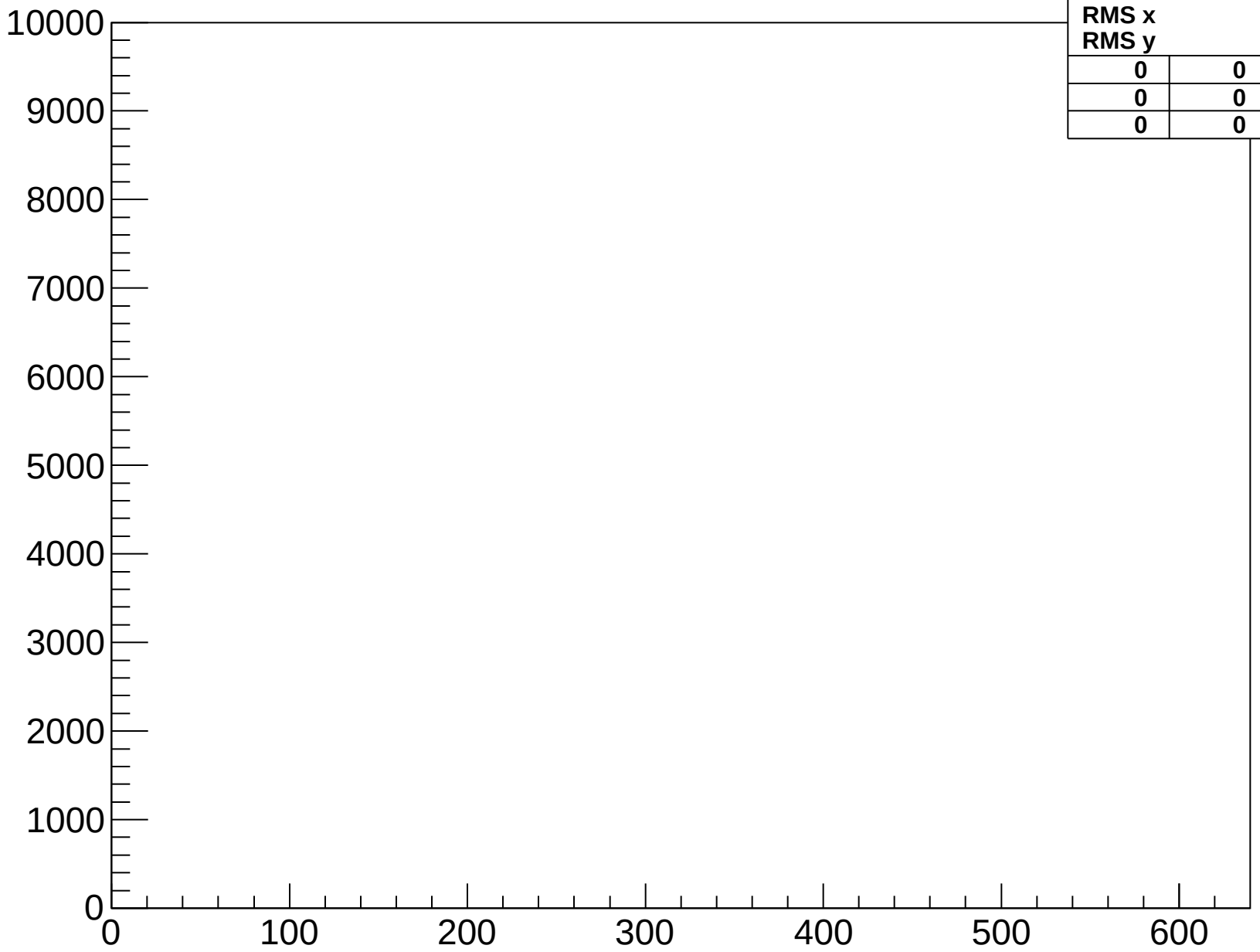
baselinesamples-fpga-1-hyb-2-sample-0



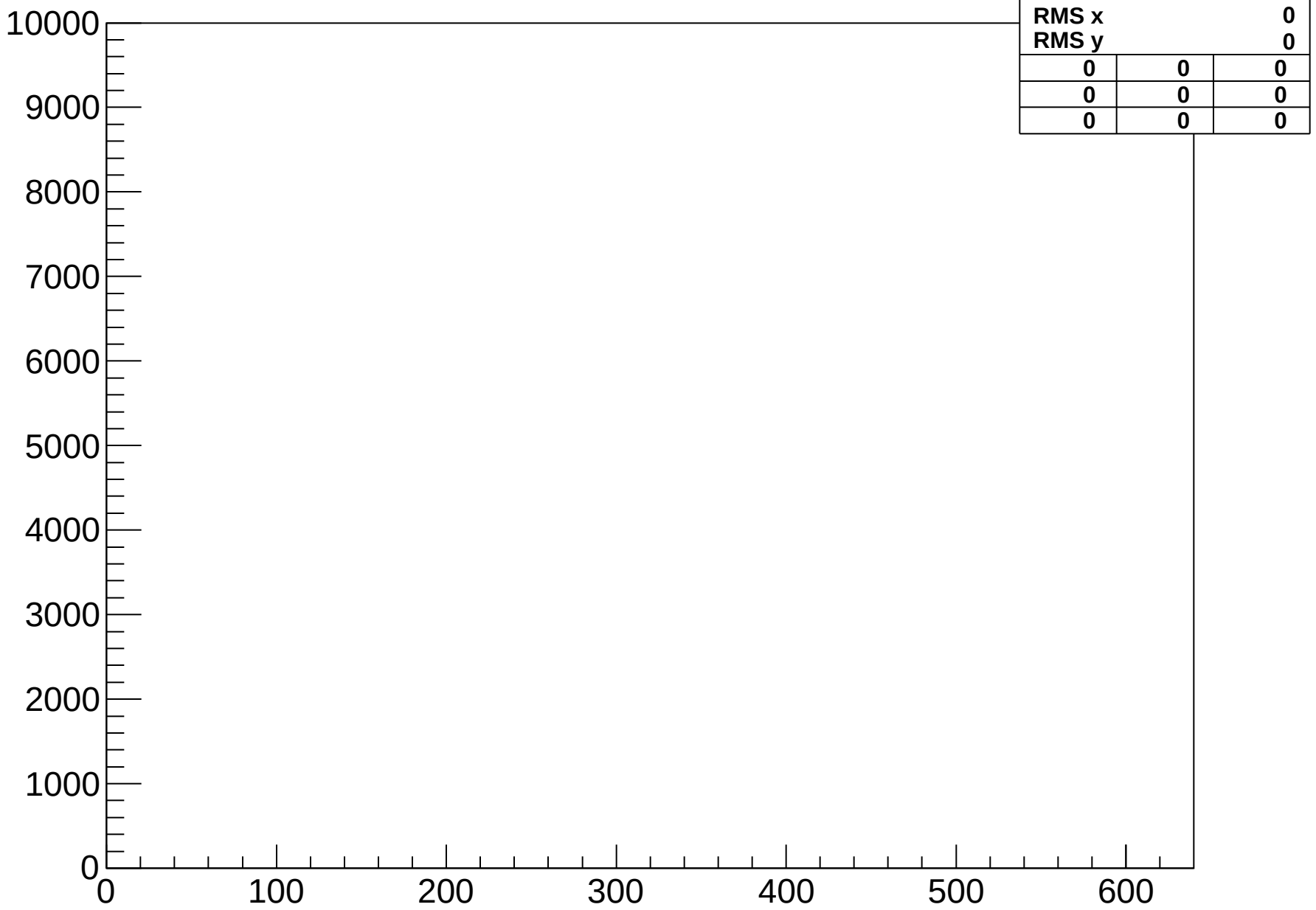
baselinesamples-fpga-1-hyb-2-sample-1



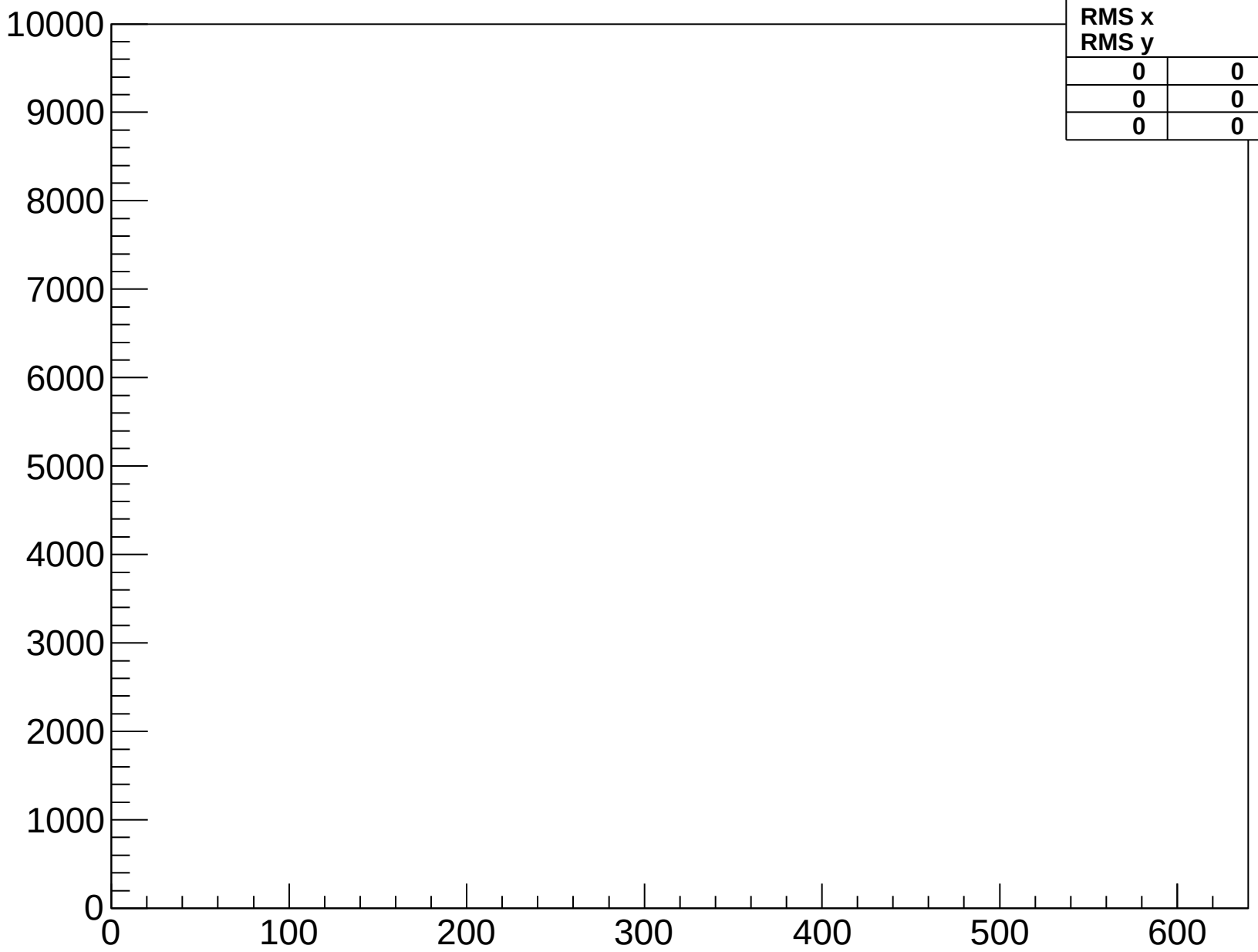
baselinesamples-fpga-1-hyb-2-sample-2



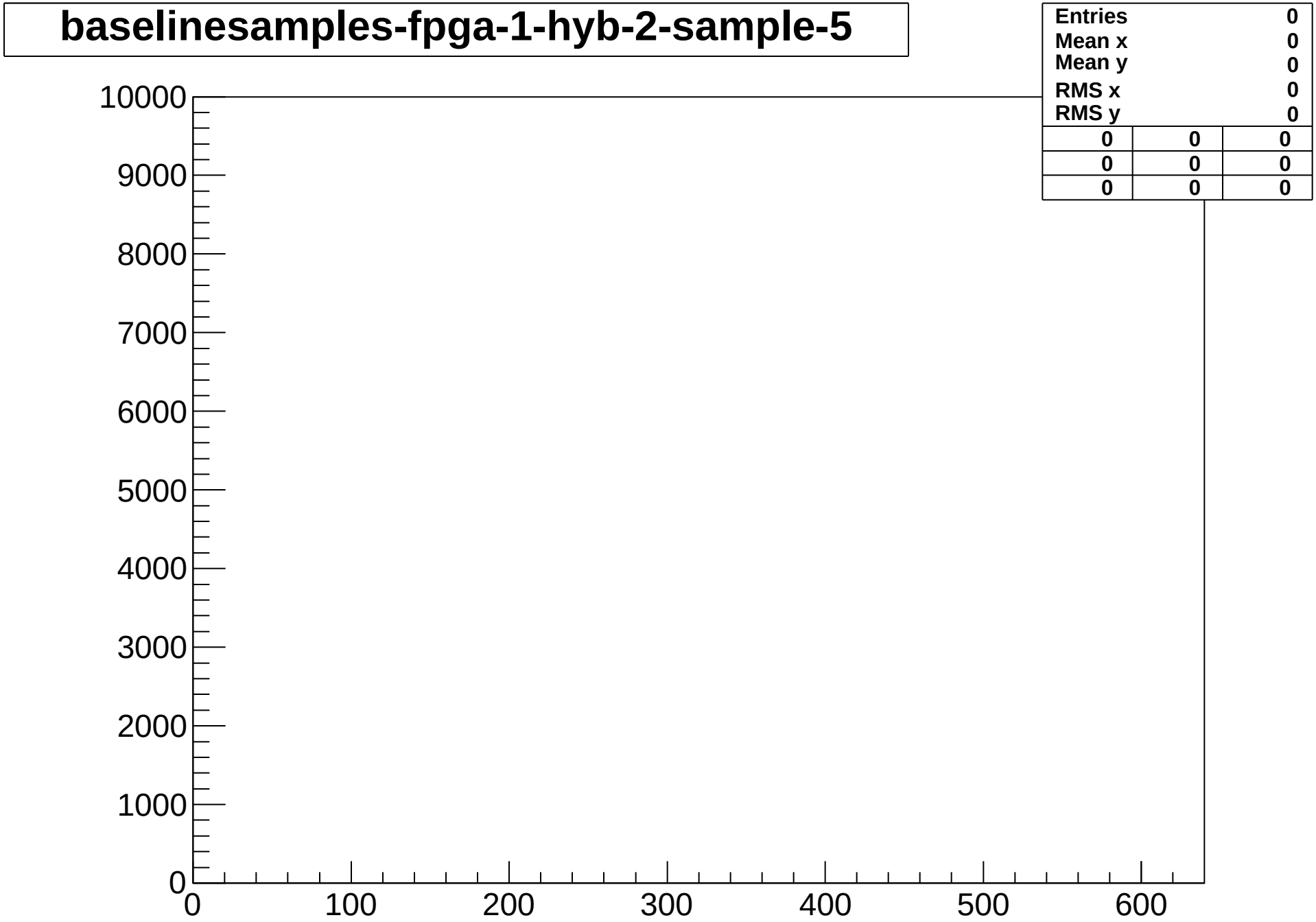
baselinesamples-fpga-1-hyb-2-sample-3



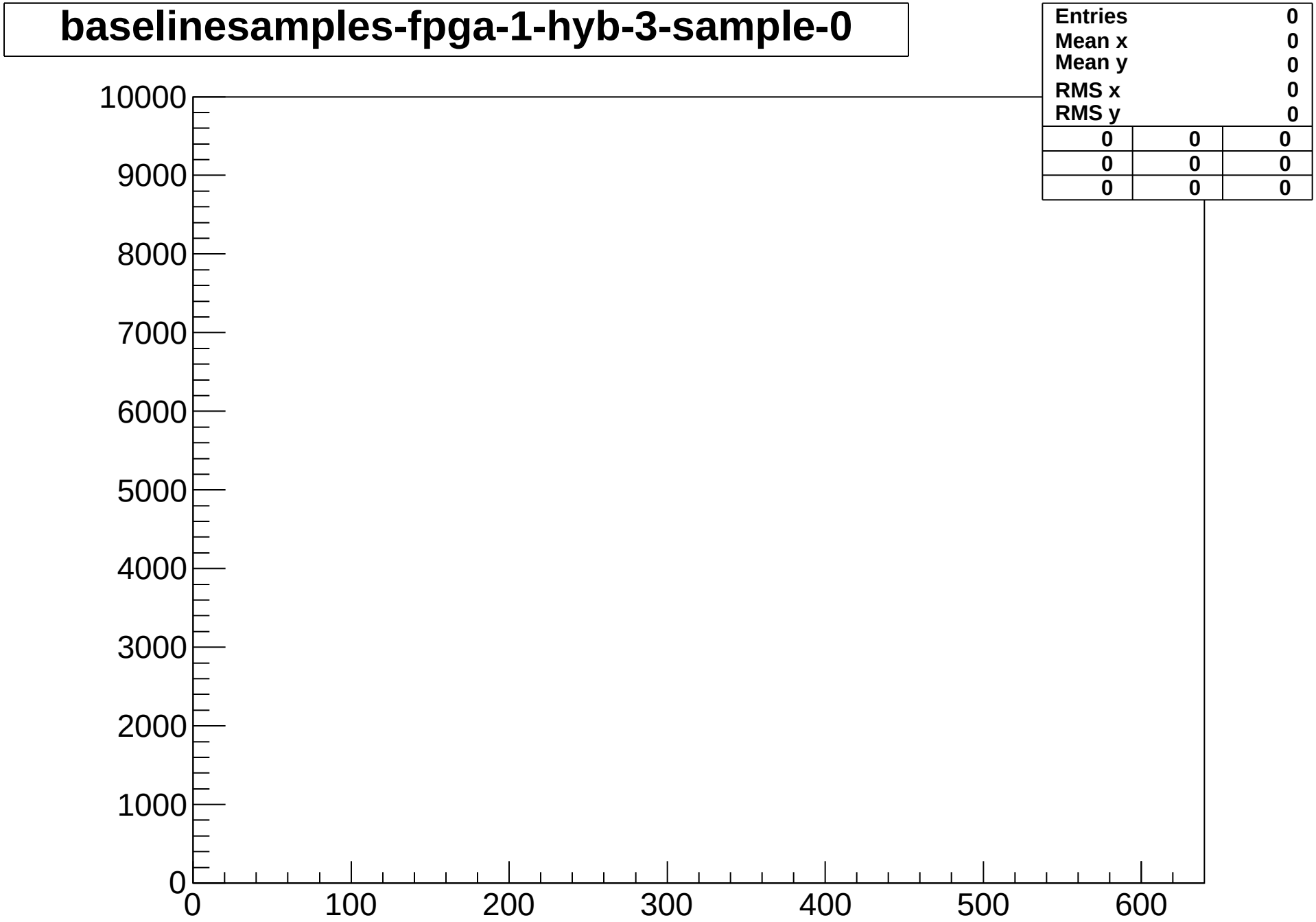
baselinesamples-fpga-1-hyb-2-sample-4



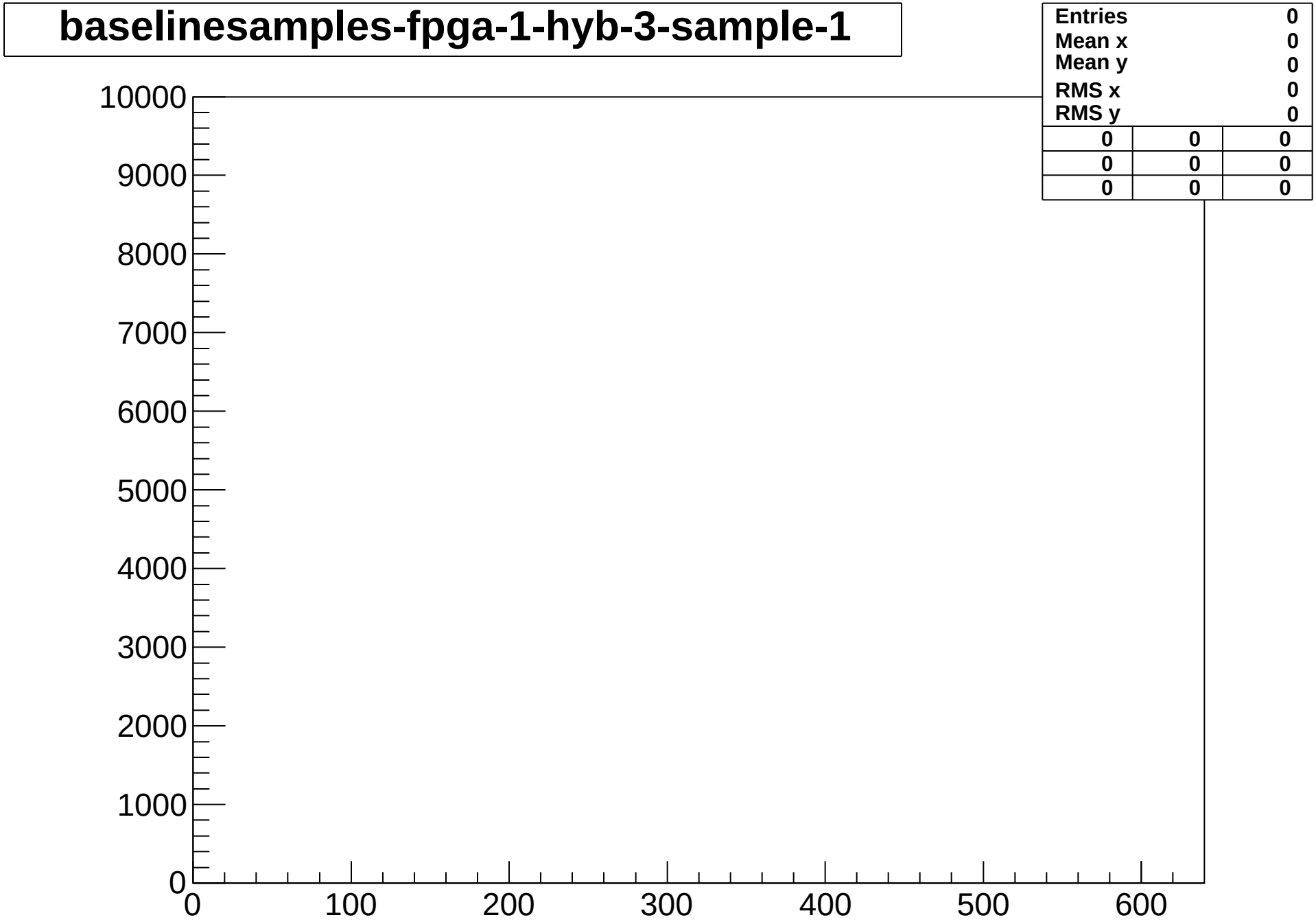
baselinesamples-fpga-1-hyb-2-sample-5



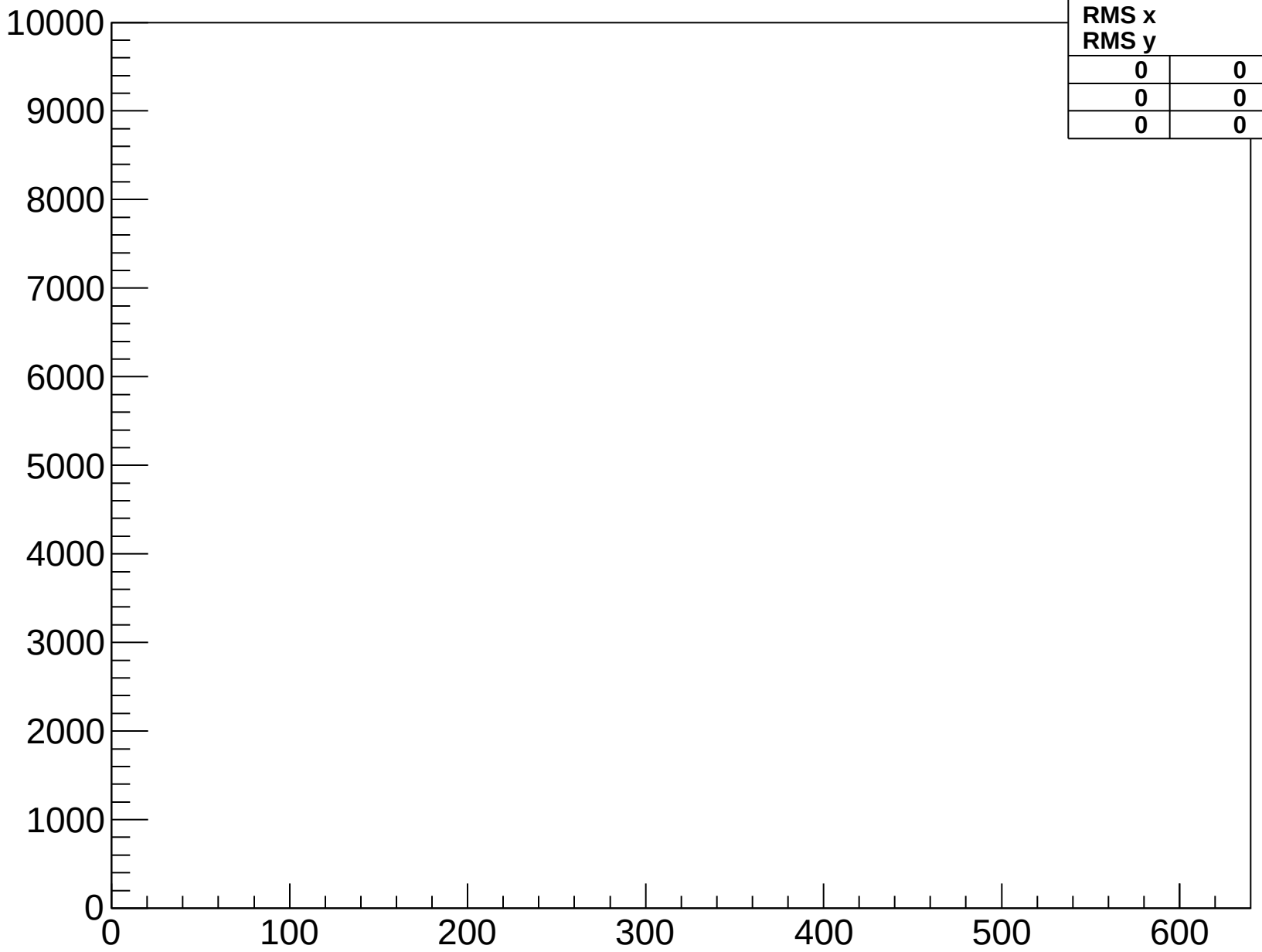
baselinesamples-fpga-1-hyb-3-sample-0



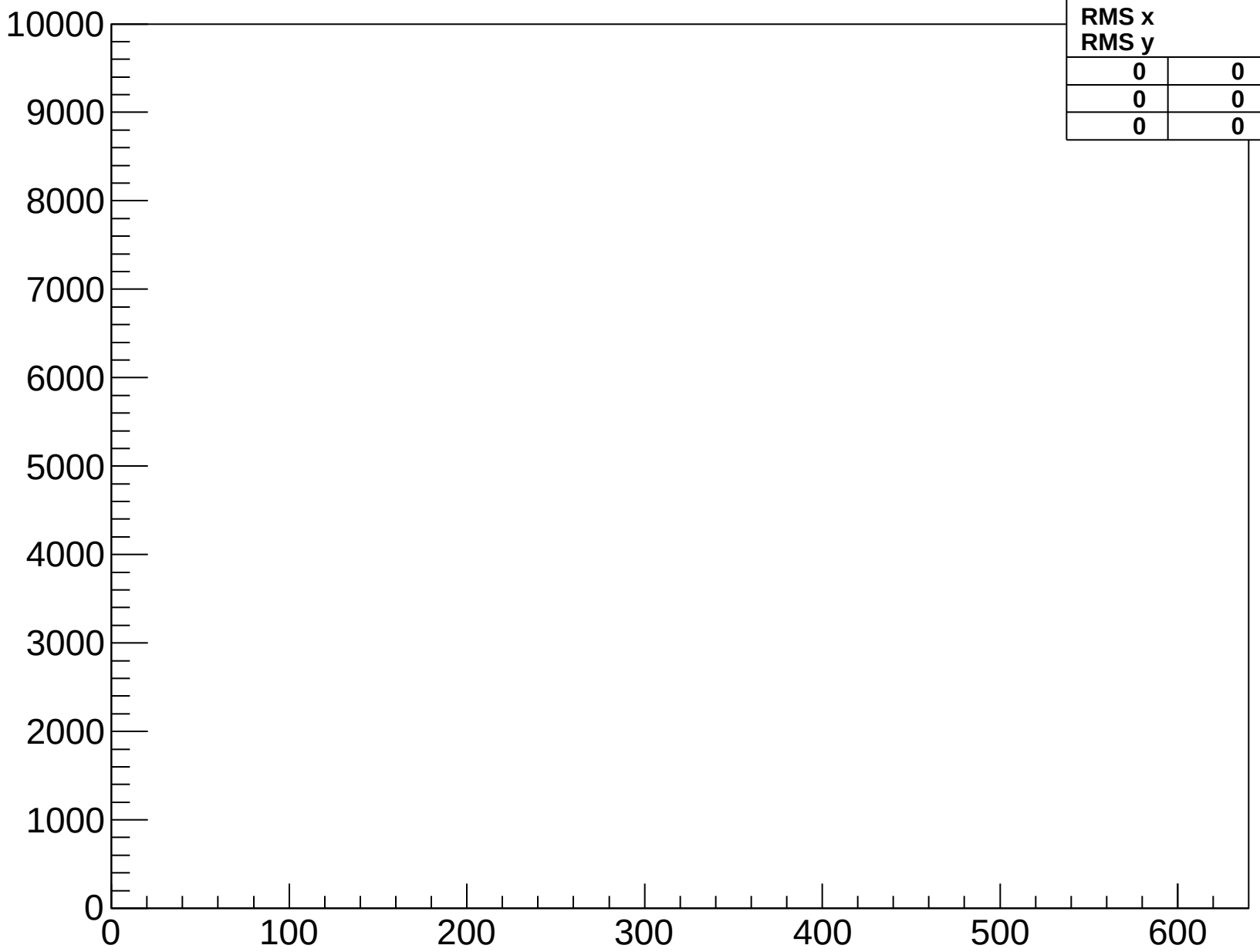
baselinesamples-fpga-1-hyb-3-sample-1



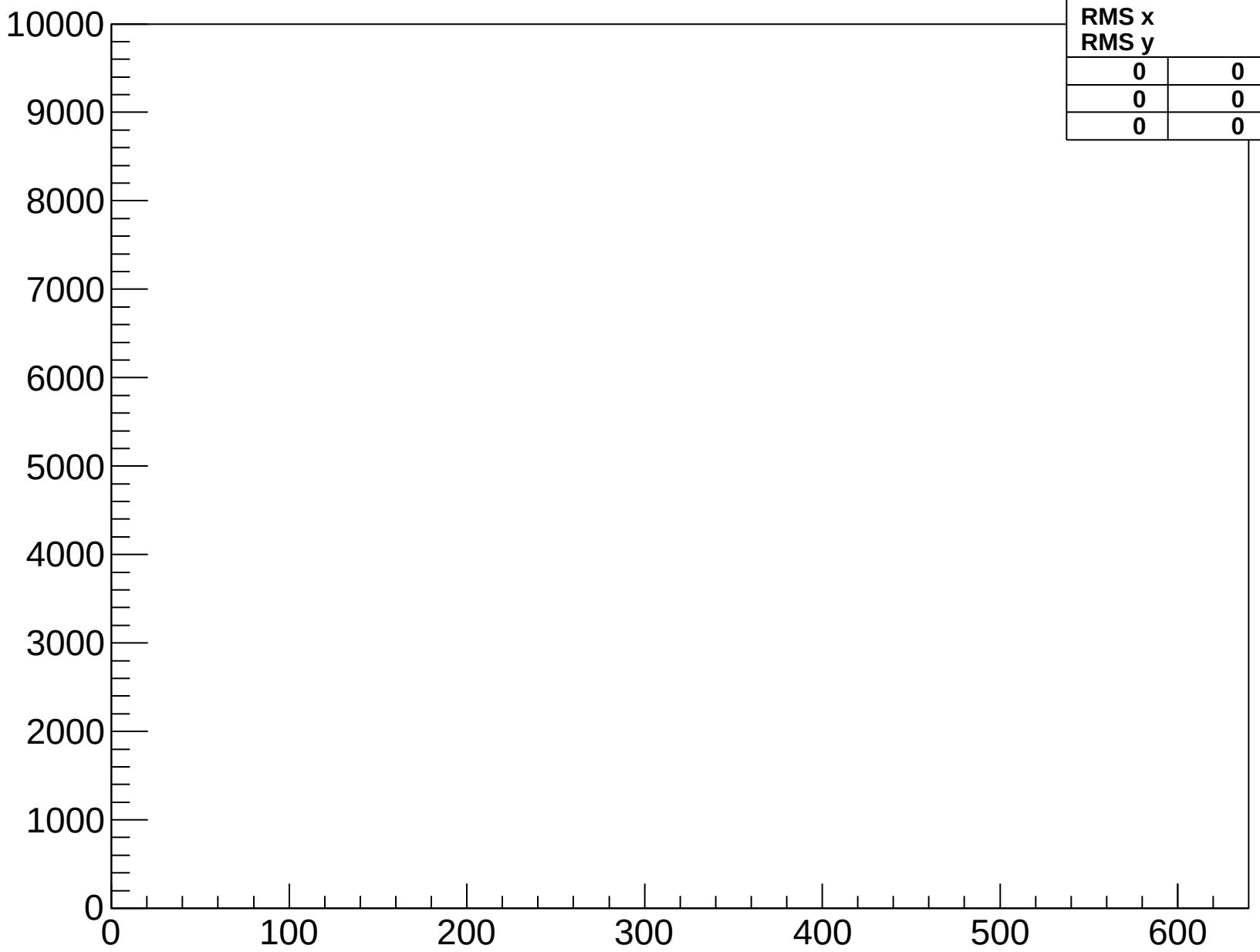
baselinesamples-fpga-1-hyb-3-sample-2



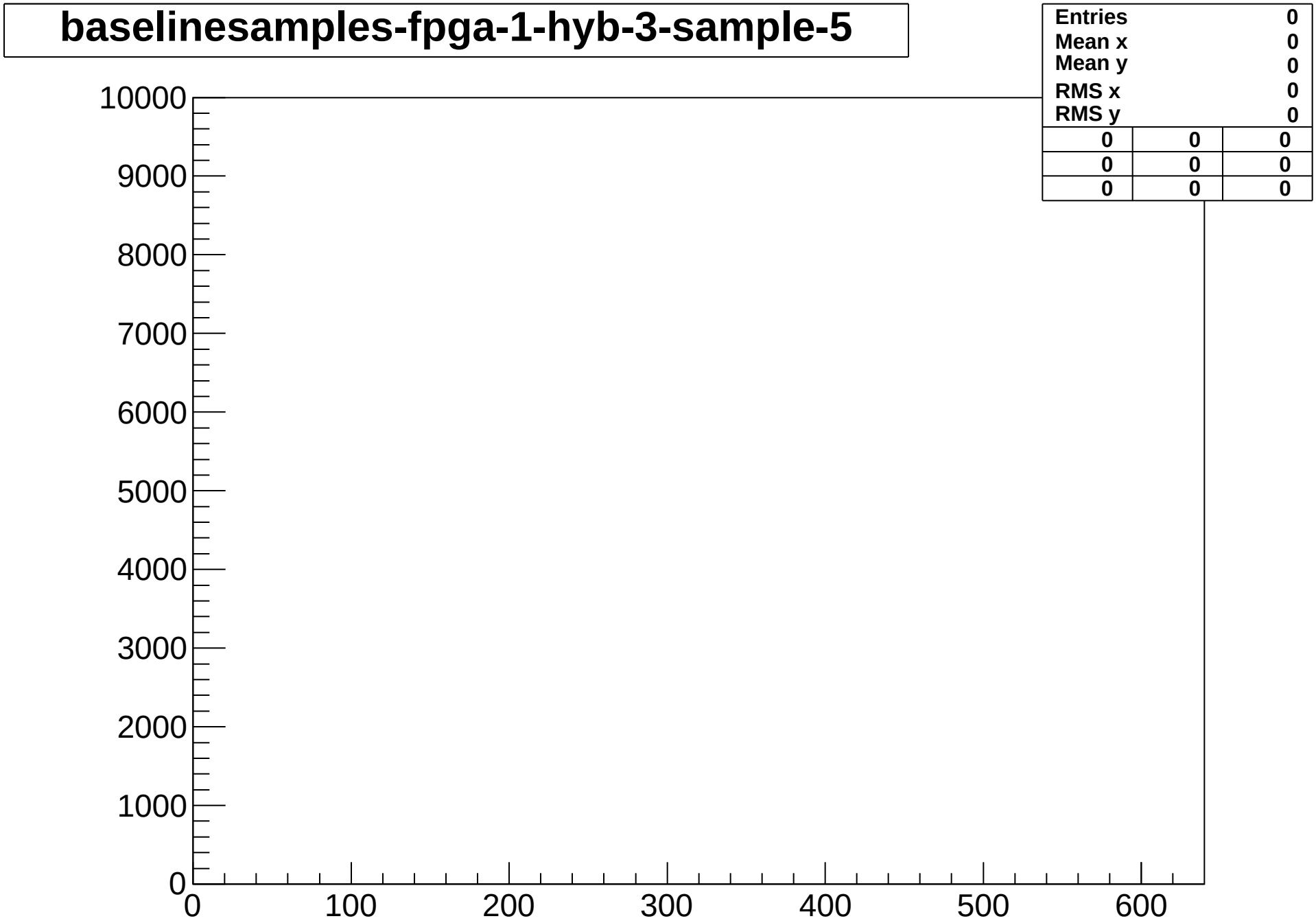
baselinesamples-fpga-1-hyb-3-sample-3



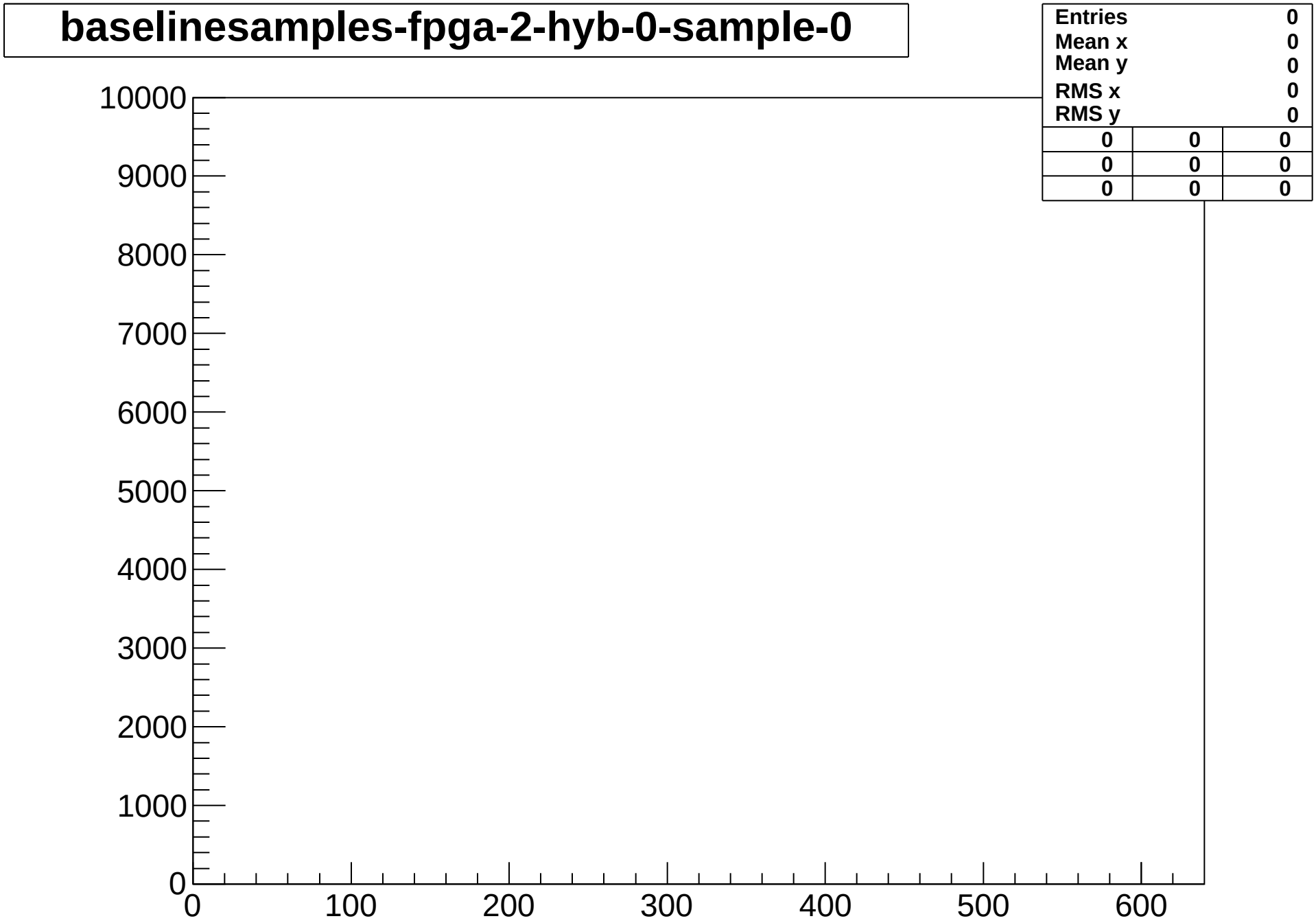
baselinesamples-fpga-1-hyb-3-sample-4

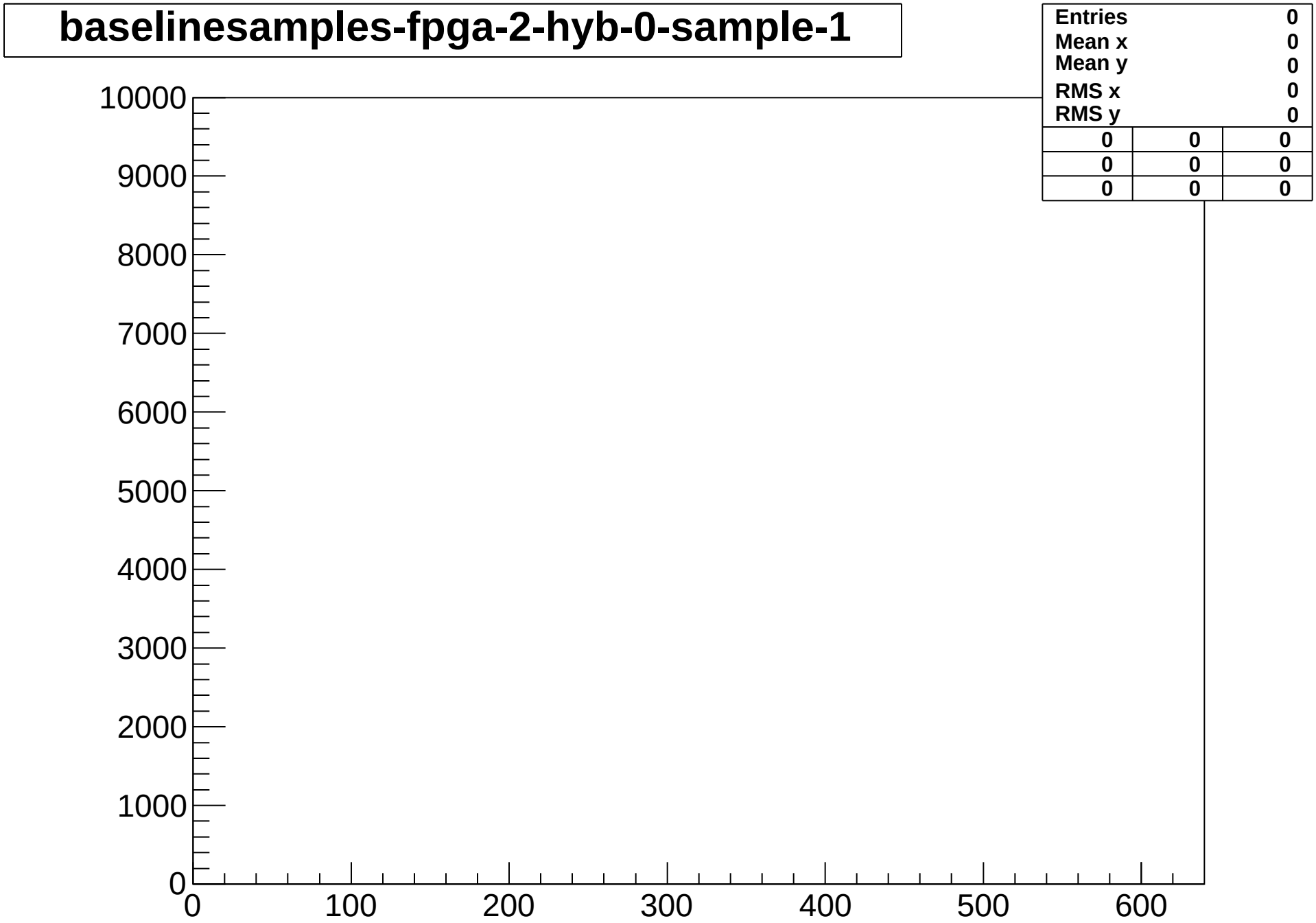


baselinesamples-fpga-1-hyb-3-sample-5

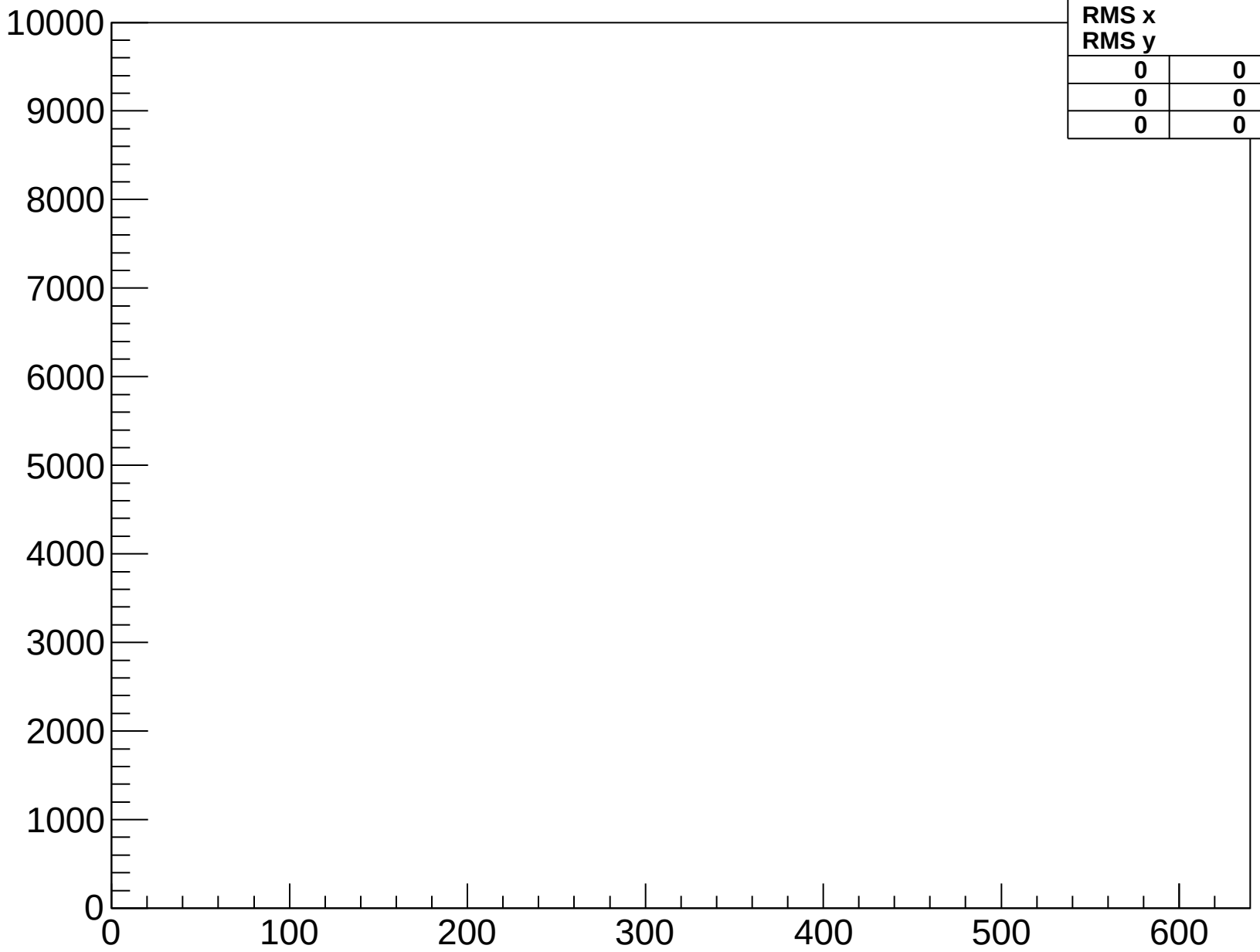


baselinesamples-fpga-2-hyb-0-sample-0

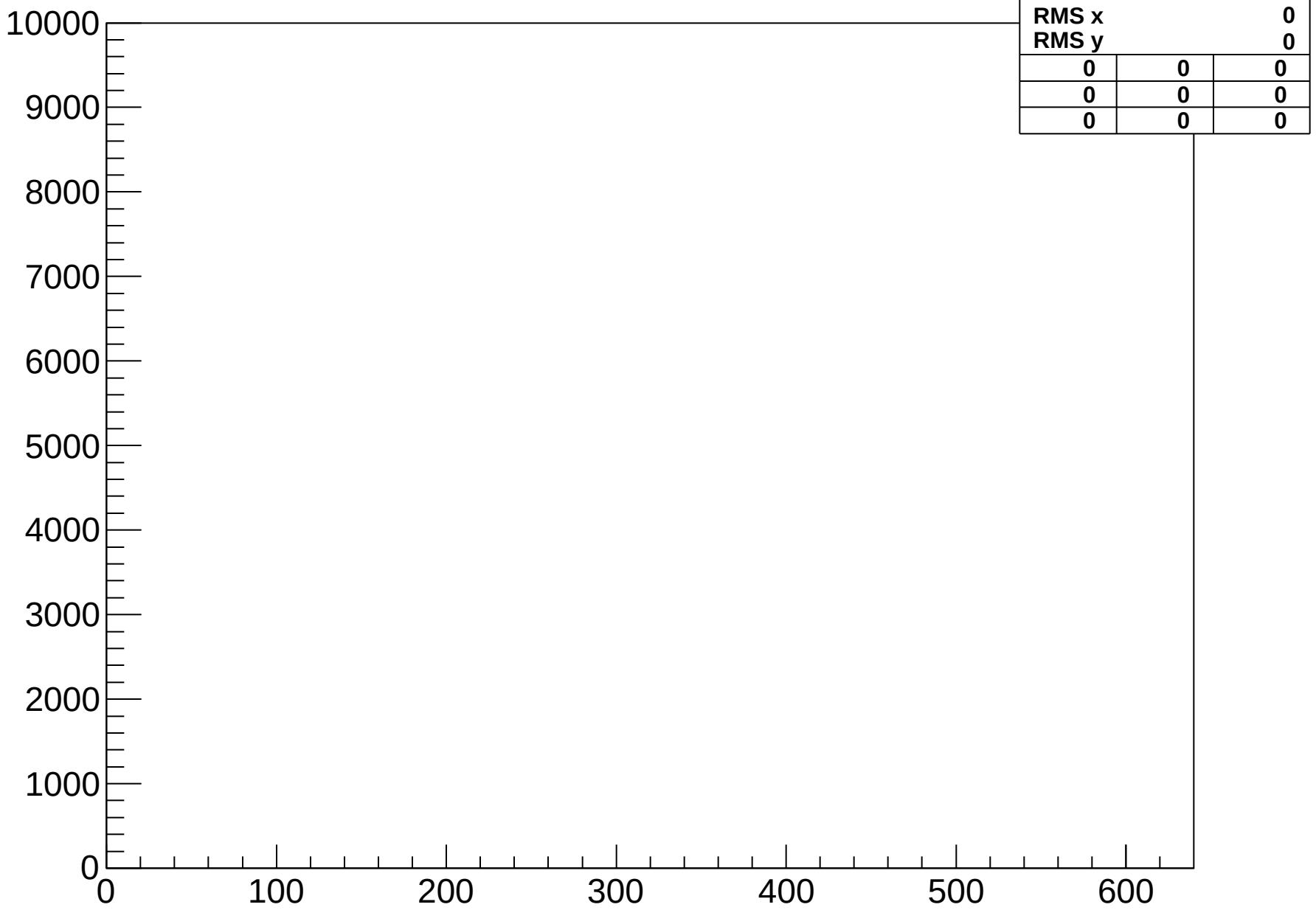



baselinesamples-fpga-2-hyb-0-sample-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

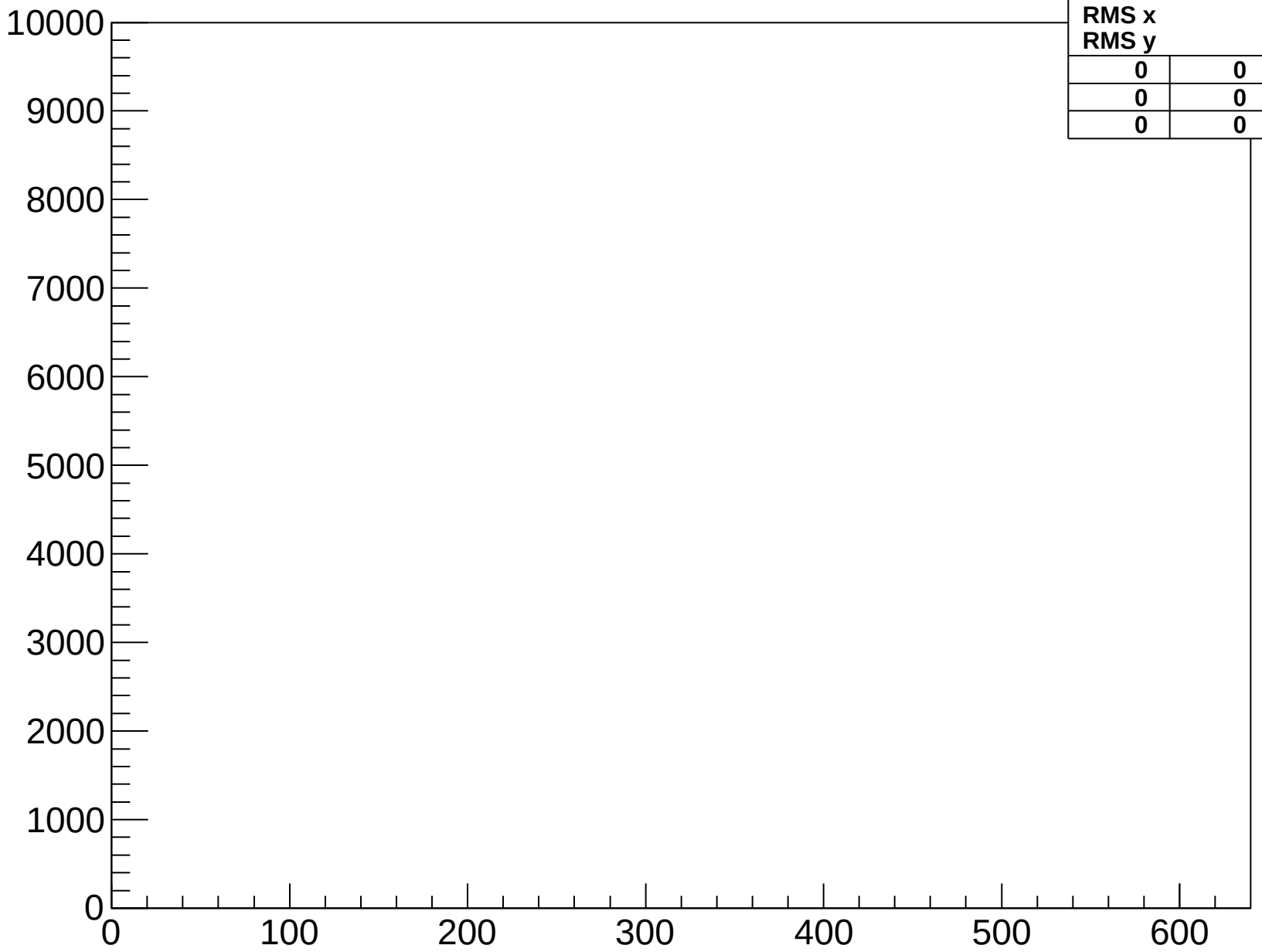
baselinesamples-fpga-2-hyb-0-sample-2



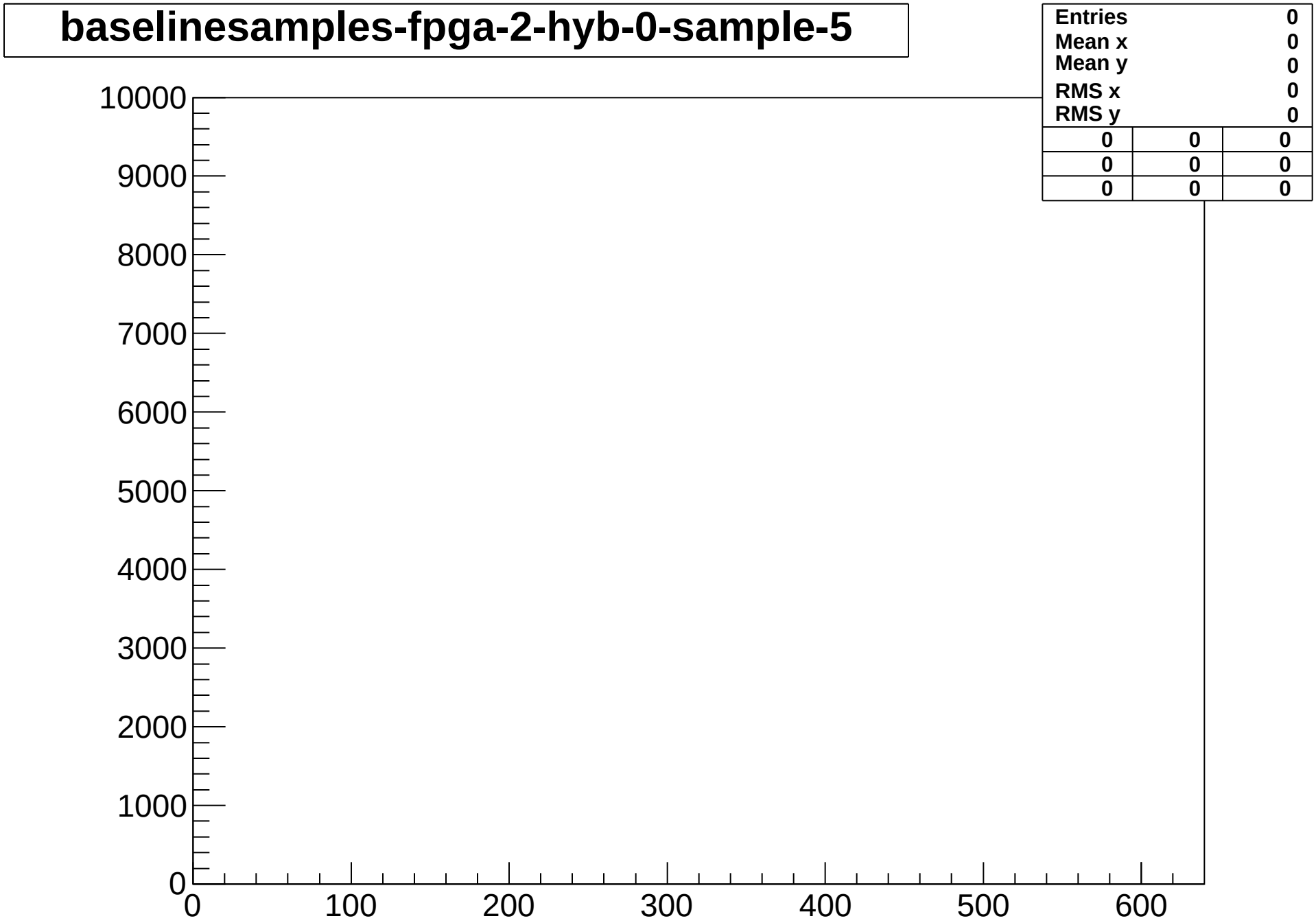
baselinesamples-fpga-2-hyb-0-sample-3

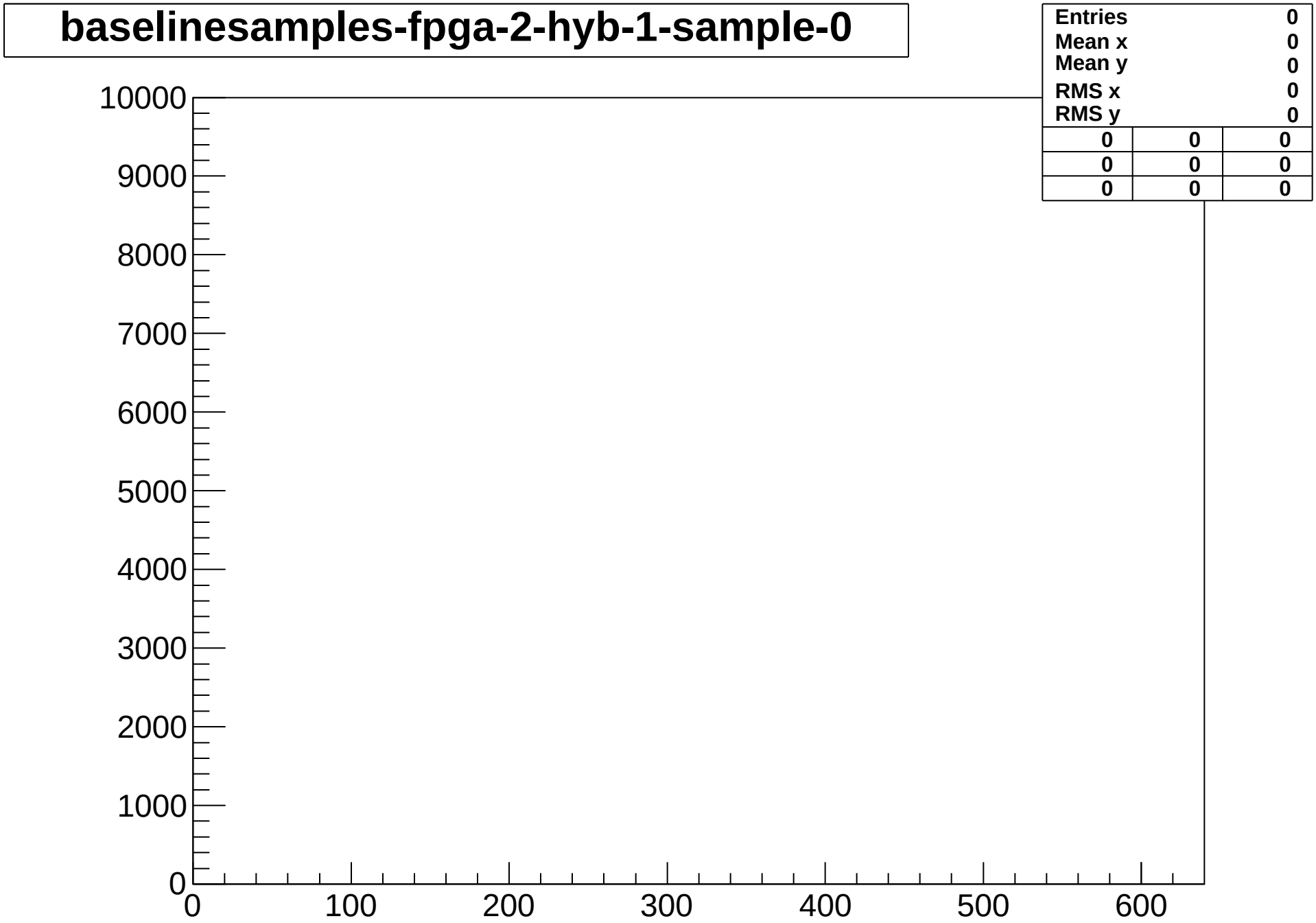


baselinesamples-fpga-2-hyb-0-sample-4

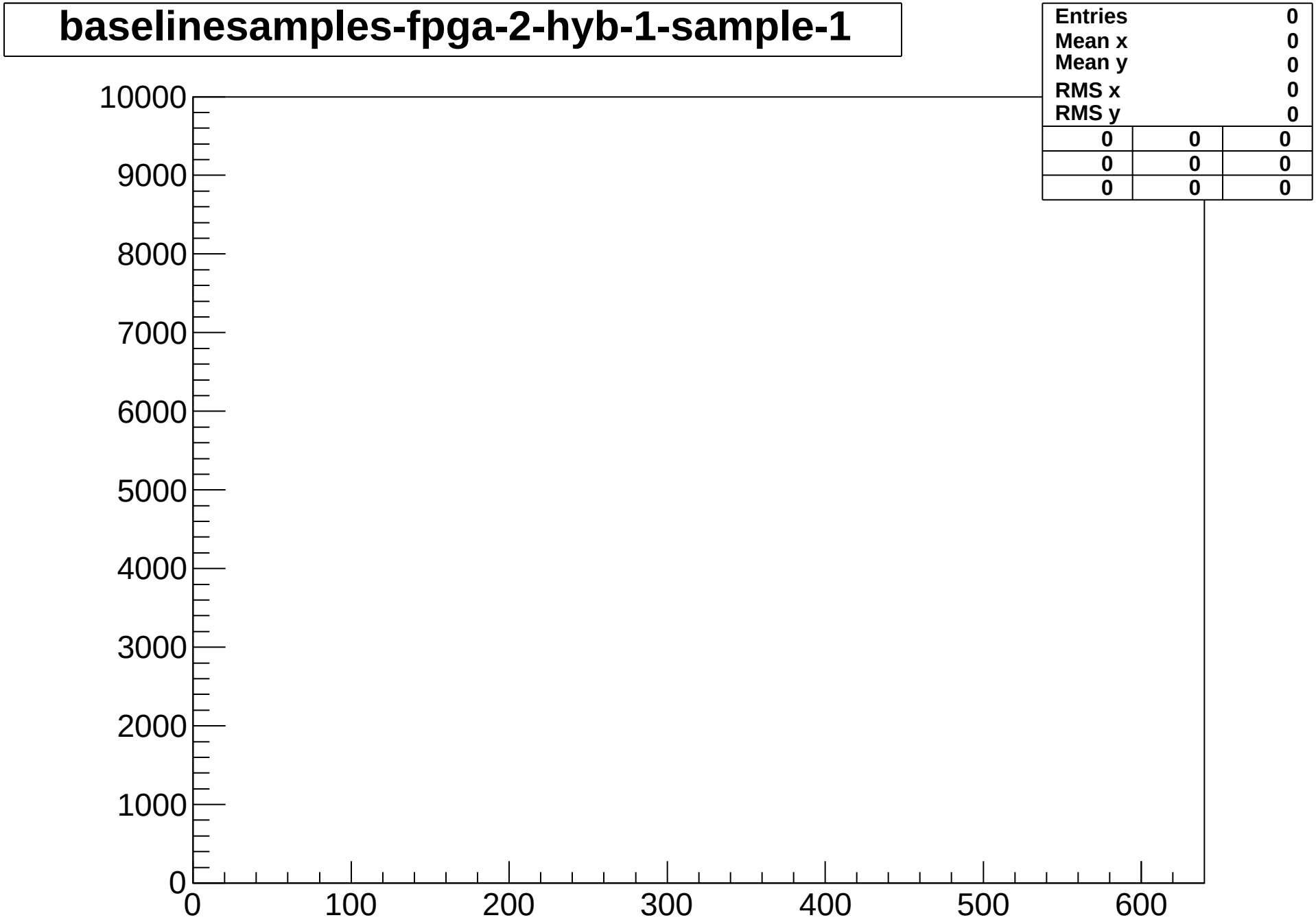


baselinesamples-fpga-2-hyb-0-sample-5

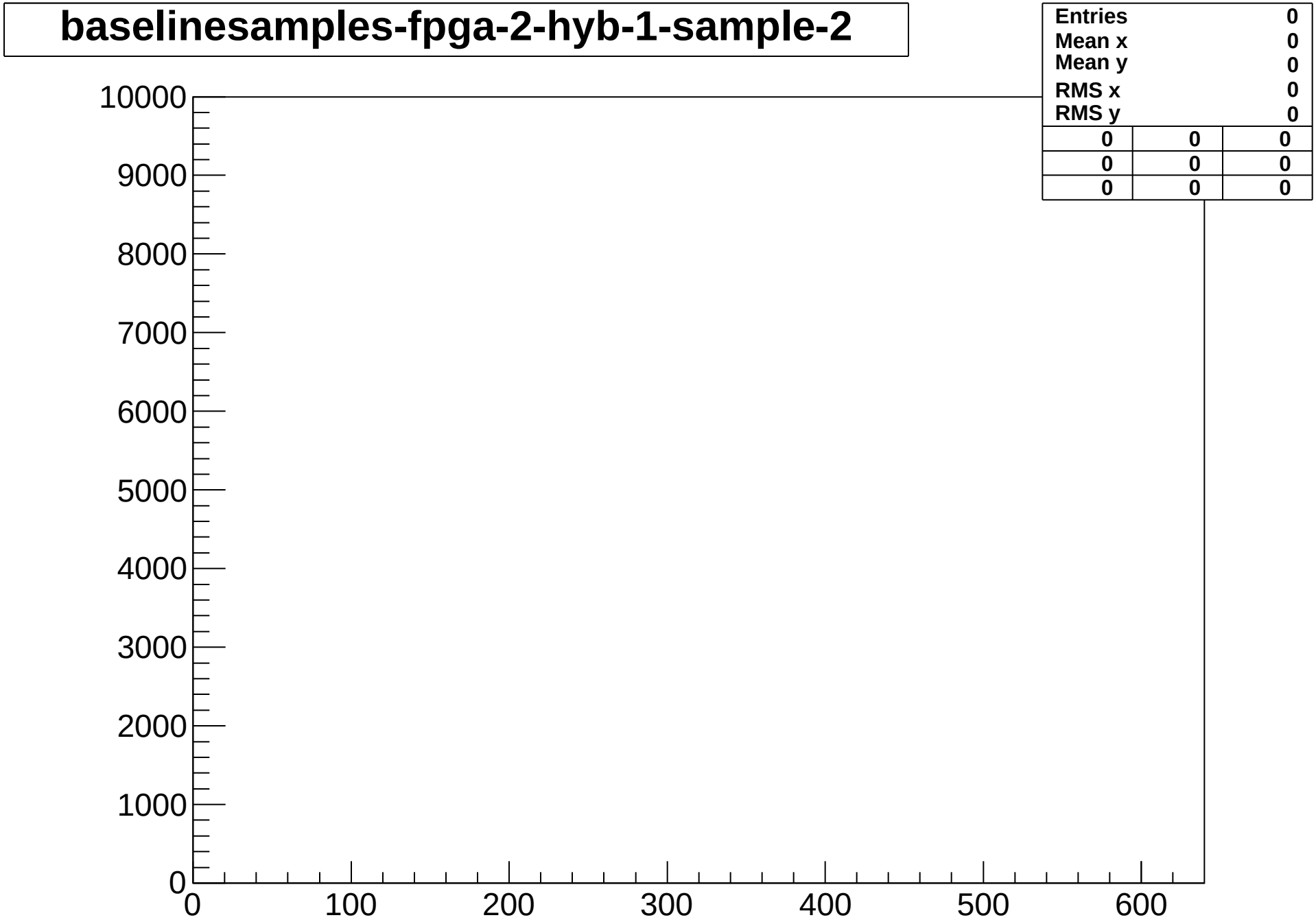



baselinesamples-fpga-2-hyb-1-sample-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

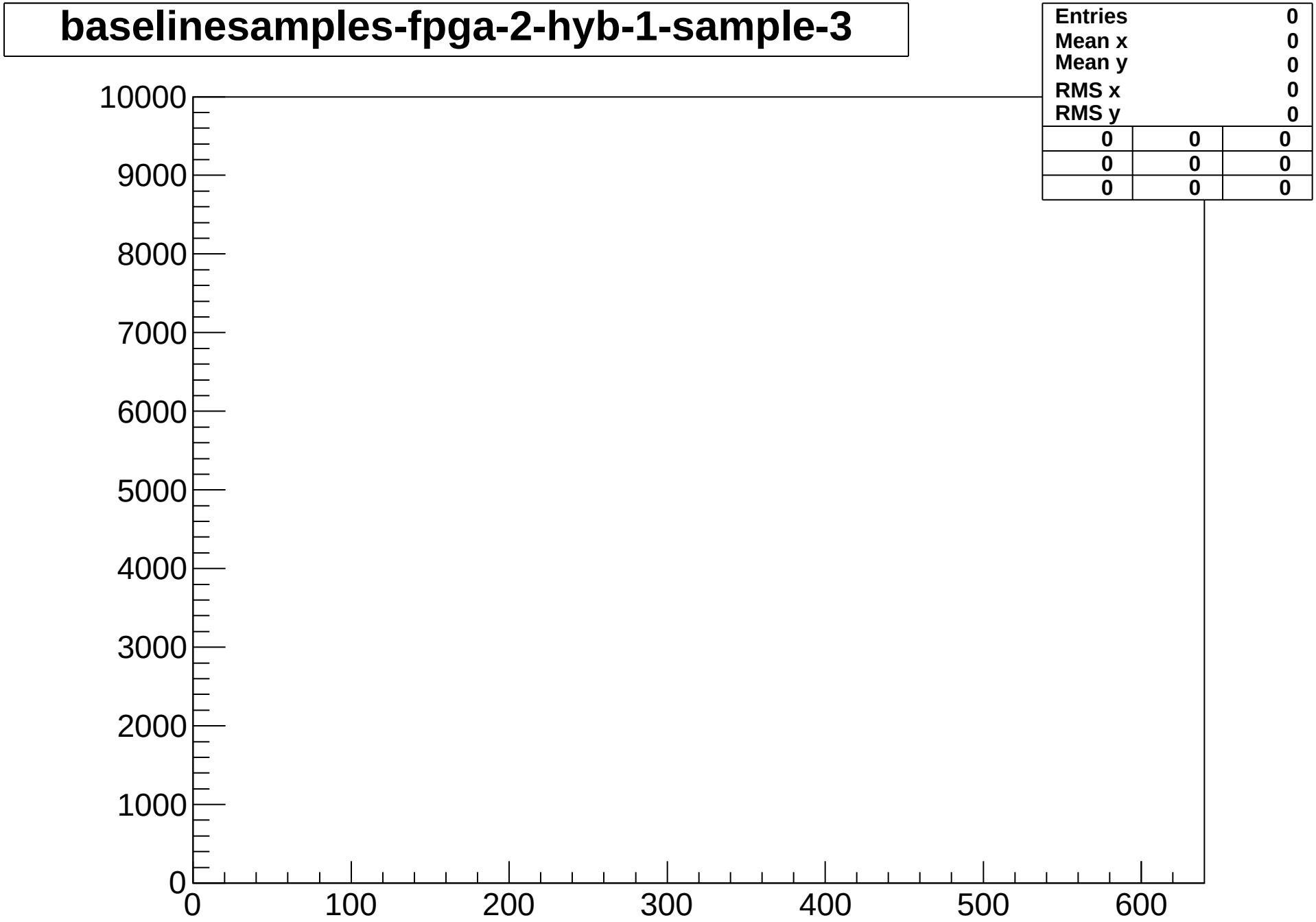
baselinesamples-fpga-2-hyb-1-sample-1



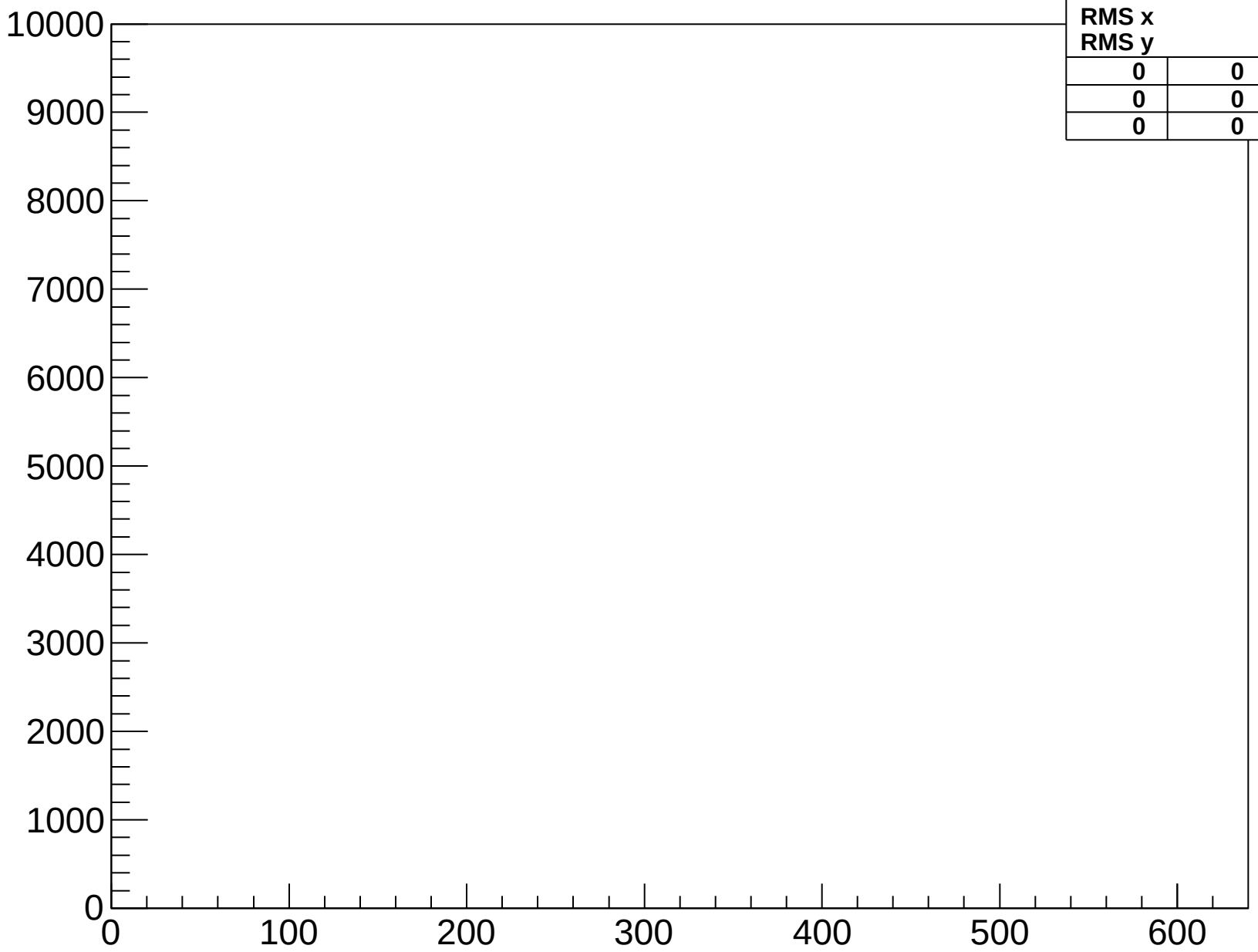
baselinesamples-fpga-2-hyb-1-sample-2



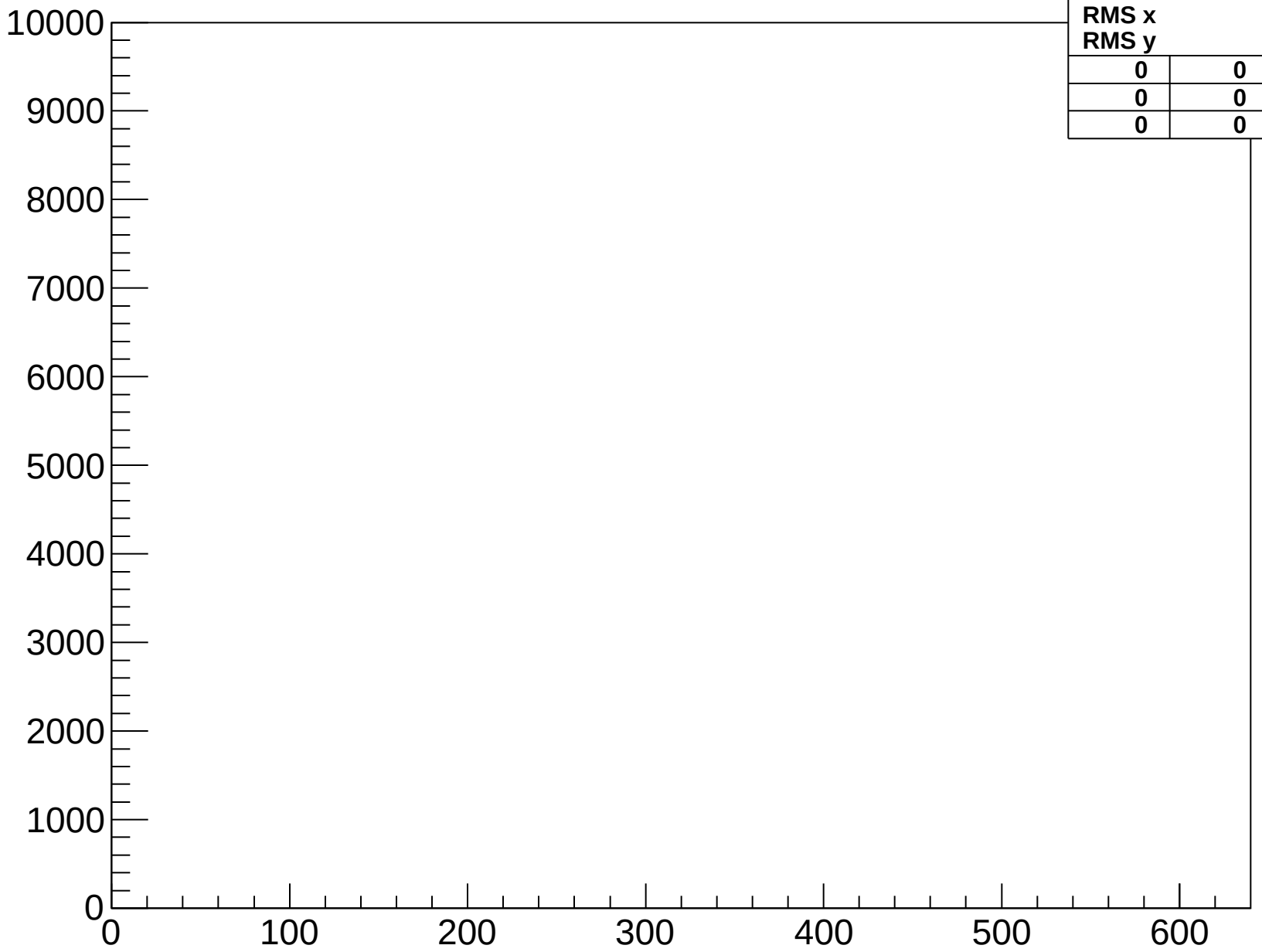
baselinesamples-fpga-2-hyb-1-sample-3



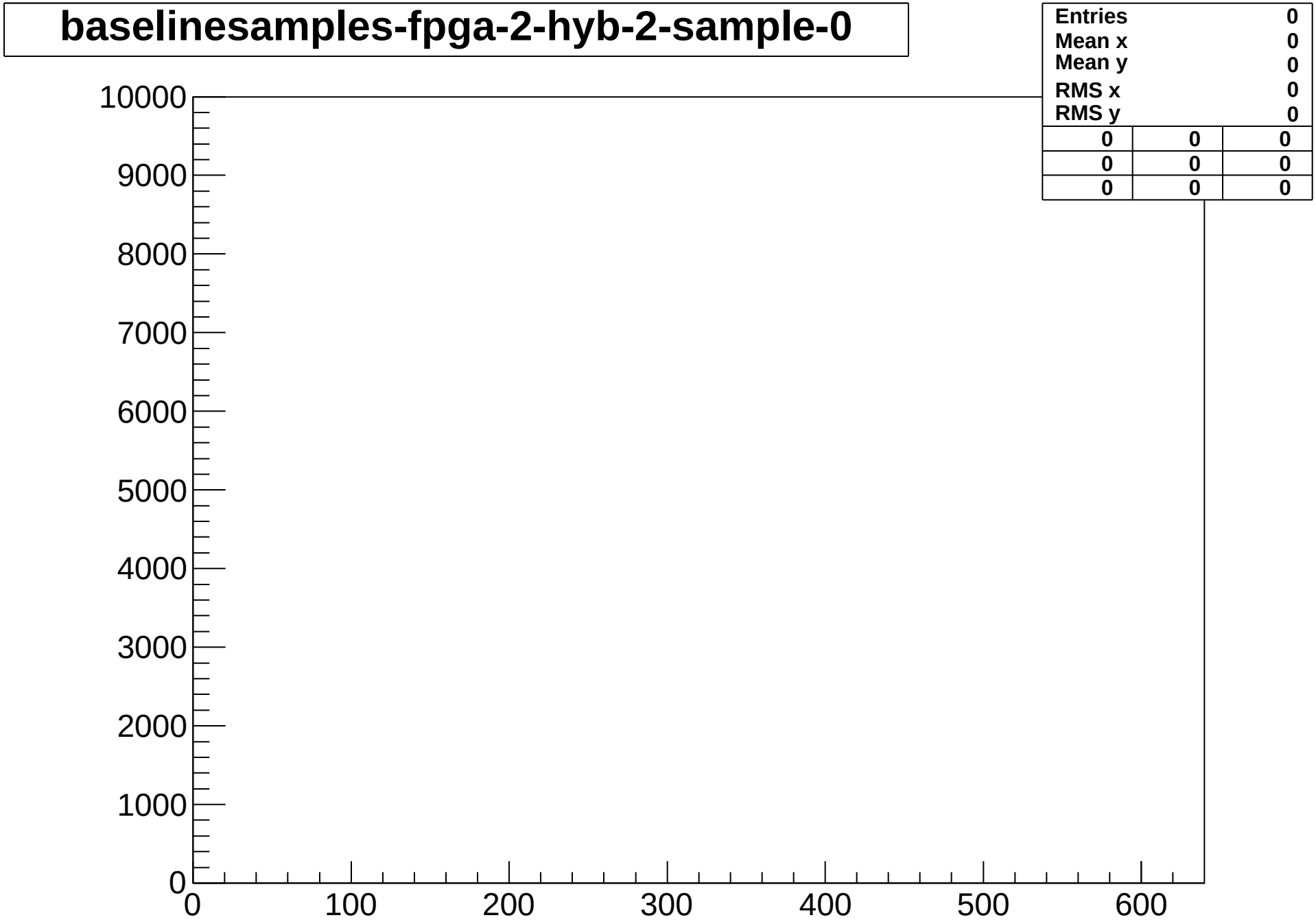
baselinesamples-fpga-2-hyb-1-sample-4



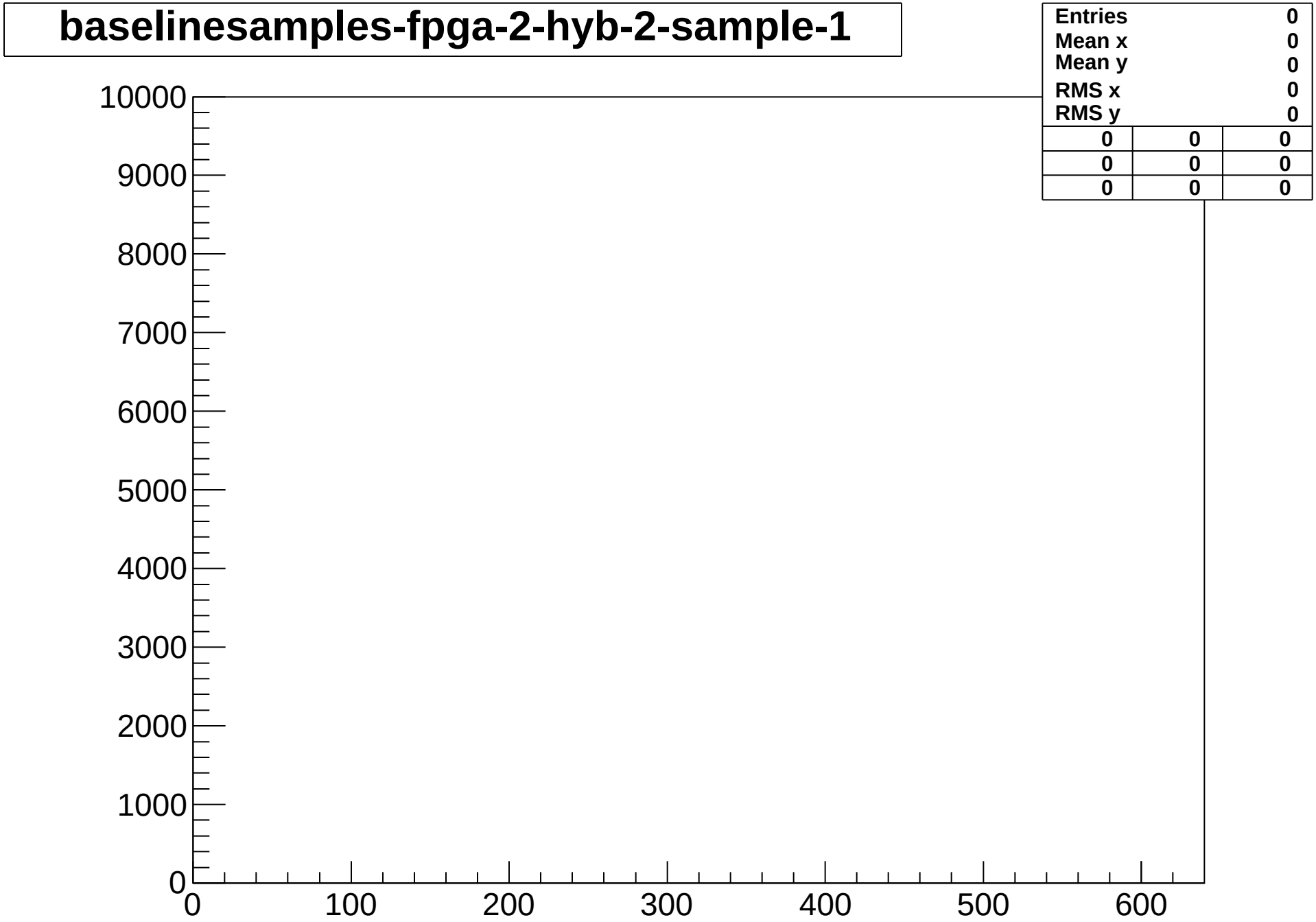
baselinesamples-fpga-2-hyb-1-sample-5



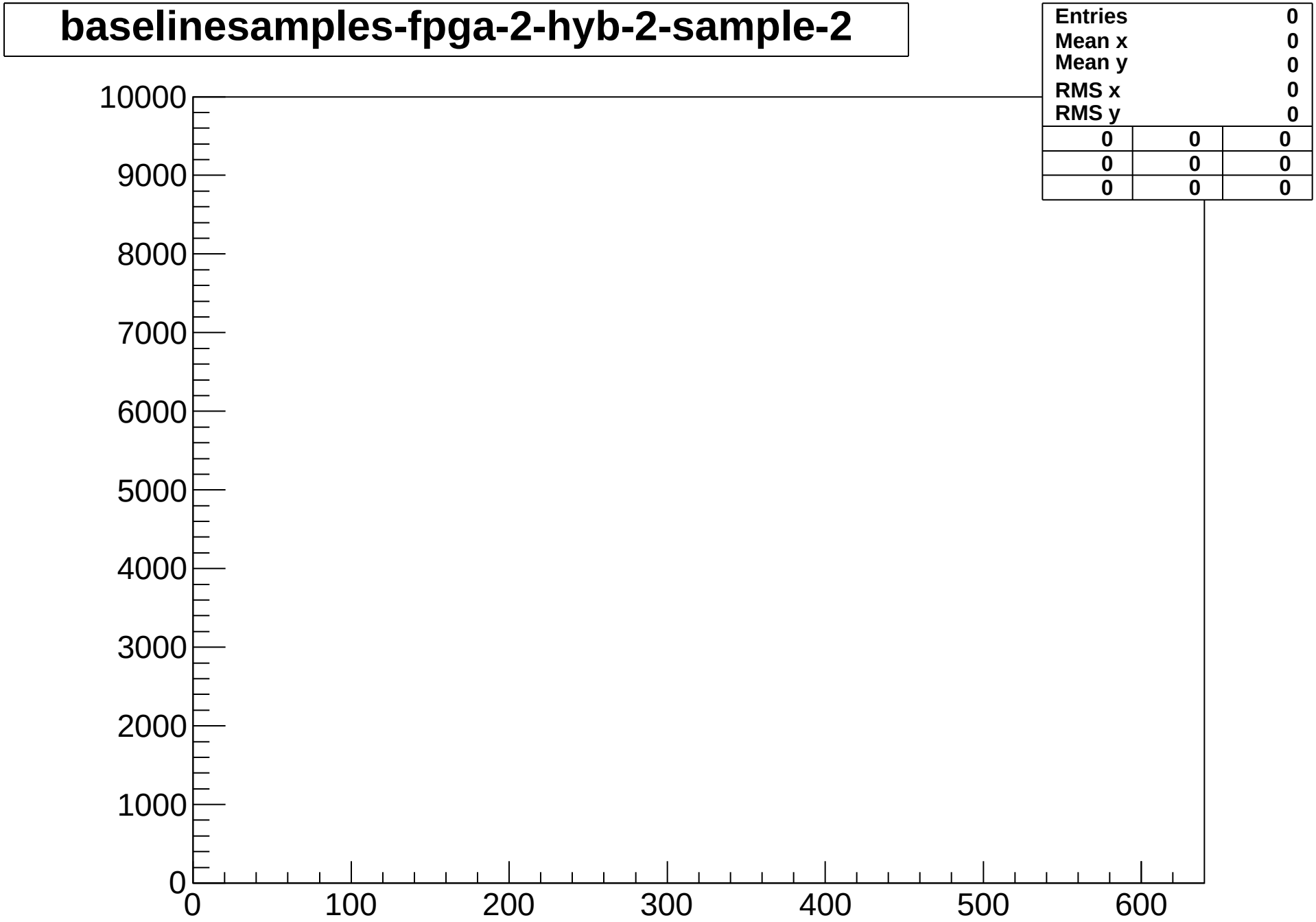
baselinesamples-fpga-2-hyb-2-sample-0



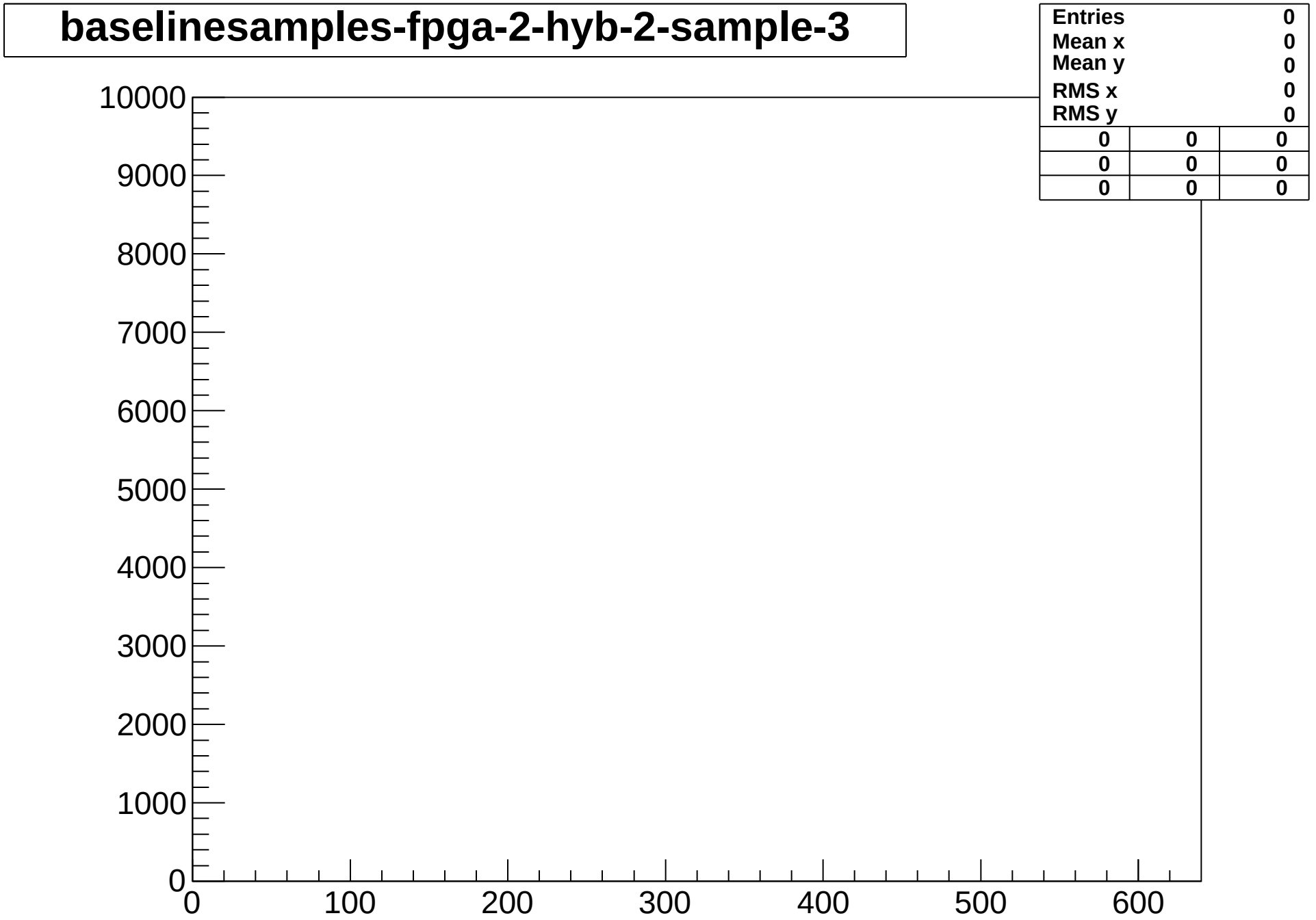
baselinesamples-fpga-2-hyb-2-sample-1



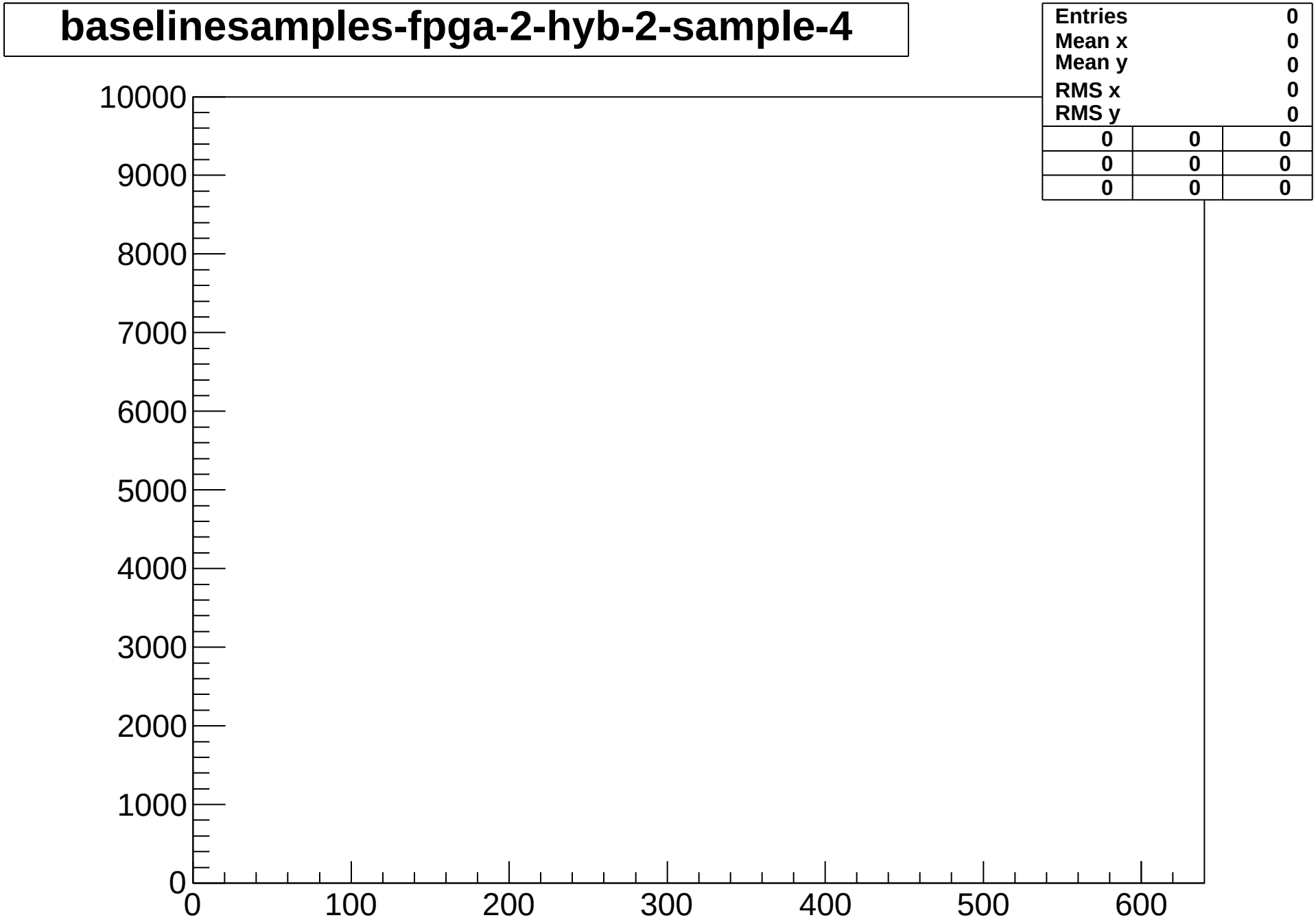
baselinesamples-fpga-2-hyb-2-sample-2



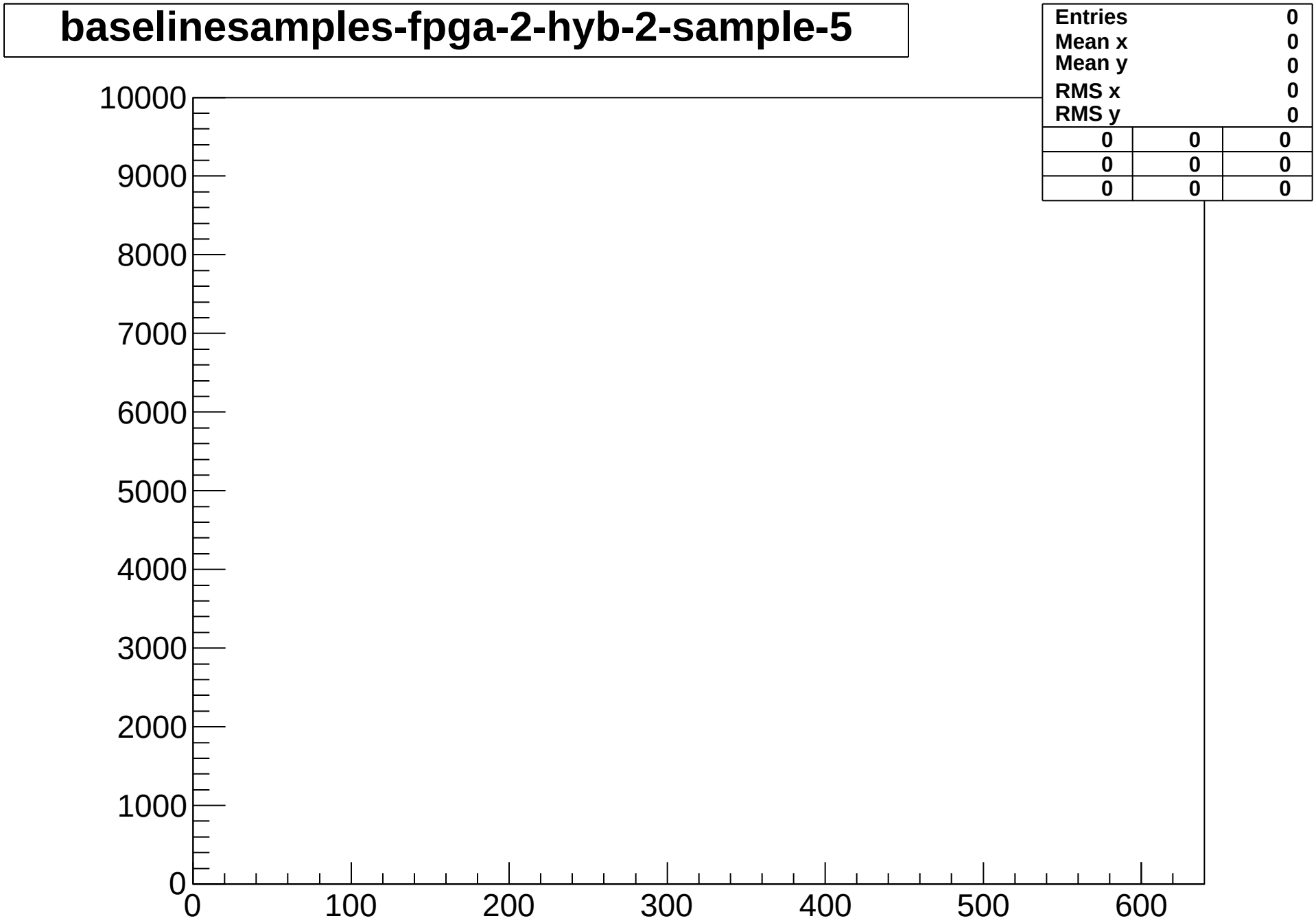
baselinesamples-fpga-2-hyb-2-sample-3



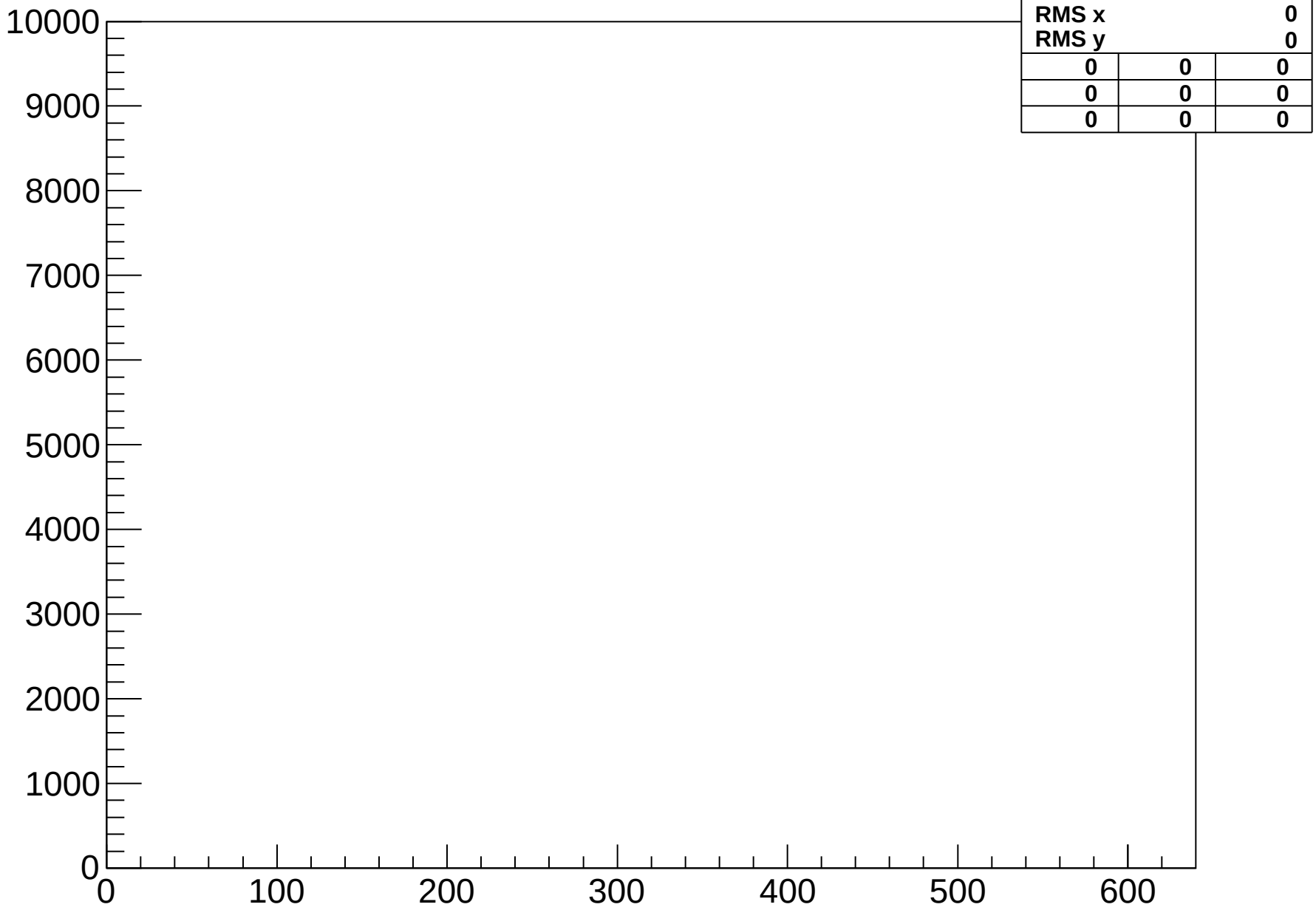
baselinesamples-fpga-2-hyb-2-sample-4



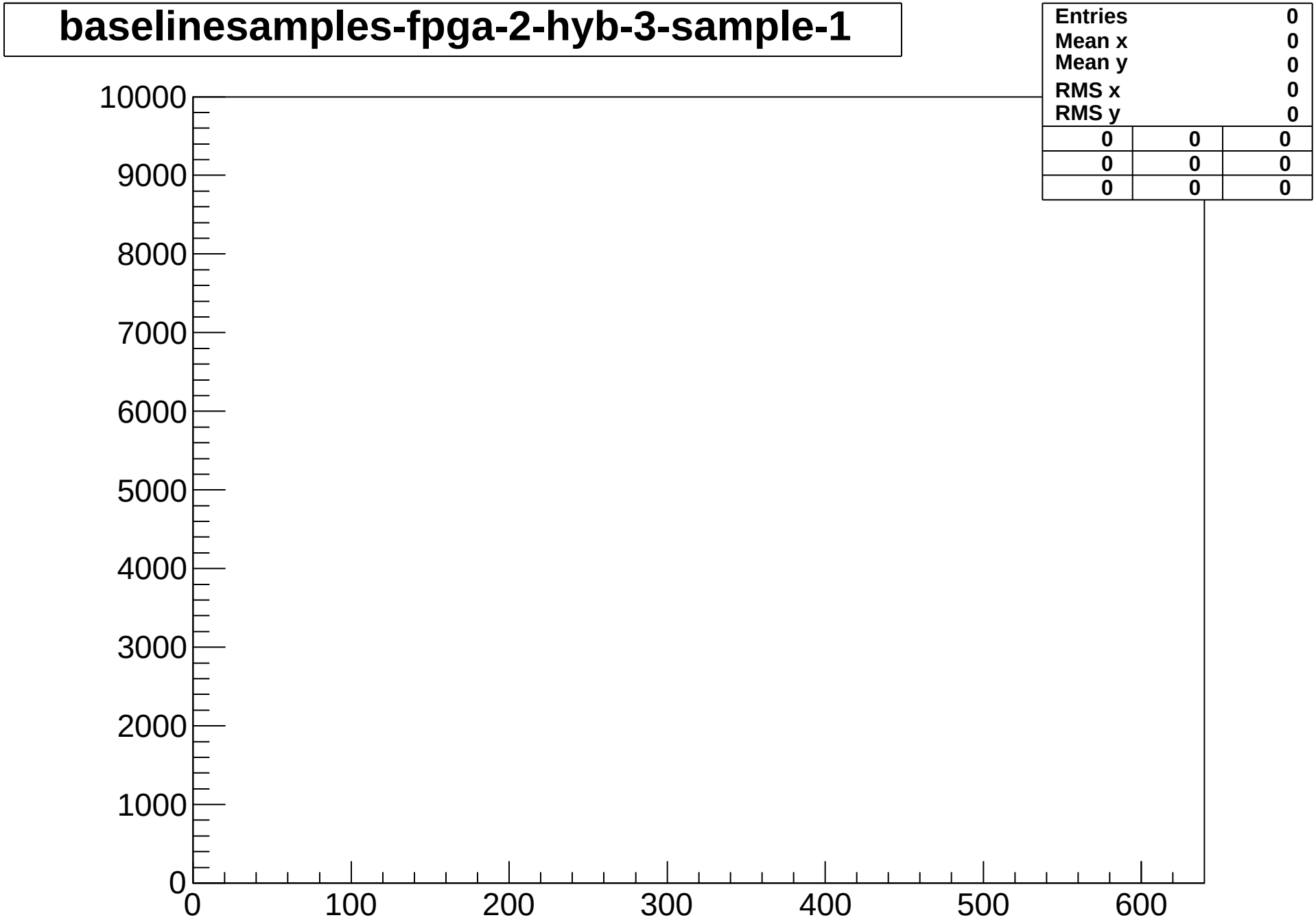
baselinesamples-fpga-2-hyb-2-sample-5



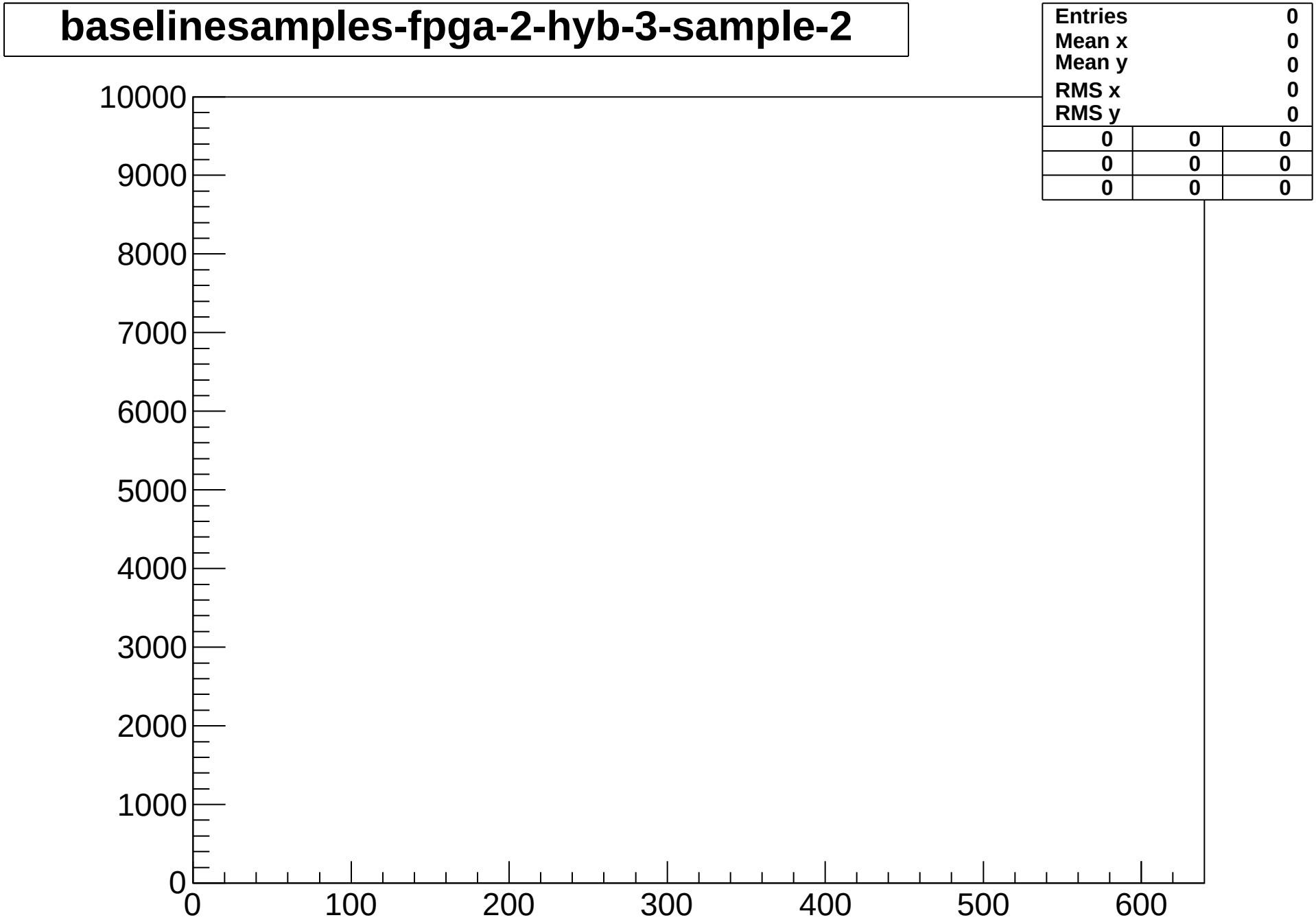
baselinesamples-fpga-2-hyb-3-sample-0



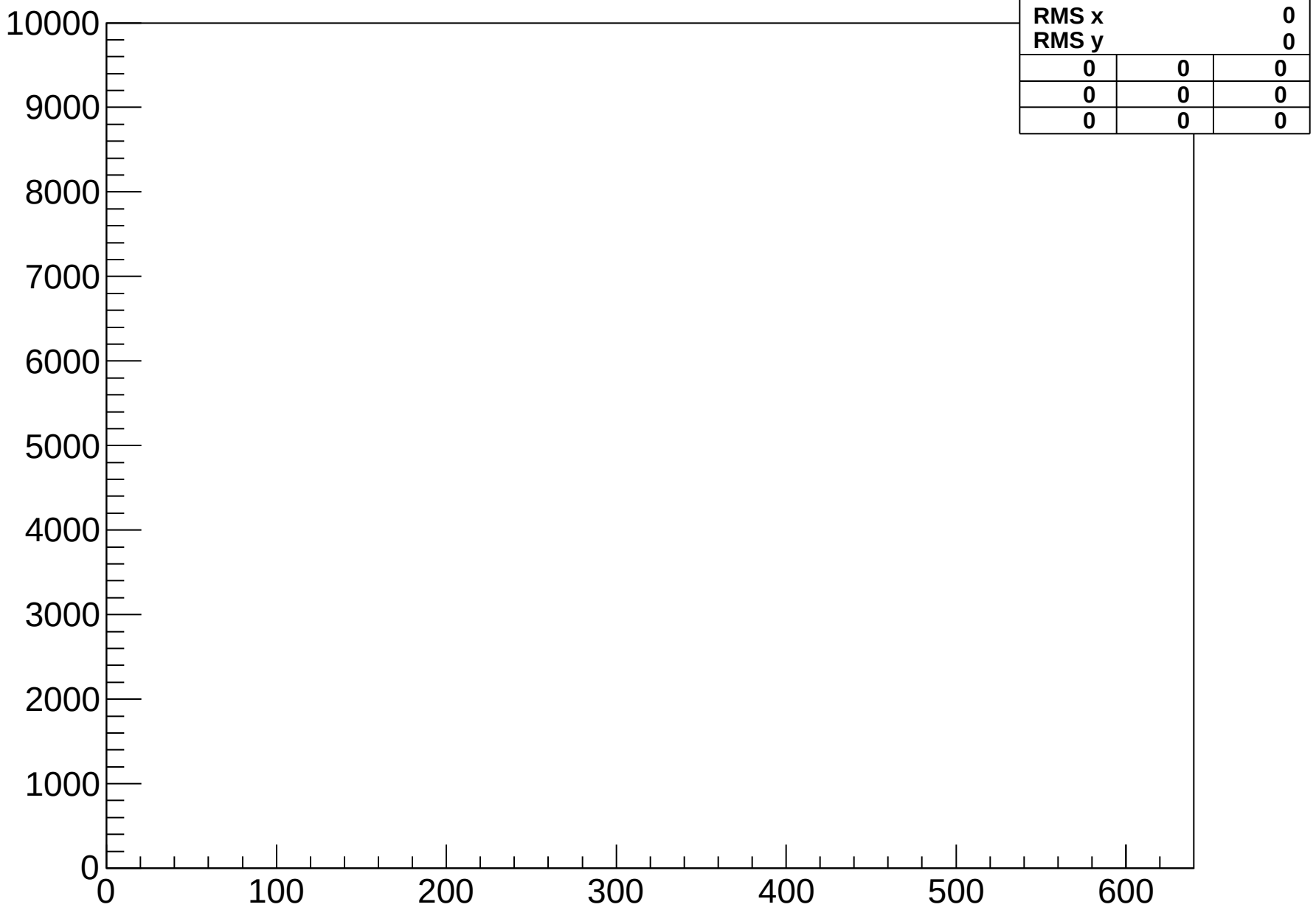
baselinesamples-fpga-2-hyb-3-sample-1



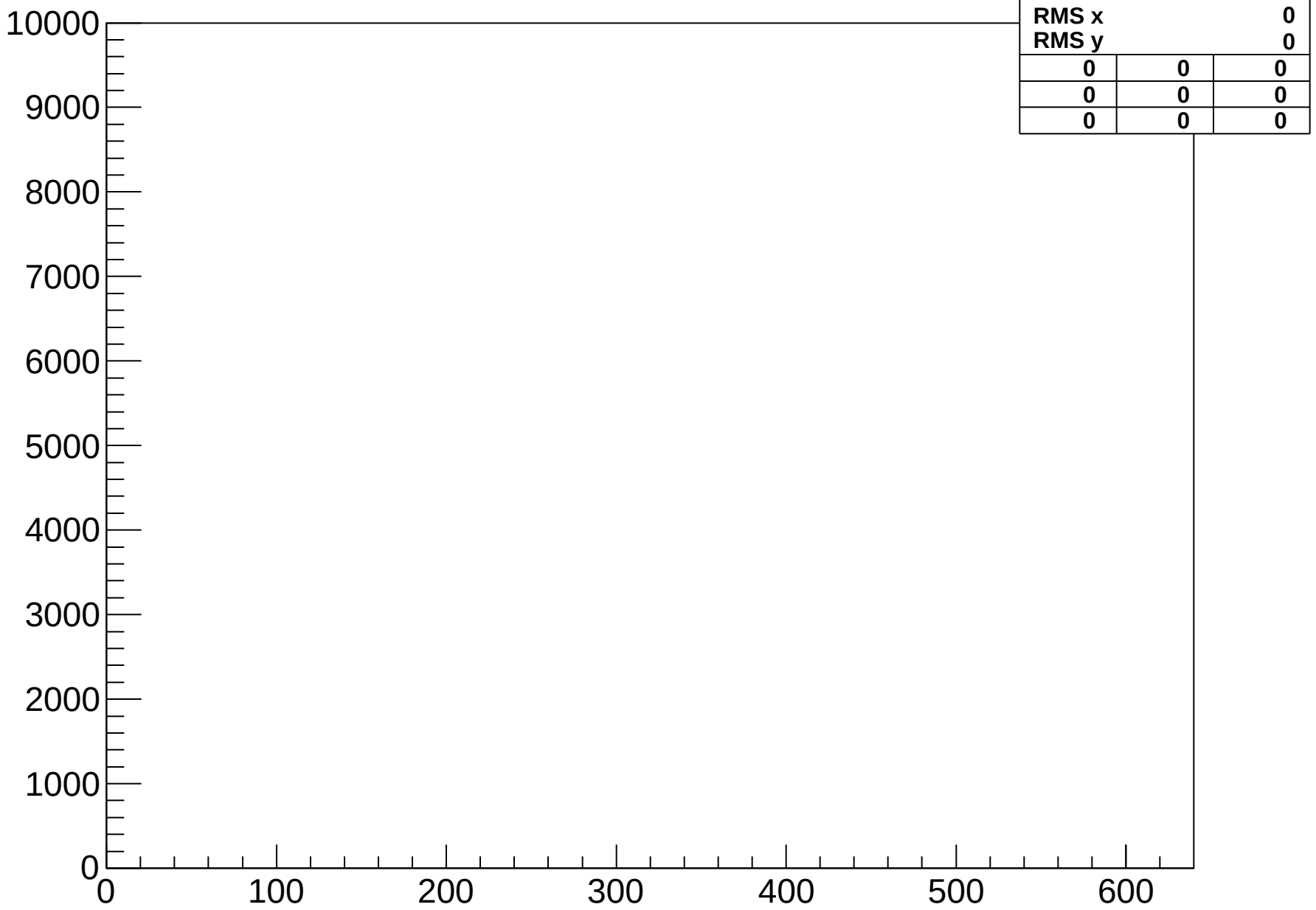
baselinesamples-fpga-2-hyb-3-sample-2



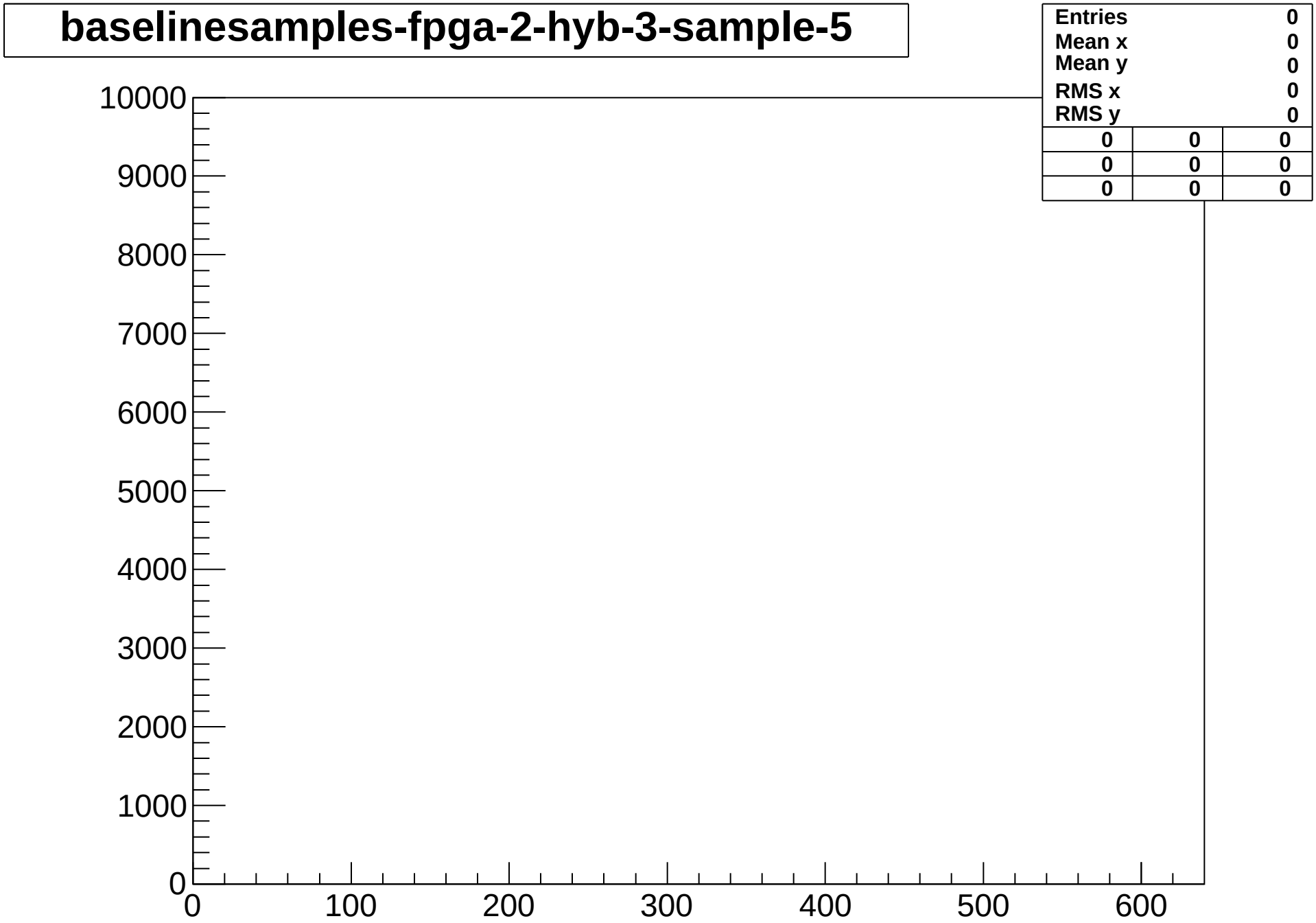
baselinesamples-fpga-2-hyb-3-sample-3



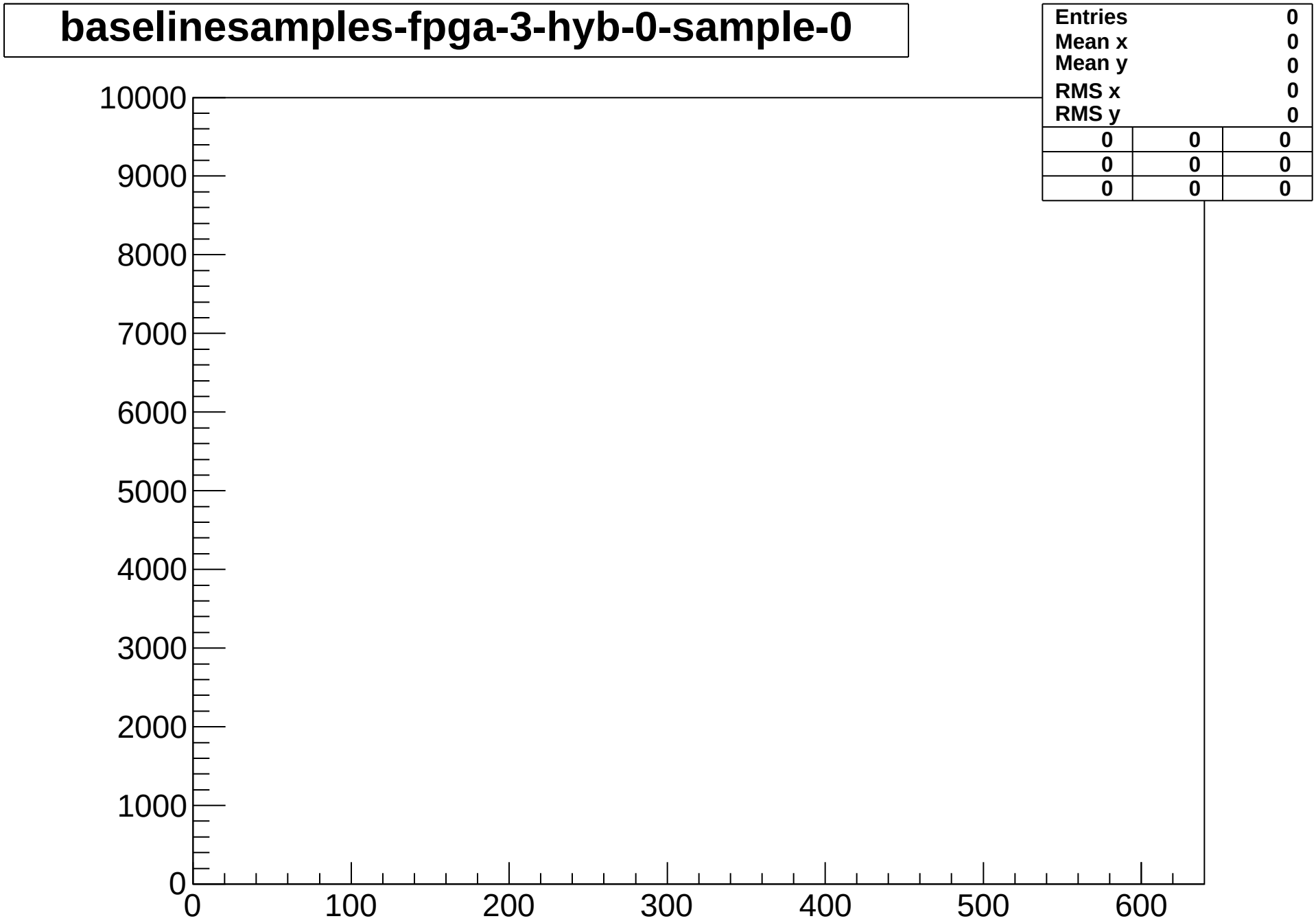
baselinesamples-fpga-2-hyb-3-sample-4

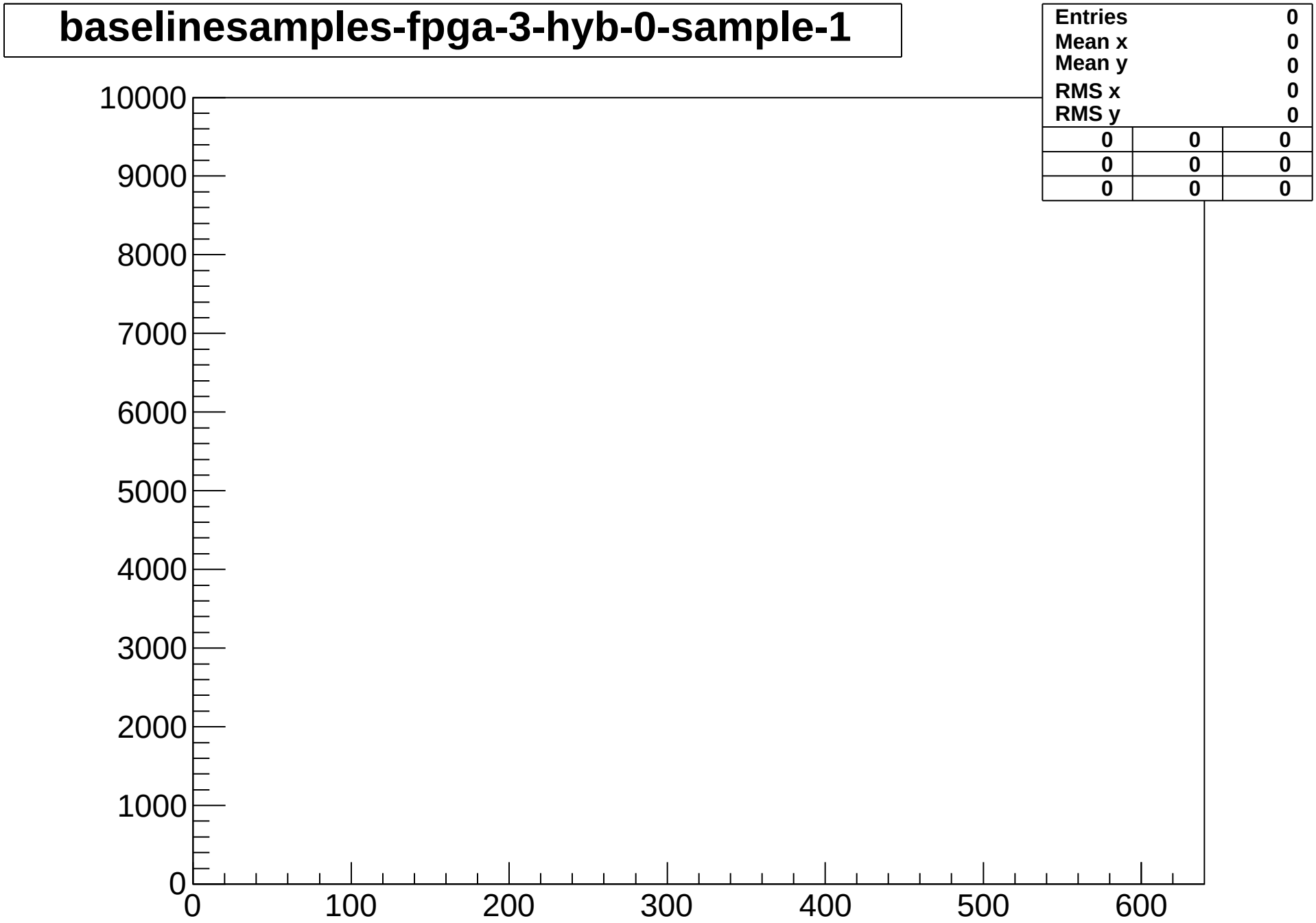


baselinesamples-fpga-2-hyb-3-sample-5

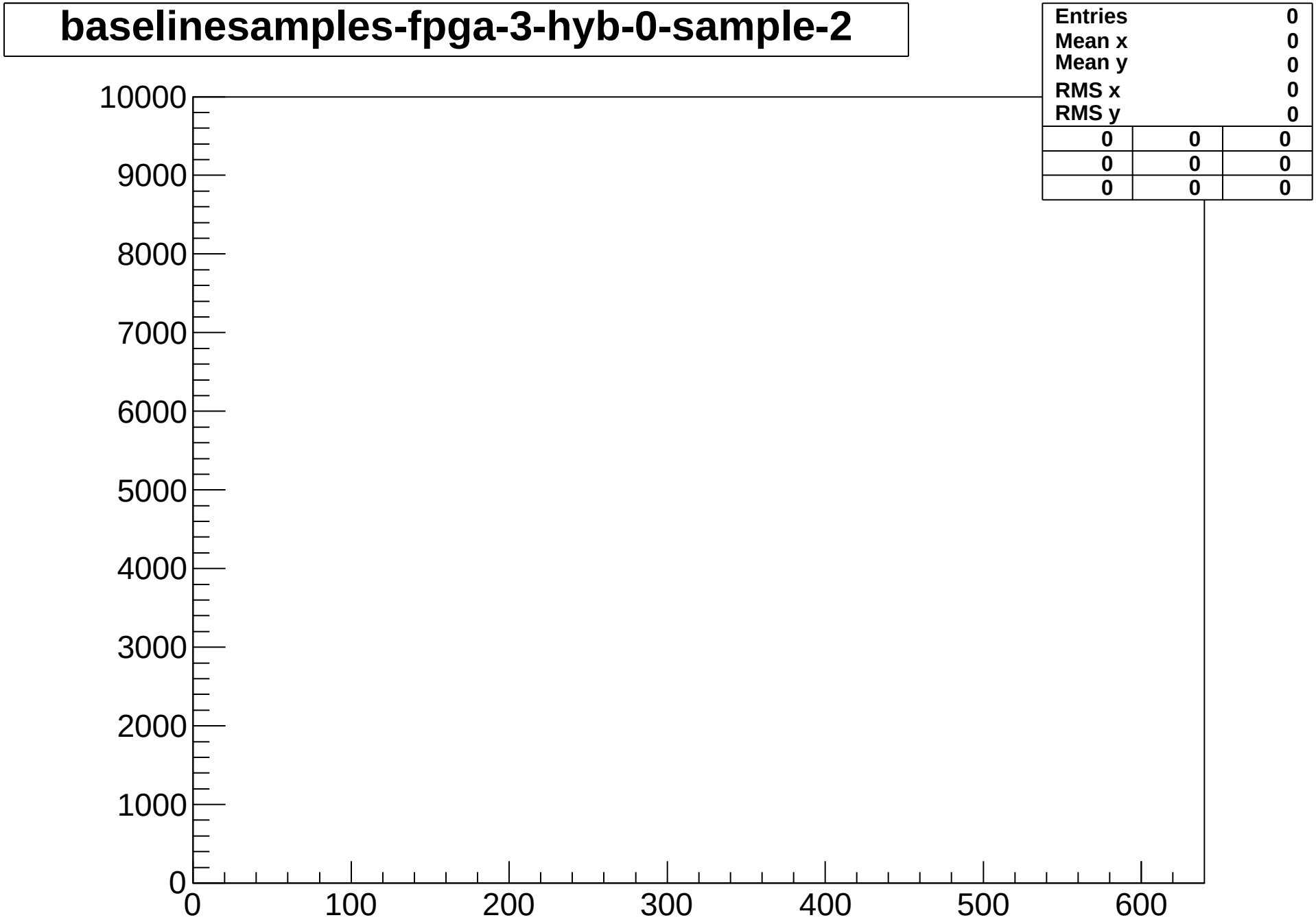


baselinesamples-fpga-3-hyb-0-sample-0

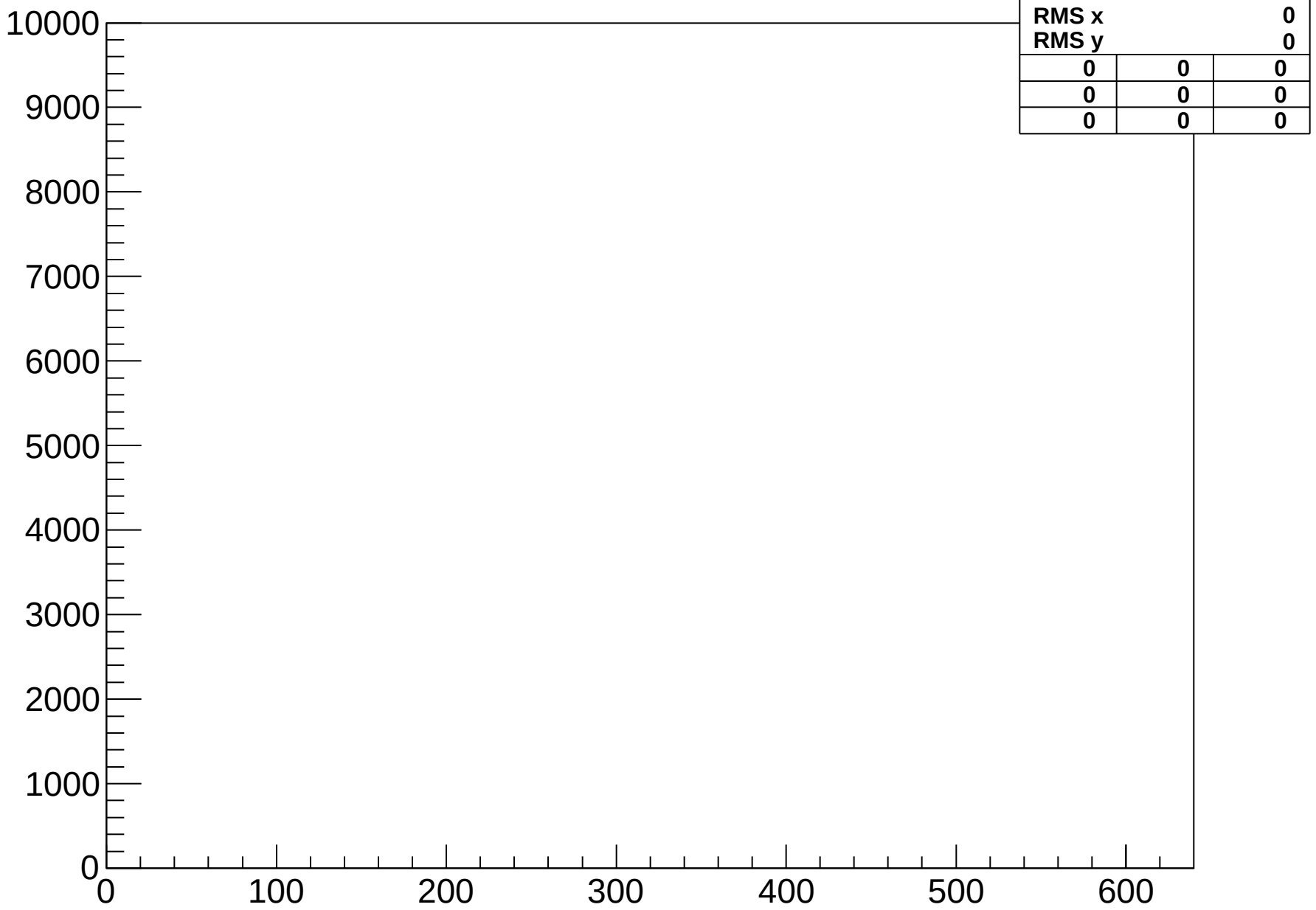



baselinesamples-fpga-3-hyb-0-sample-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

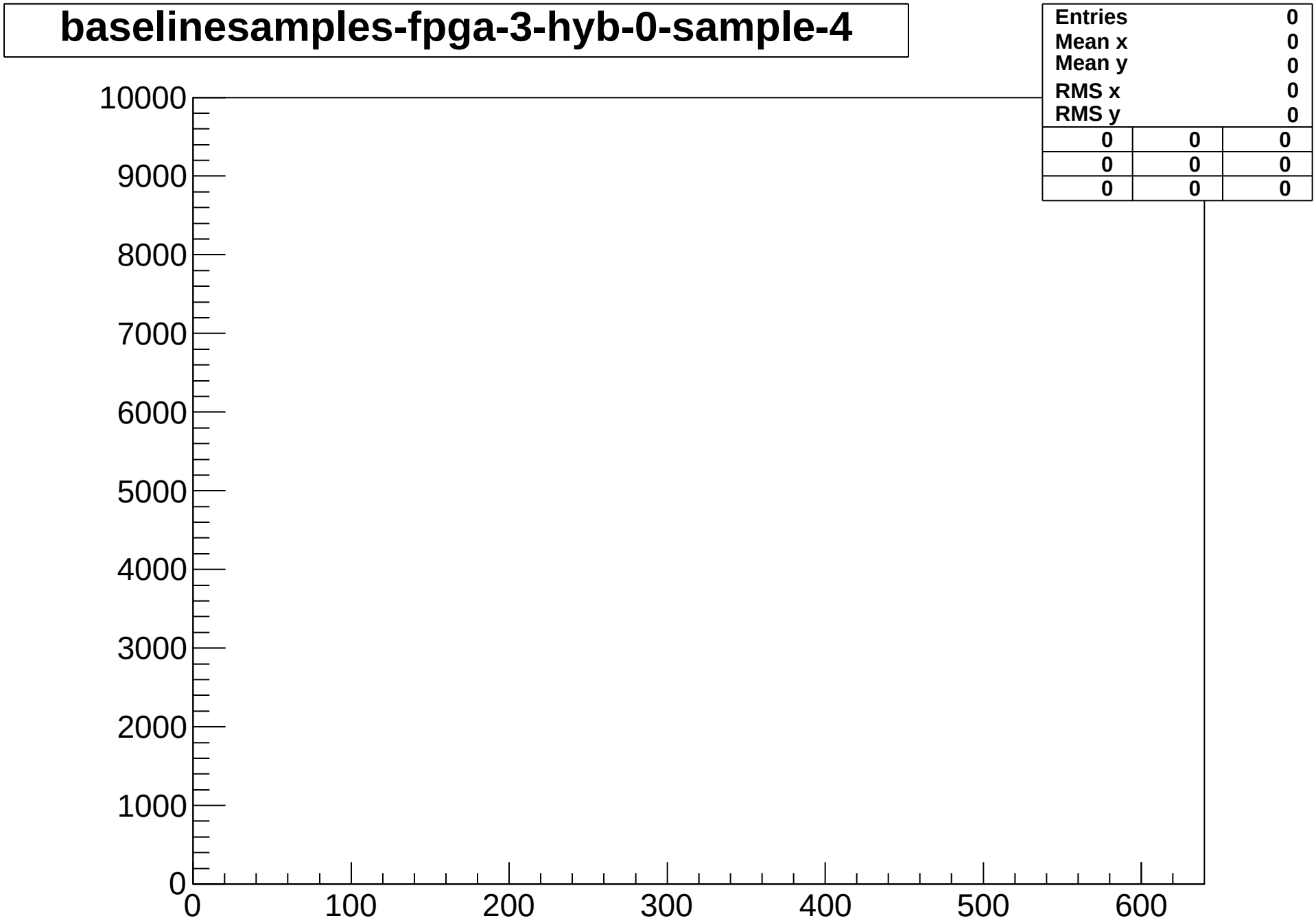
baselinesamples-fpga-3-hyb-0-sample-2



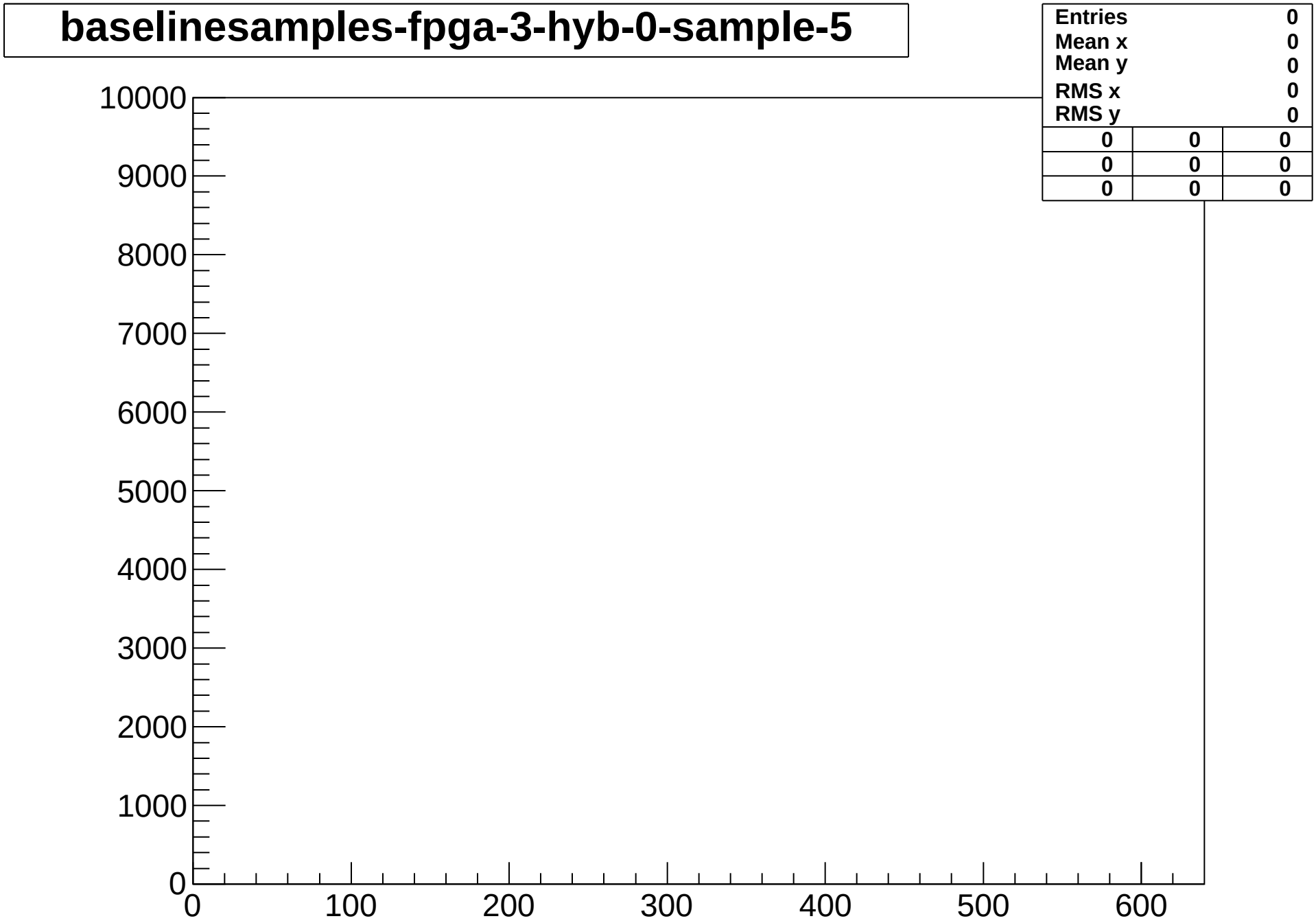
baselinesamples-fpga-3-hyb-0-sample-3



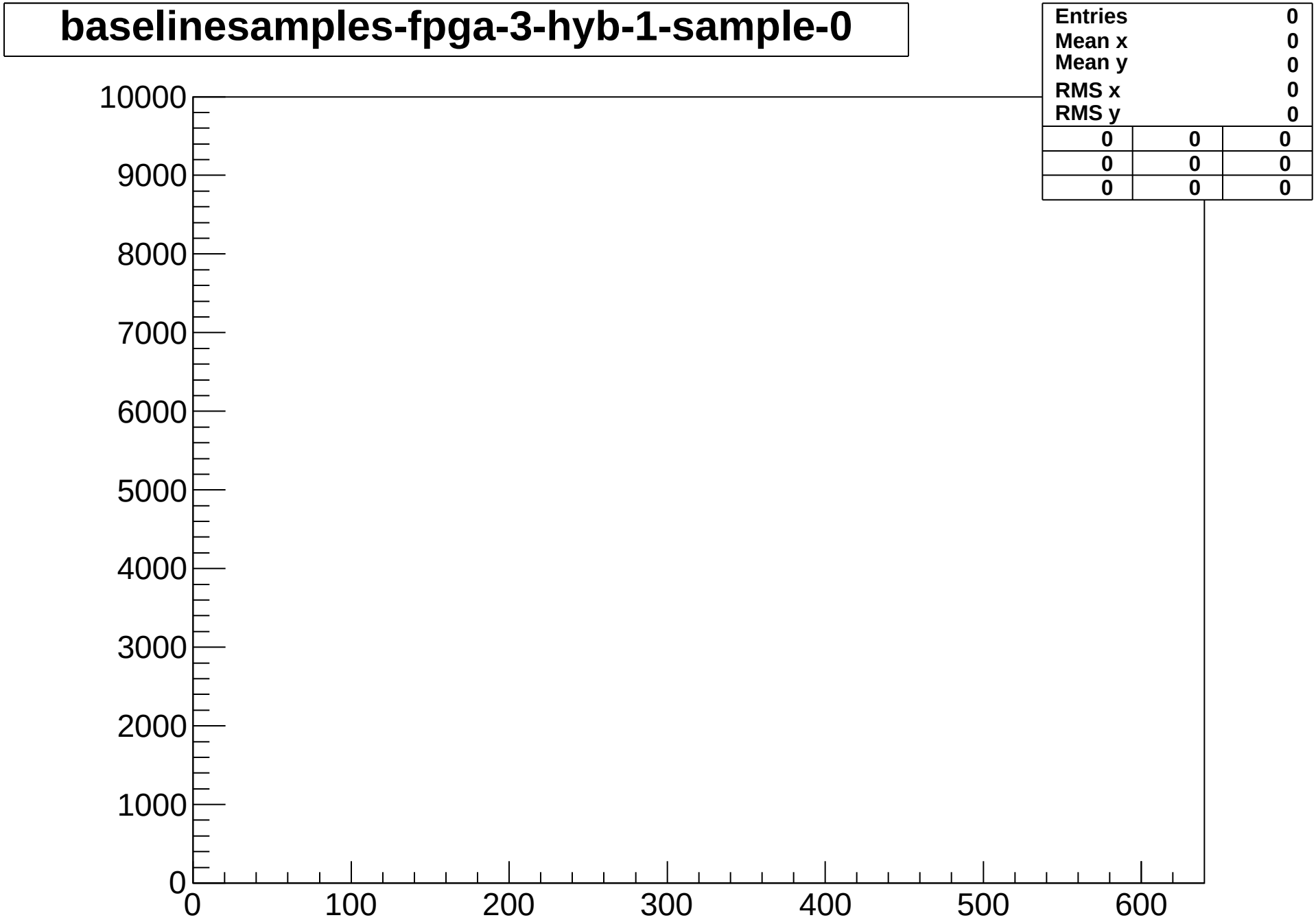
baselinesamples-fpga-3-hyb-0-sample-4



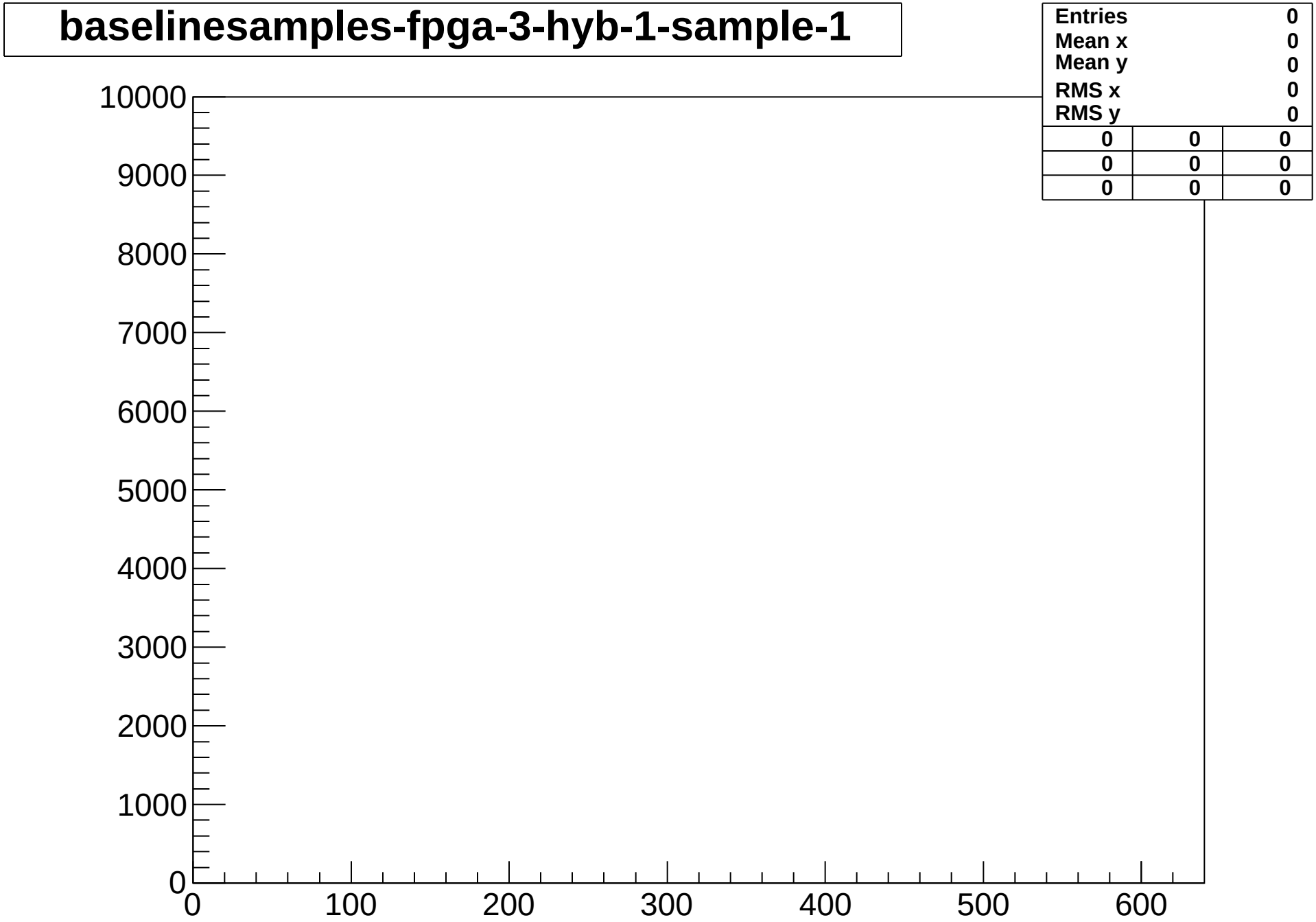
baselinesamples-fpga-3-hyb-0-sample-5



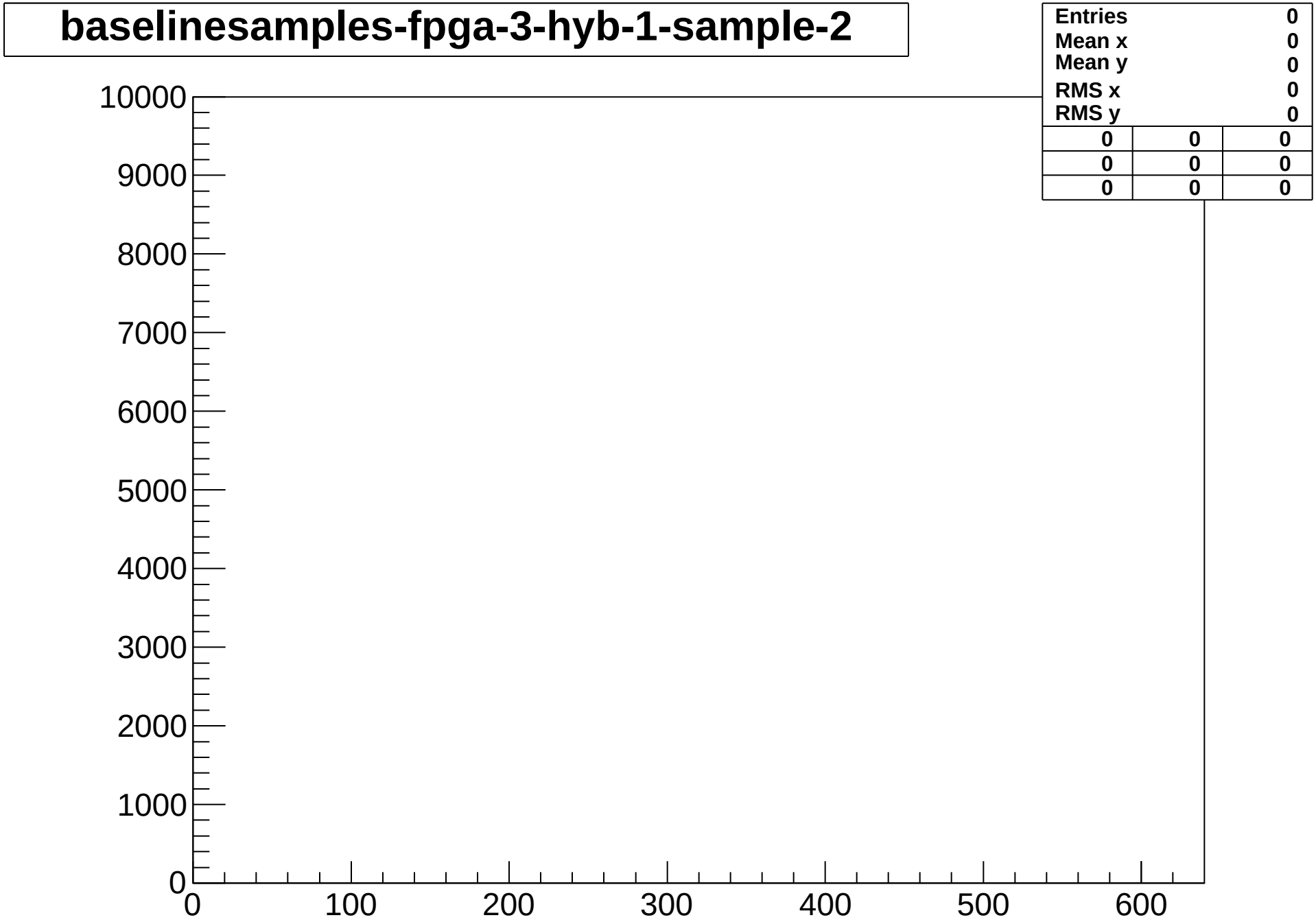
baselinesamples-fpga-3-hyb-1-sample-0



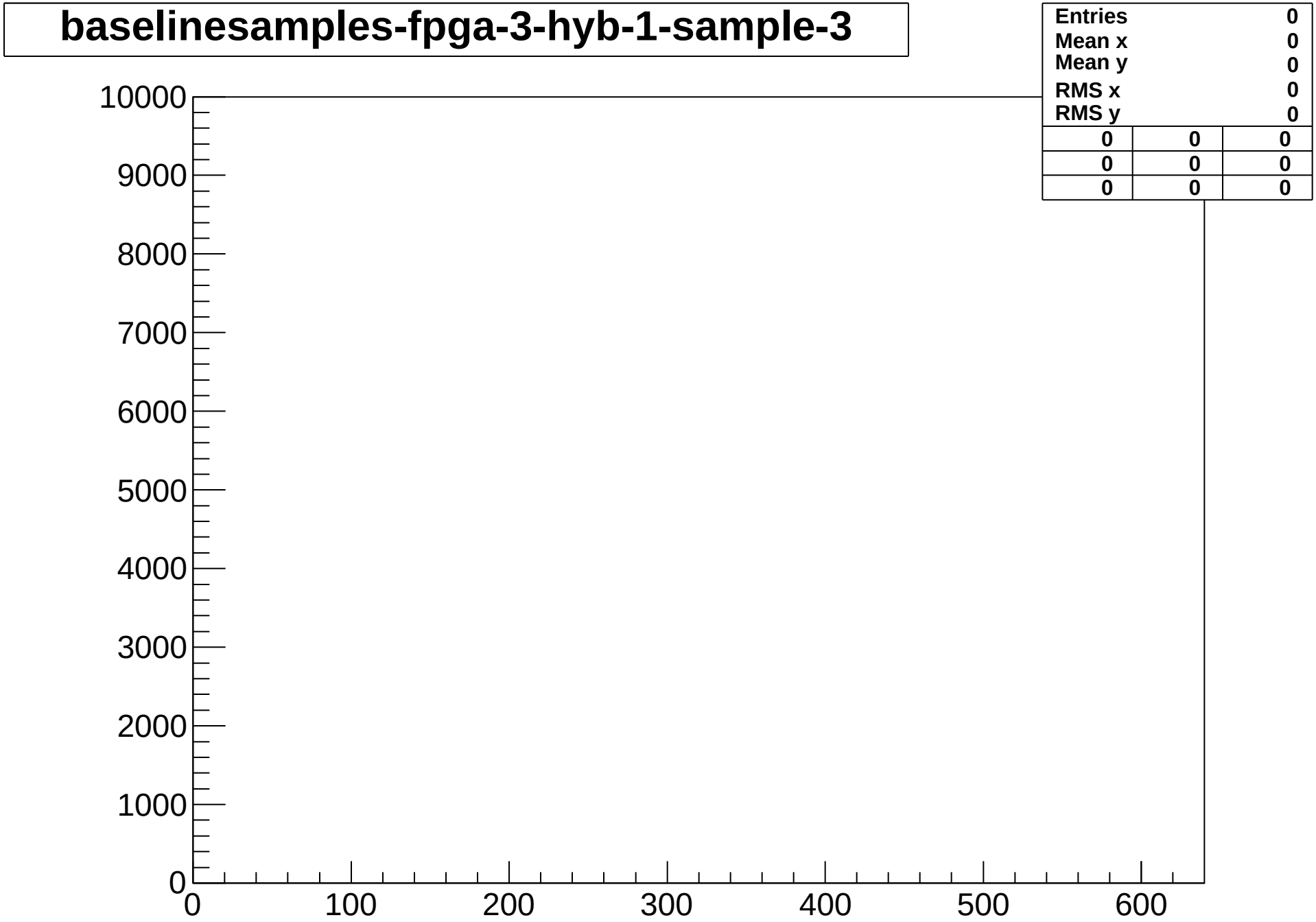
baselinesamples-fpga-3-hyb-1-sample-1



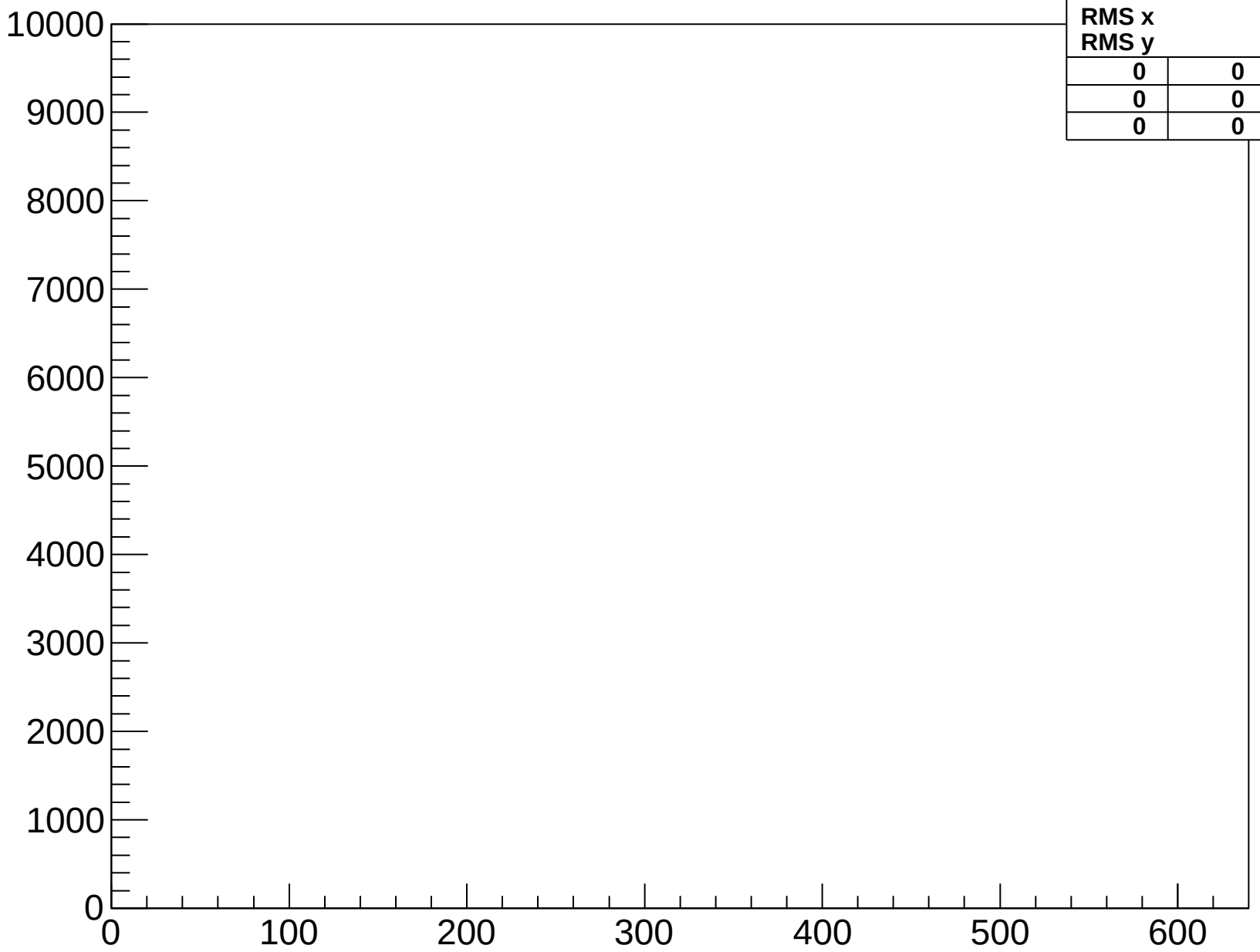
baselinesamples-fpga-3-hyb-1-sample-2



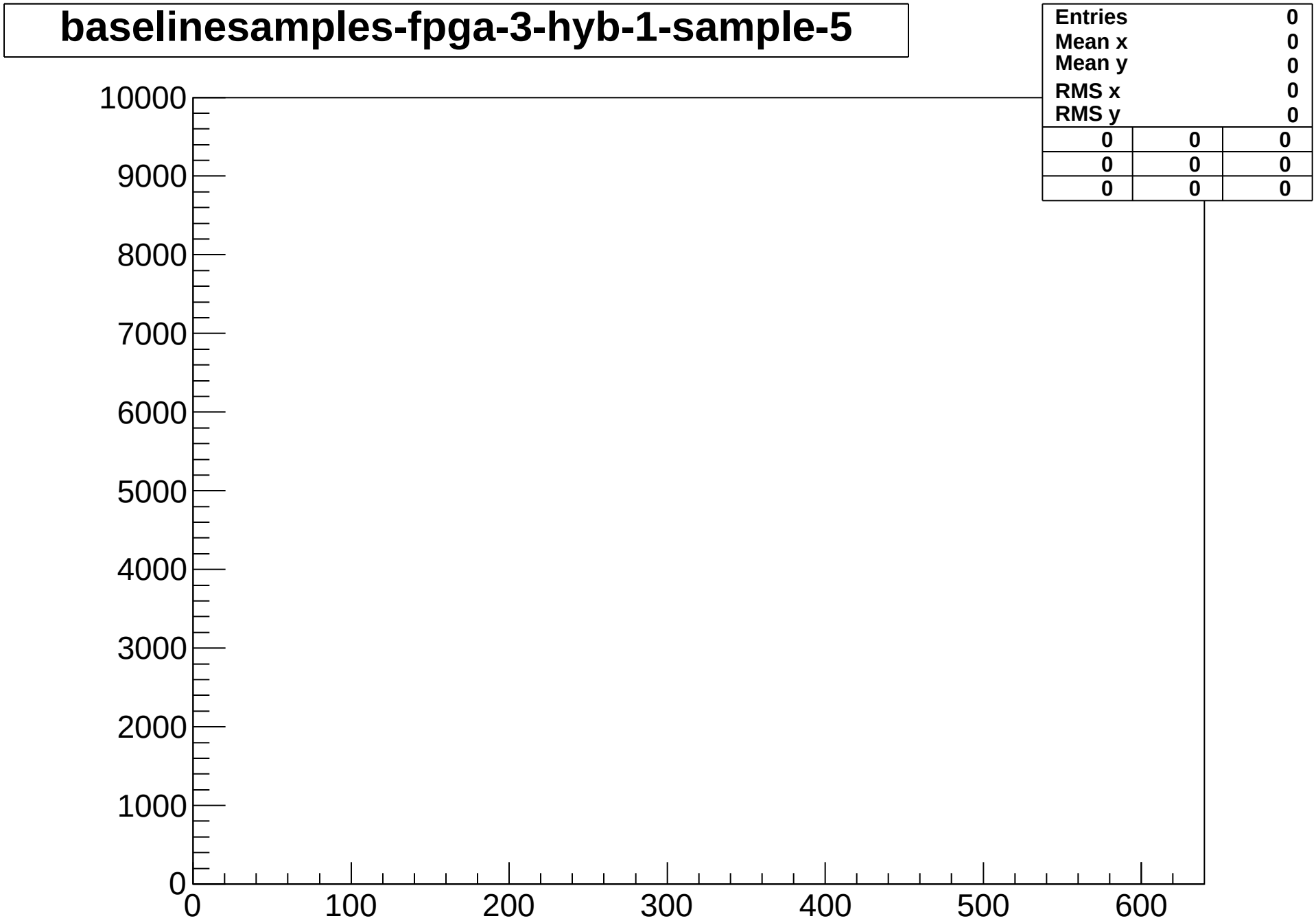
baselinesamples-fpga-3-hyb-1-sample-3



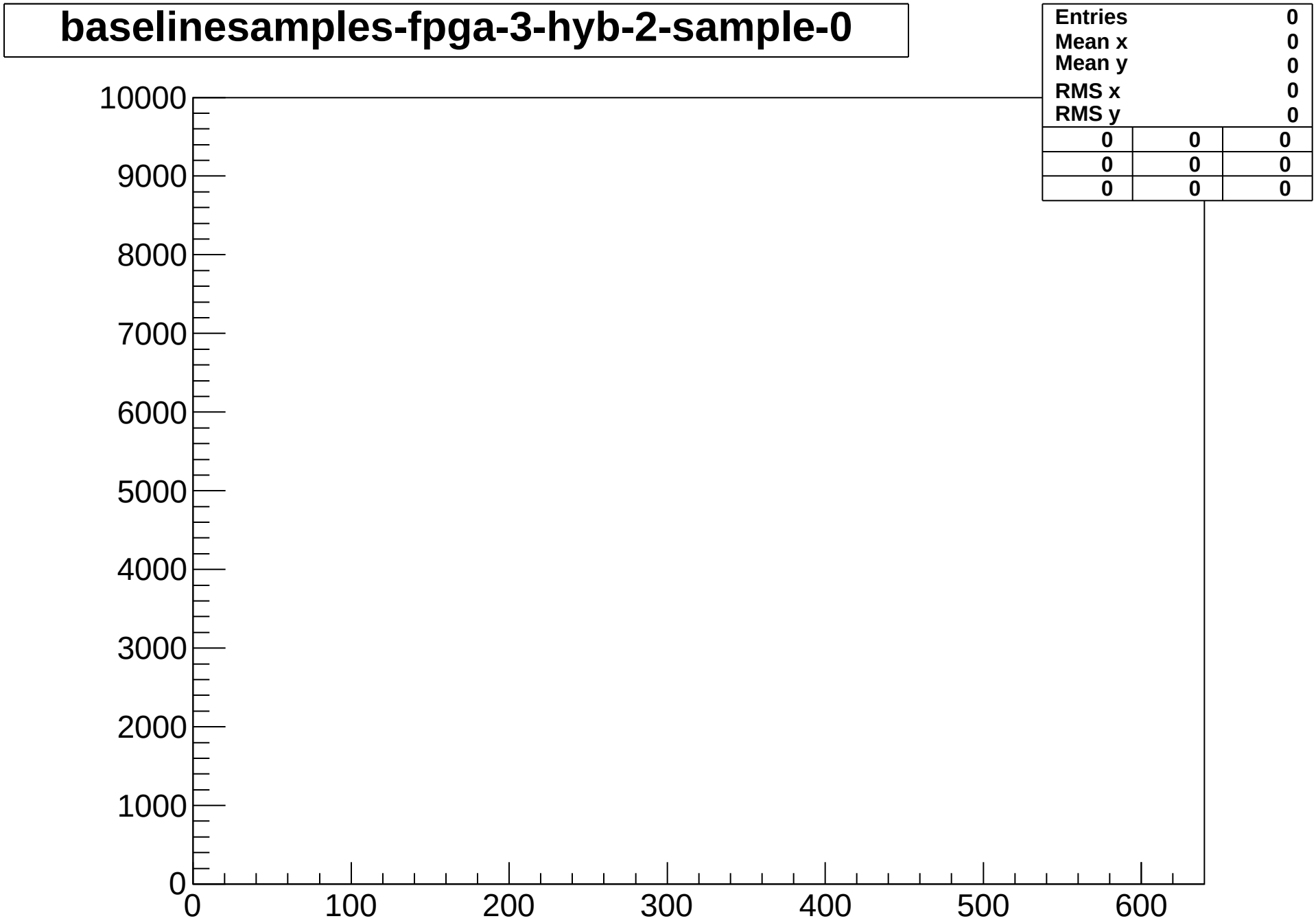
baselinesamples-fpga-3-hyb-1-sample-4



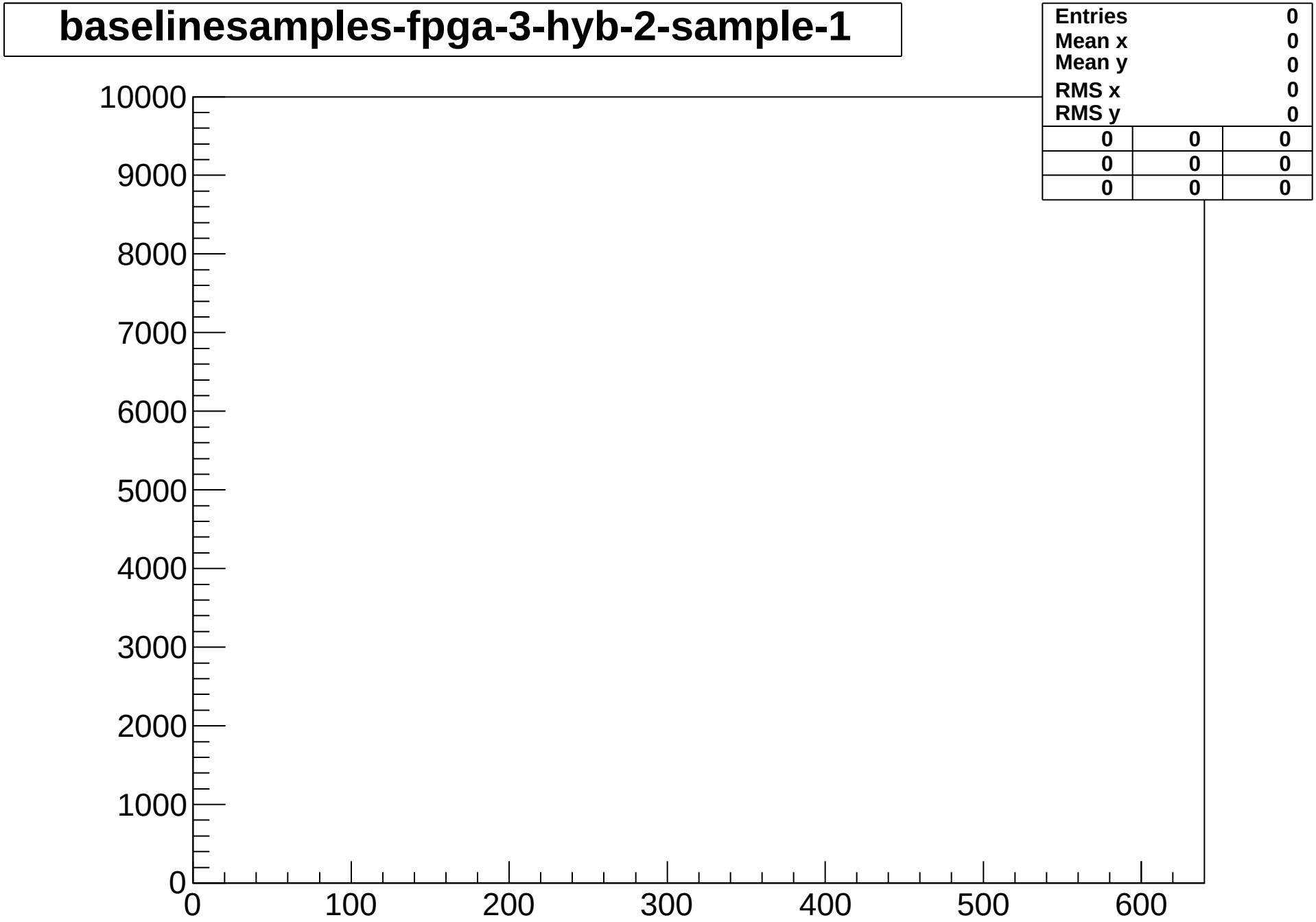
baselinesamples-fpga-3-hyb-1-sample-5



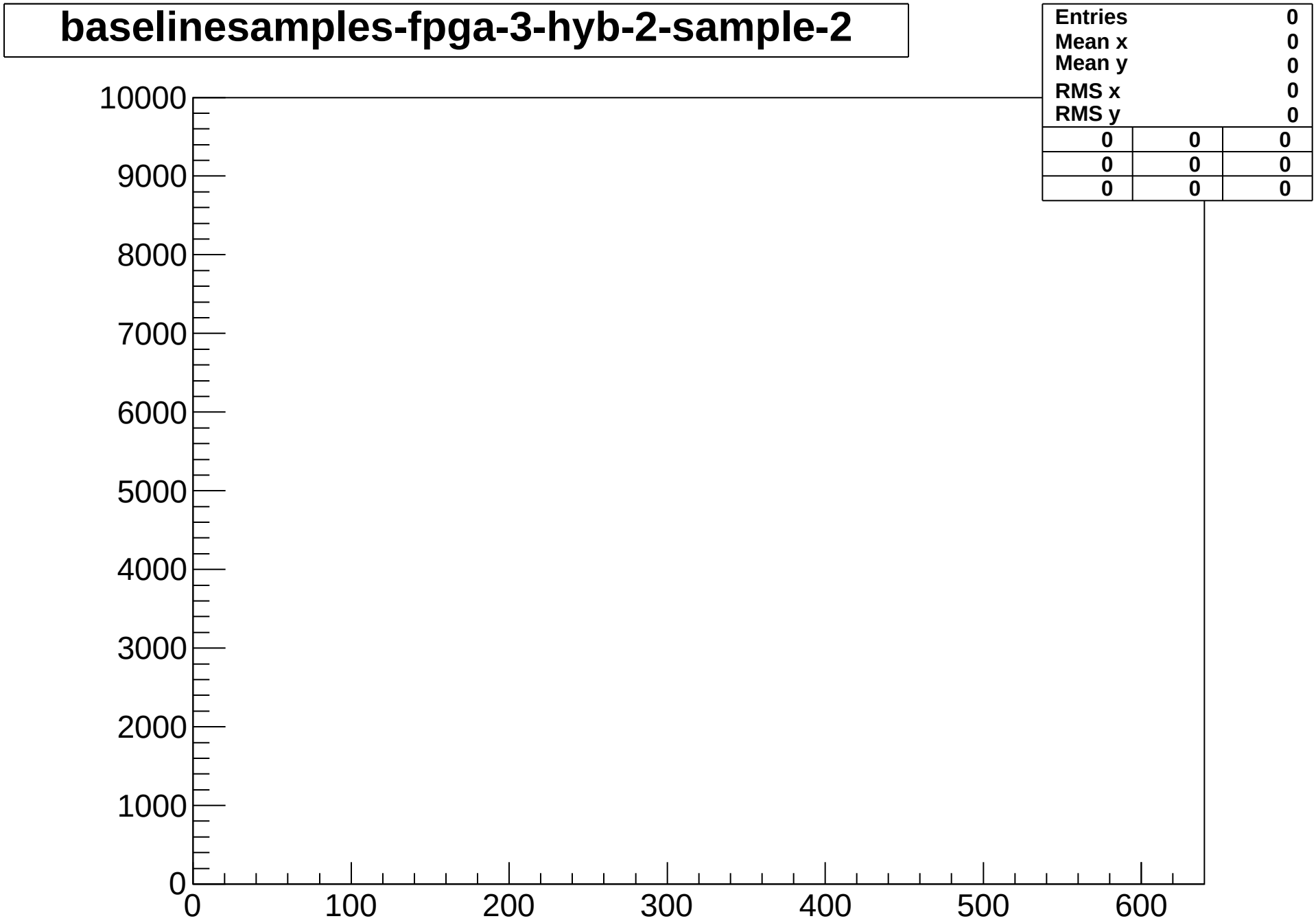
baselinesamples-fpga-3-hyb-2-sample-0



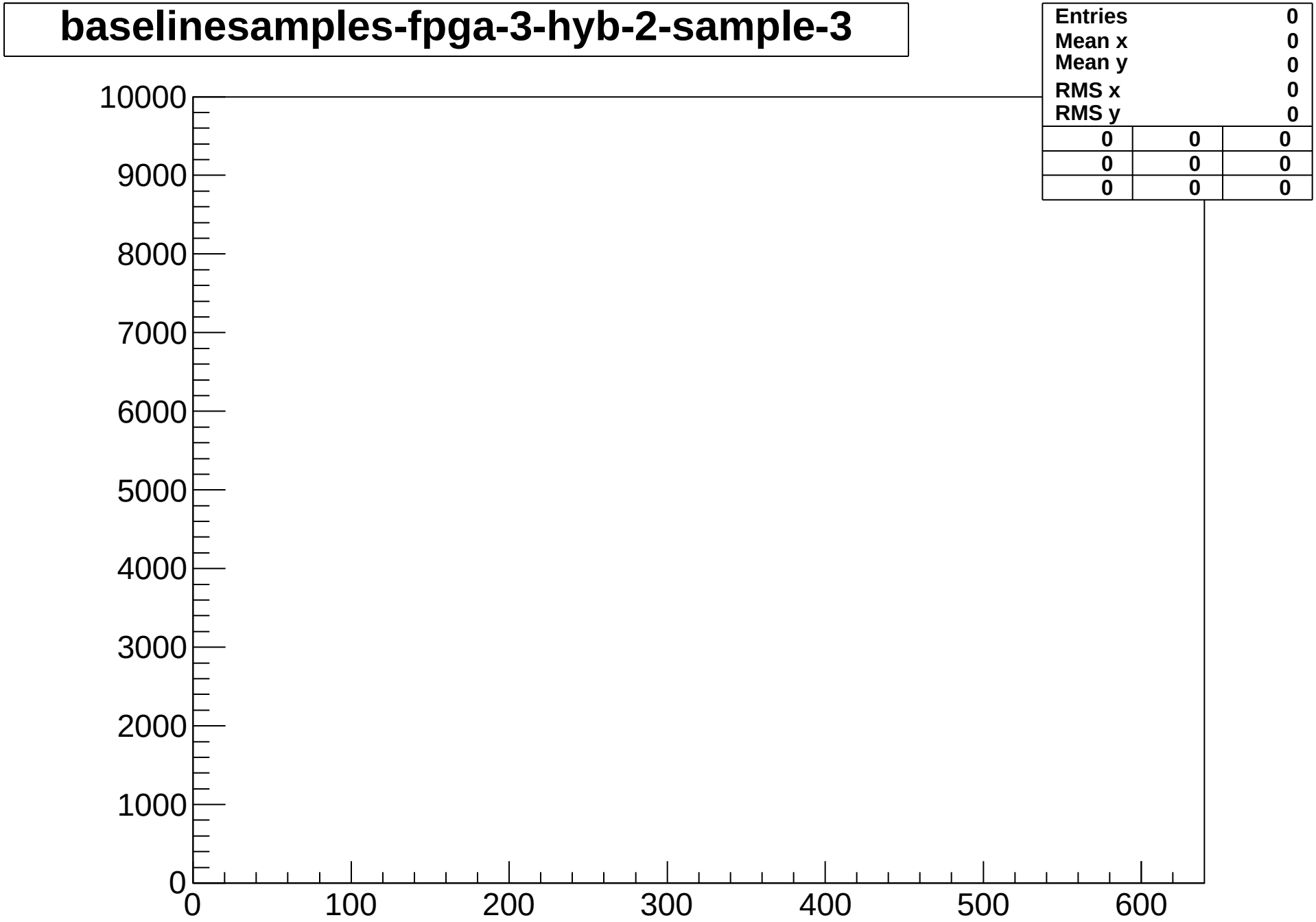
baselinesamples-fpga-3-hyb-2-sample-1



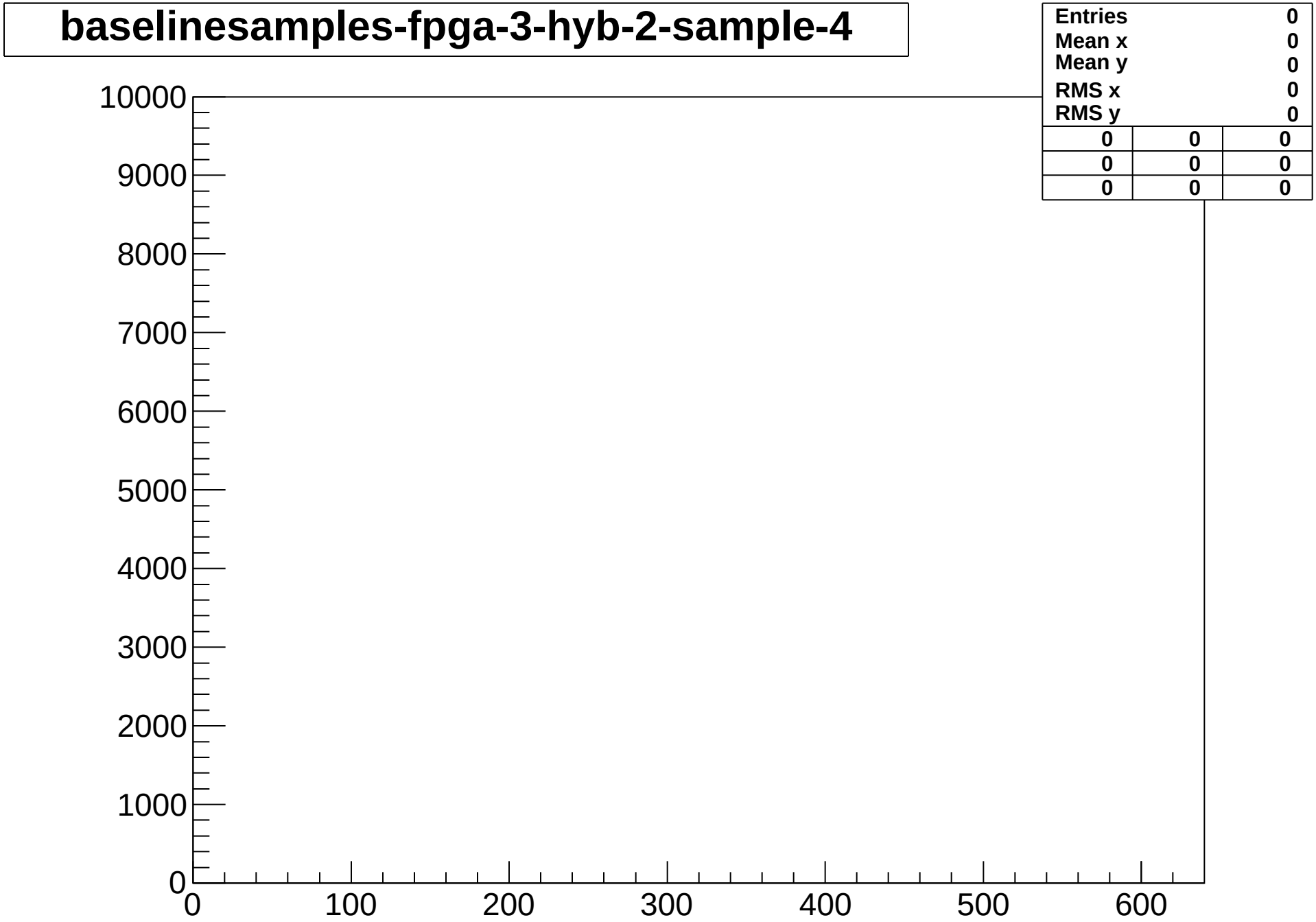
baselinesamples-fpga-3-hyb-2-sample-2



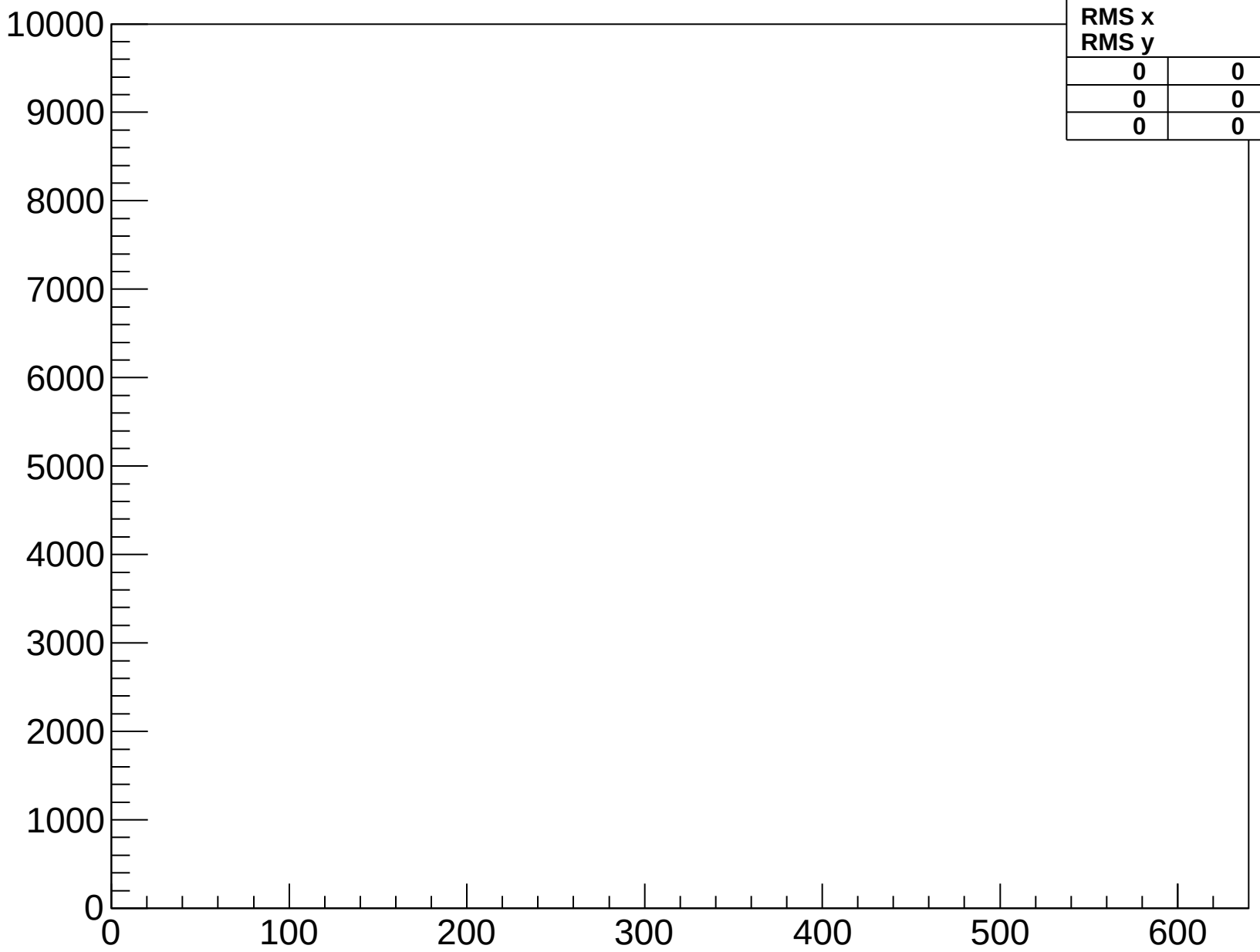
baselinesamples-fpga-3-hyb-2-sample-3



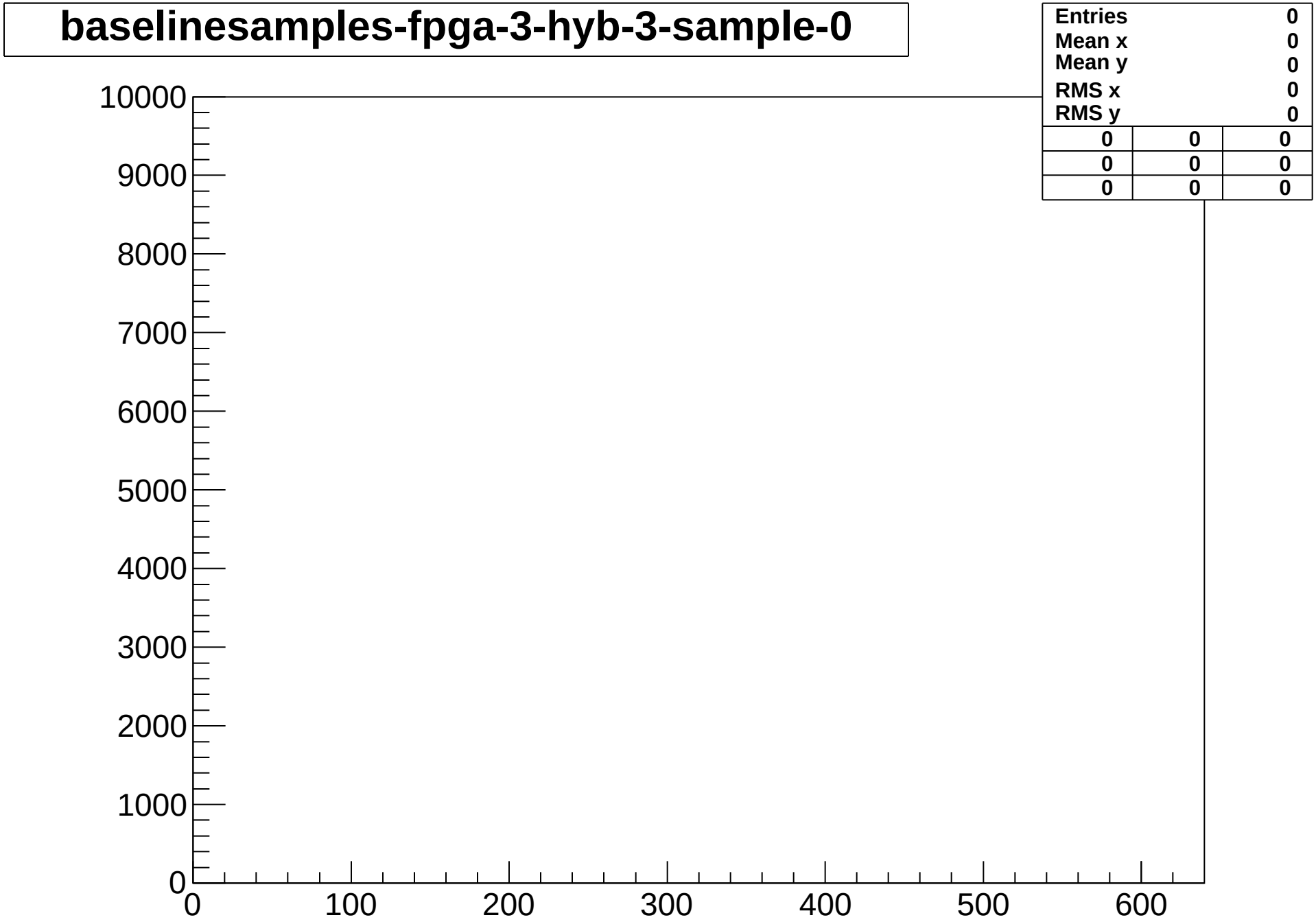
baselinesamples-fpga-3-hyb-2-sample-4



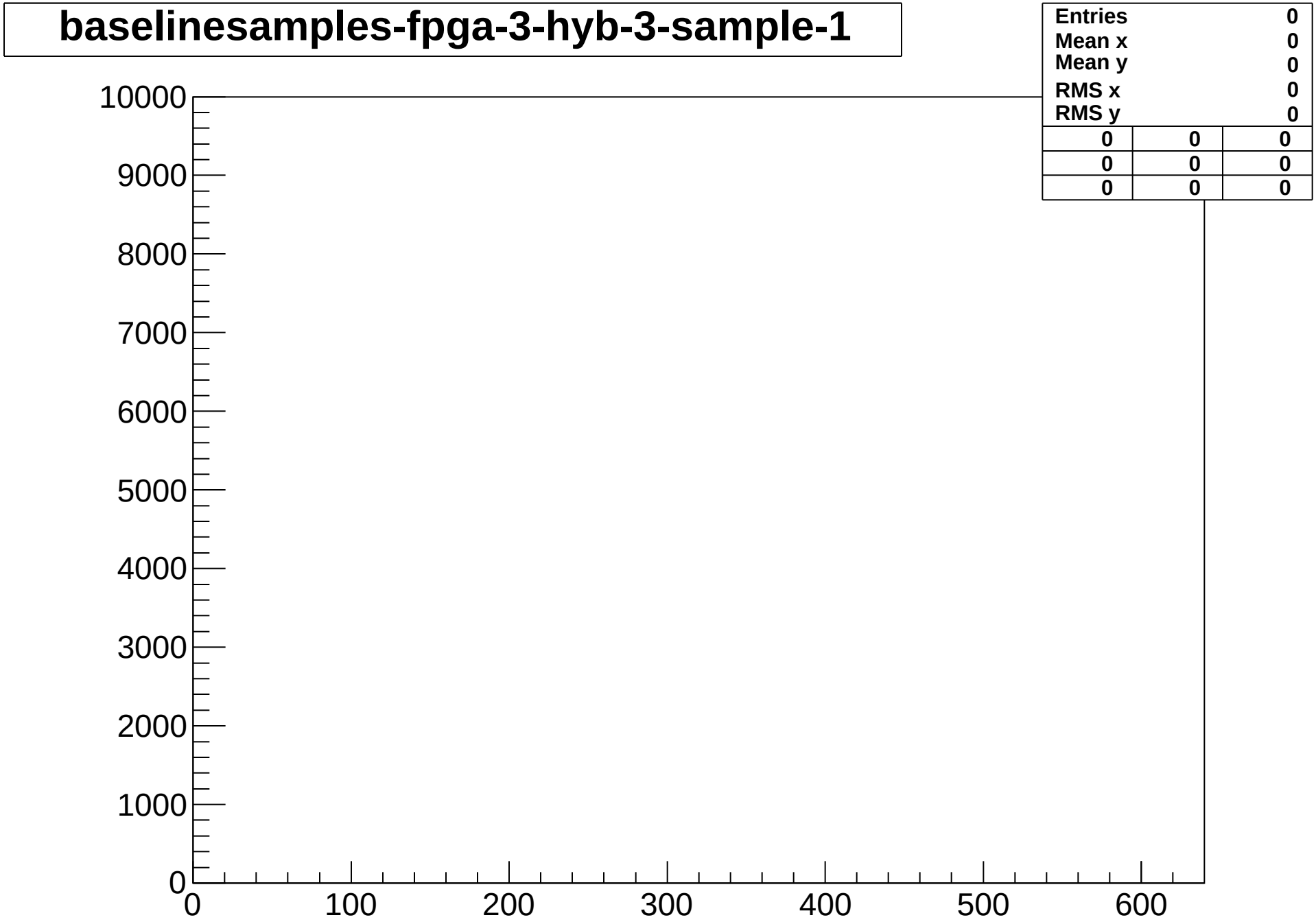
baselinesamples-fpga-3-hyb-2-sample-5



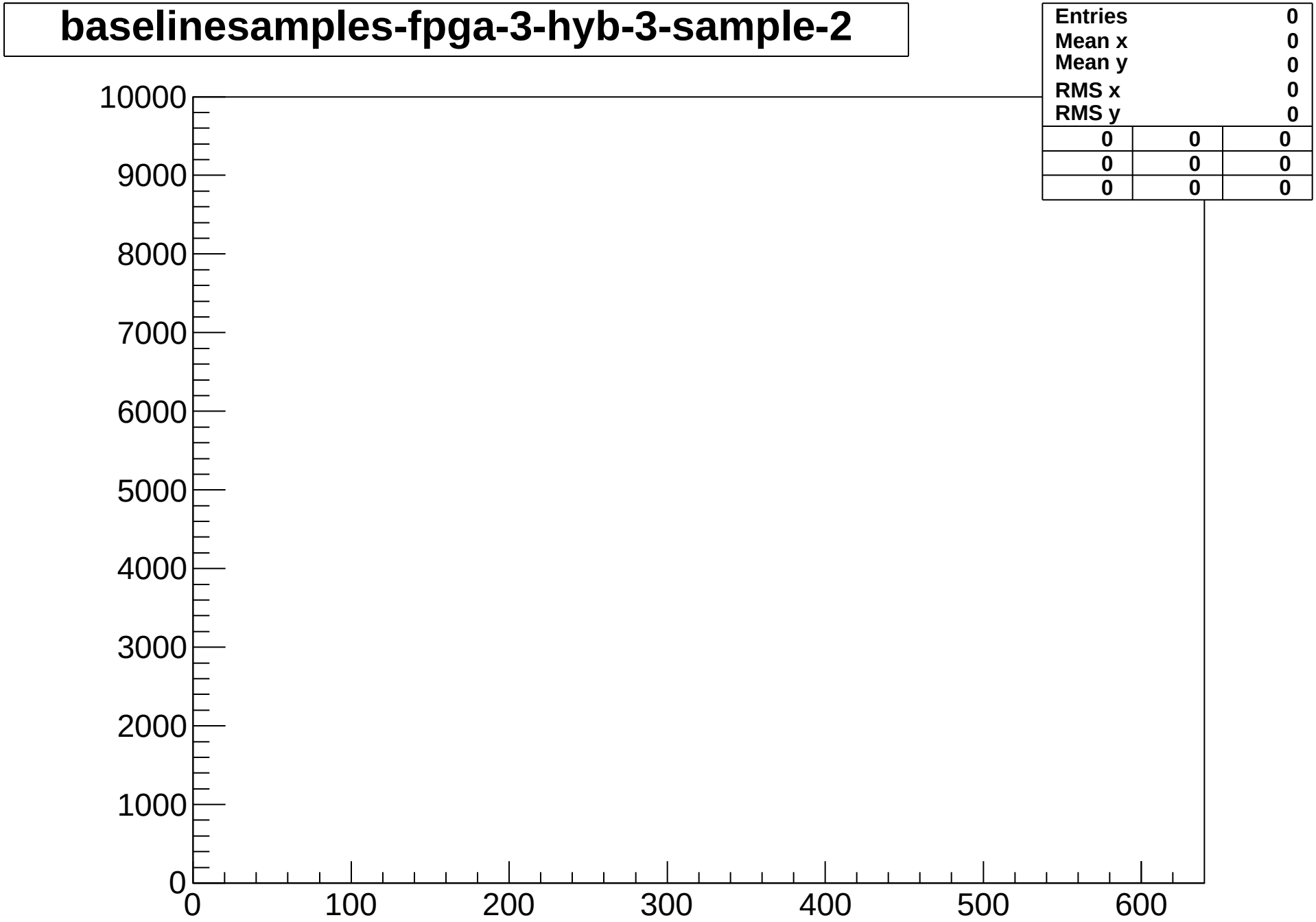
baselinesamples-fpga-3-hyb-3-sample-0



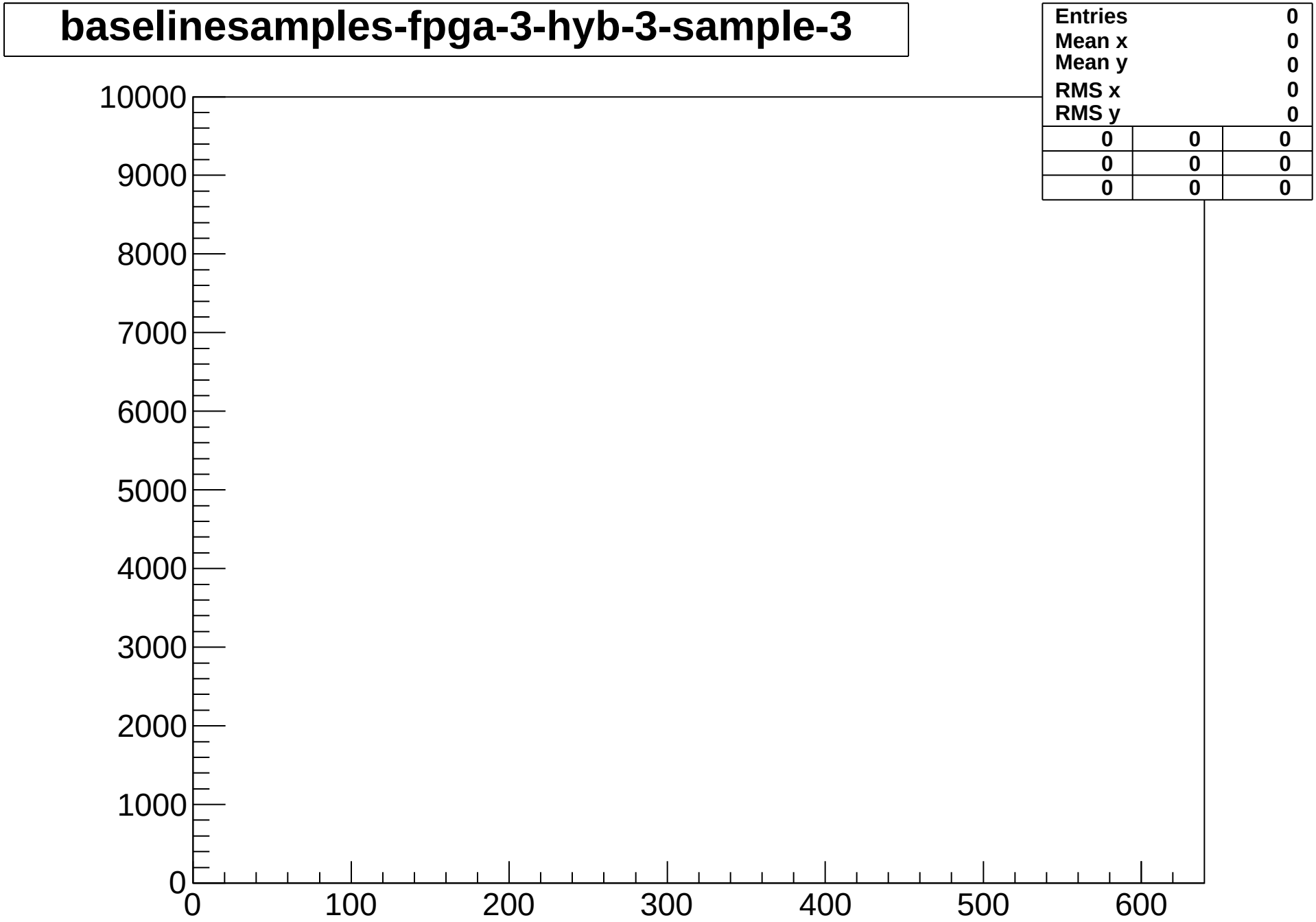
baselinesamples-fpga-3-hyb-3-sample-1



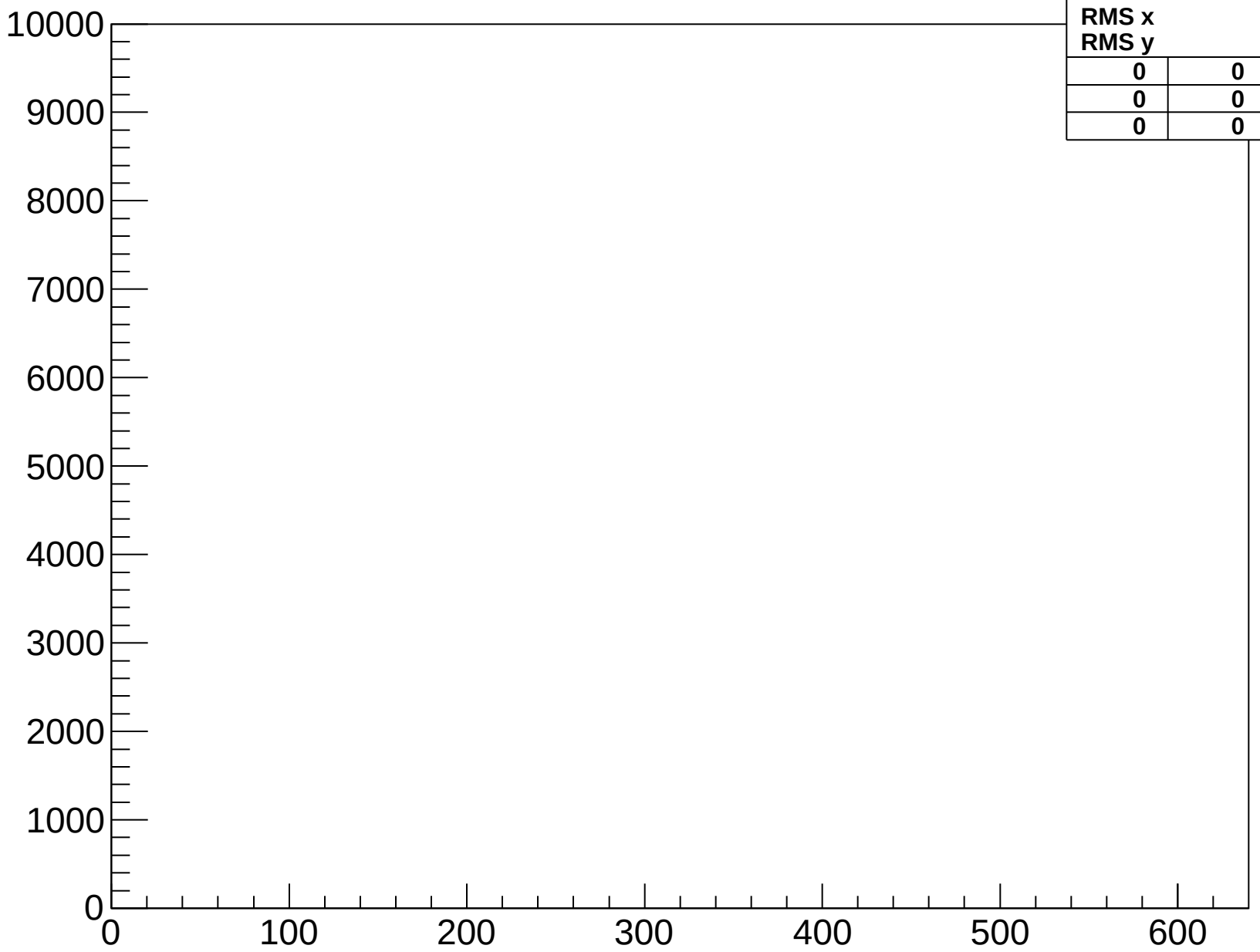
baselinesamples-fpga-3-hyb-3-sample-2



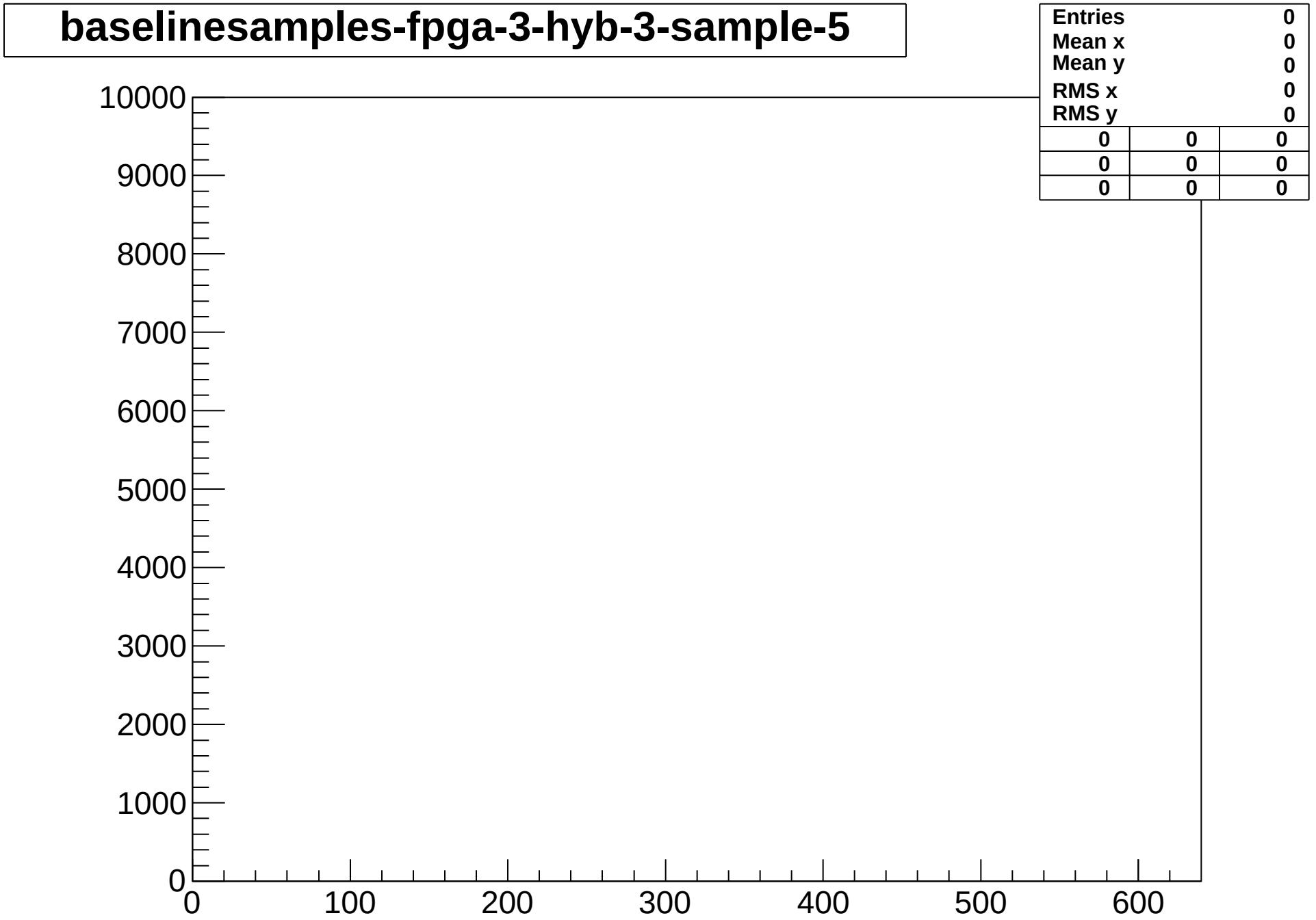
baselinesamples-fpga-3-hyb-3-sample-3



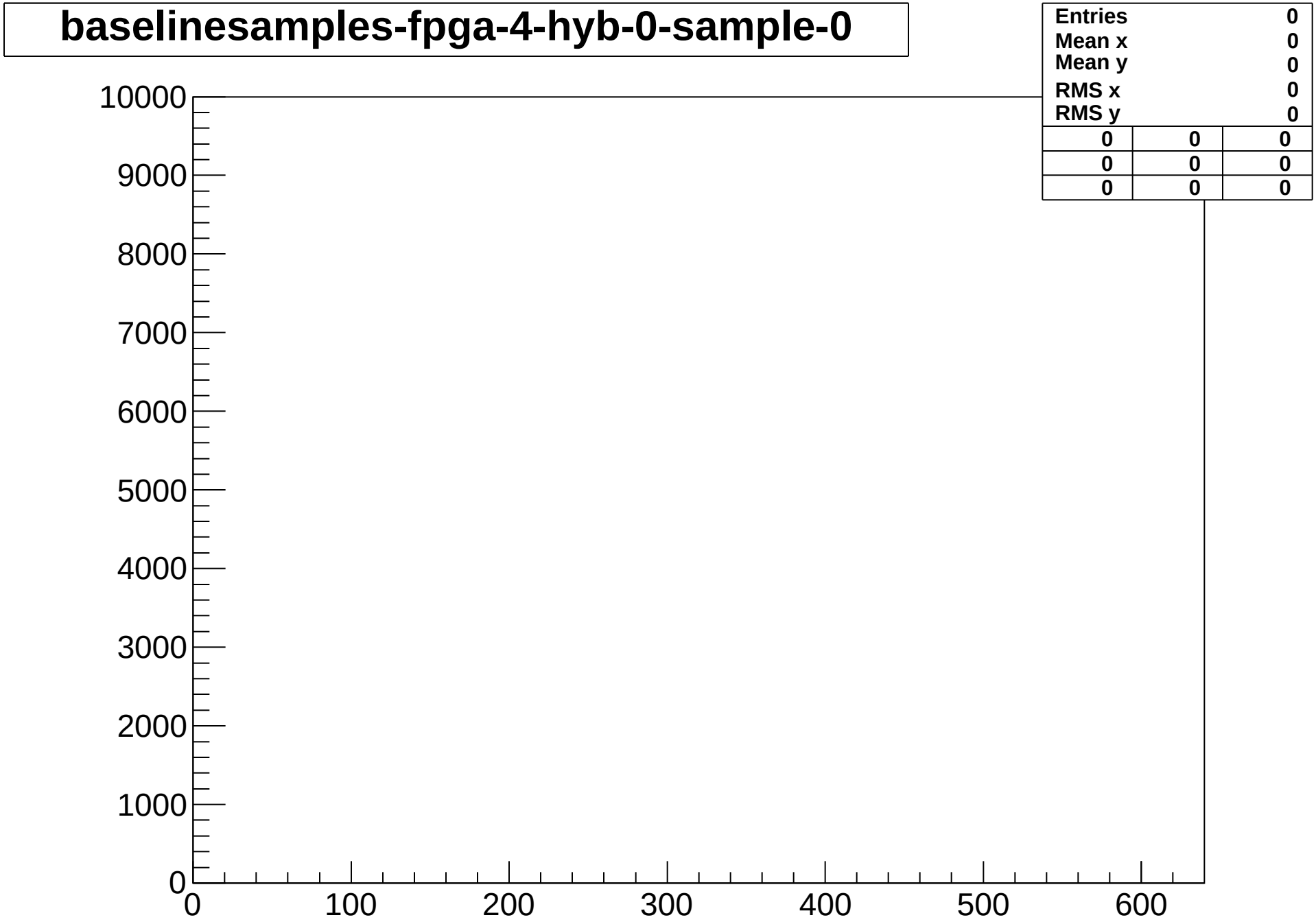
baselinesamples-fpga-3-hyb-3-sample-4

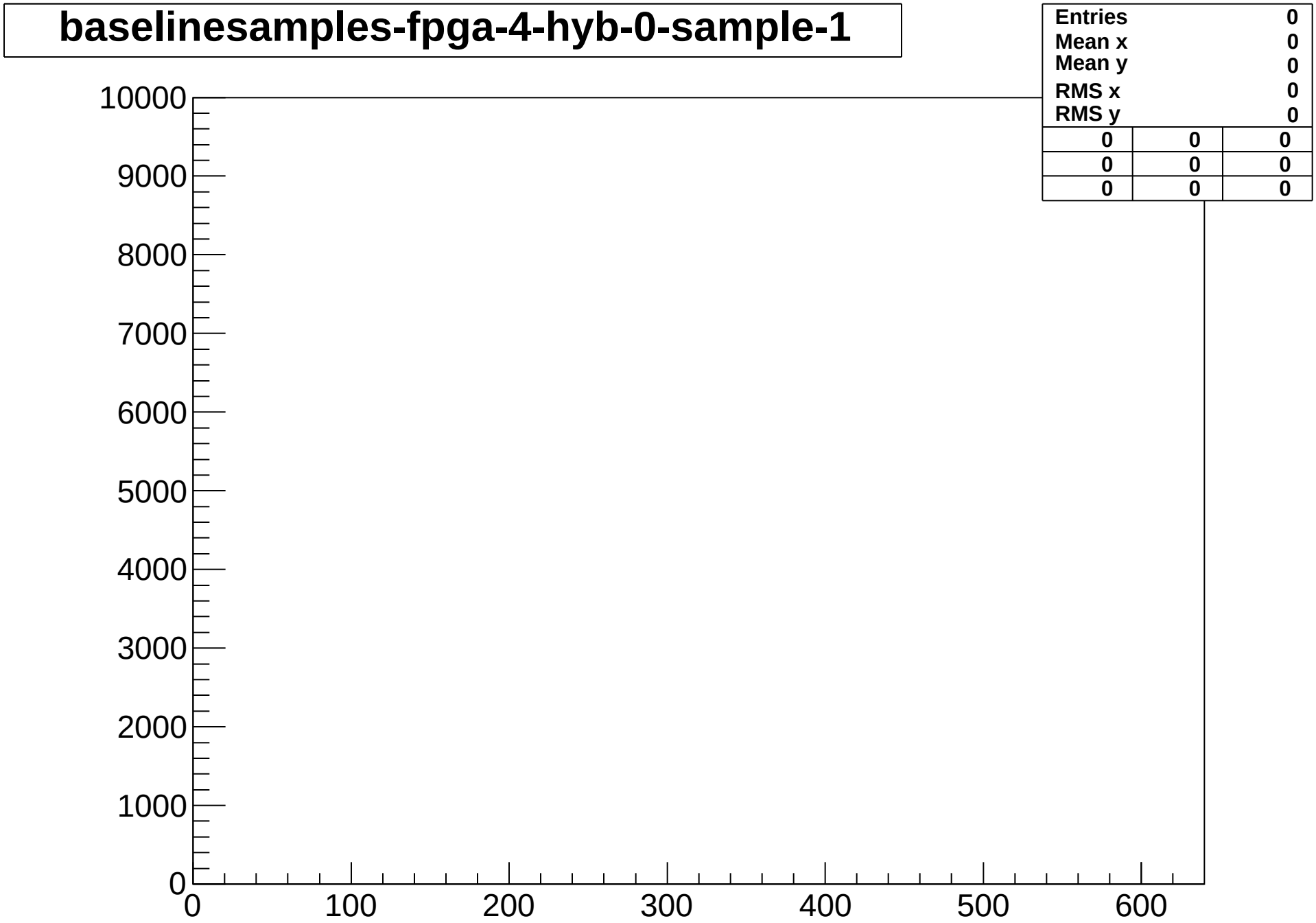


baselinesamples-fpga-3-hyb-3-sample-5

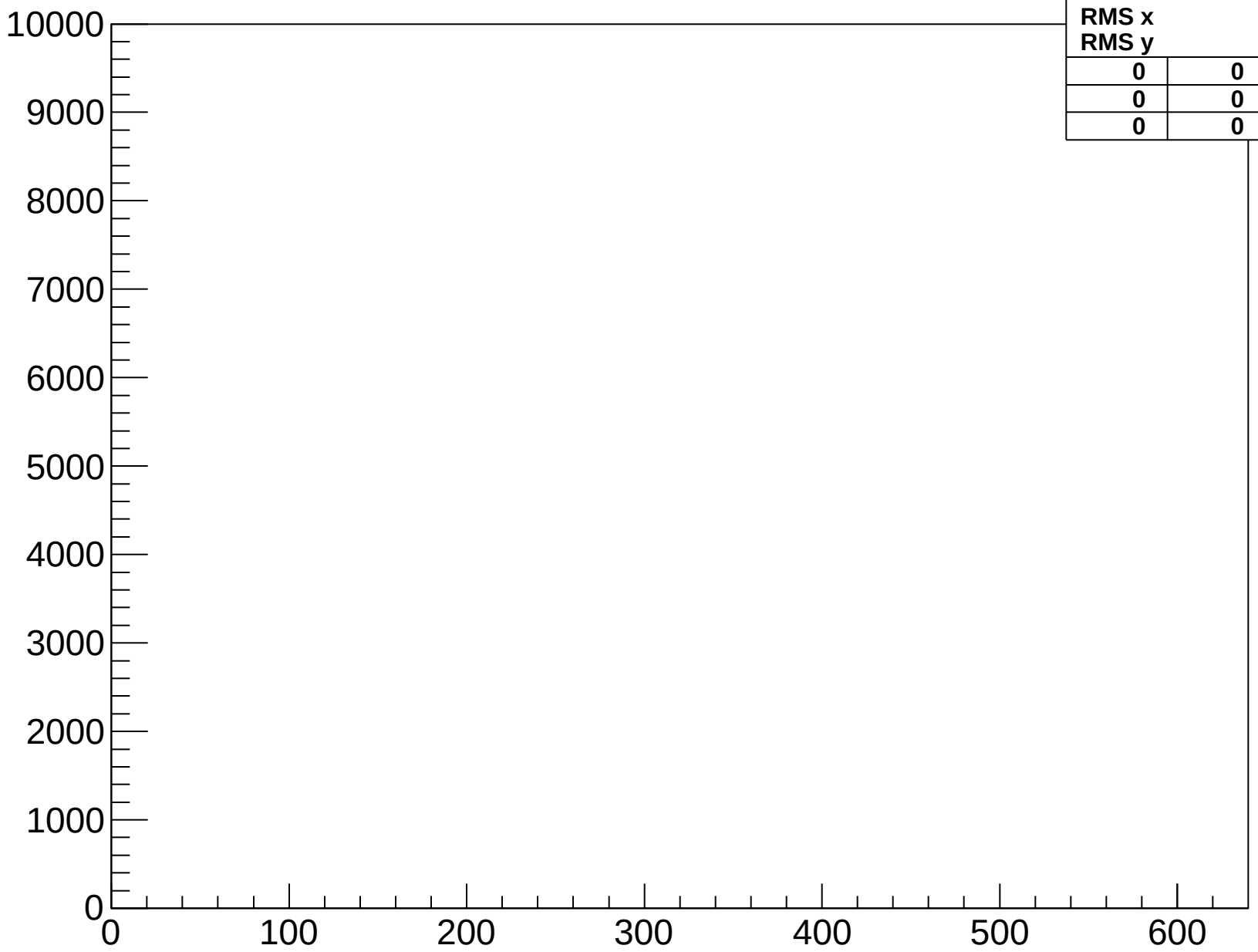


baselinesamples-fpga-4-hyb-0-sample-0

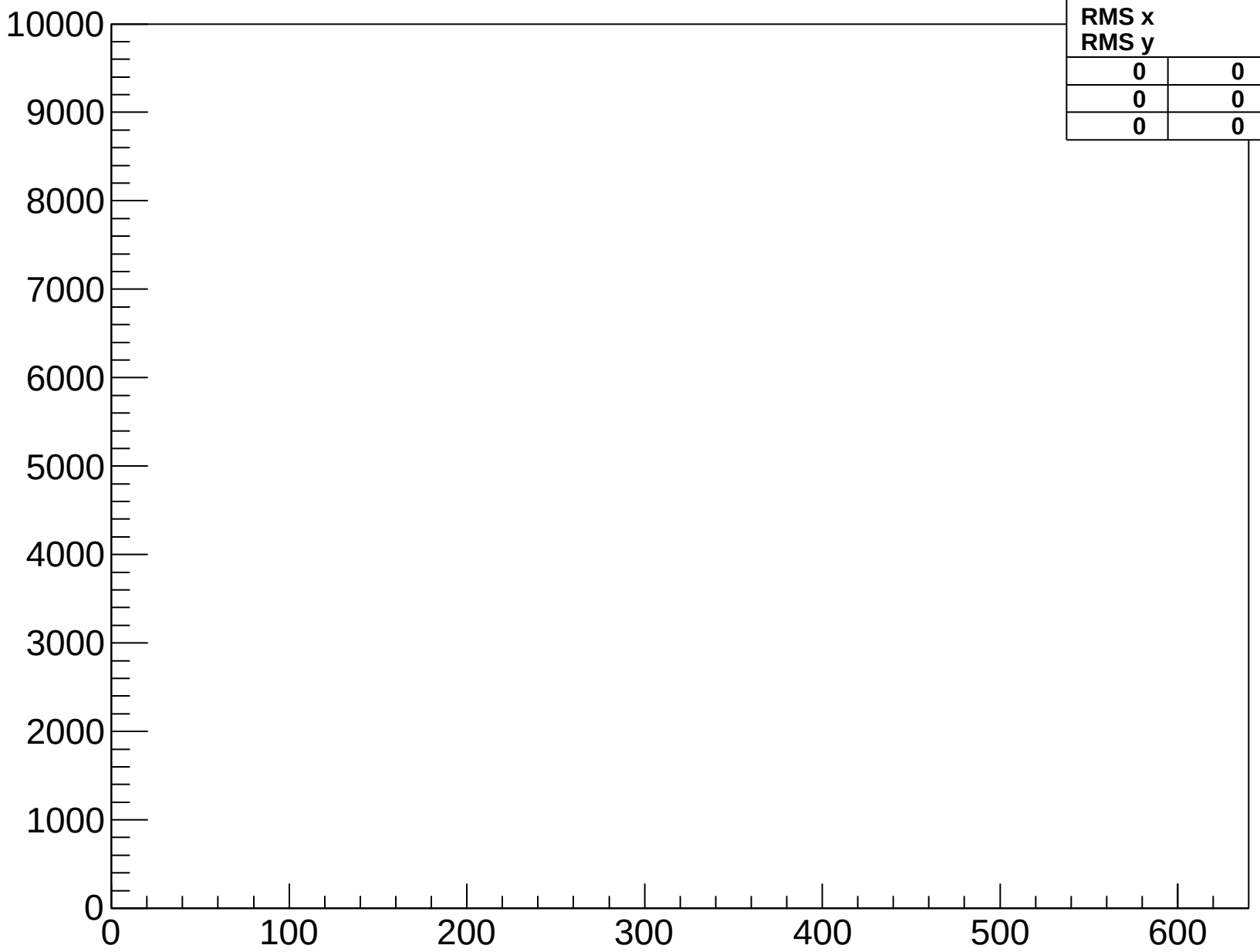



baselinesamples-fpga-4-hyb-0-sample-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

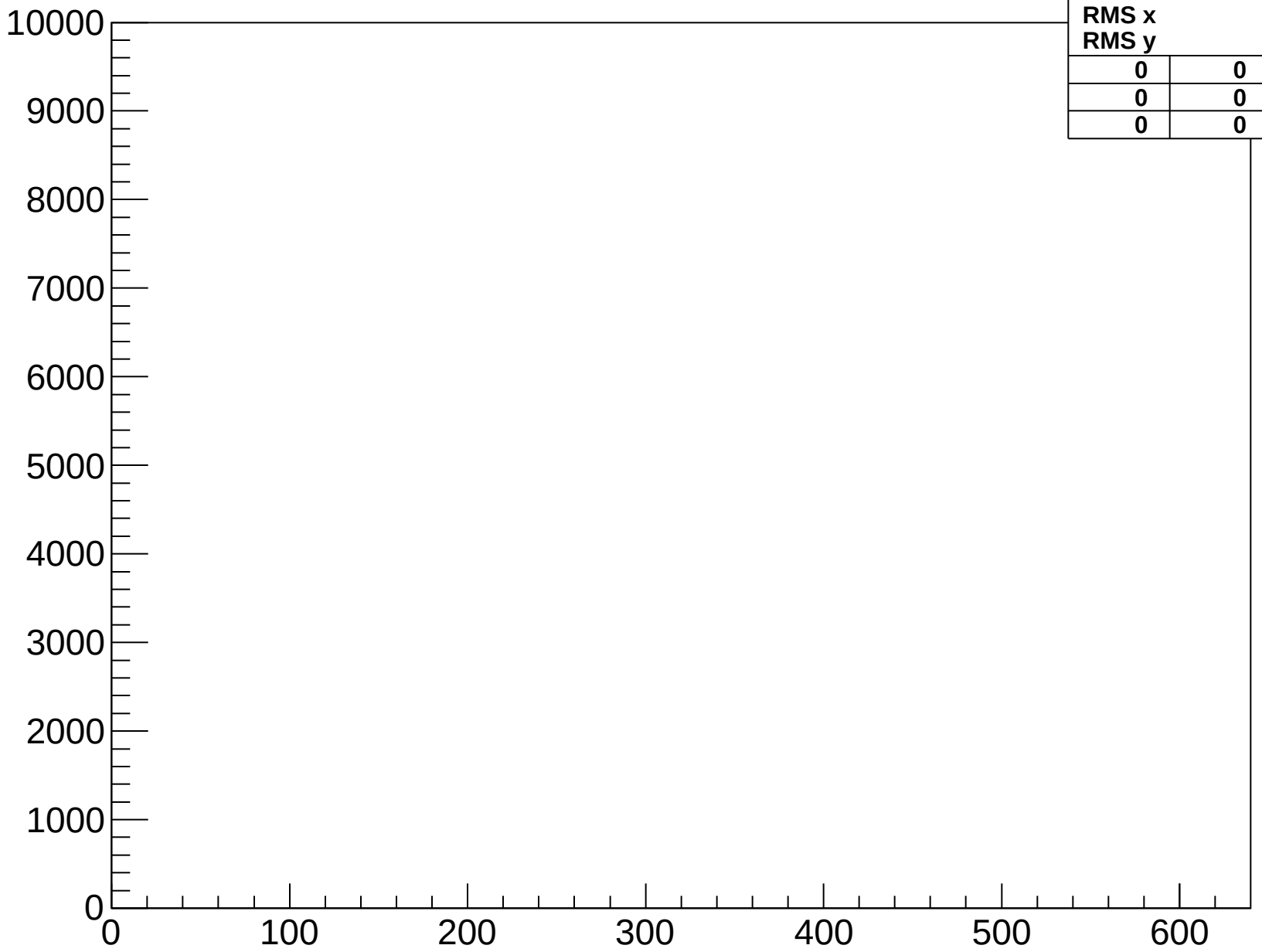
baselinesamples-fpga-4-hyb-0-sample-2



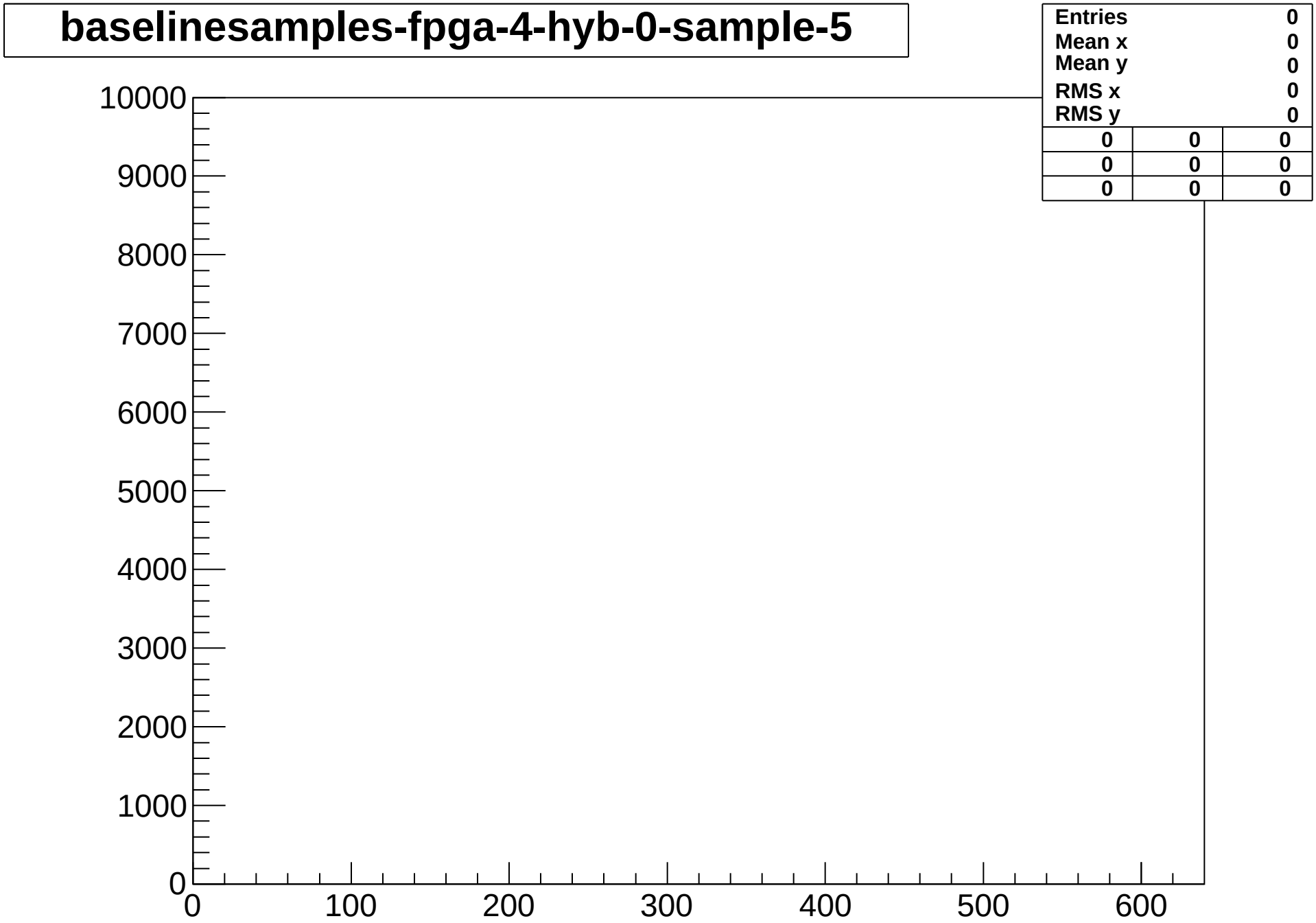
baselinesamples-fpga-4-hyb-0-sample-3

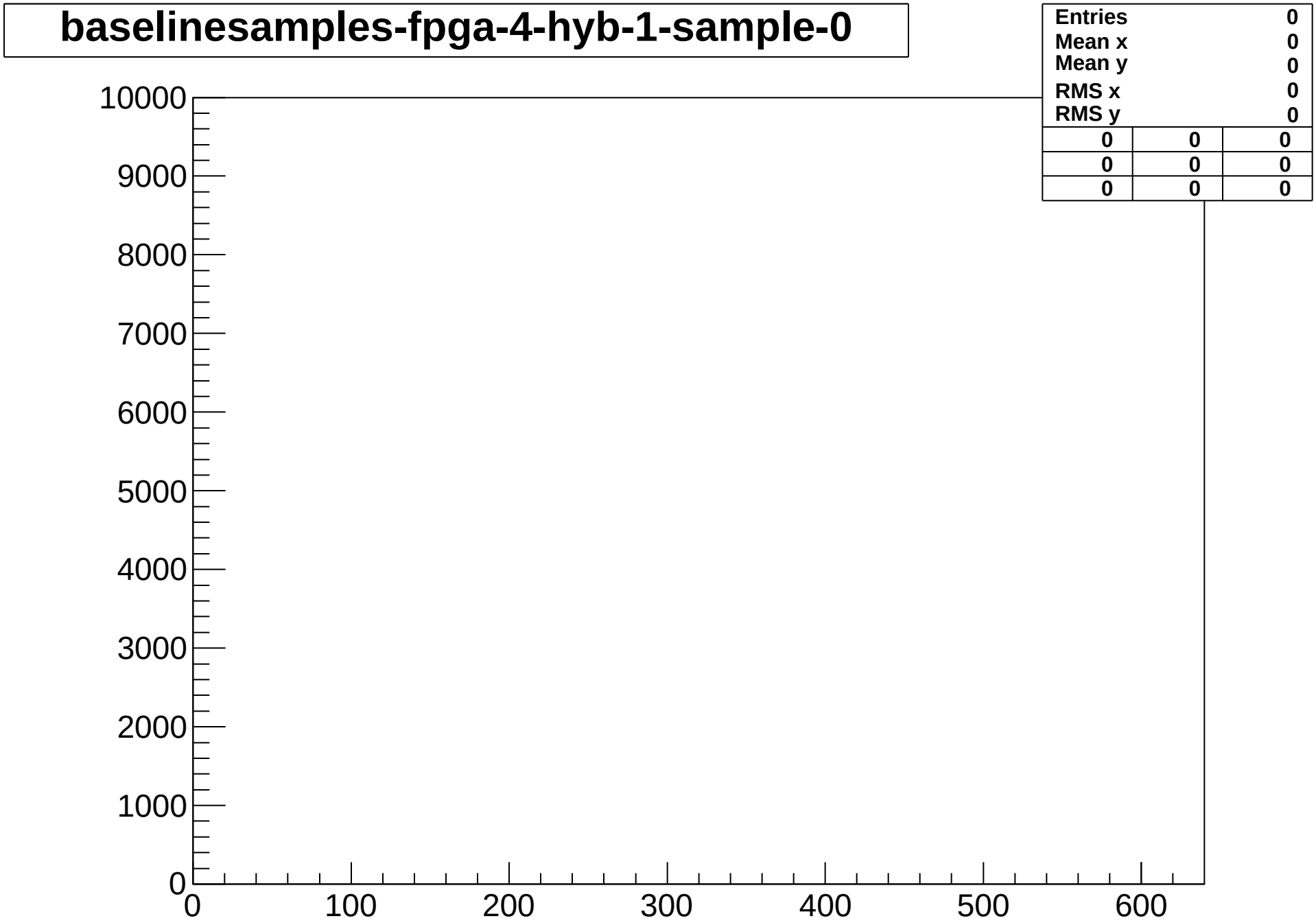


baselinesamples-fpga-4-hyb-0-sample-4

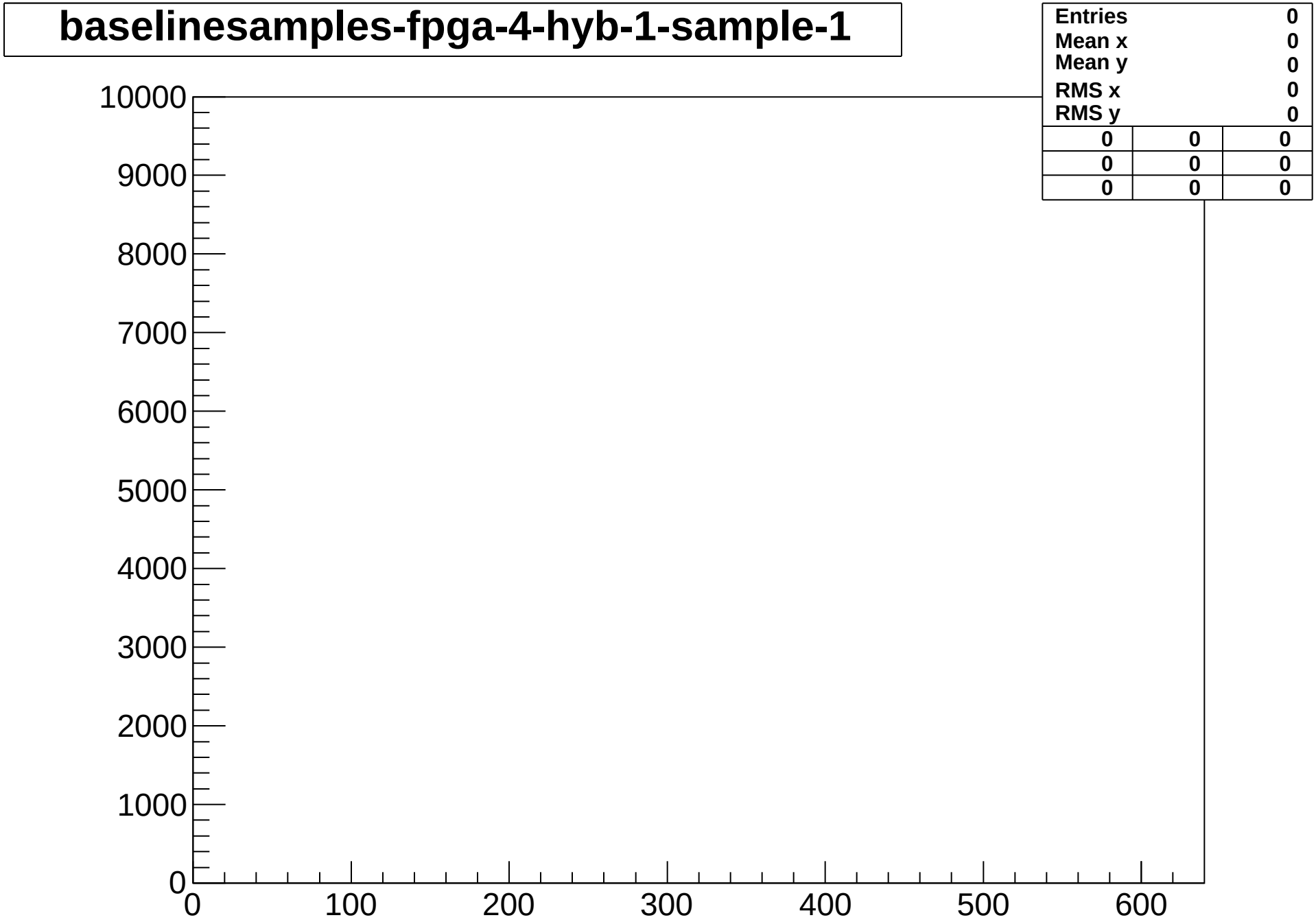


baselinesamples-fpga-4-hyb-0-sample-5

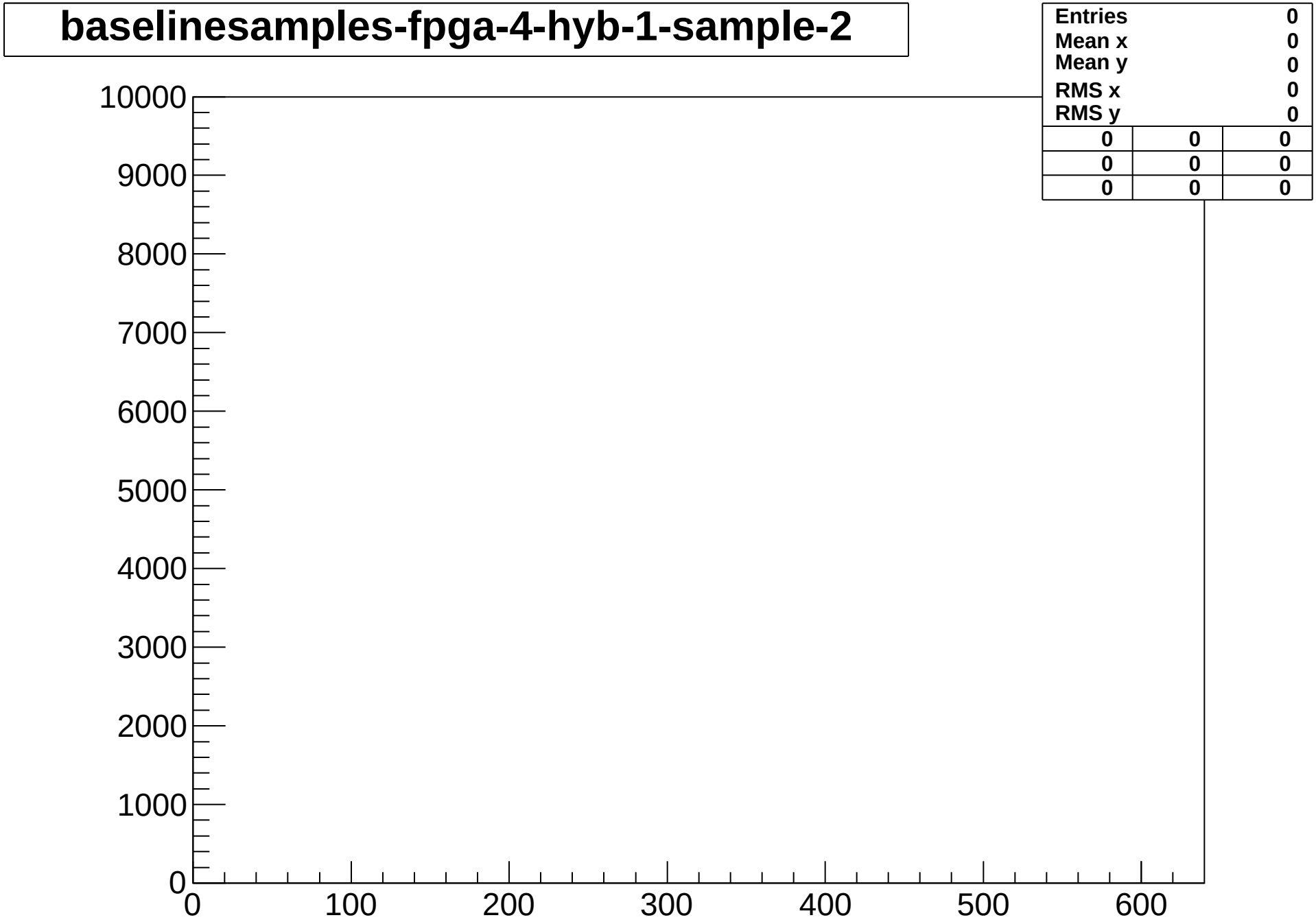



baselinesamples-fpga-4-hyb-1-sample-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

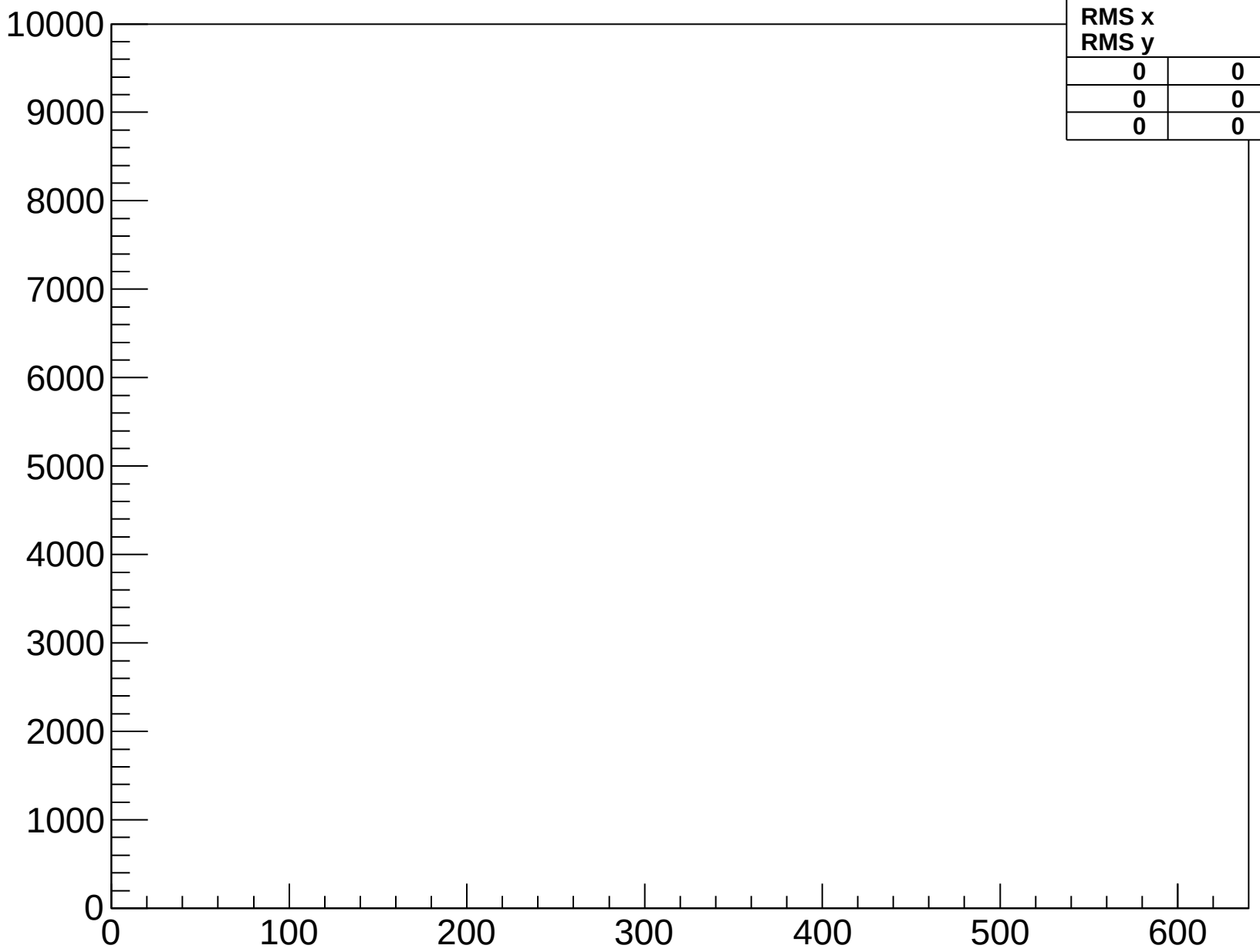
baselinesamples-fpga-4-hyb-1-sample-1



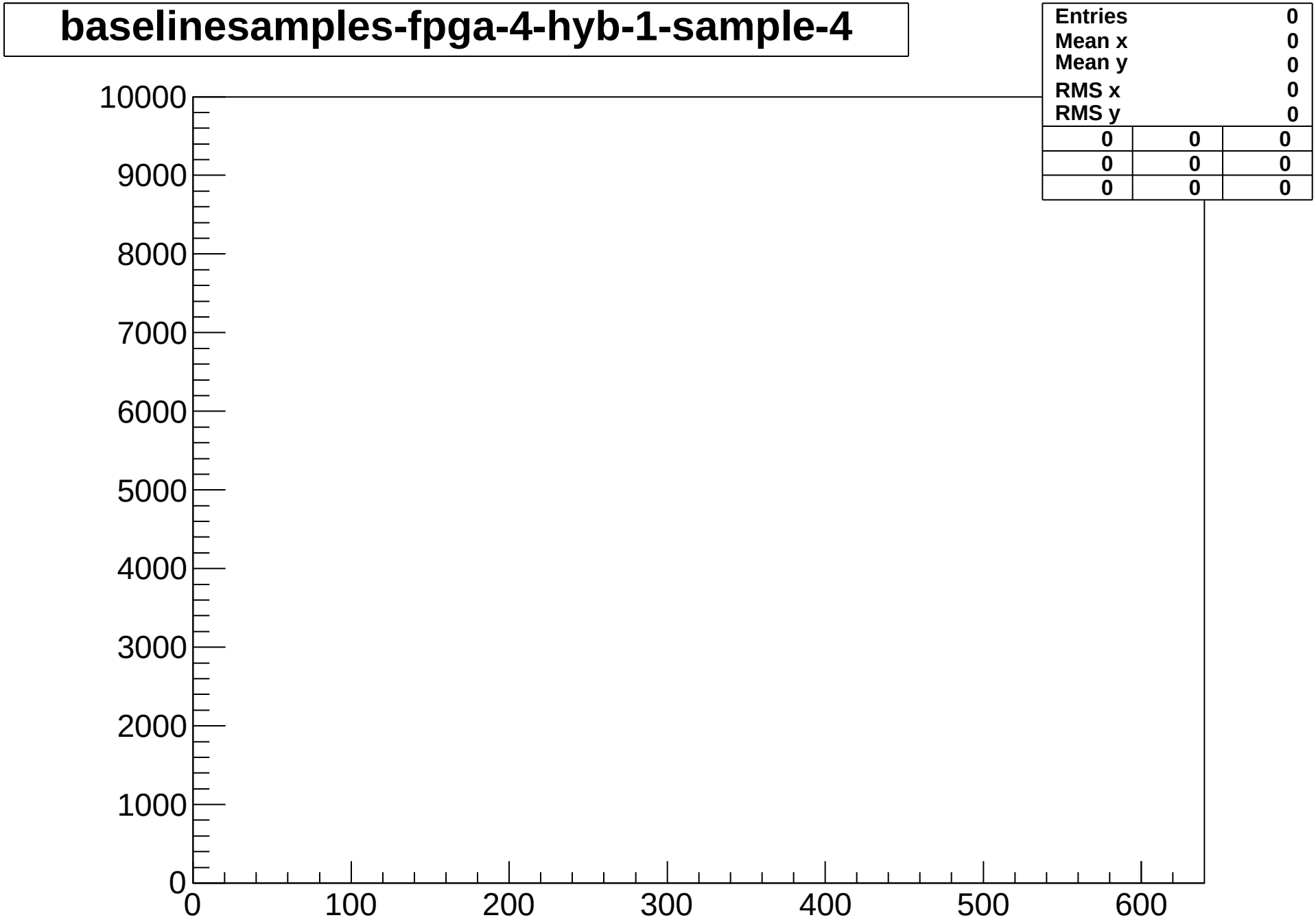
baselinesamples-fpga-4-hyb-1-sample-2



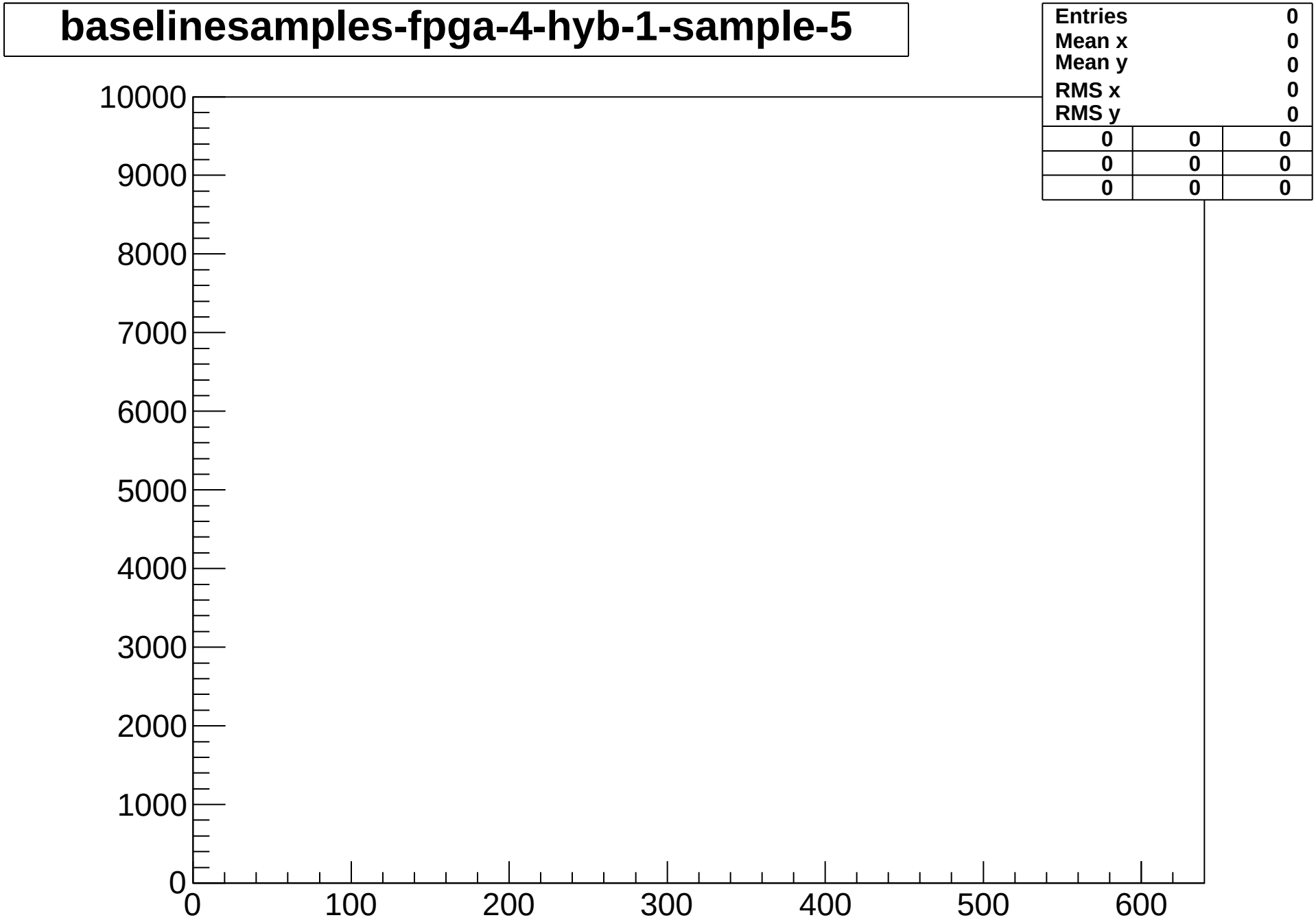
baselinesamples-fpga-4-hyb-1-sample-3



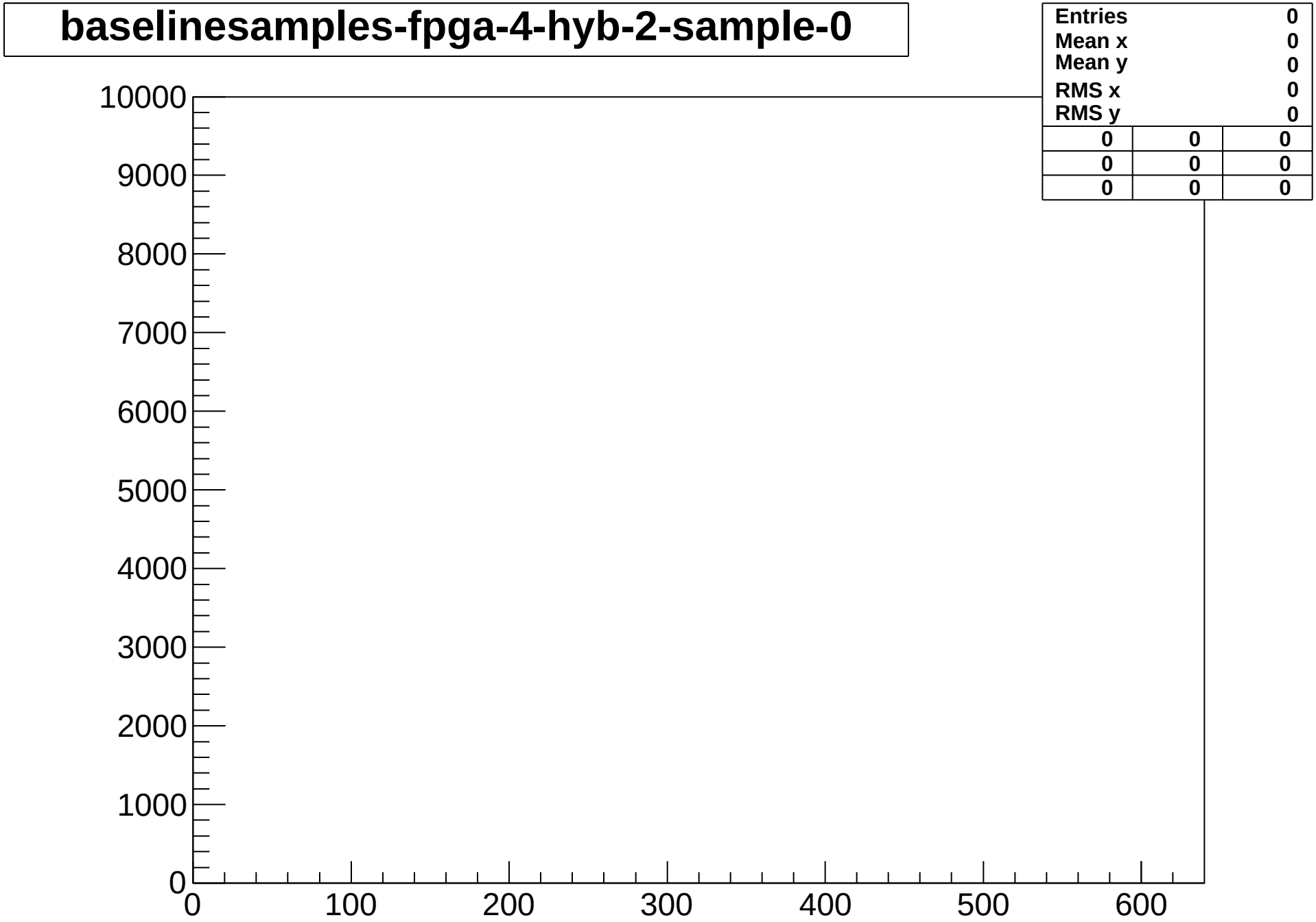
baselinesamples-fpga-4-hyb-1-sample-4



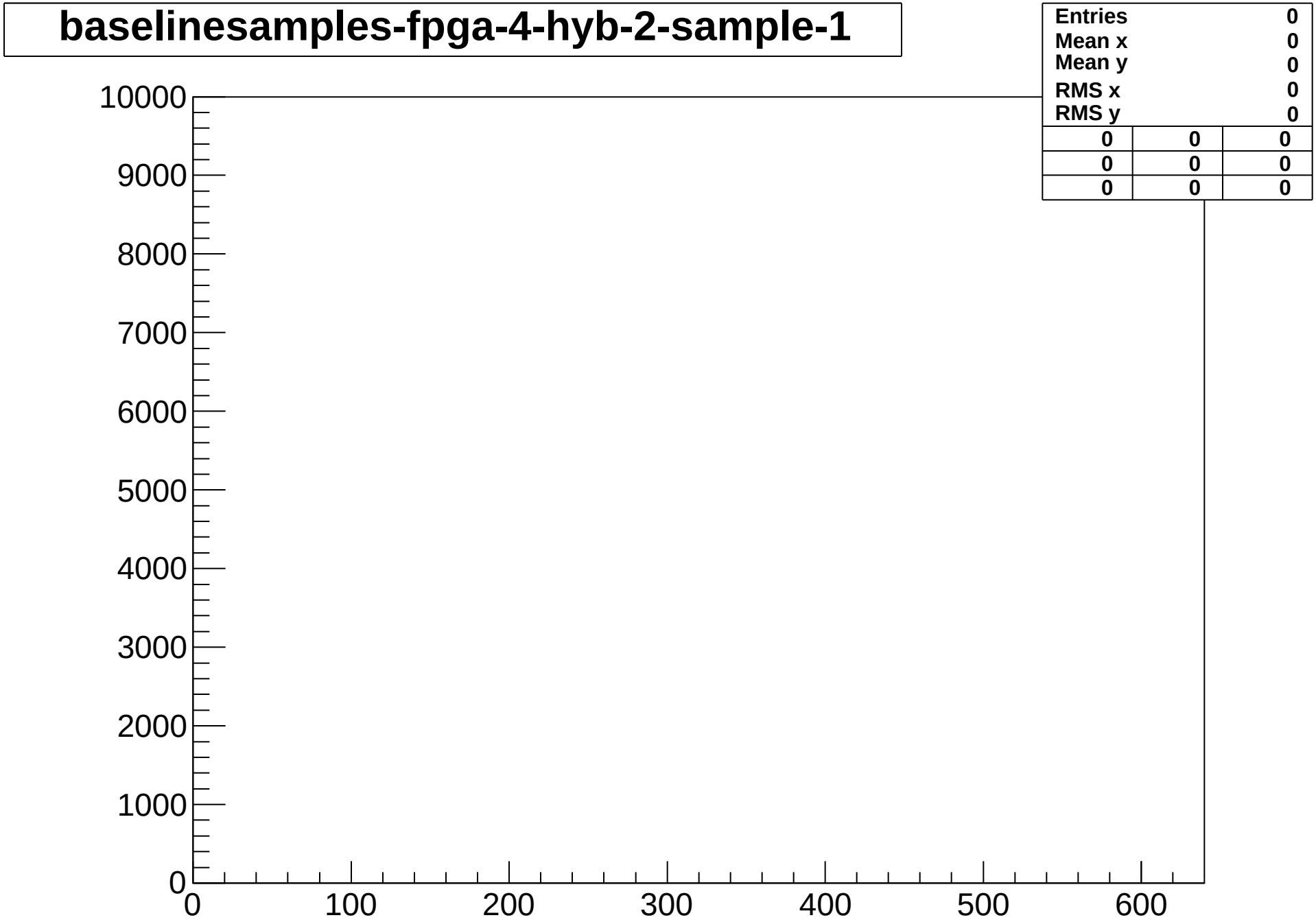
baselinesamples-fpga-4-hyb-1-sample-5



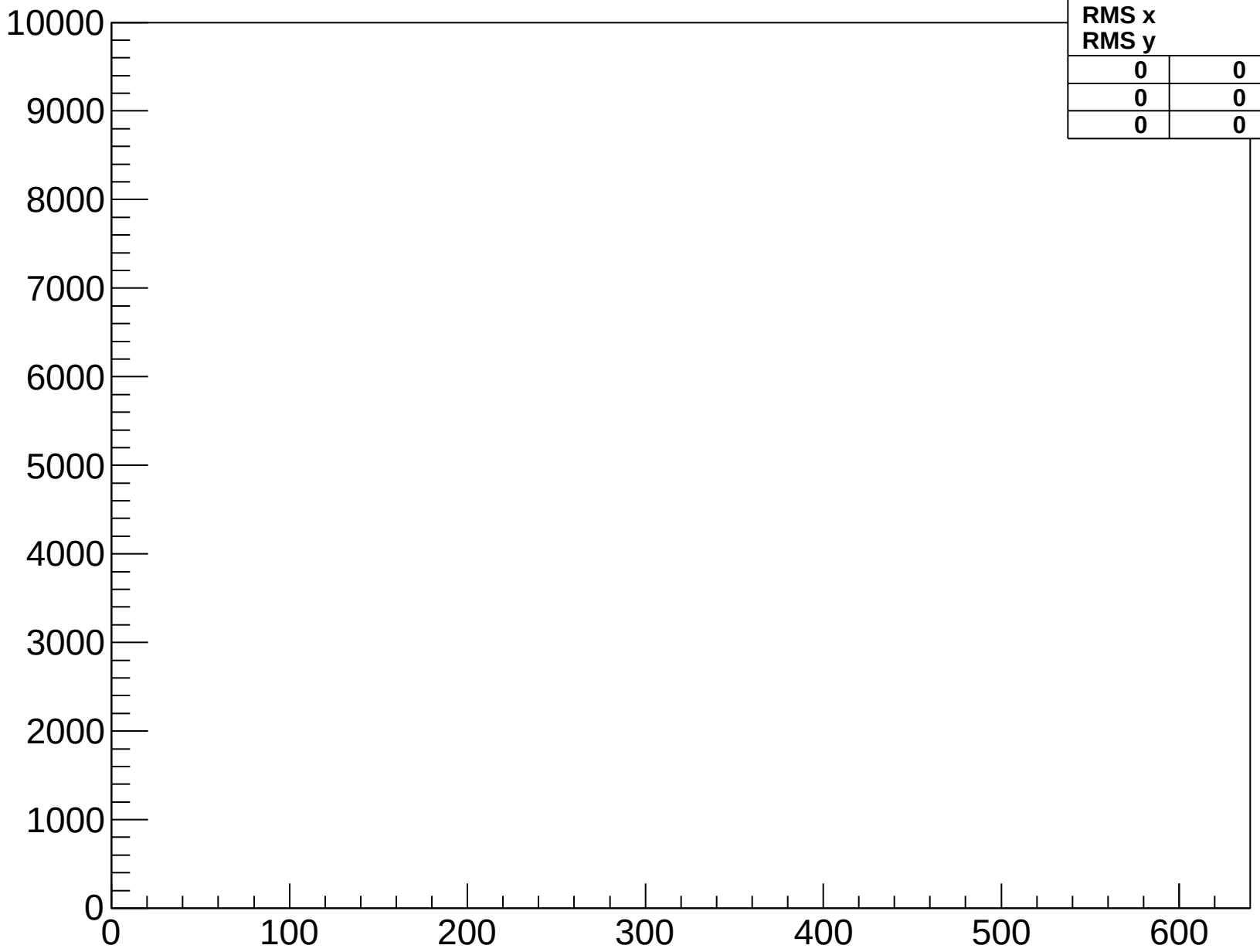
baselinesamples-fpga-4-hyb-2-sample-0



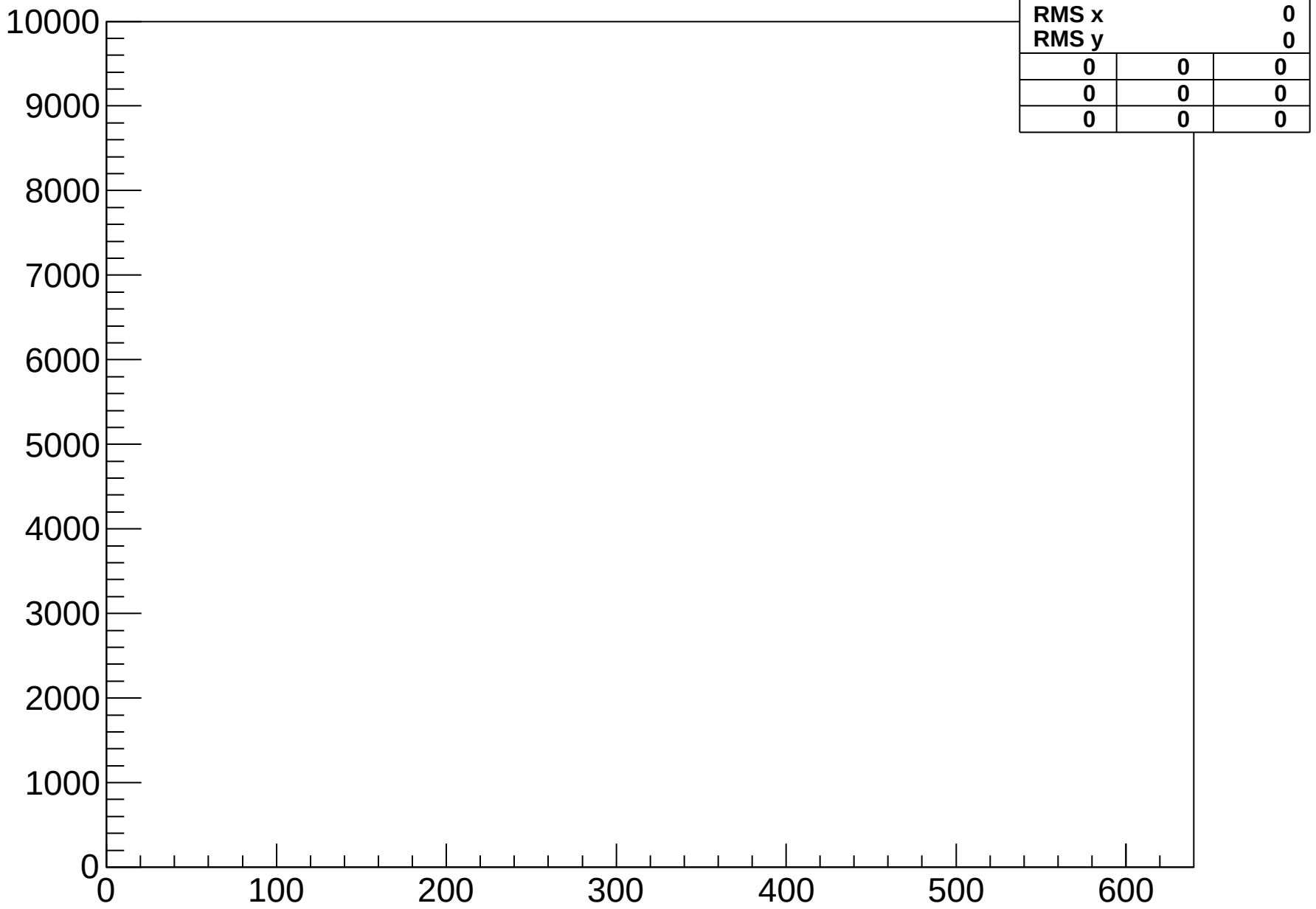
baselinesamples-fpga-4-hyb-2-sample-1



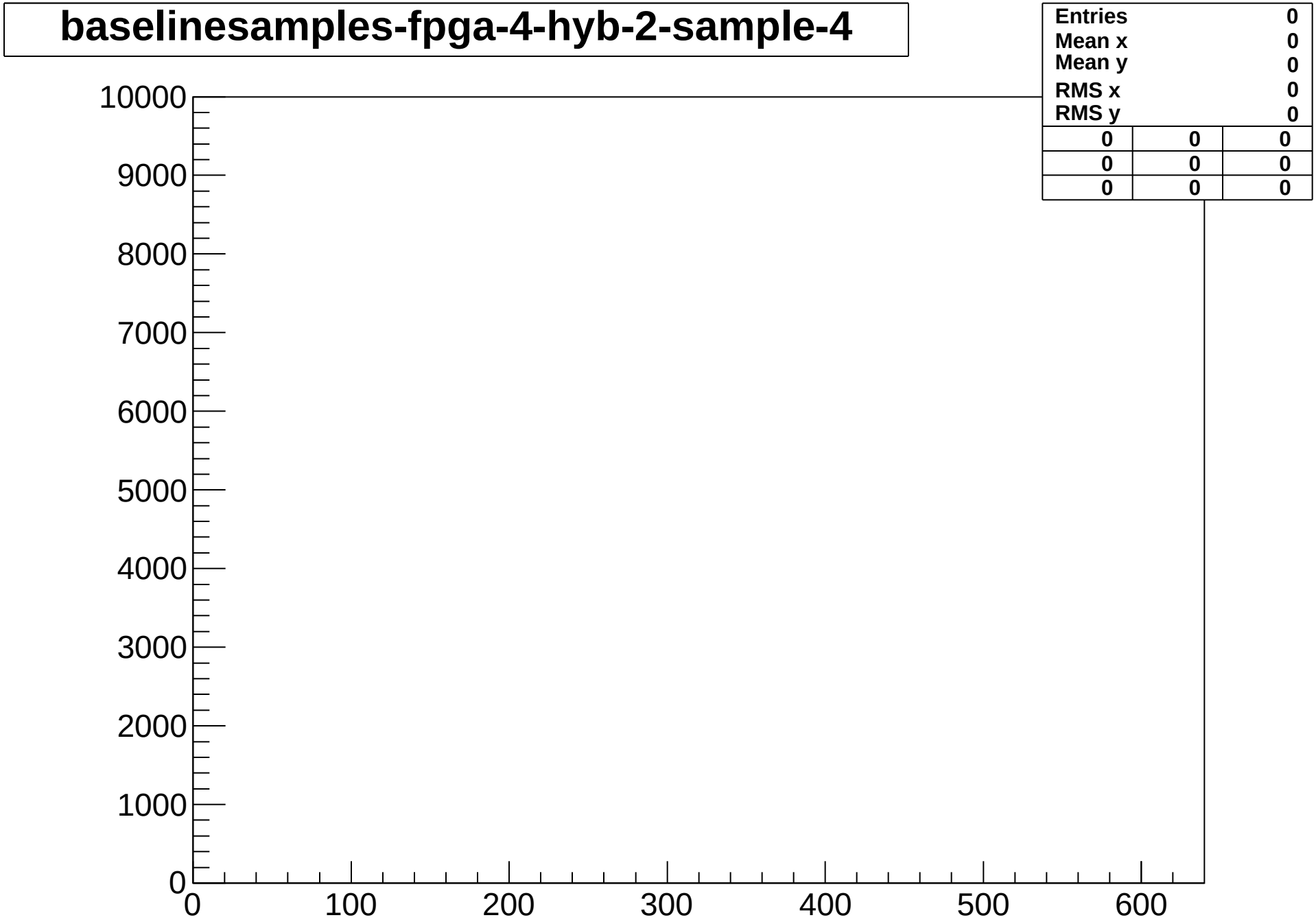
baselinesamples-fpga-4-hyb-2-sample-2



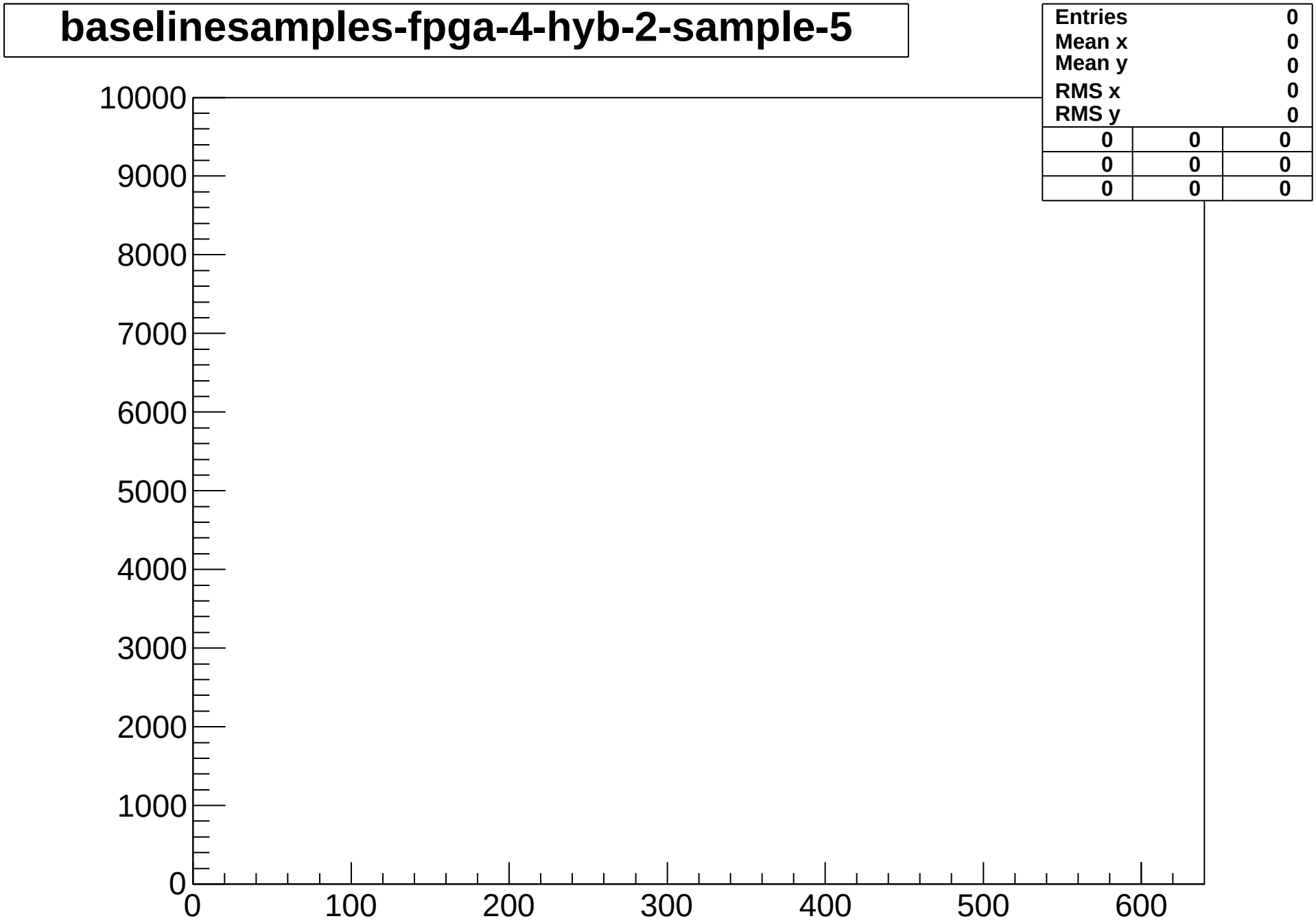
baselinesamples-fpga-4-hyb-2-sample-3

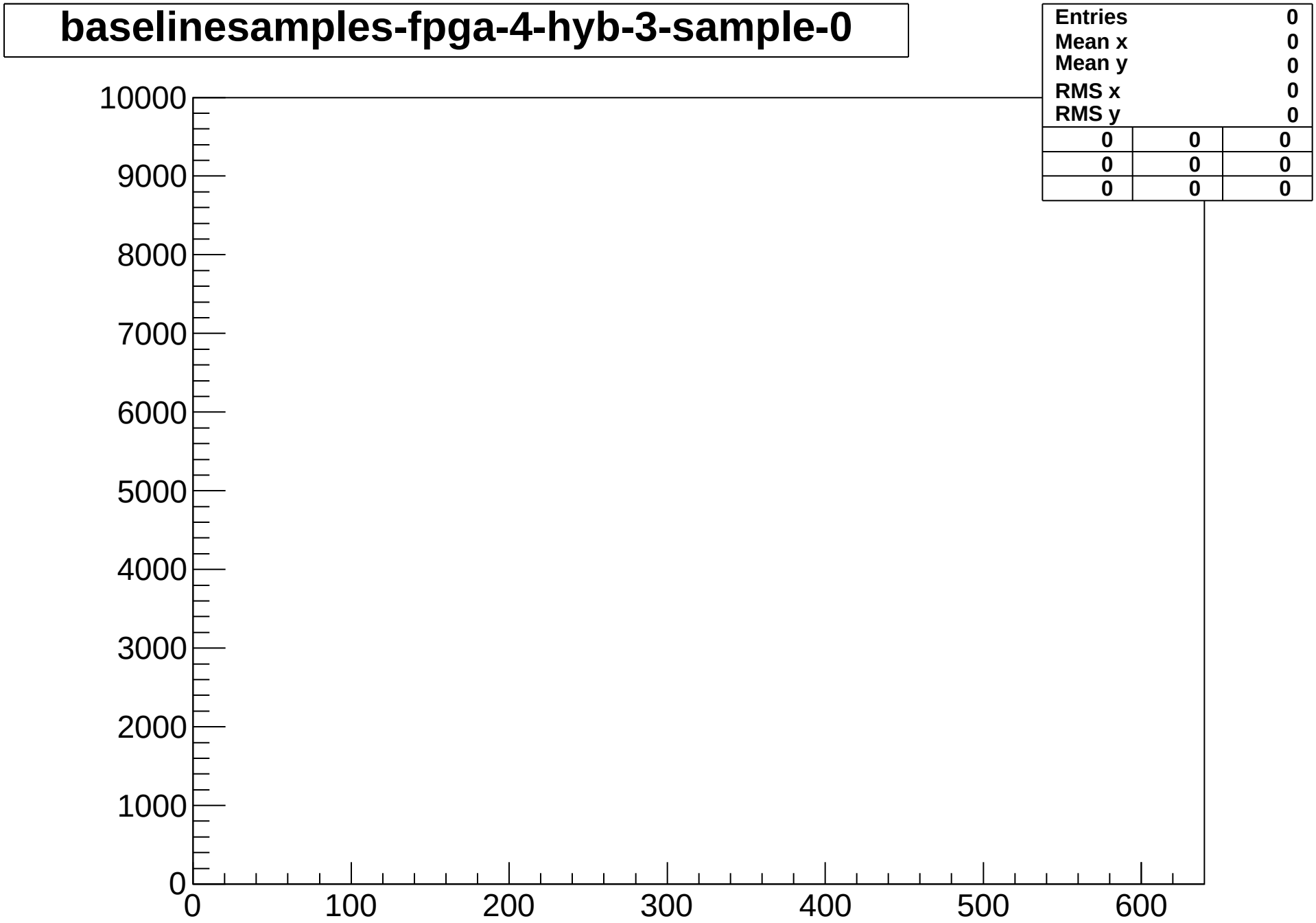


baselinesamples-fpga-4-hyb-2-sample-4

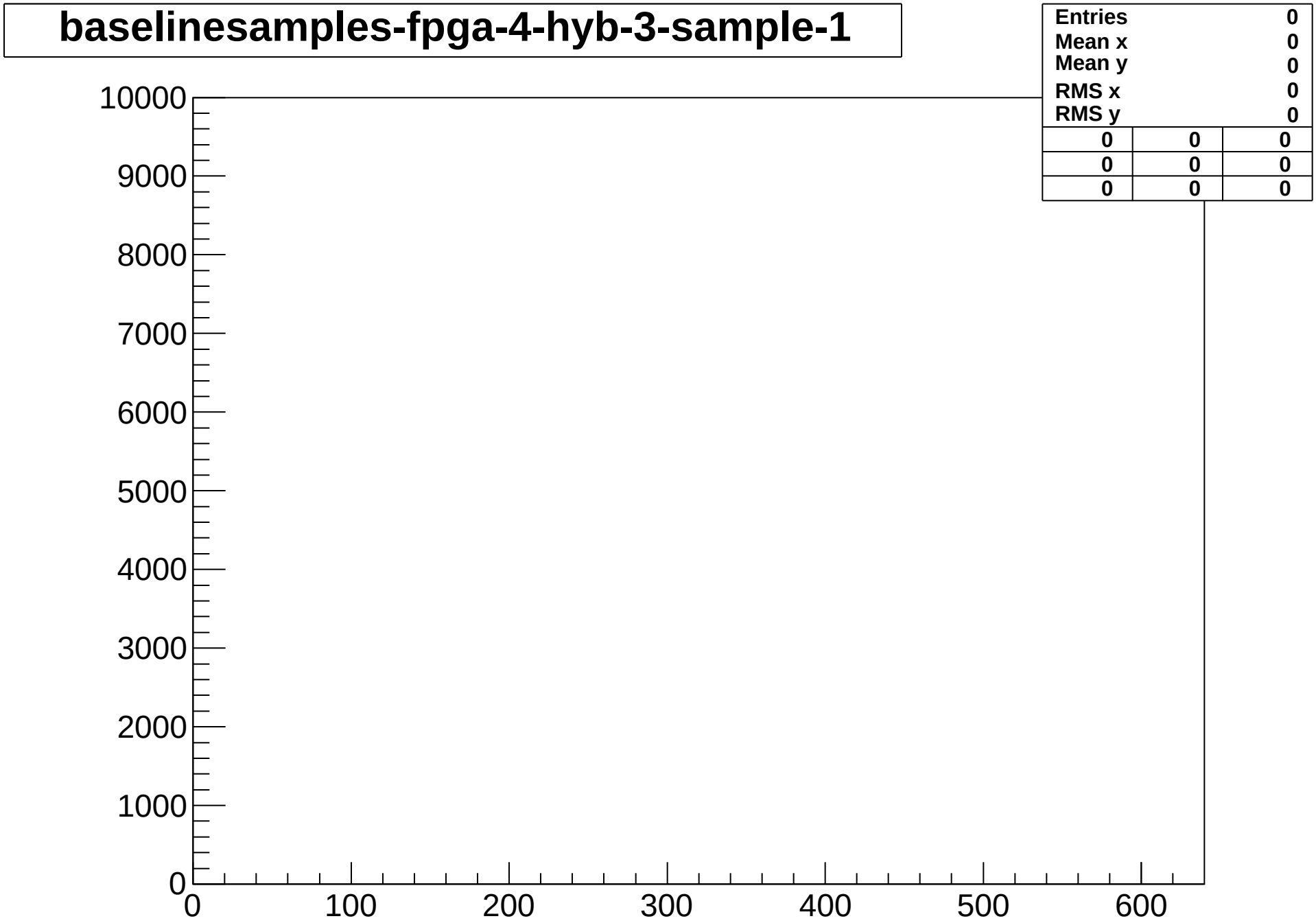


baselinesamples-fpga-4-hyb-2-sample-5

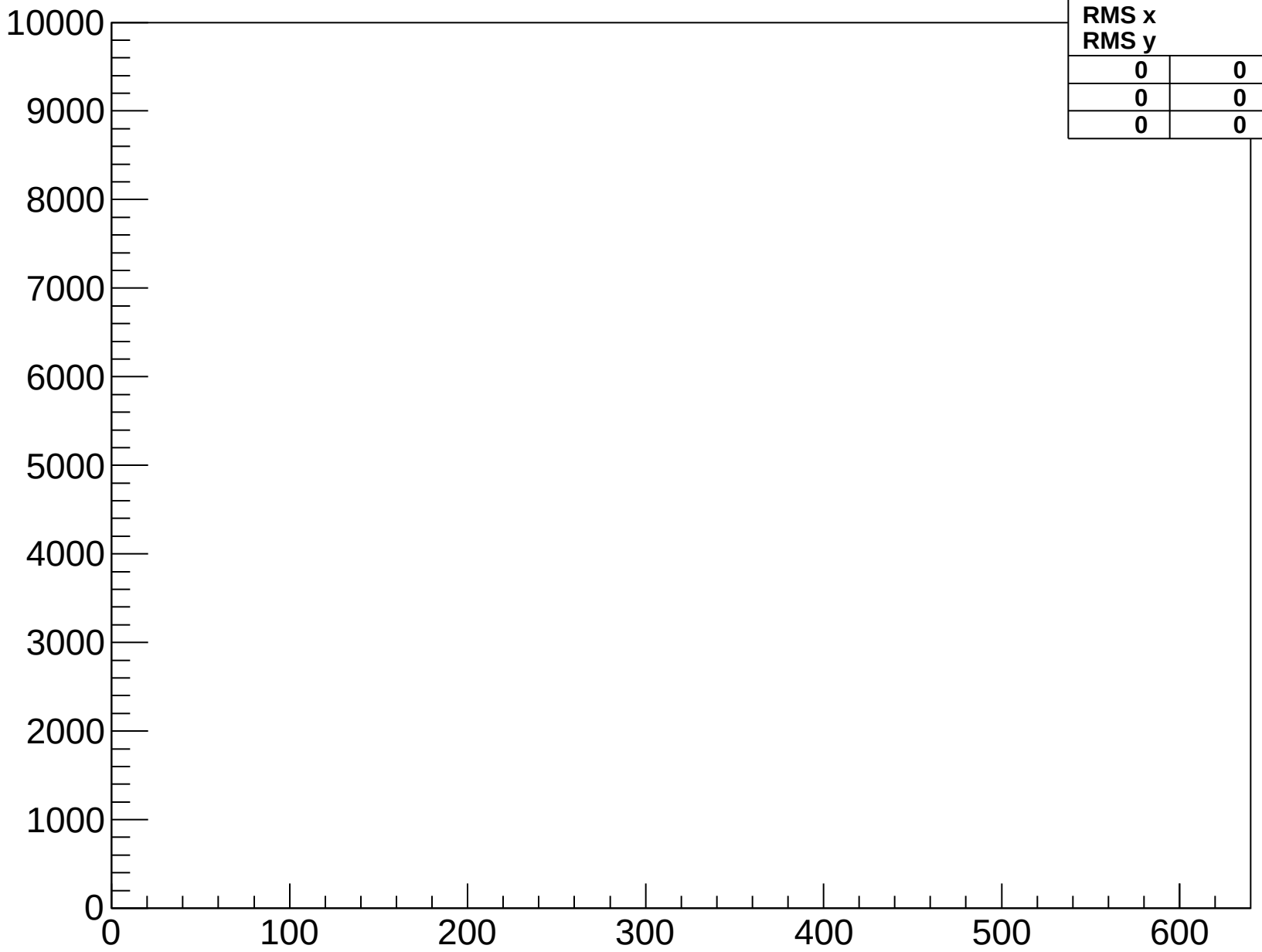



baselinesamples-fpga-4-hyb-3-sample-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

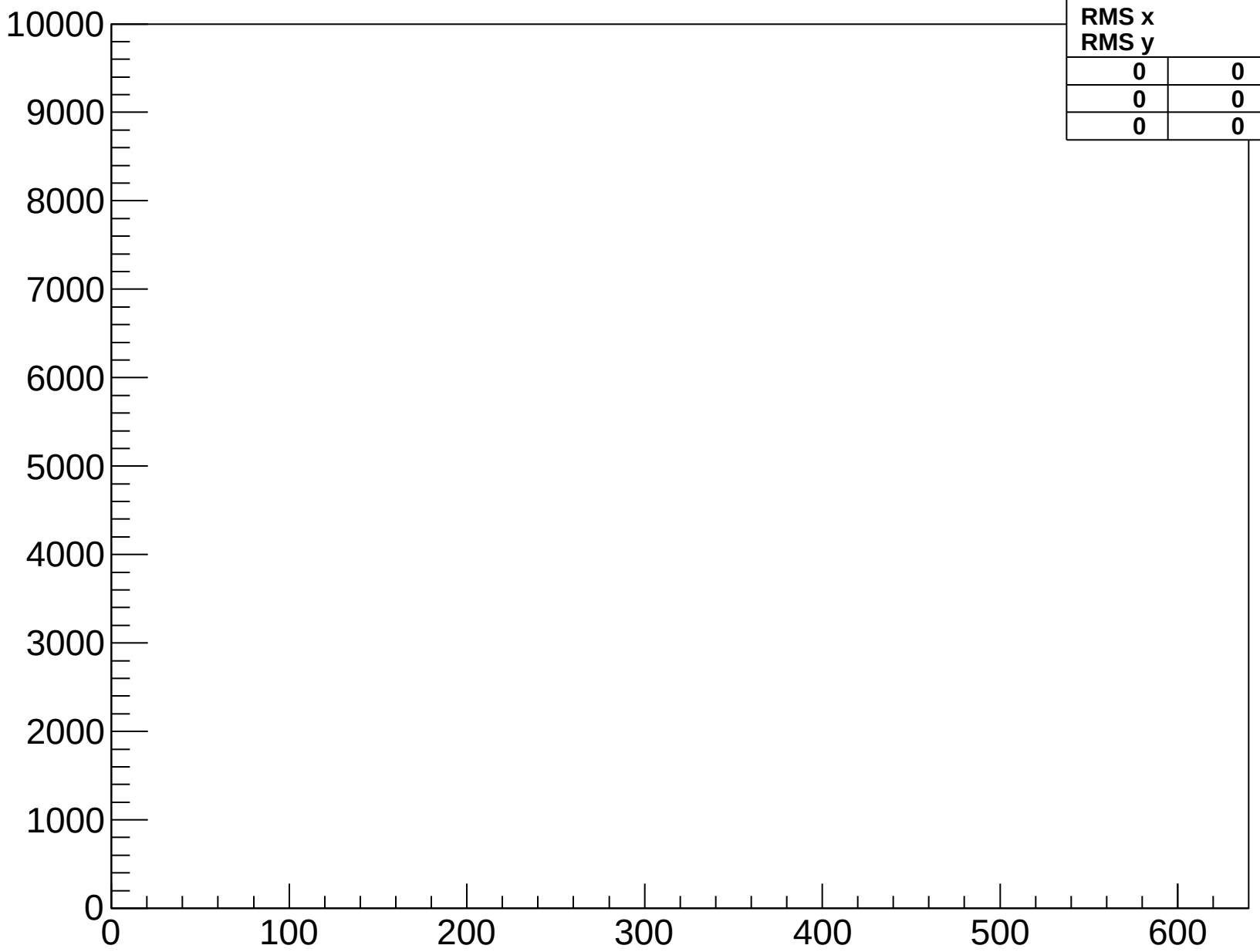
baselinesamples-fpga-4-hyb-3-sample-1



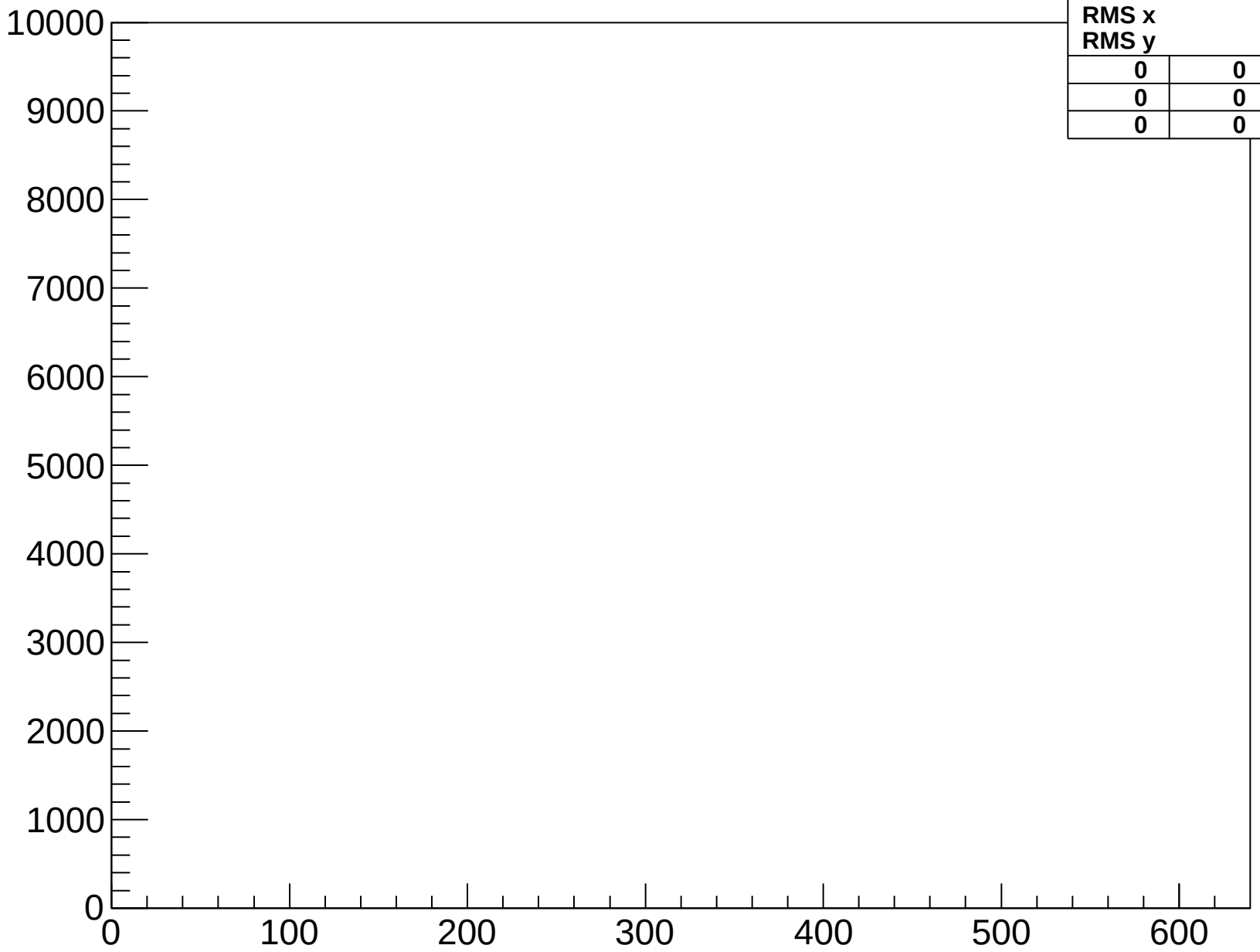
baselinesamples-fpga-4-hyb-3-sample-2



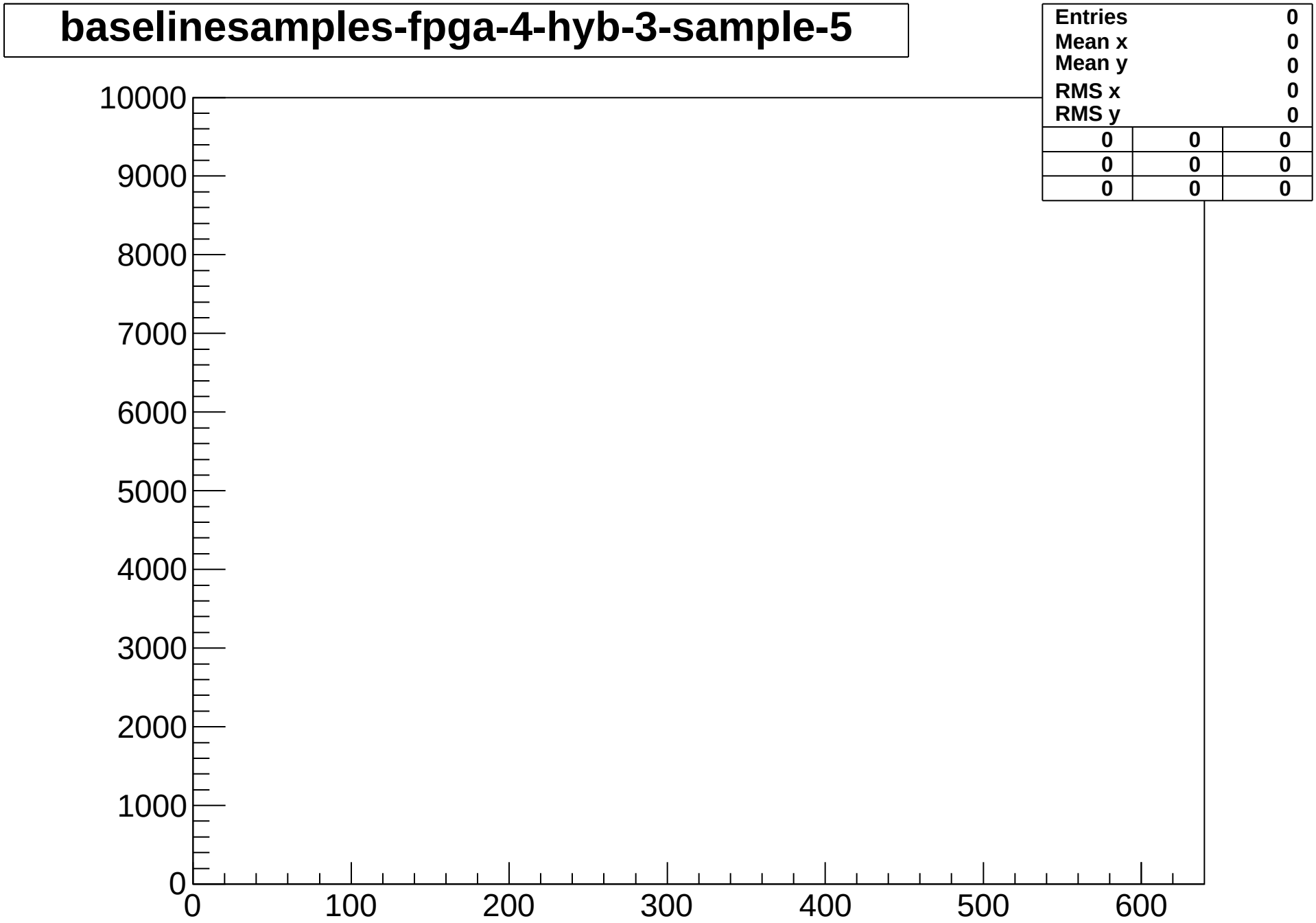
baselinesamples-fpga-4-hyb-3-sample-3



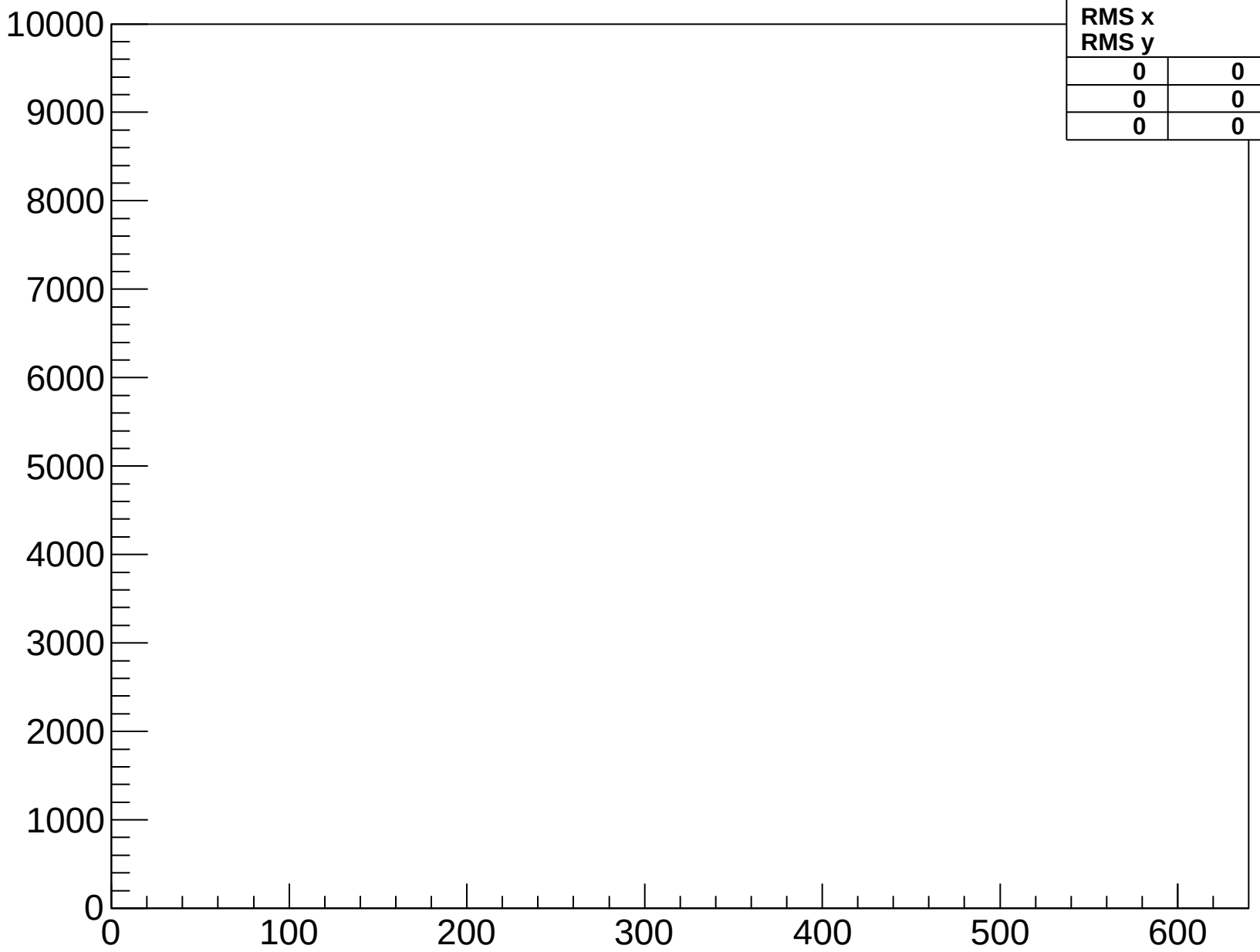
baselinesamples-fpga-4-hyb-3-sample-4



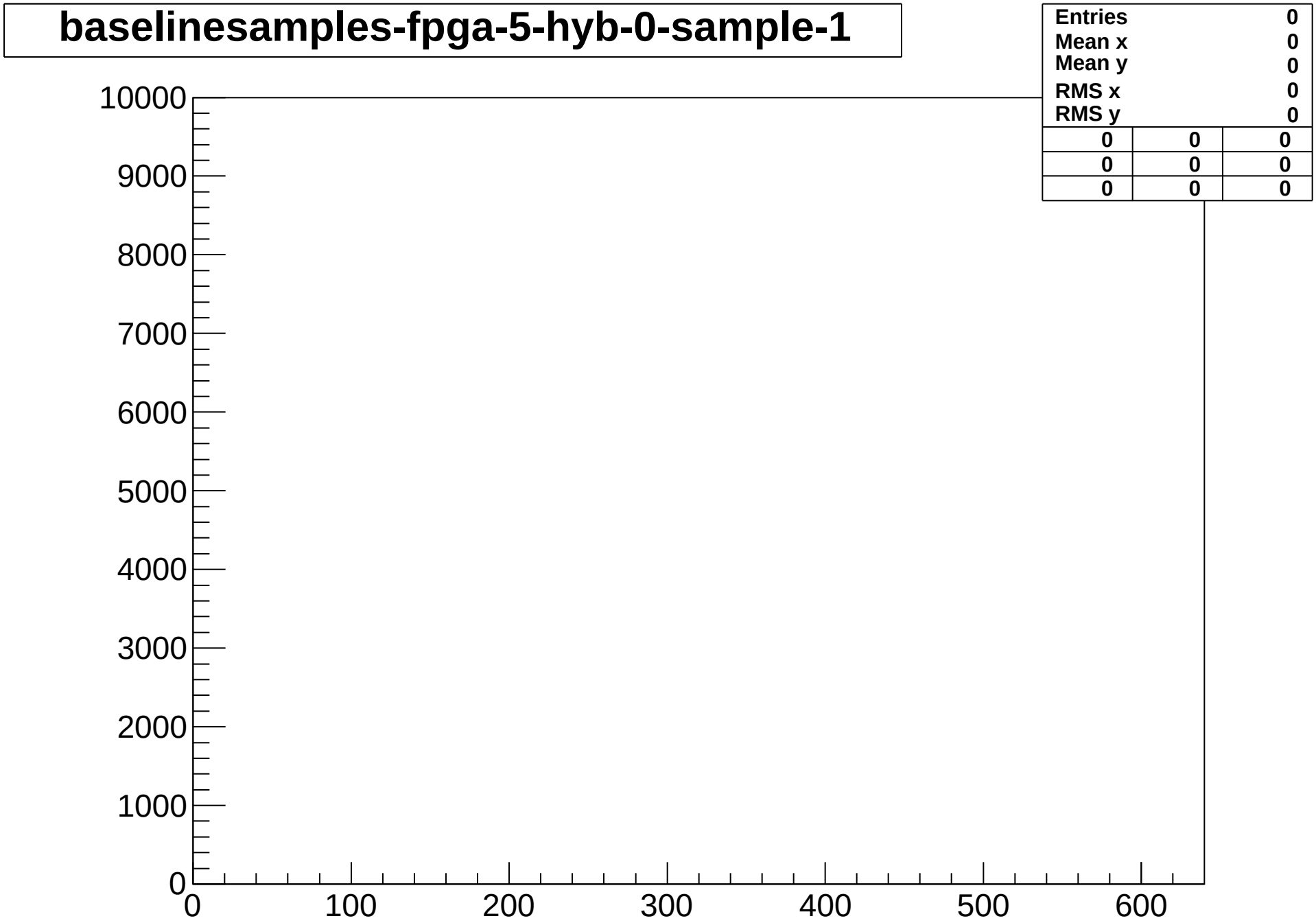
baselinesamples-fpga-4-hyb-3-sample-5



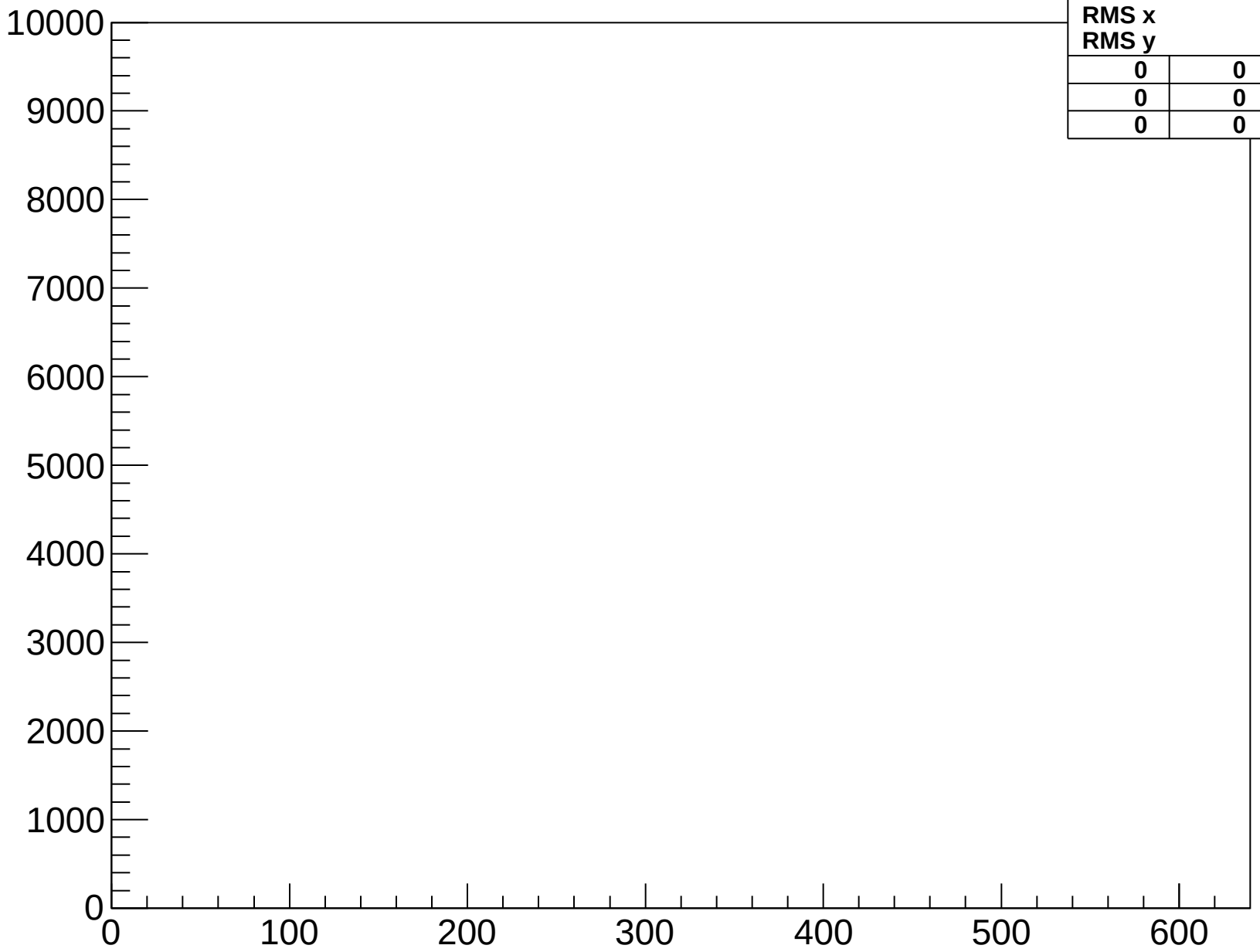
baselinesamples-fpga-5-hyb-0-sample-0



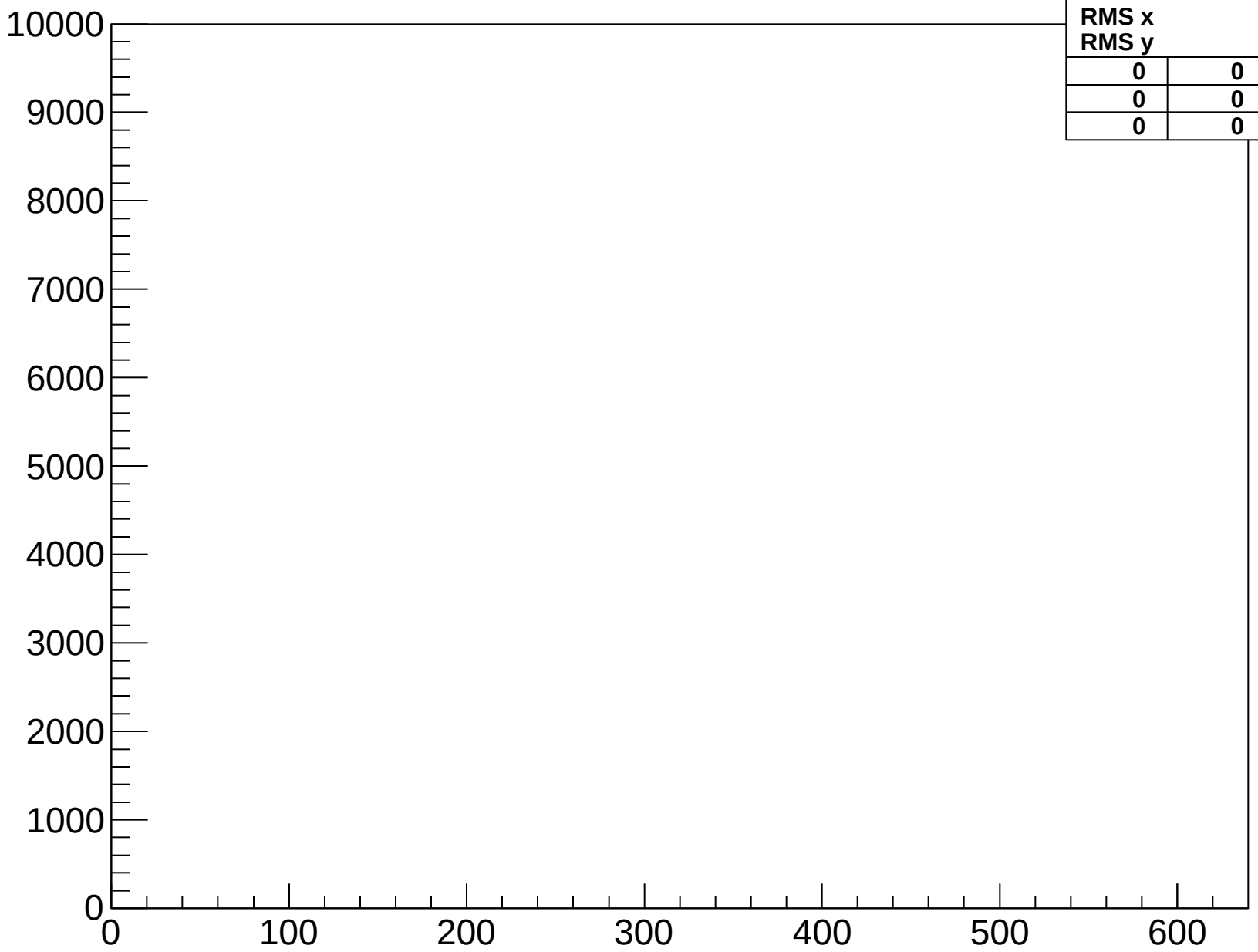
baselinesamples-fpga-5-hyb-0-sample-1



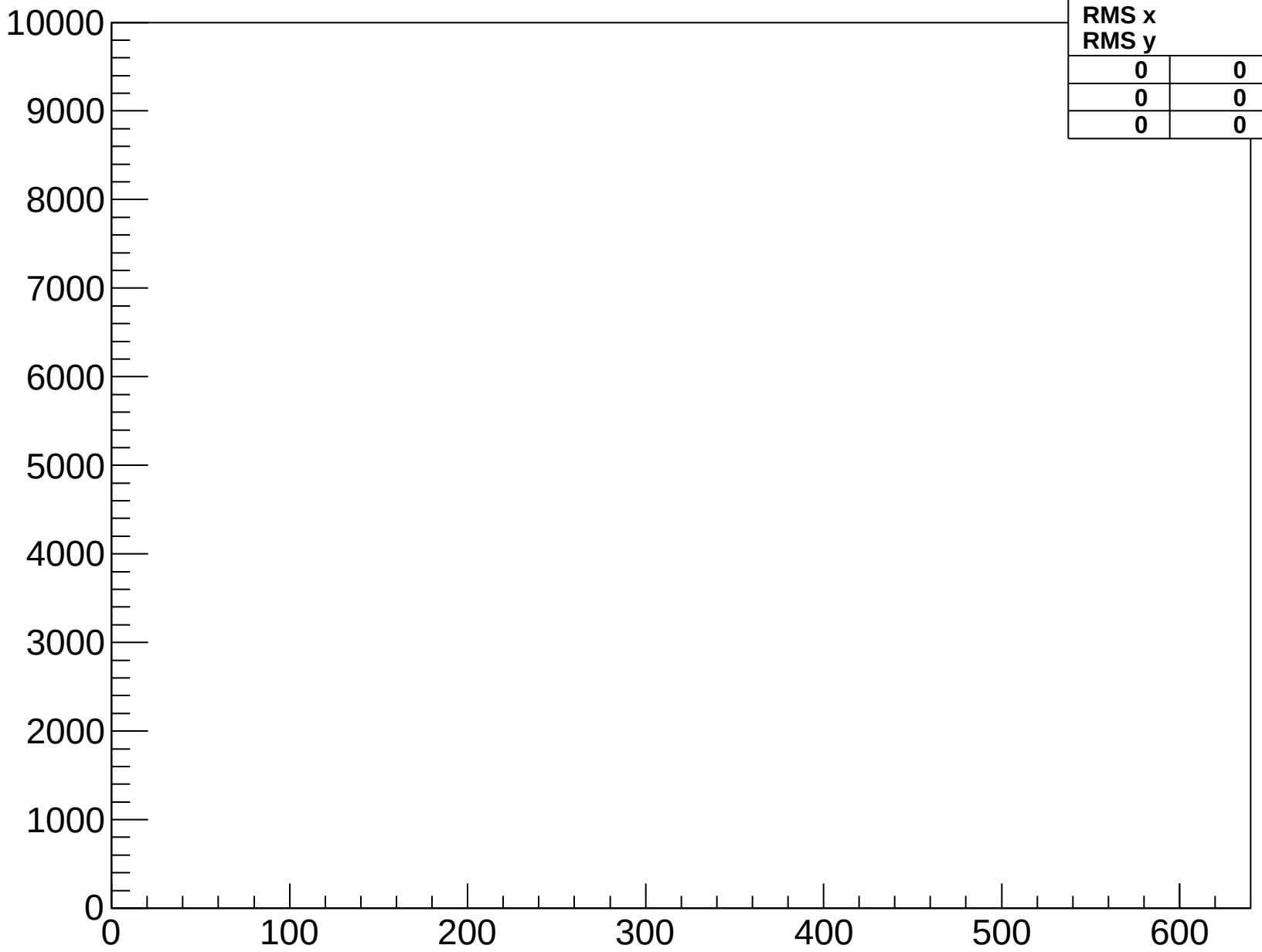
baselinesamples-fpga-5-hyb-0-sample-2



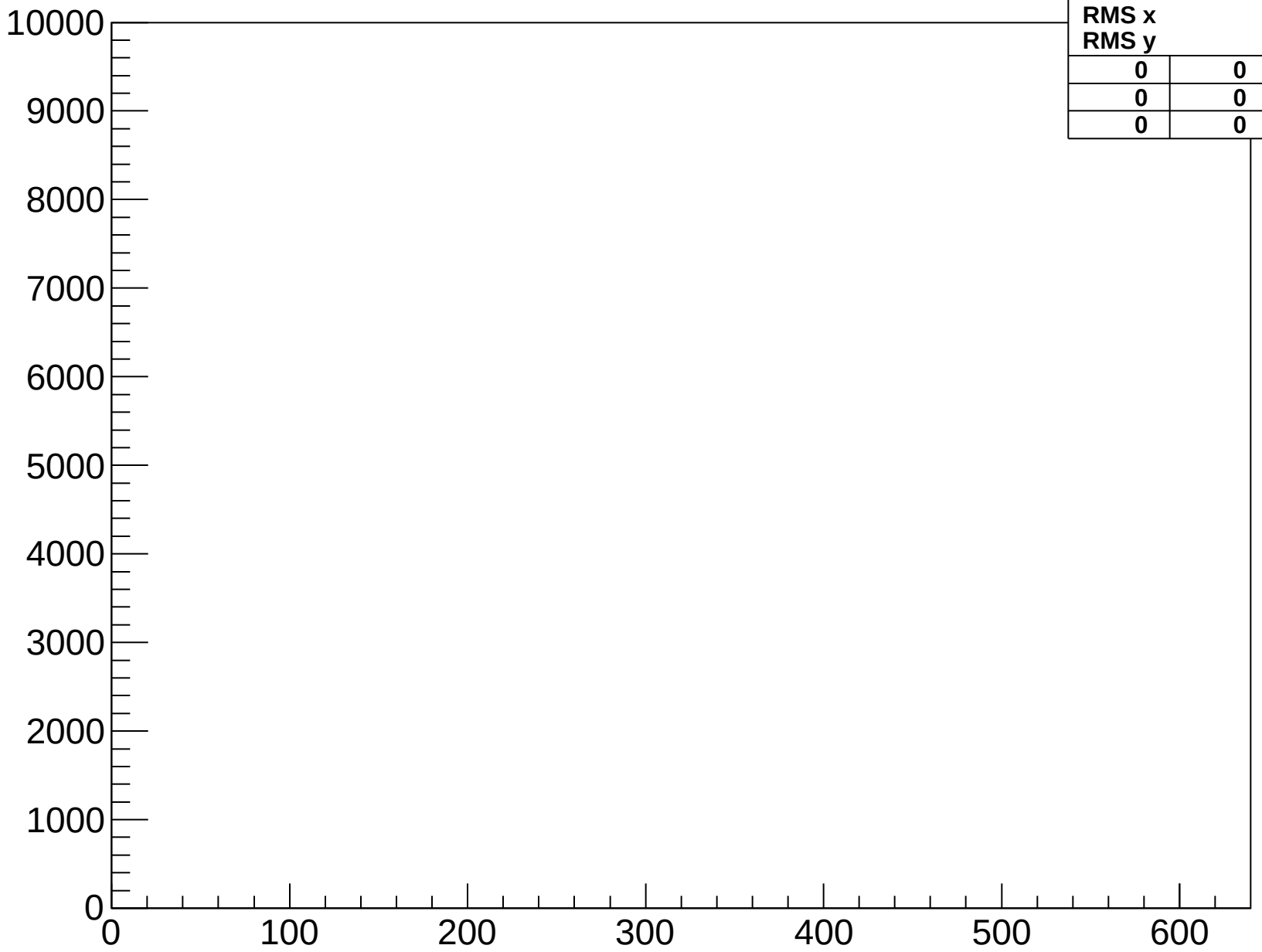
baselinesamples-fpga-5-hyb-0-sample-3



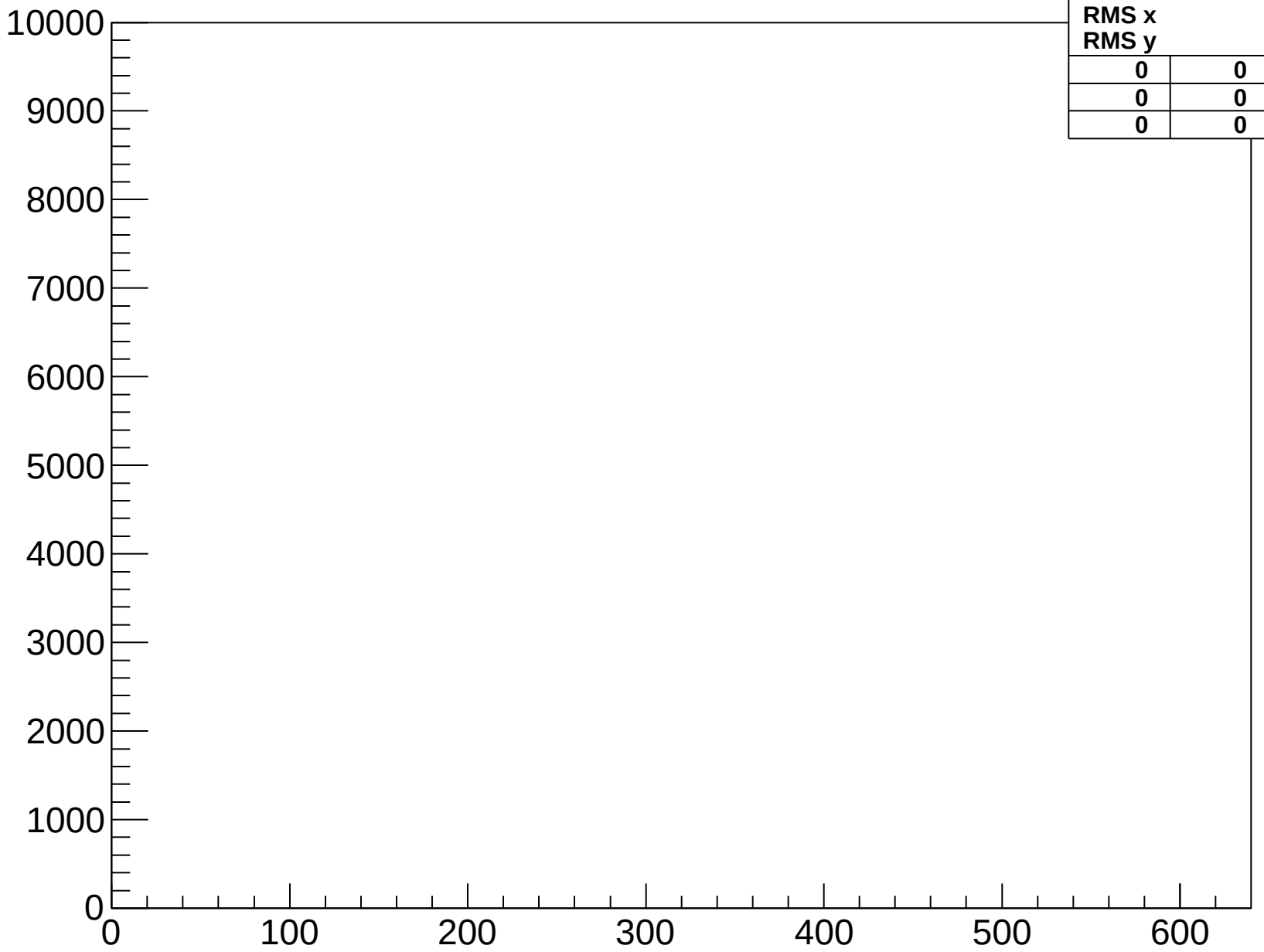
baselinesamples-fpga-5-hyb-0-sample-4

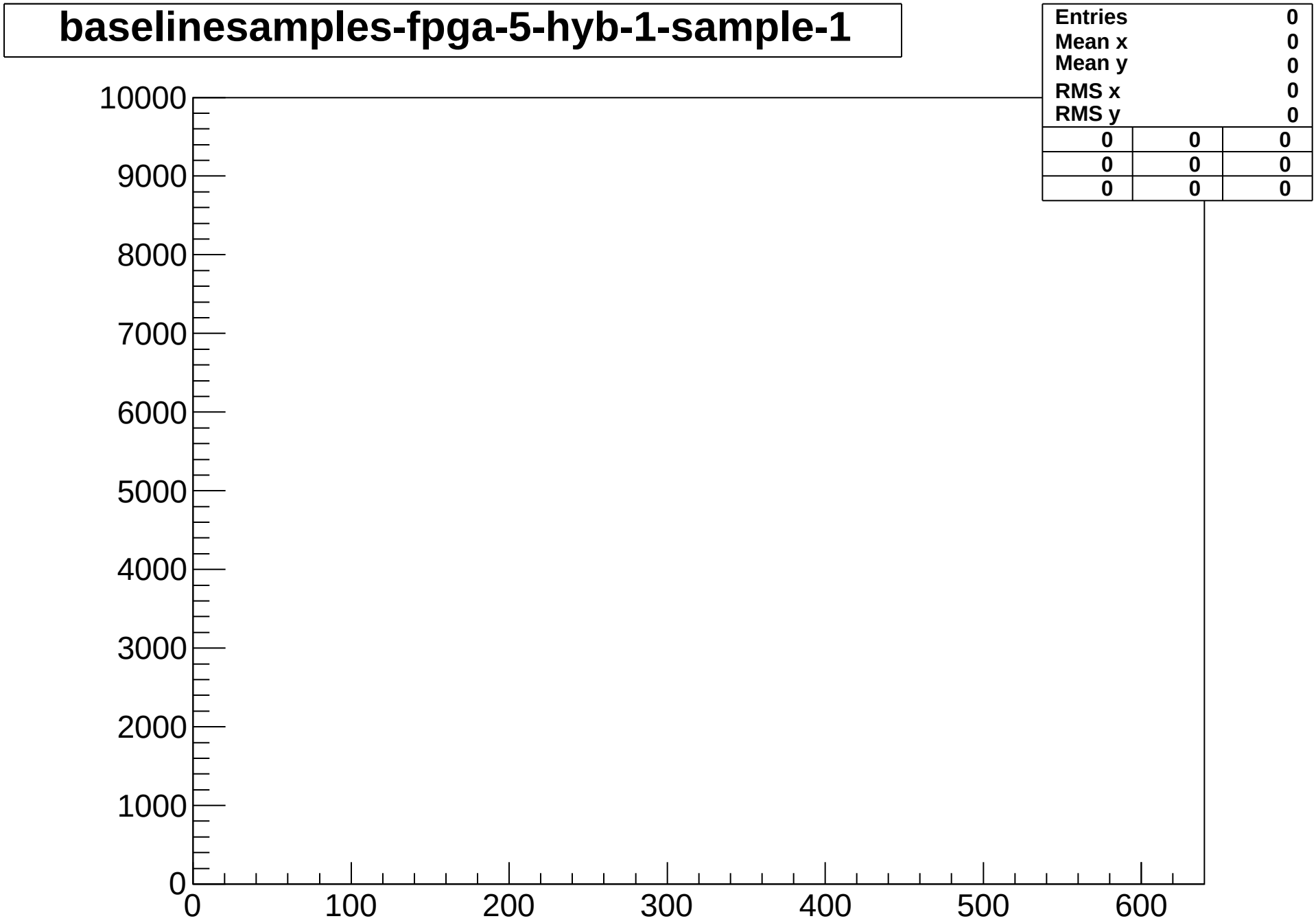


baselinesamples-fpga-5-hyb-0-sample-5

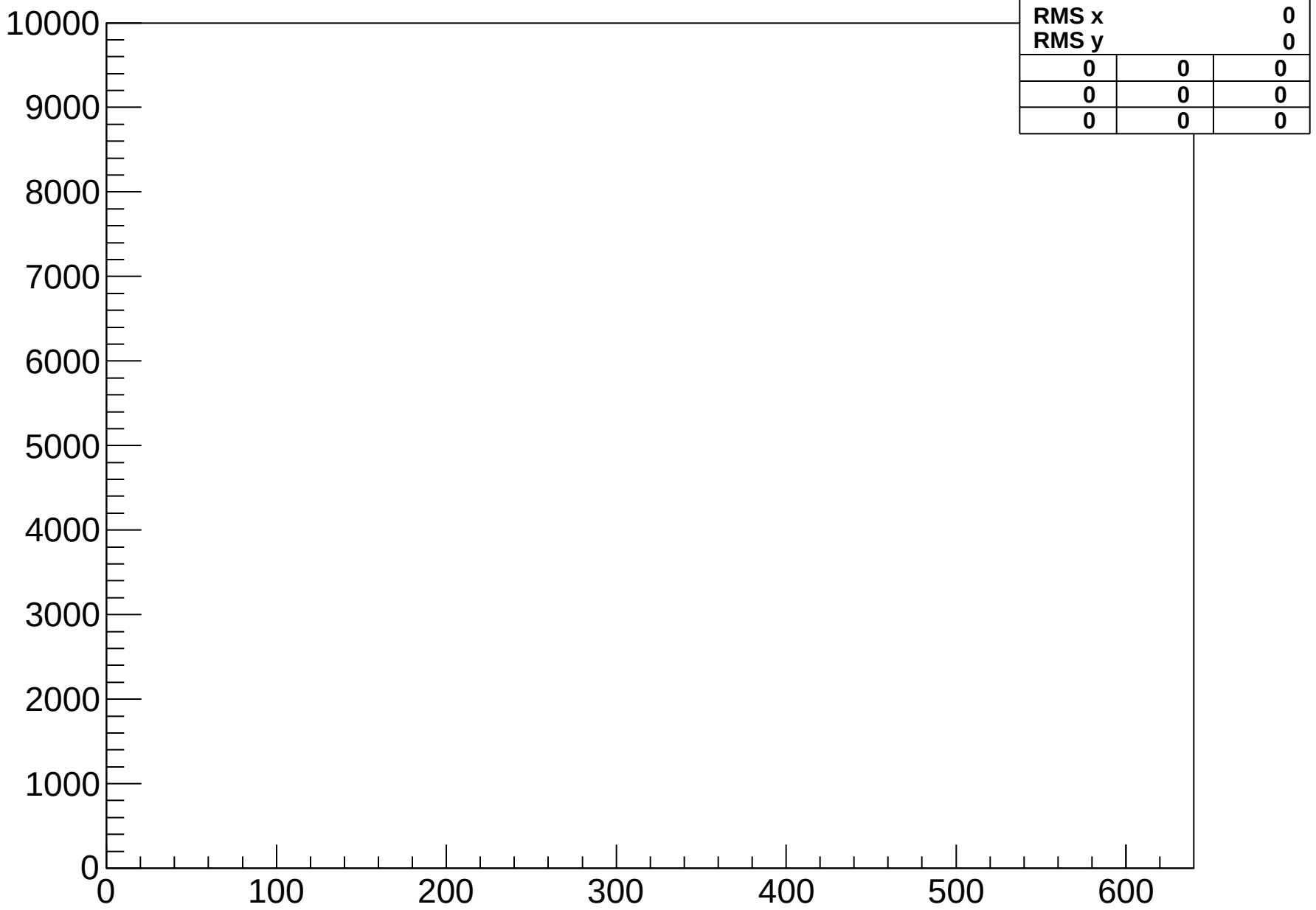


baselinesamples-fpga-5-hyb-1-sample-0

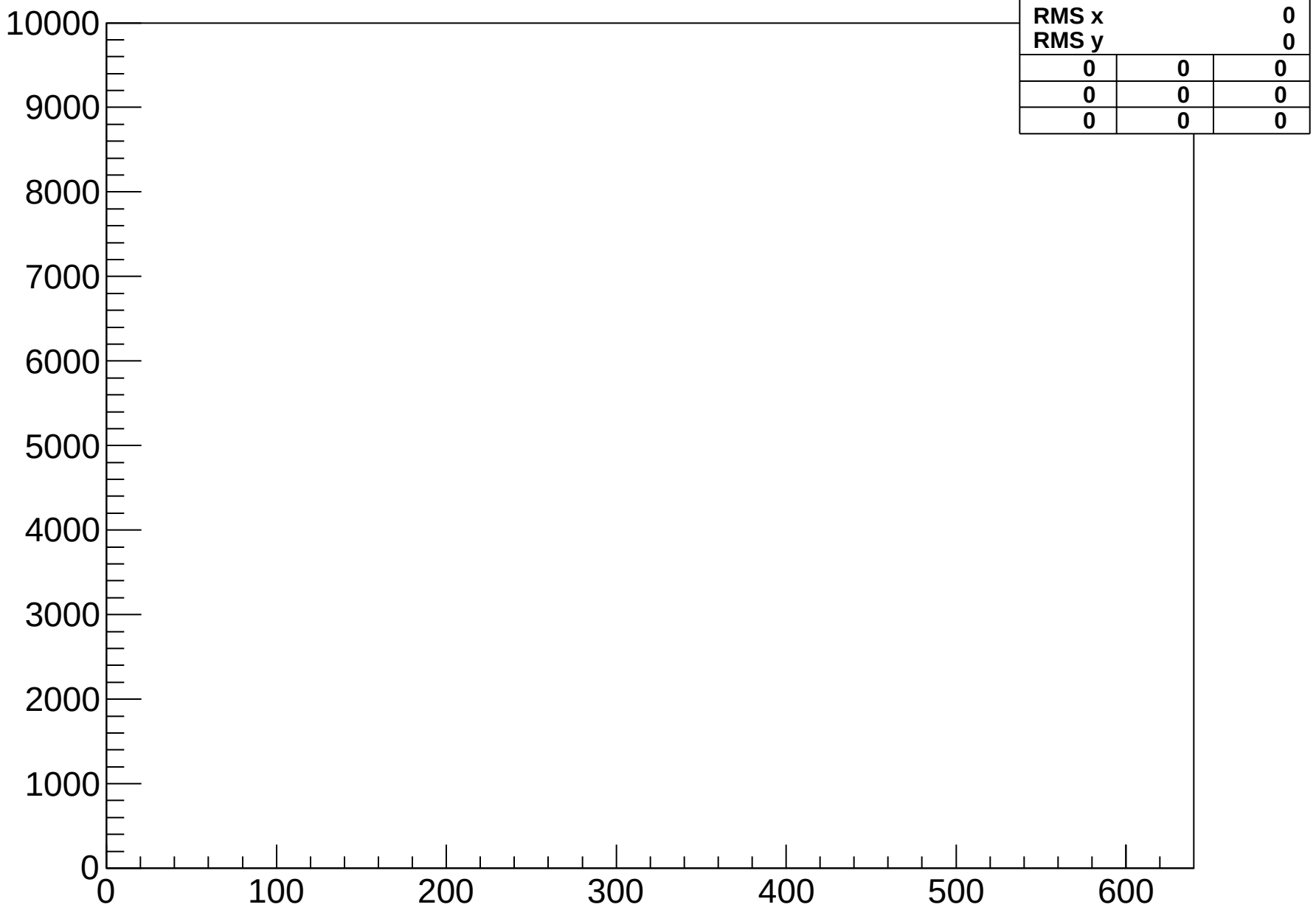



baselinesamples-fpga-5-hyb-1-sample-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

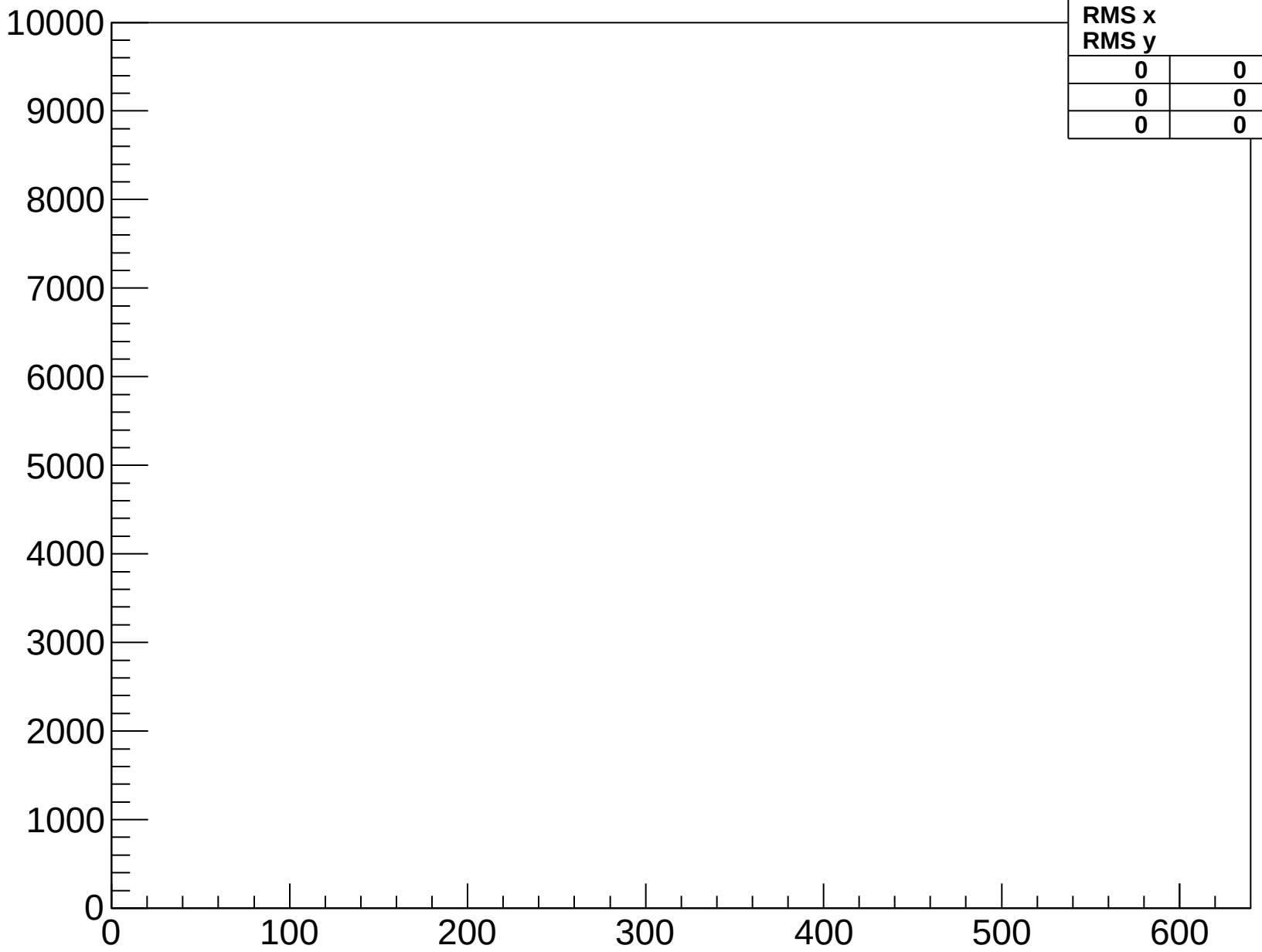
baselinesamples-fpga-5-hyb-1-sample-2



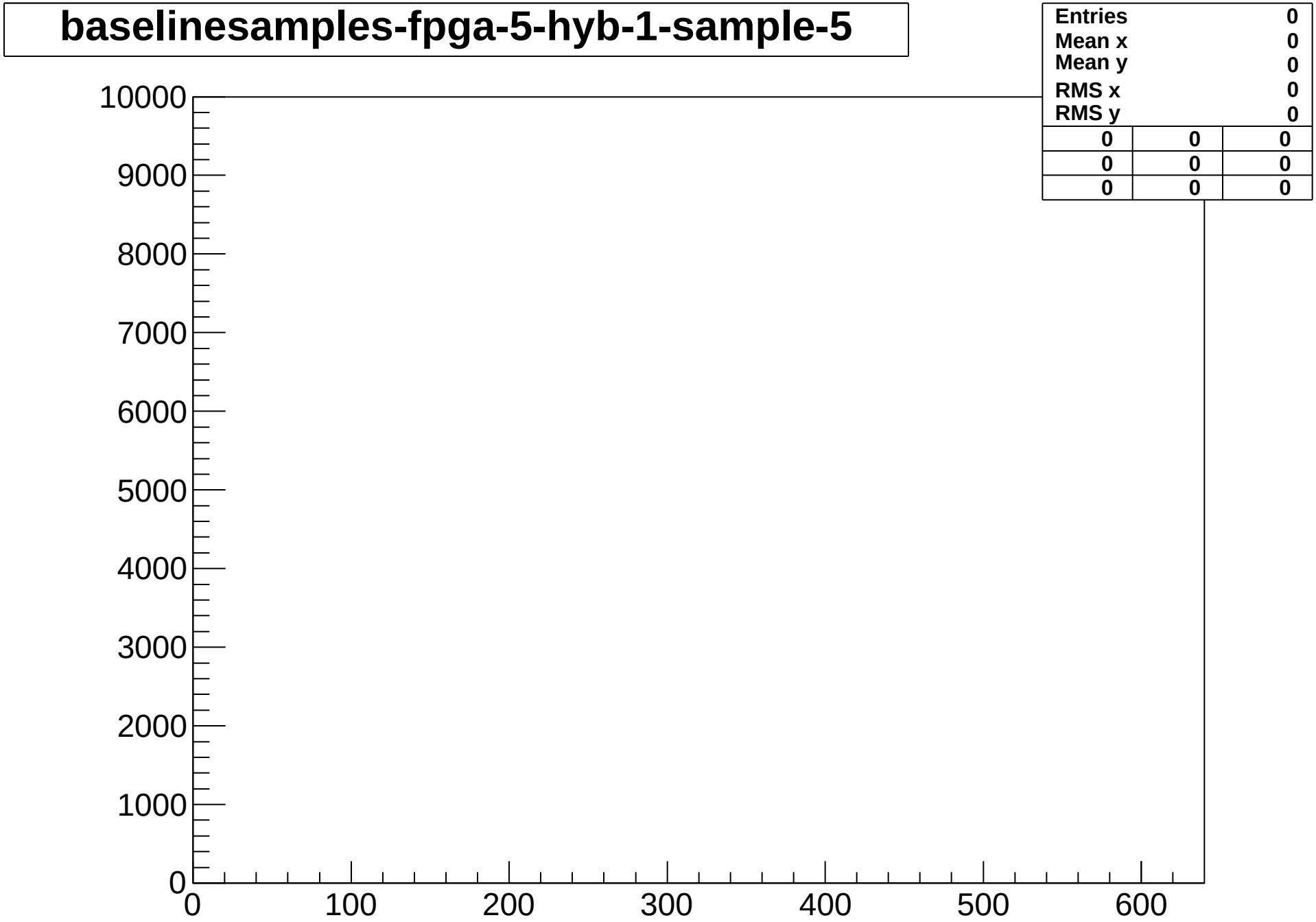
baselinesamples-fpga-5-hyb-1-sample-3



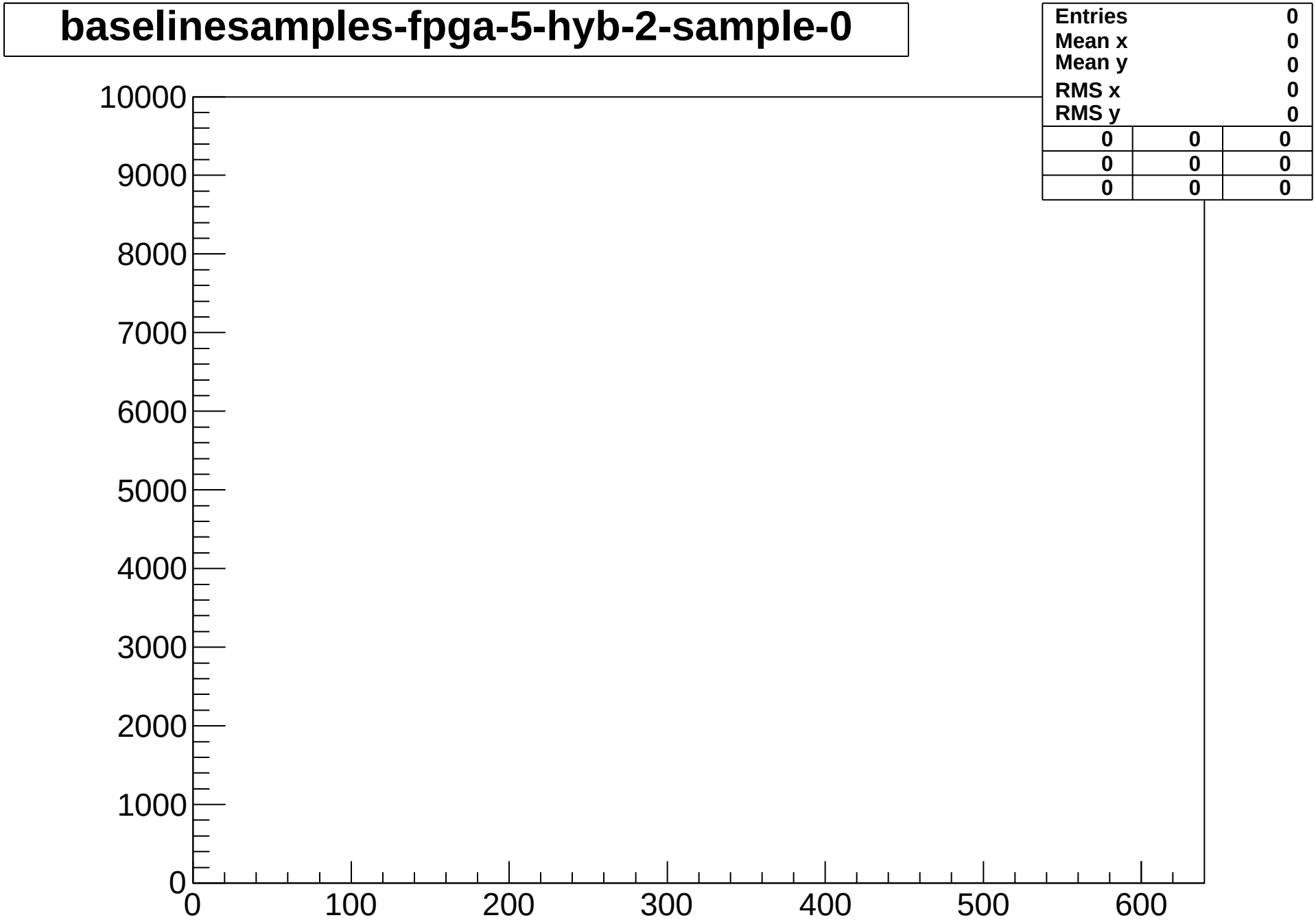
baselinesamples-fpga-5-hyb-1-sample-4

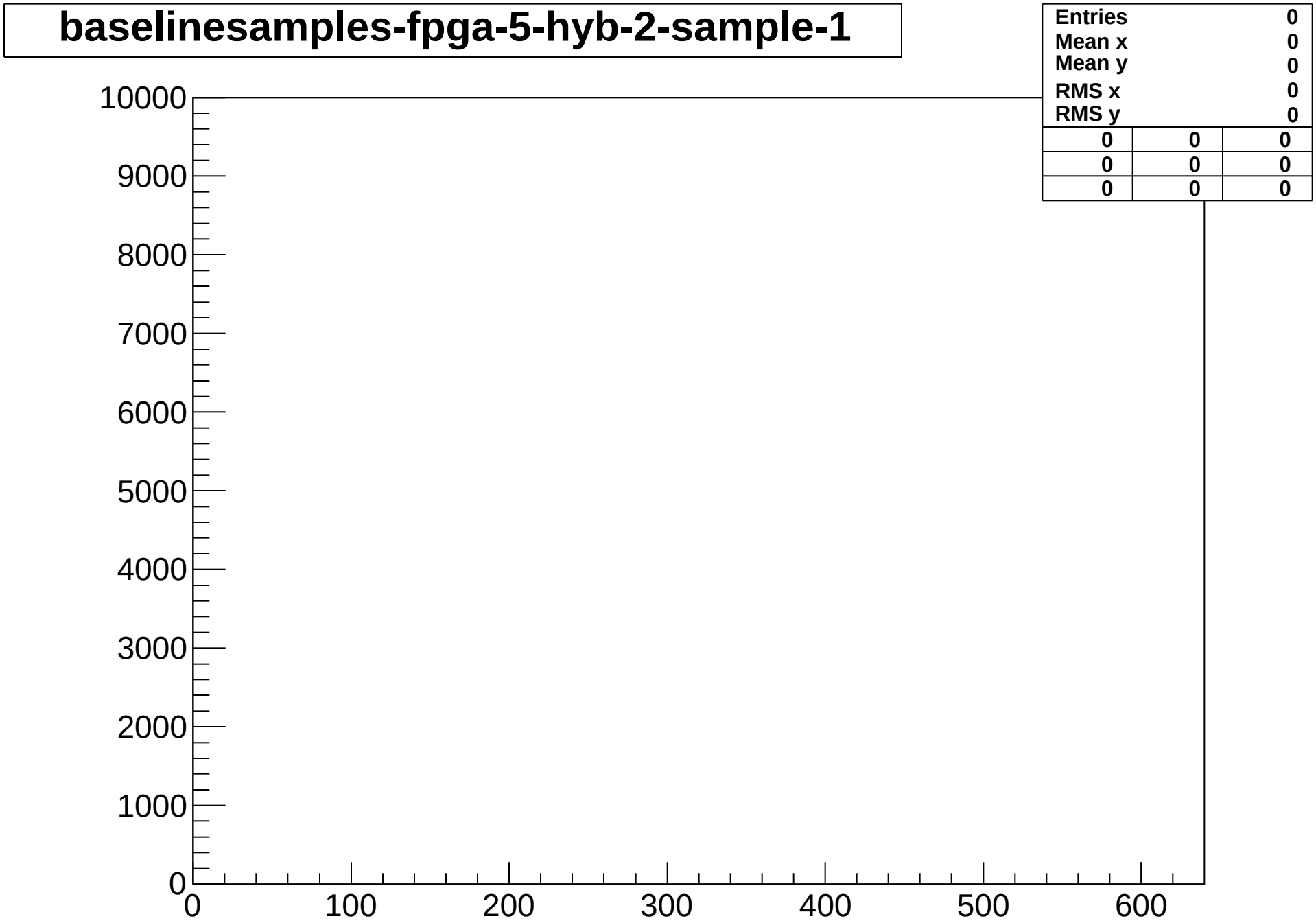


baselinesamples-fpga-5-hyb-1-sample-5

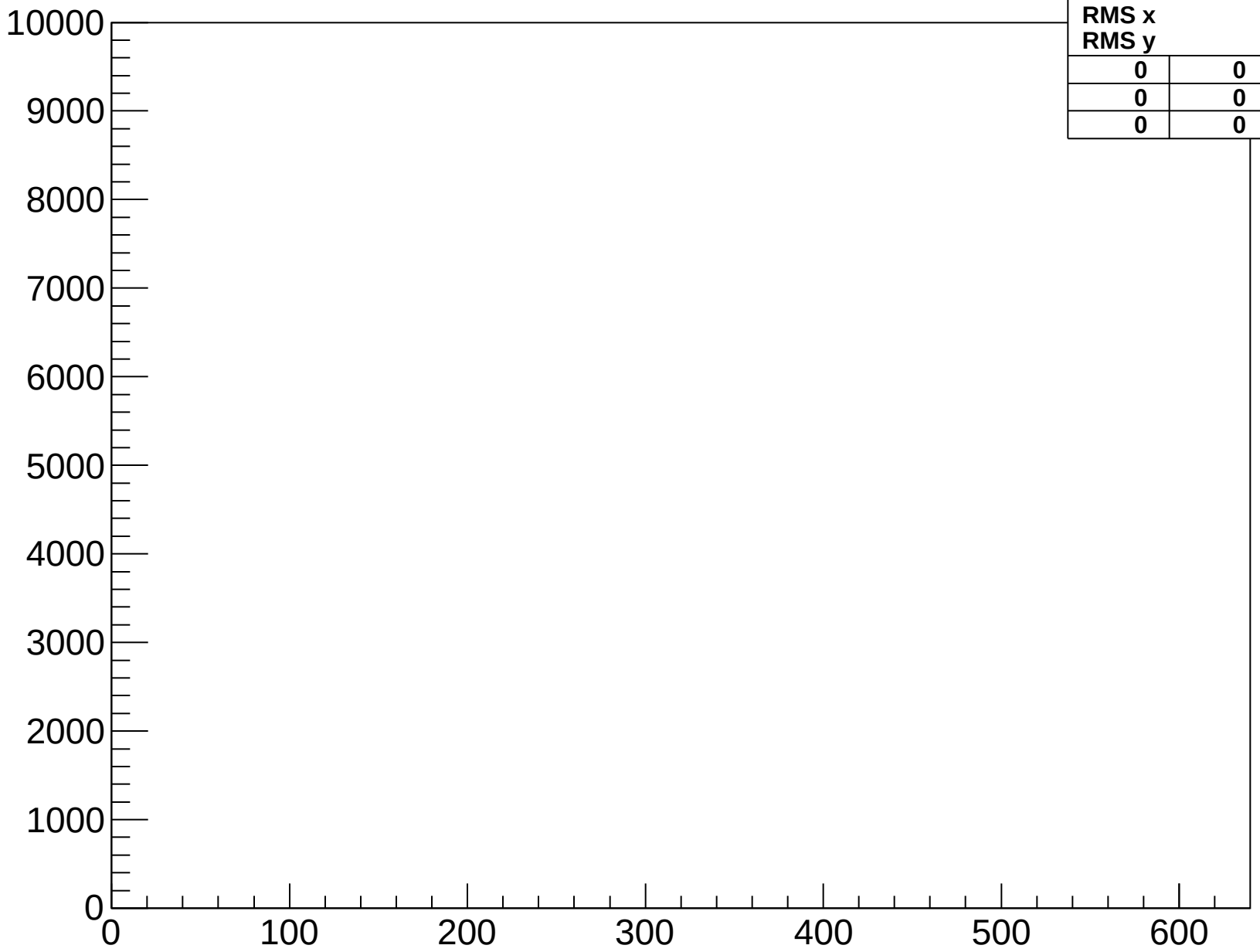


baselinesamples-fpga-5-hyb-2-sample-0

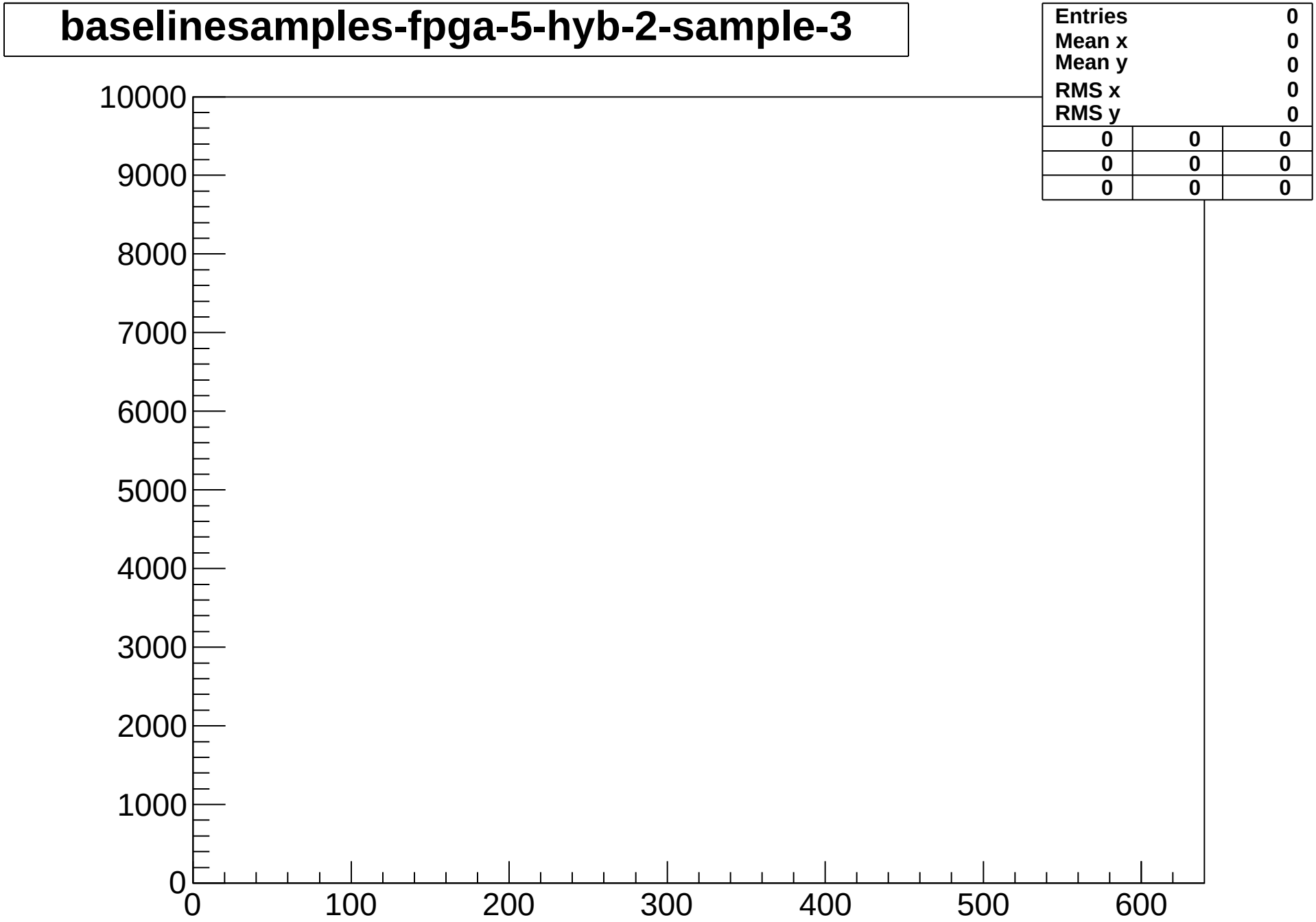



baselinesamples-fpga-5-hyb-2-sample-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

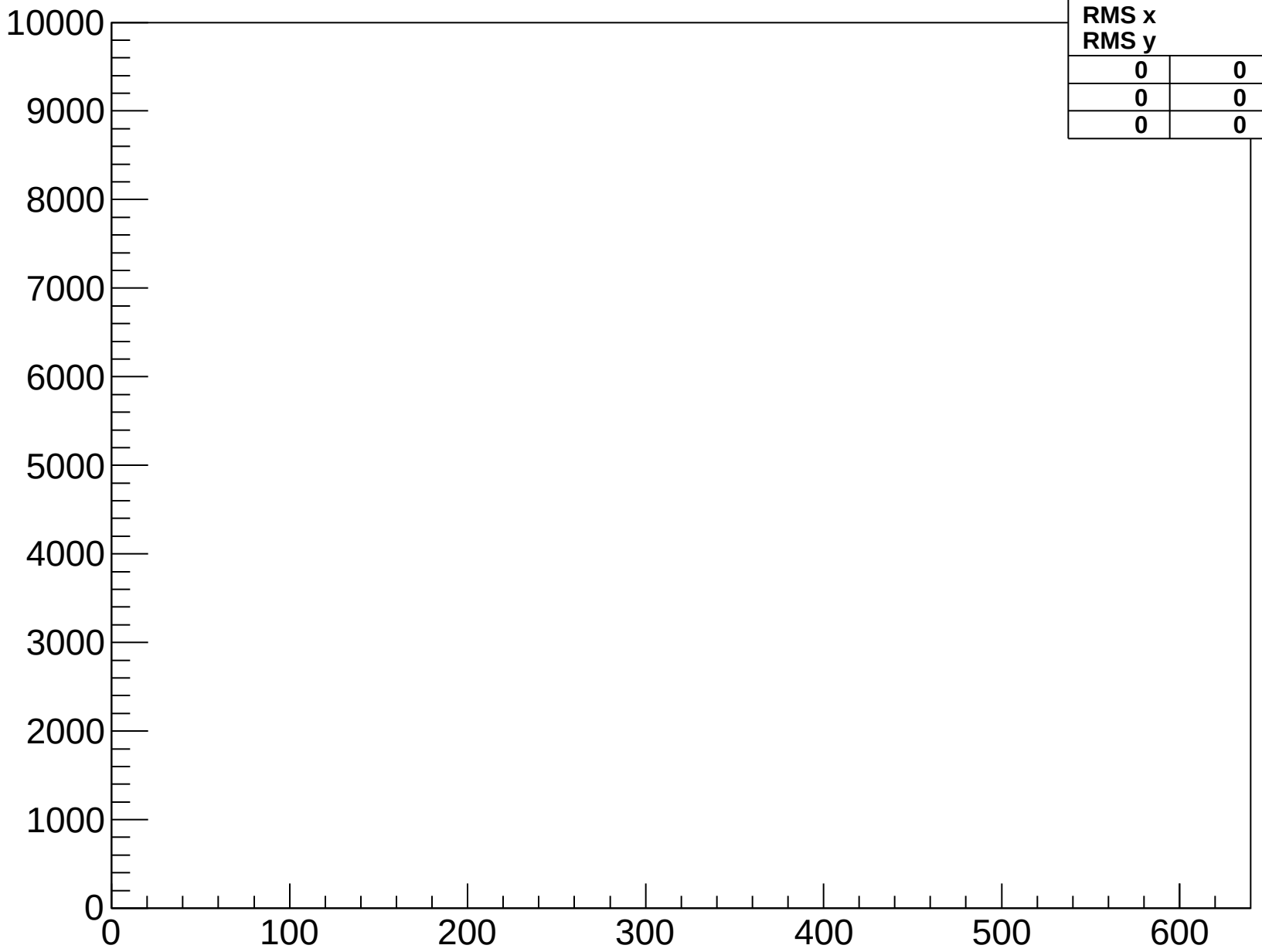
baselinesamples-fpga-5-hyb-2-sample-2



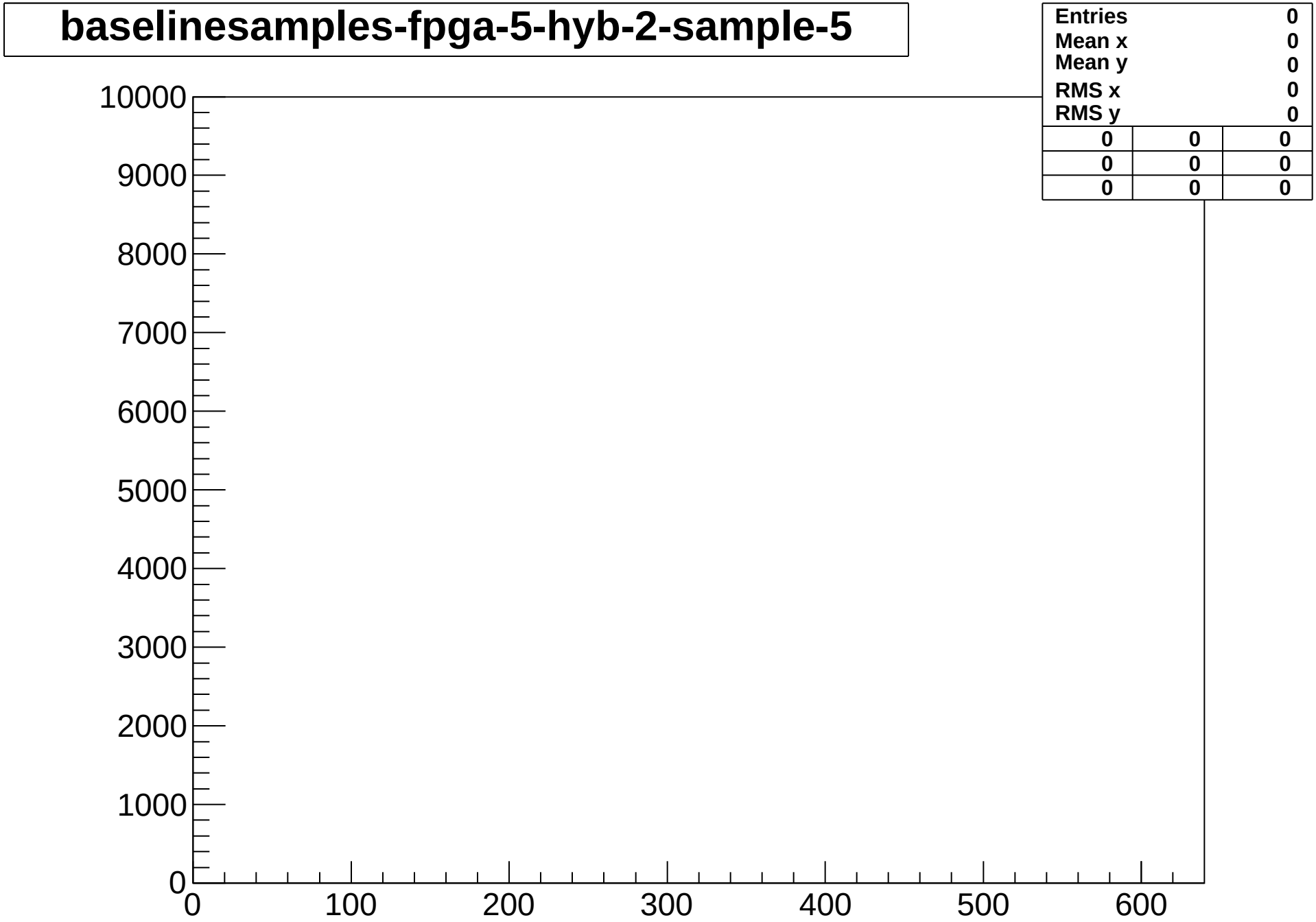
baselinesamples-fpga-5-hyb-2-sample-3



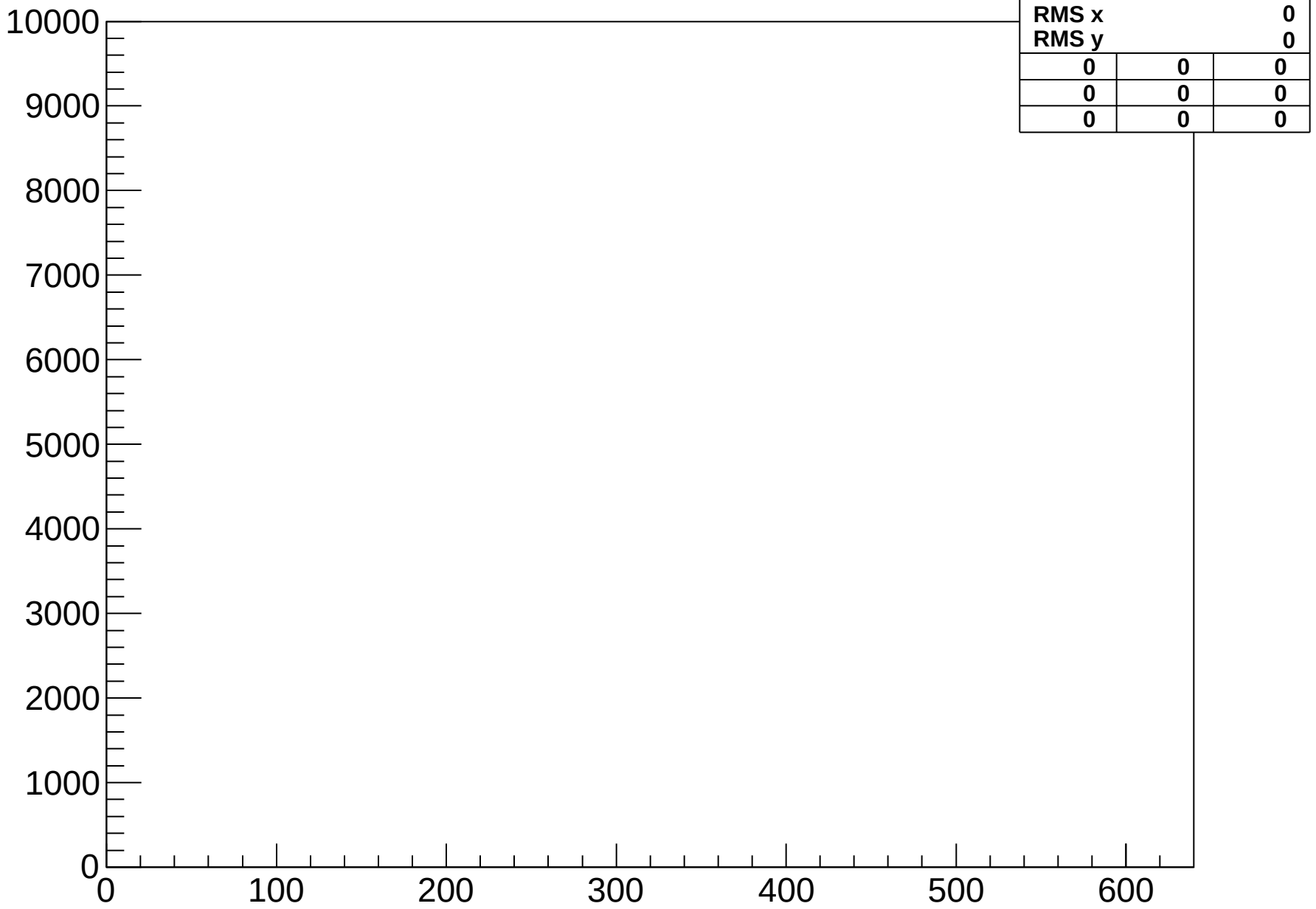
baselinesamples-fpga-5-hyb-2-sample-4



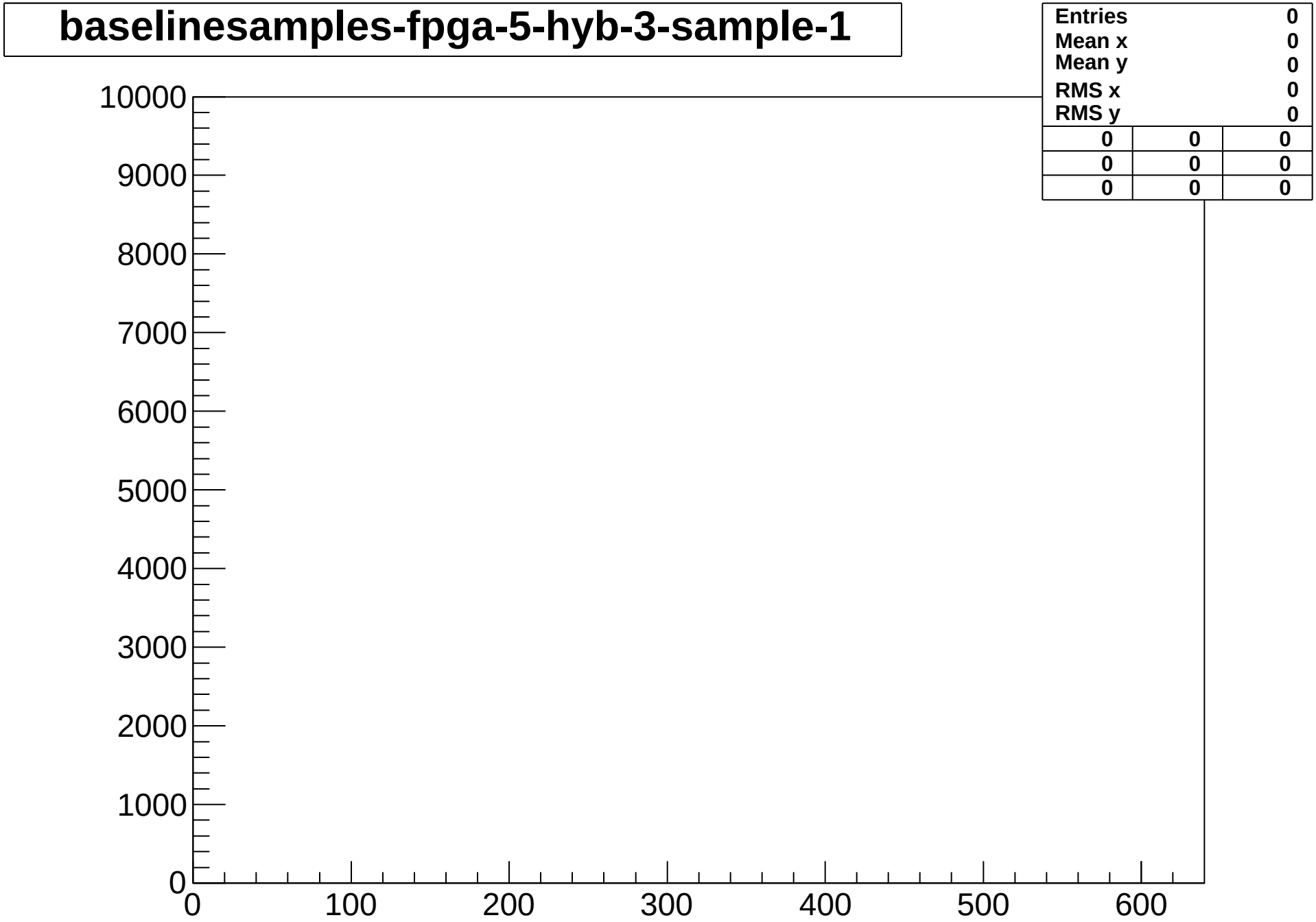
baselinesamples-fpga-5-hyb-2-sample-5



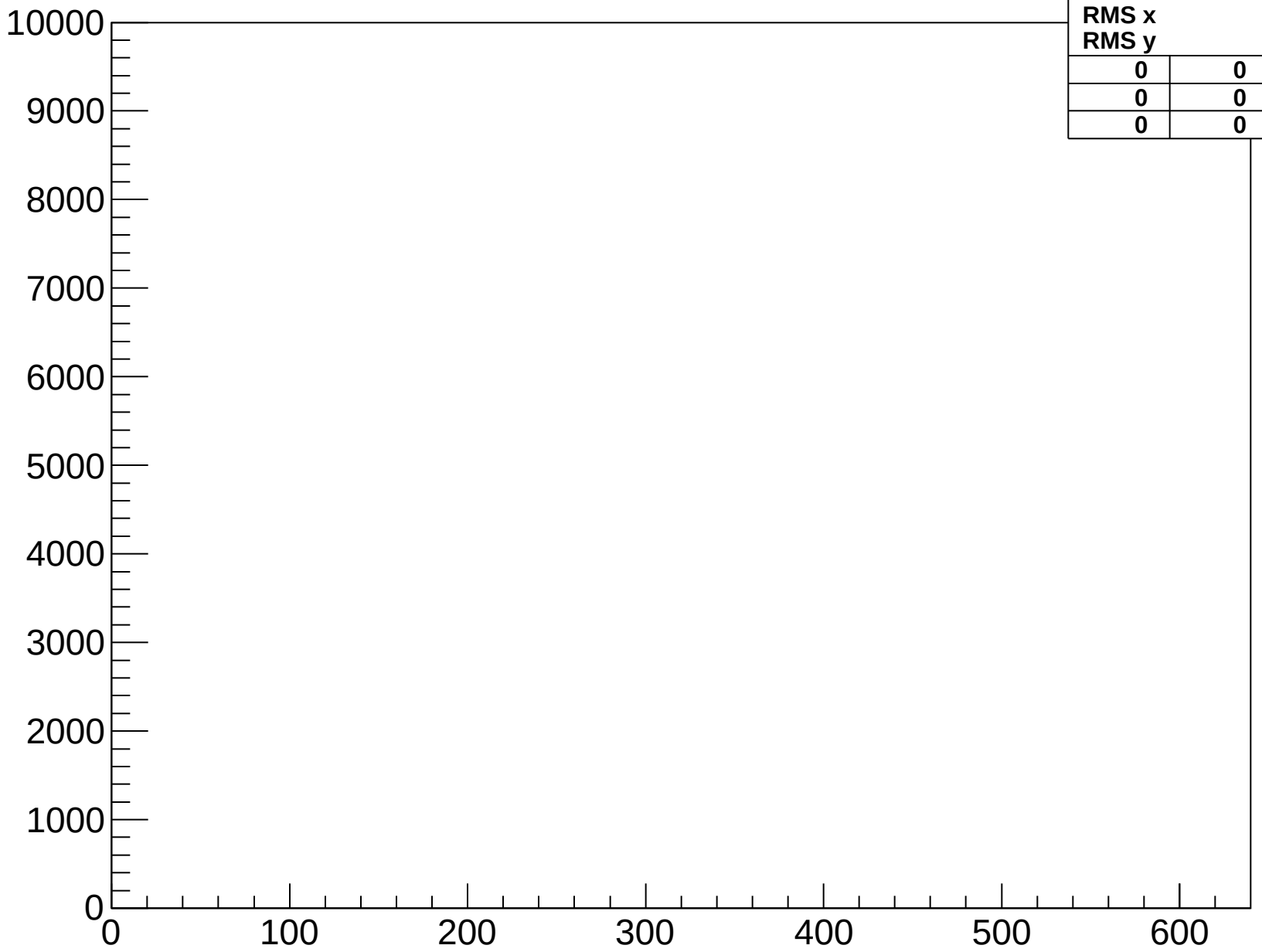
baselinesamples-fpga-5-hyb-3-sample-0



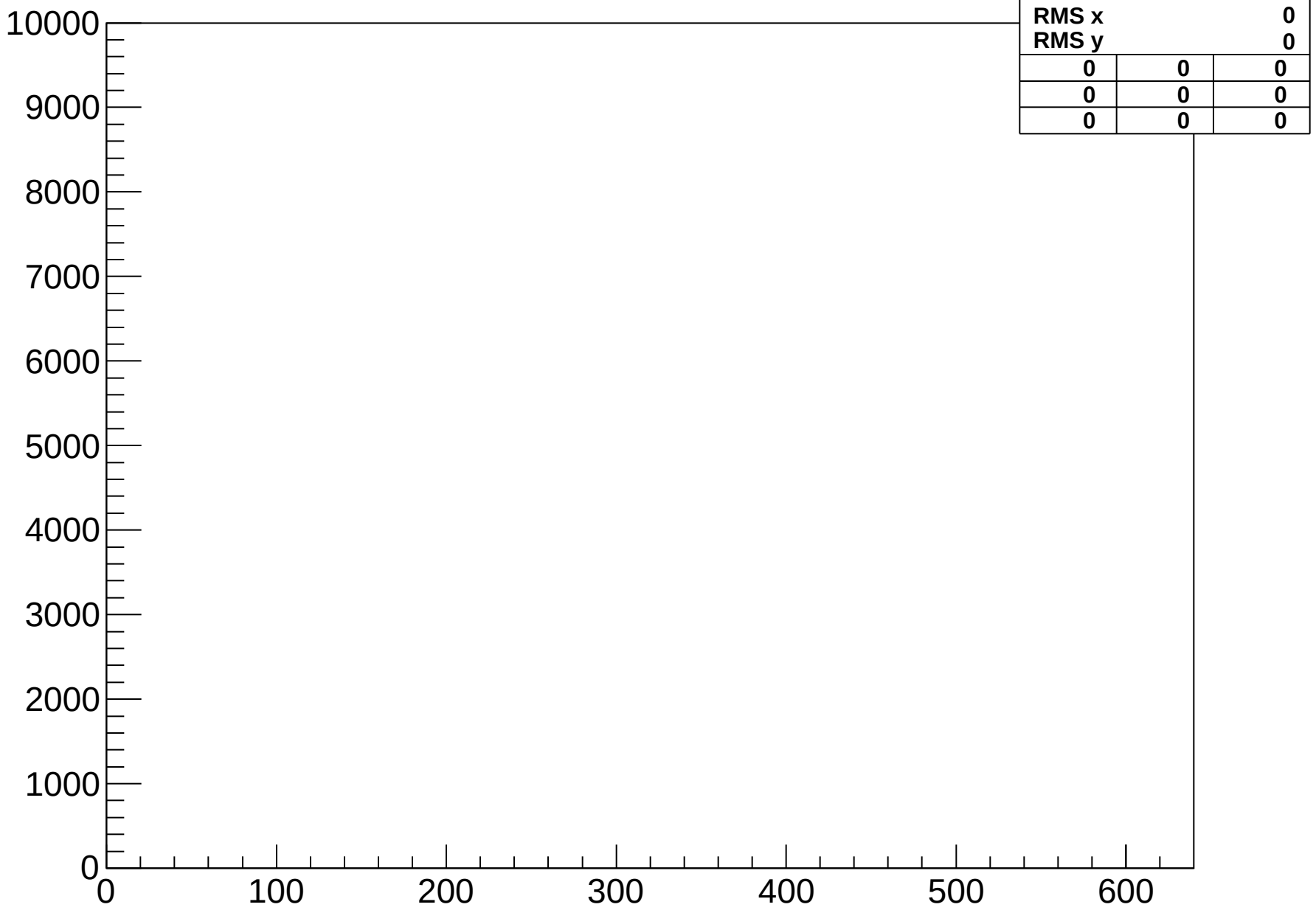
baselinesamples-fpga-5-hyb-3-sample-1



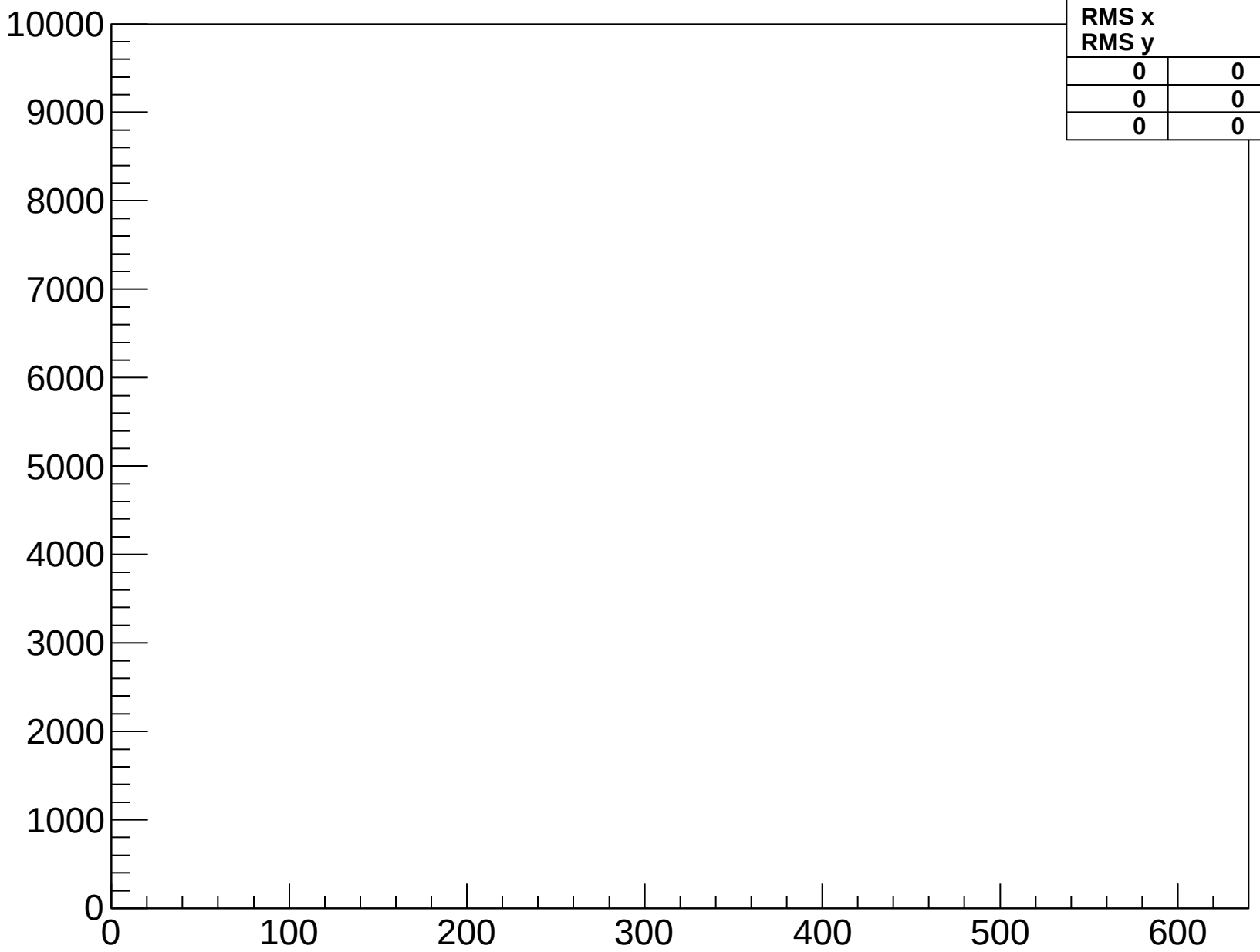
baselinesamples-fpga-5-hyb-3-sample-2



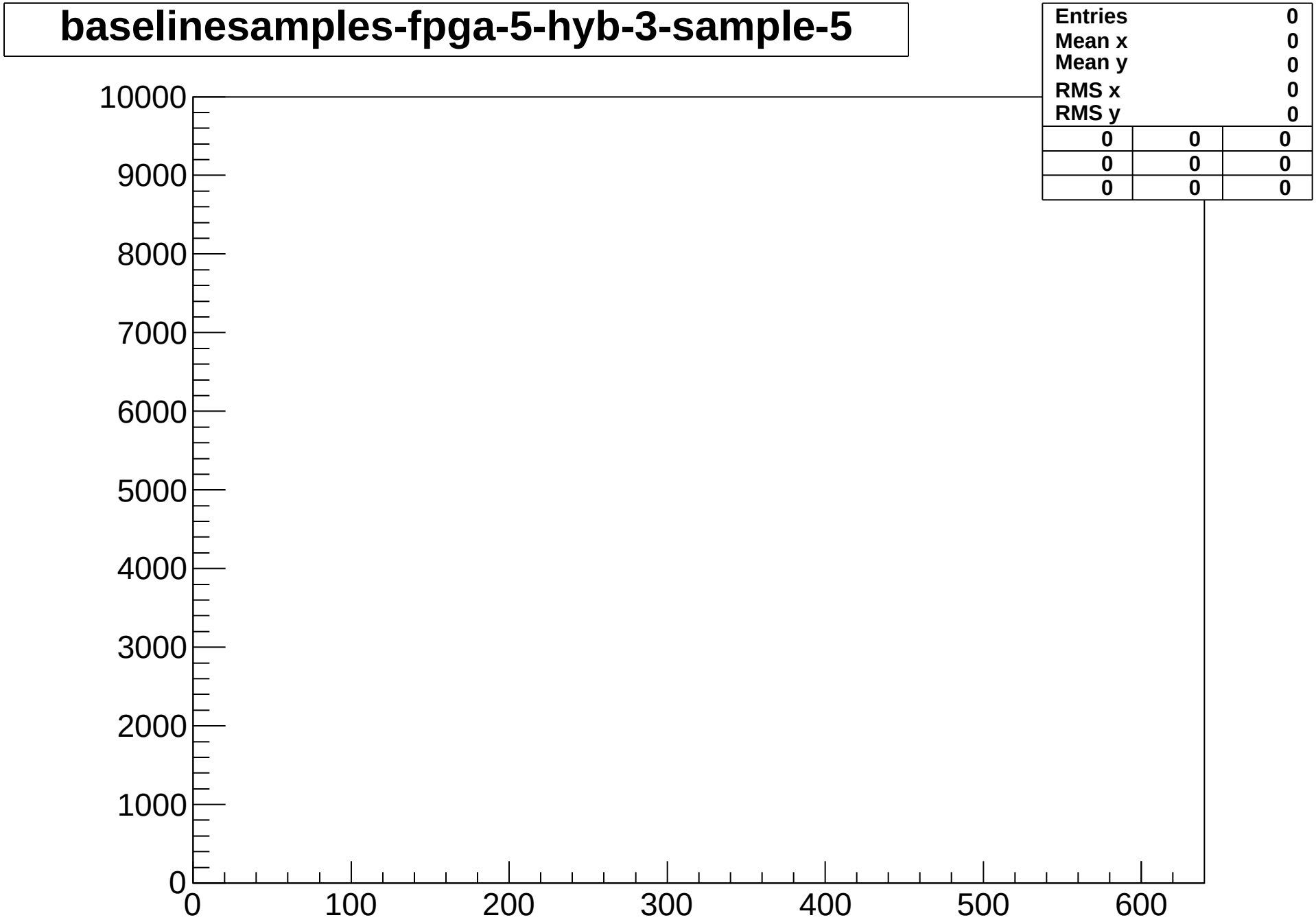
baselinesamples-fpga-5-hyb-3-sample-3



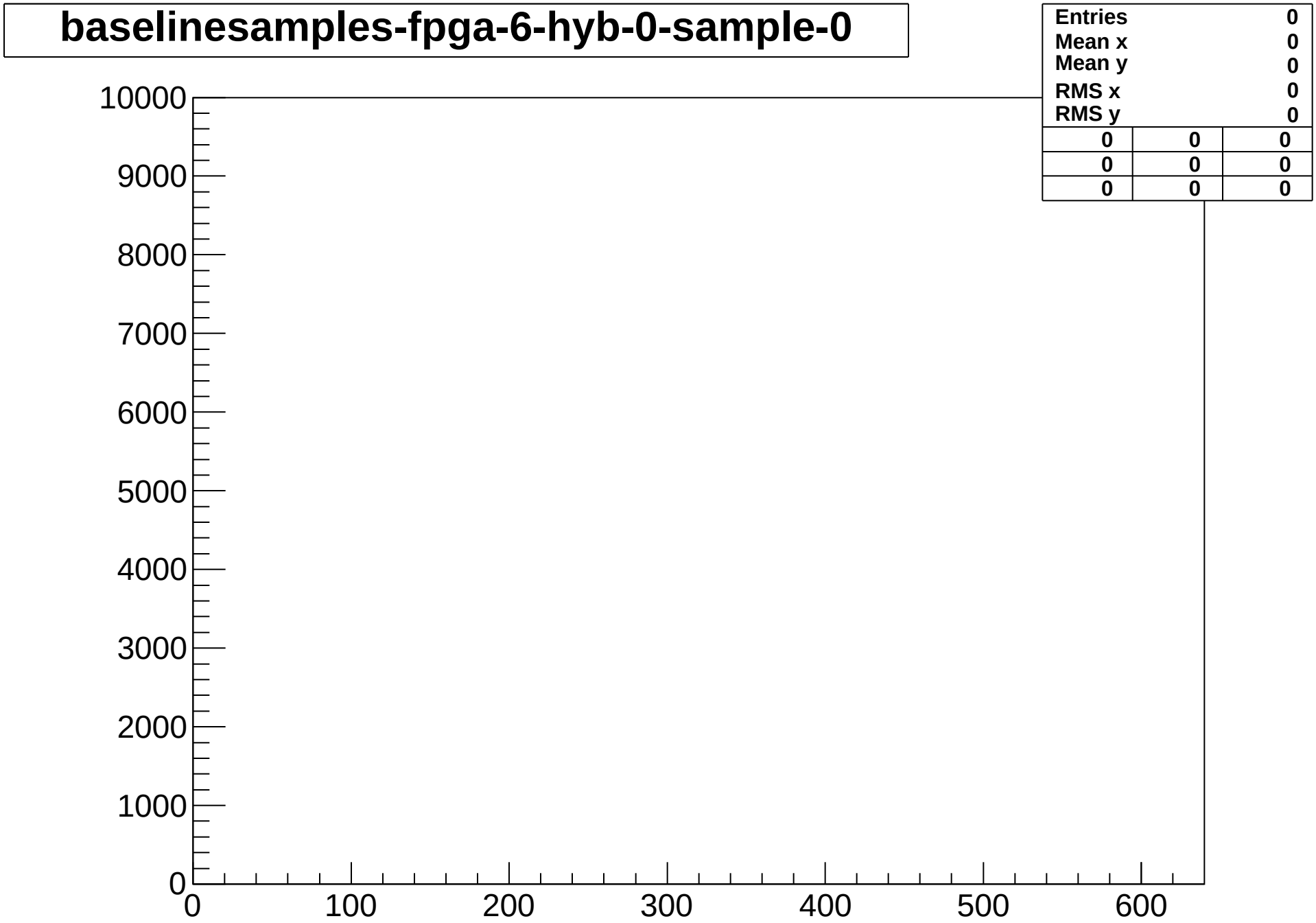
baselinesamples-fpga-5-hyb-3-sample-4



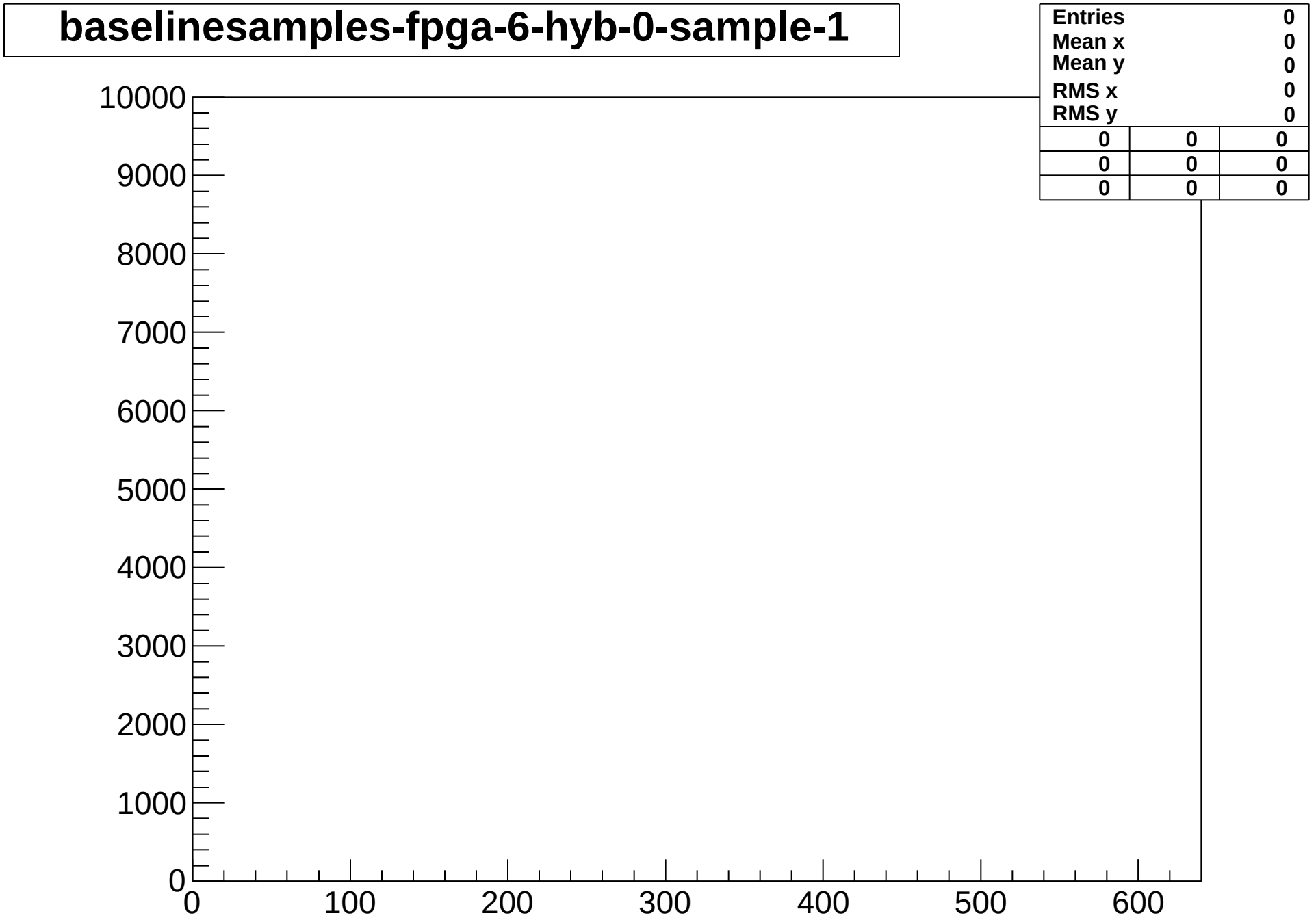
baselinesamples-fpga-5-hyb-3-sample-5



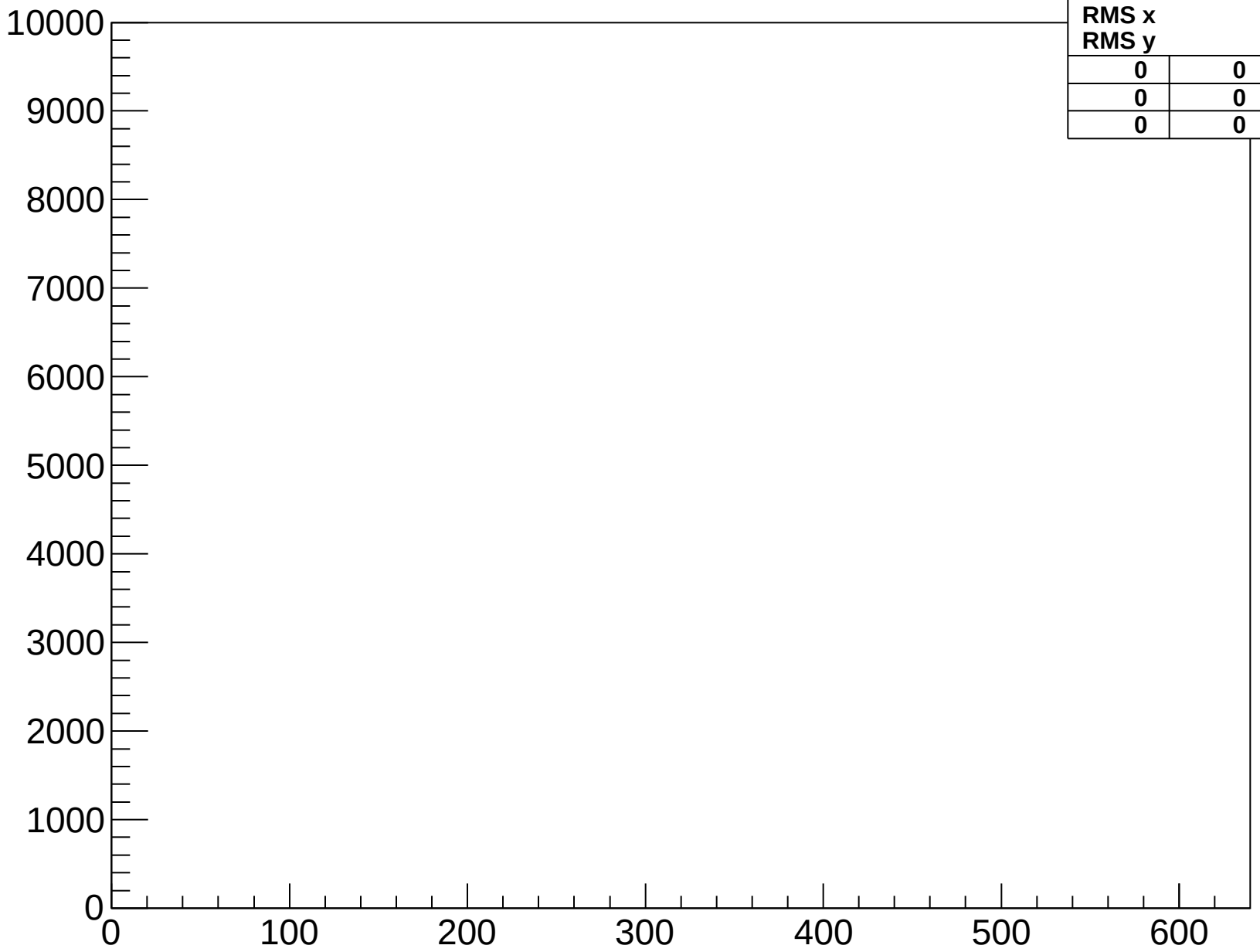
baselinesamples-fpga-6-hyb-0-sample-0



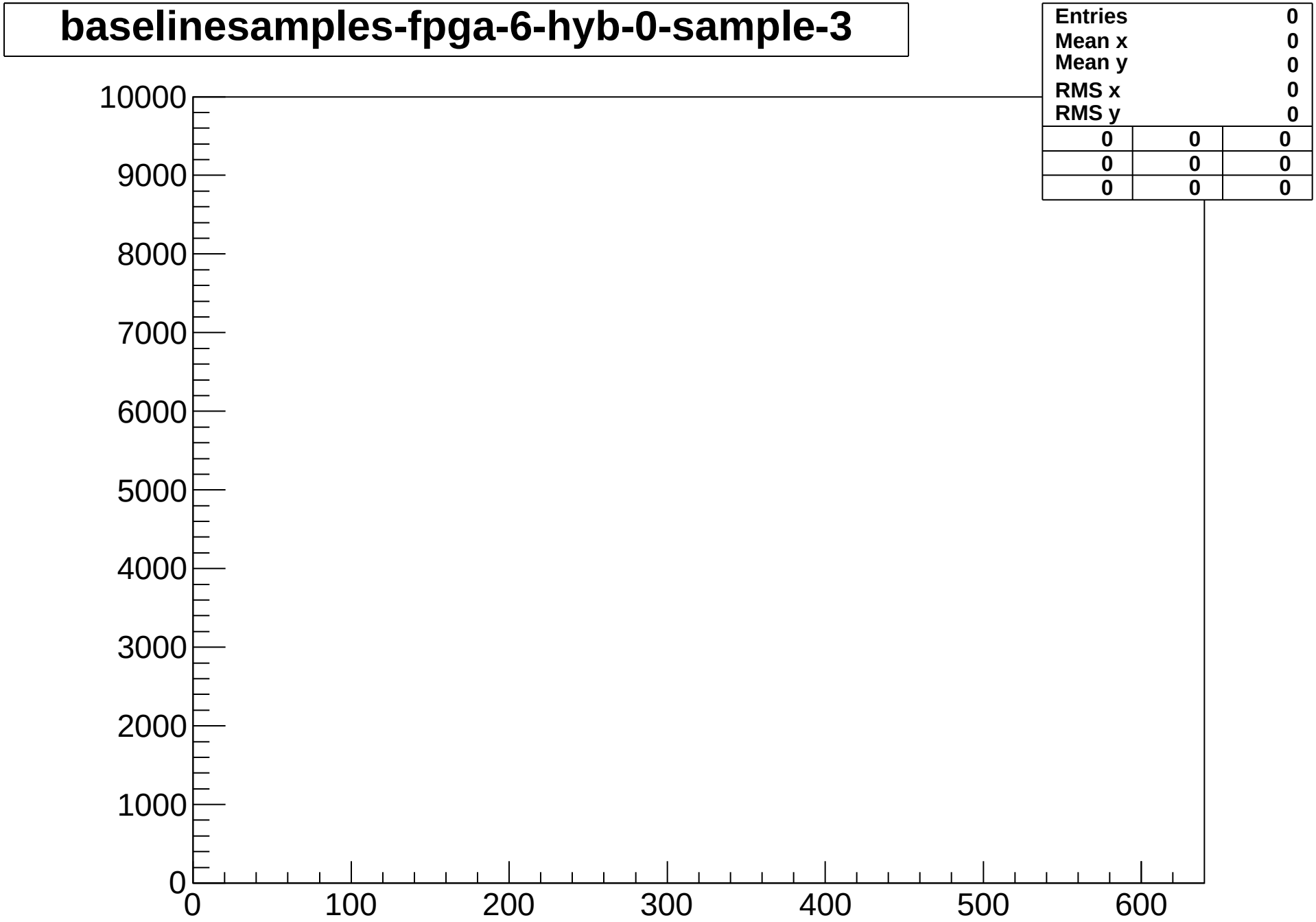
baselinesamples-fpga-6-hyb-0-sample-1



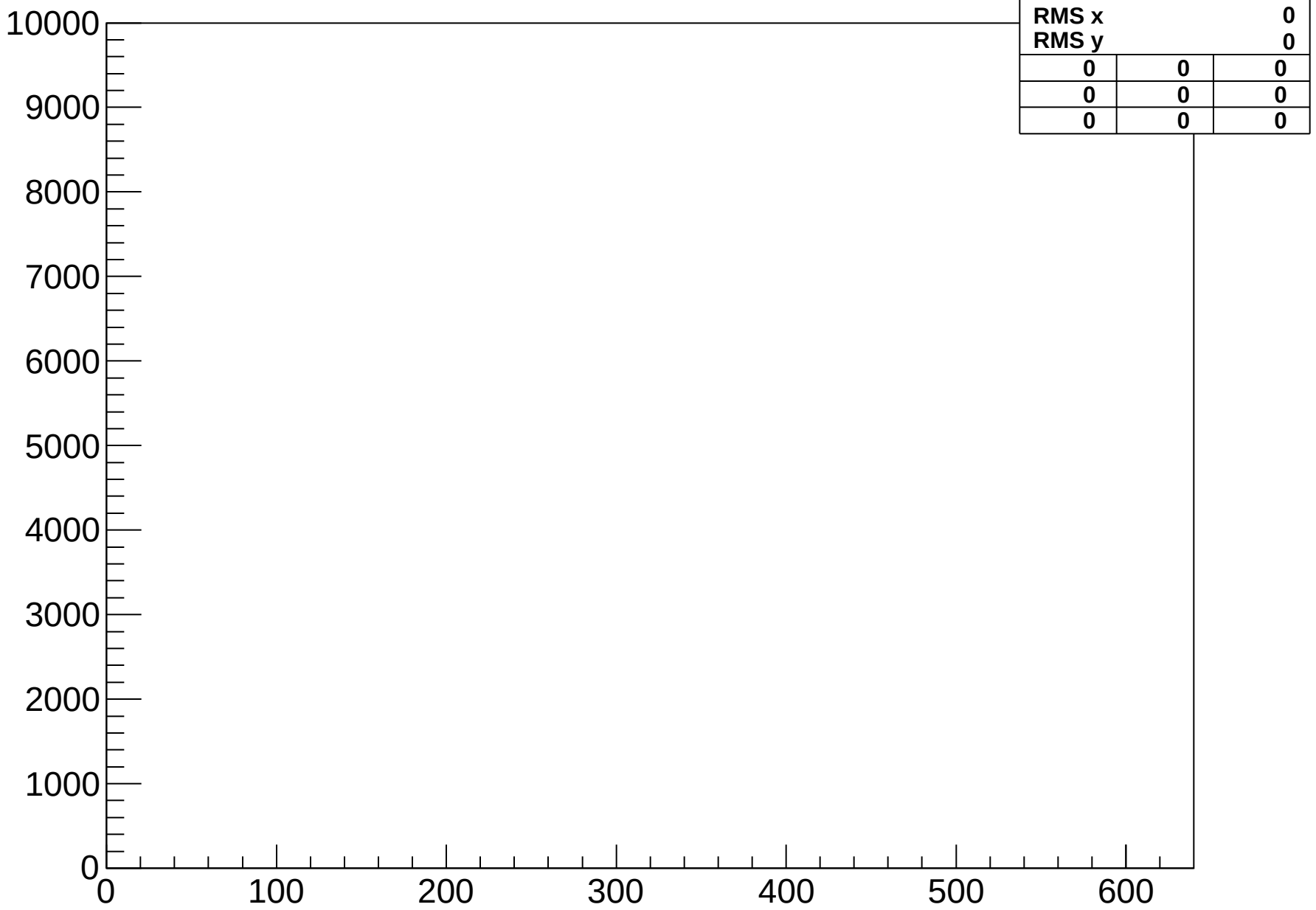
baselinesamples-fpga-6-hyb-0-sample-2



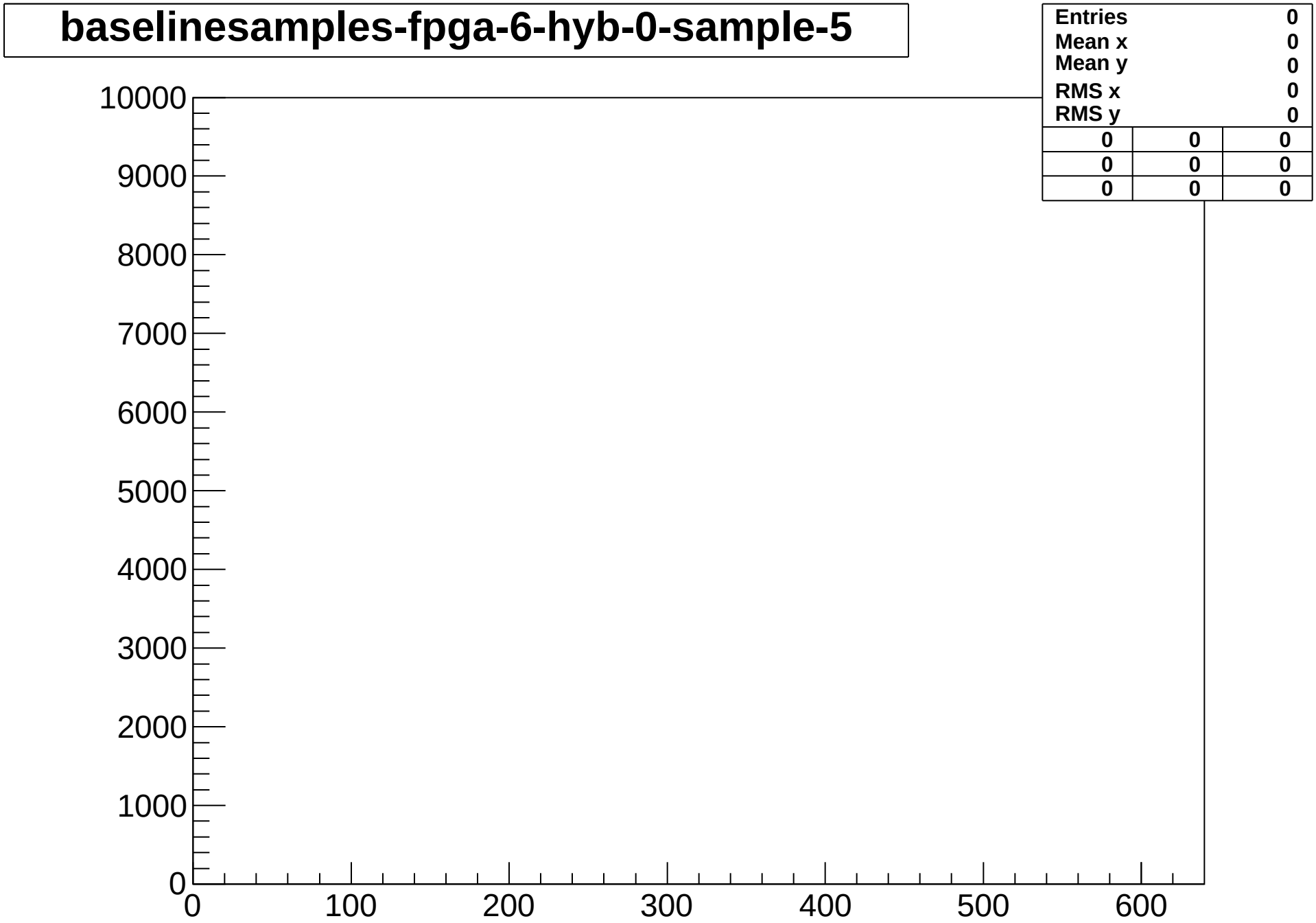
baselinesamples-fpga-6-hyb-0-sample-3



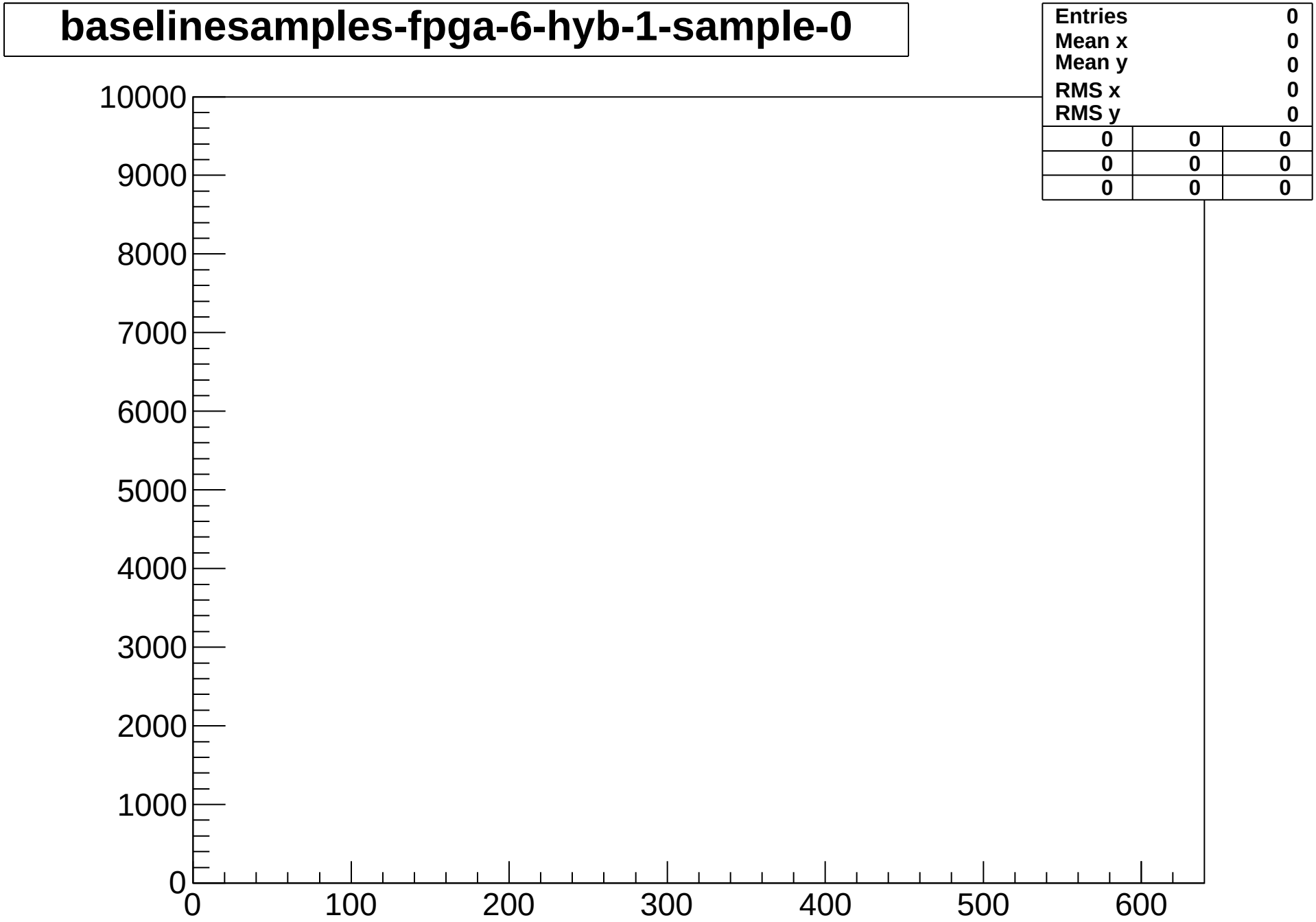
baselinesamples-fpga-6-hyb-0-sample-4

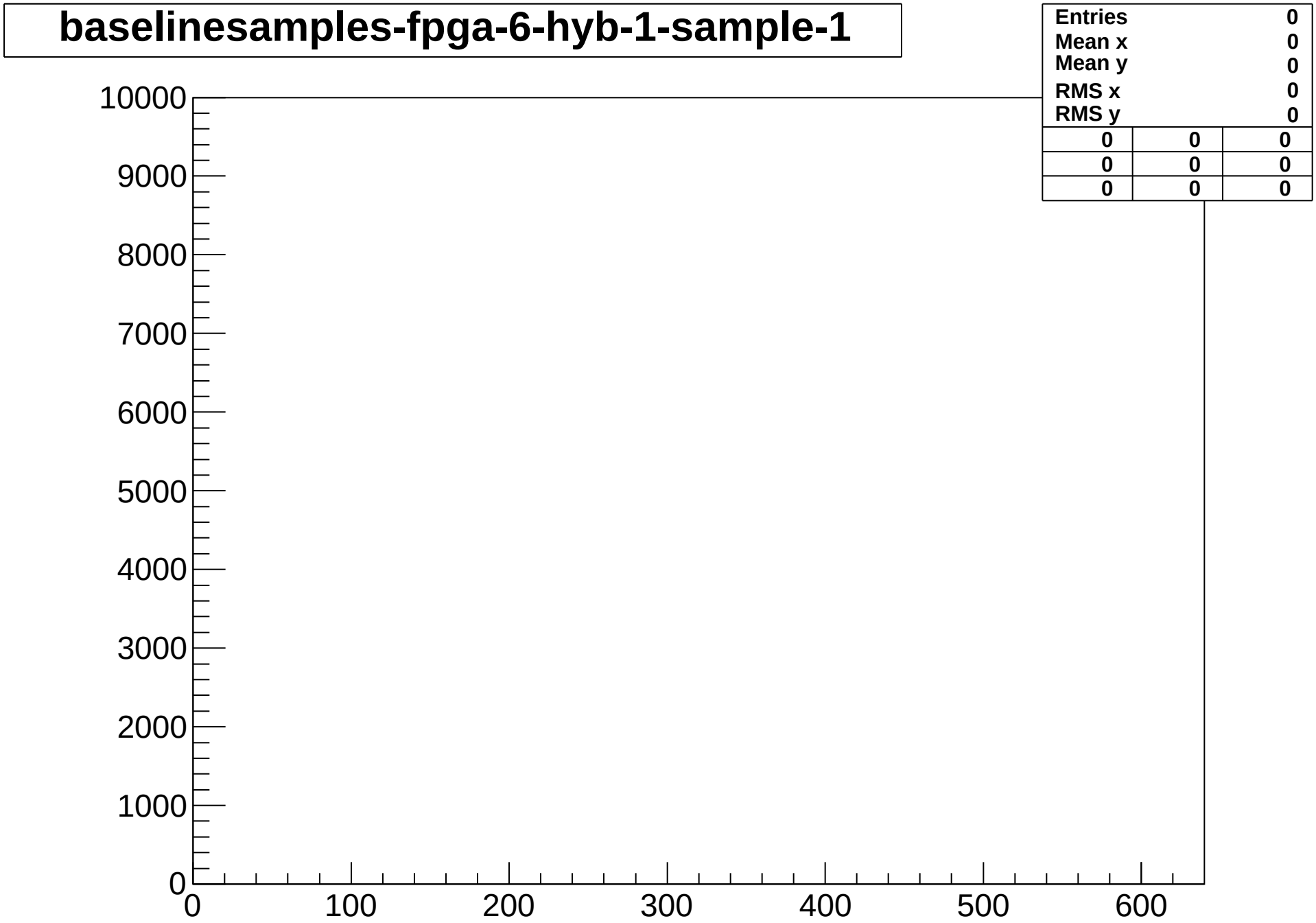


baselinesamples-fpga-6-hyb-0-sample-5

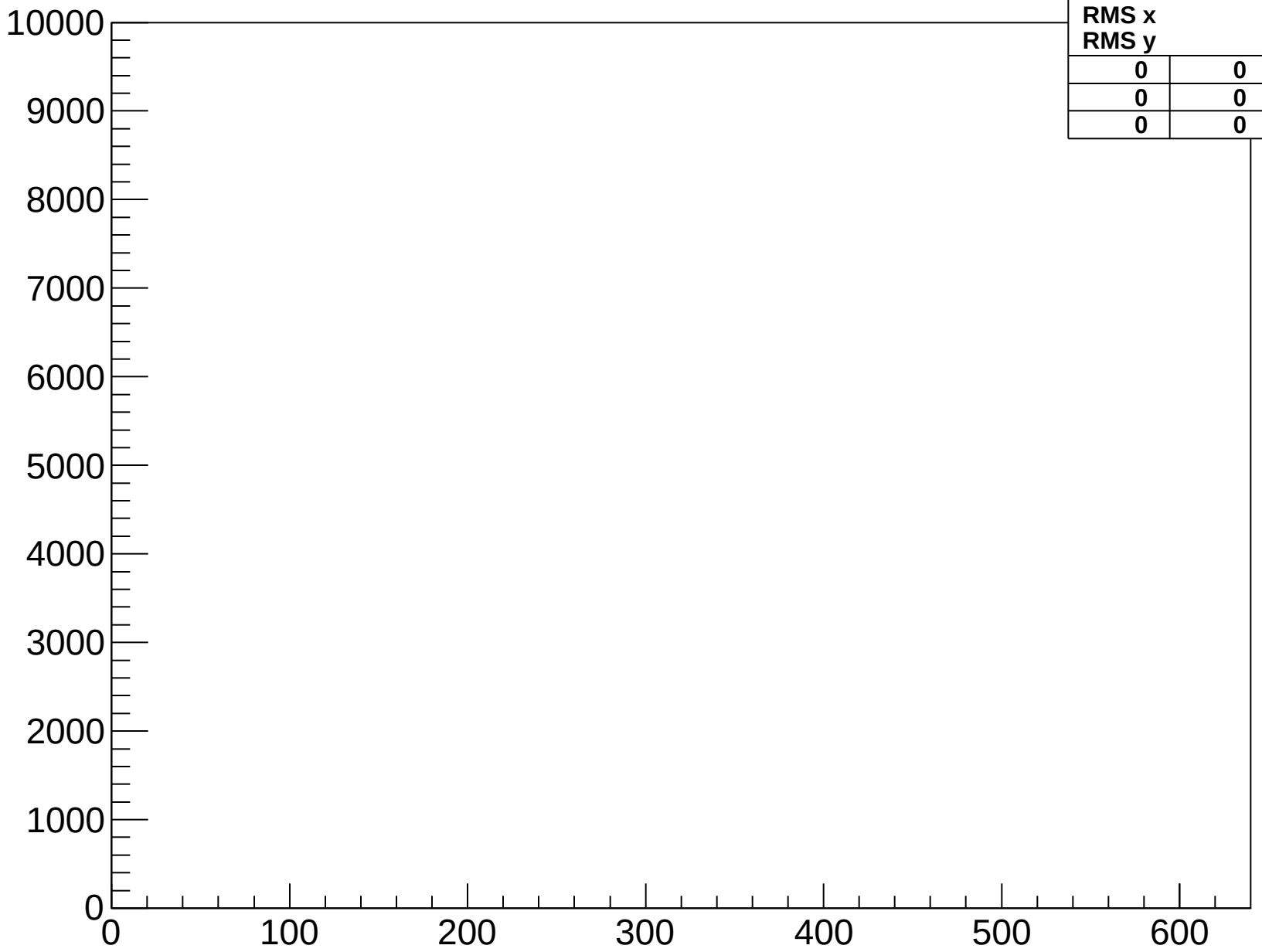


baselinesamples-fpga-6-hyb-1-sample-0

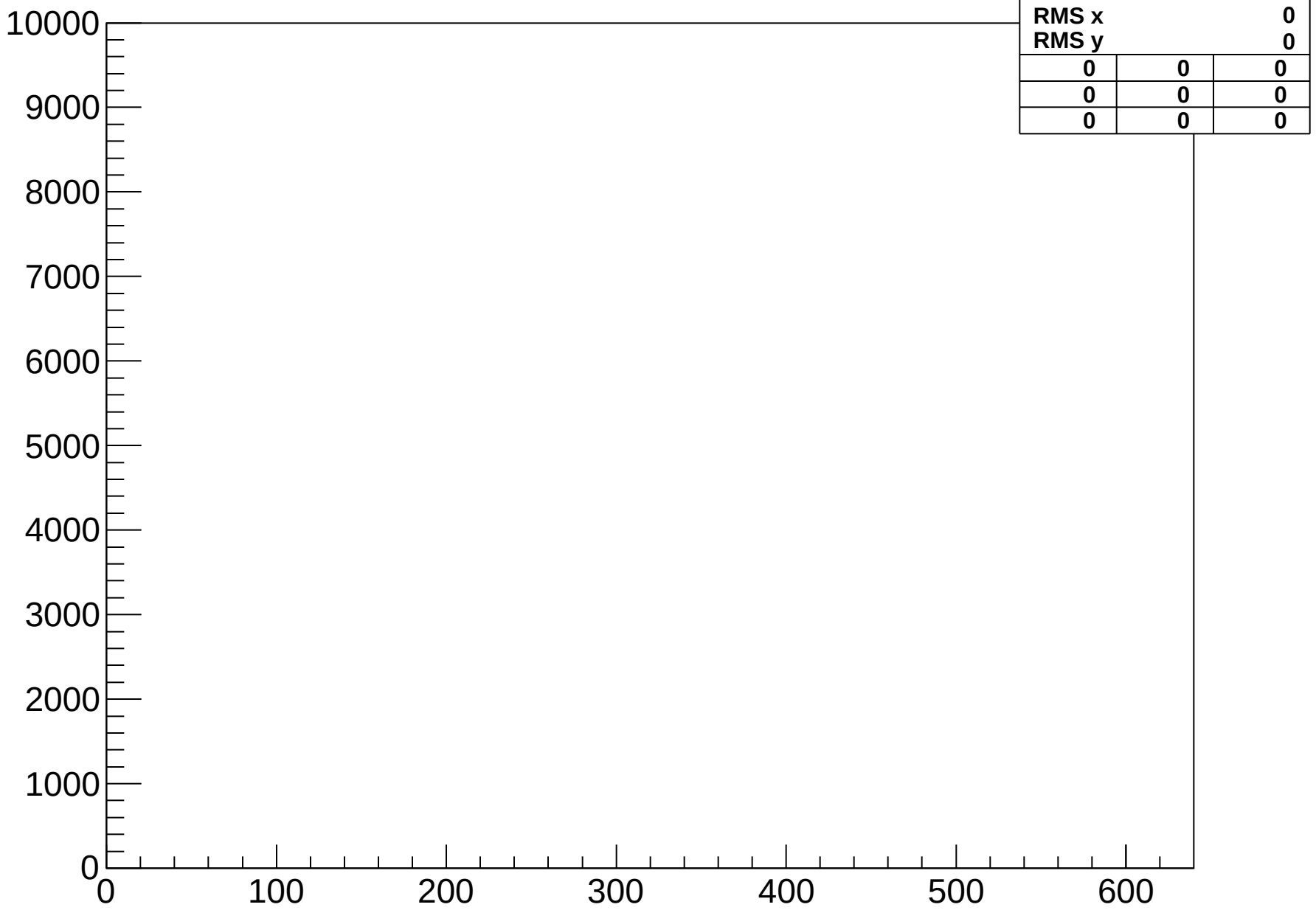



baselinesamples-fpga-6-hyb-1-sample-1
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

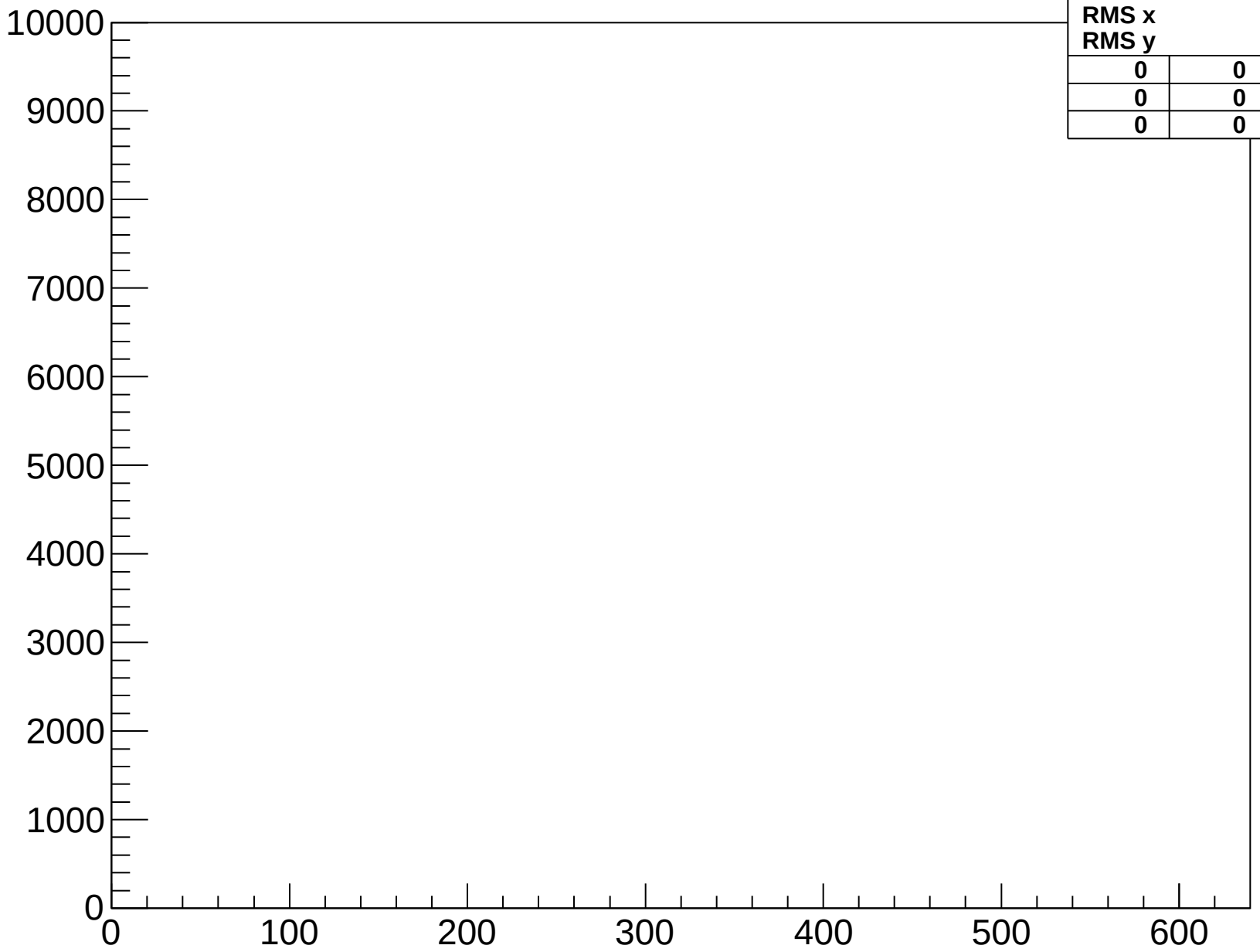
baselinesamples-fpga-6-hyb-1-sample-2



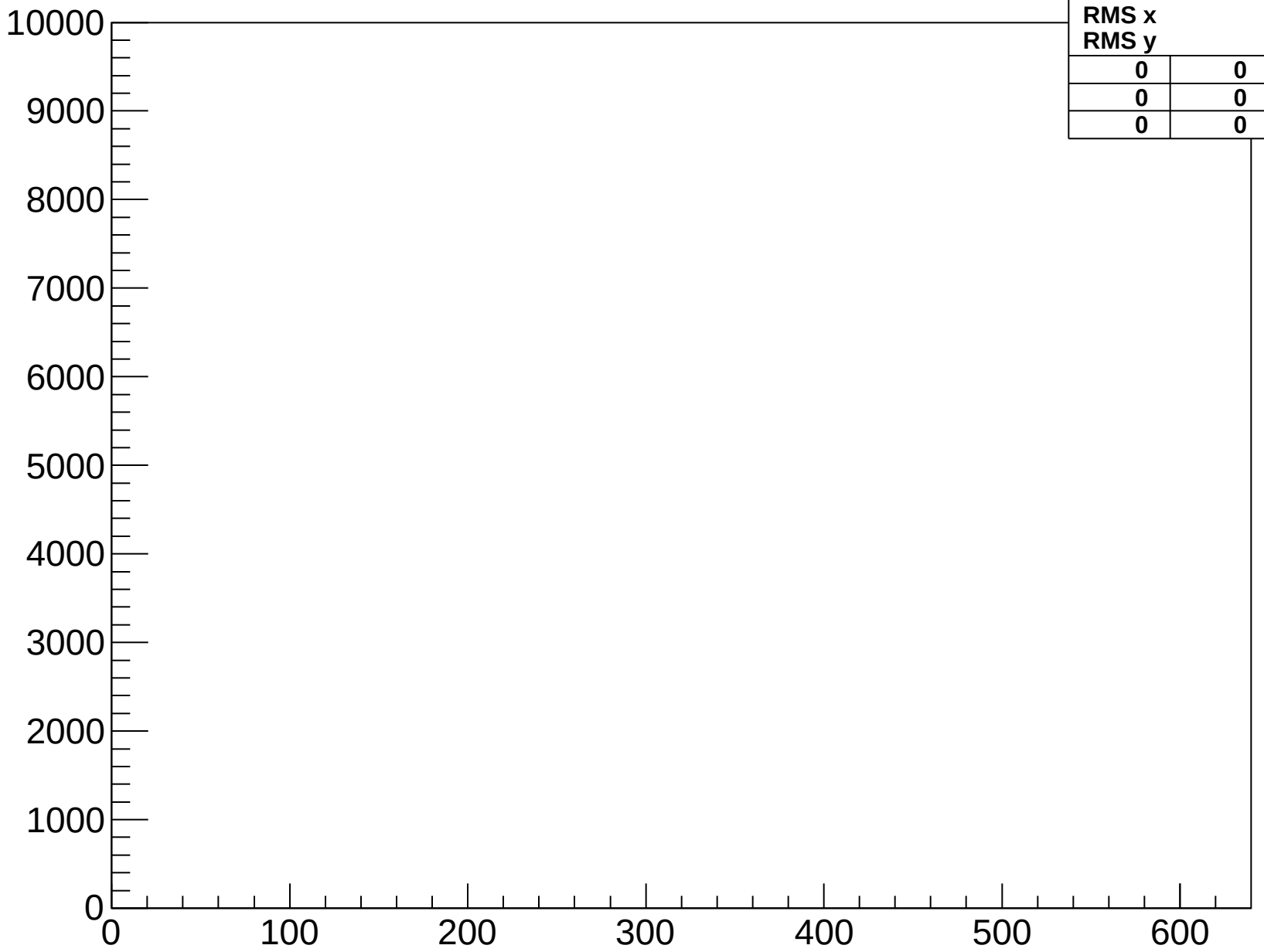
baselinesamples-fpga-6-hyb-1-sample-3



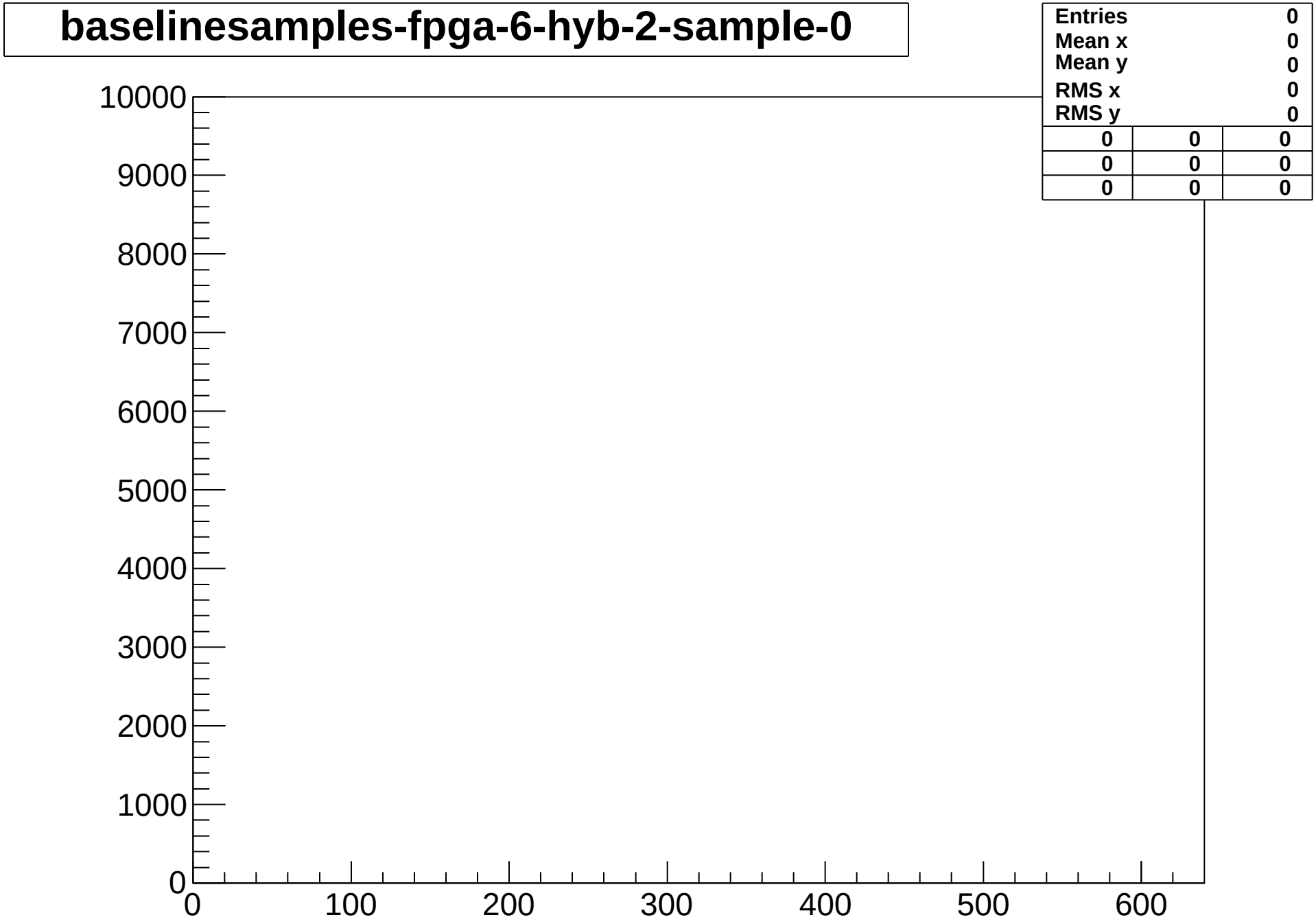
baselinesamples-fpga-6-hyb-1-sample-4



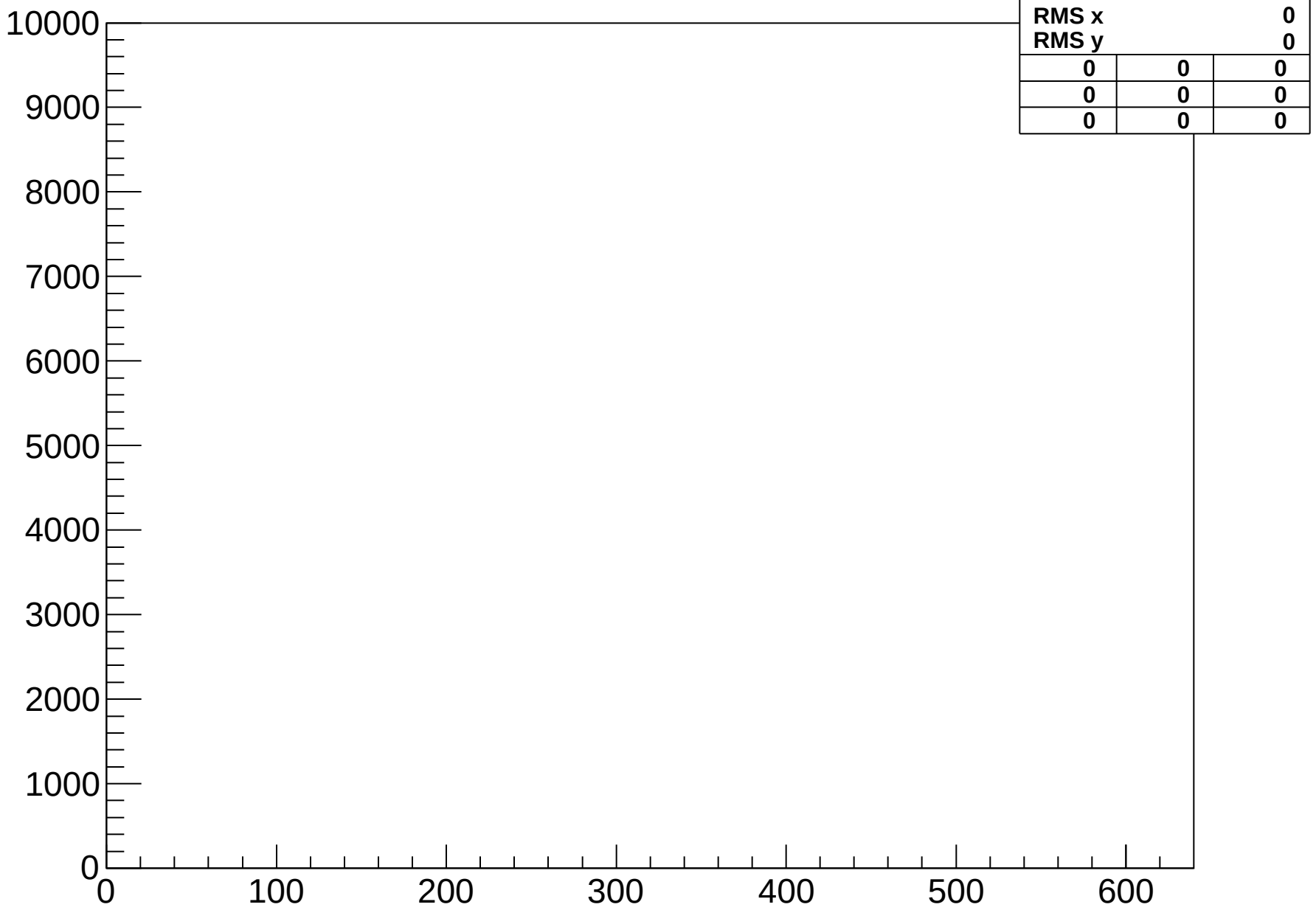
baselinesamples-fpga-6-hyb-1-sample-5



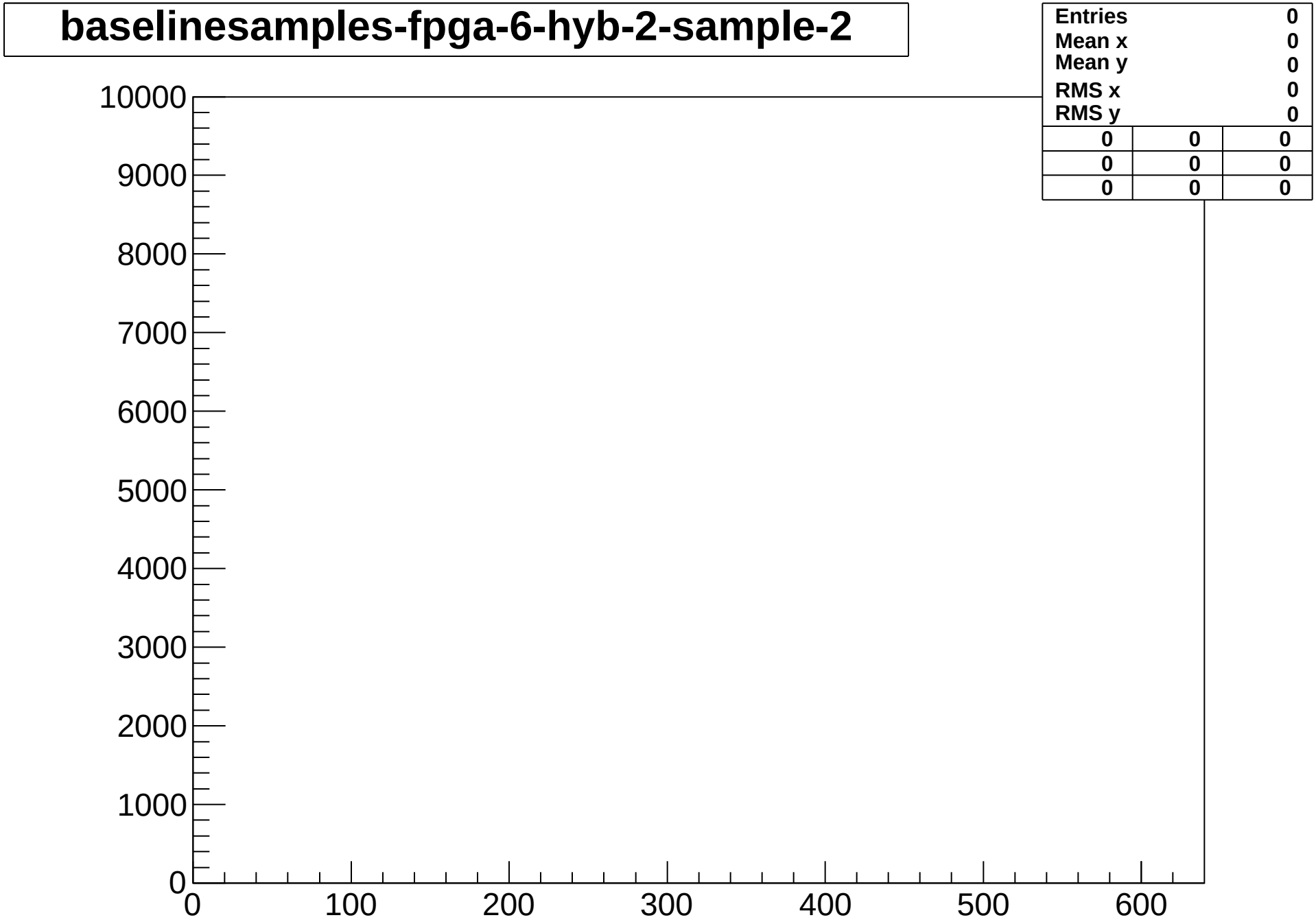
baselinesamples-fpga-6-hyb-2-sample-0



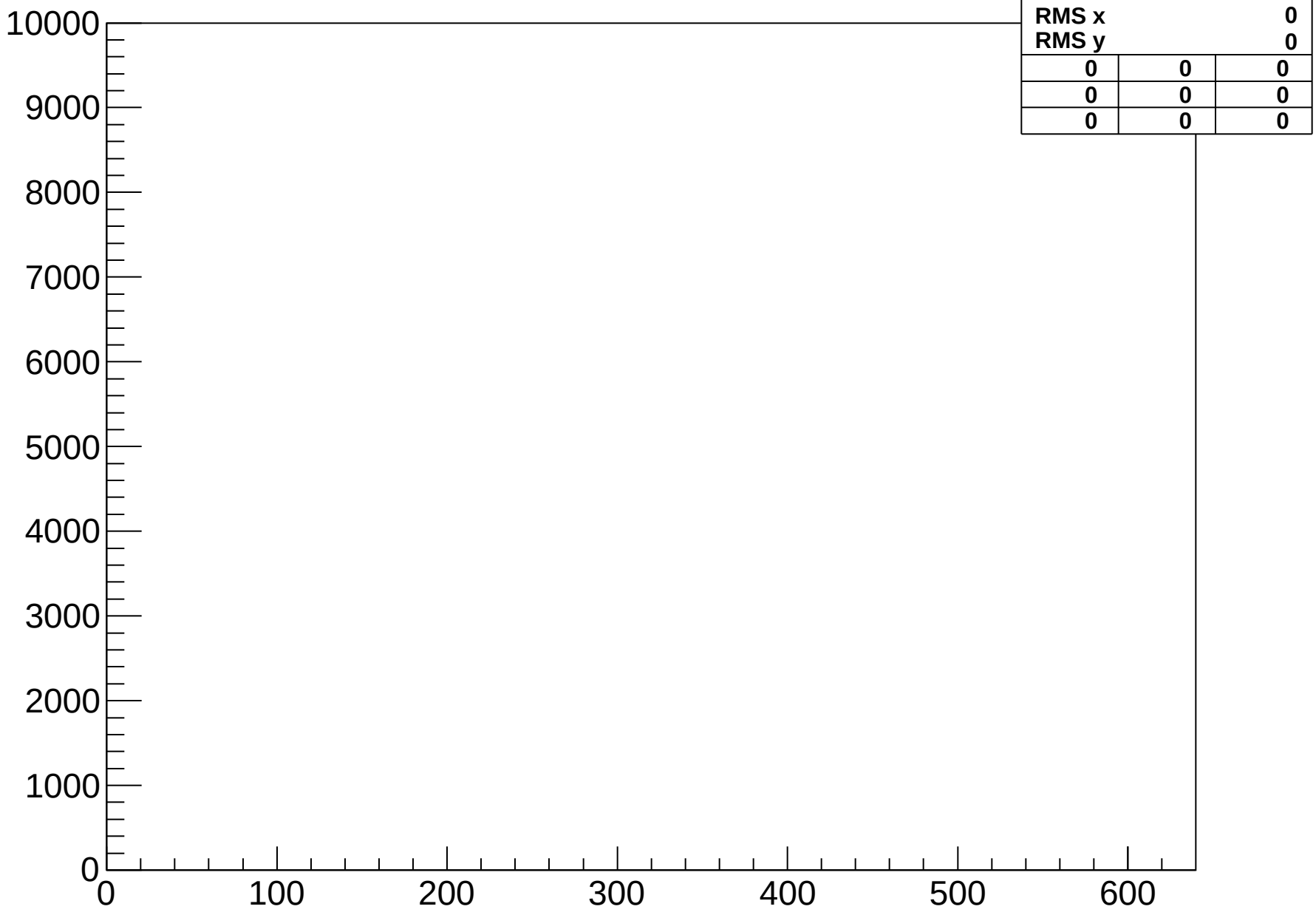
baselinesamples-fpga-6-hyb-2-sample-1



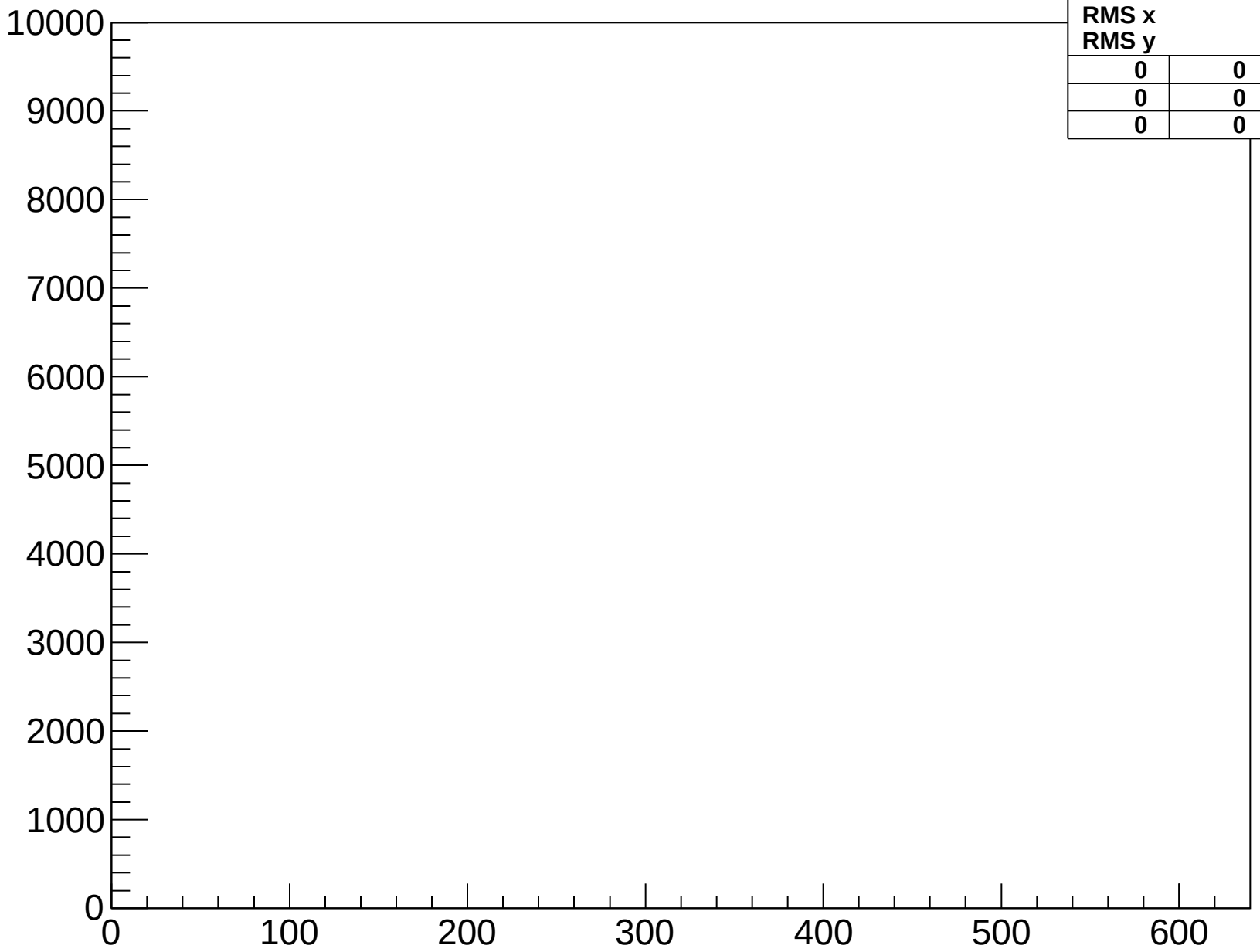
baselinesamples-fpga-6-hyb-2-sample-2



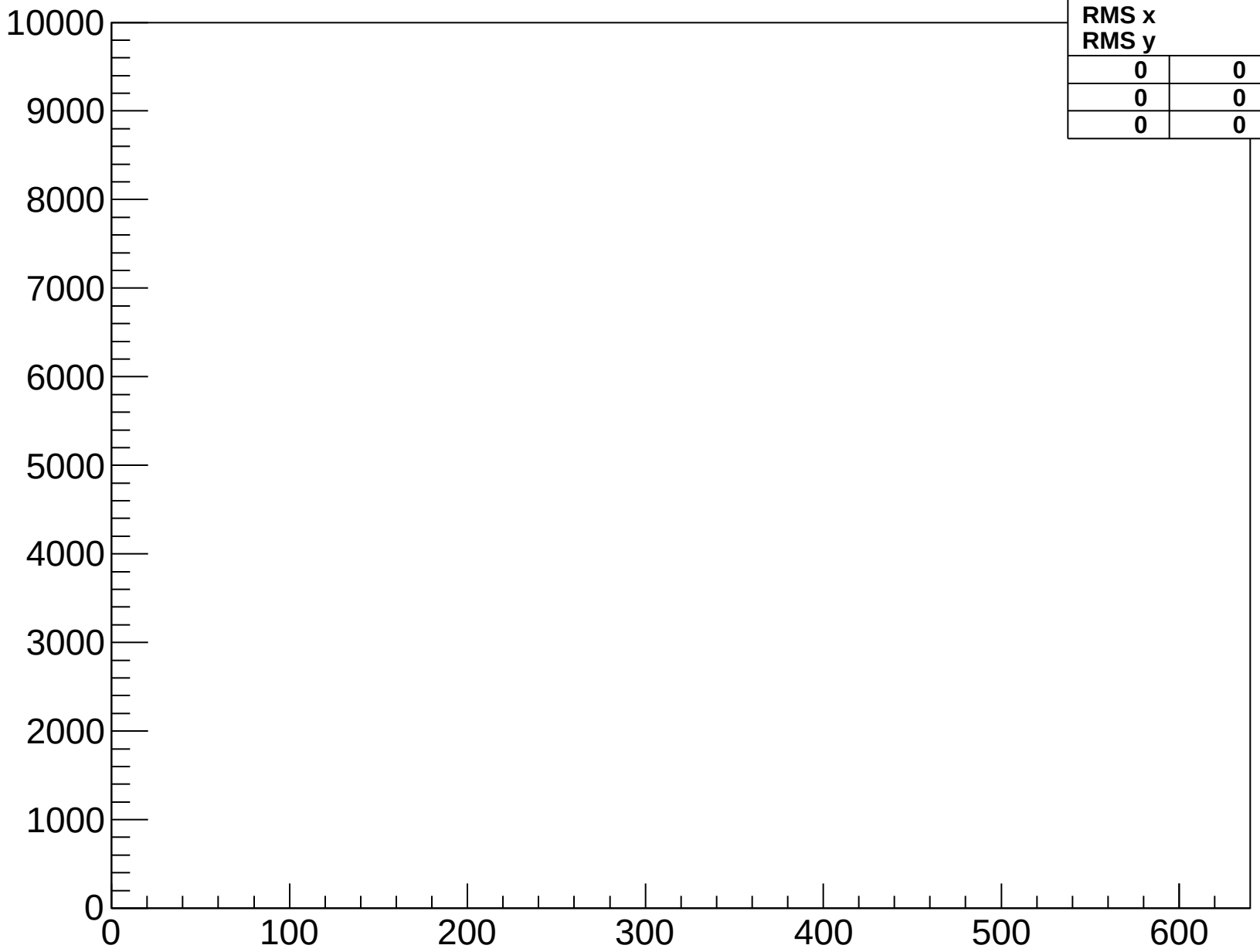
baselinesamples-fpga-6-hyb-2-sample-3



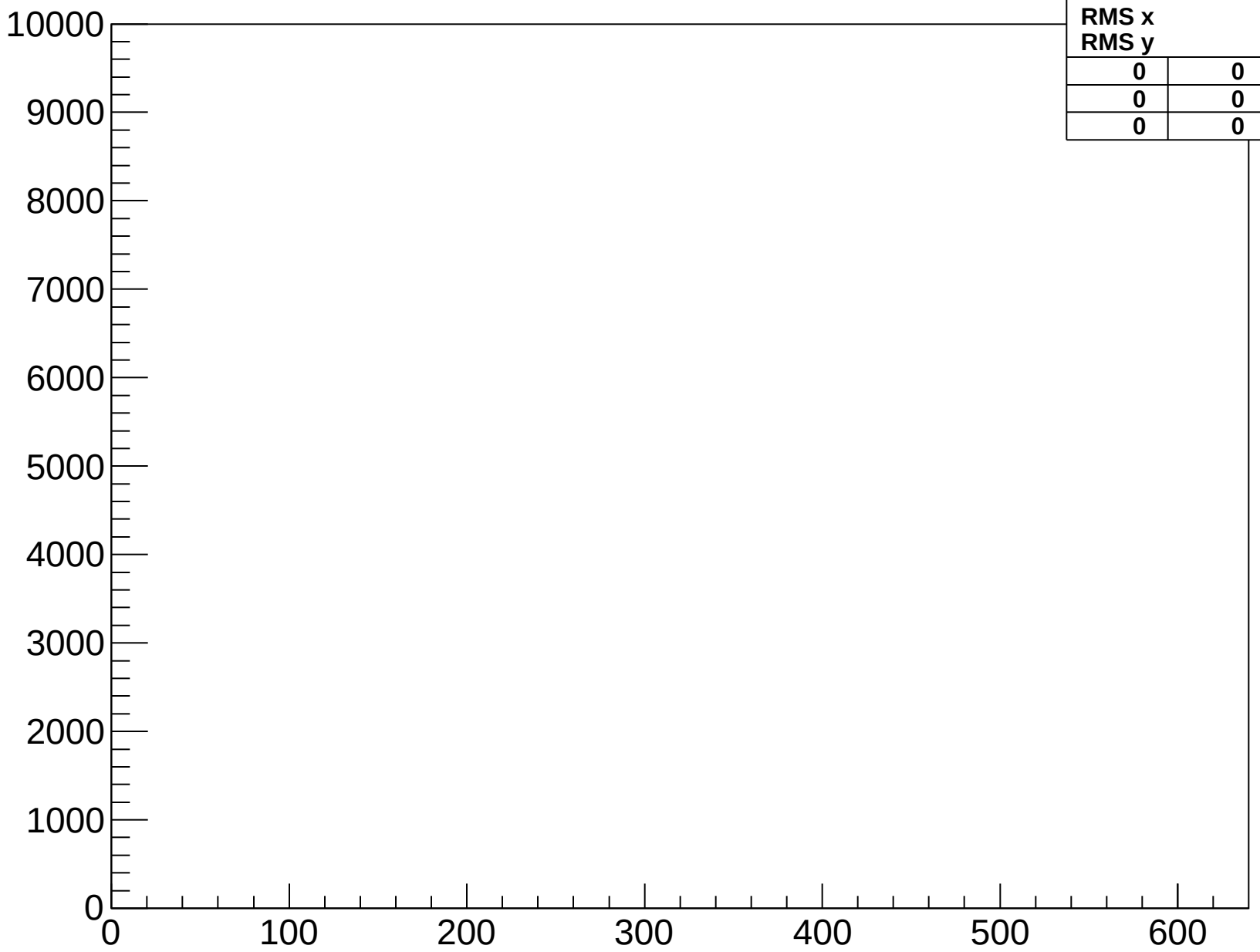
baselinesamples-fpga-6-hyb-2-sample-4



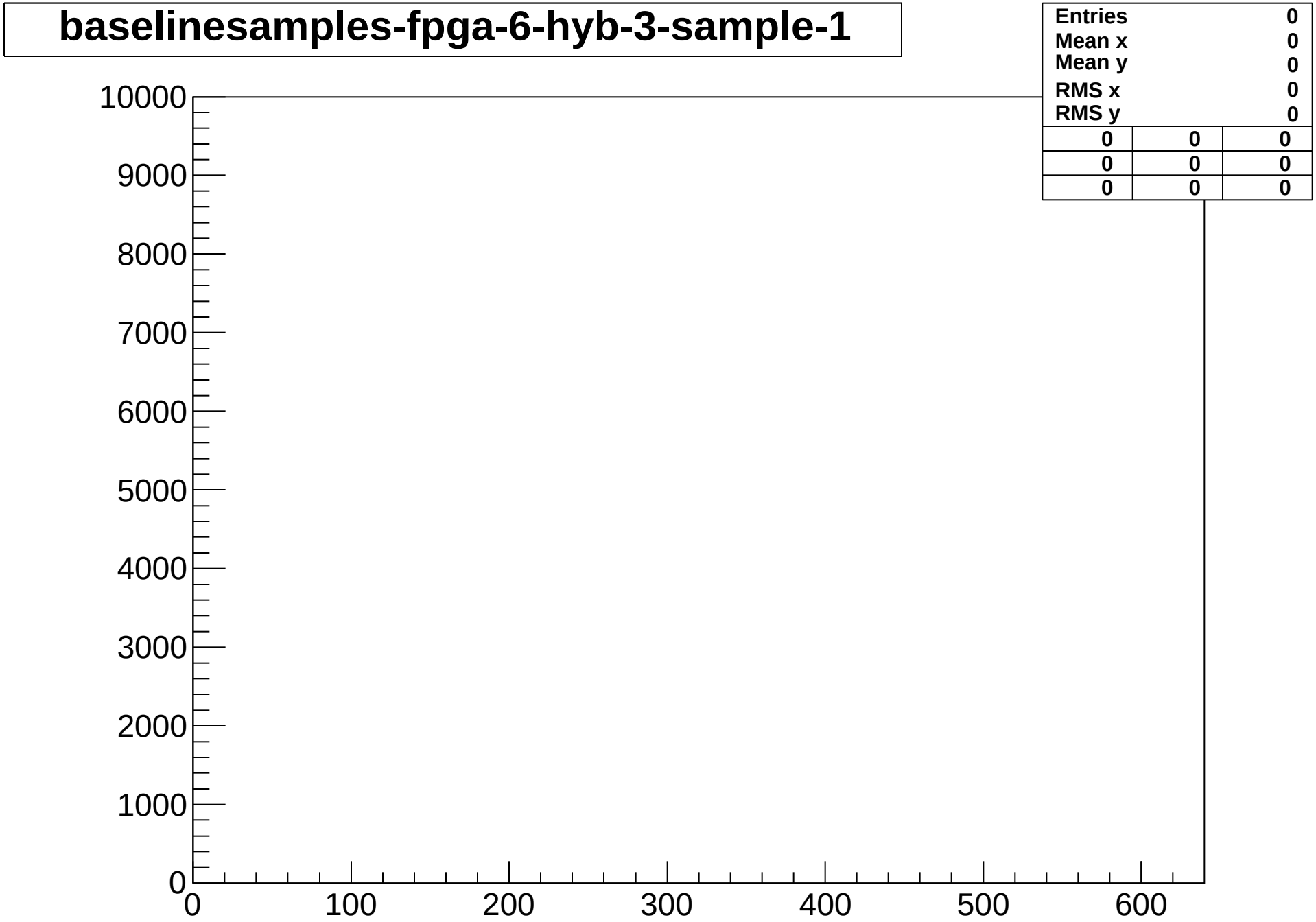
baselinesamples-fpga-6-hyb-2-sample-5



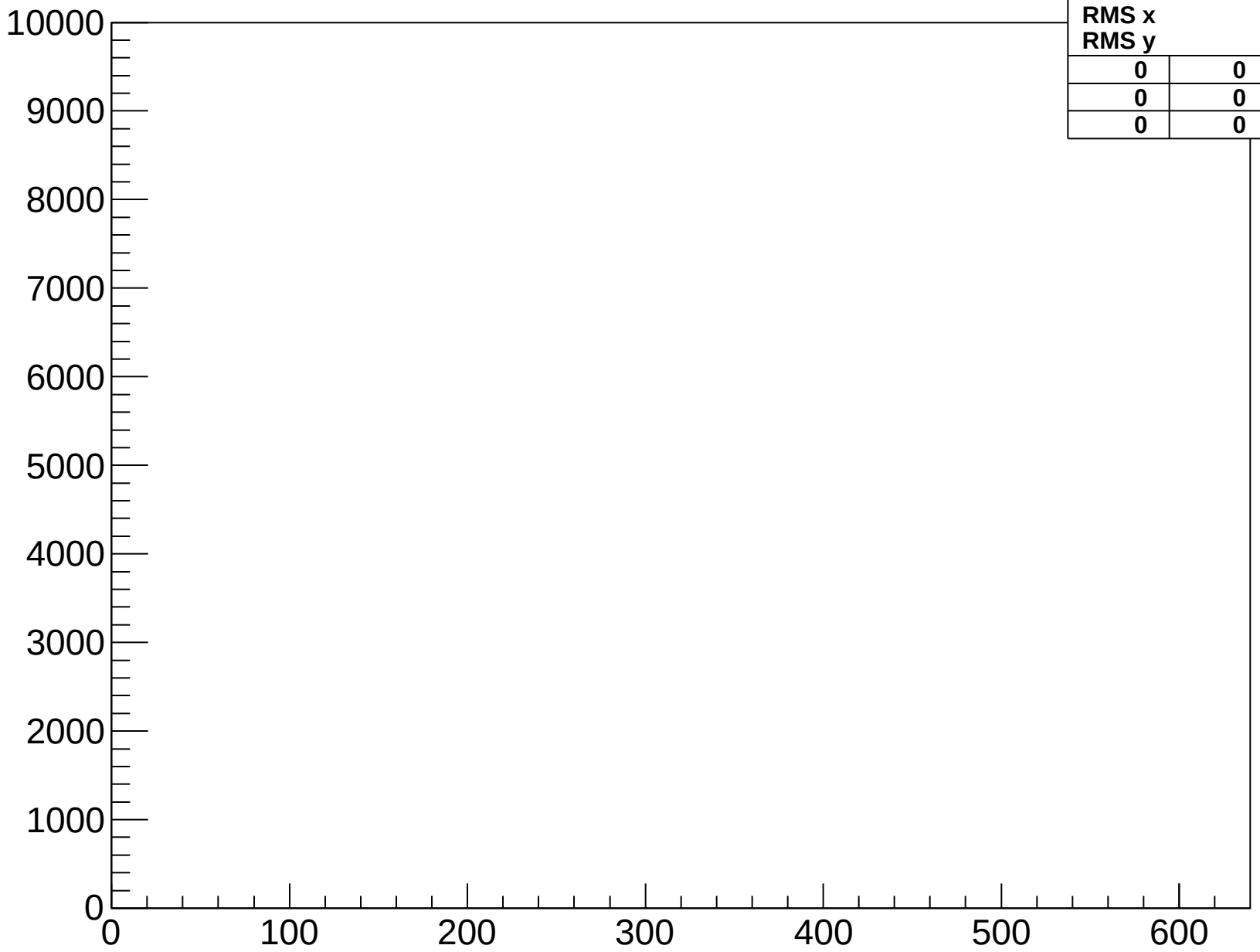
baselinesamples-fpga-6-hyb-3-sample-0



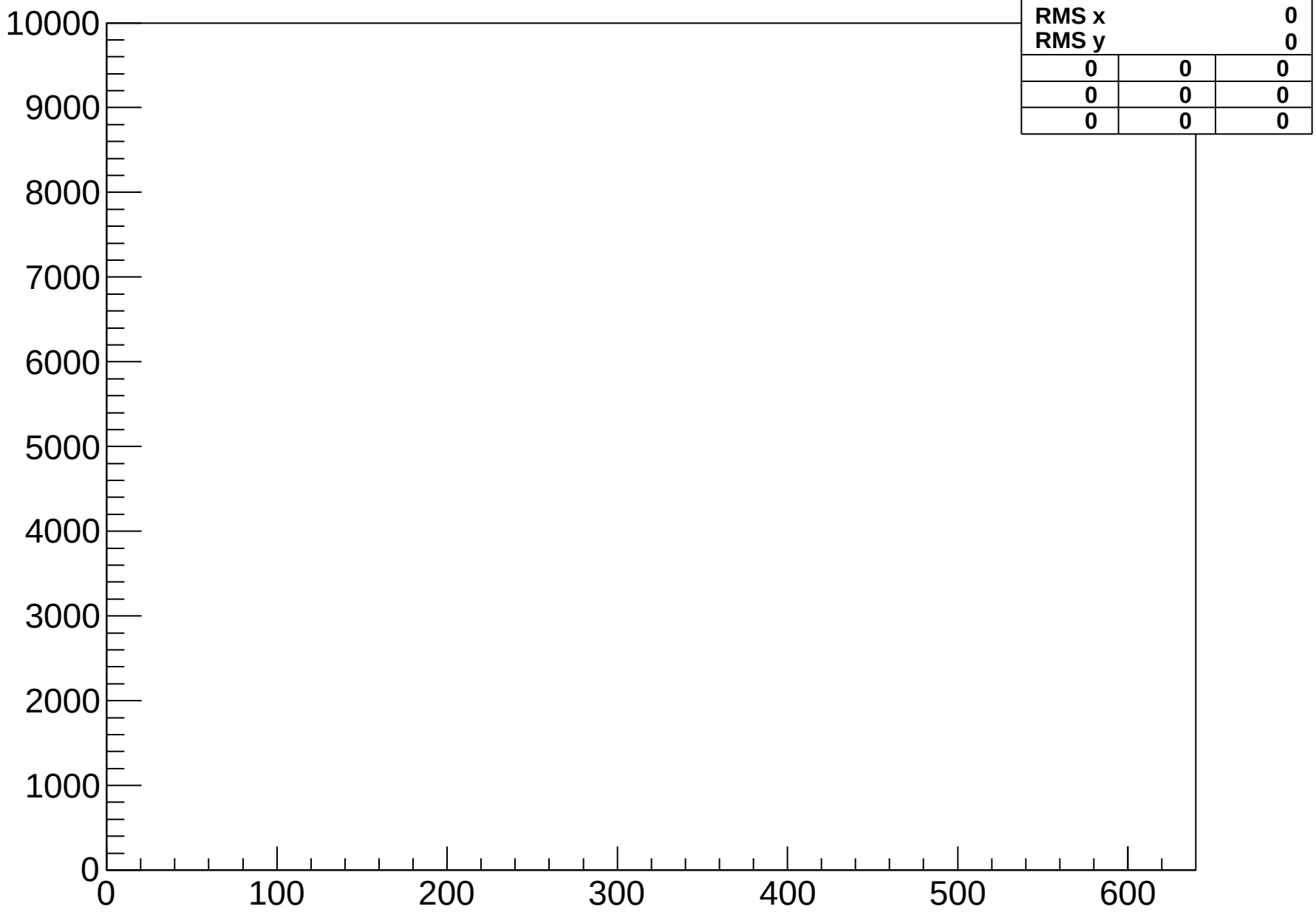
baselinesamples-fpga-6-hyb-3-sample-1



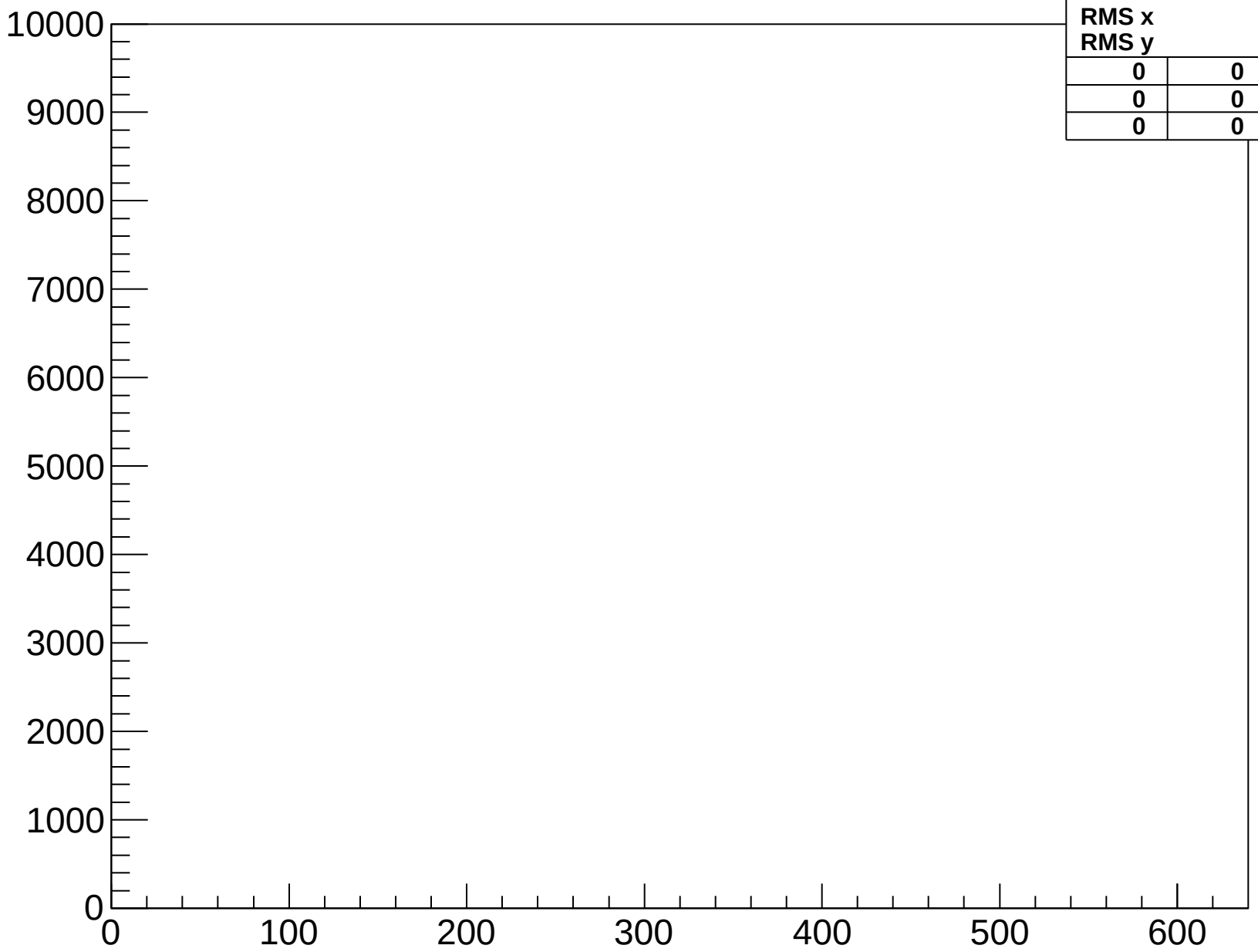
baselinesamples-fpga-6-hyb-3-sample-2



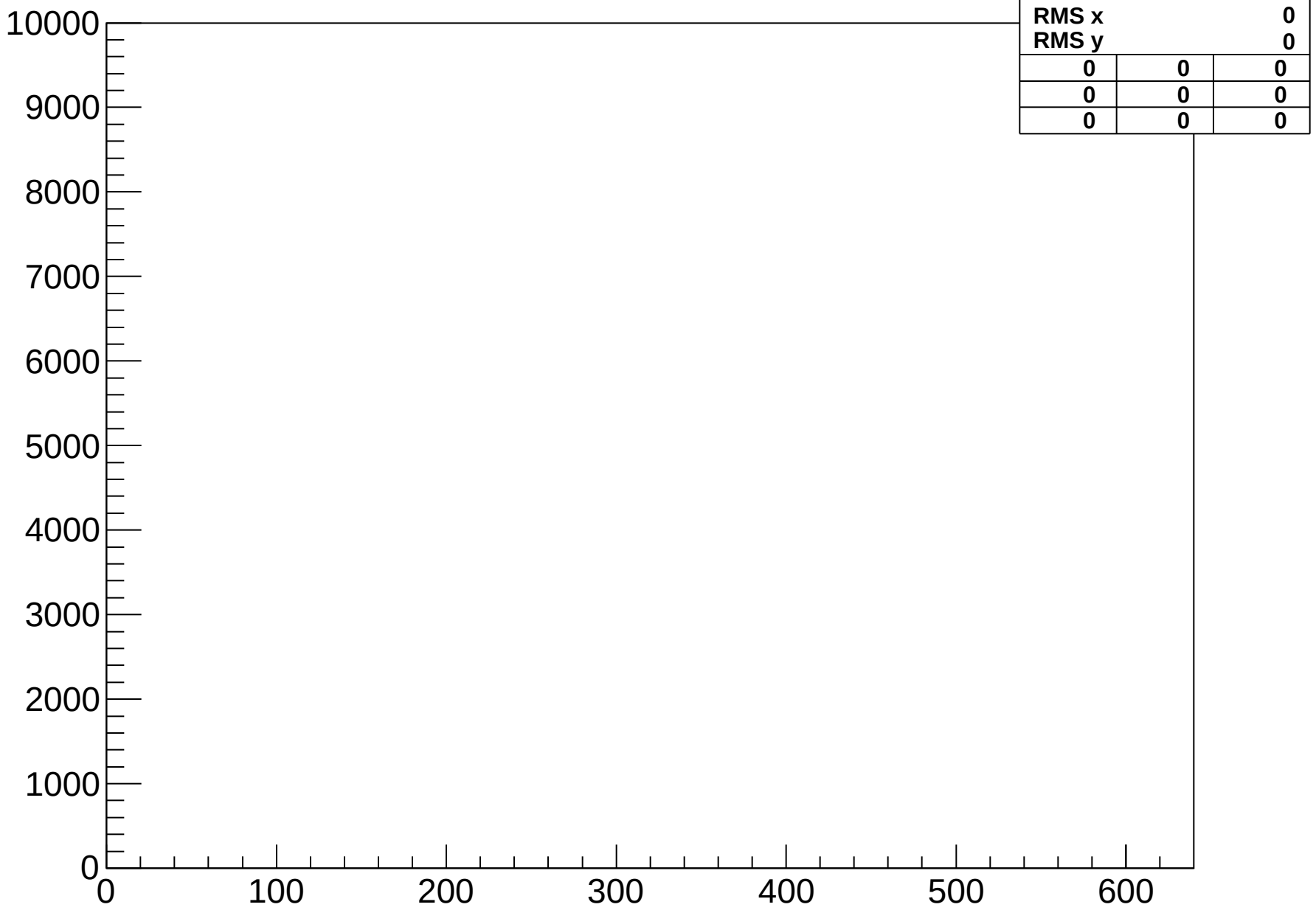
baselinesamples-fpga-6-hyb-3-sample-3



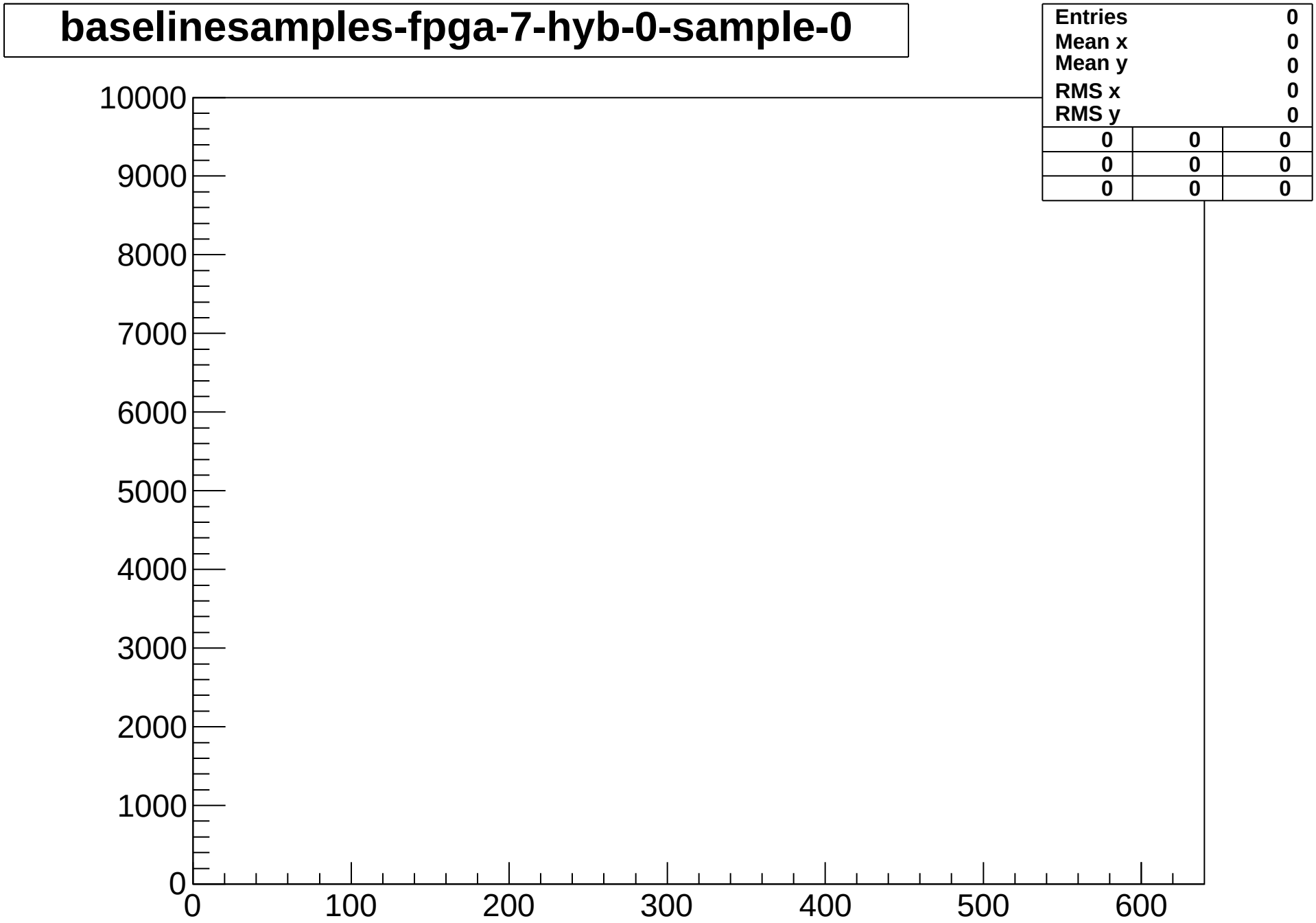
baselinesamples-fpga-6-hyb-3-sample-4



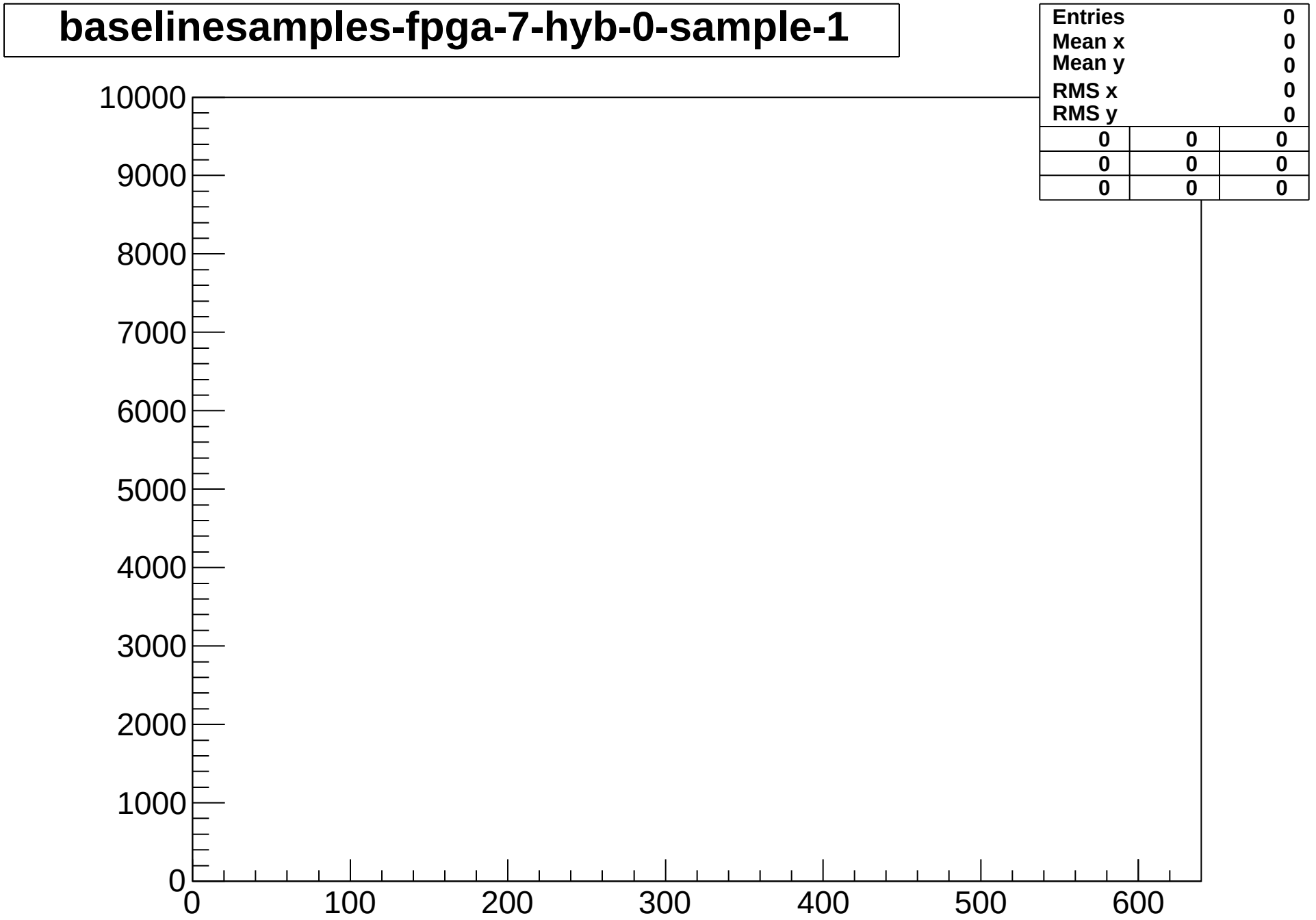
baselinesamples-fpga-6-hyb-3-sample-5



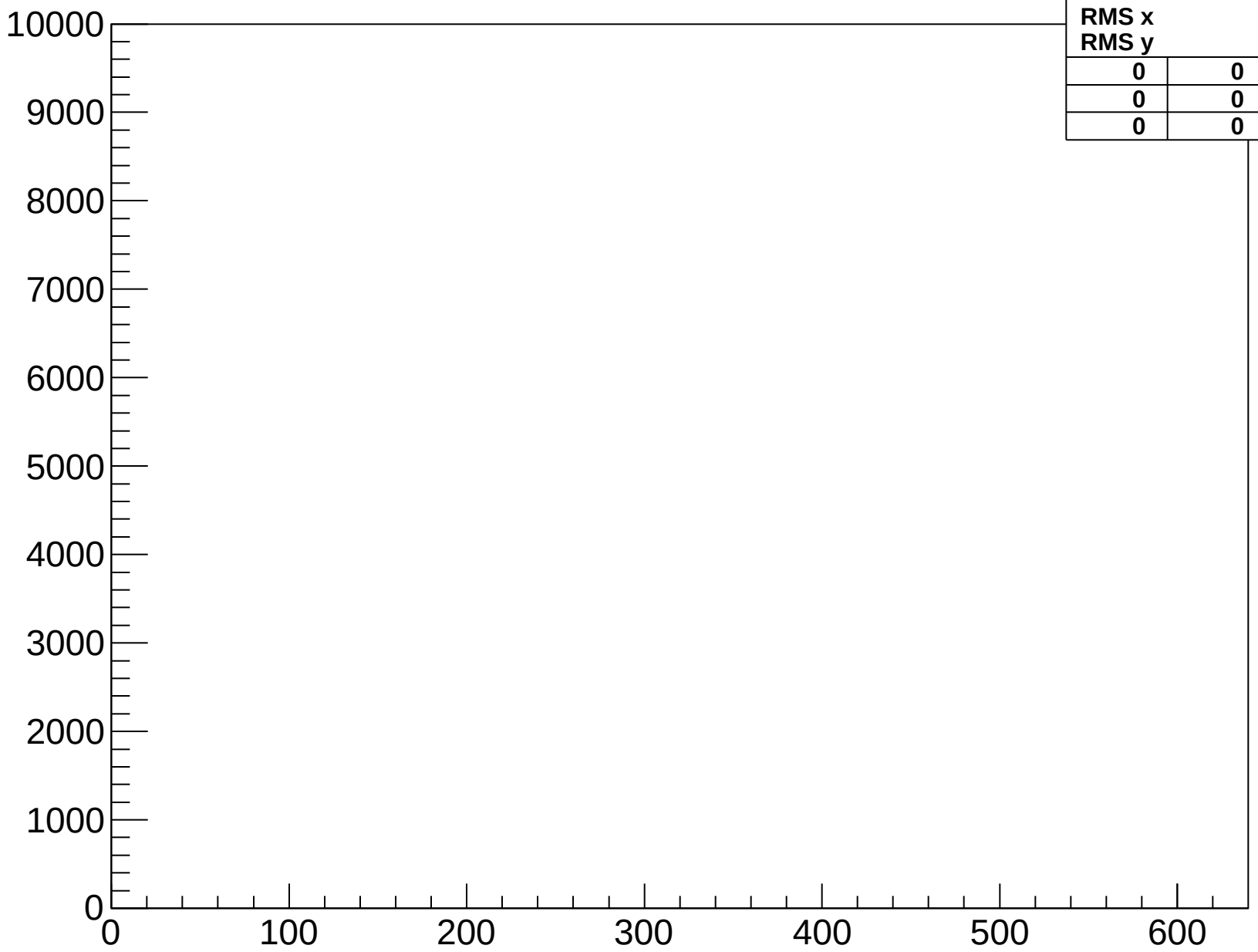
baselinesamples-fpga-7-hyb-0-sample-0



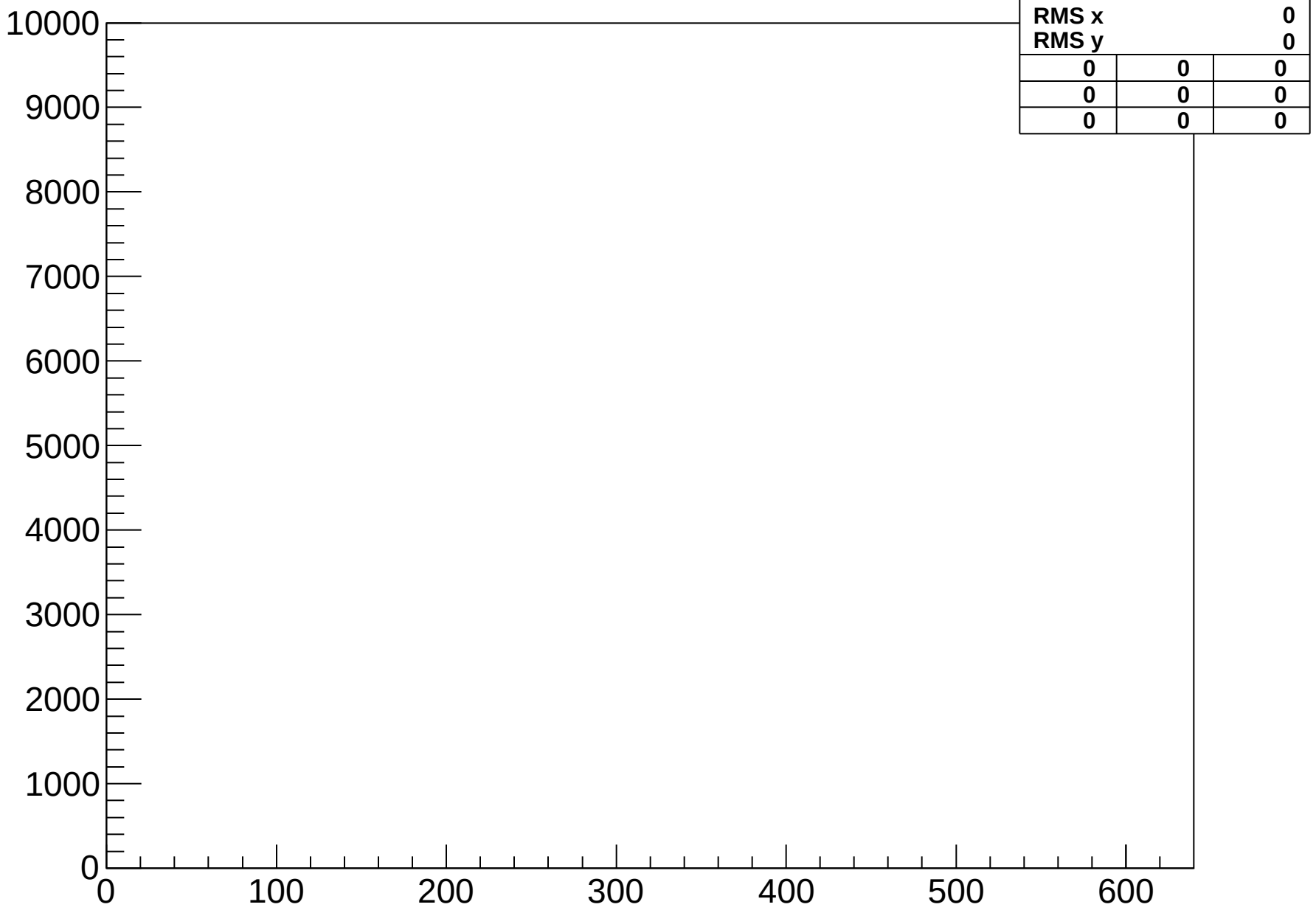
baselinesamples-fpga-7-hyb-0-sample-1



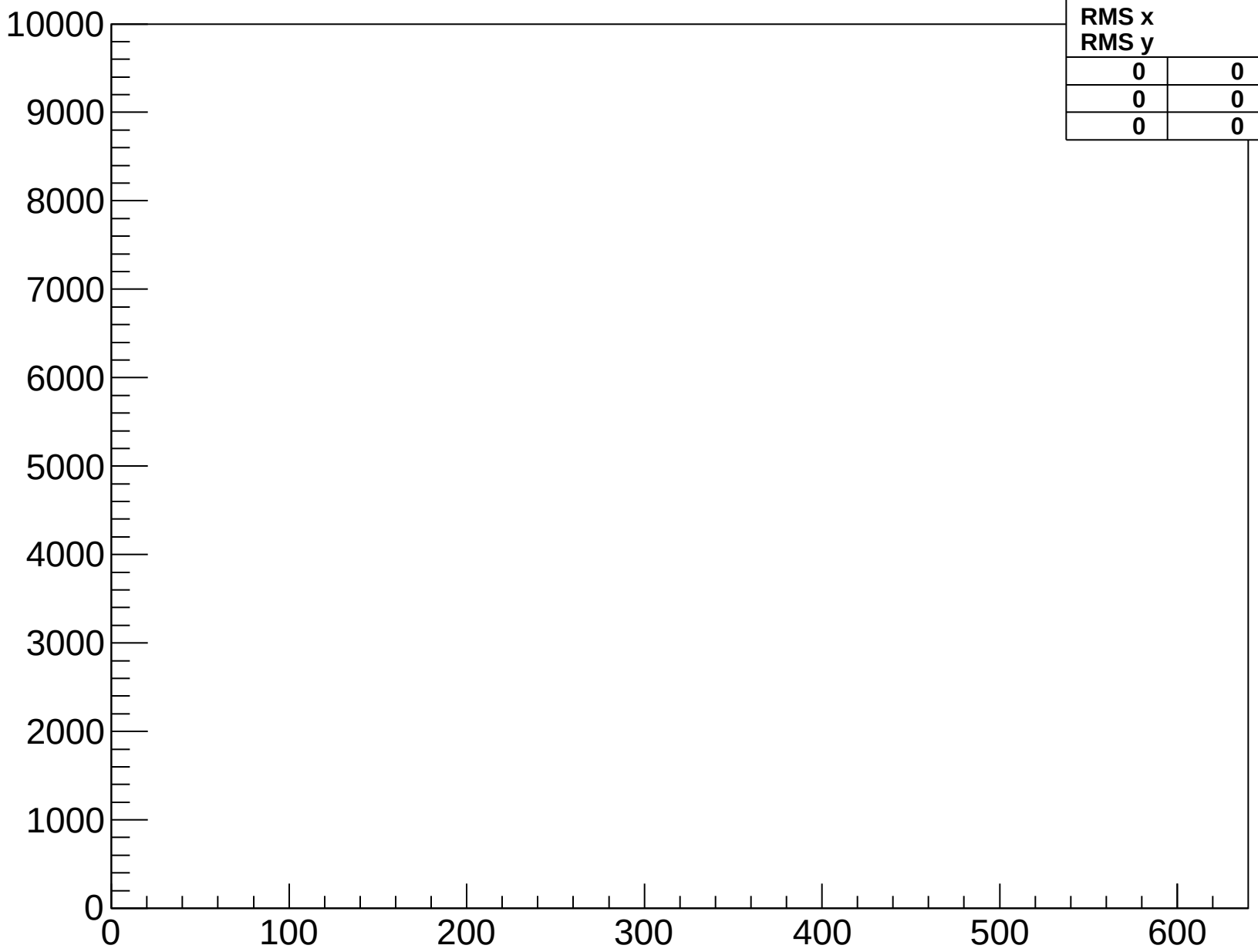
baselinesamples-fpga-7-hyb-0-sample-2



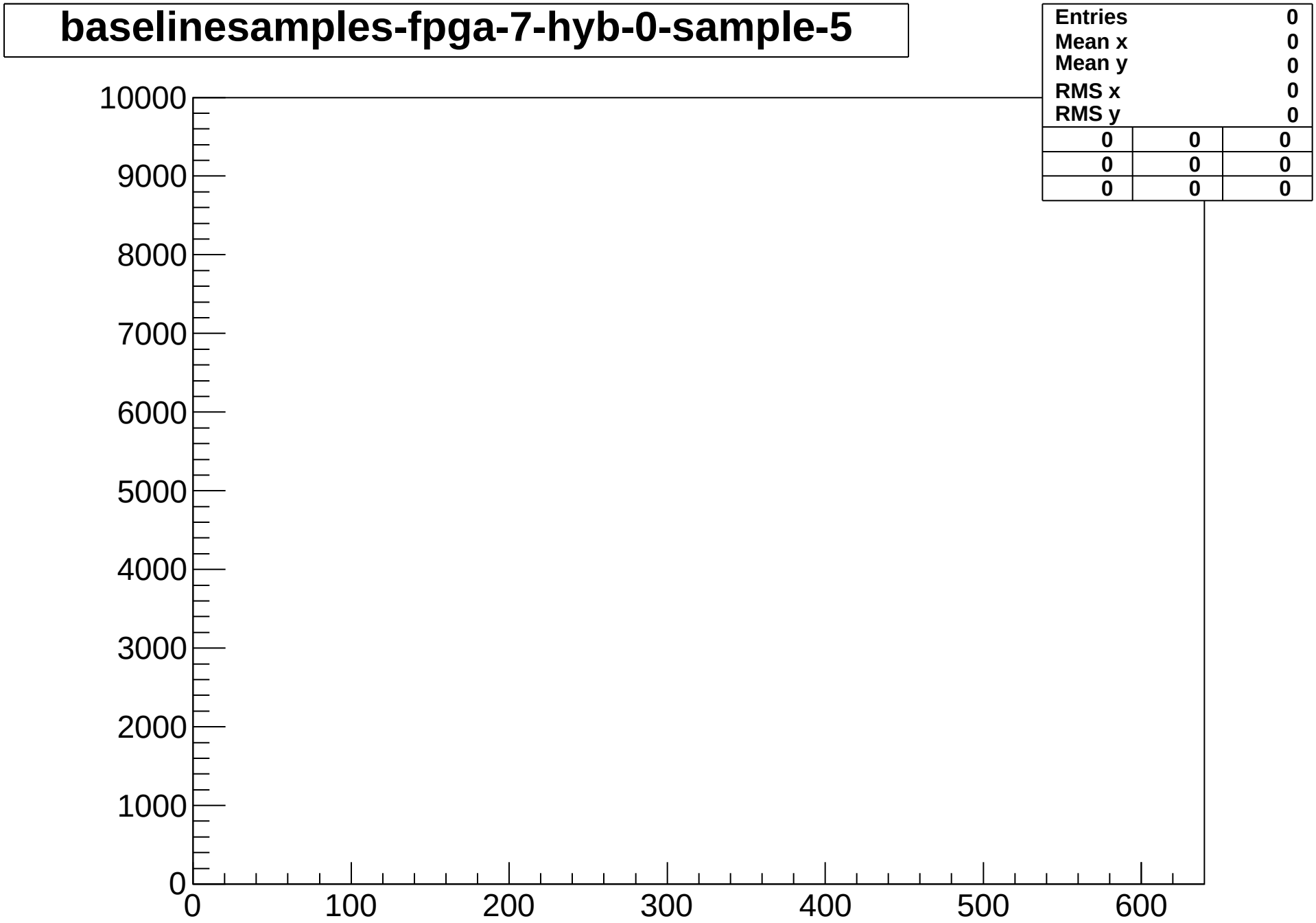
baselinesamples-fpga-7-hyb-0-sample-3



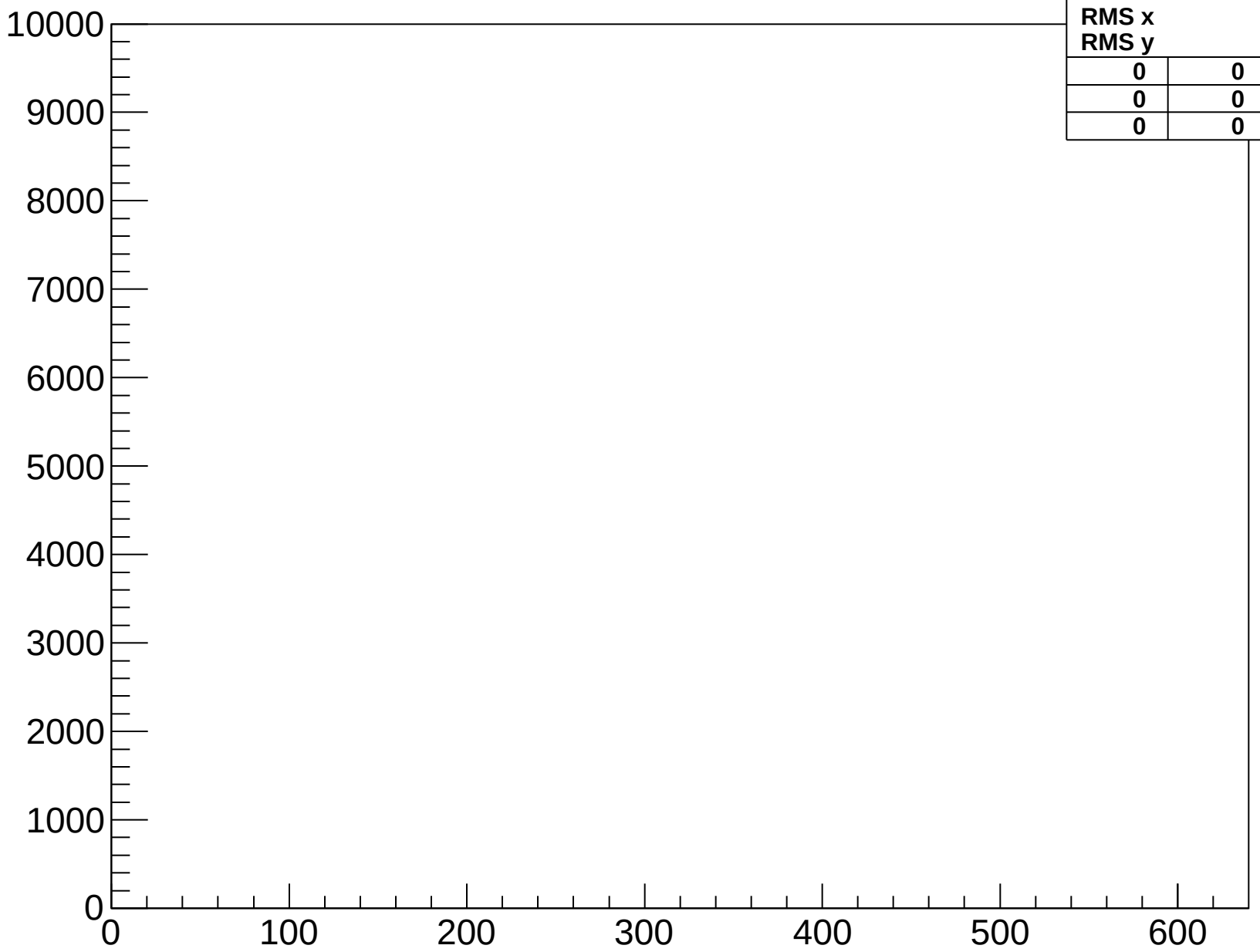
baselinesamples-fpga-7-hyb-0-sample-4



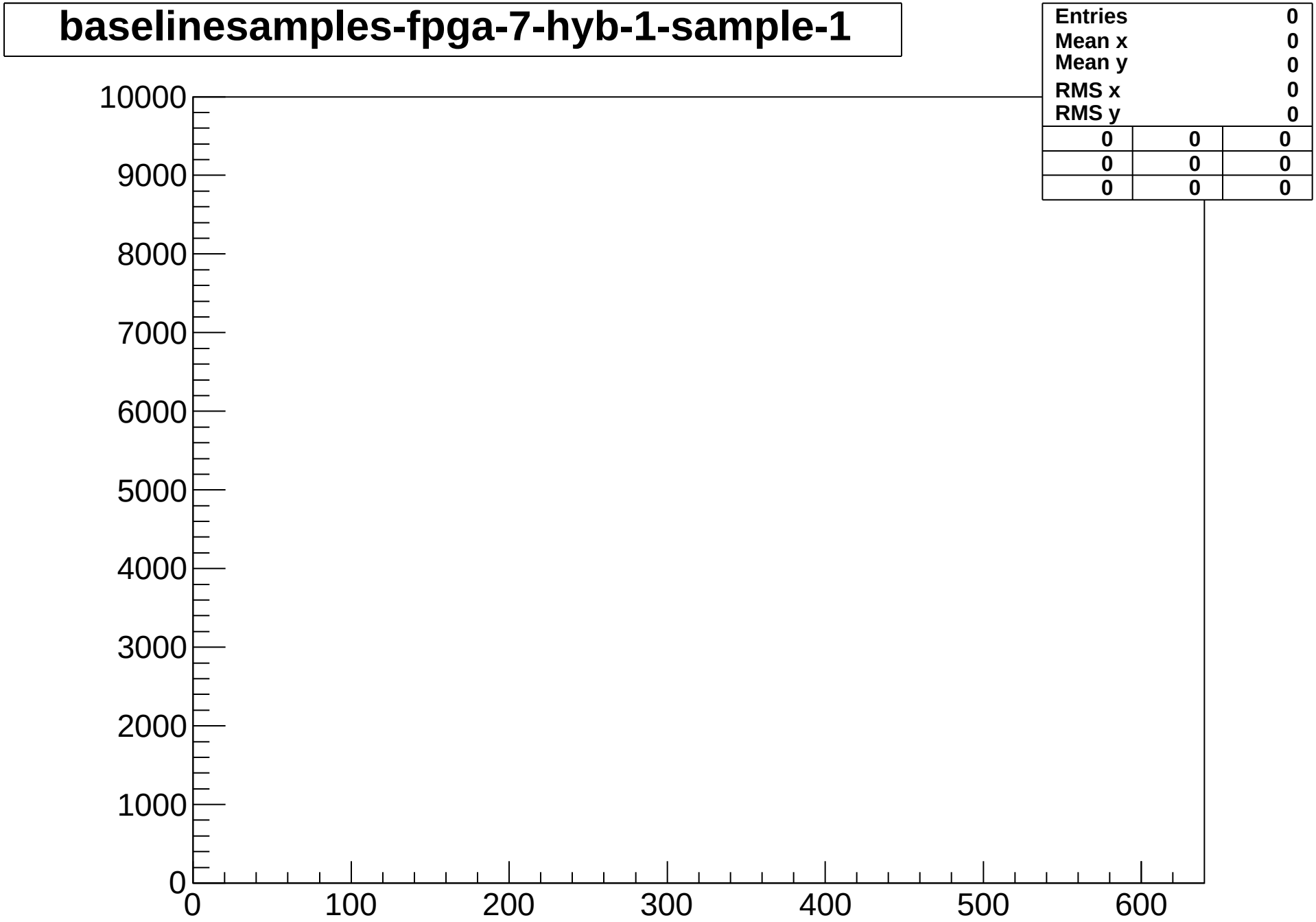
baselinesamples-fpga-7-hyb-0-sample-5



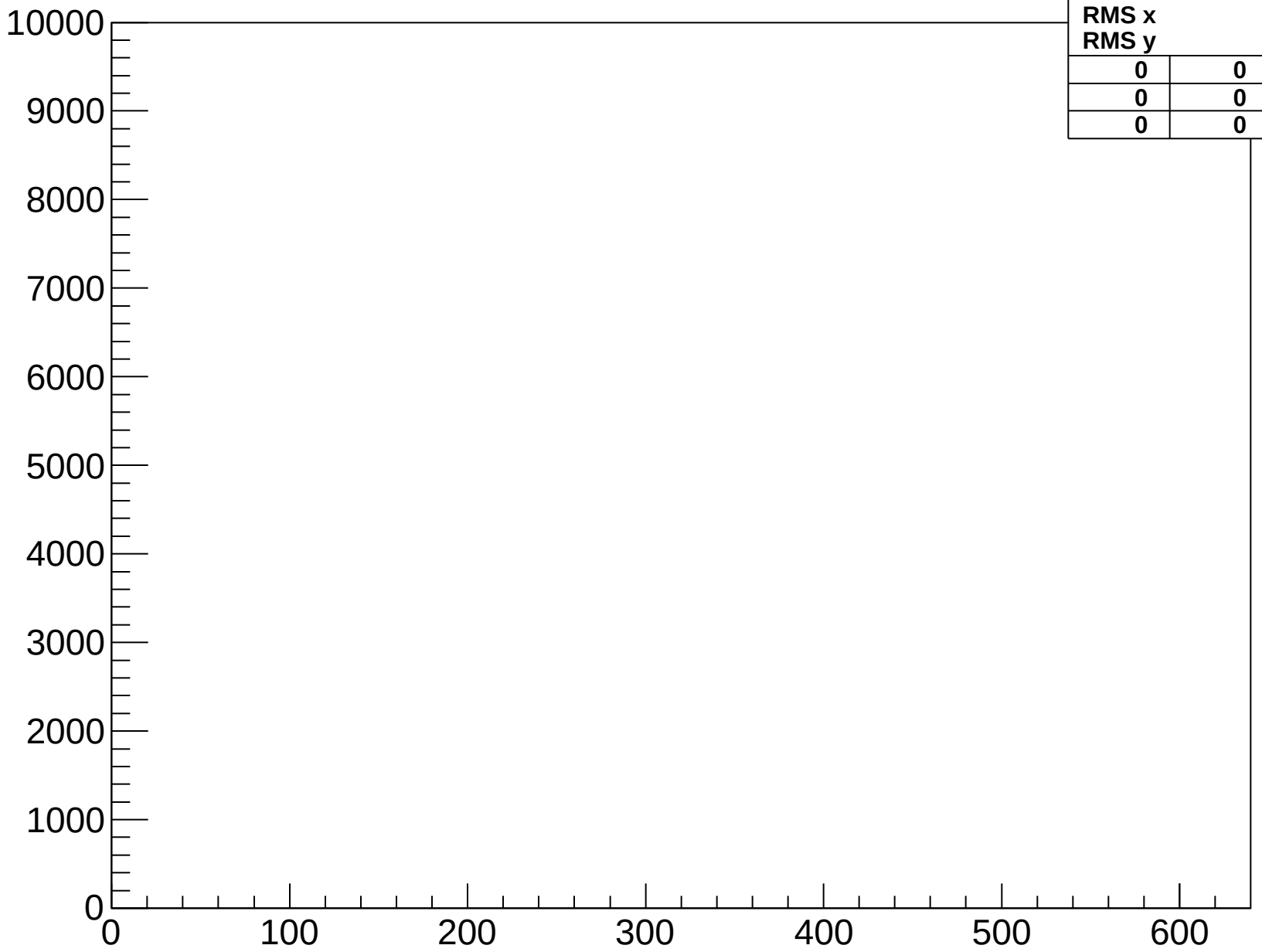
baselinesamples-fpga-7-hyb-1-sample-0



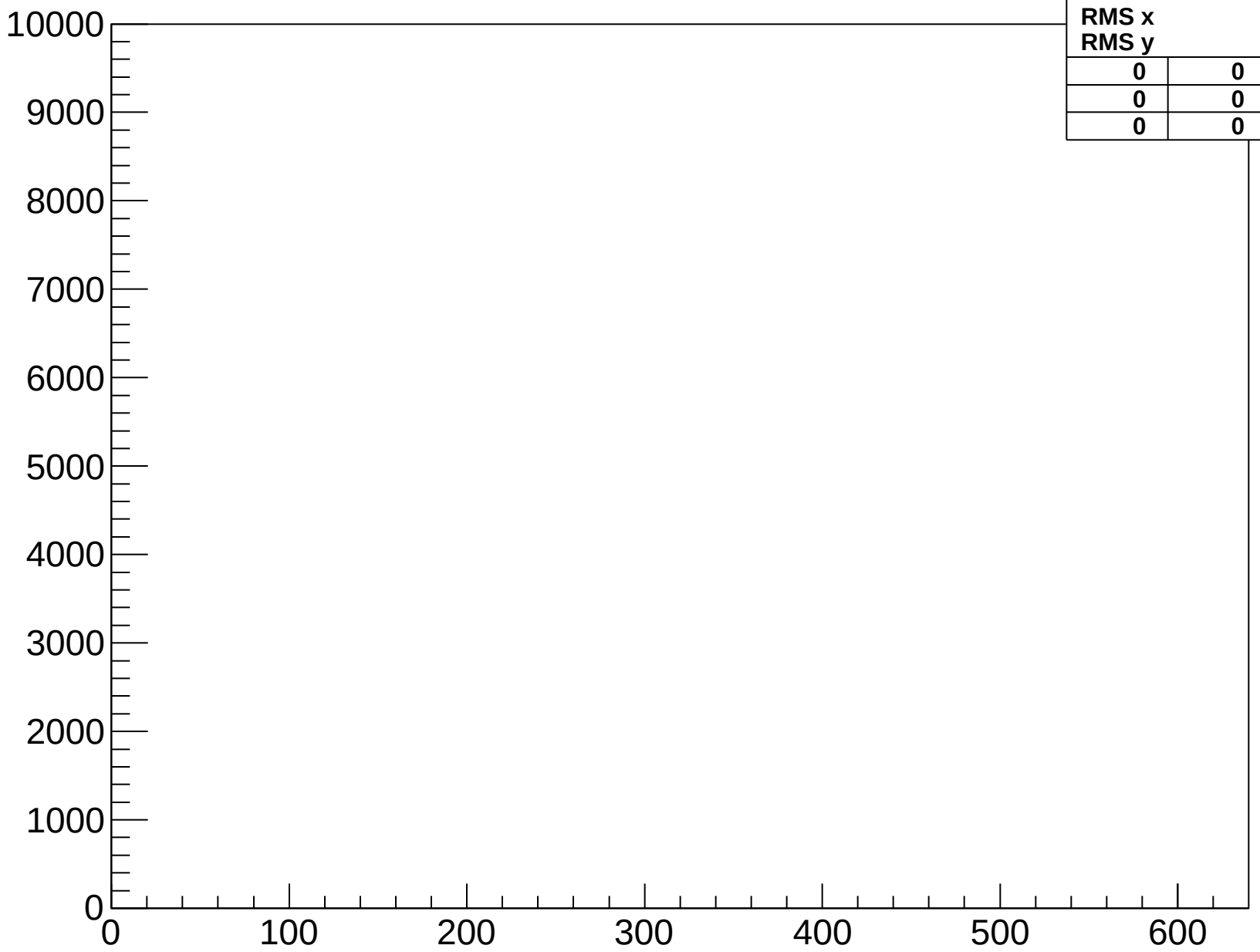
baselinesamples-fpga-7-hyb-1-sample-1



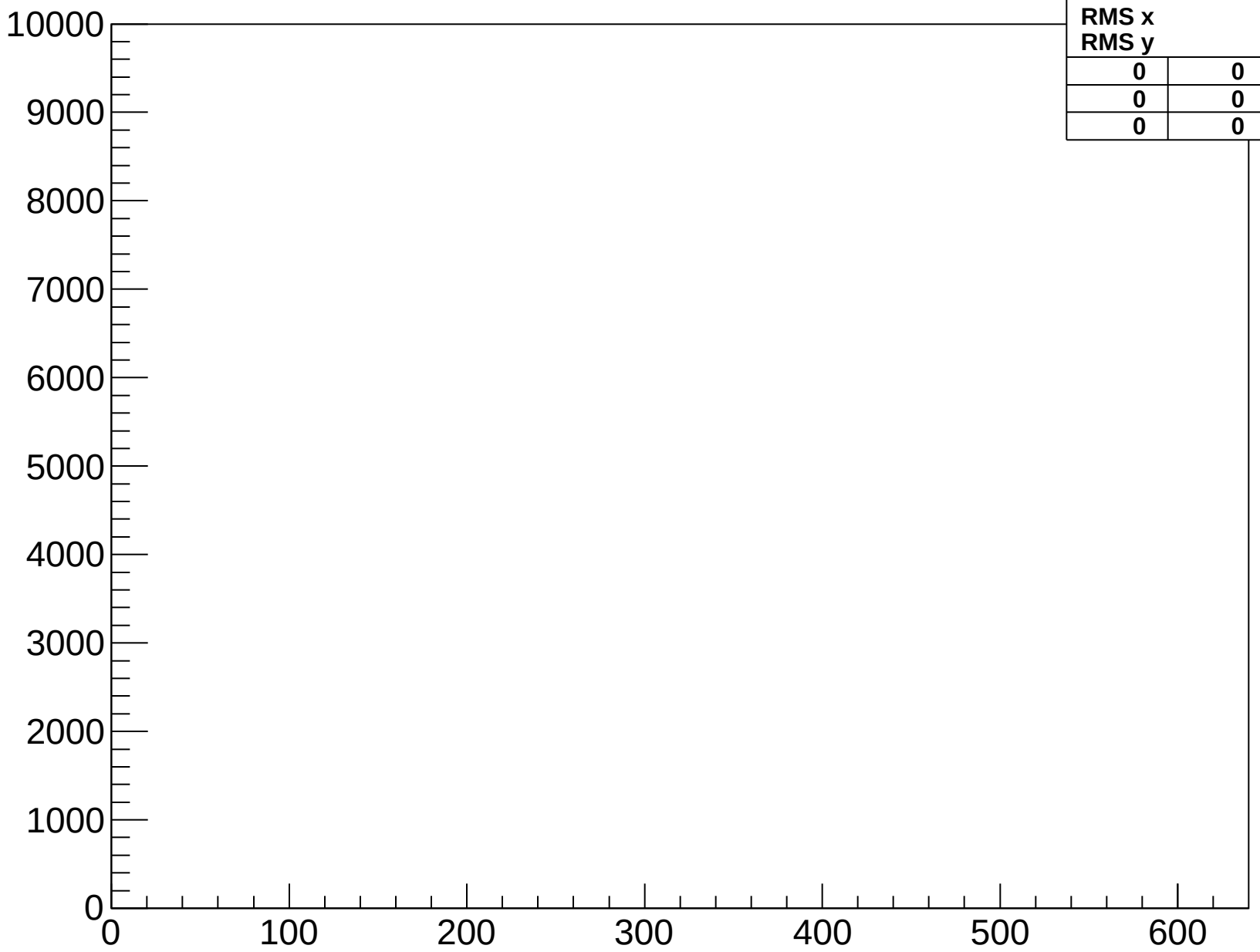
baselinesamples-fpga-7-hyb-1-sample-2



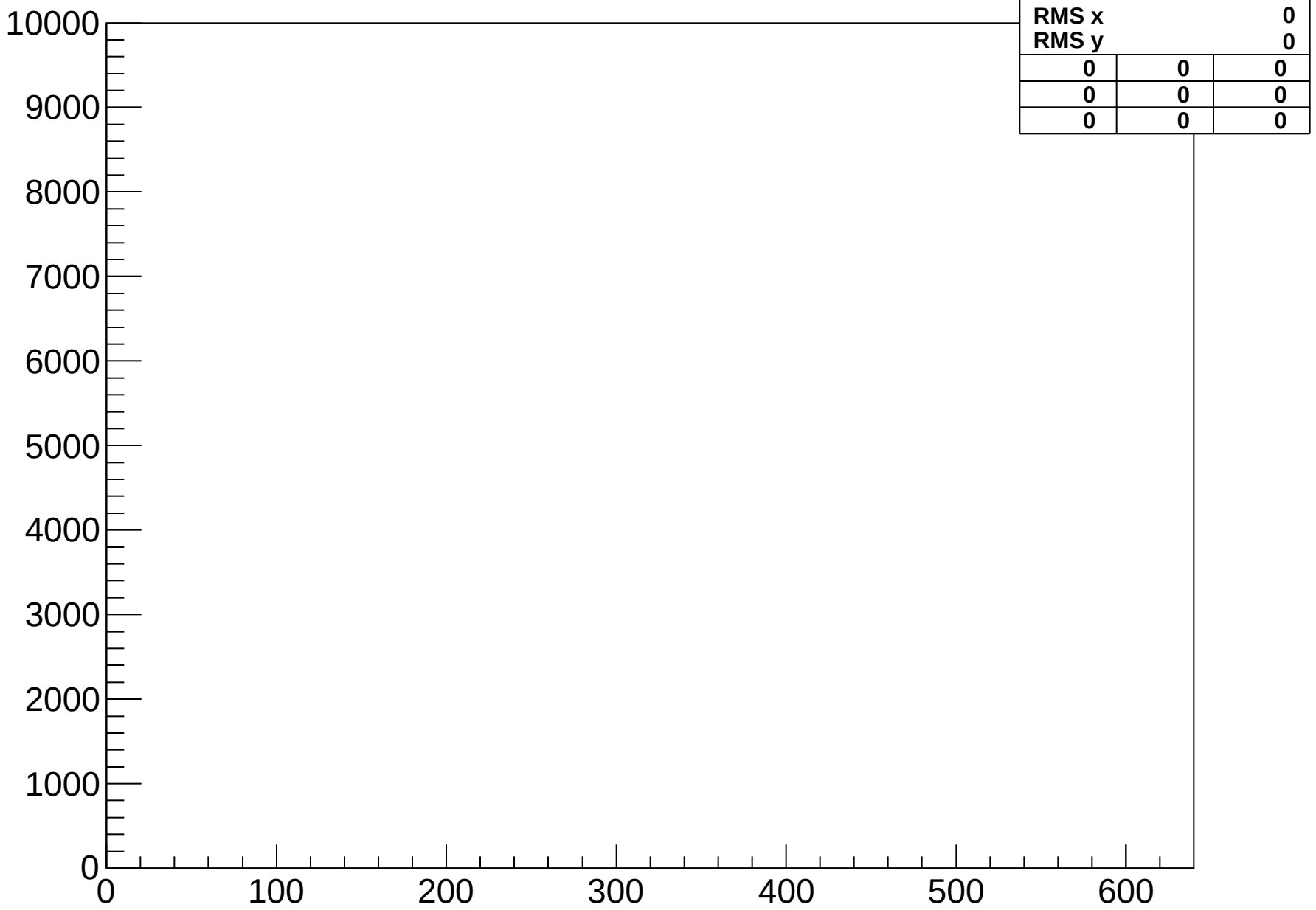
baselinesamples-fpga-7-hyb-1-sample-3



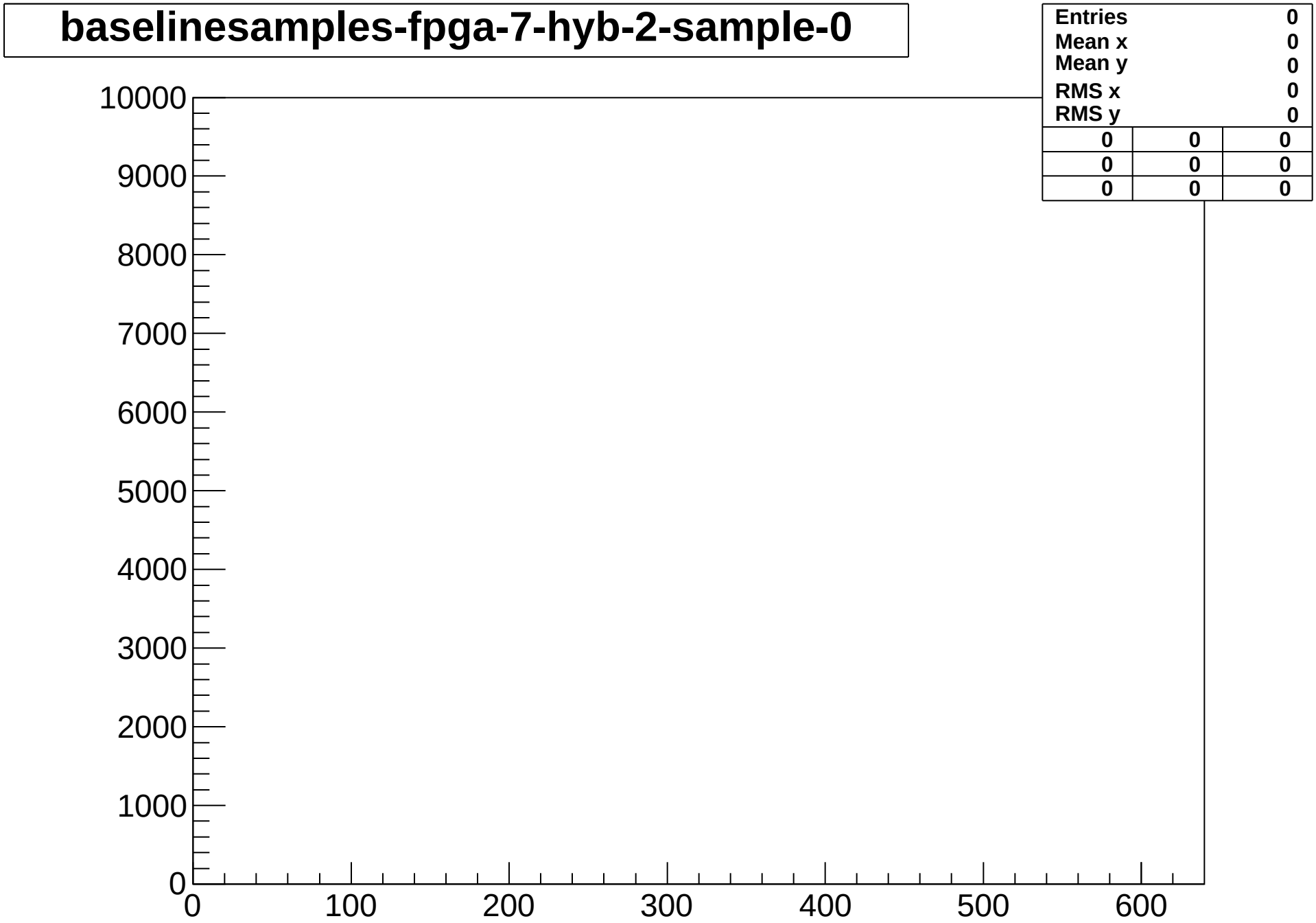
baselinesamples-fpga-7-hyb-1-sample-4



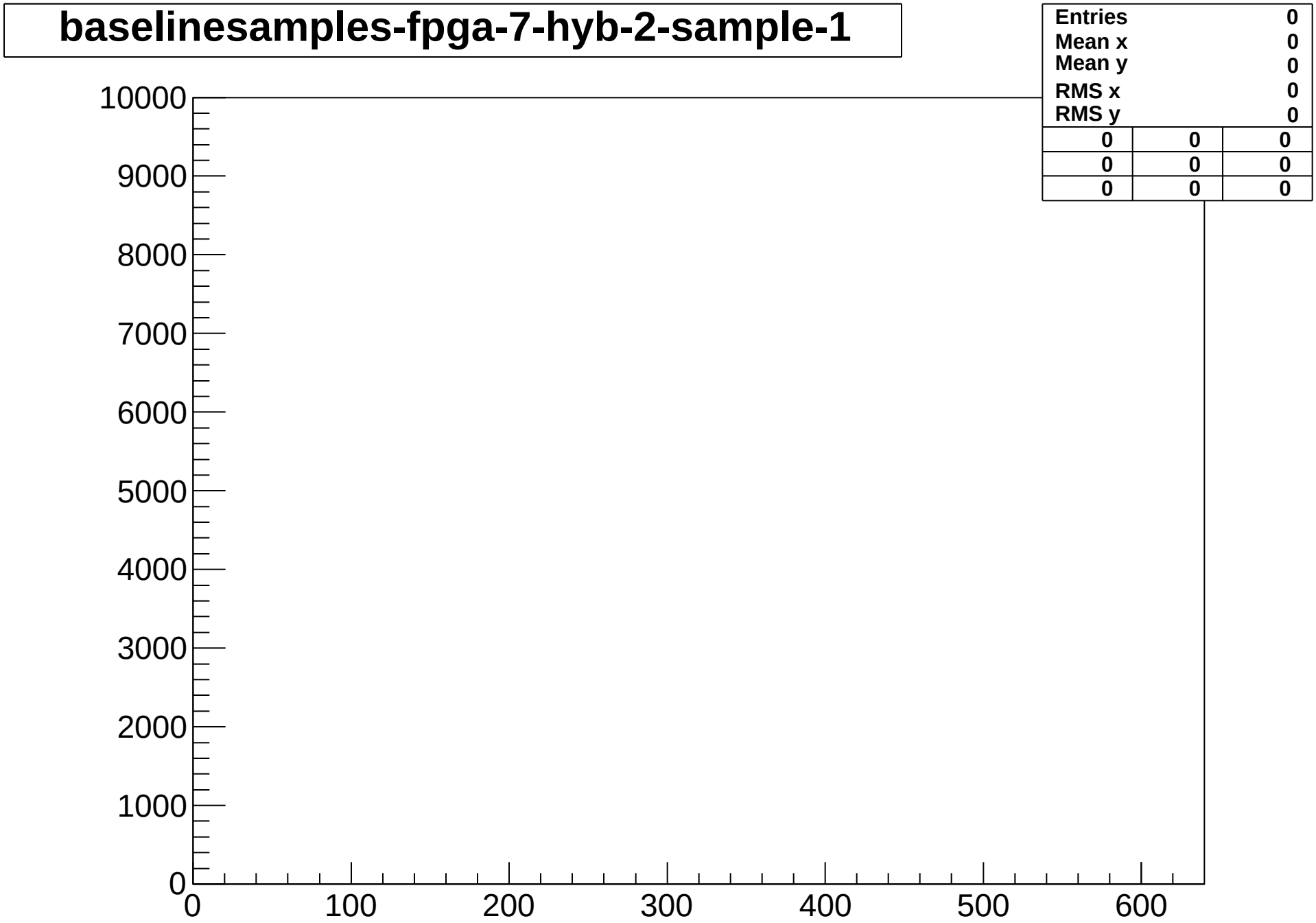
baselinesamples-fpga-7-hyb-1-sample-5



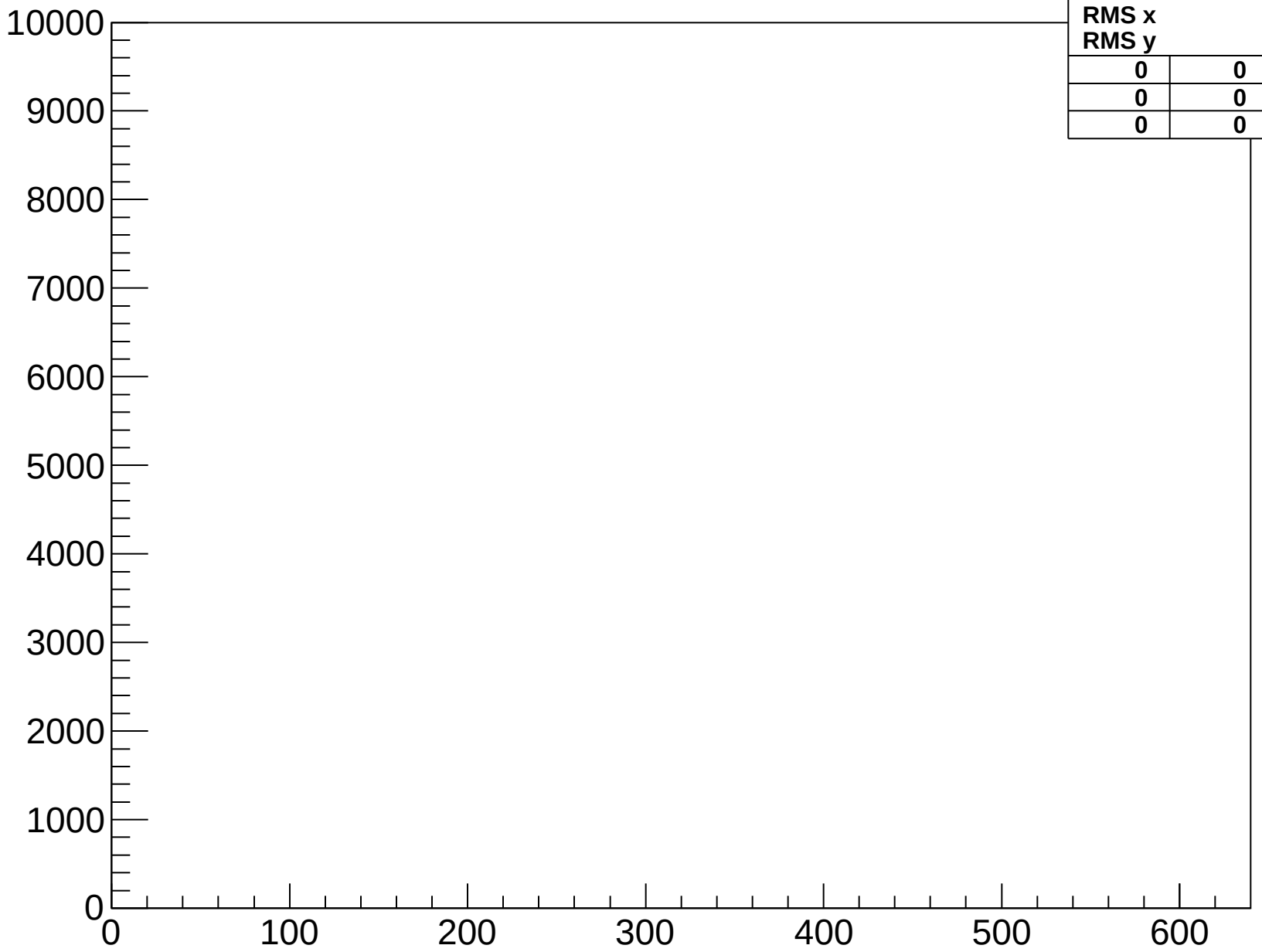
baselinesamples-fpga-7-hyb-2-sample-0



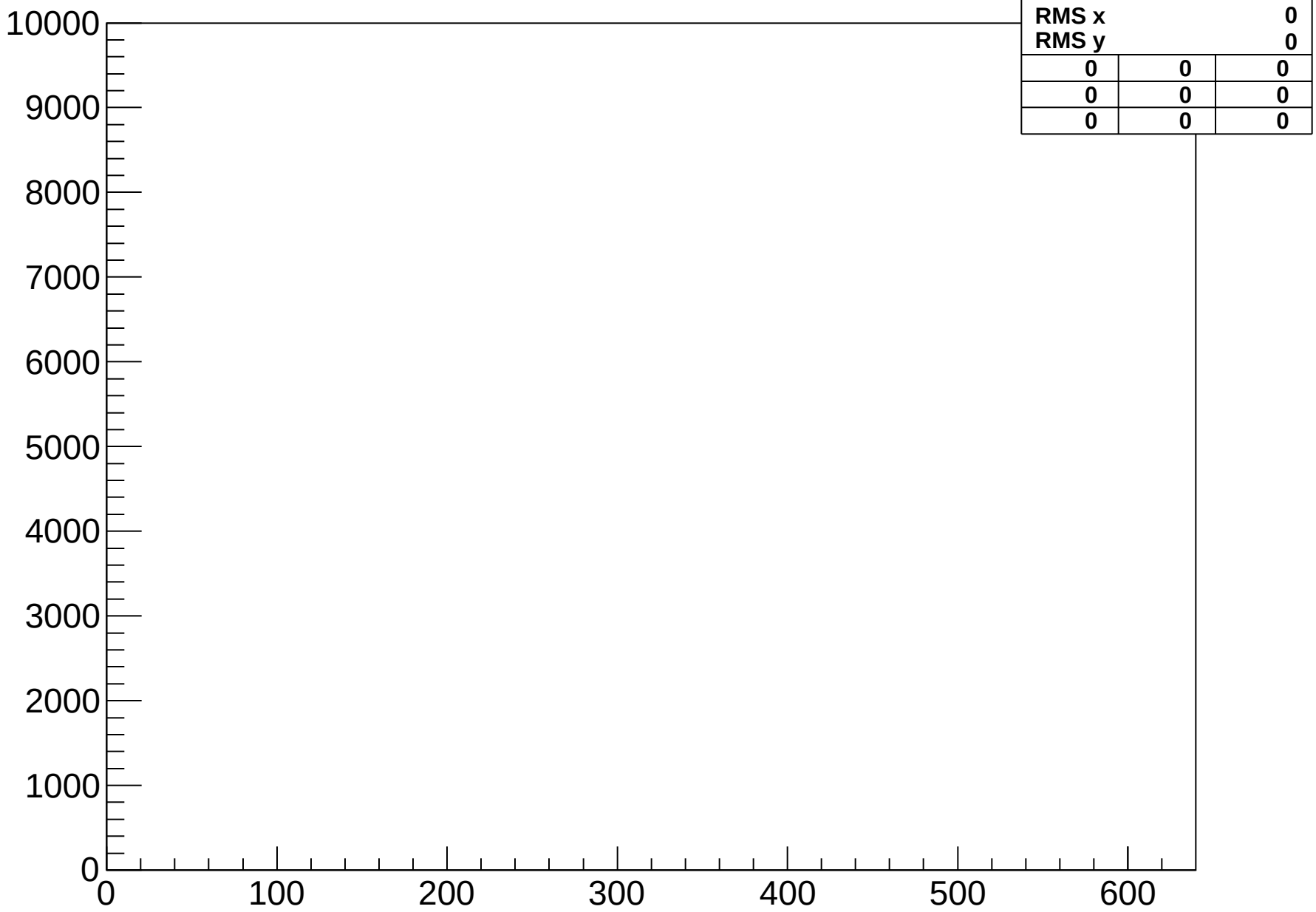
baselinesamples-fpga-7-hyb-2-sample-1



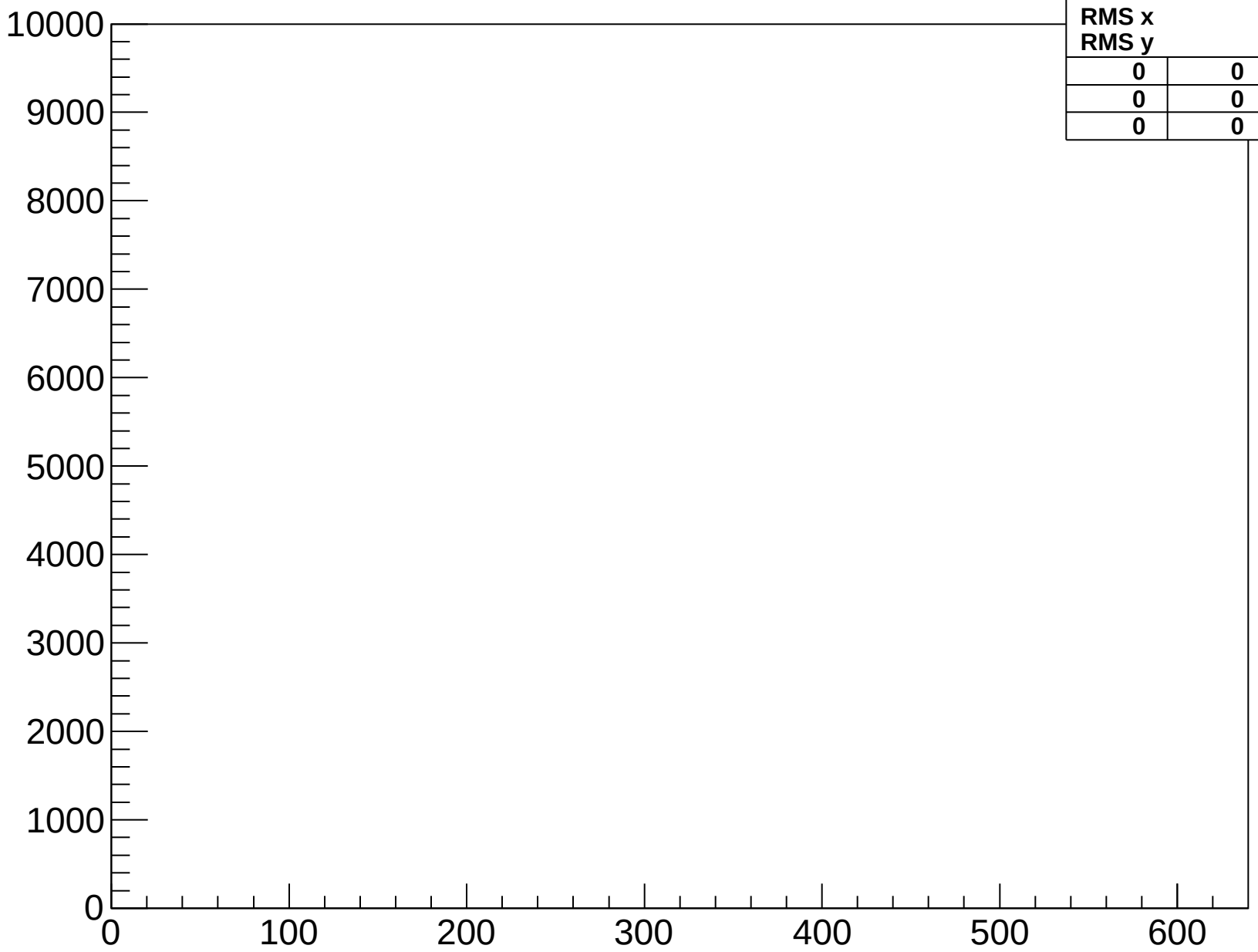
baselinesamples-fpga-7-hyb-2-sample-2



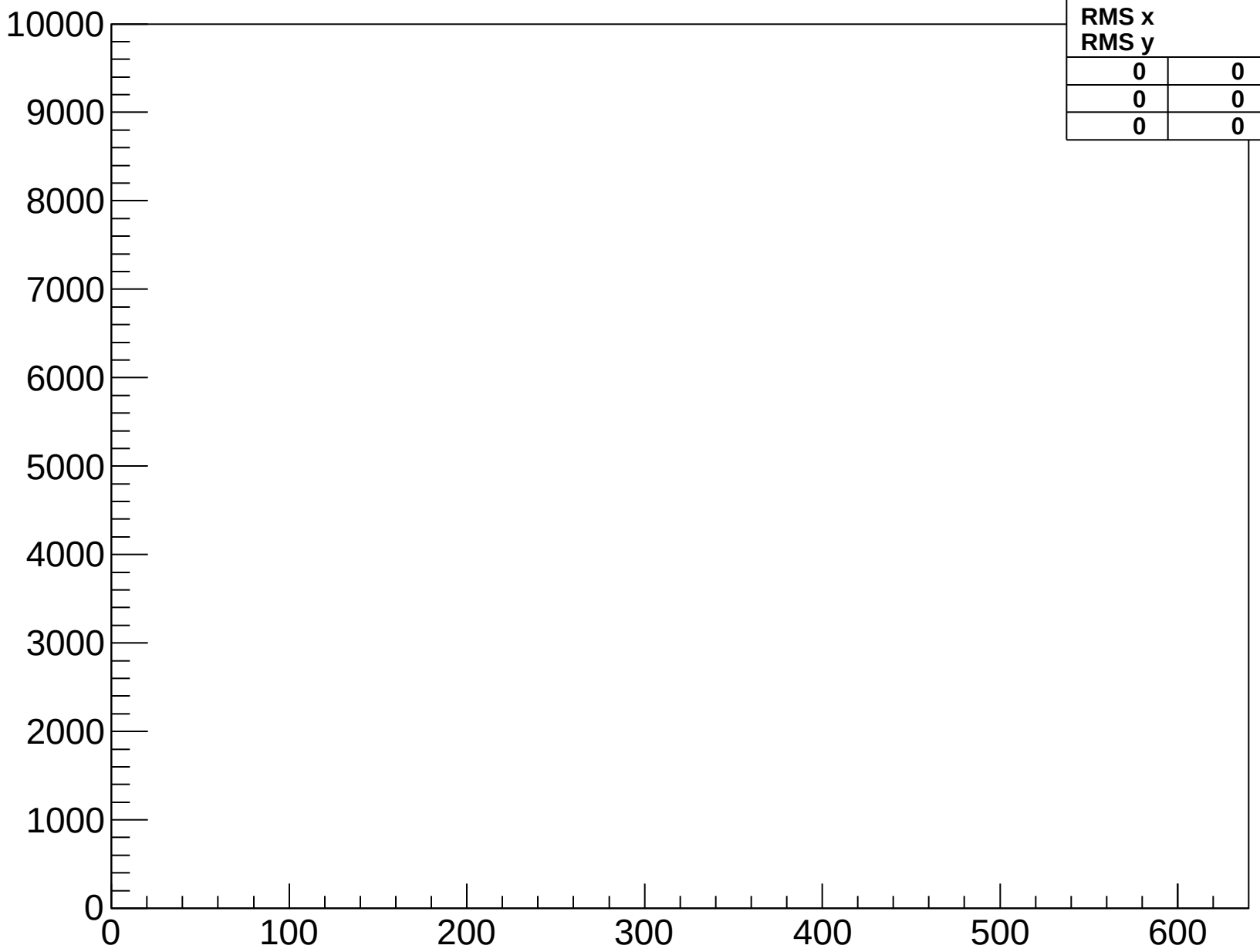
baselinesamples-fpga-7-hyb-2-sample-3



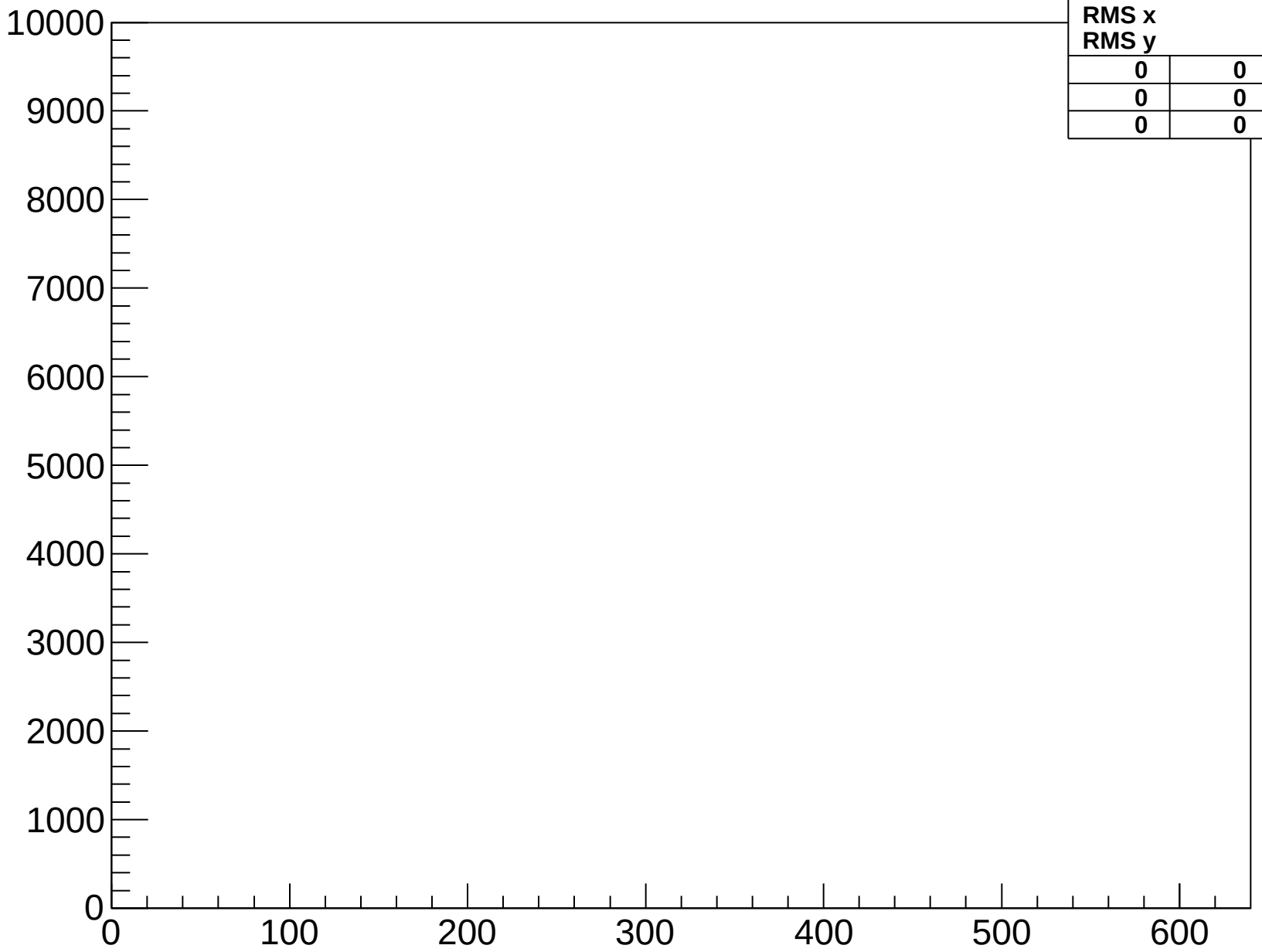
baselinesamples-fpga-7-hyb-2-sample-4



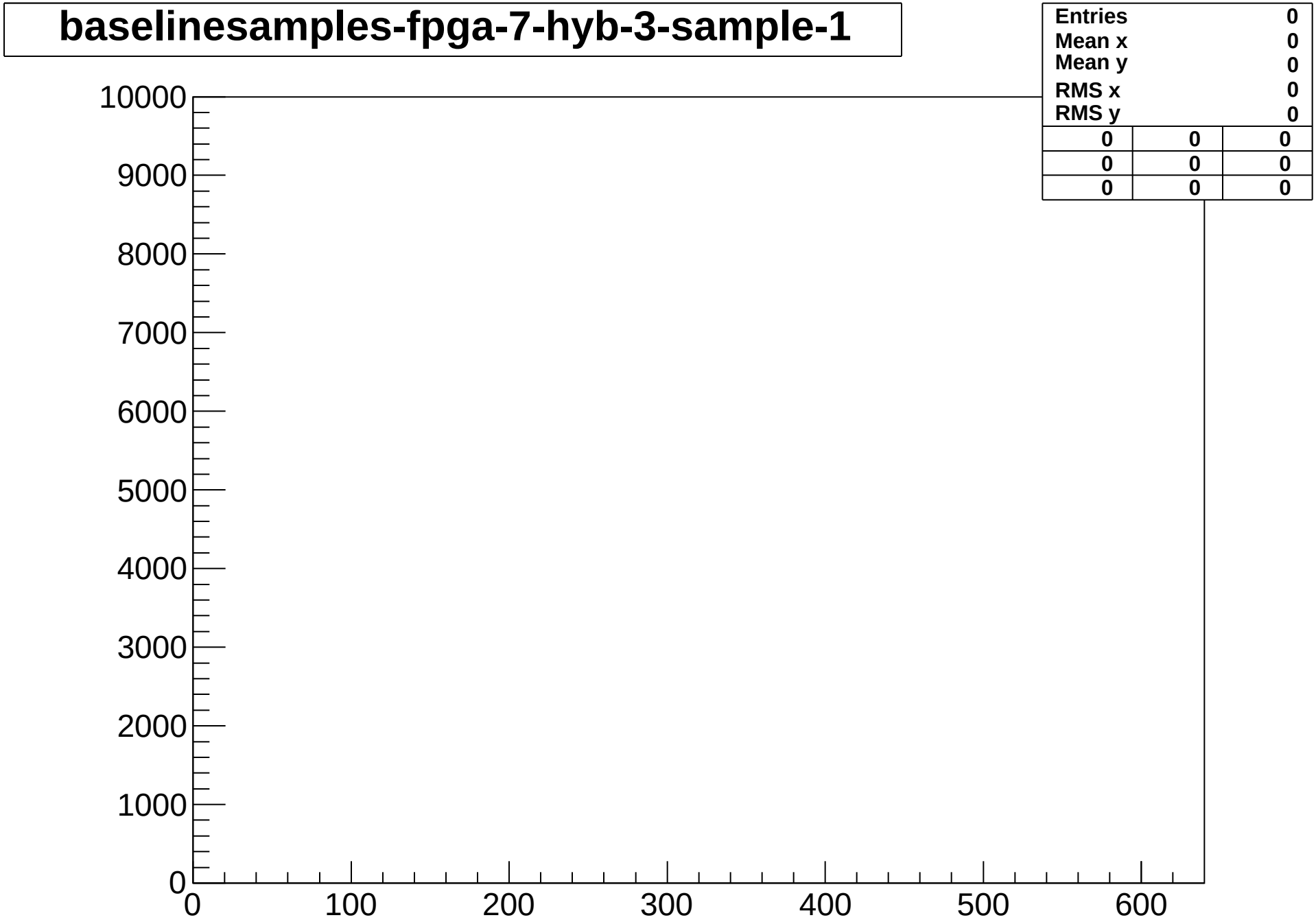
baselinesamples-fpga-7-hyb-2-sample-5



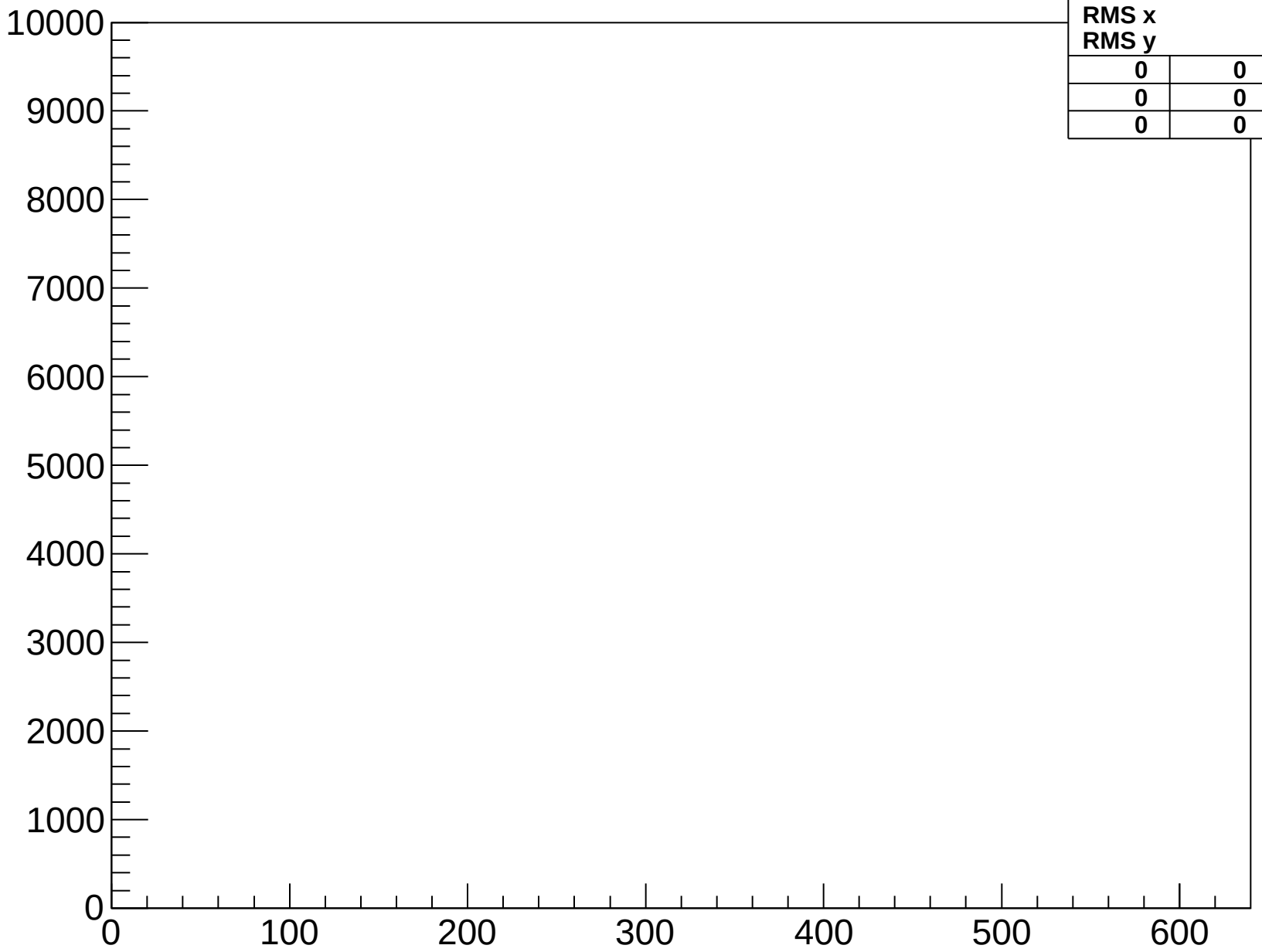
baselinesamples-fpga-7-hyb-3-sample-0



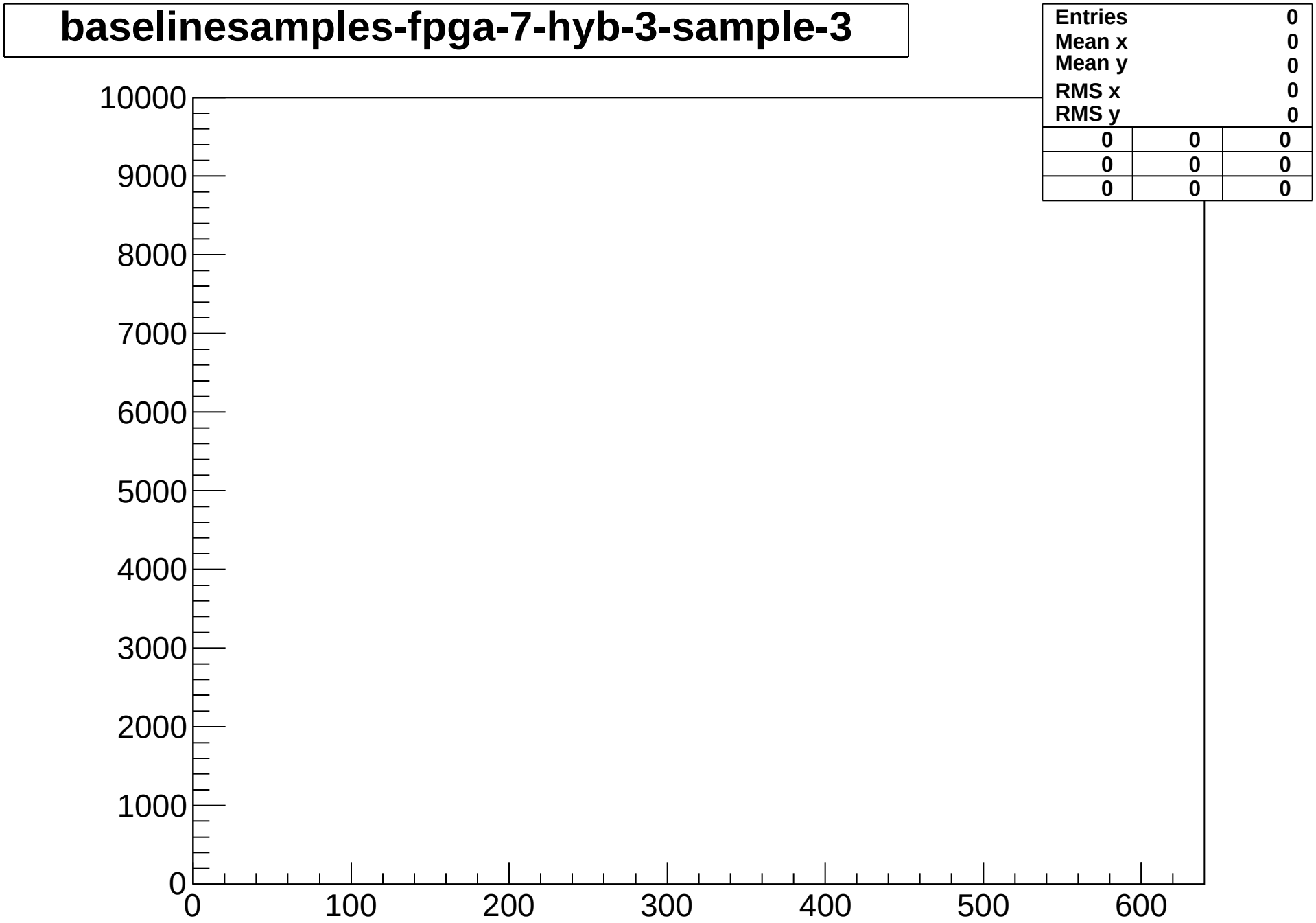
baselinesamples-fpga-7-hyb-3-sample-1



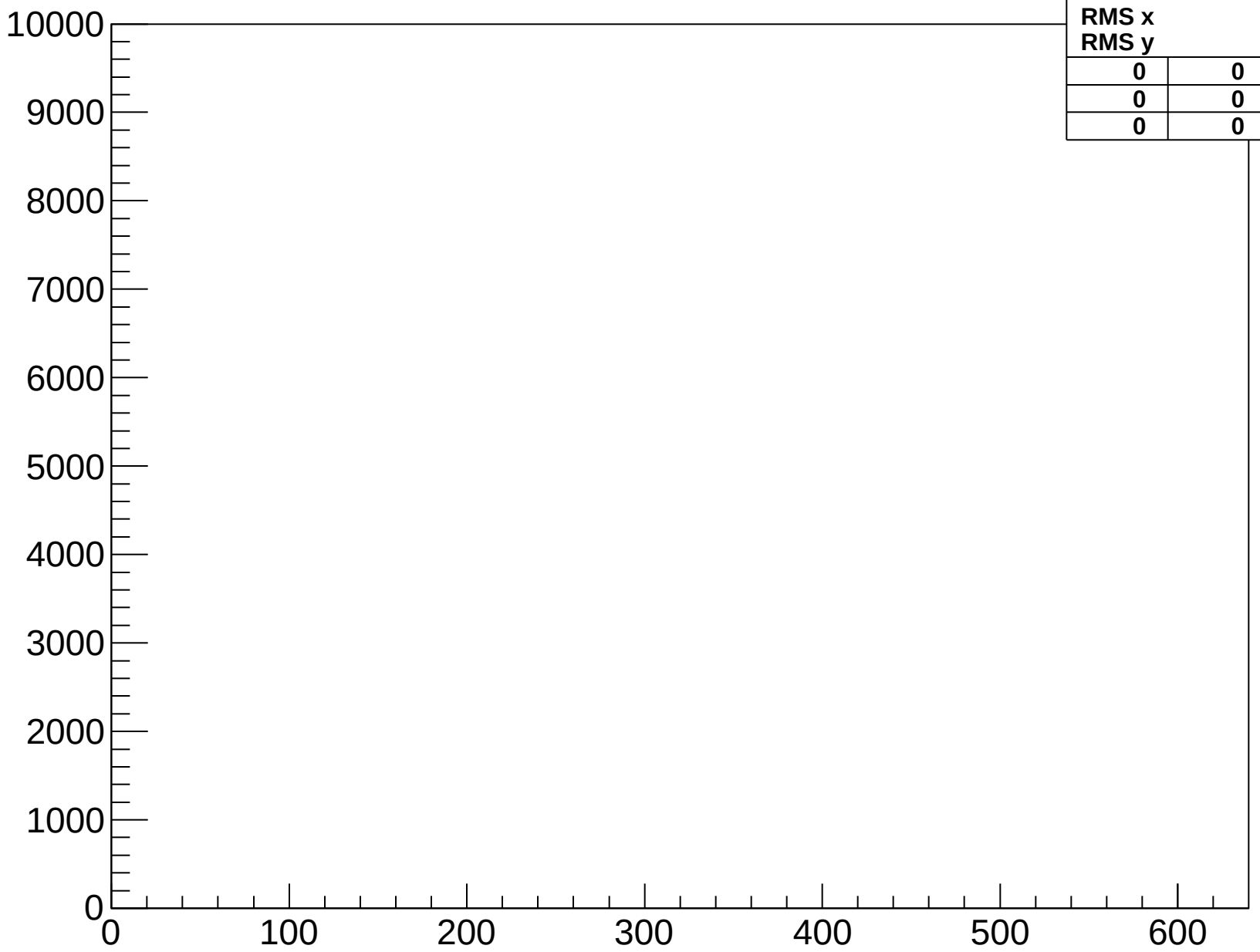
baselinesamples-fpga-7-hyb-3-sample-2



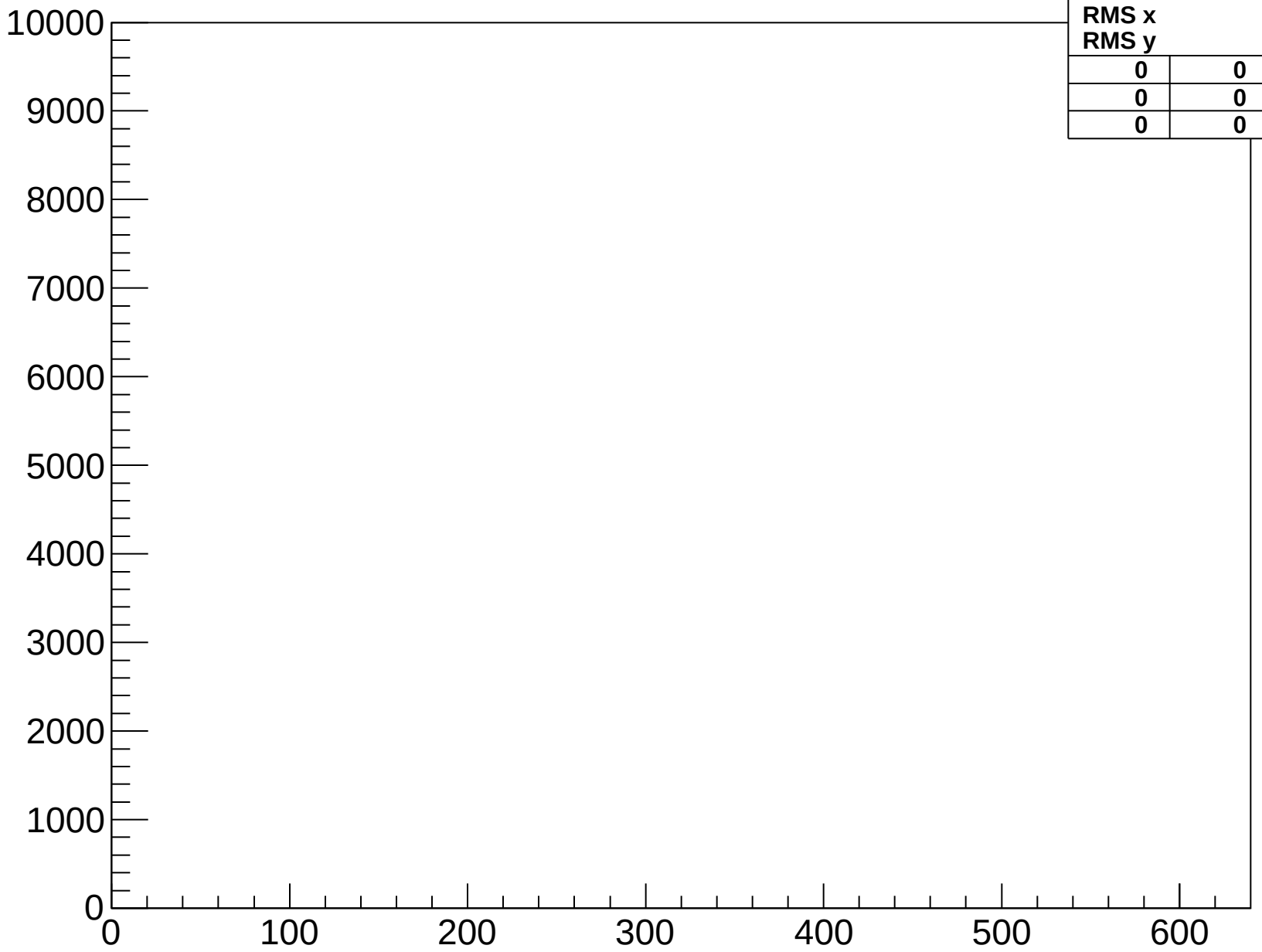
baselinesamples-fpga-7-hyb-3-sample-3



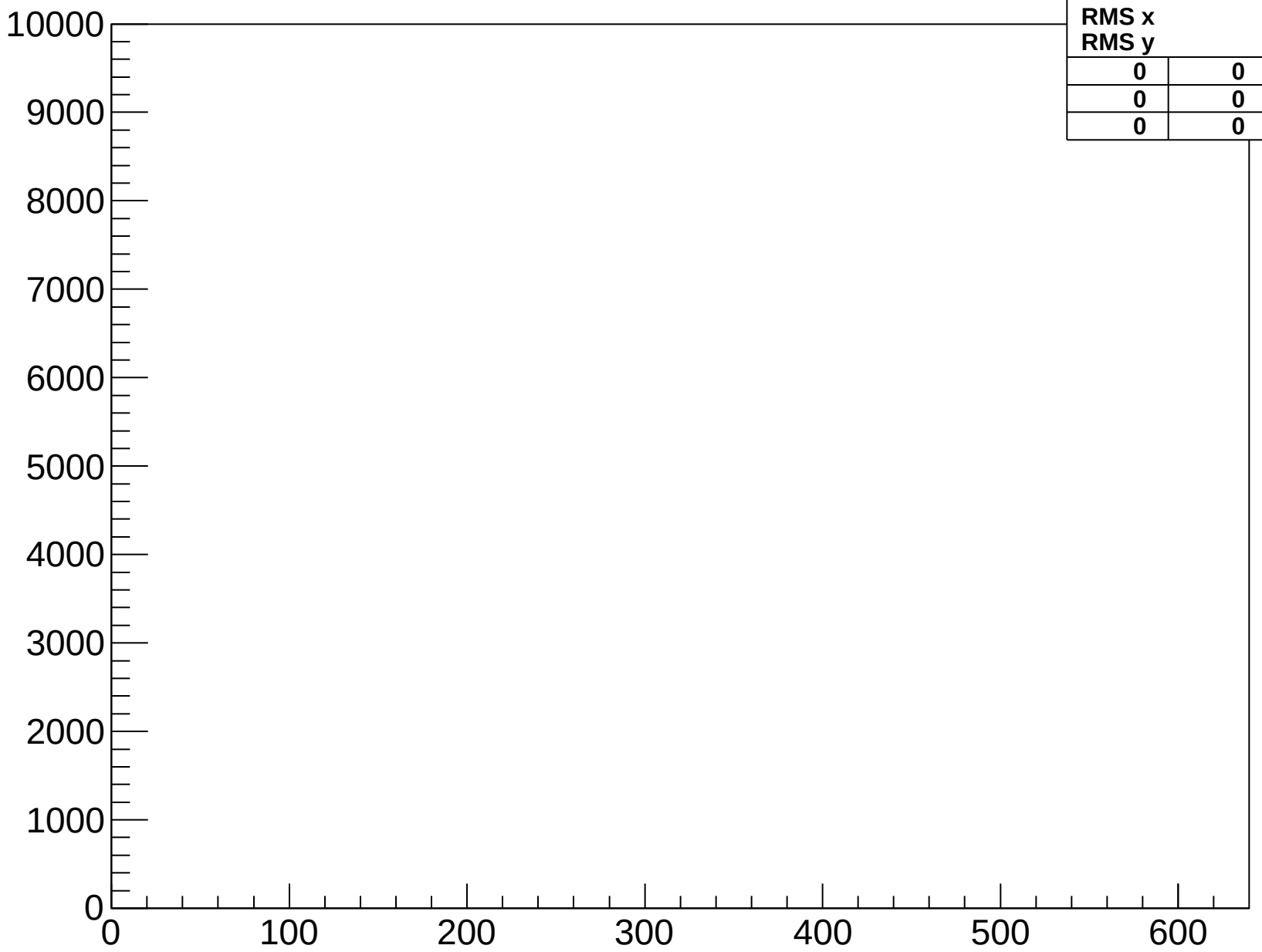
baselinesamples-fpga-7-hyb-3-sample-4



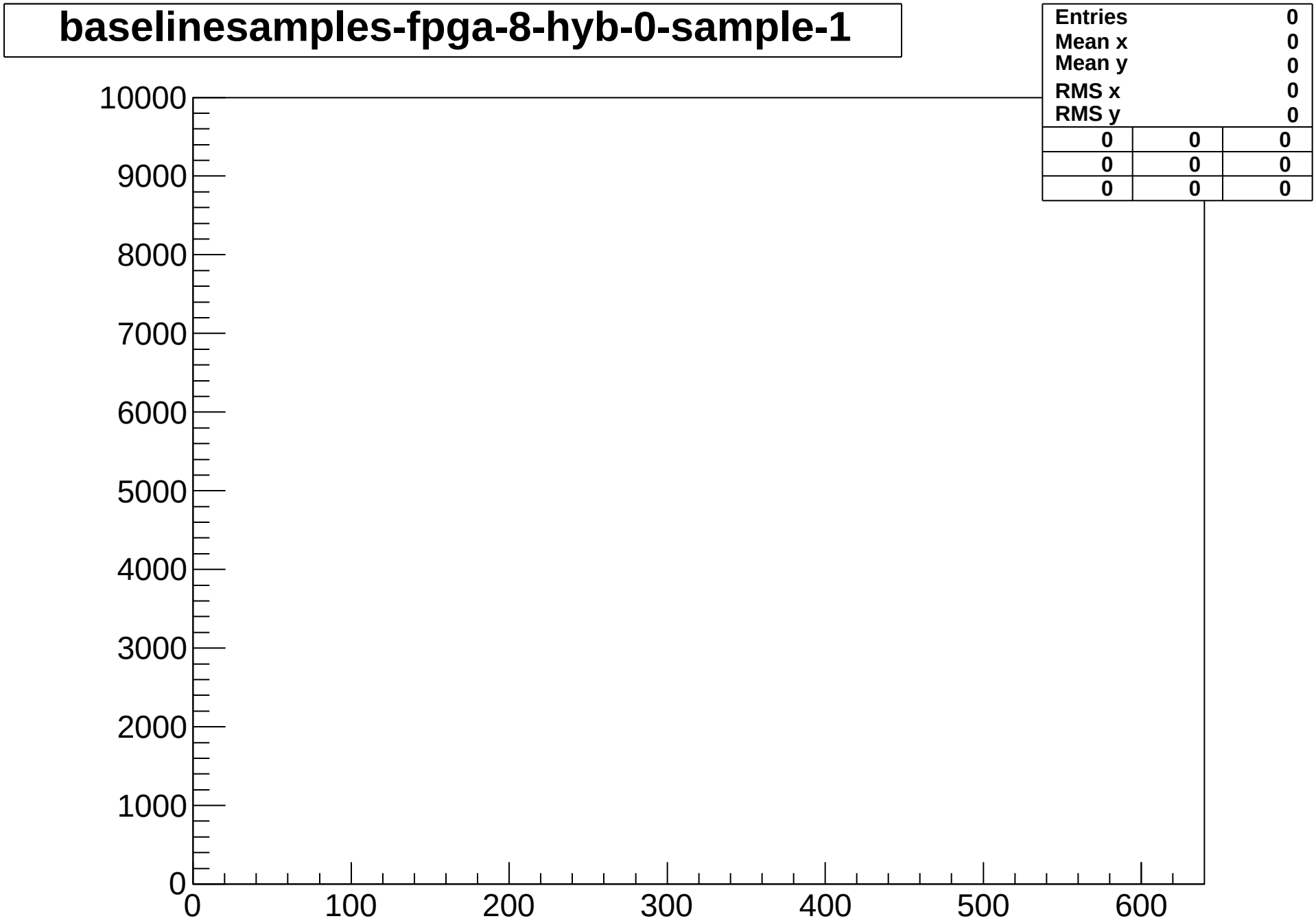
baselinesamples-fpga-7-hyb-3-sample-5



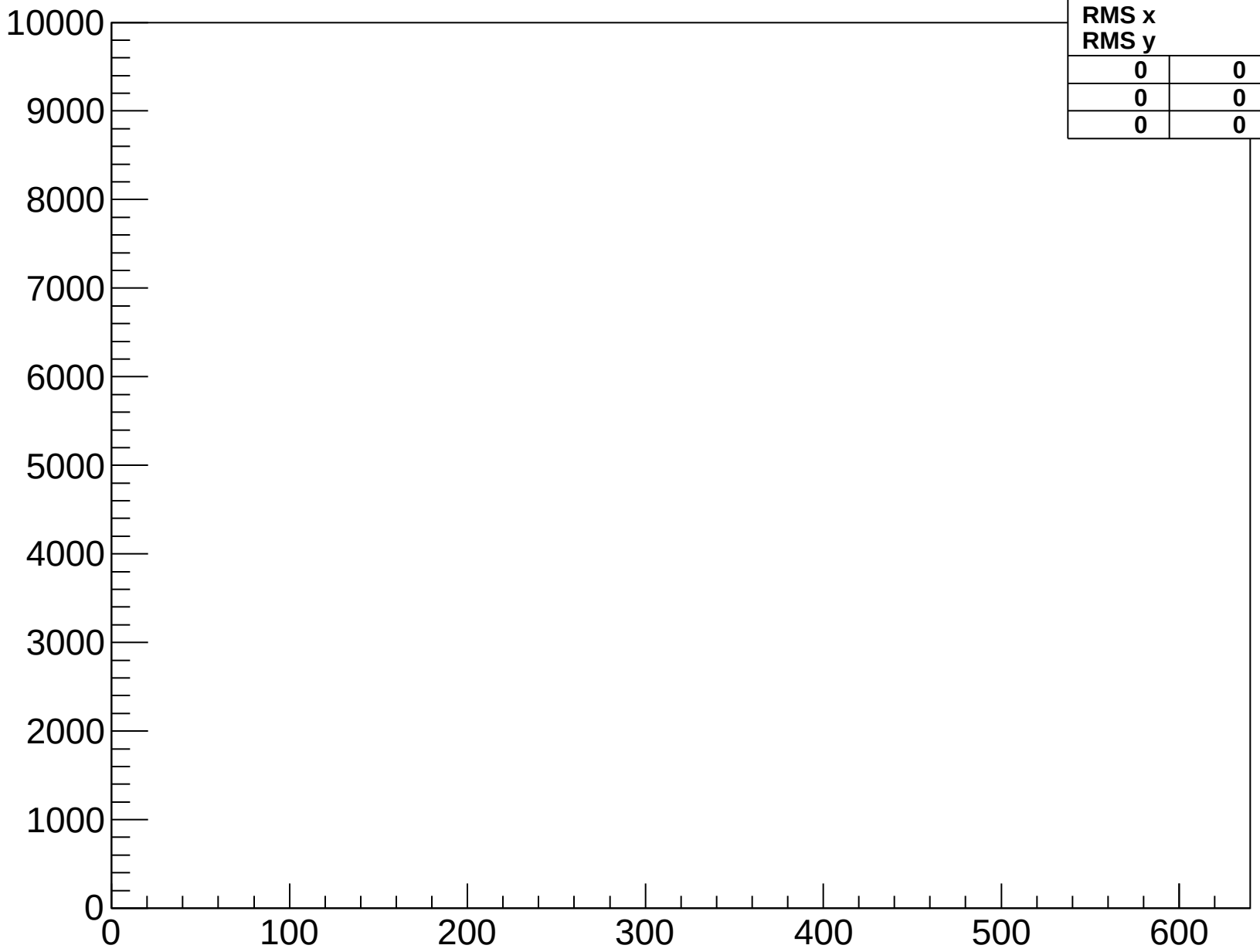
baselinesamples-fpga-8-hyb-0-sample-0



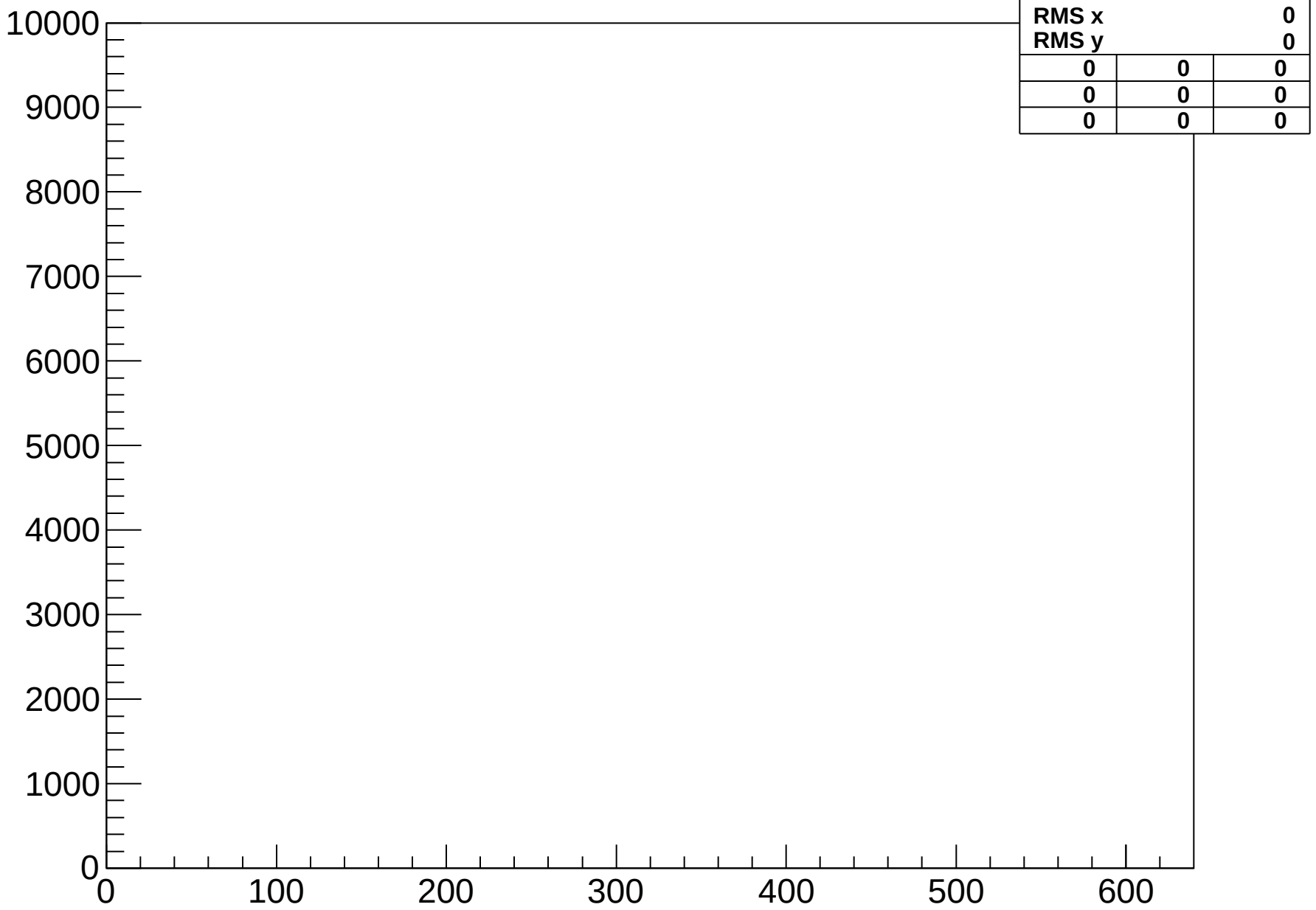
baselinesamples-fpga-8-hyb-0-sample-1



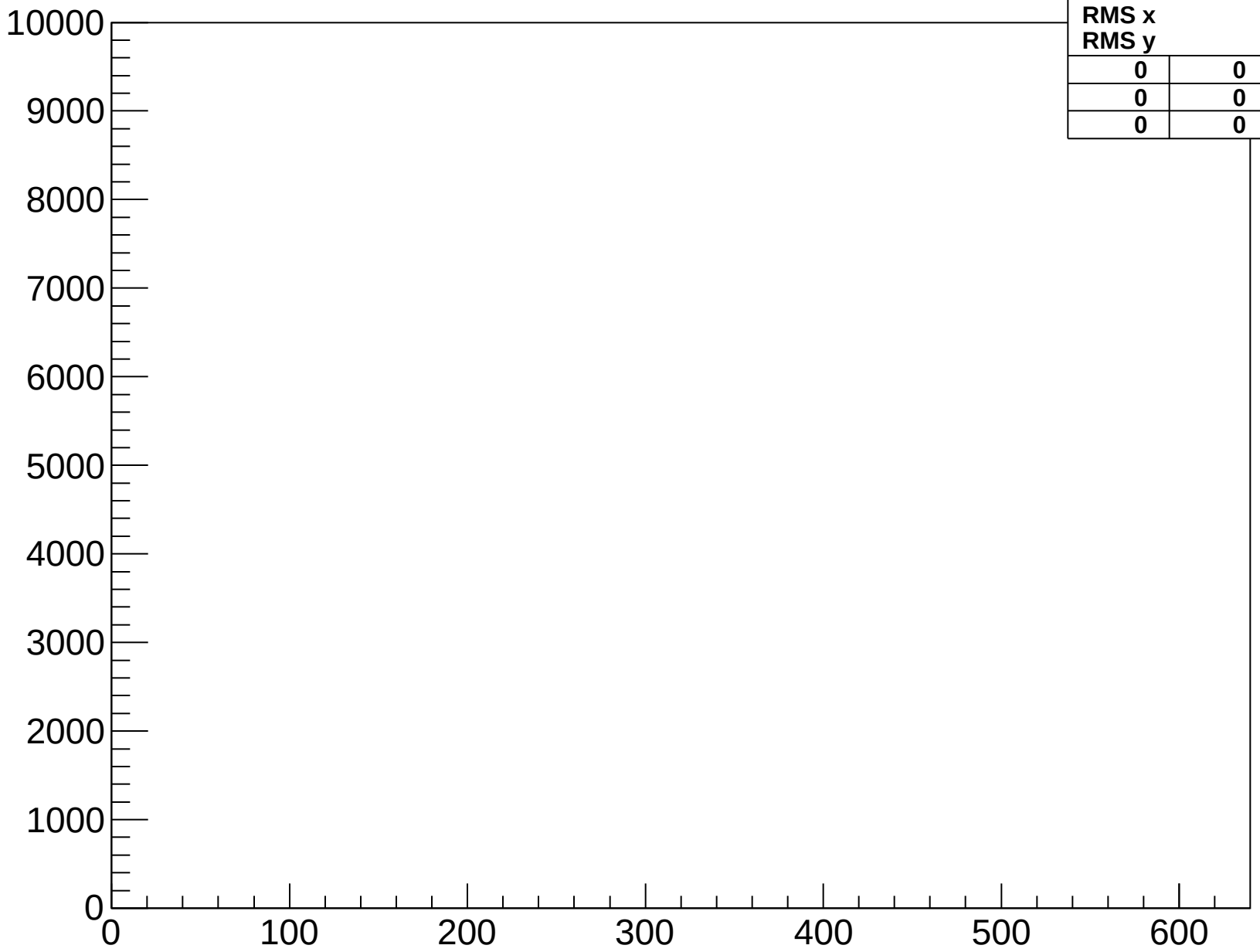
baselinesamples-fpga-8-hyb-0-sample-2



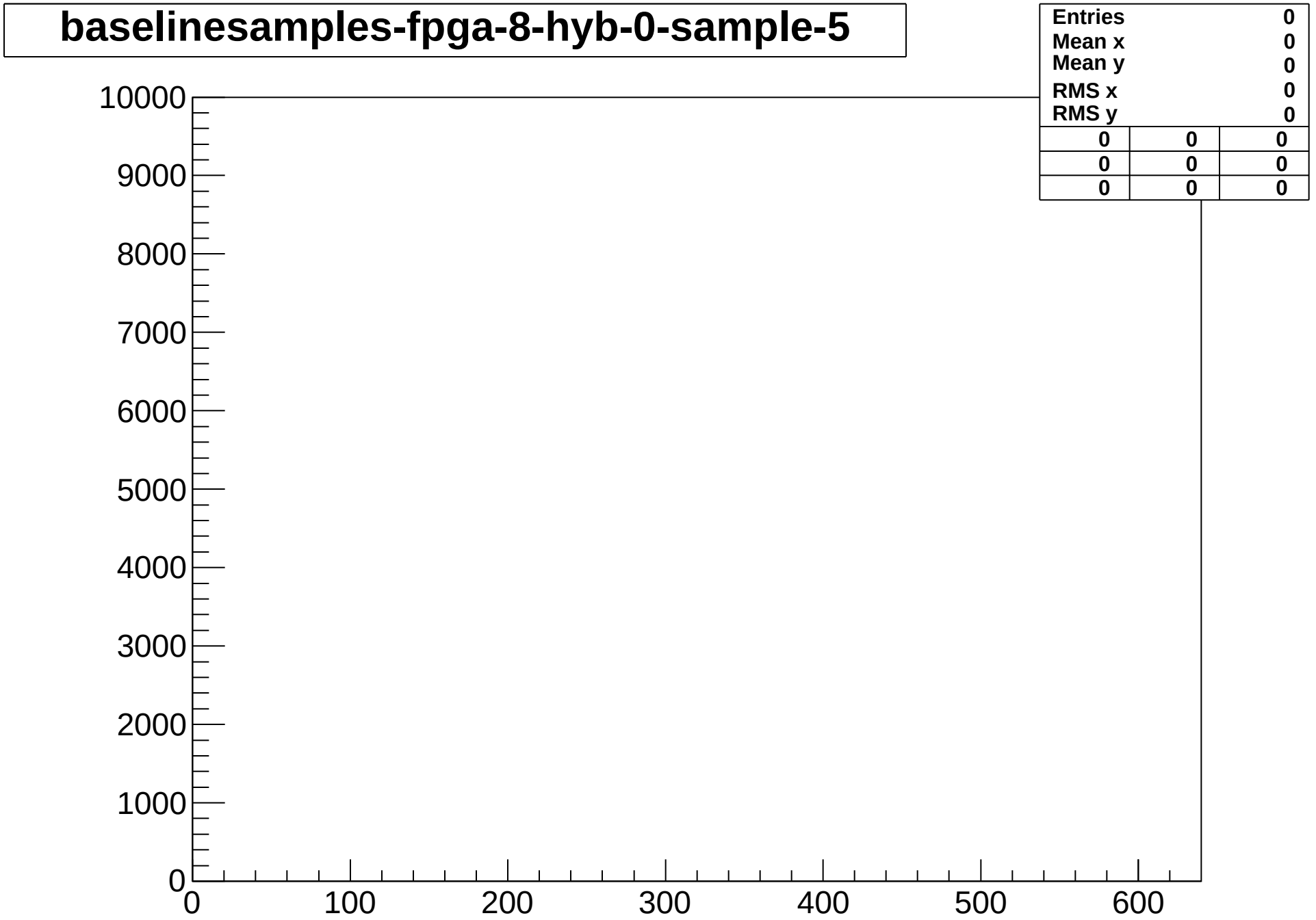
baselinesamples-fpga-8-hyb-0-sample-3



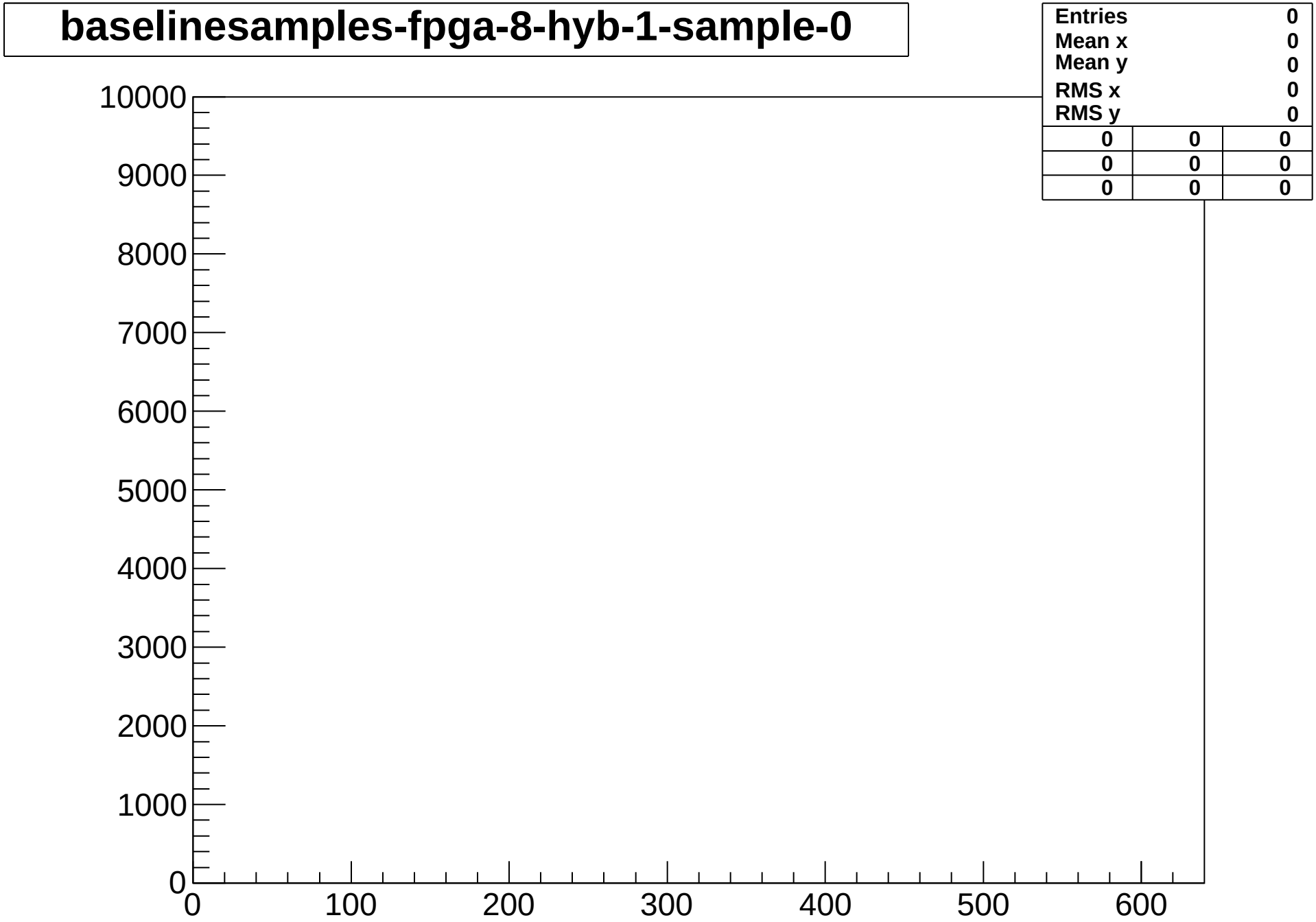
baselinesamples-fpga-8-hyb-0-sample-4



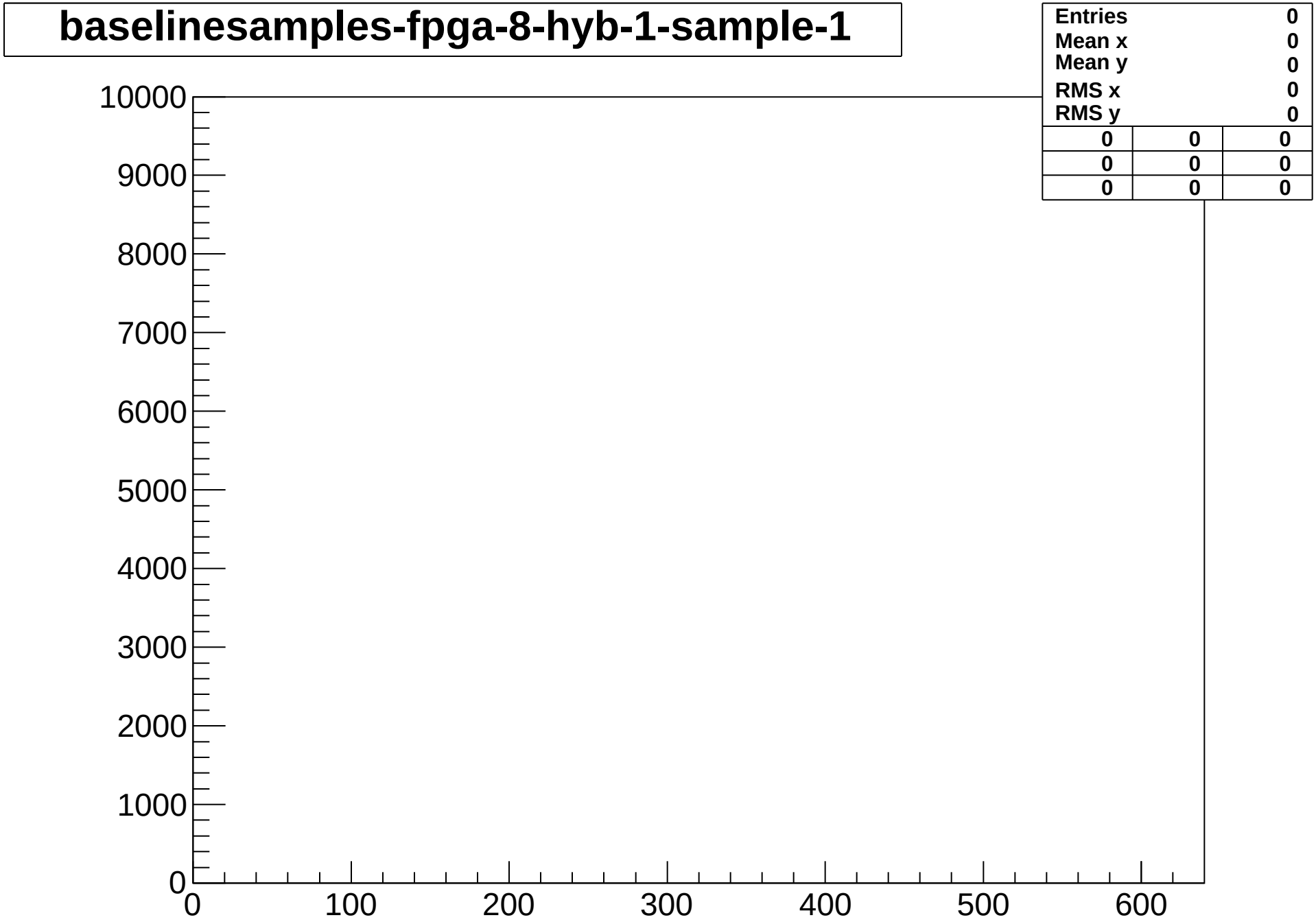
baselinesamples-fpga-8-hyb-0-sample-5



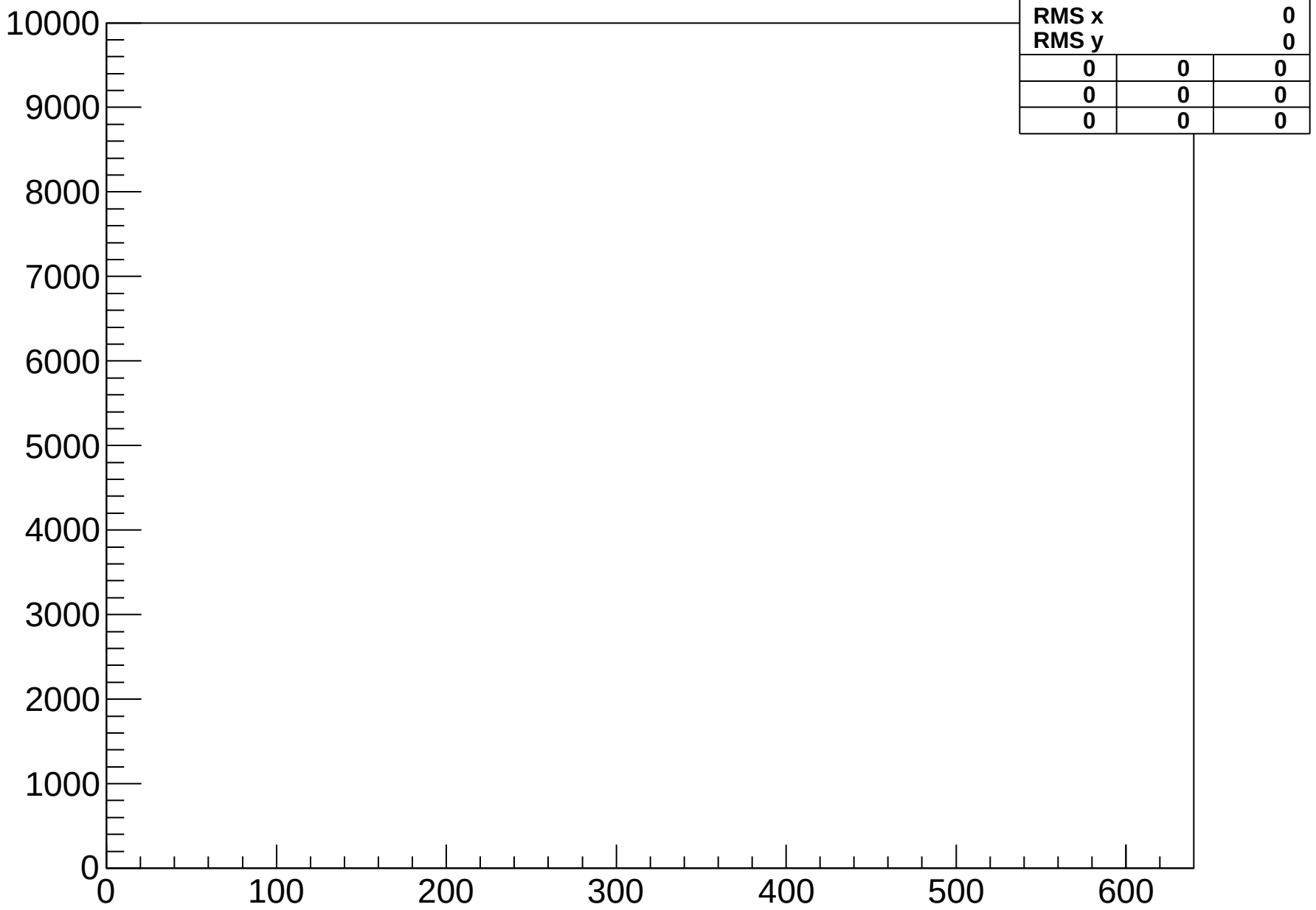
baselinesamples-fpga-8-hyb-1-sample-0



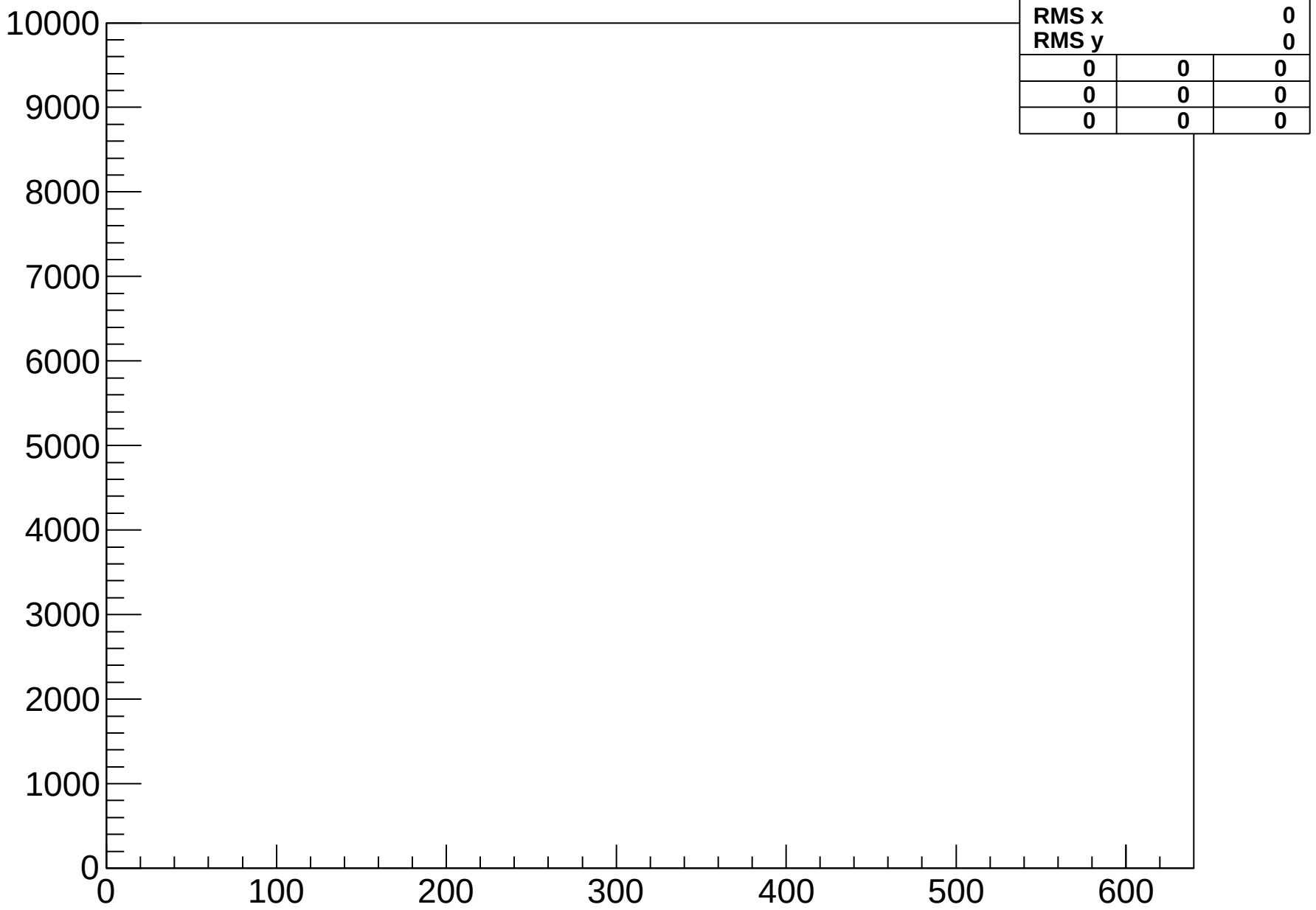
baselinesamples-fpga-8-hyb-1-sample-1



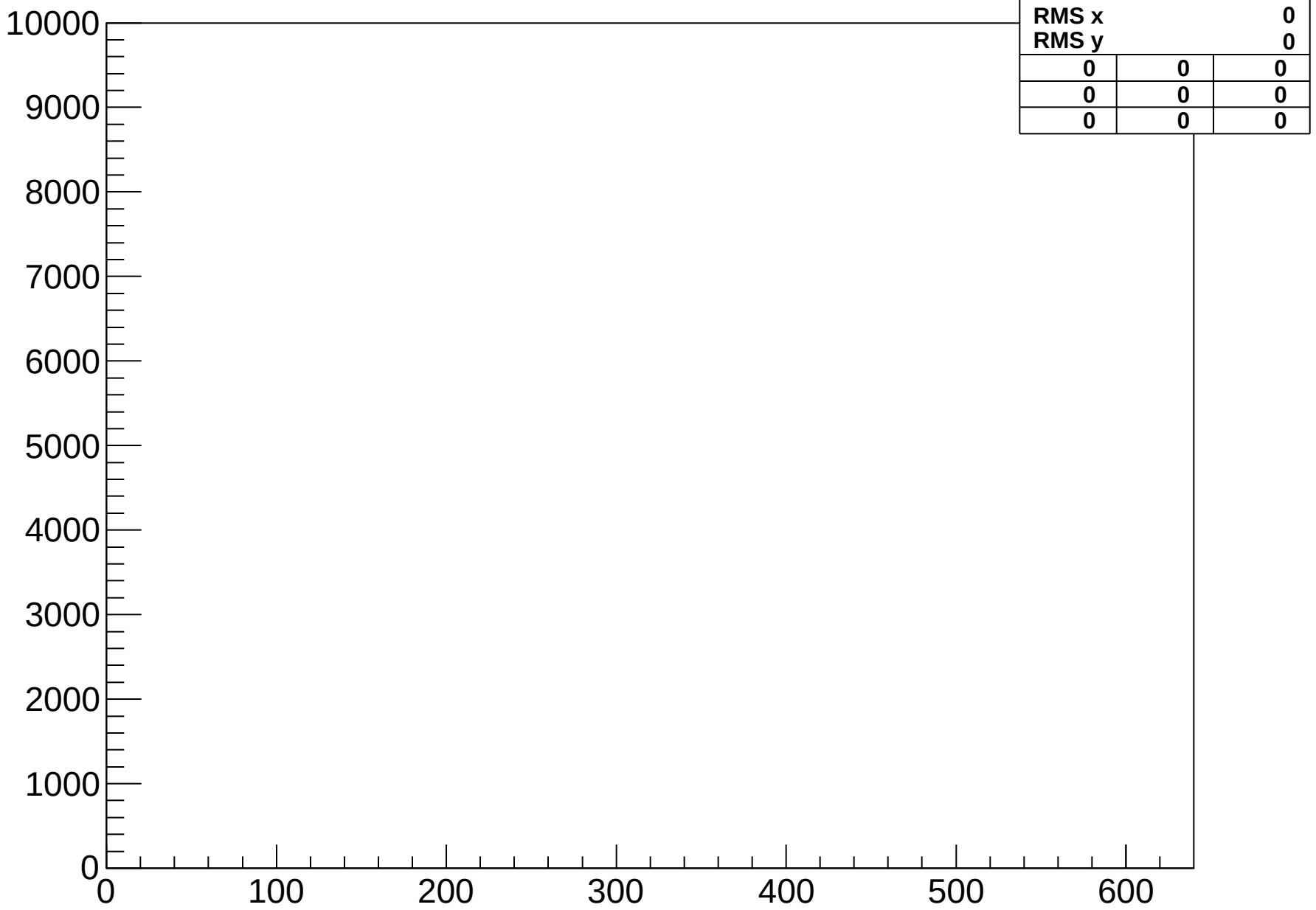
baselinesamples-fpga-8-hyb-1-sample-2



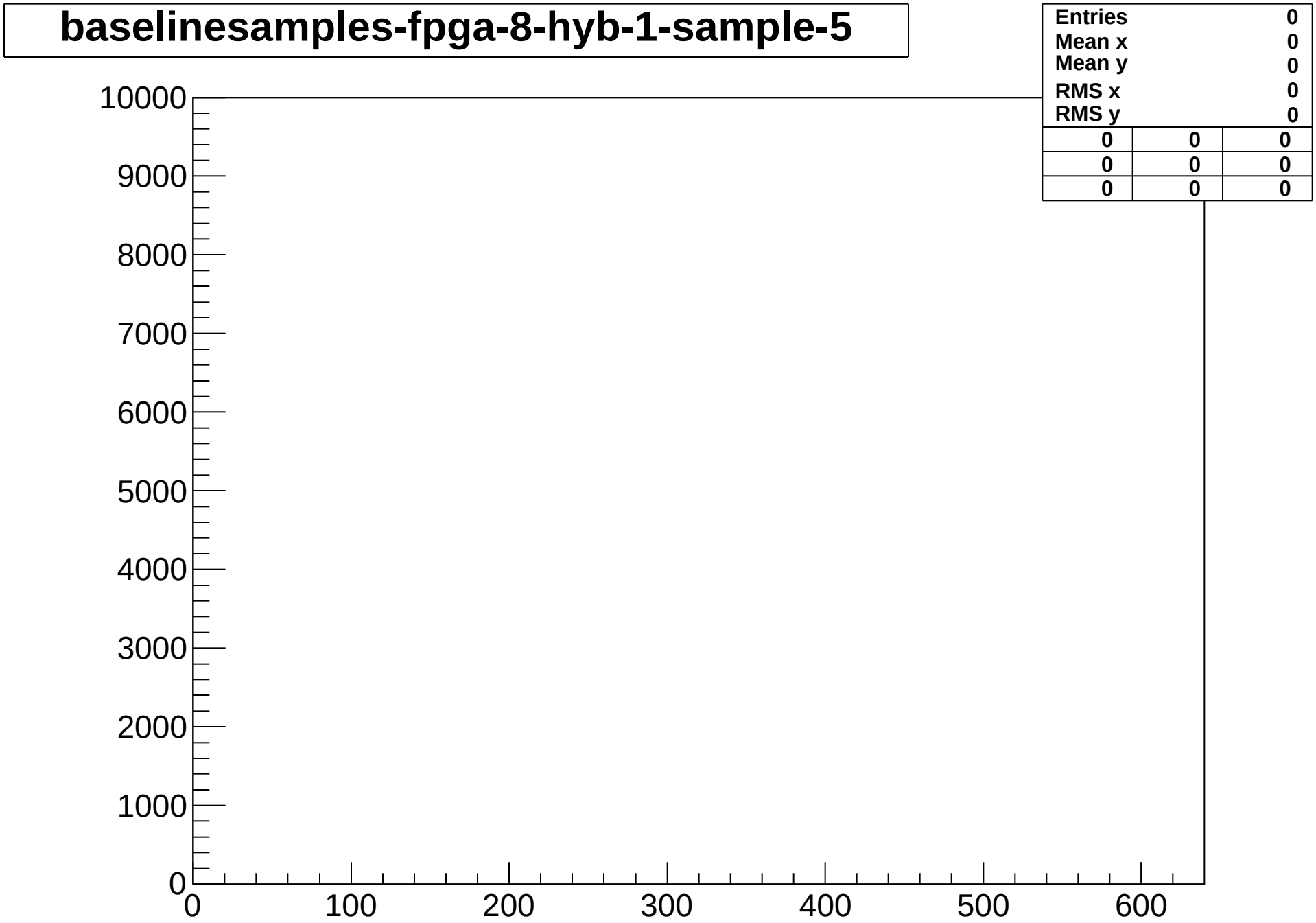
baselinesamples-fpga-8-hyb-1-sample-3



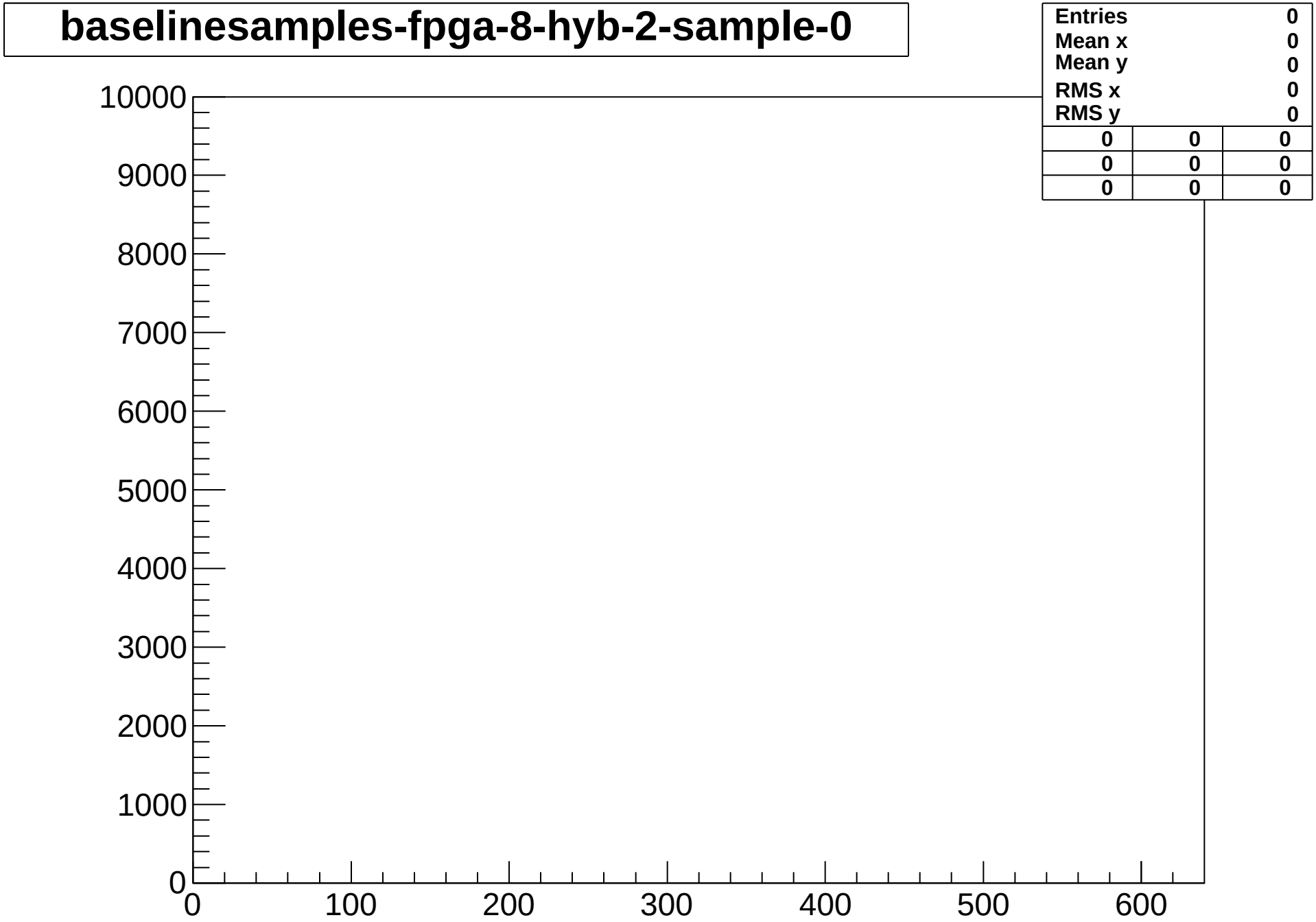
baselinesamples-fpga-8-hyb-1-sample-4



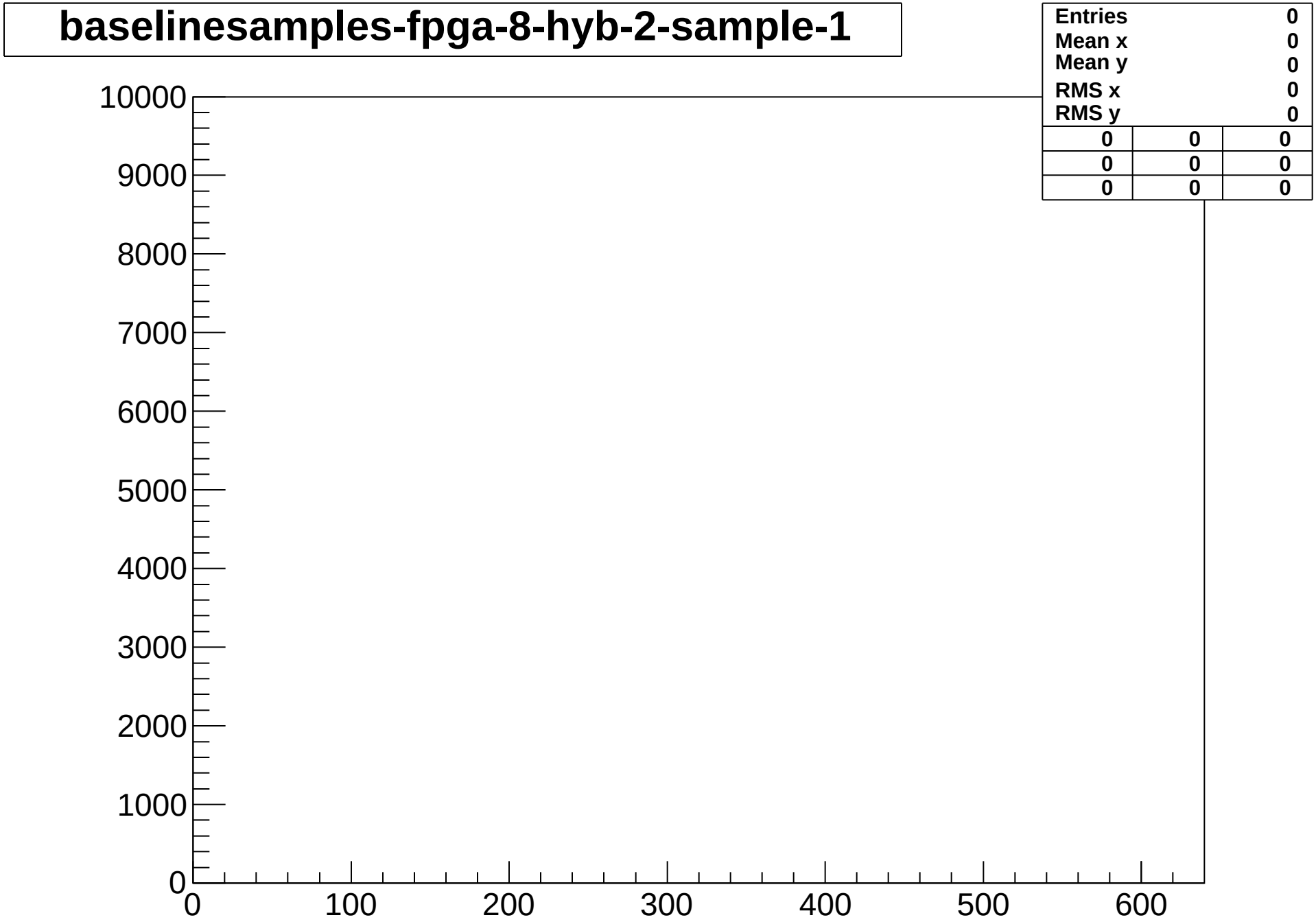
baselinesamples-fpga-8-hyb-1-sample-5



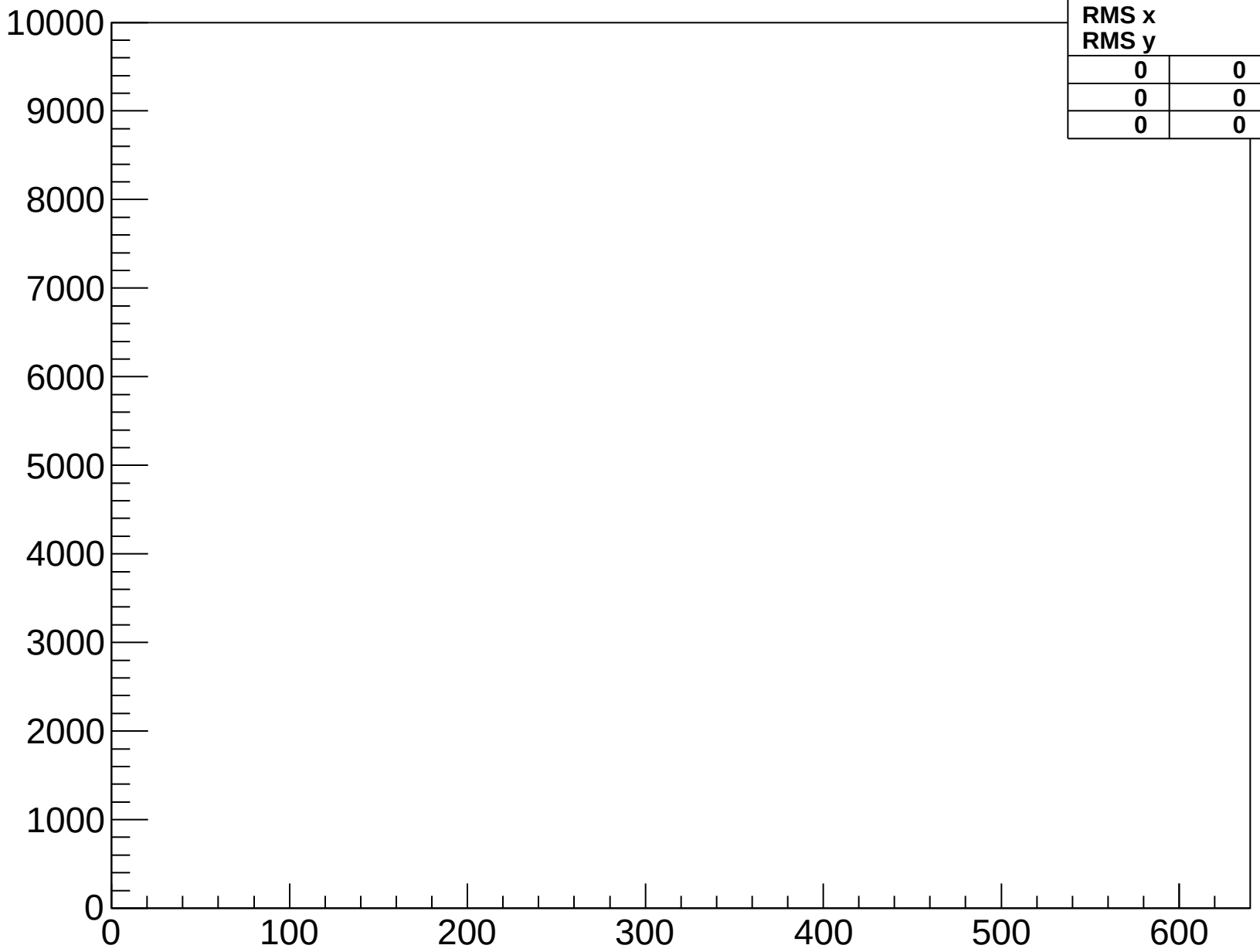
baselinesamples-fpga-8-hyb-2-sample-0



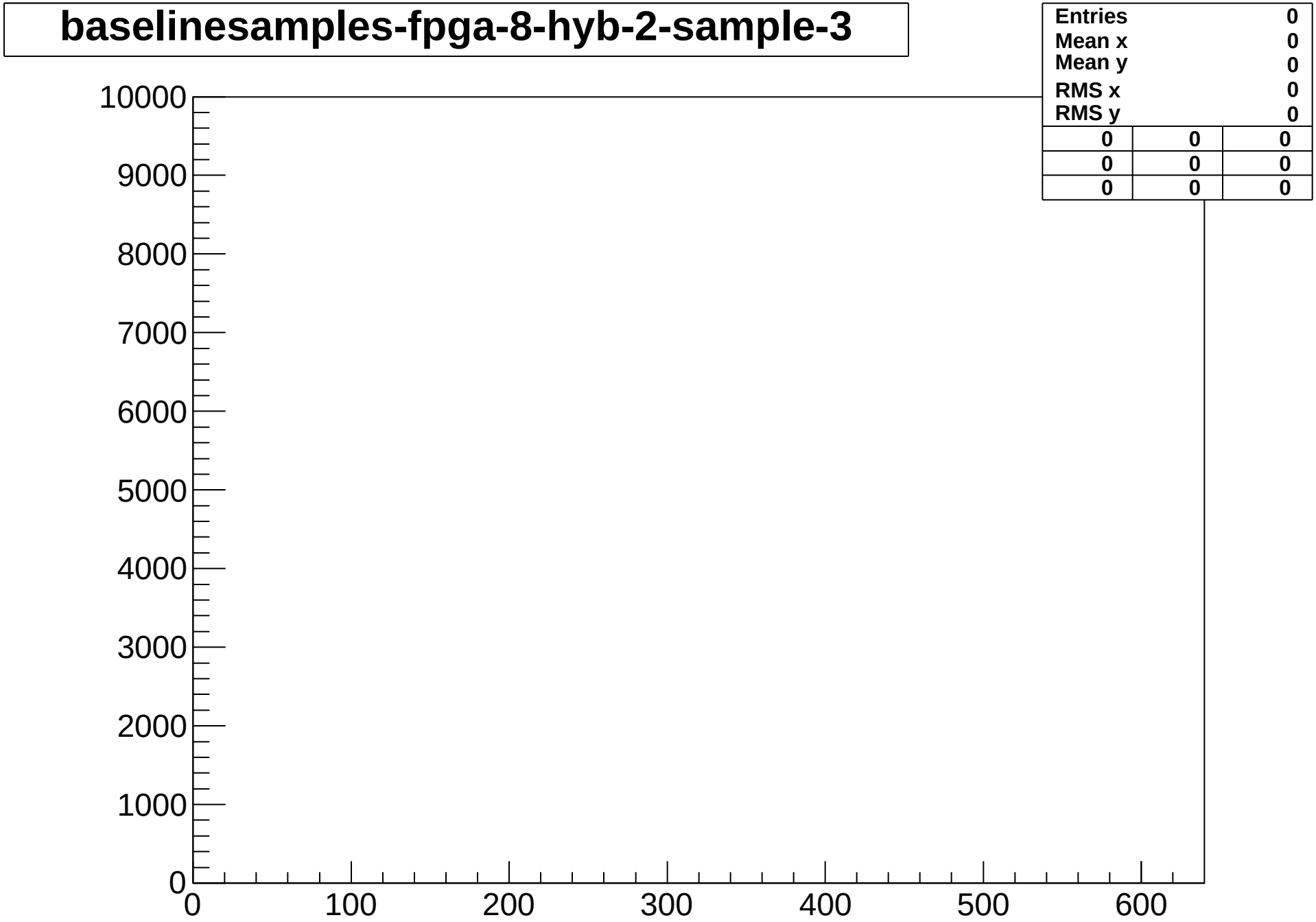
baselinesamples-fpga-8-hyb-2-sample-1



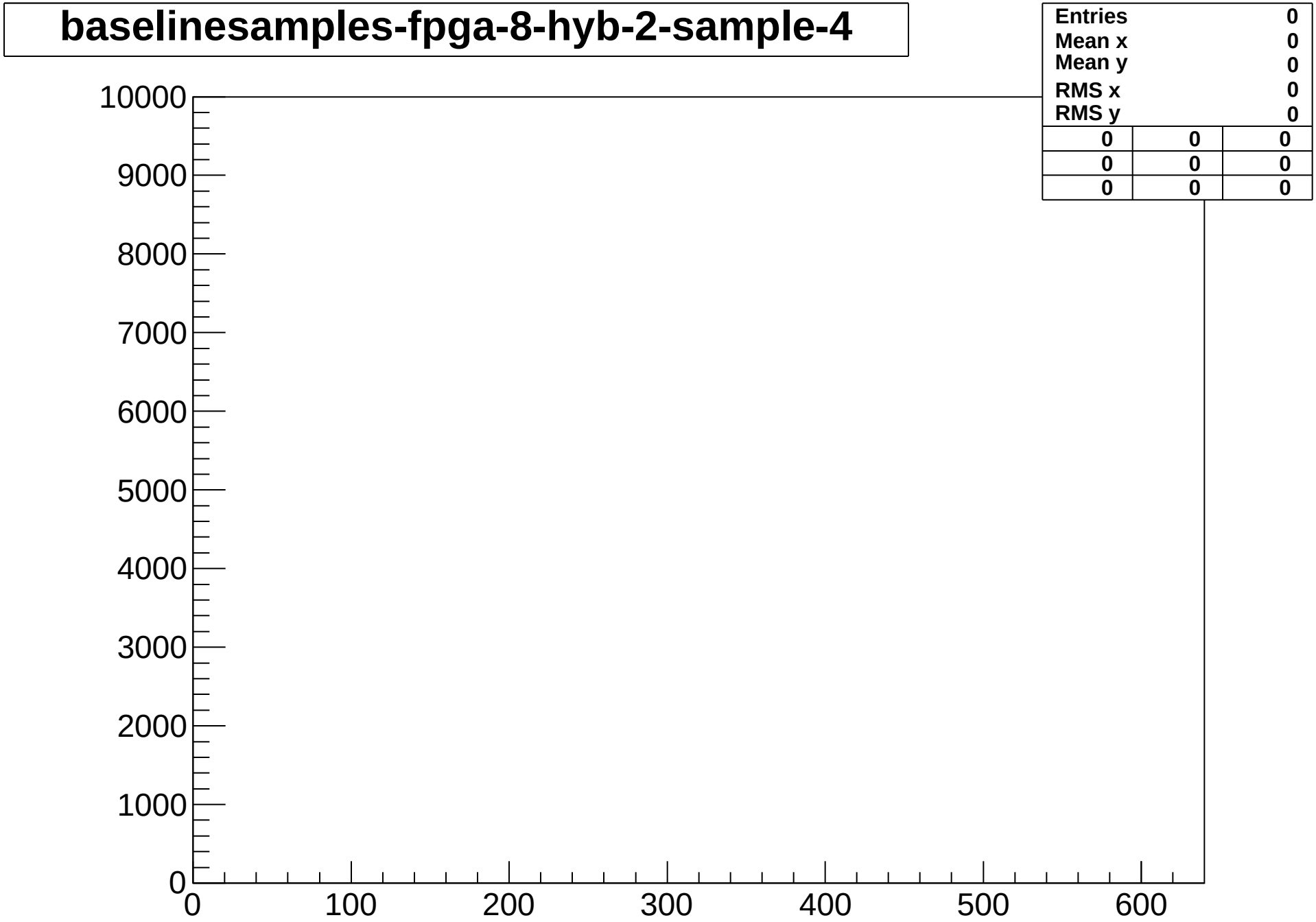
baselinesamples-fpga-8-hyb-2-sample-2



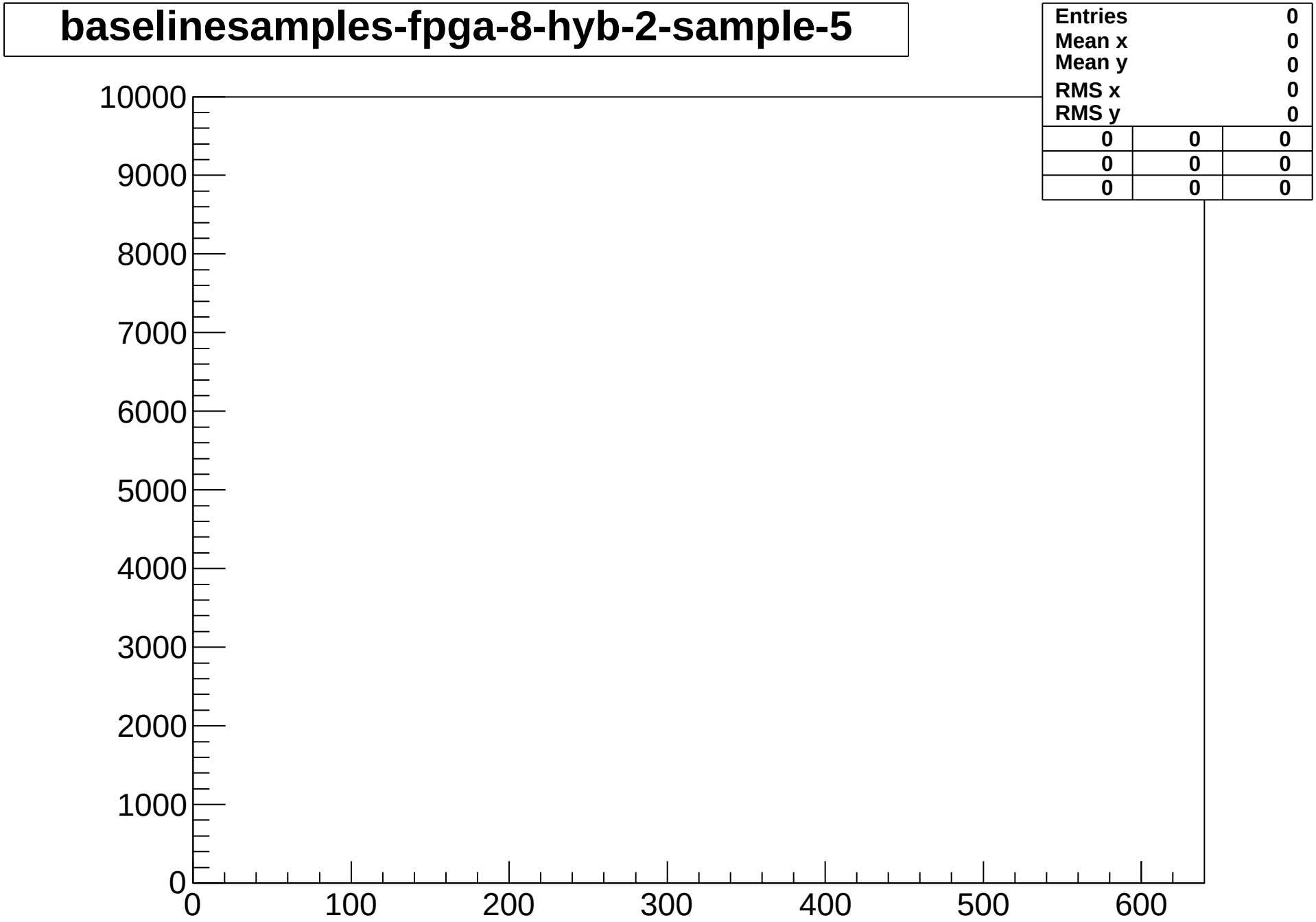
baselinesamples-fpga-8-hyb-2-sample-3

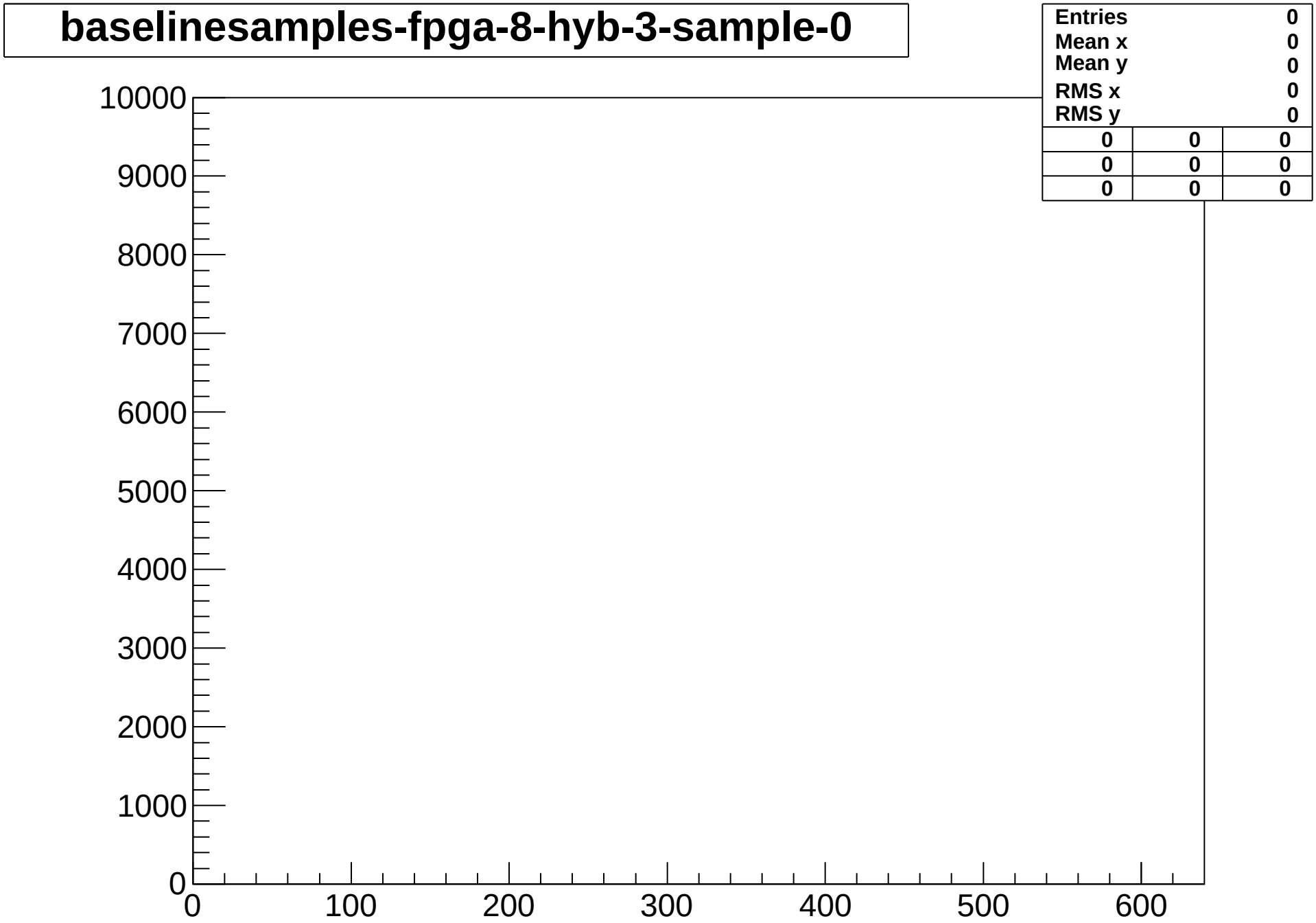


baselinesamples-fpga-8-hyb-2-sample-4

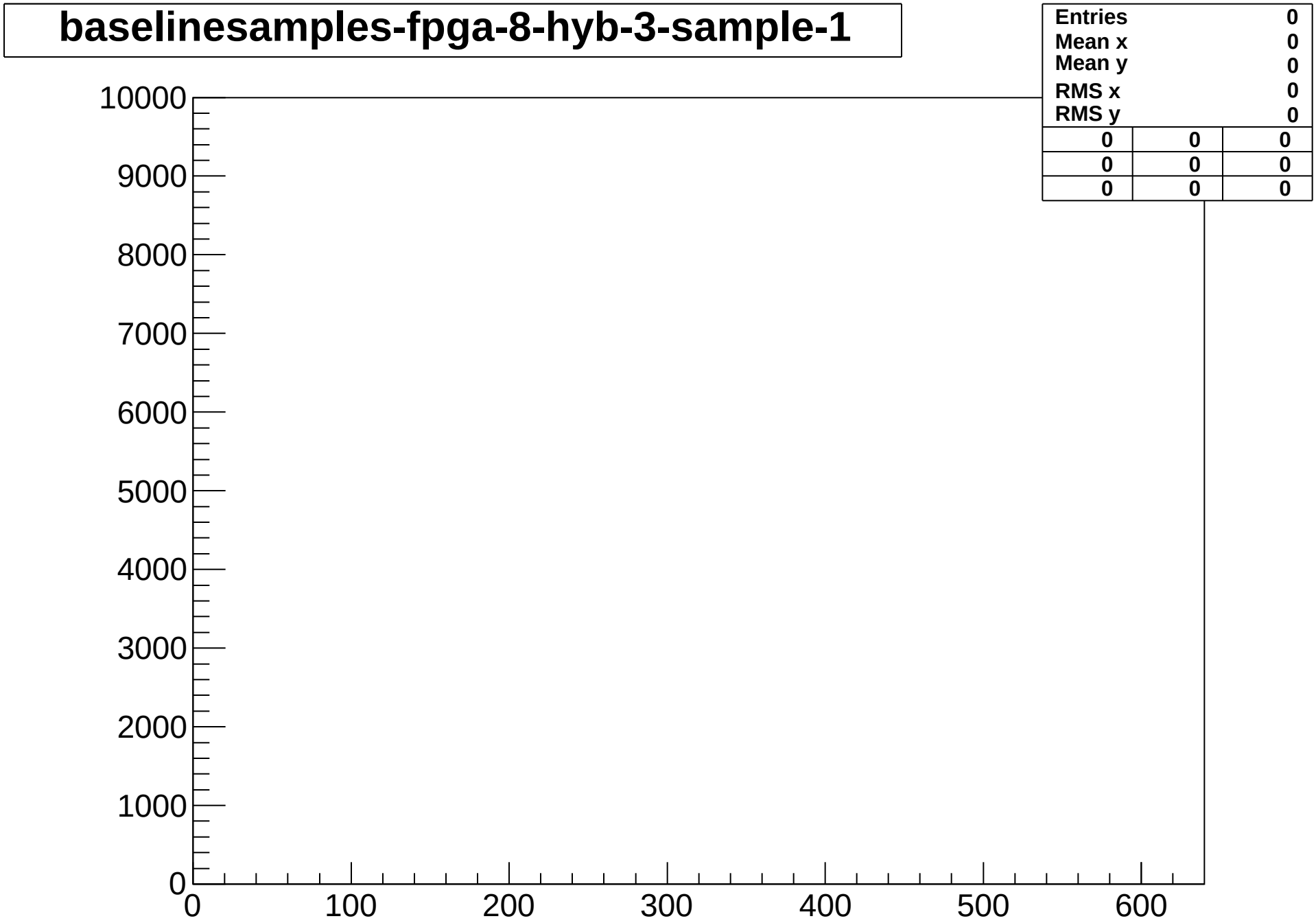


baselinesamples-fpga-8-hyb-2-sample-5

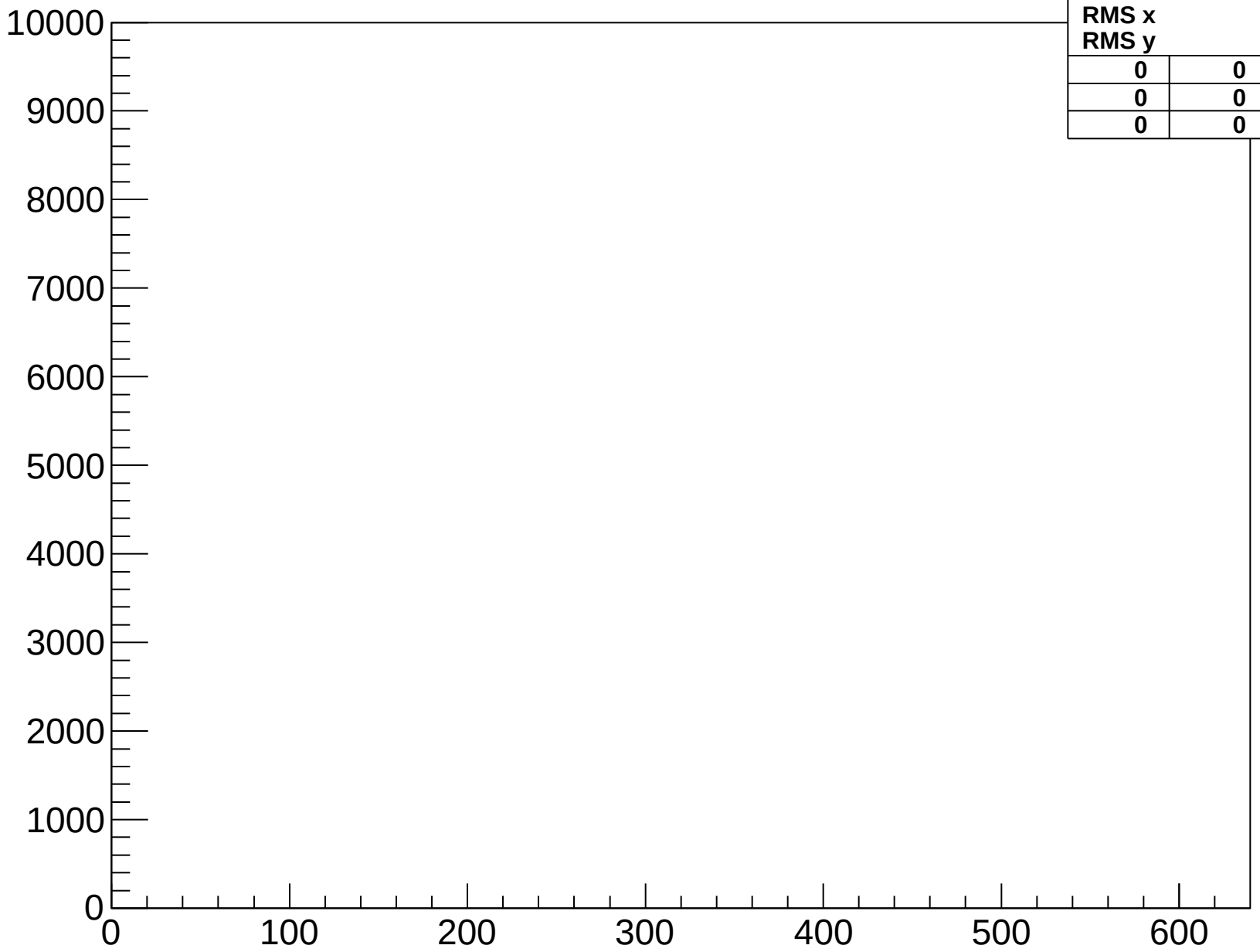



baselinesamples-fpga-8-hyb-3-sample-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

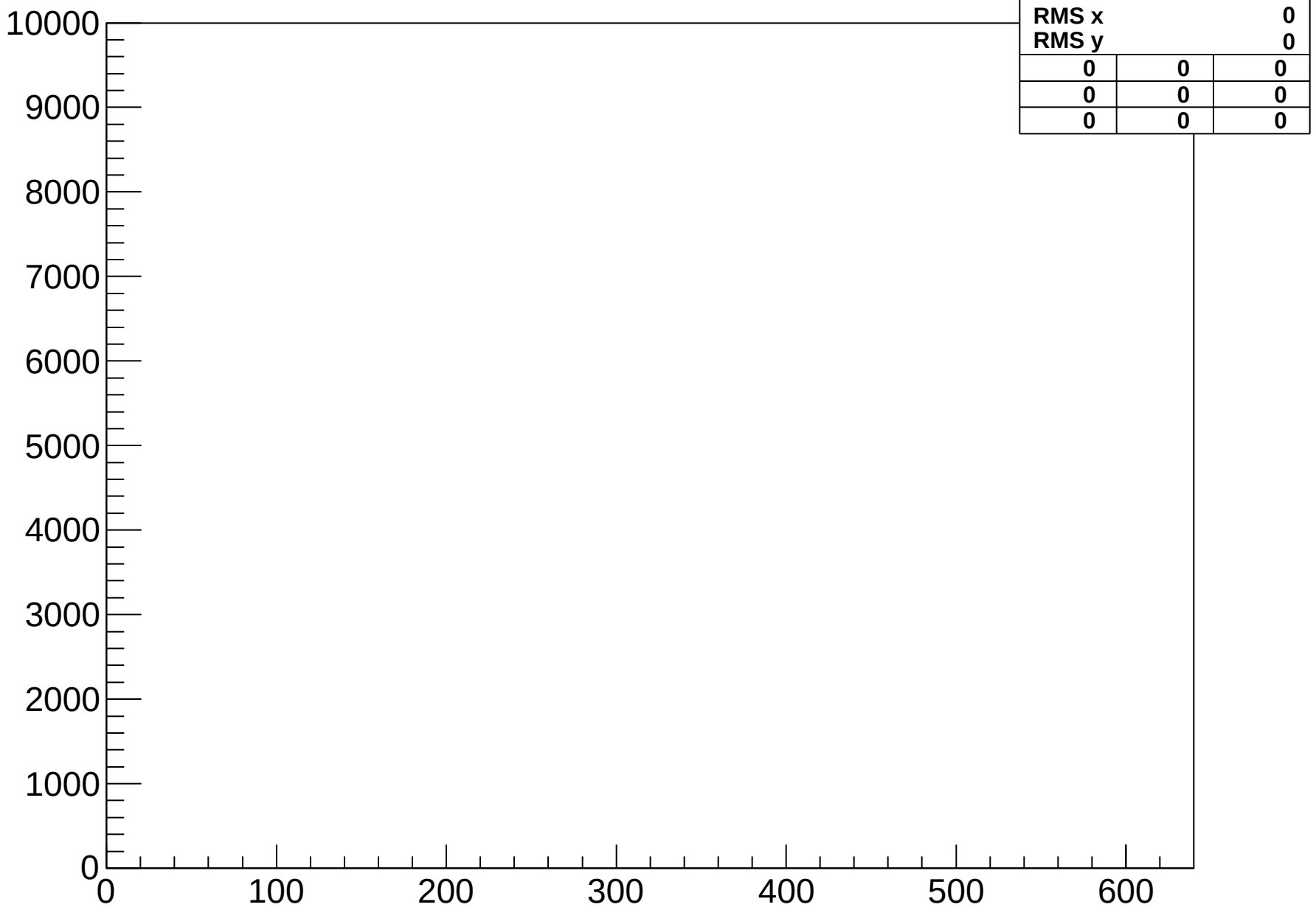
baselinesamples-fpga-8-hyb-3-sample-1



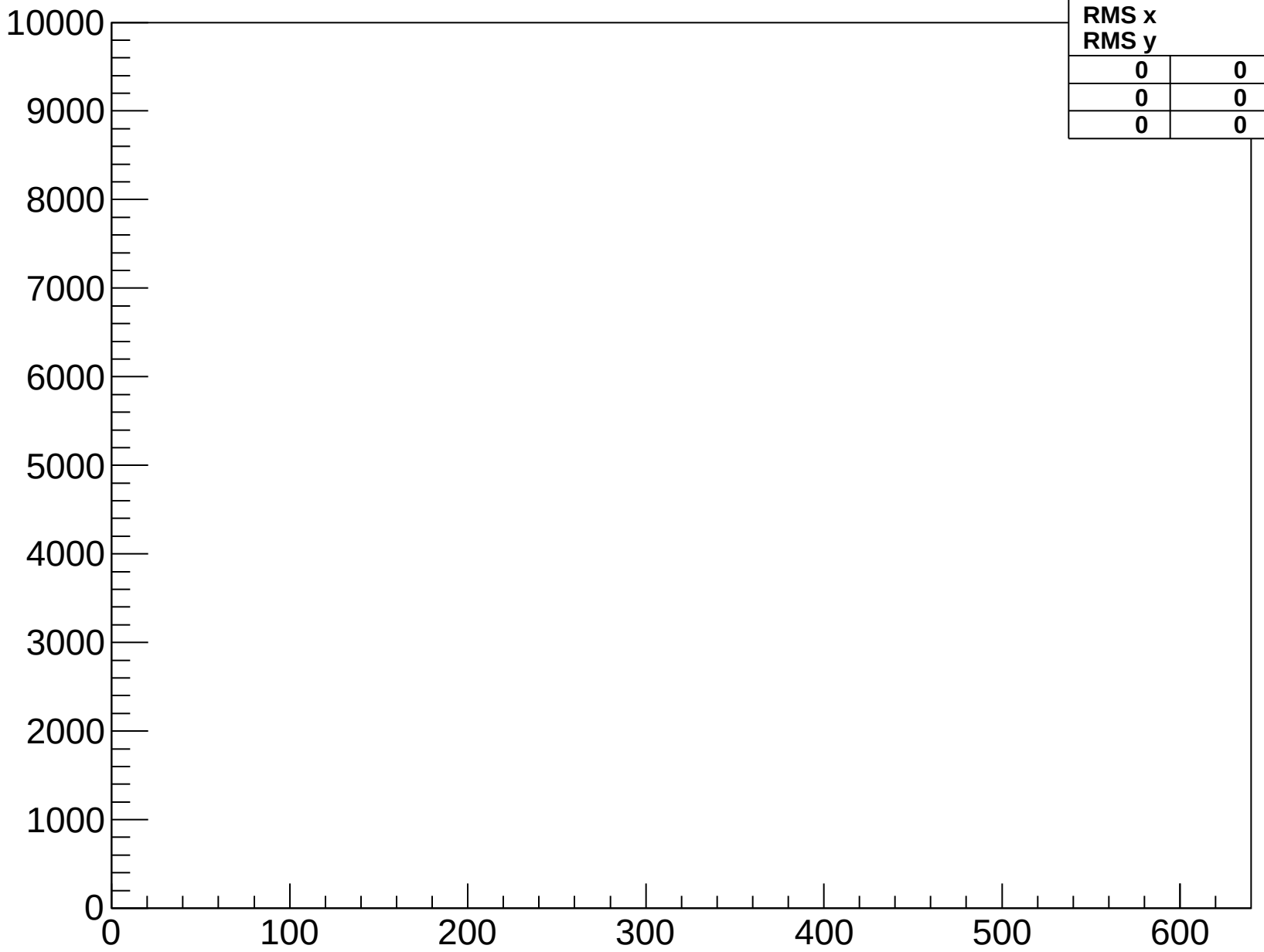
baselinesamples-fpga-8-hyb-3-sample-2



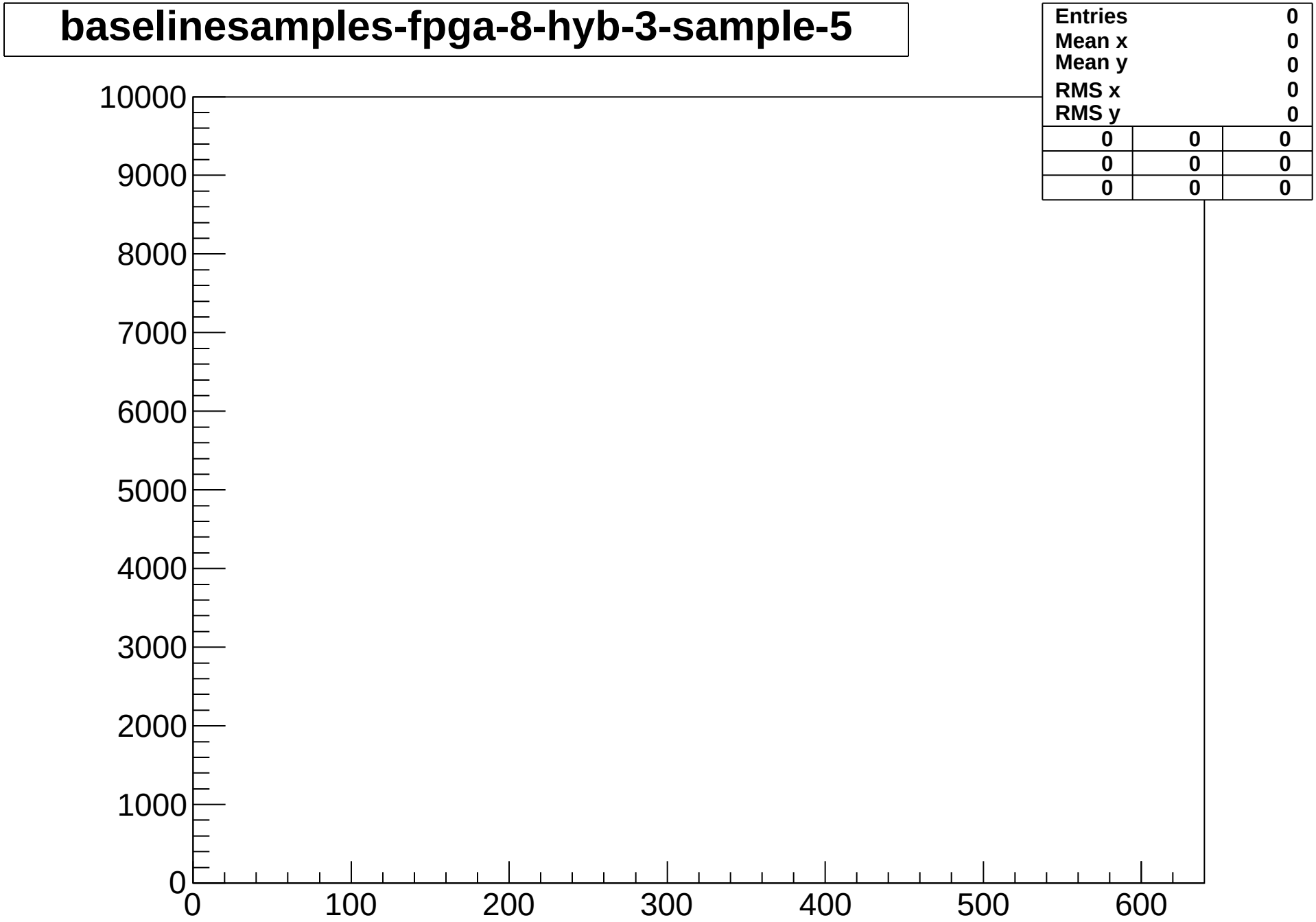
baselinesamples-fpga-8-hyb-3-sample-3



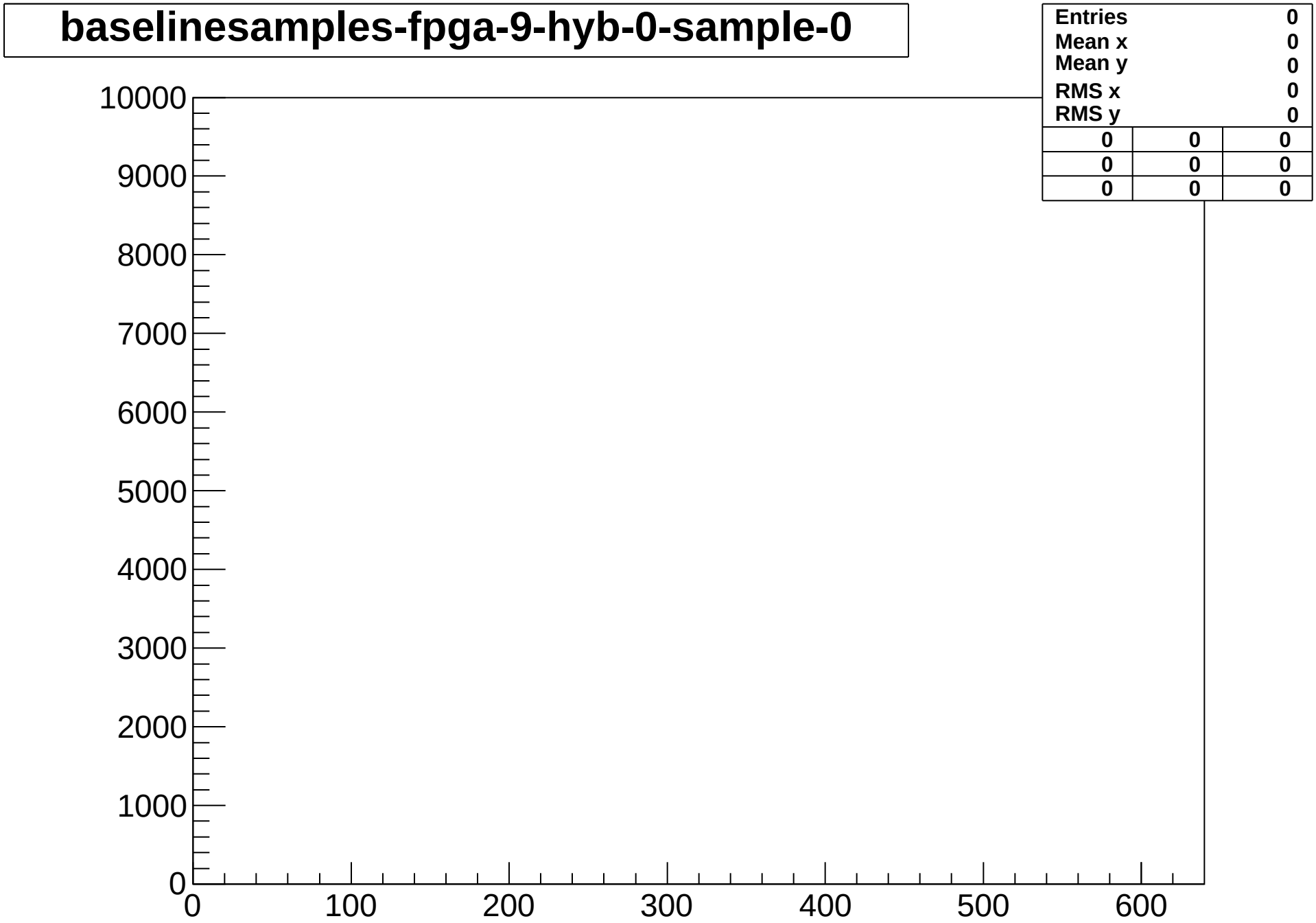
baselinesamples-fpga-8-hyb-3-sample-4



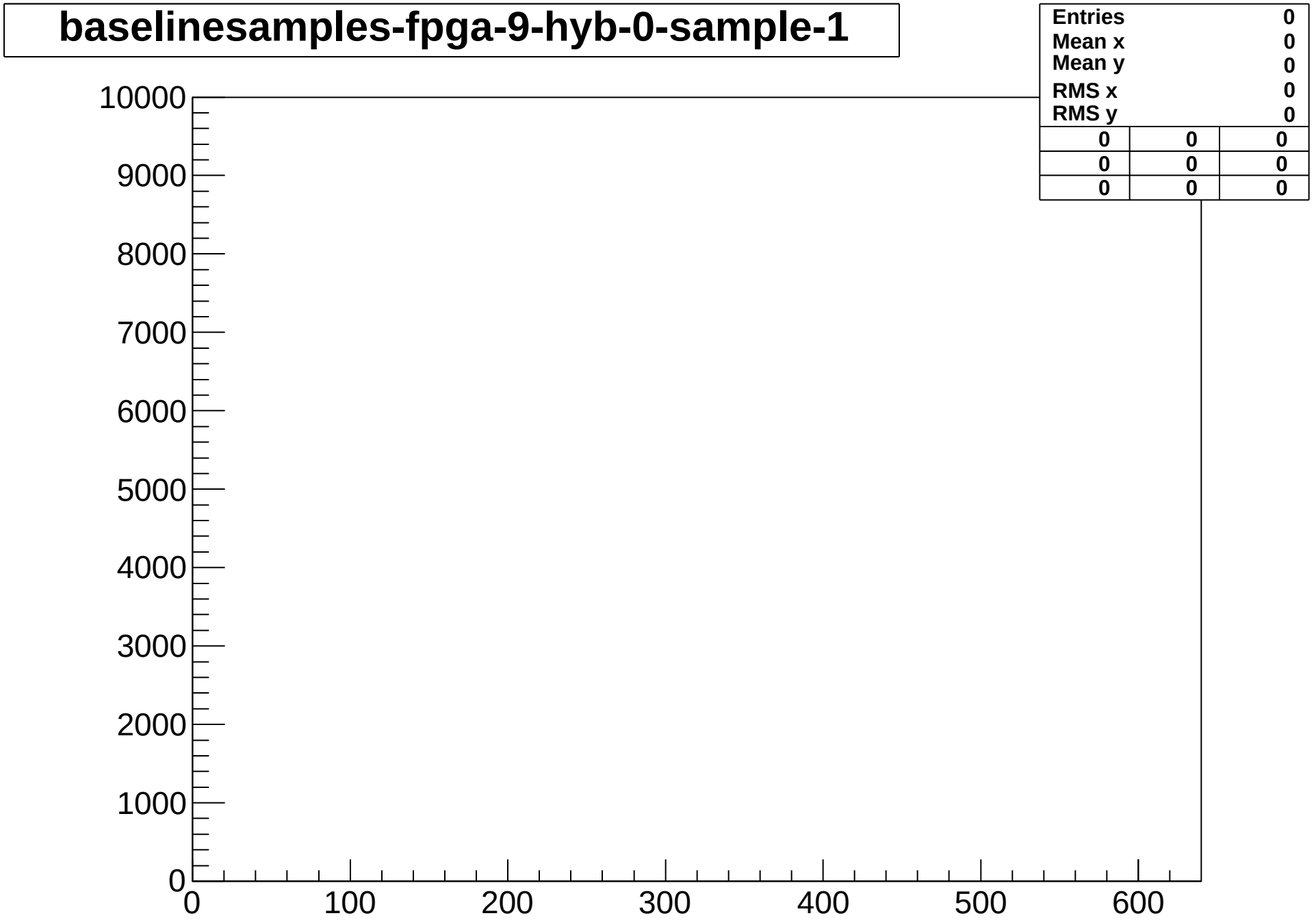
baselinesamples-fpga-8-hyb-3-sample-5



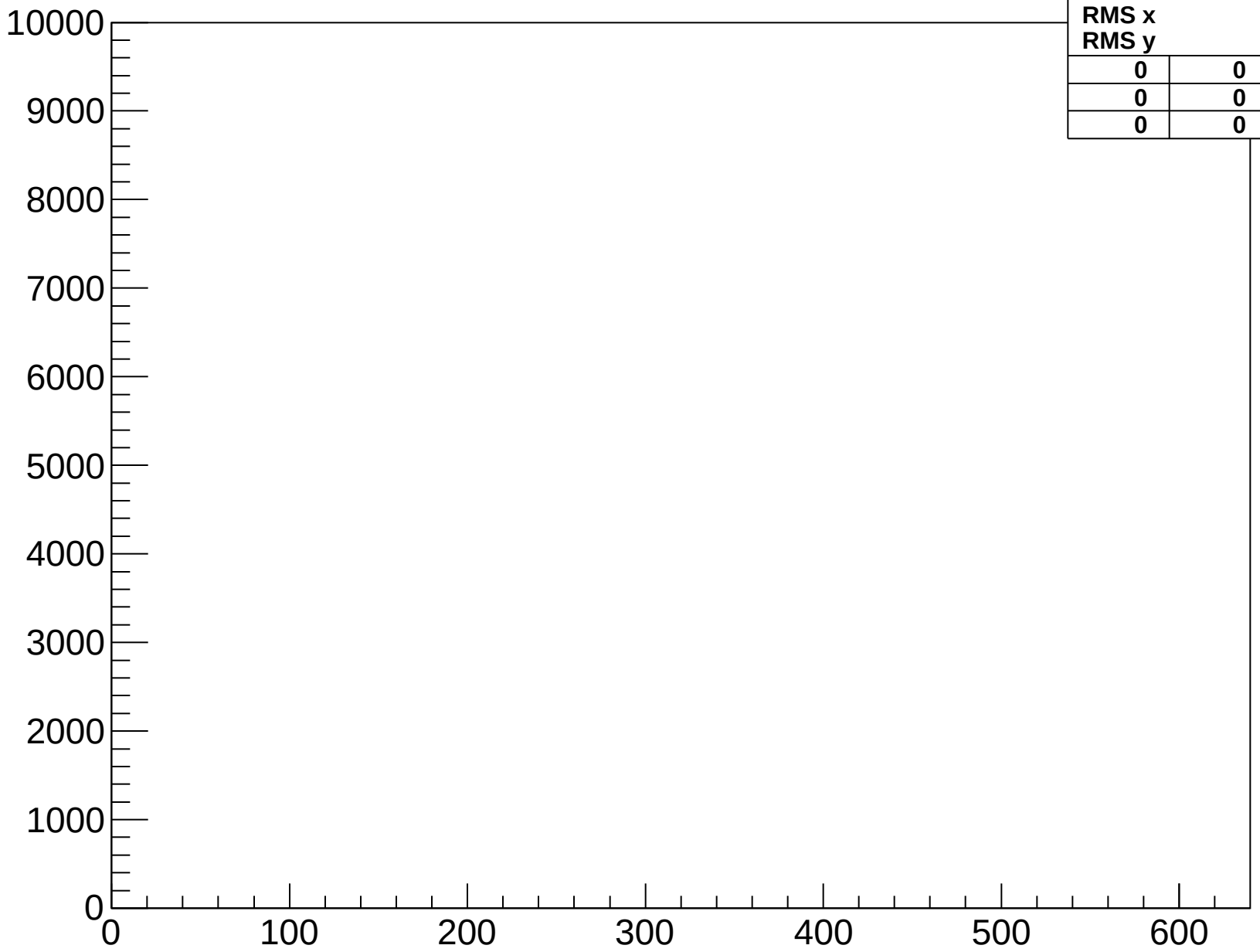
baselinesamples-fpga-9-hyb-0-sample-0



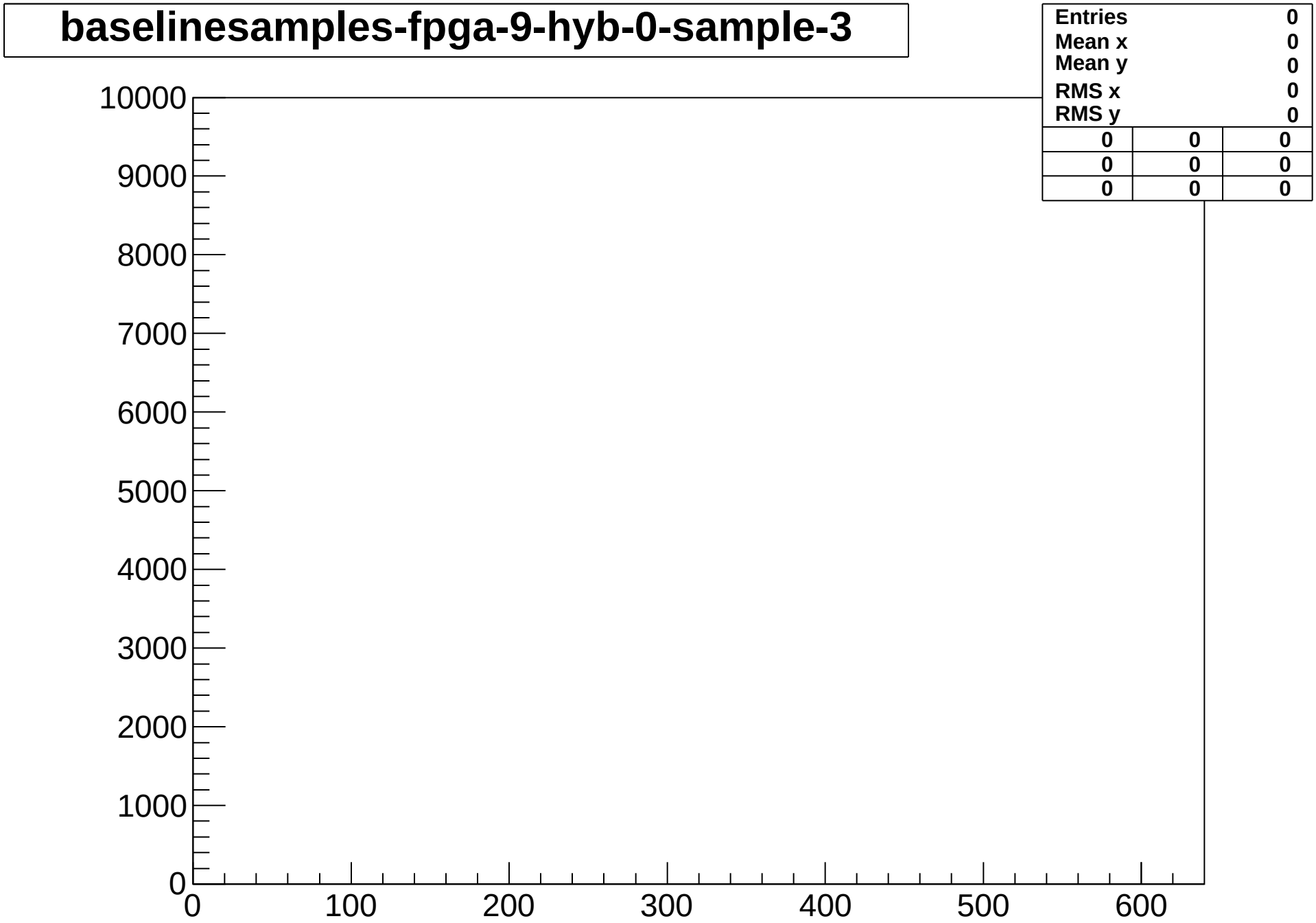
baselinesamples-fpga-9-hyb-0-sample-1



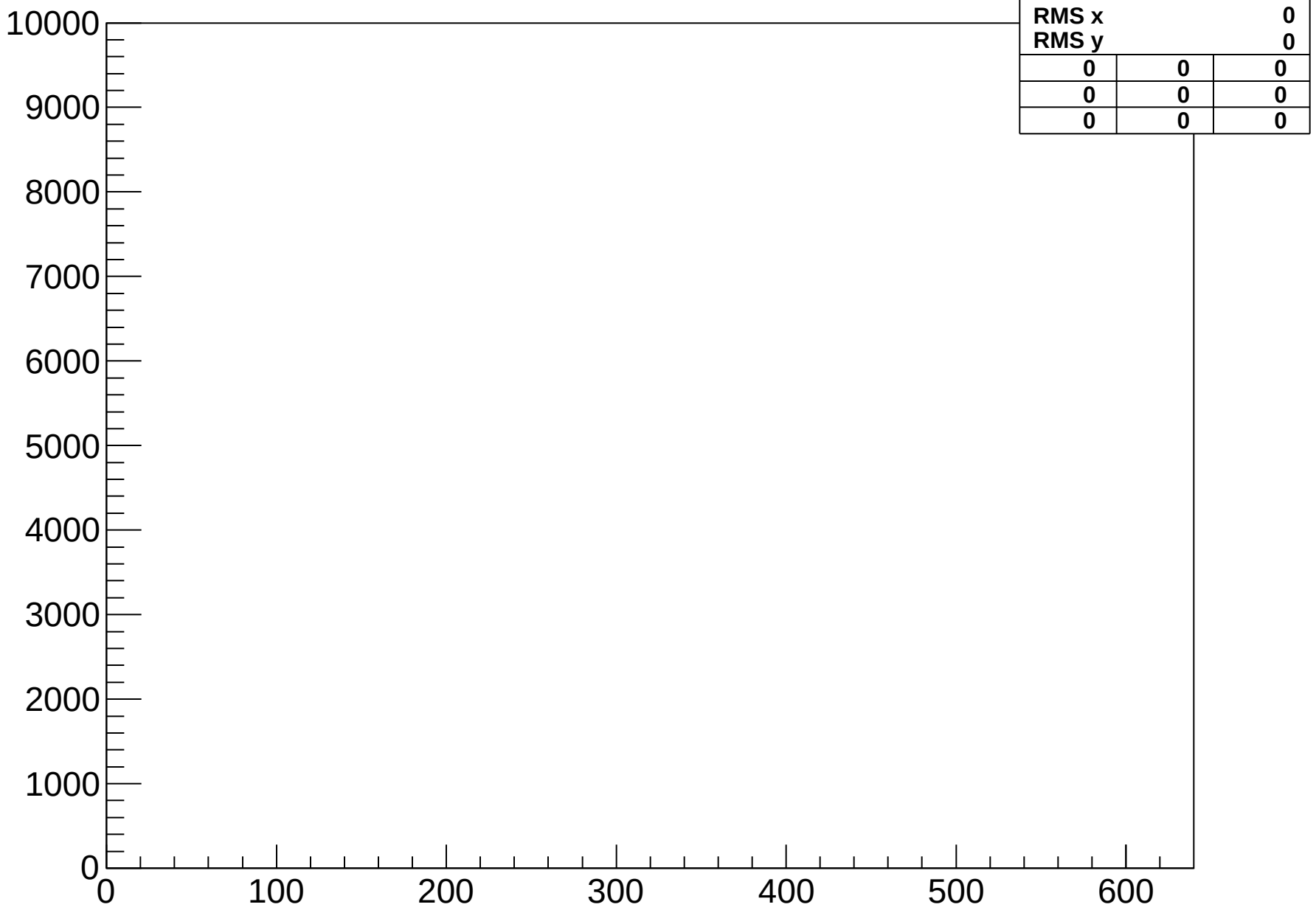
baselinesamples-fpga-9-hyb-0-sample-2



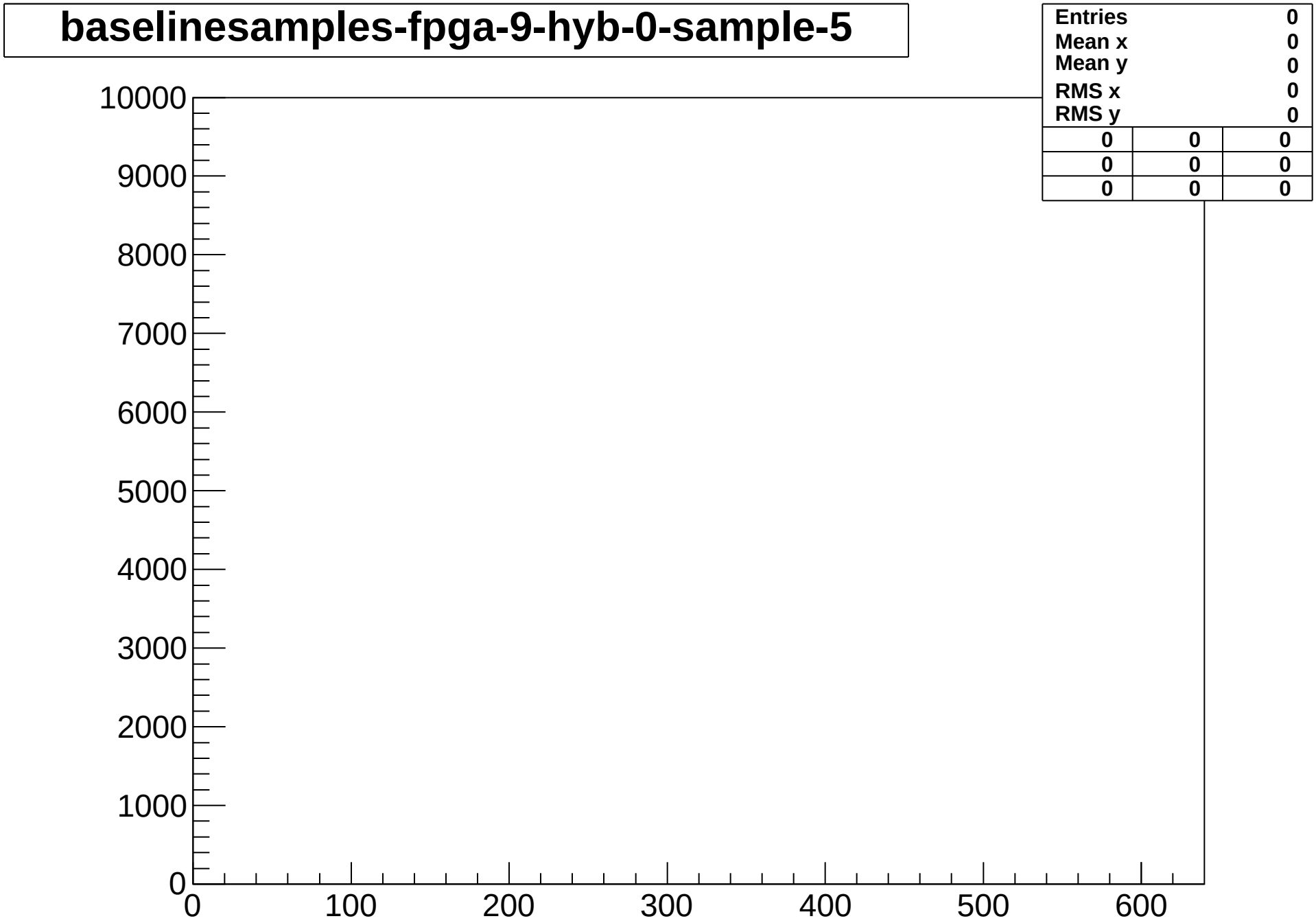
baselinesamples-fpga-9-hyb-0-sample-3

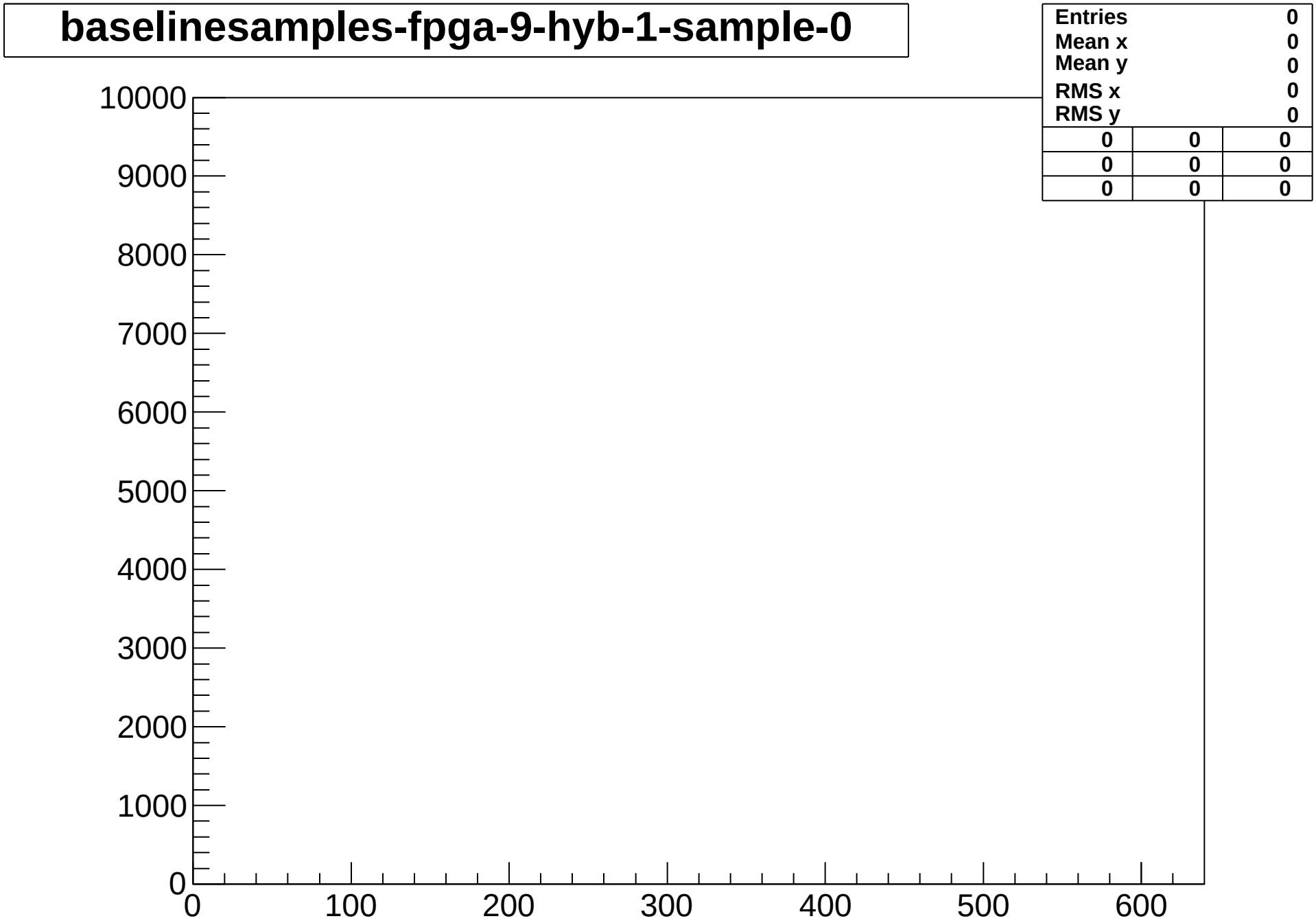


baselinesamples-fpga-9-hyb-0-sample-4

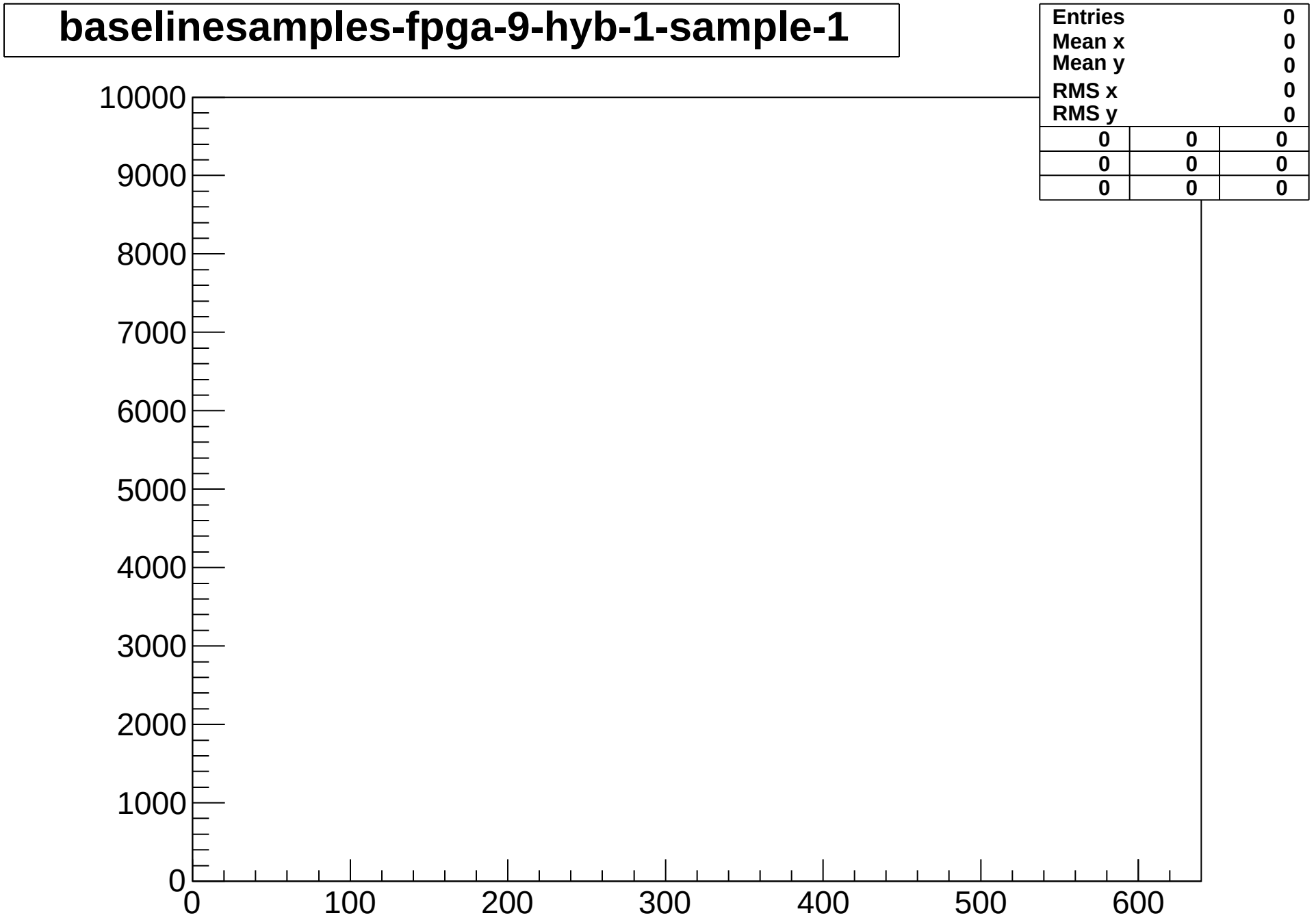


baselinesamples-fpga-9-hyb-0-sample-5

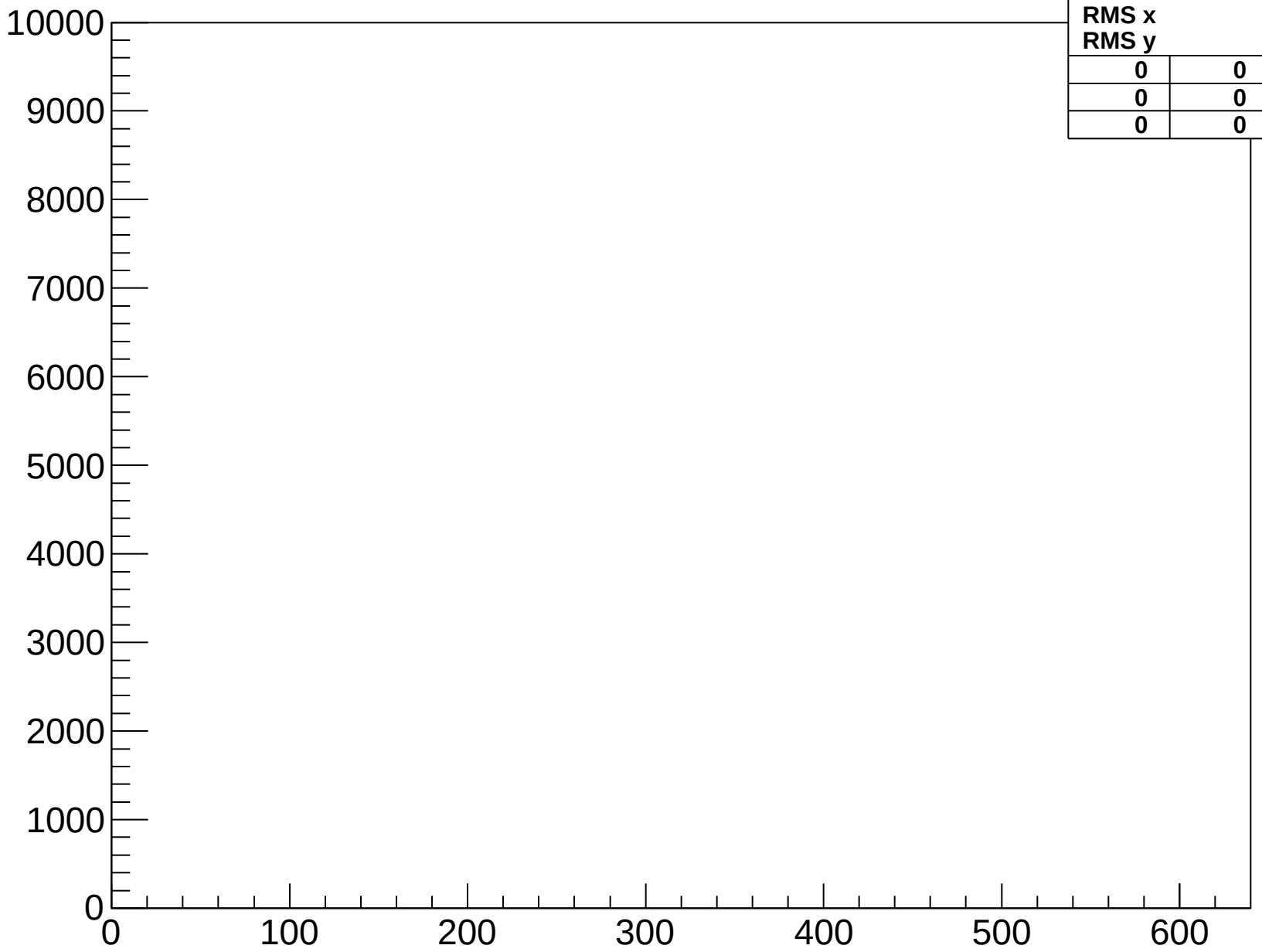



baselinesamples-fpga-9-hyb-1-sample-0
Entries 0
Mean x 0
Mean y 0
RMS x 0
RMS y 0
0 0 0
0 0 0
0 0 0
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600

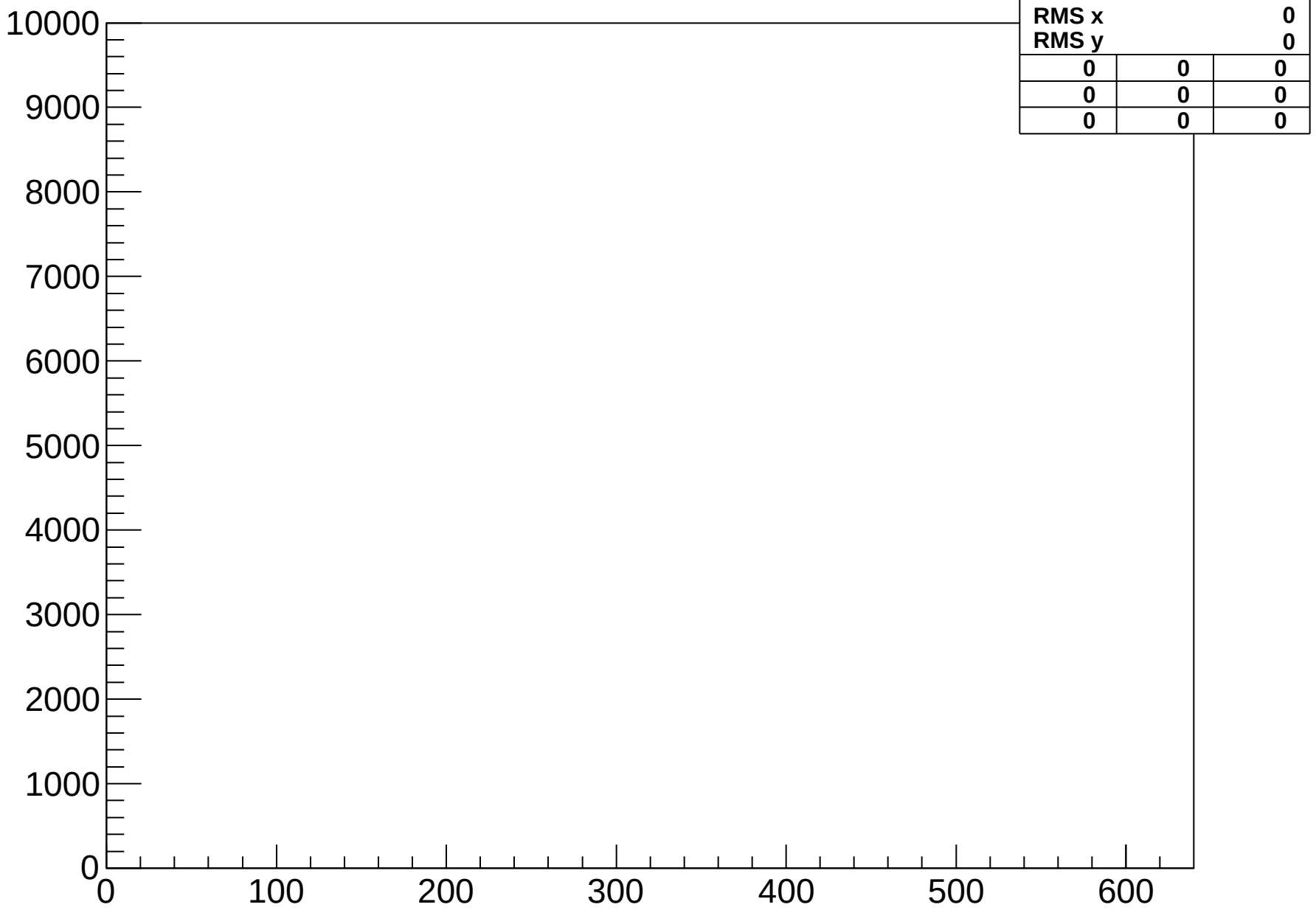
baselinesamples-fpga-9-hyb-1-sample-1



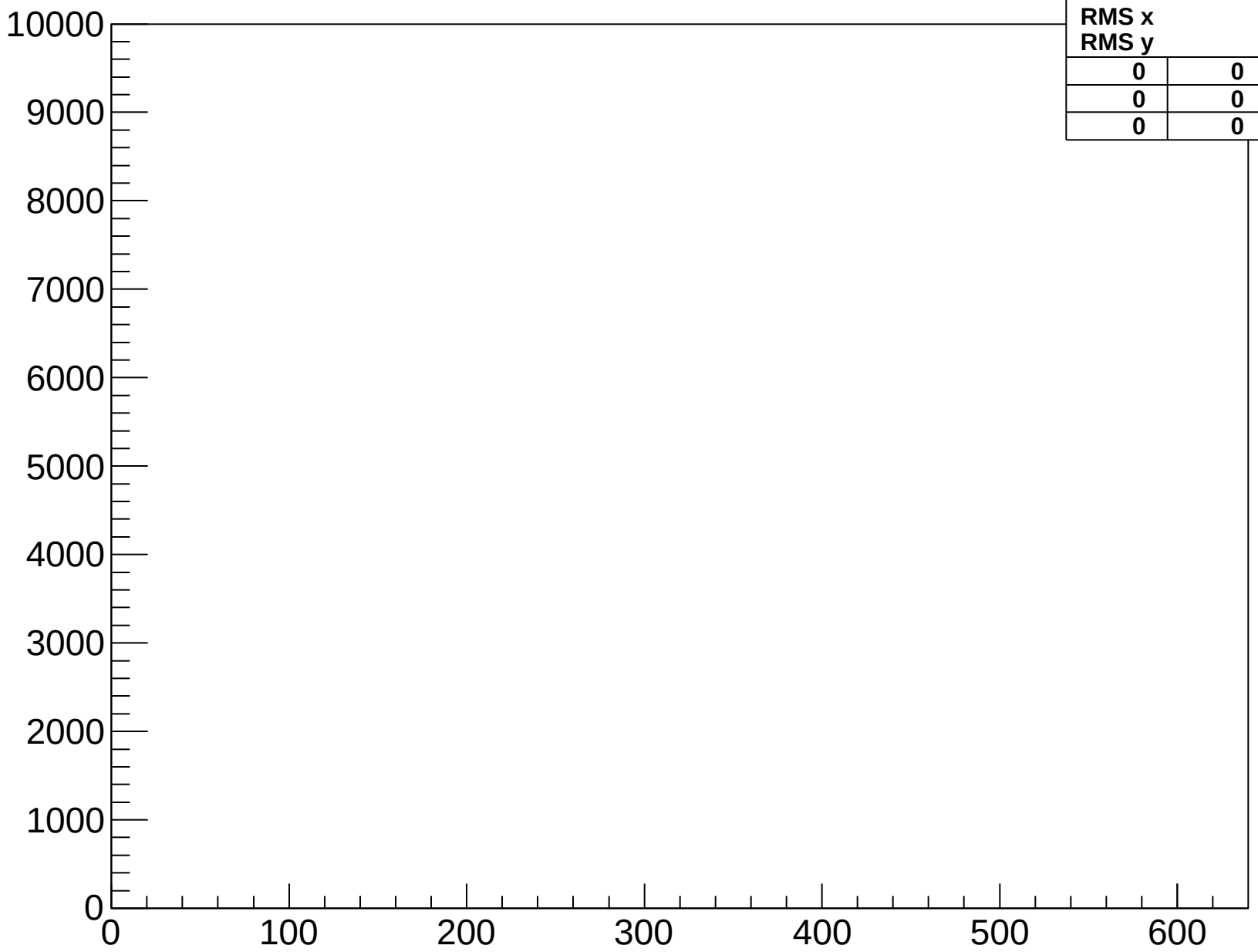
baselinesamples-fpga-9-hyb-1-sample-2



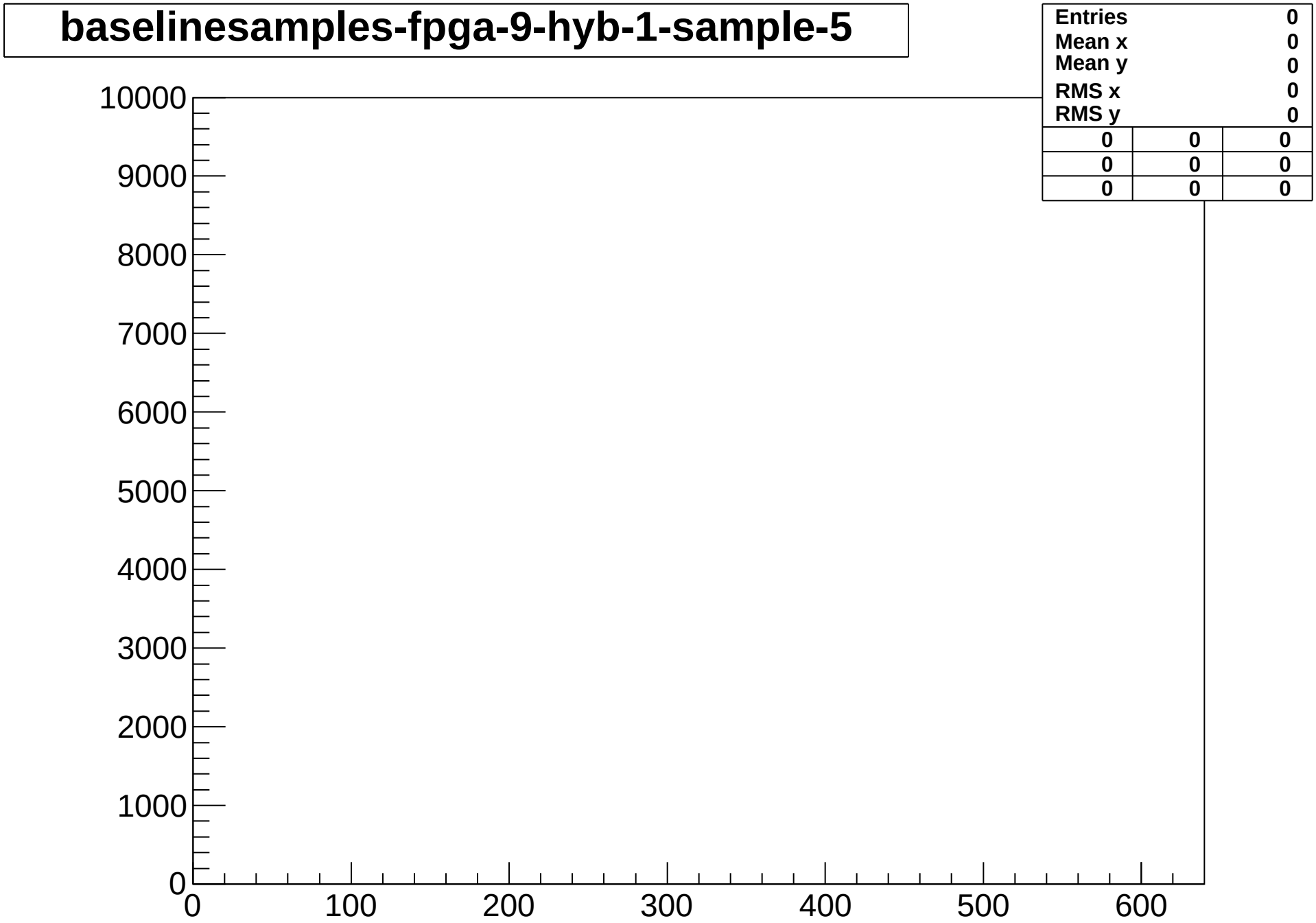
baselinesamples-fpga-9-hyb-1-sample-3



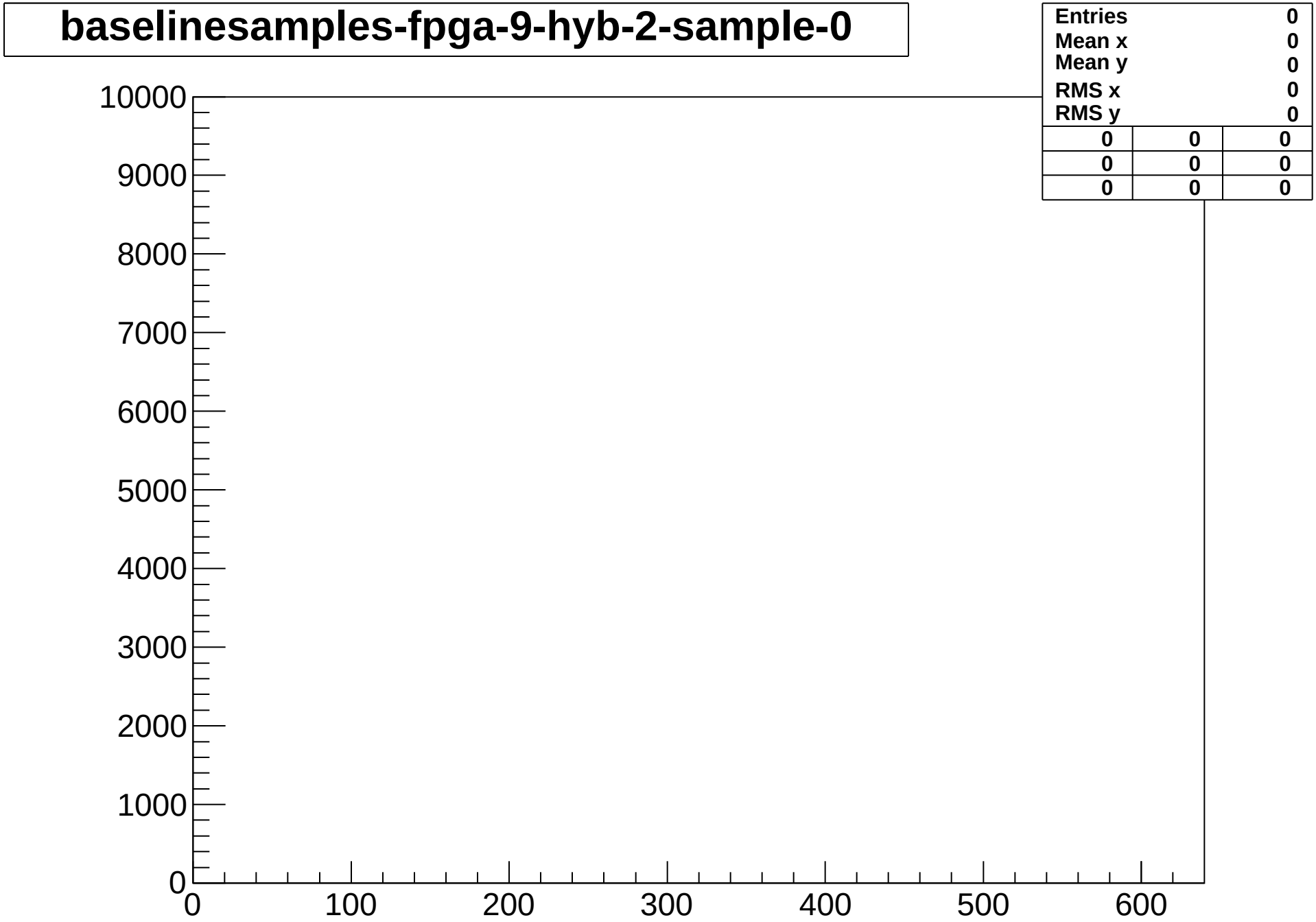
baselinesamples-fpga-9-hyb-1-sample-4



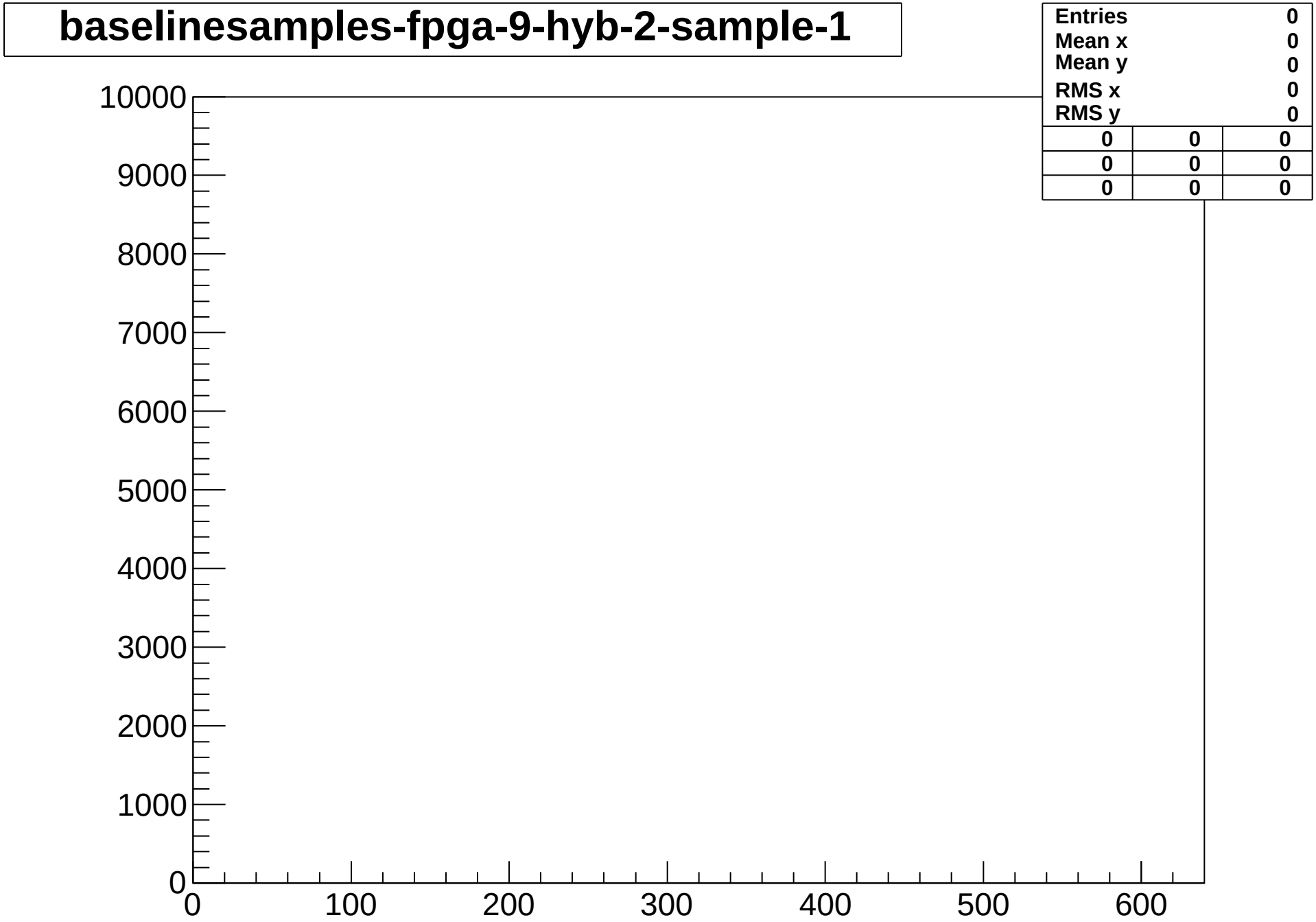
baselinesamples-fpga-9-hyb-1-sample-5



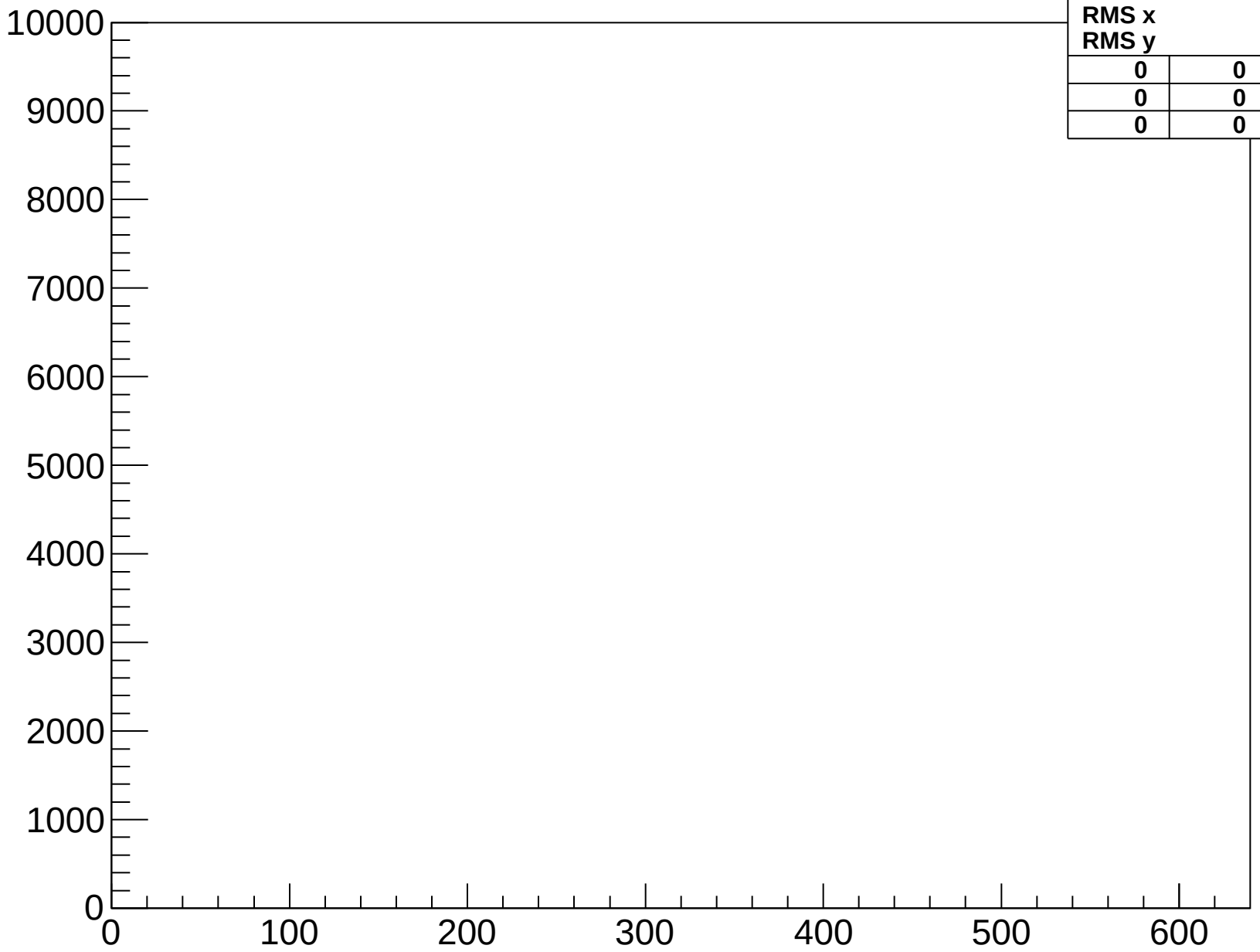
baselinesamples-fpga-9-hyb-2-sample-0



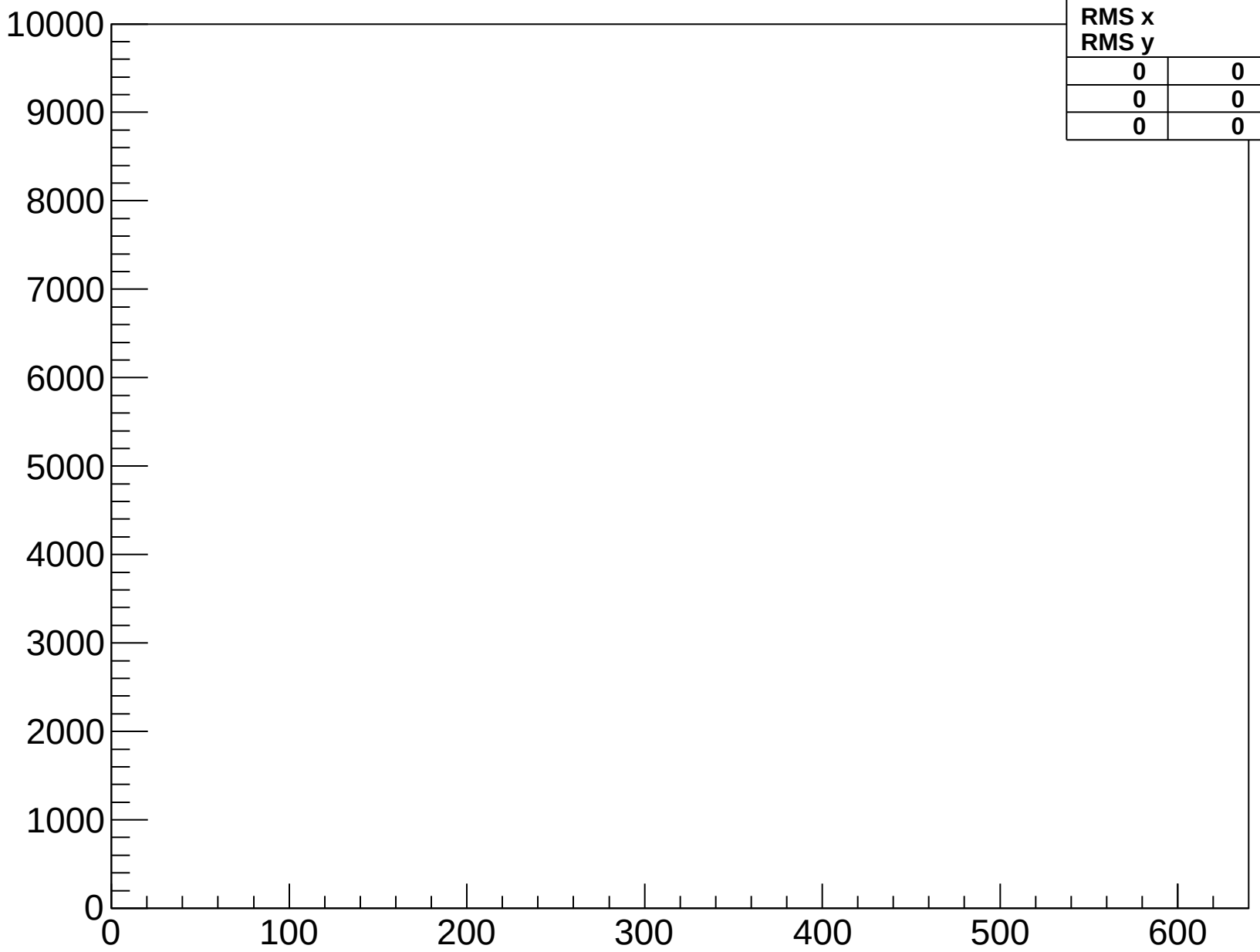
baselinesamples-fpga-9-hyb-2-sample-1



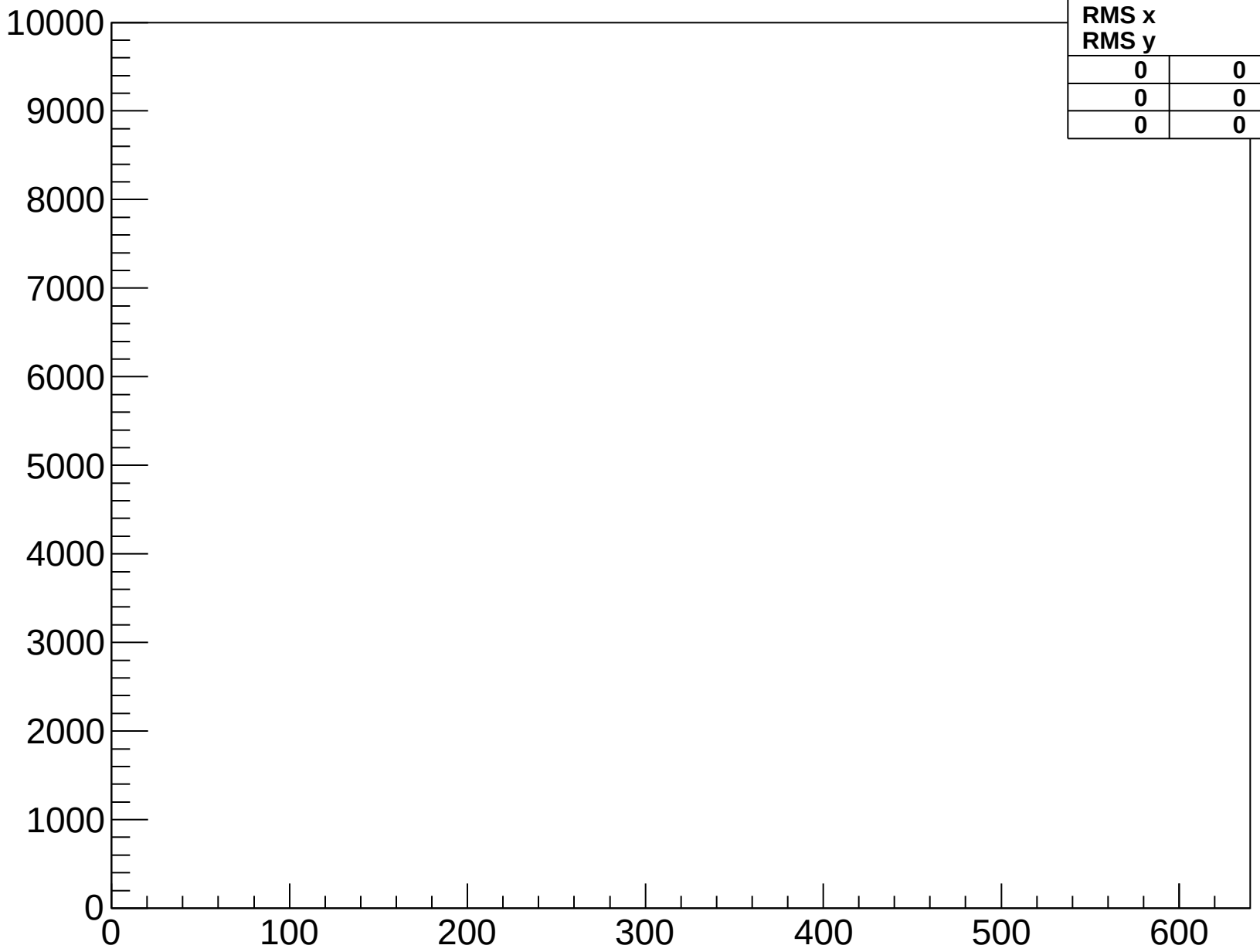
baselinesamples-fpga-9-hyb-2-sample-2



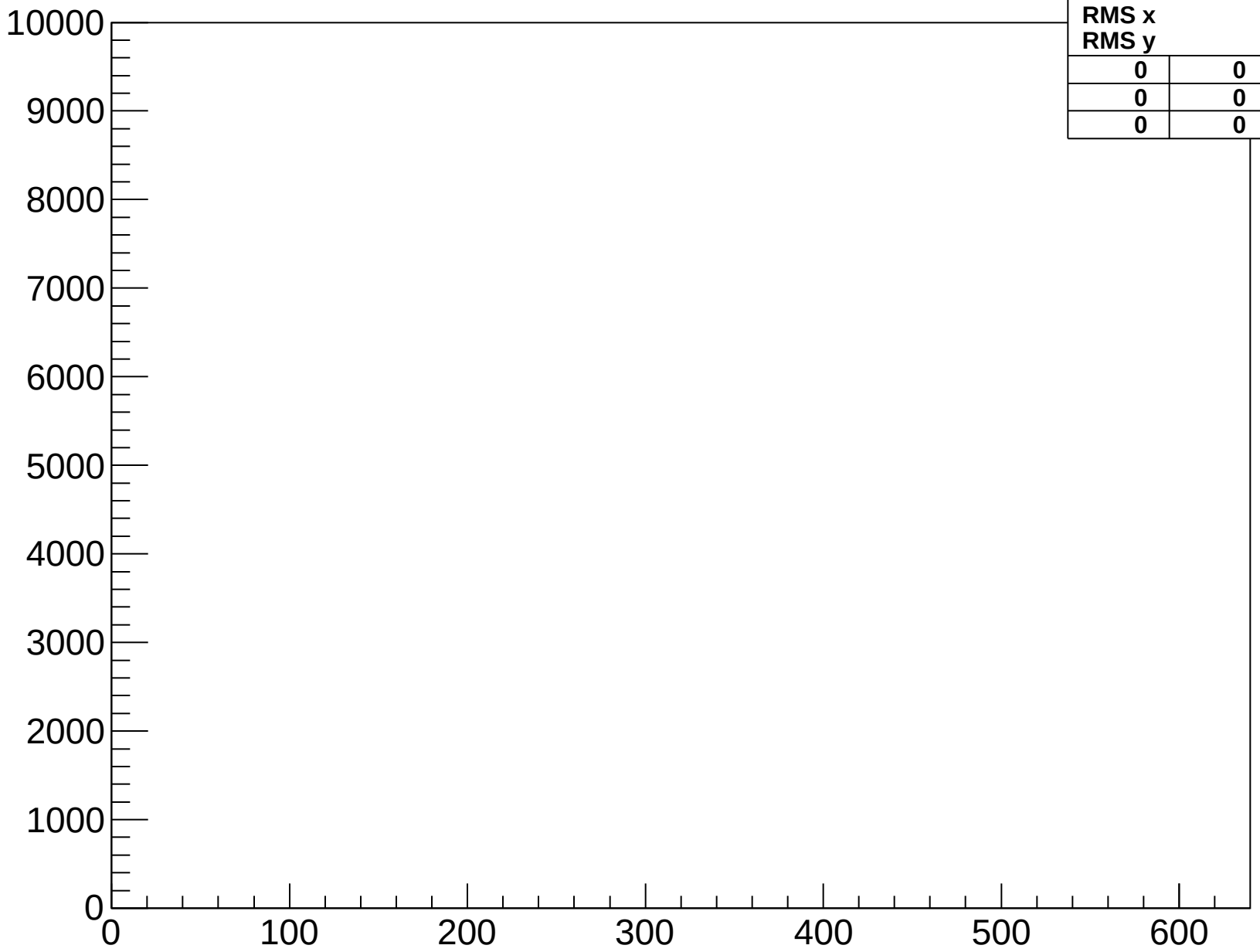
baselinesamples-fpga-9-hyb-2-sample-3



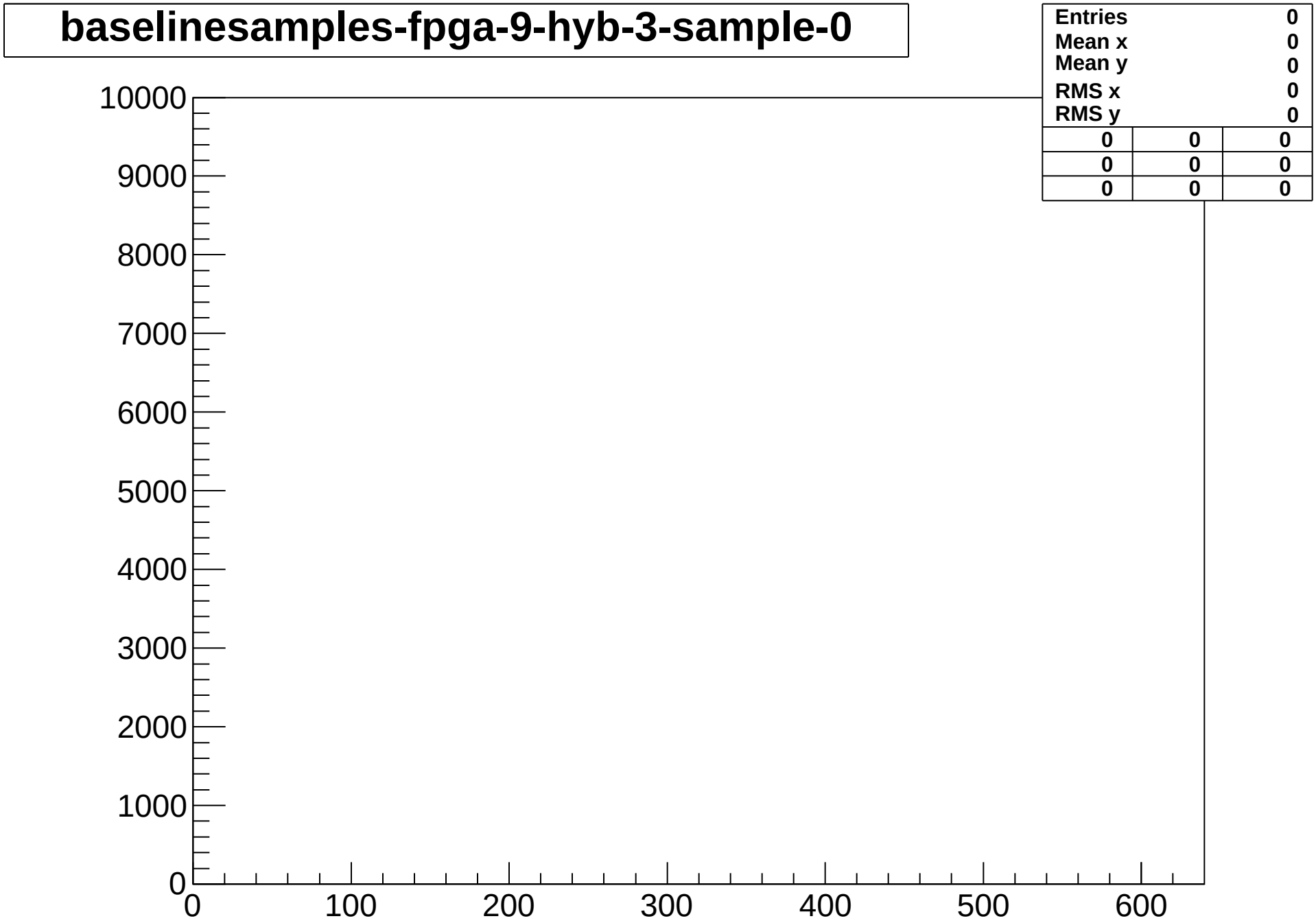
baselinesamples-fpga-9-hyb-2-sample-4



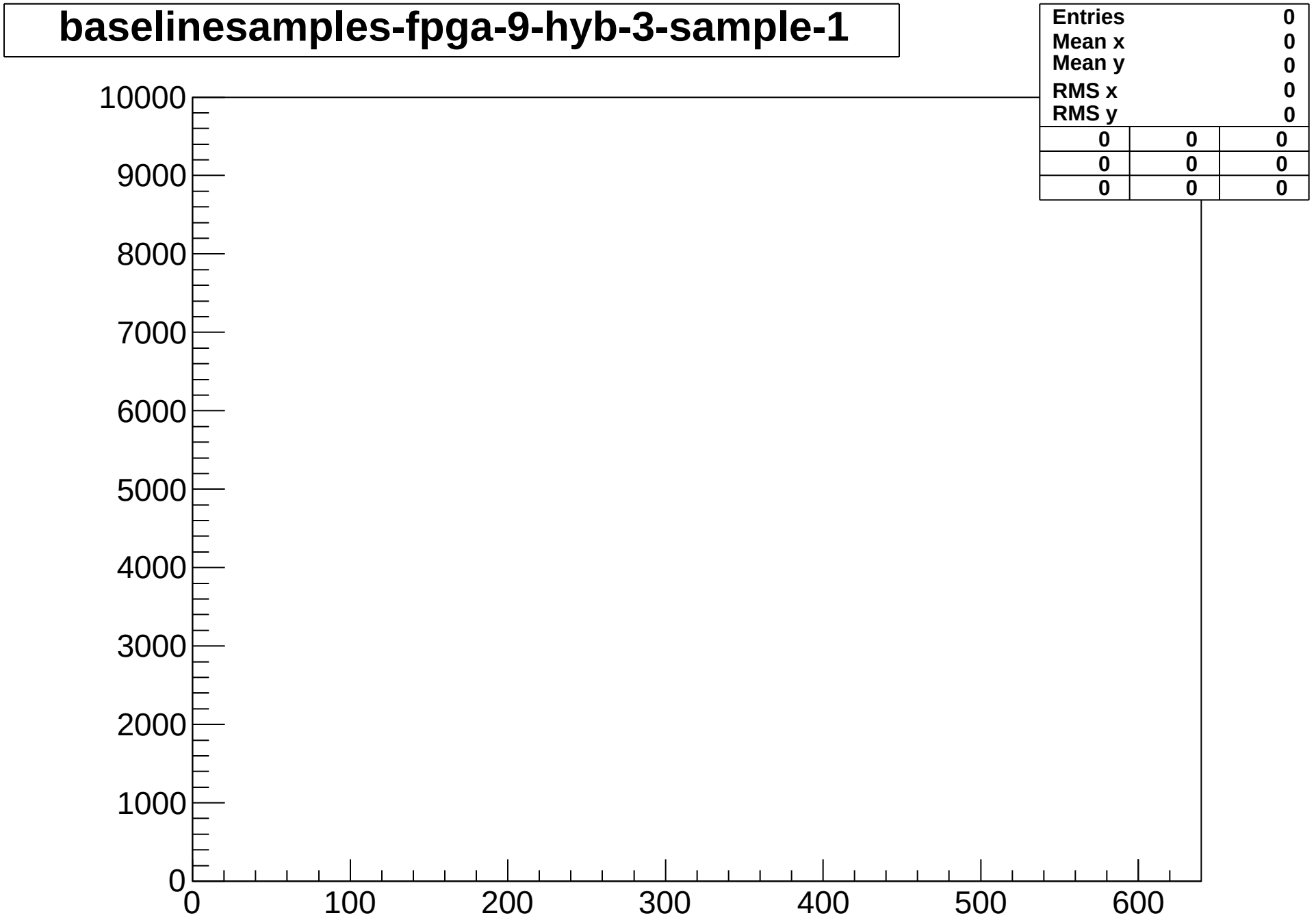
baselinesamples-fpga-9-hyb-2-sample-5



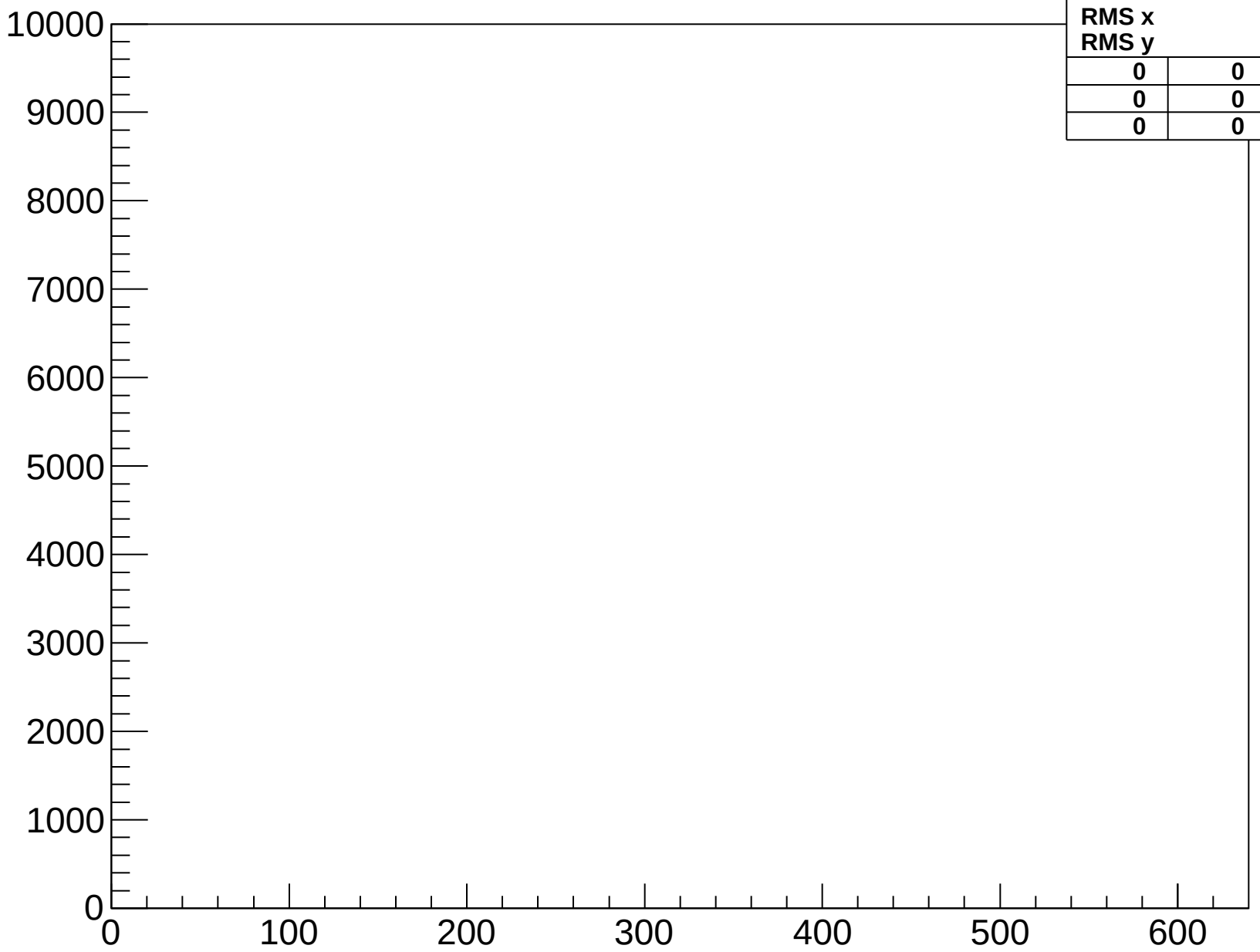
baselinesamples-fpga-9-hyb-3-sample-0



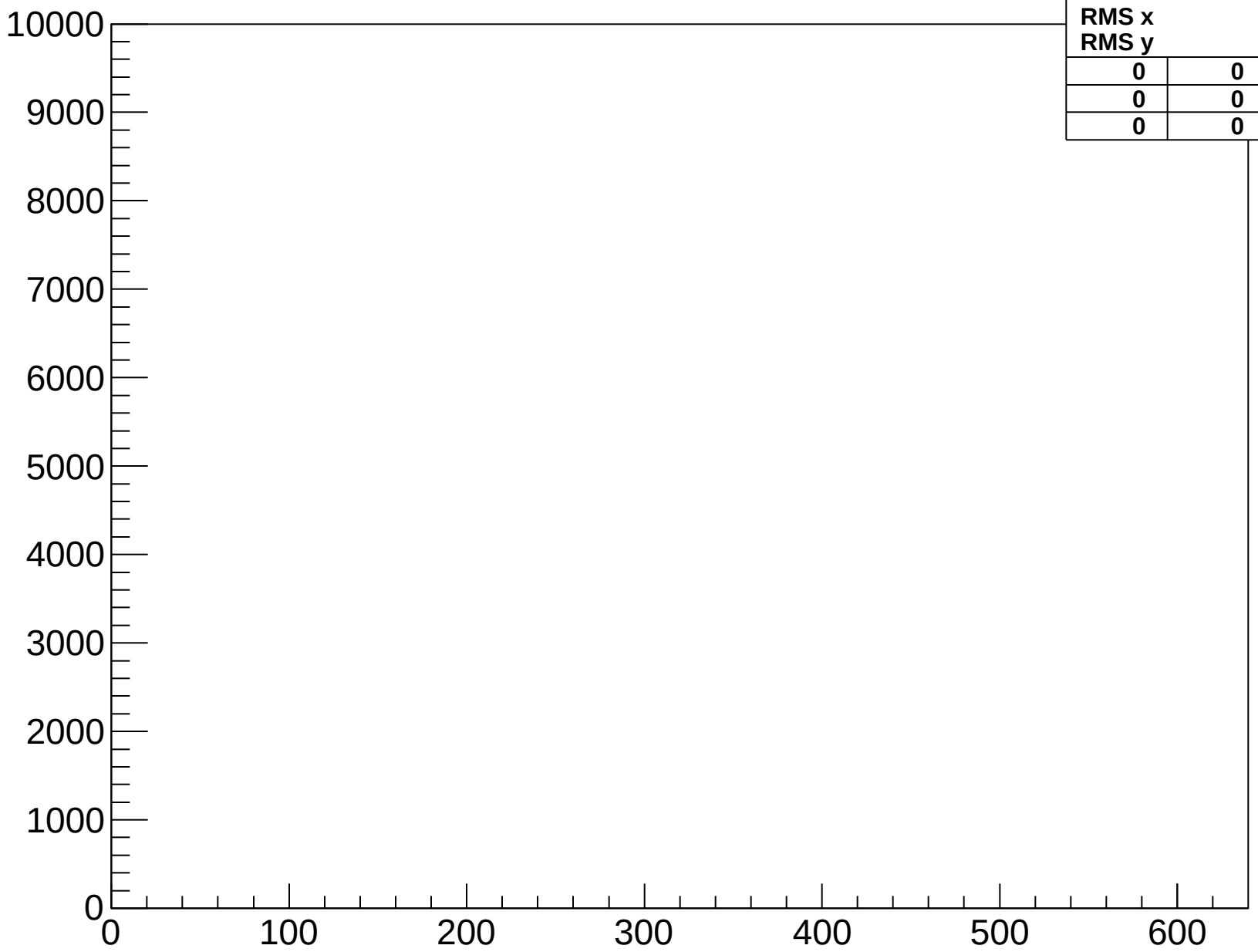
baselinesamples-fpga-9-hyb-3-sample-1



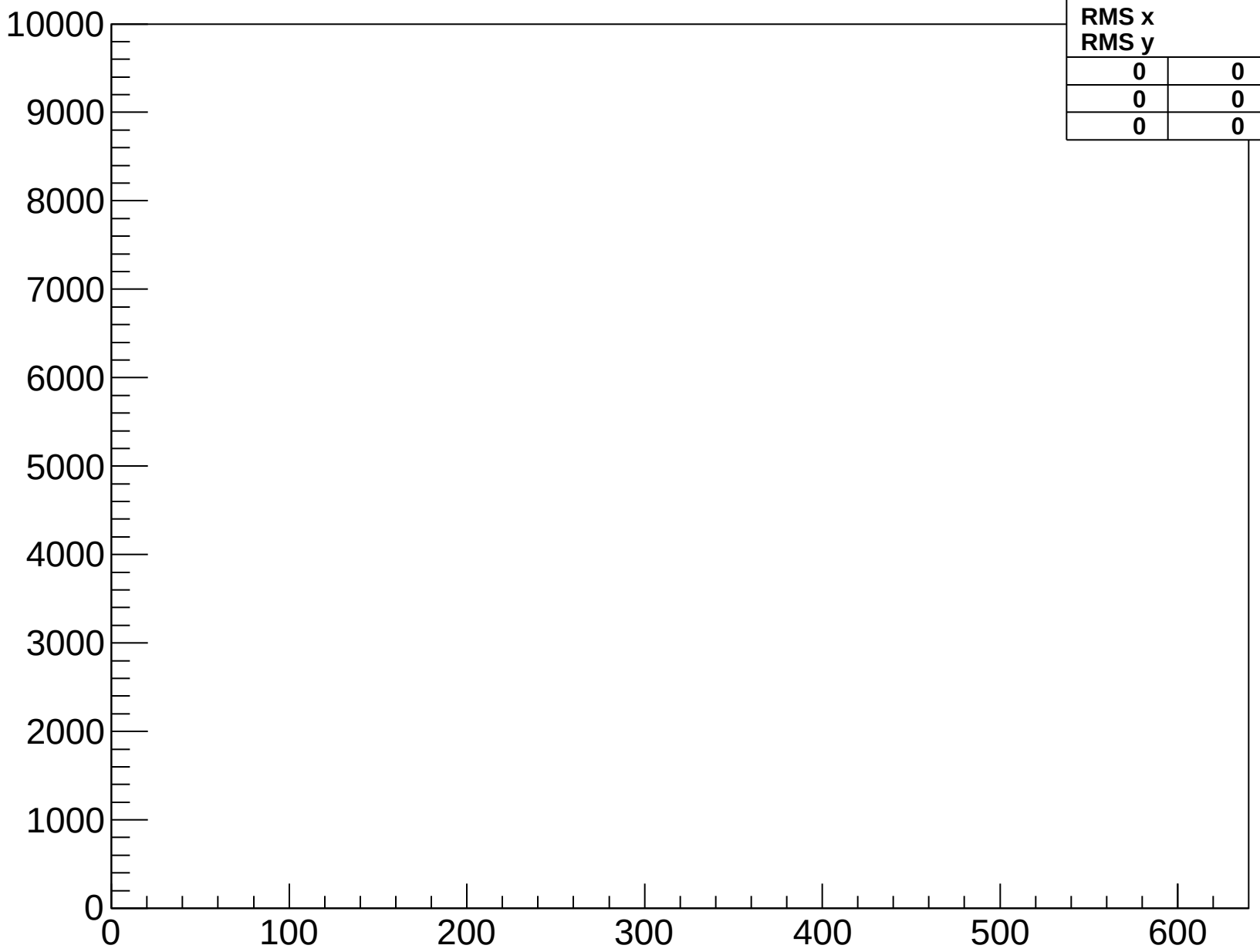
baselinesamples-fpga-9-hyb-3-sample-2



baselinesamples-fpga-9-hyb-3-sample-3



baselinesamples-fpga-9-hyb-3-sample-4



baselinesamples-fpga-9-hyb-3-sample-5