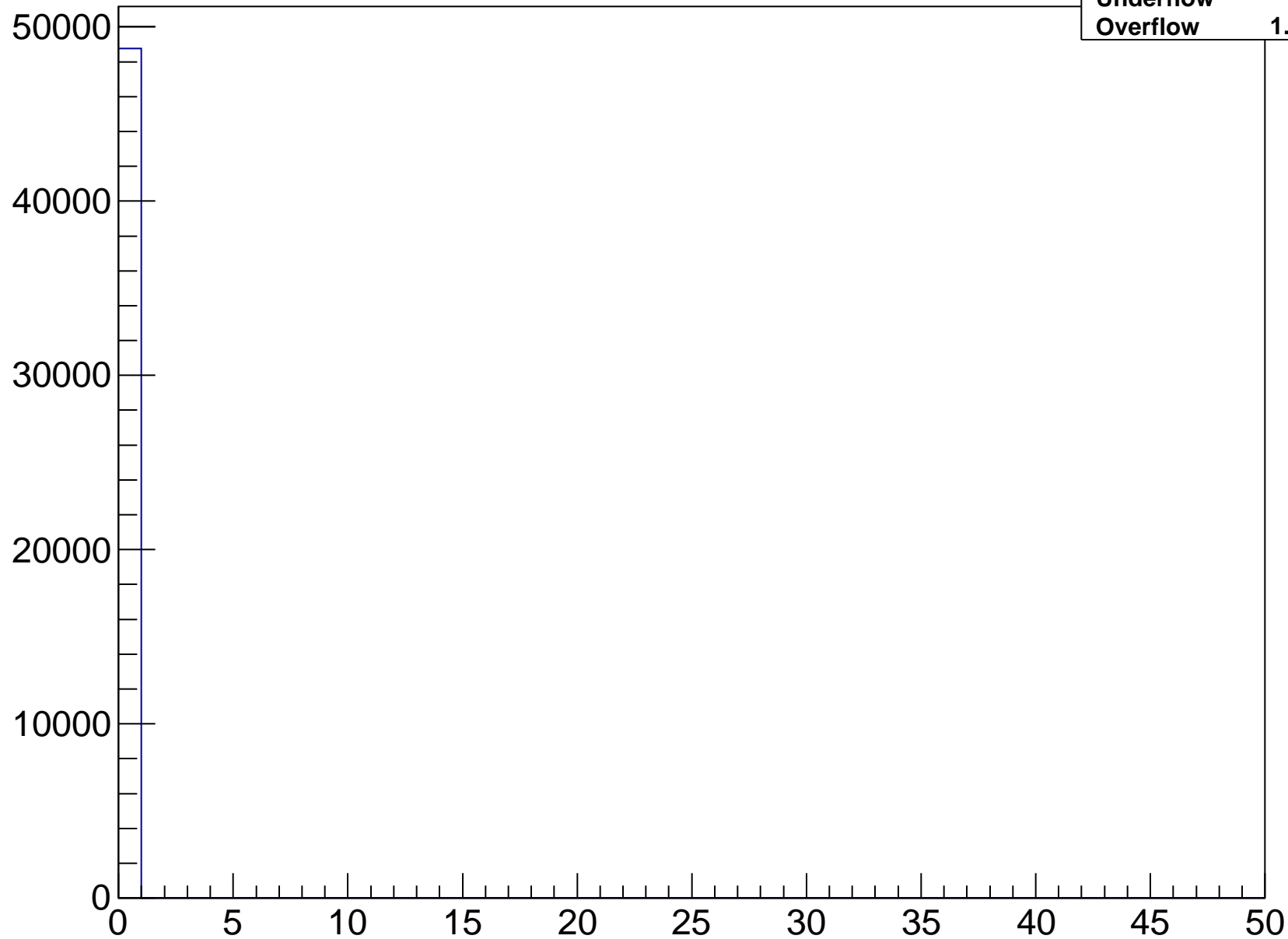
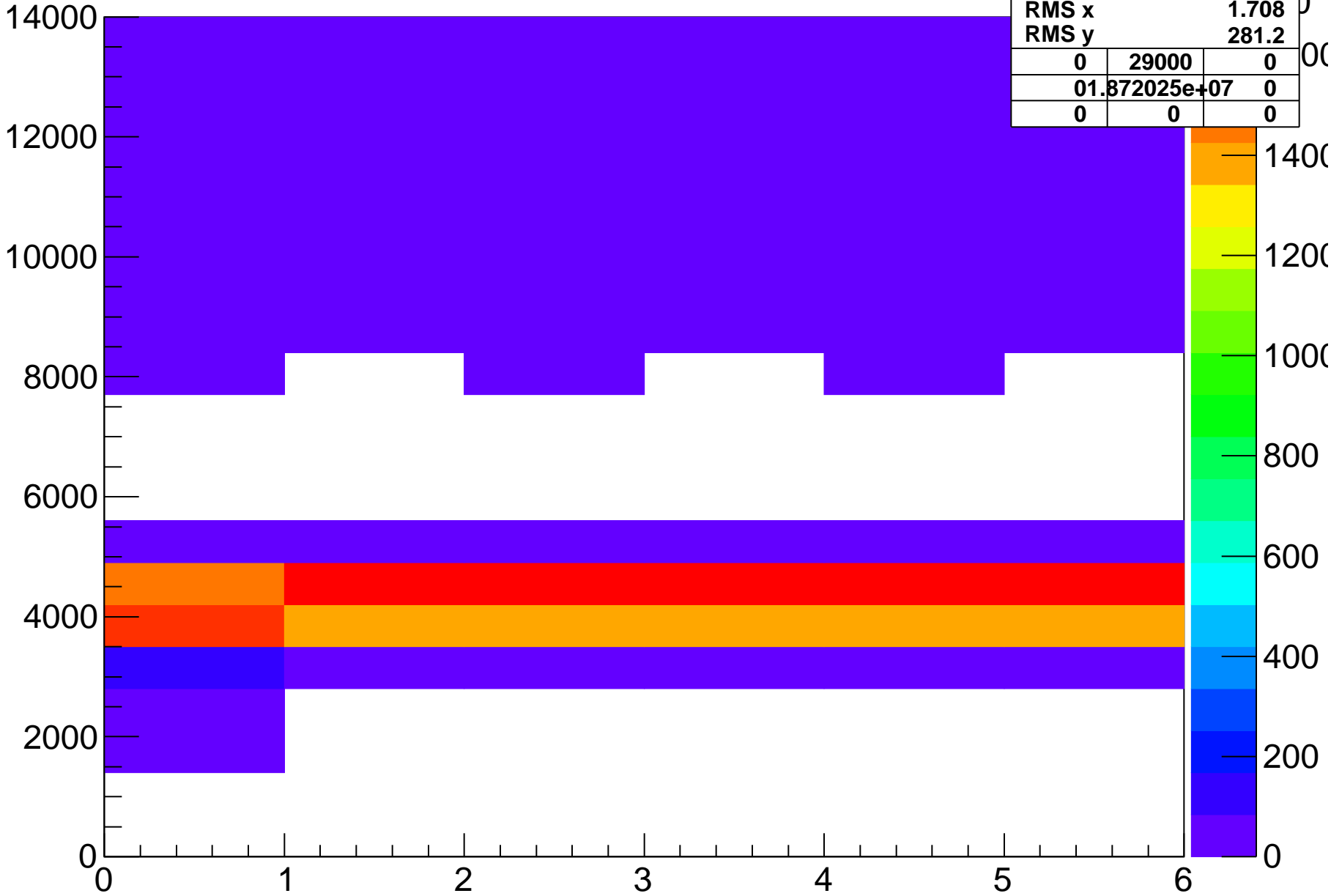


sampleCountHist

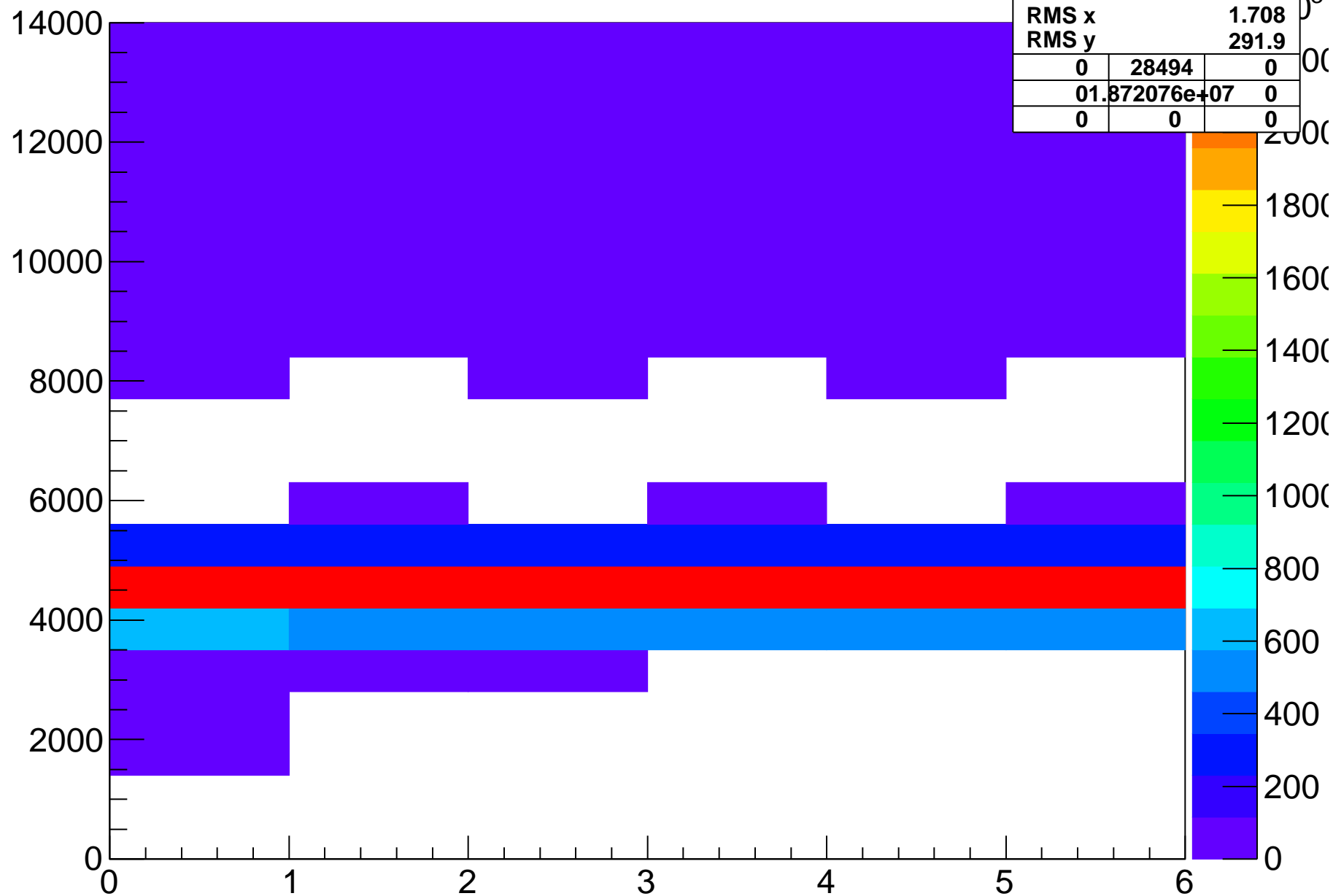
Entries	68250
Mean	0
RMS	0
Underflow	0
Overflow	1.95e+04



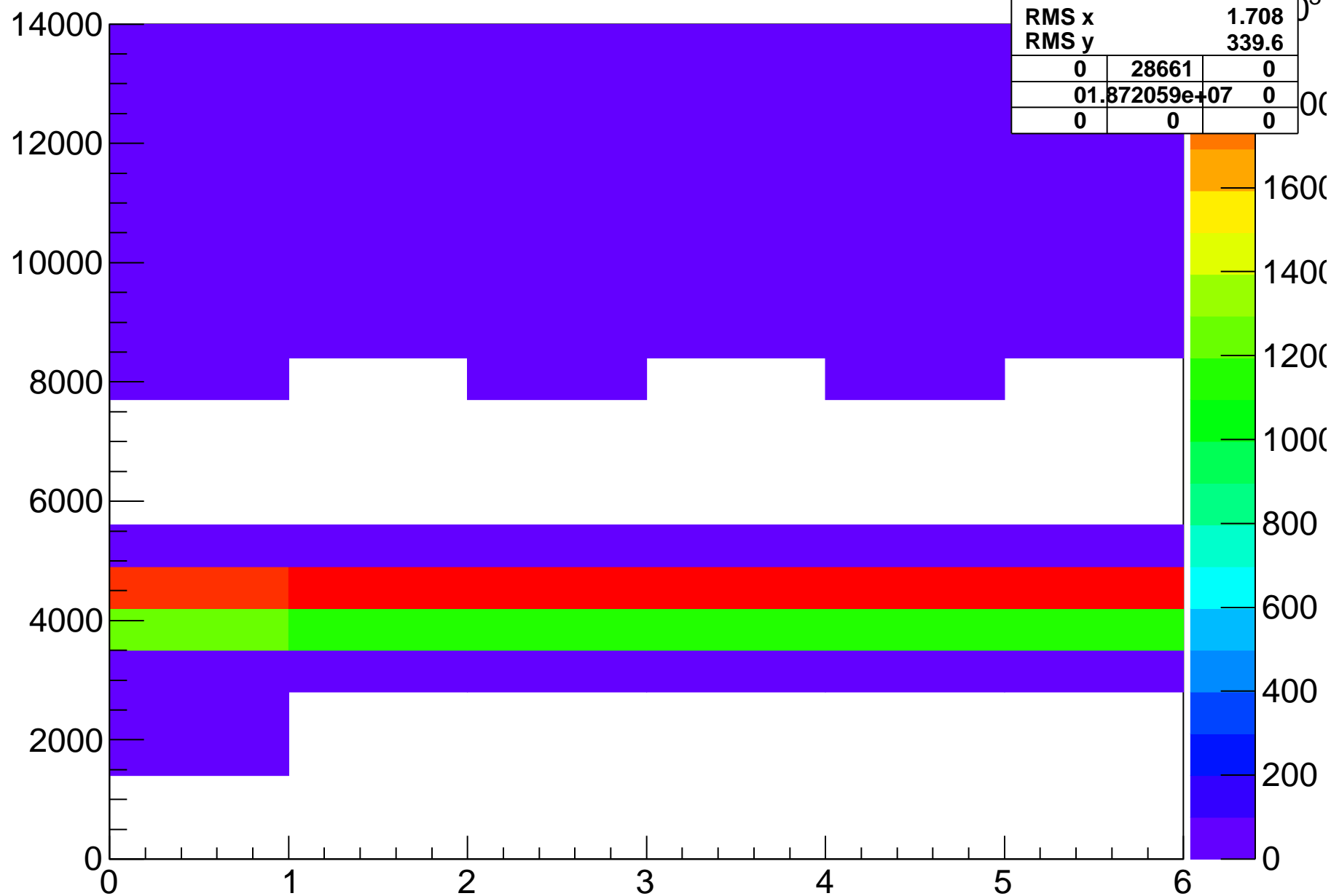
samples-fpga-0-hyb-0



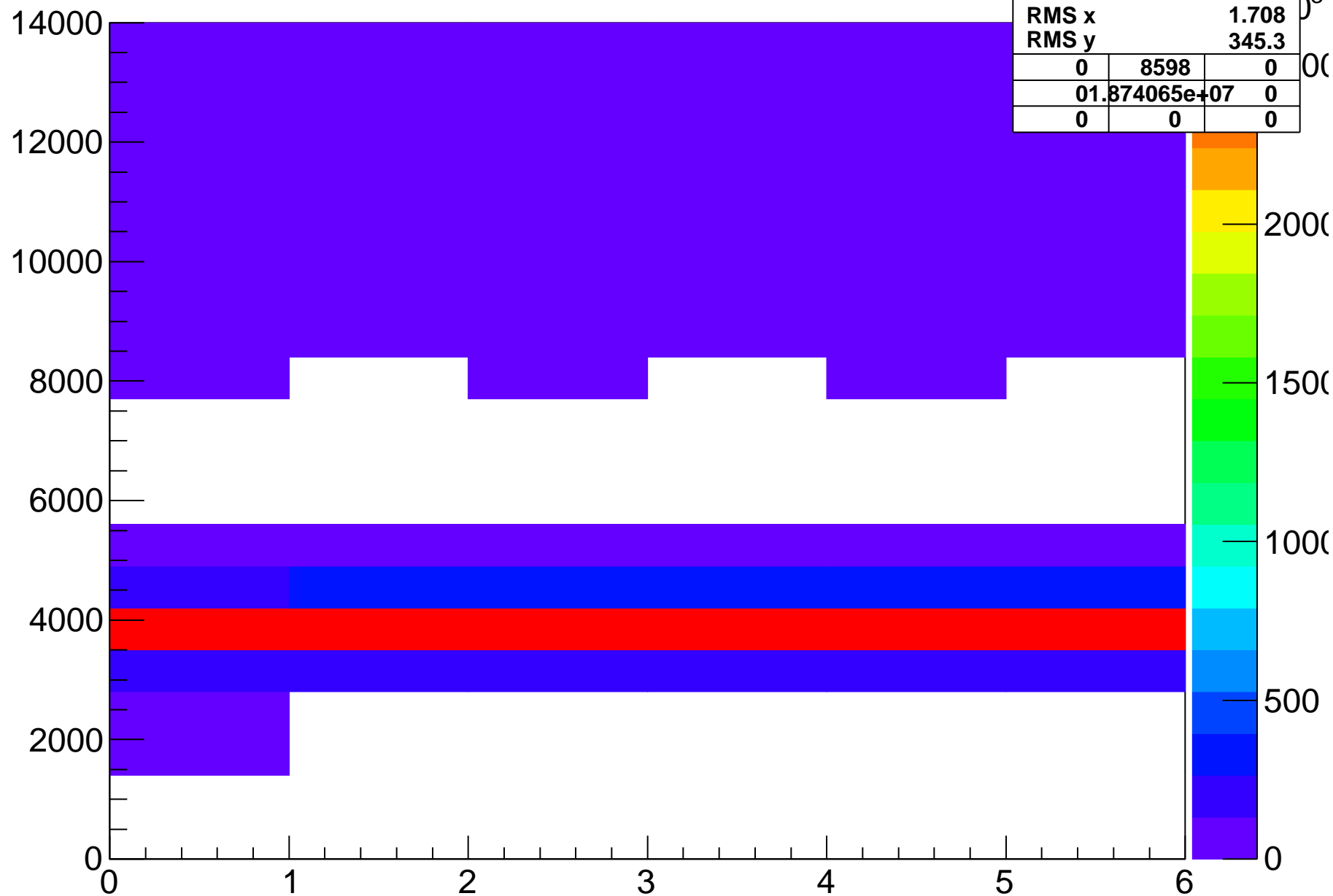
samples-fpga-0-hyb-1



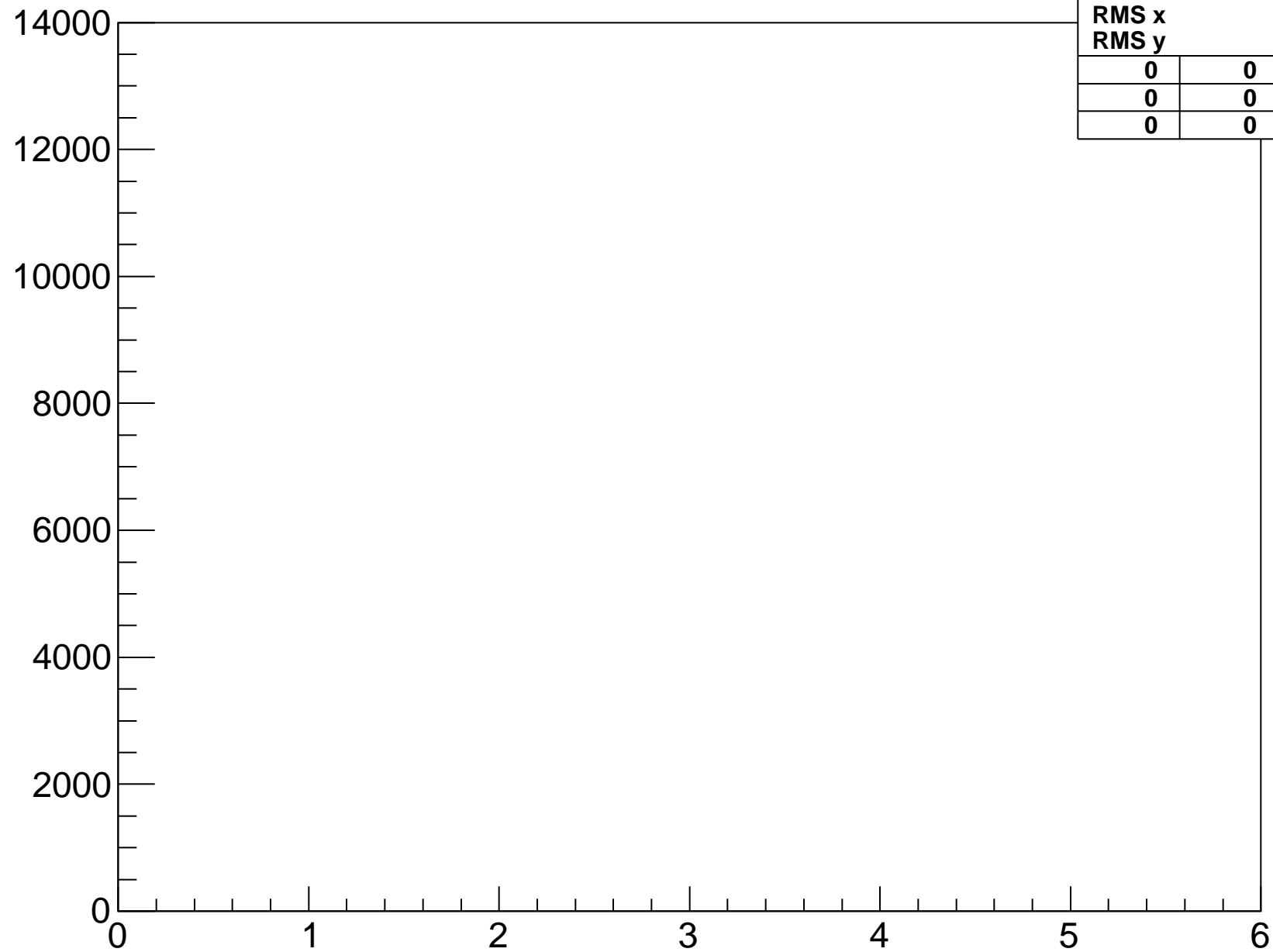
samples-fpga-0-hyb-2



samples-fpga-0-hyb-3

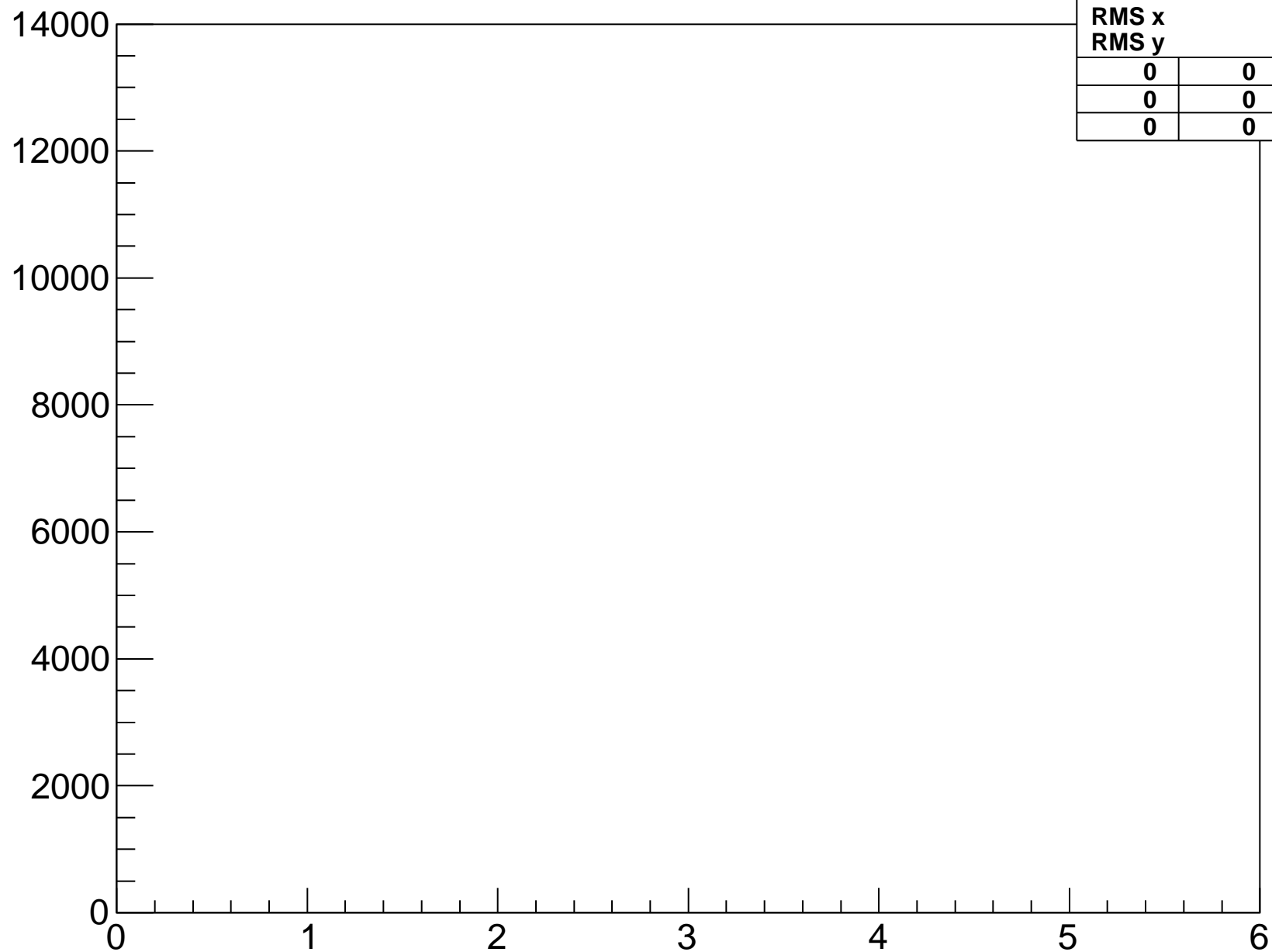


samples-fpga-1-hyb-0



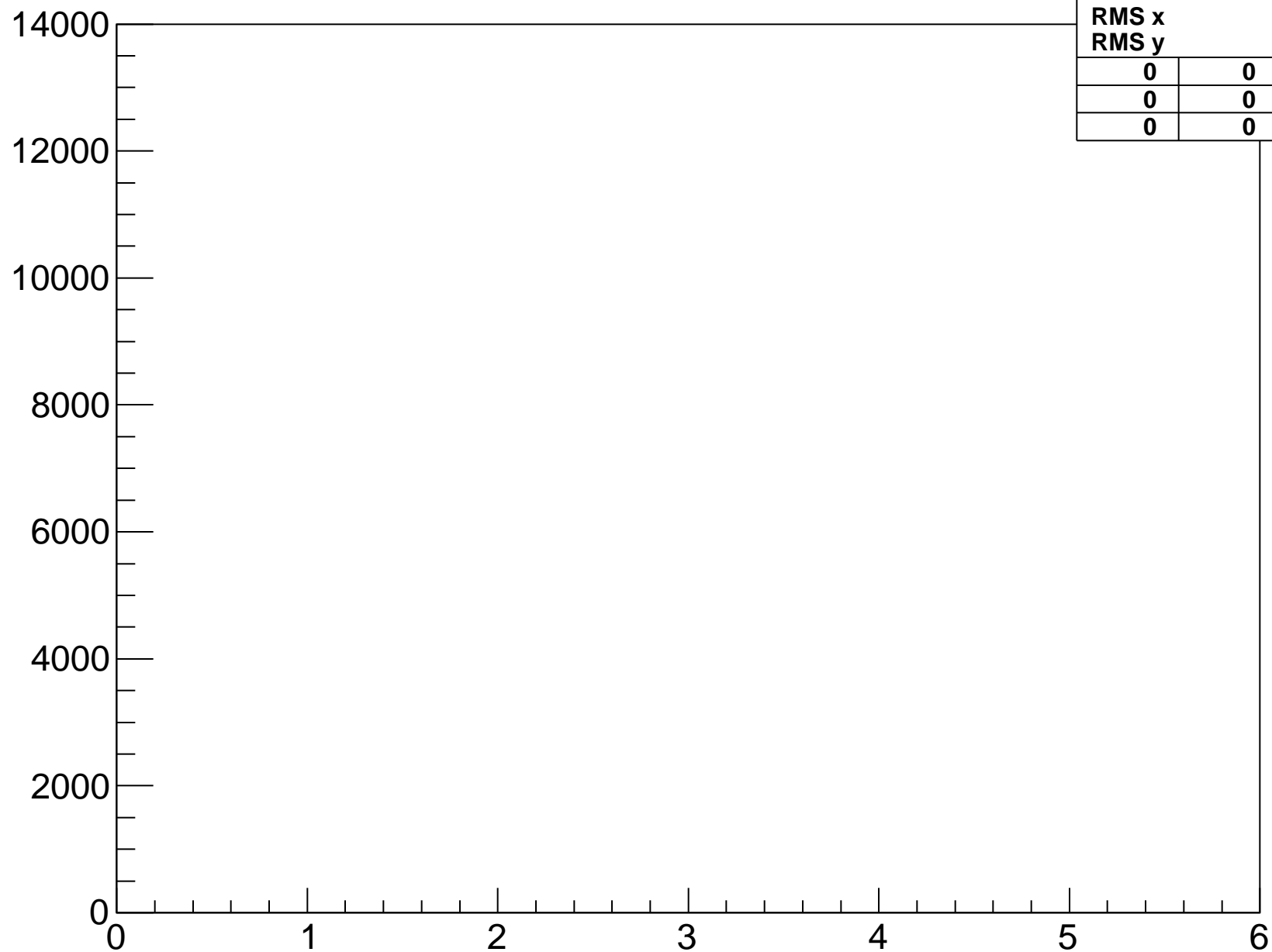
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-1-hyb-1



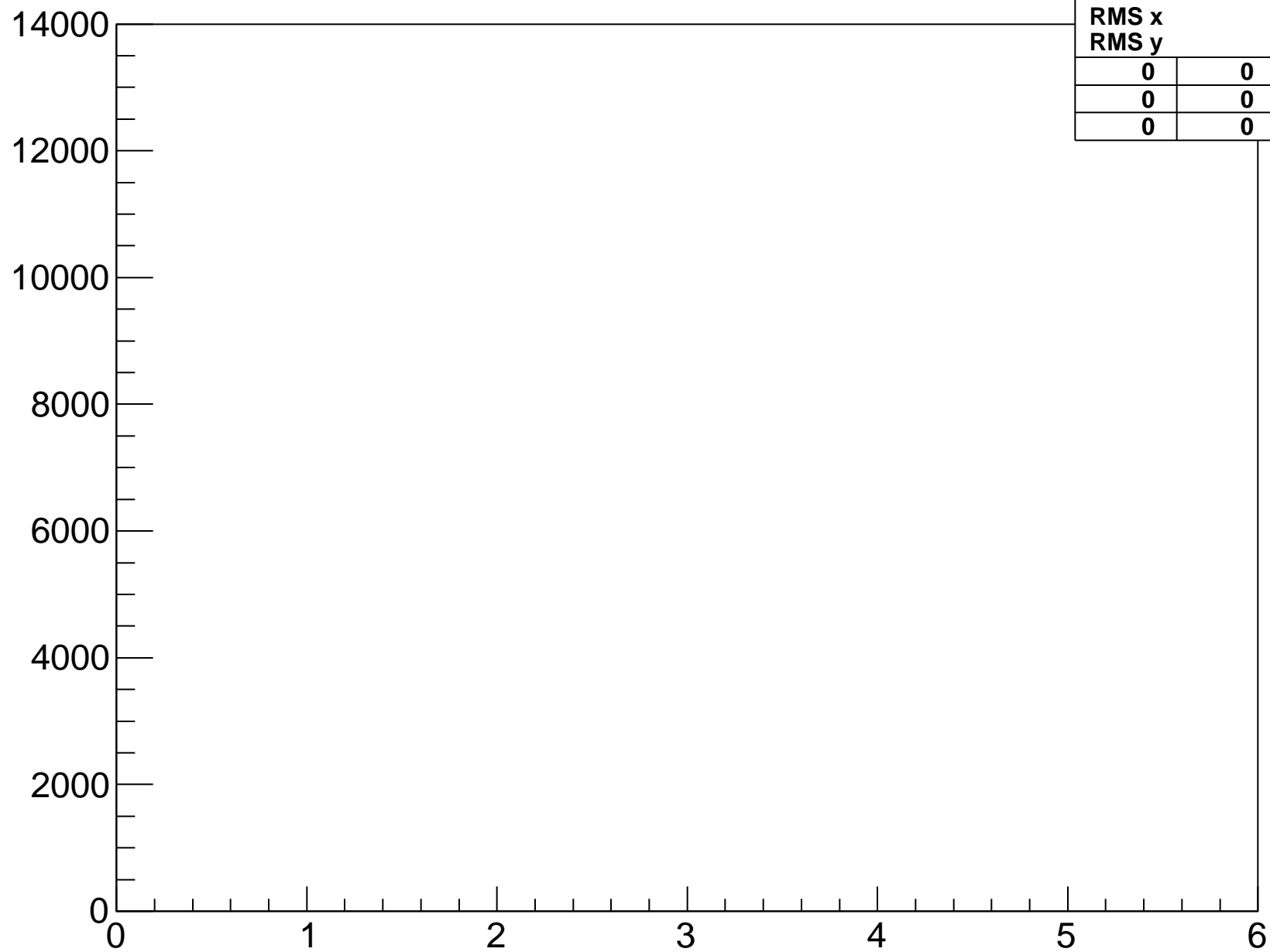
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-1-hyb-2



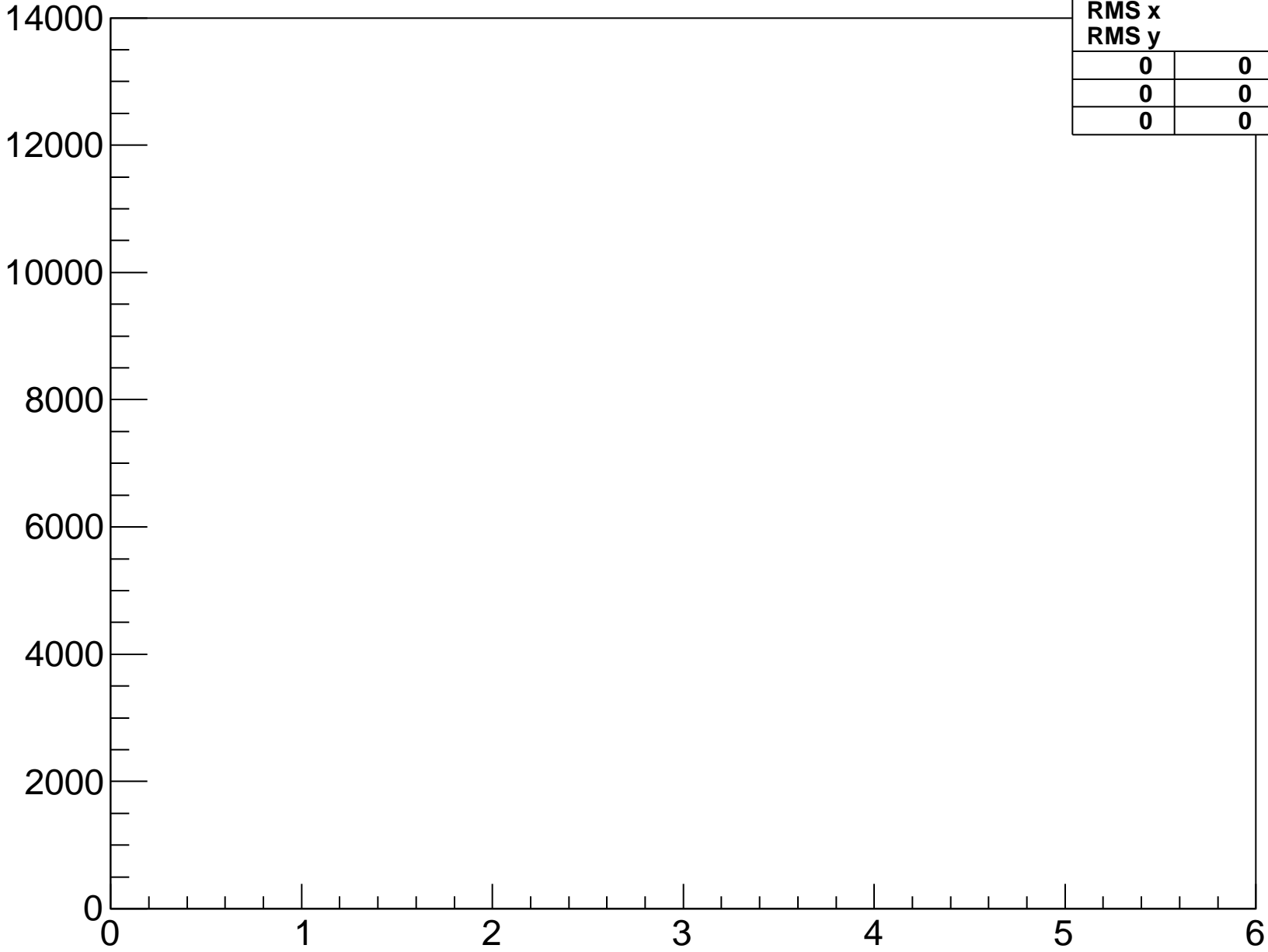
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-1-hyb-3



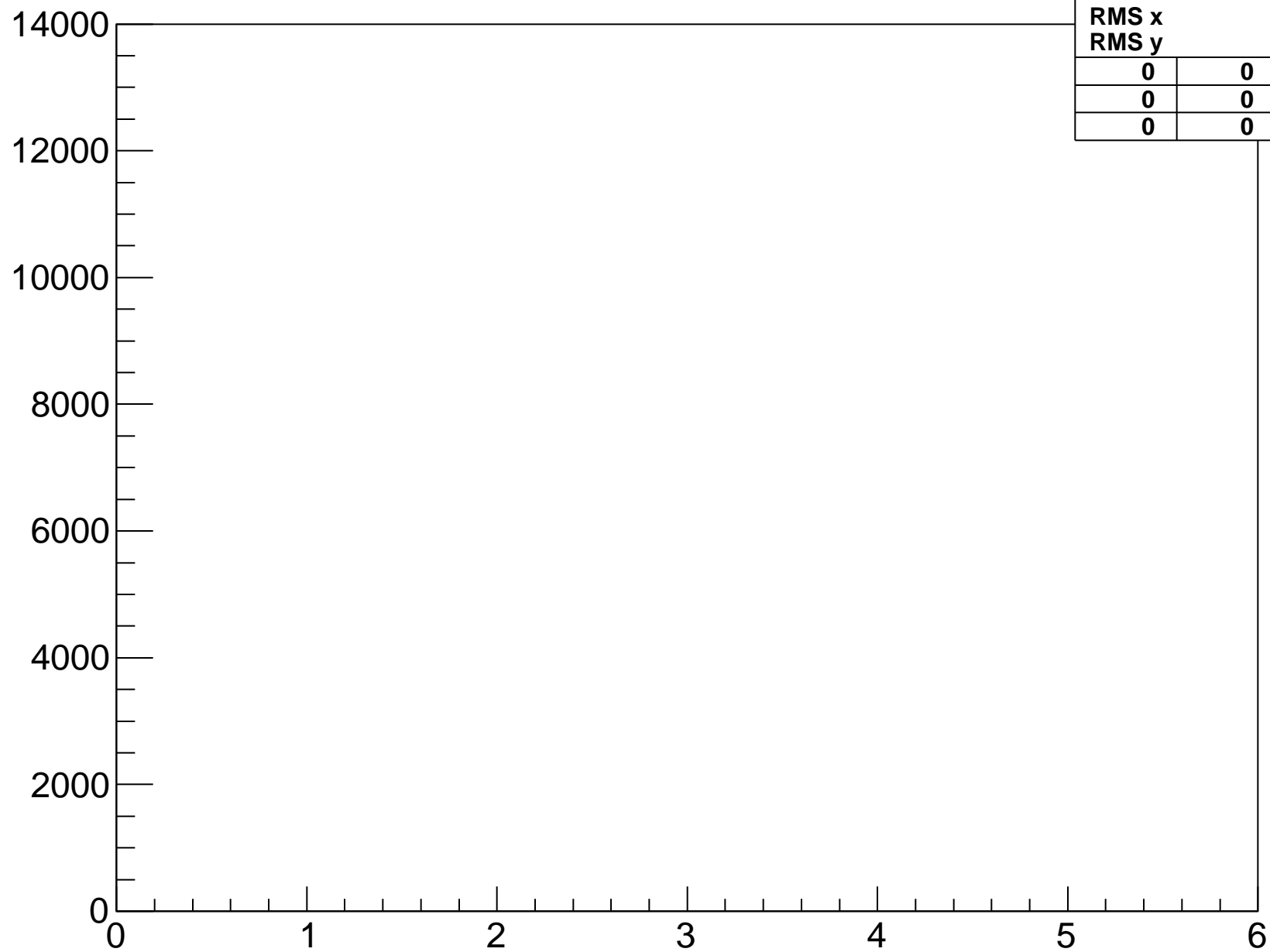
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-2-hyb-0



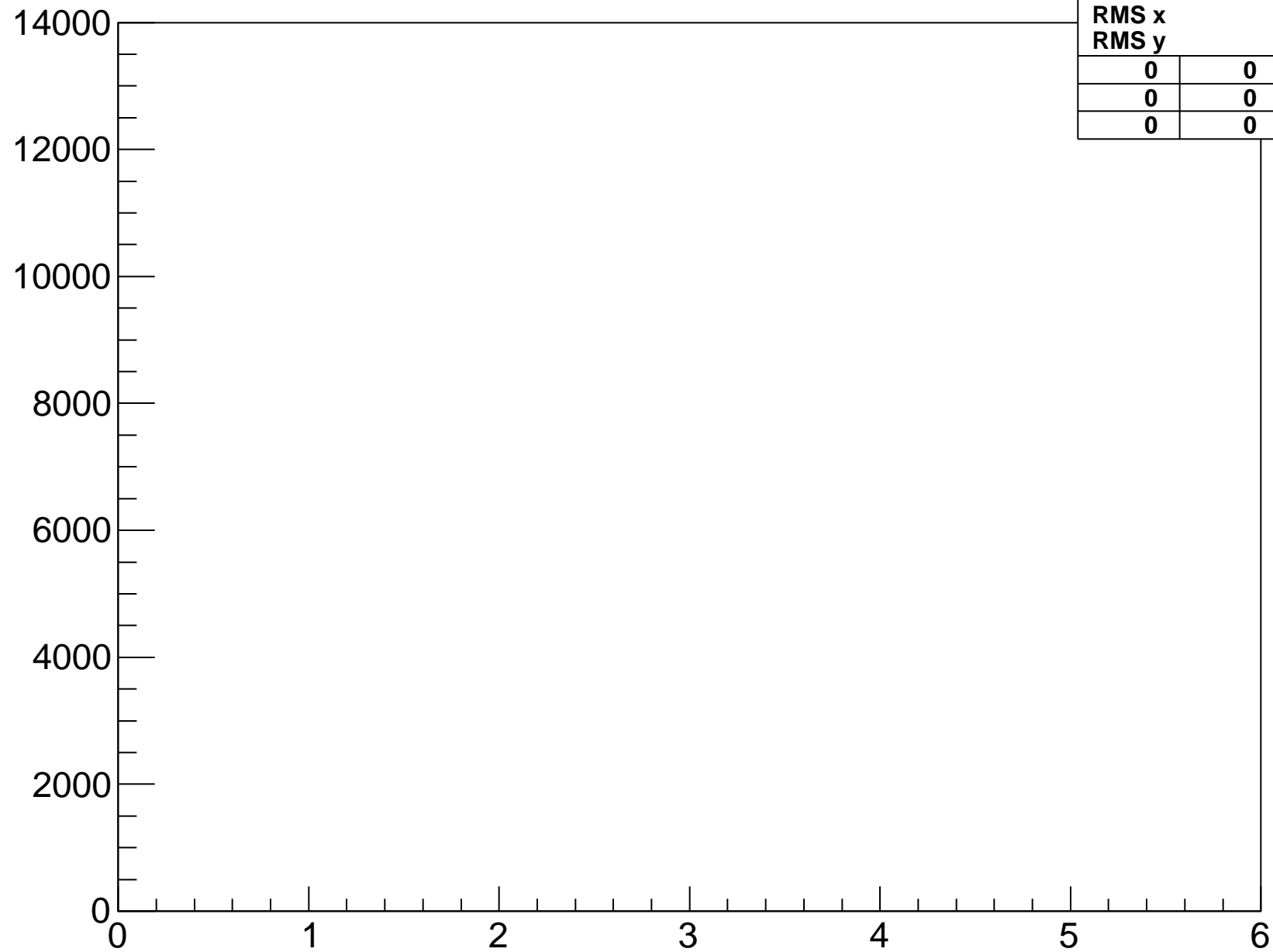
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-2-hyb-1



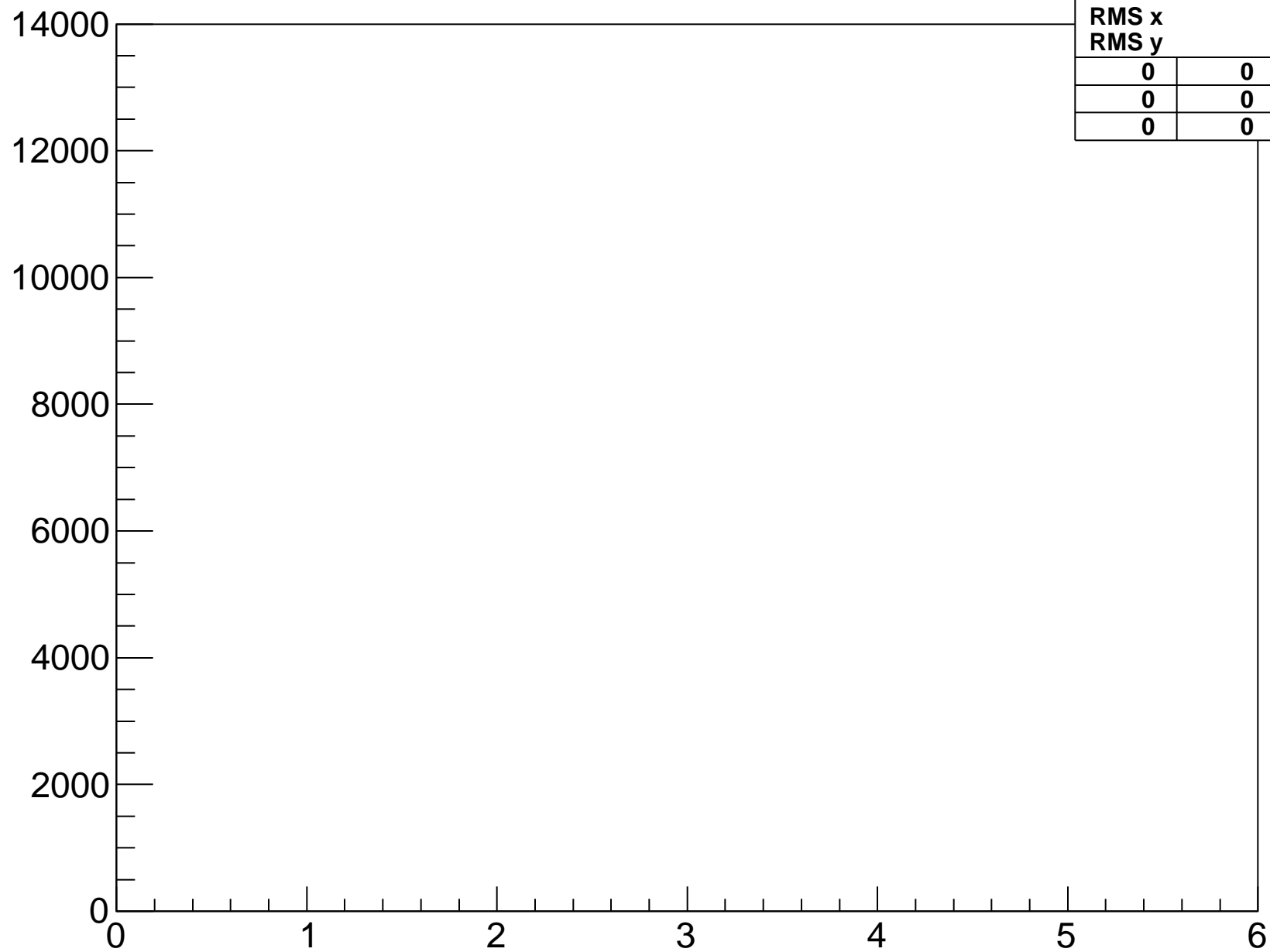
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

samples-fpga-2-hyb-2



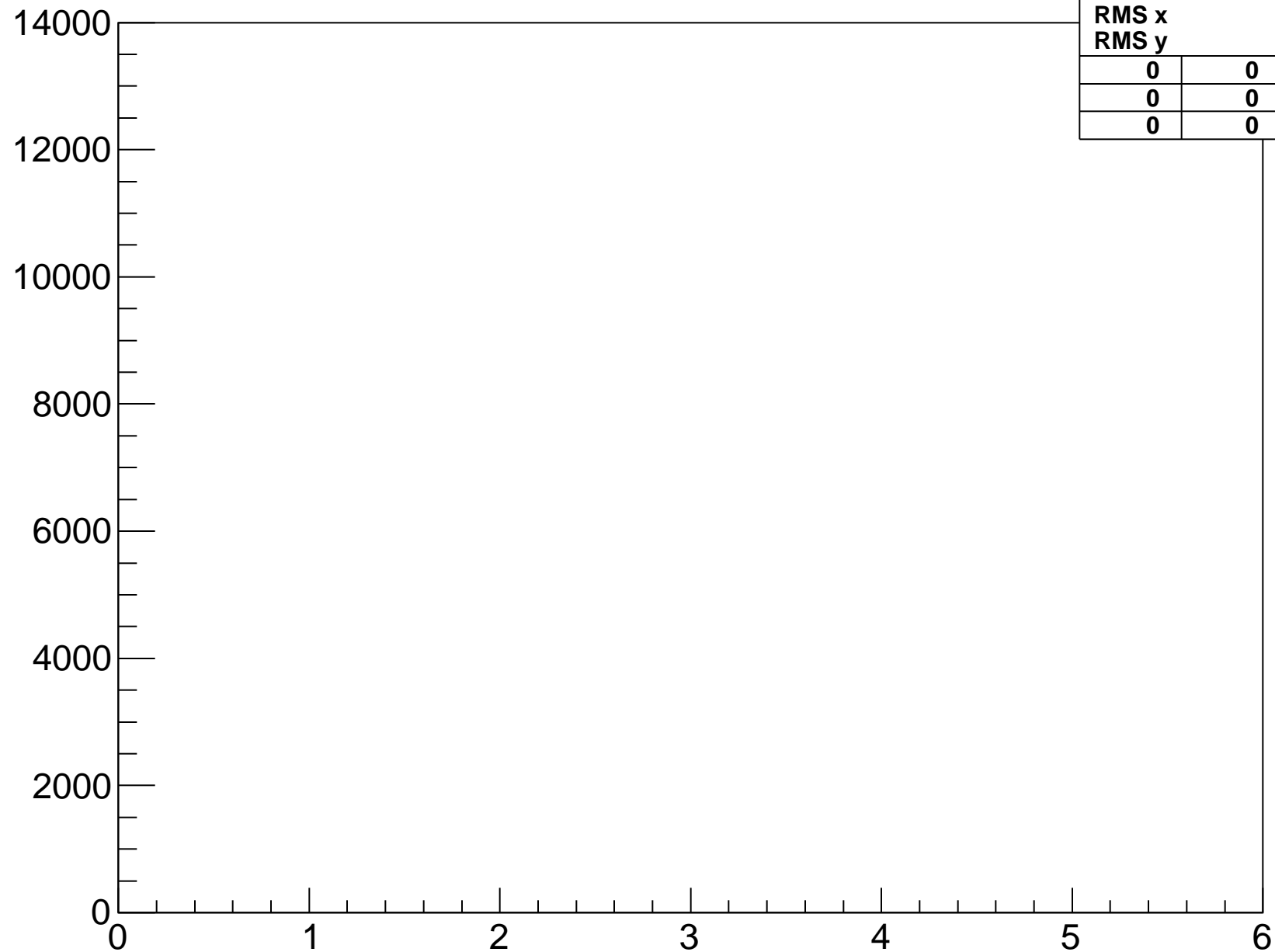
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-2-hyb-3



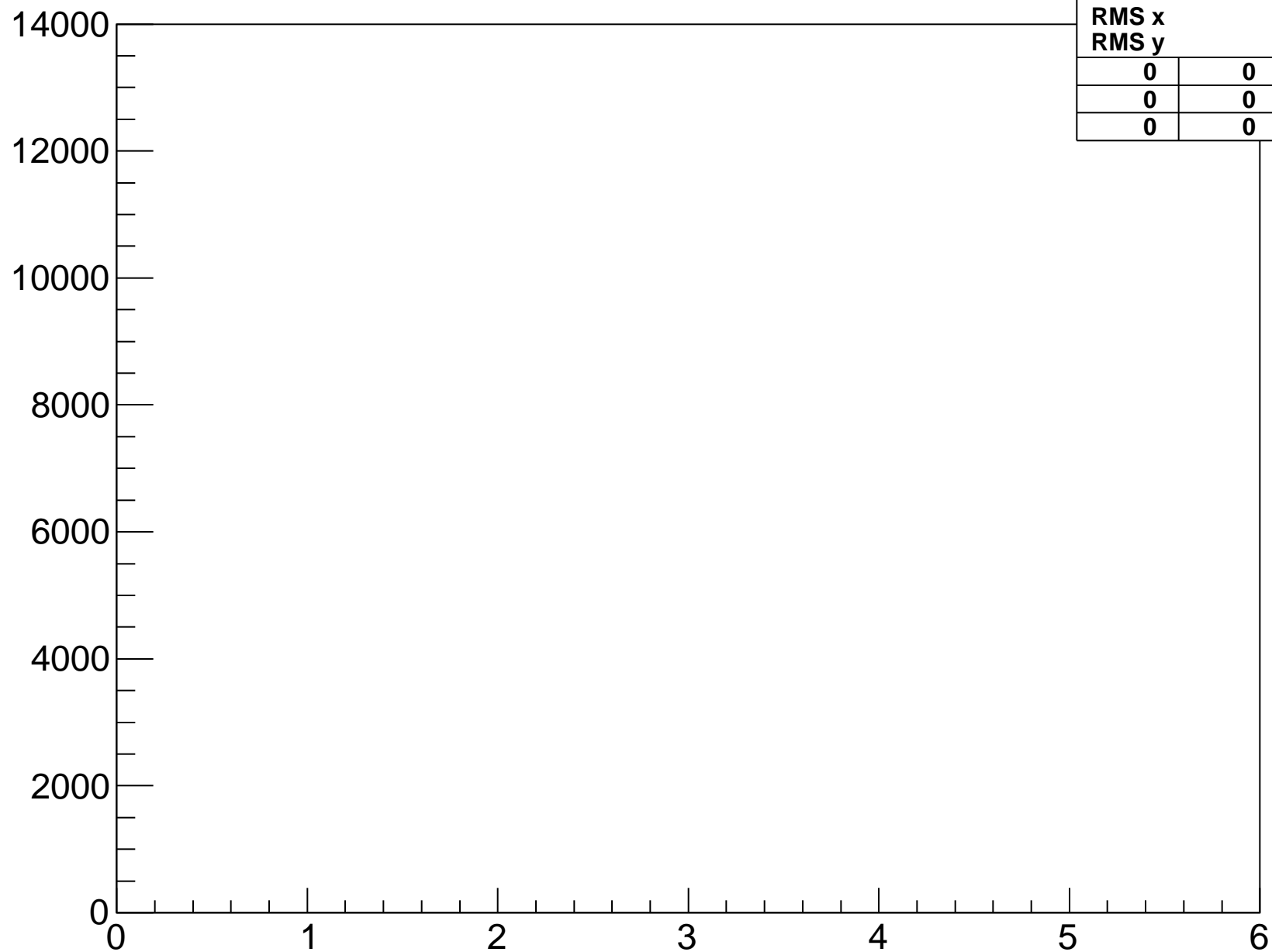
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-3-hyb-0



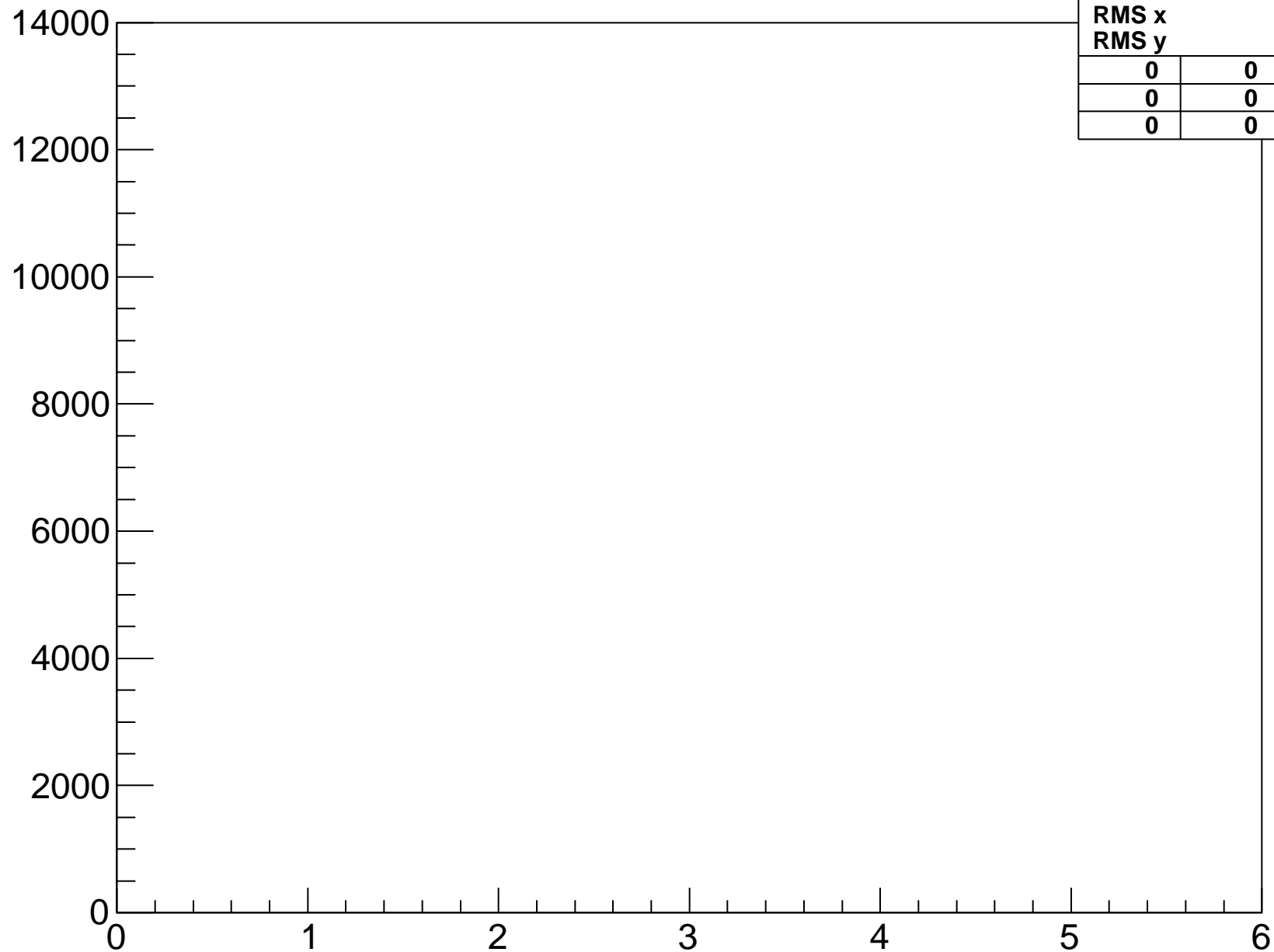
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-3-hyb-1



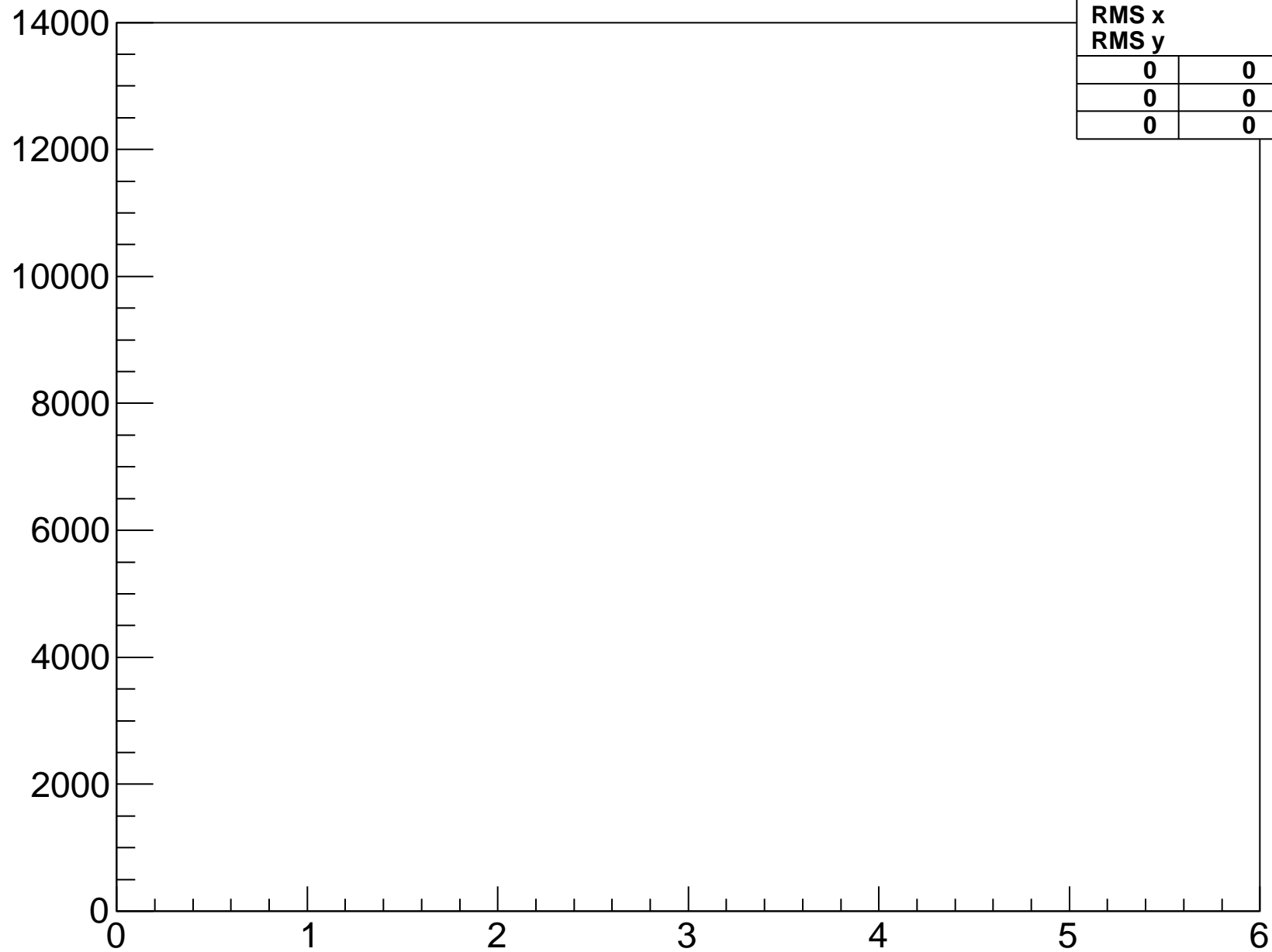
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-3-hyb-2



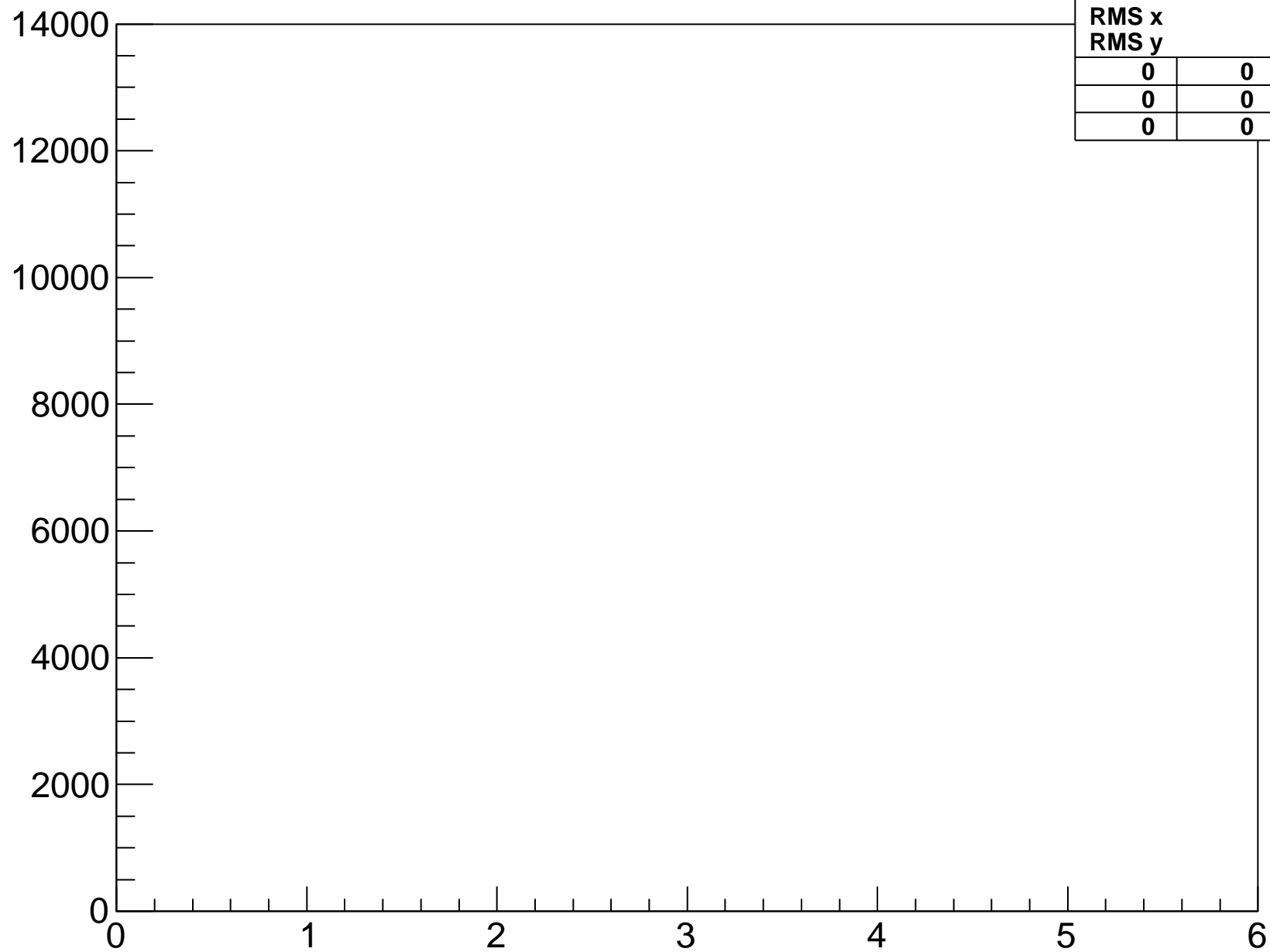
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-3-hyb-3



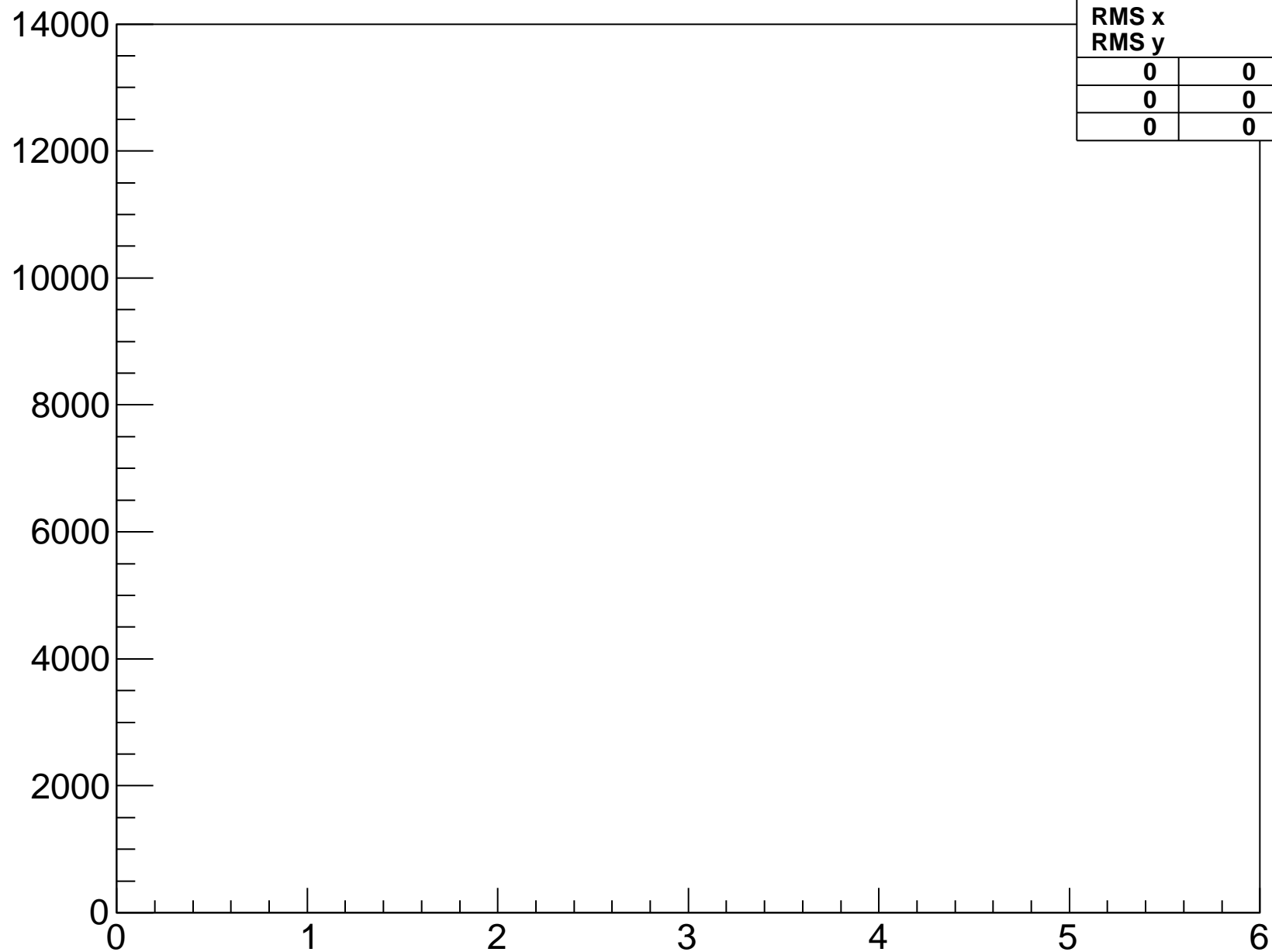
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-4-hyb-0



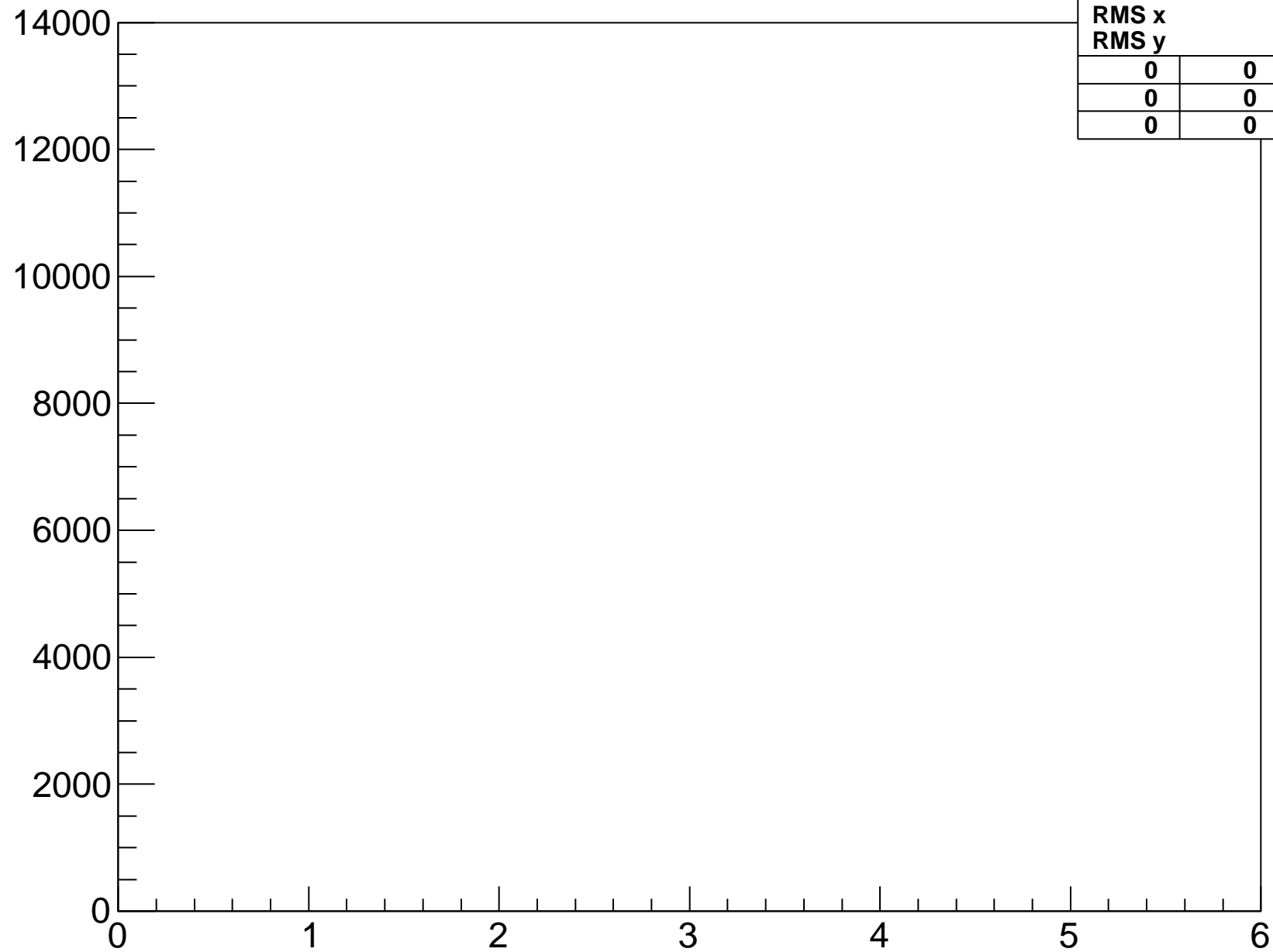
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-4-hyb-1



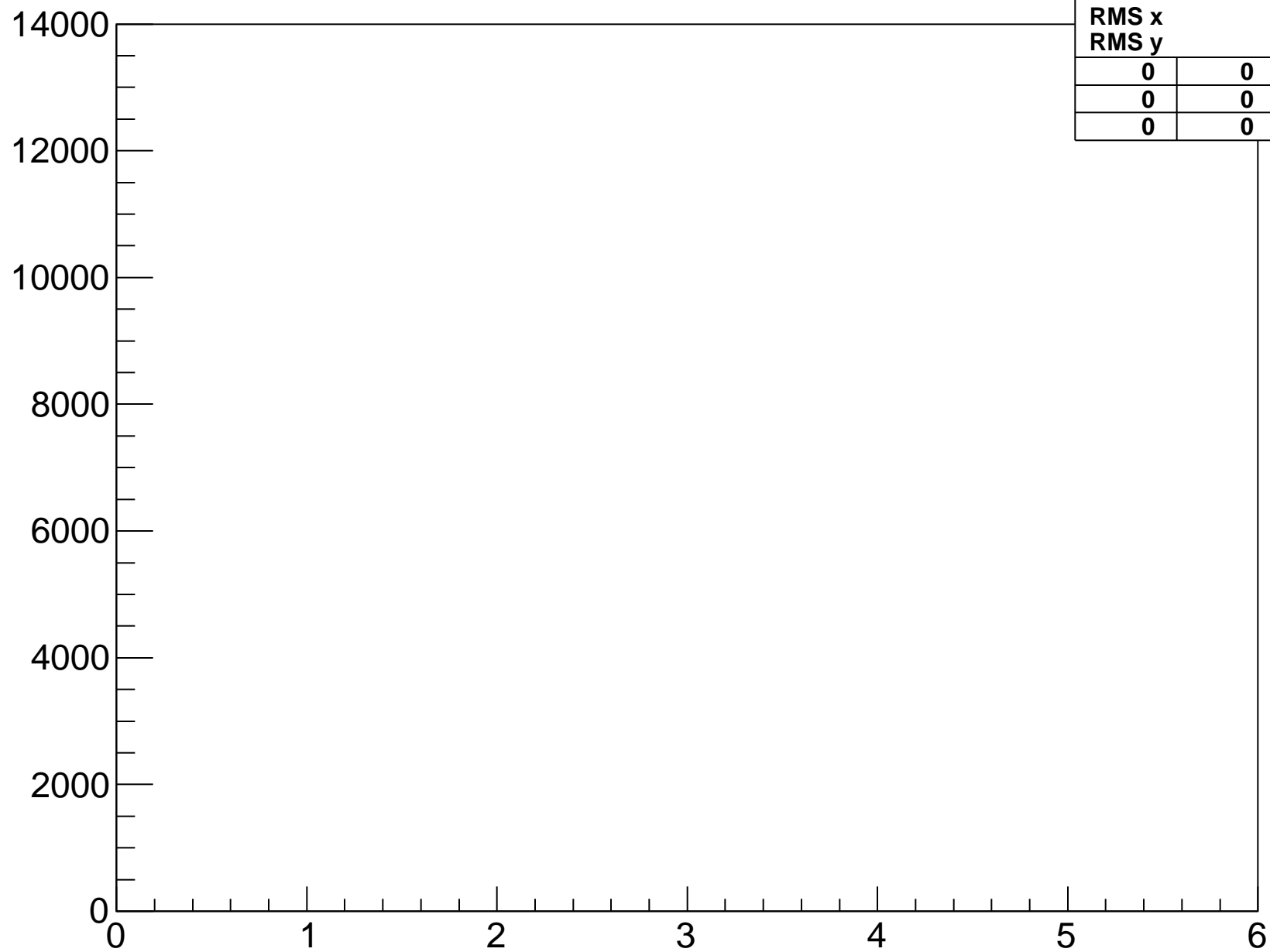
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-4-hyb-2



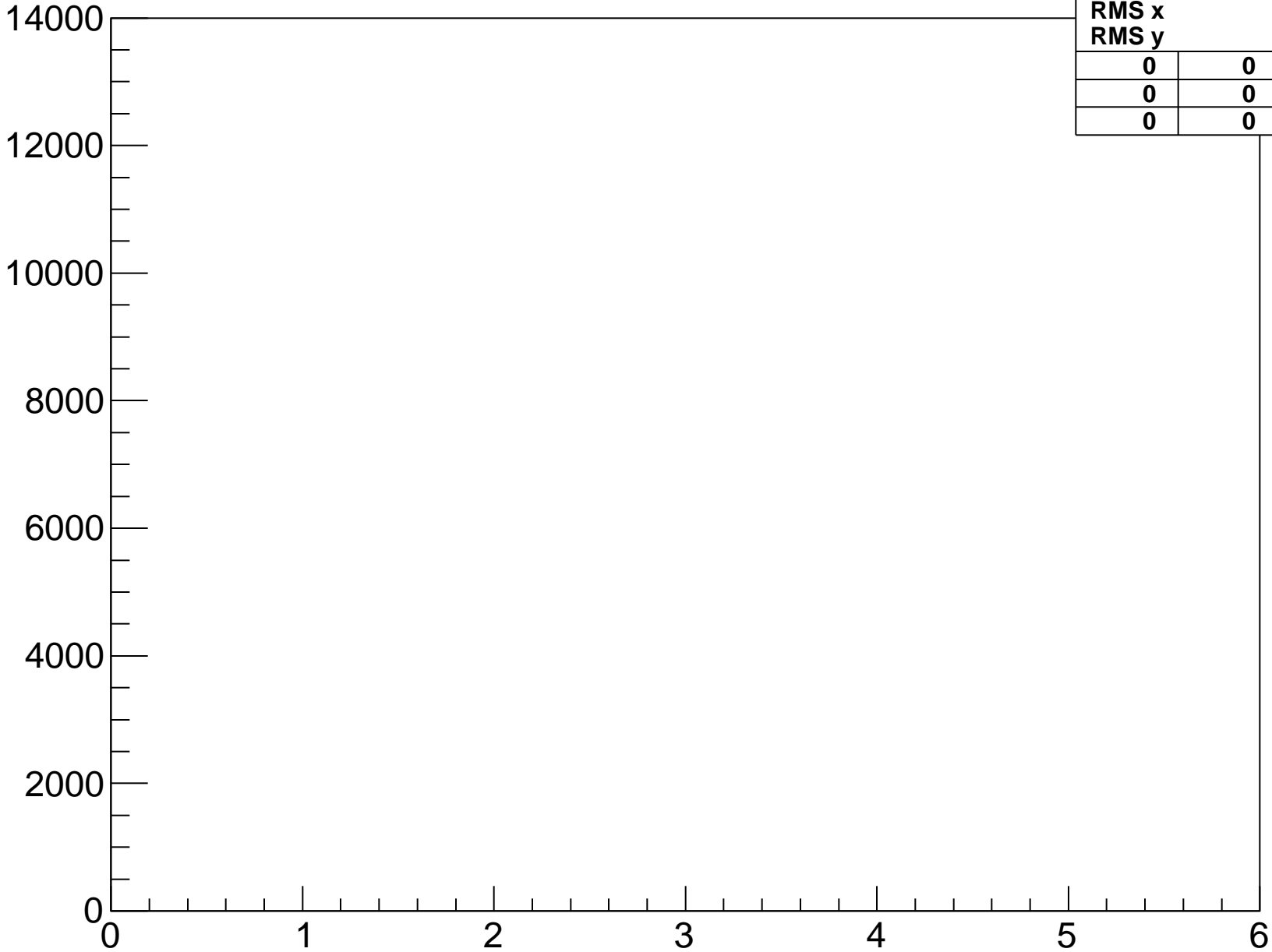
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-4-hyb-3



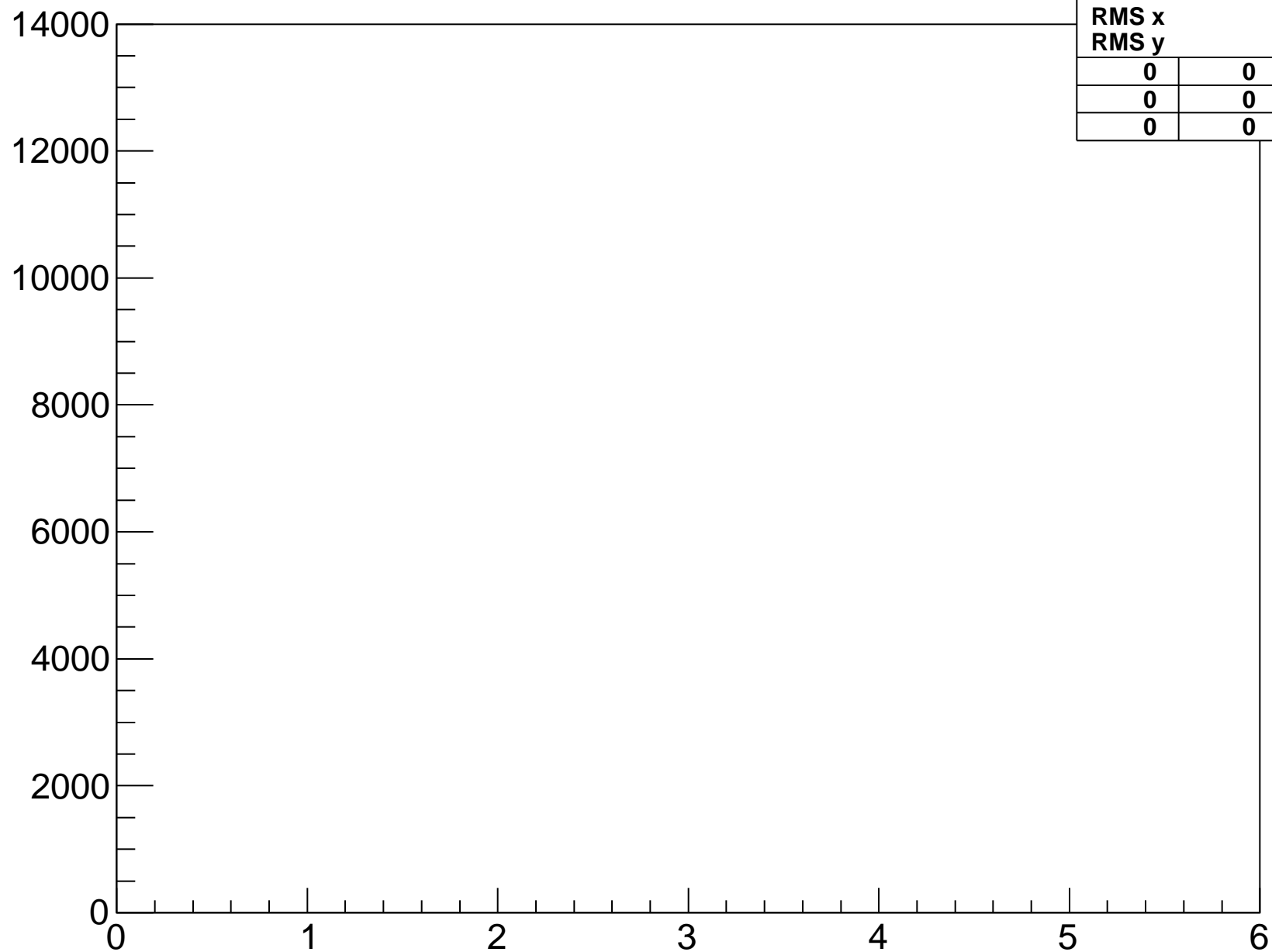
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-5-hyb-0



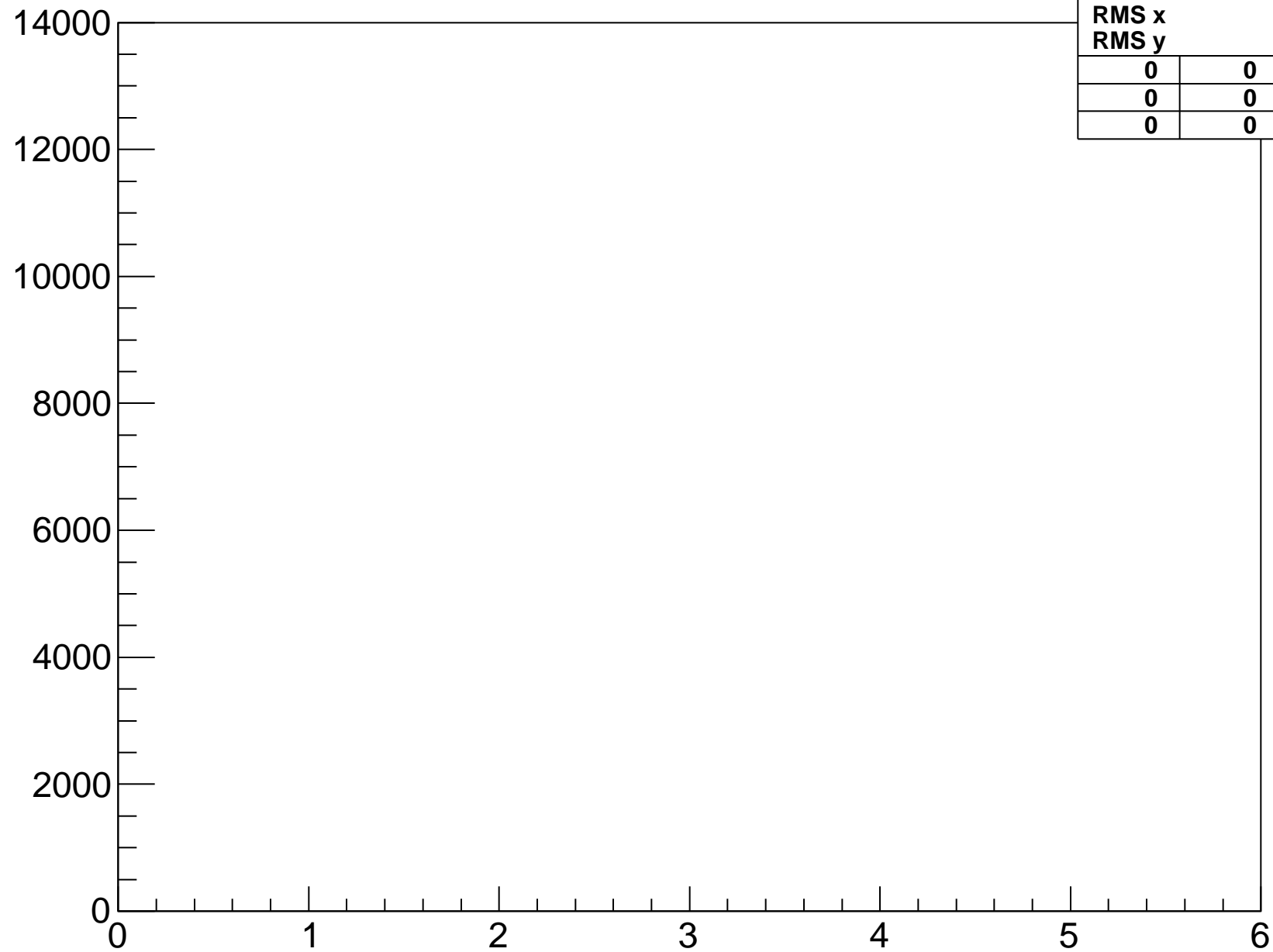
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-5-hyb-1



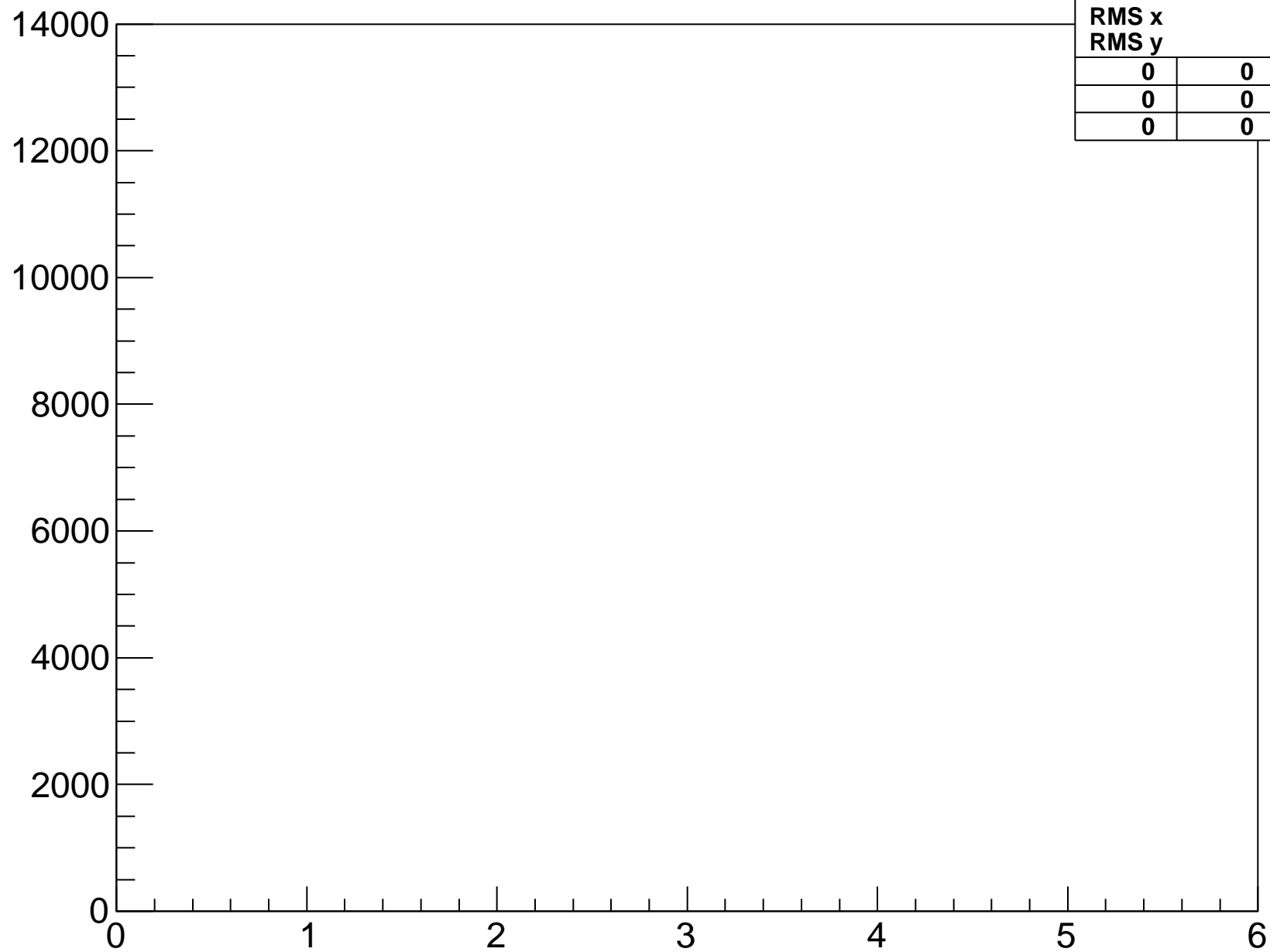
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-5-hyb-2



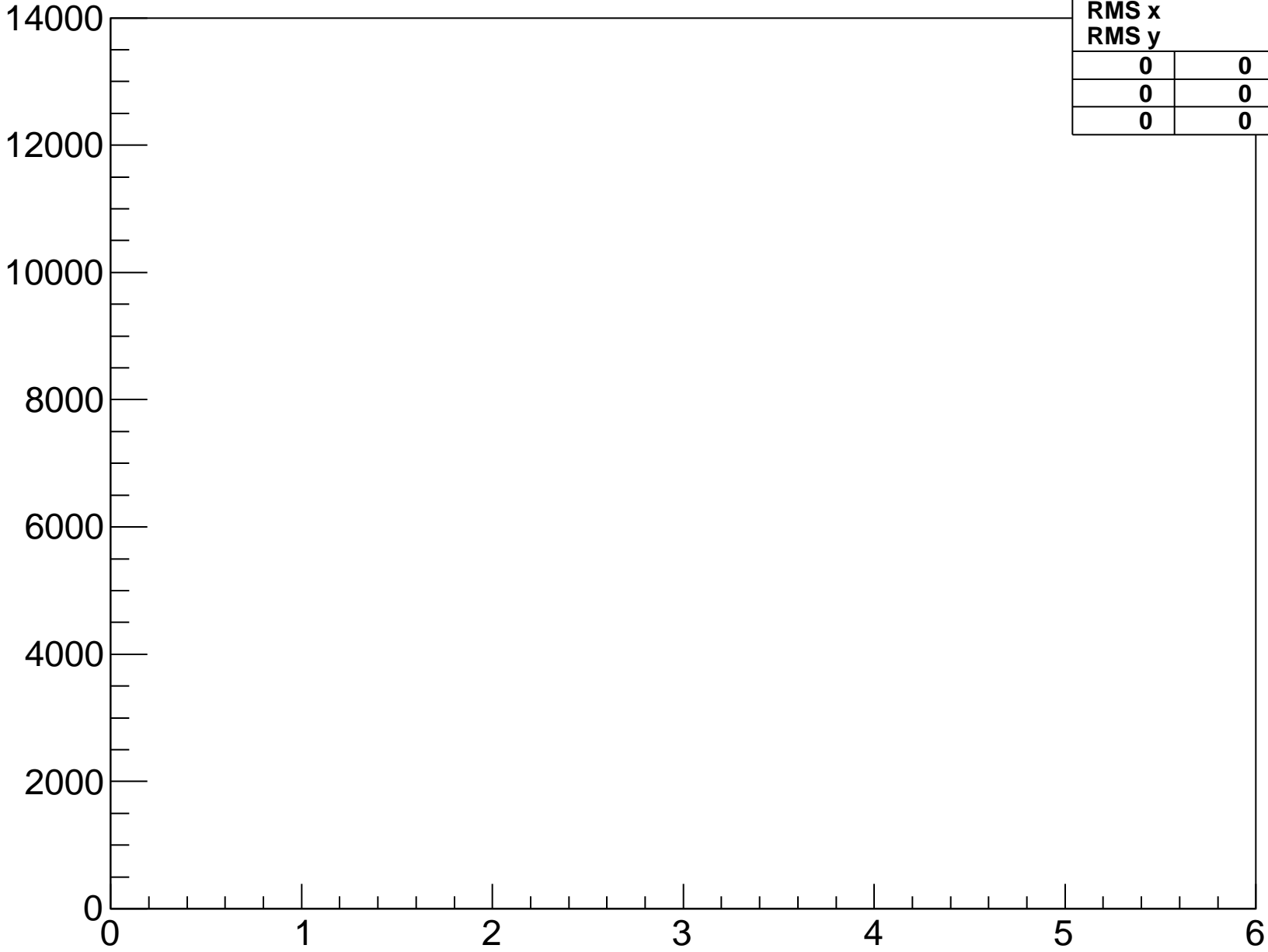
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-5-hyb-3



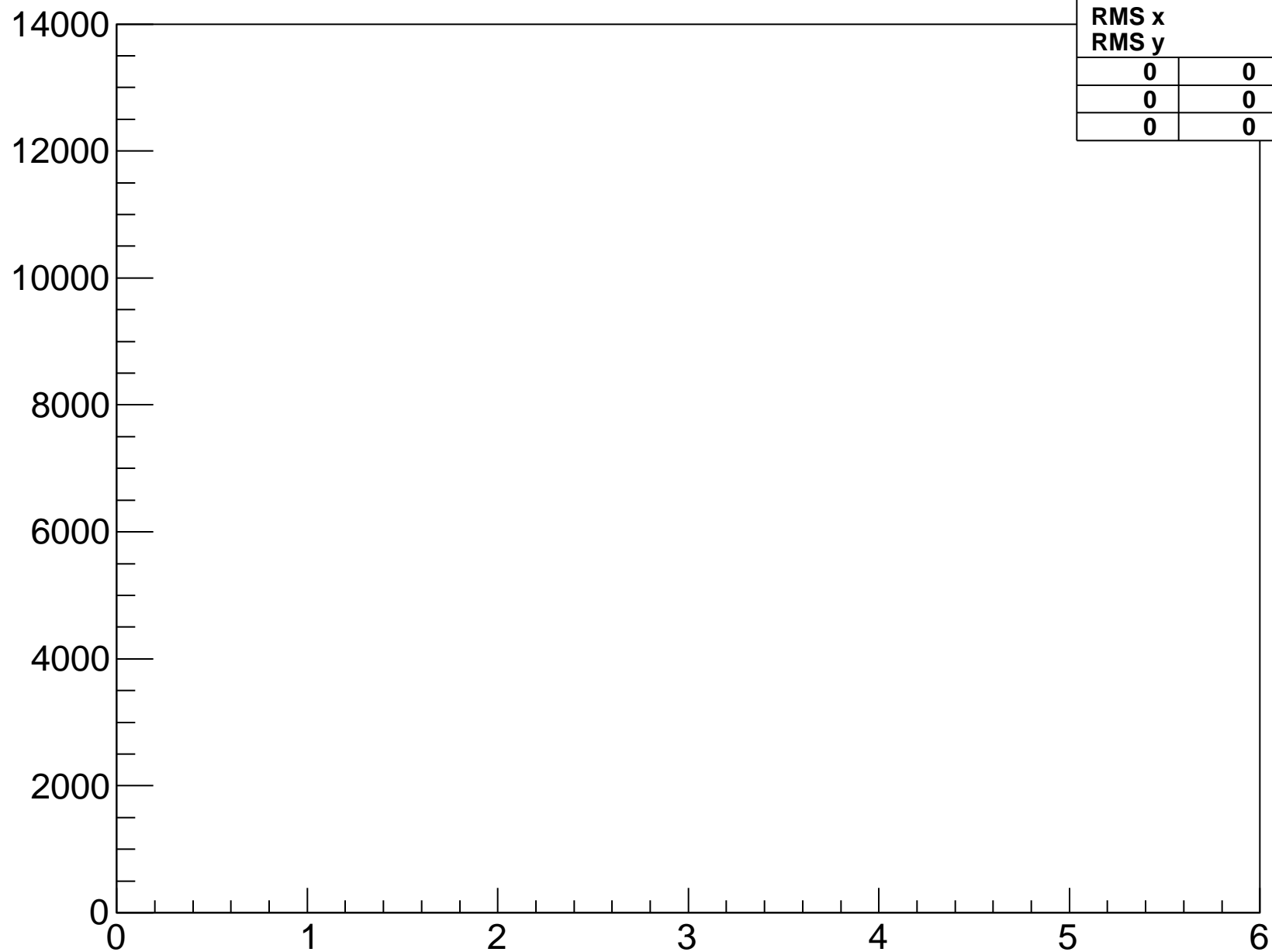
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

samples-fpga-6-hyb-0



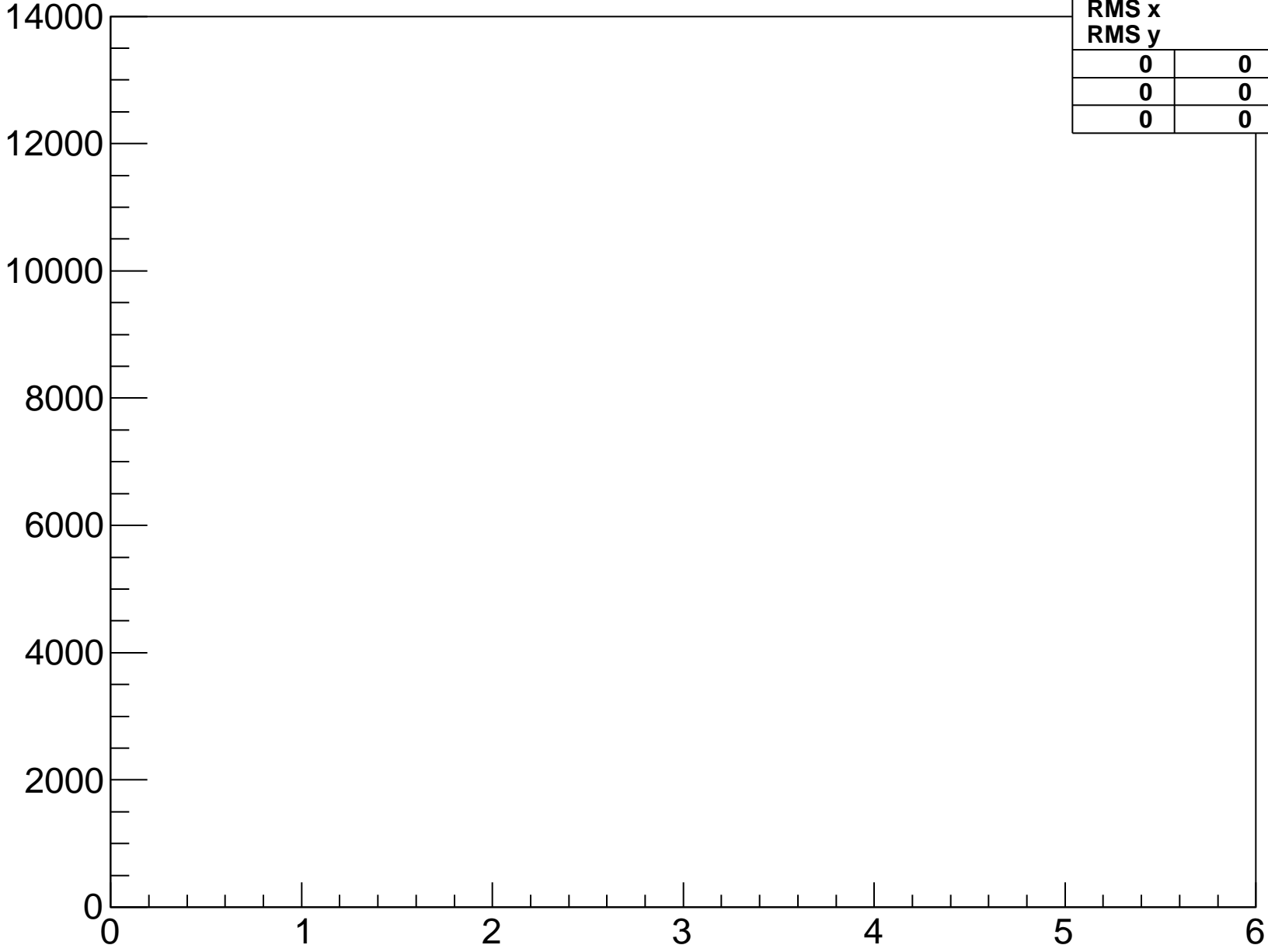
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-6-hyb-1



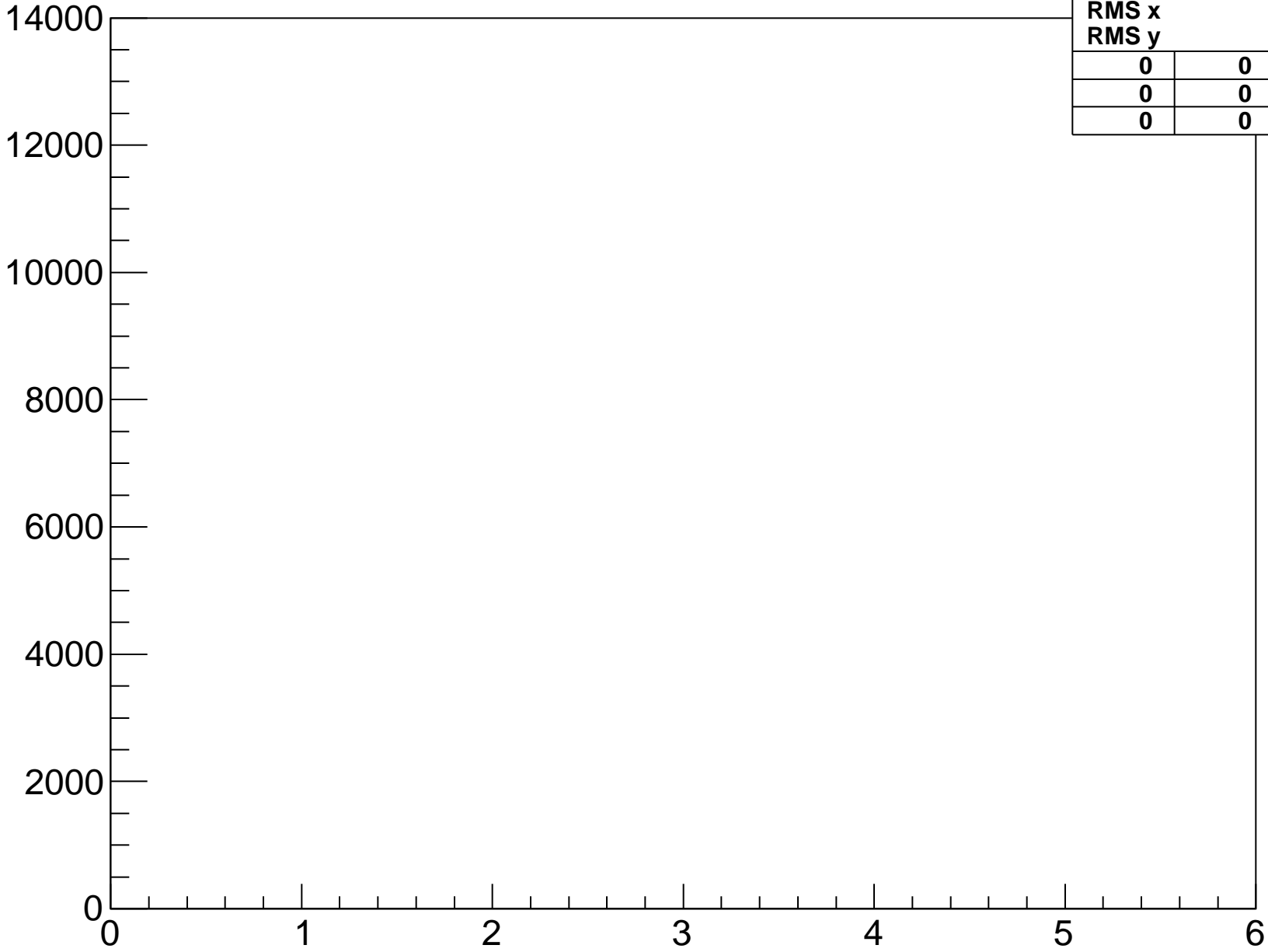
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-6-hyb-2



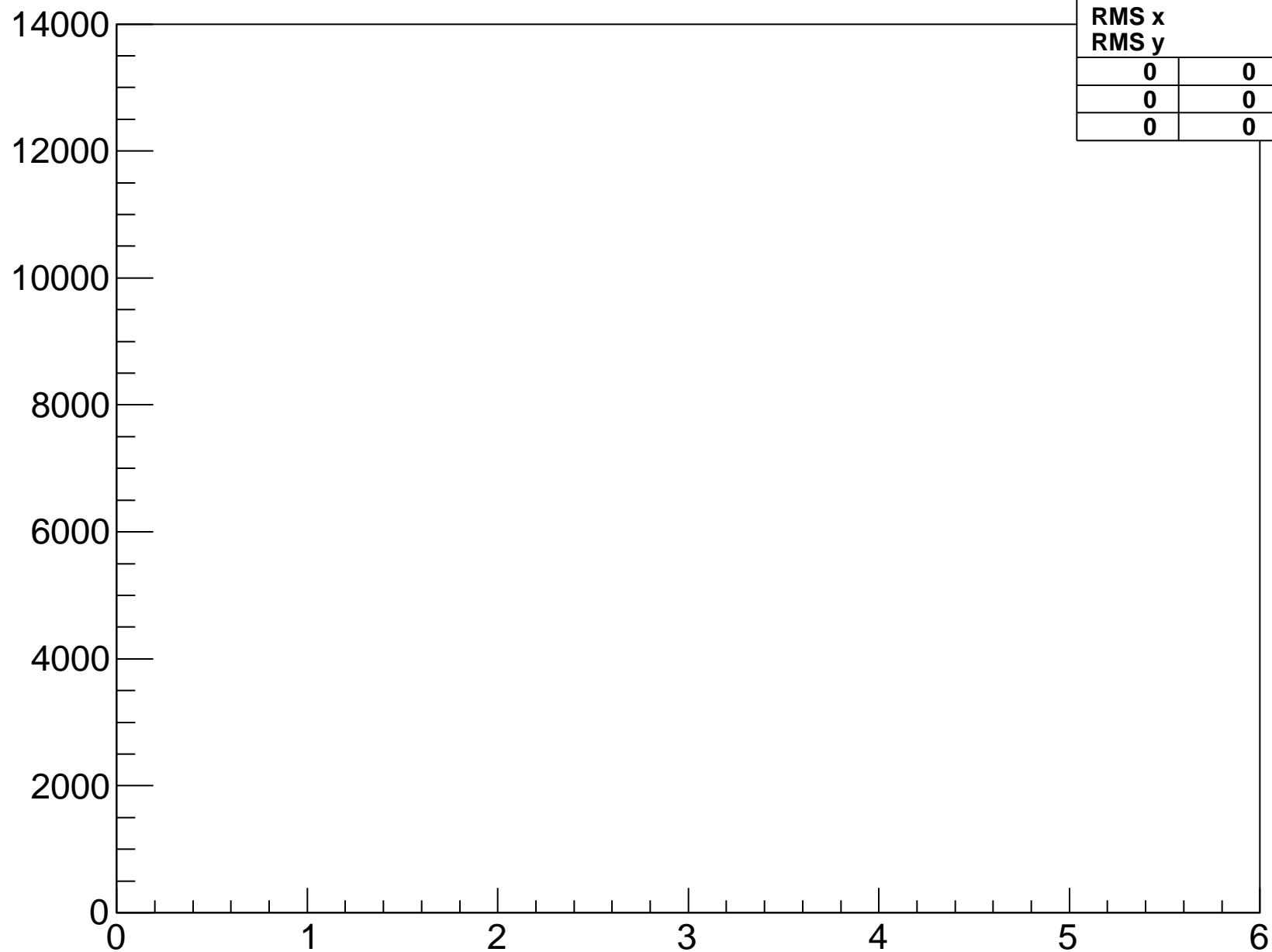
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-6-hyb-3



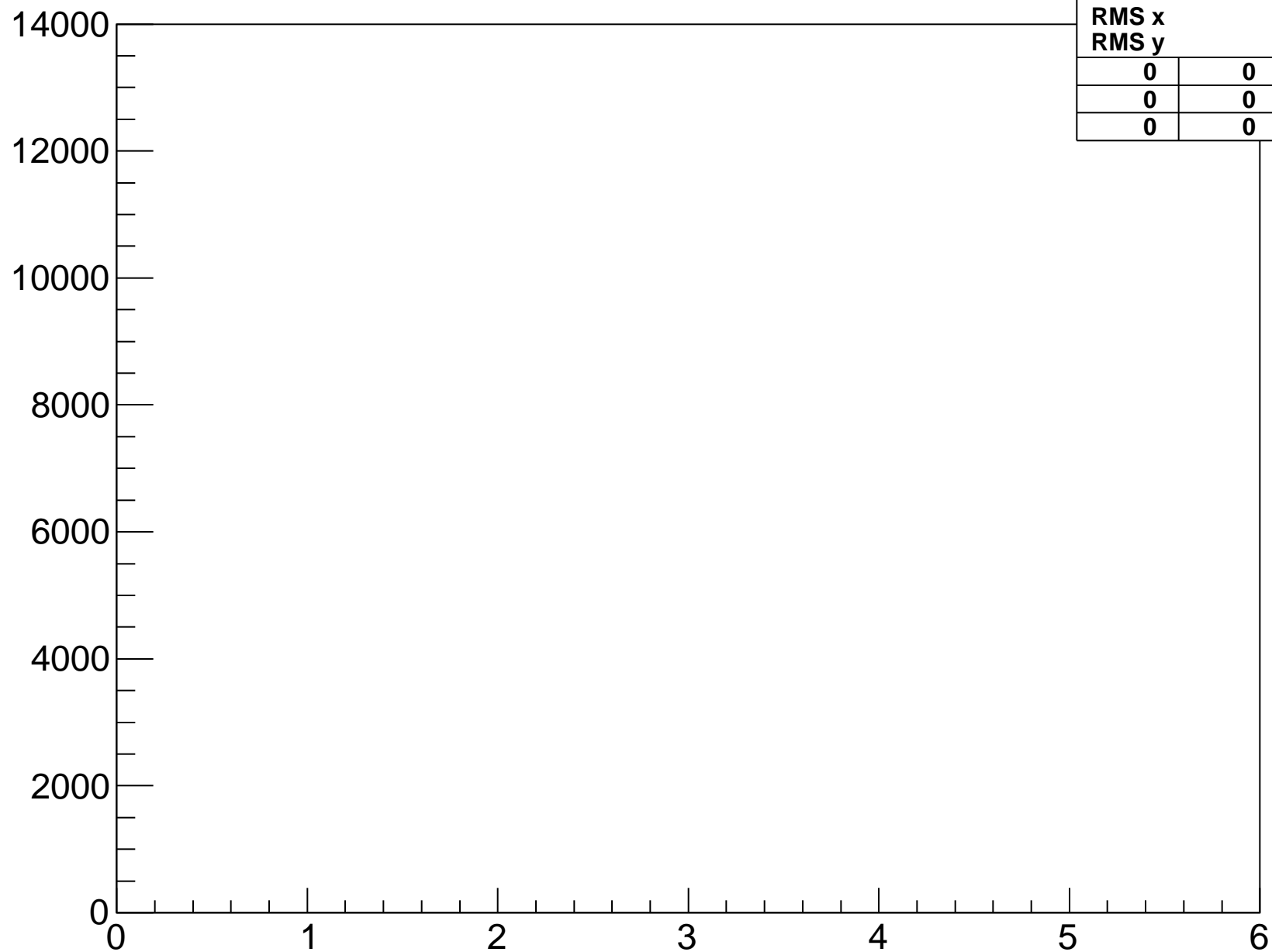
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-7-hyb-0



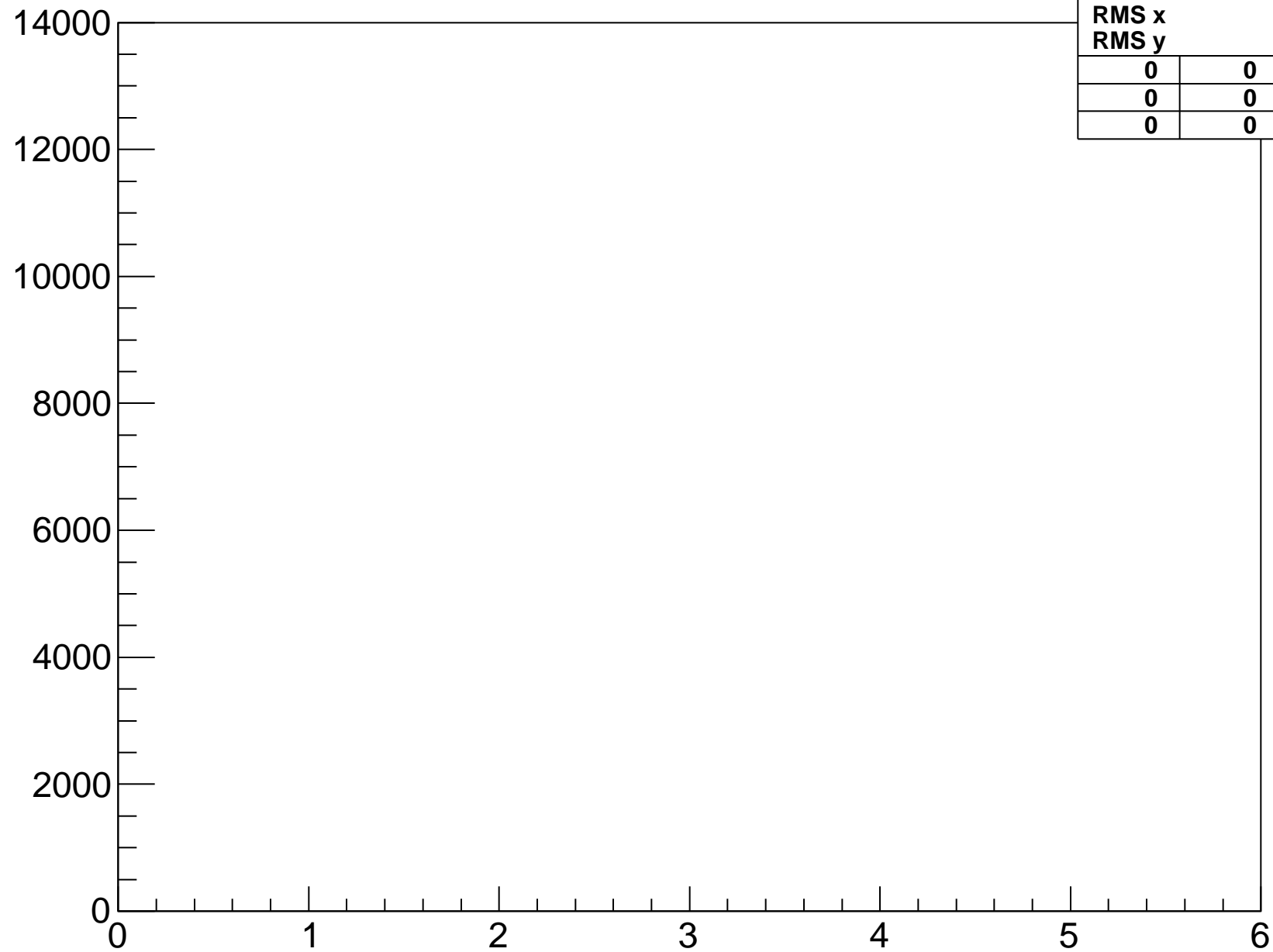
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-7-hyb-1



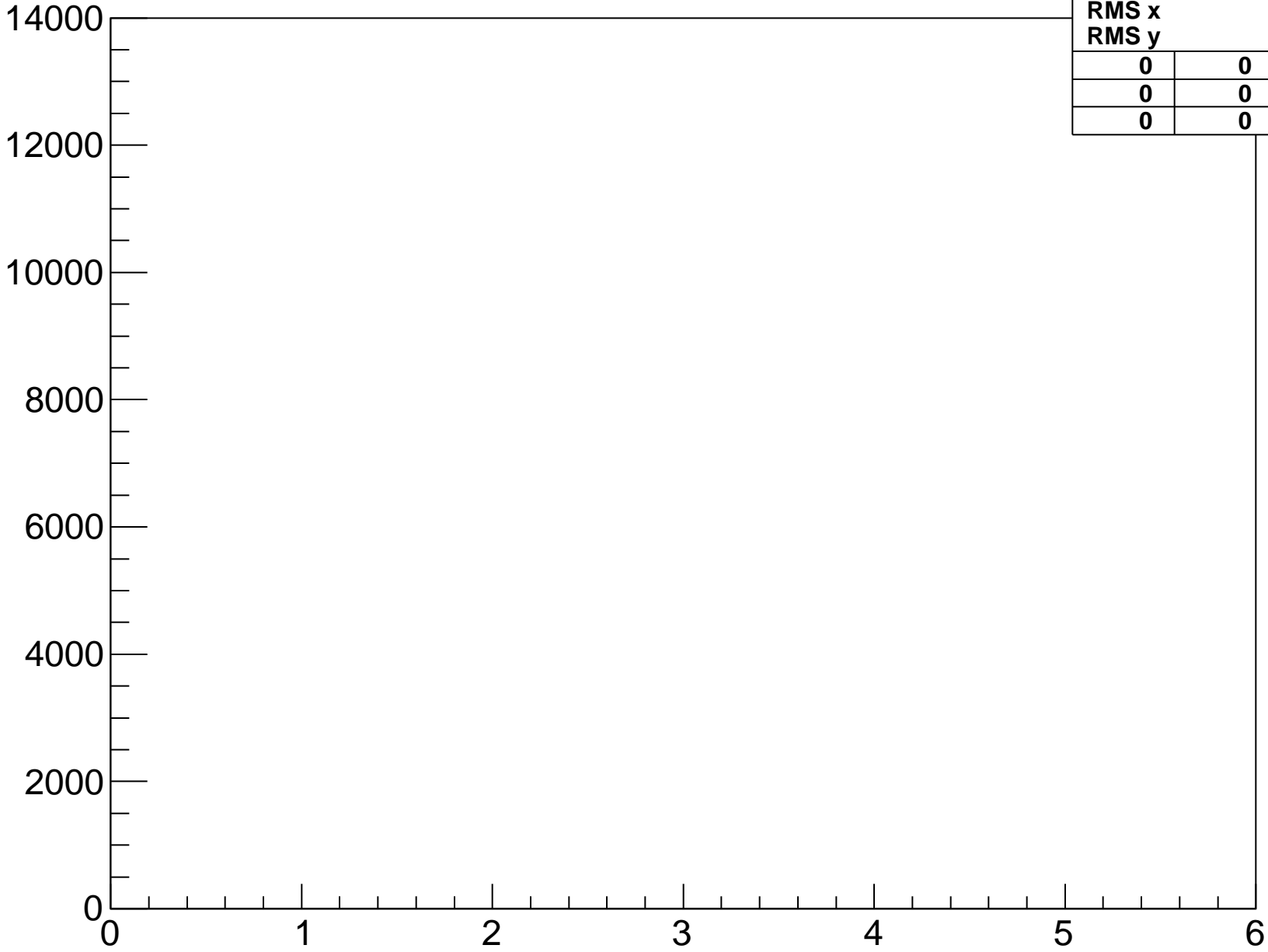
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-7-hyb-2



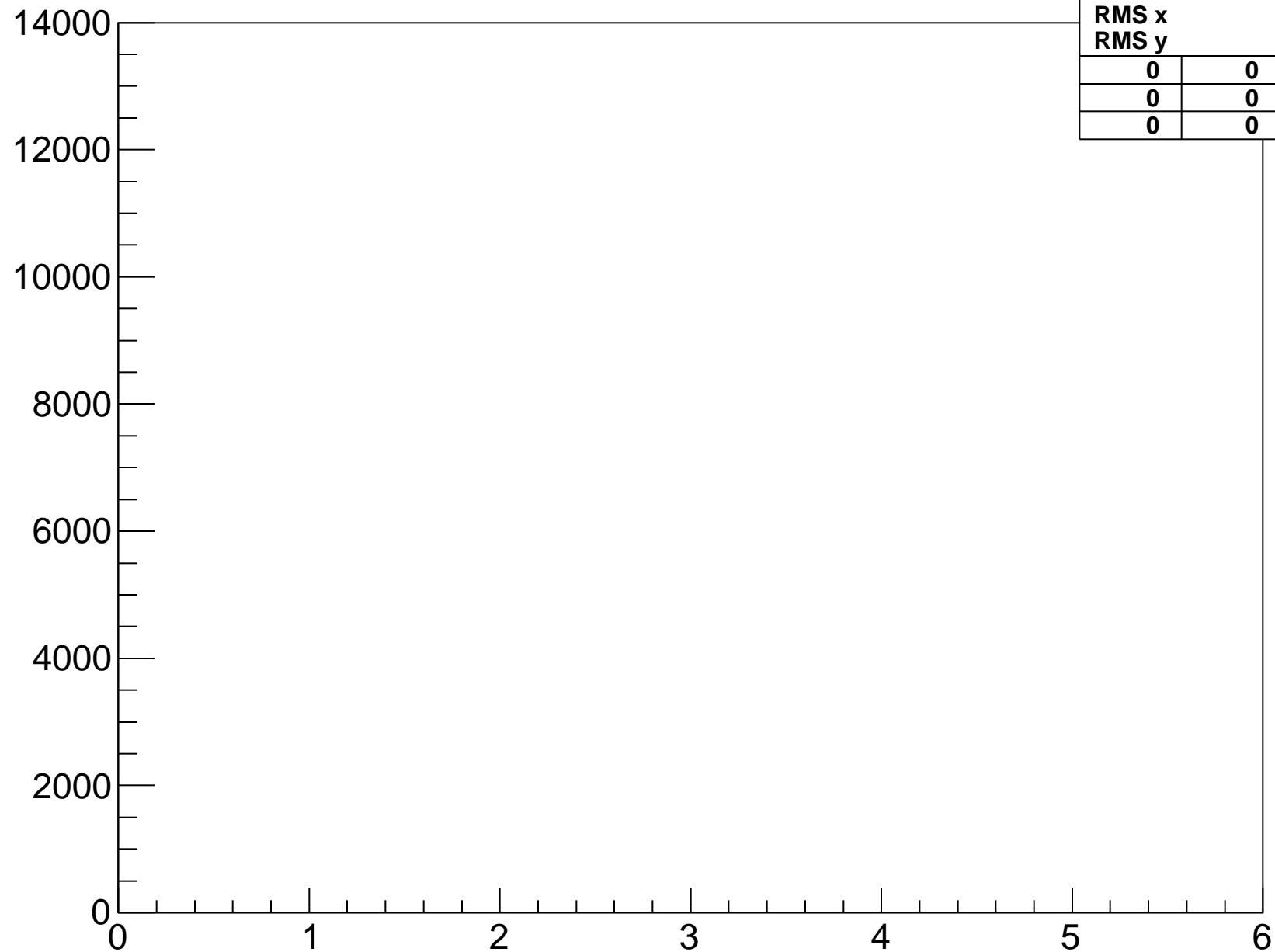
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-7-hyb-3



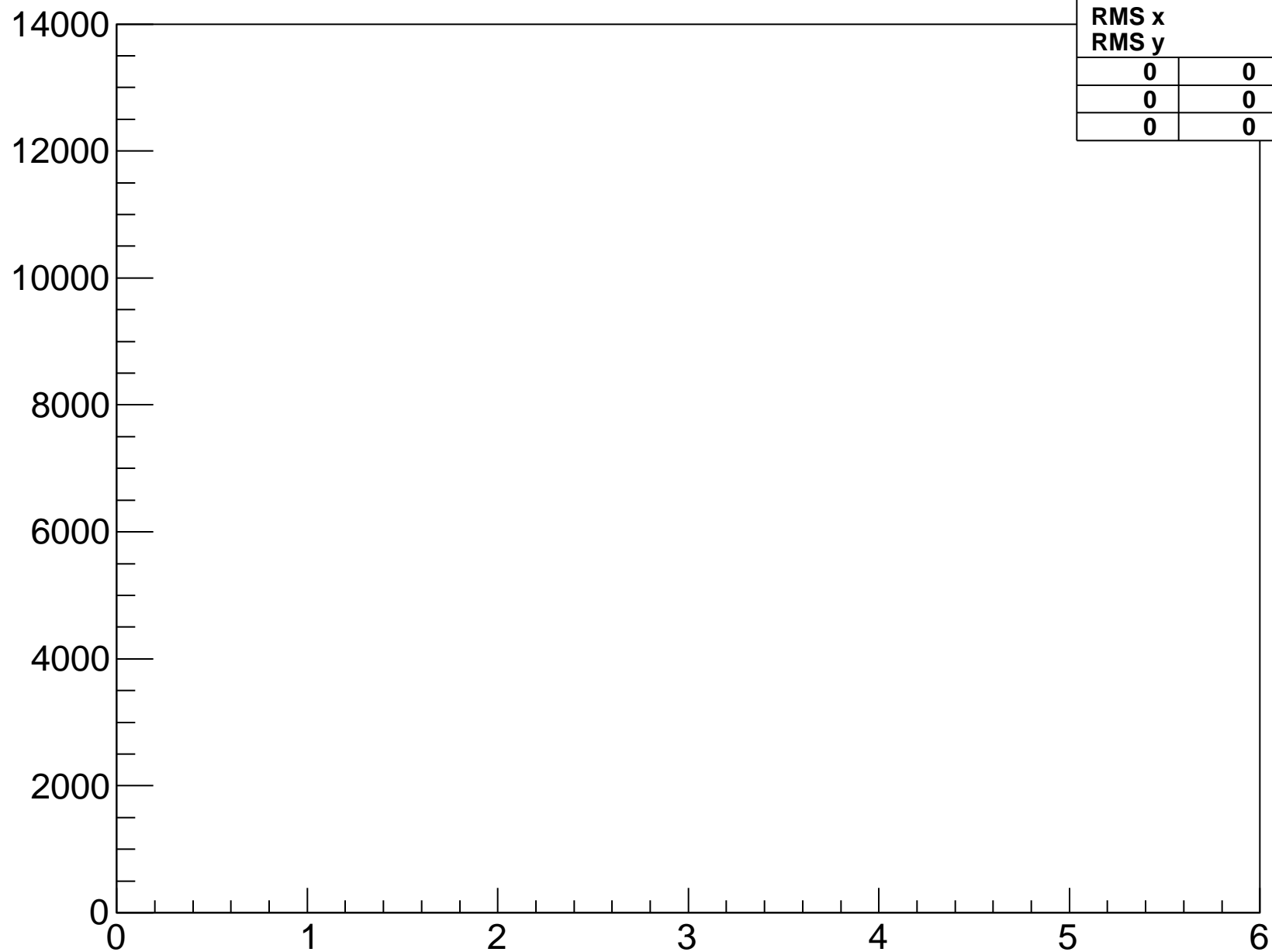
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-8-hyb-0



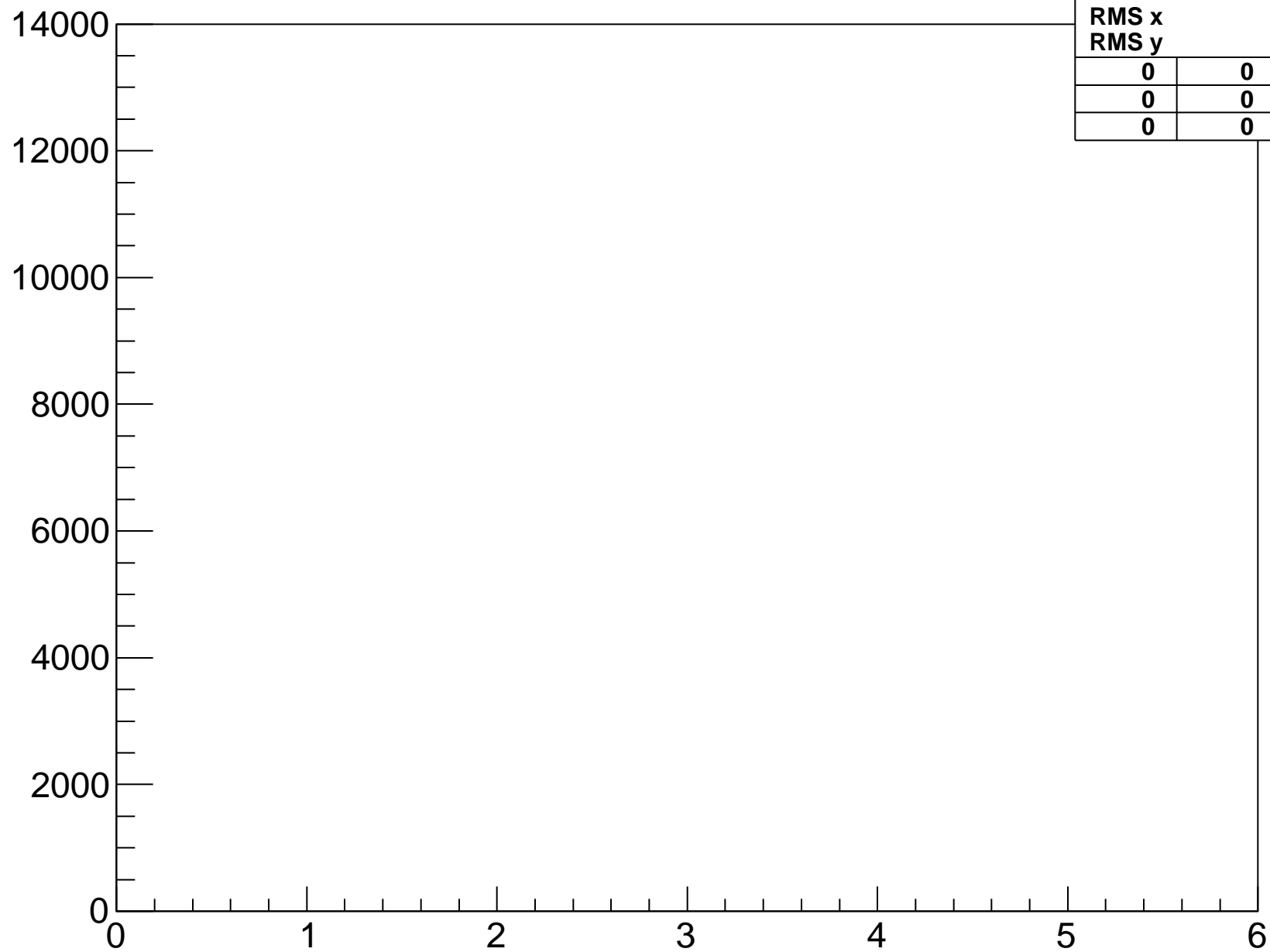
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-8-hyb-1



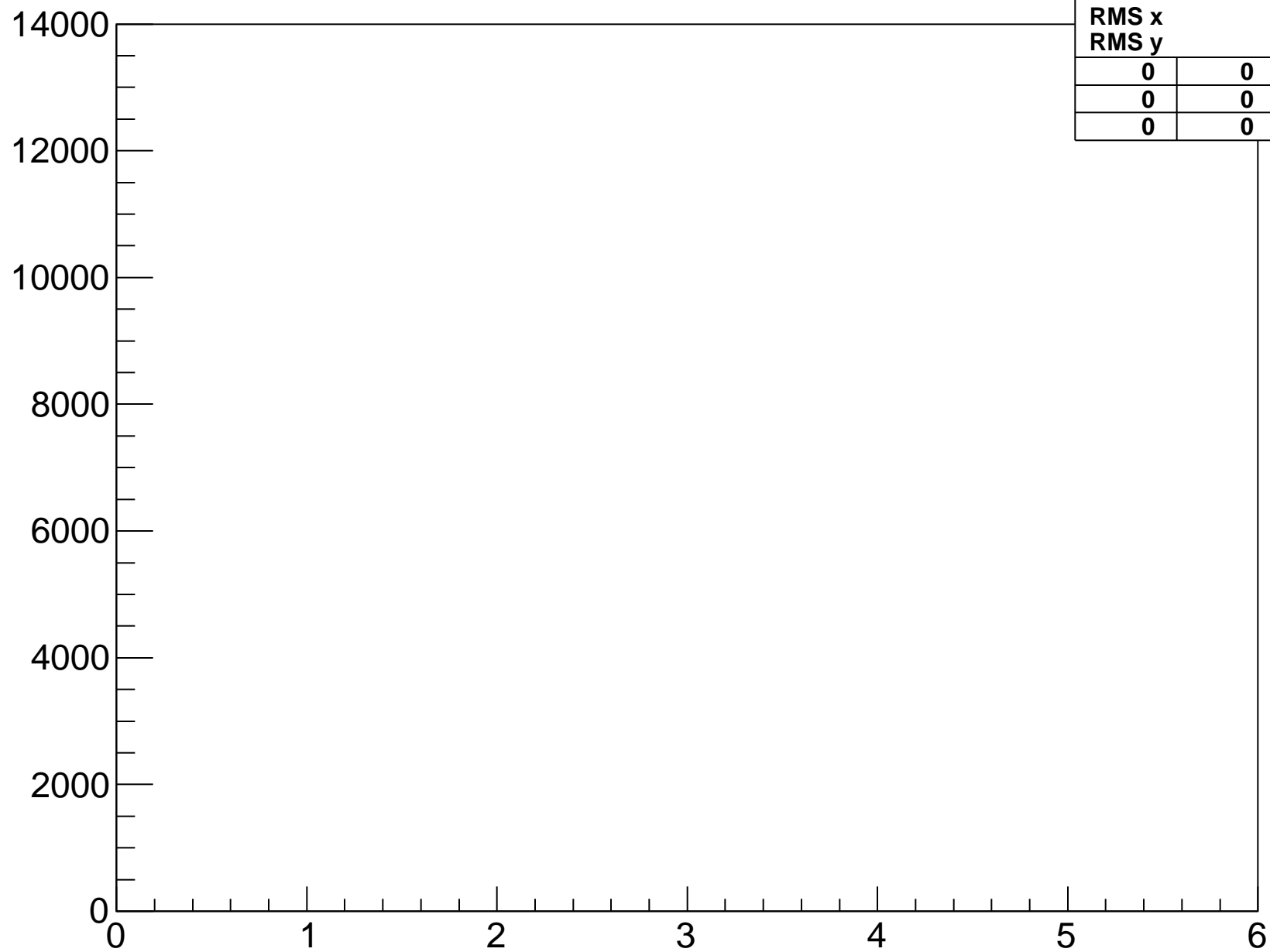
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-8-hyb-2



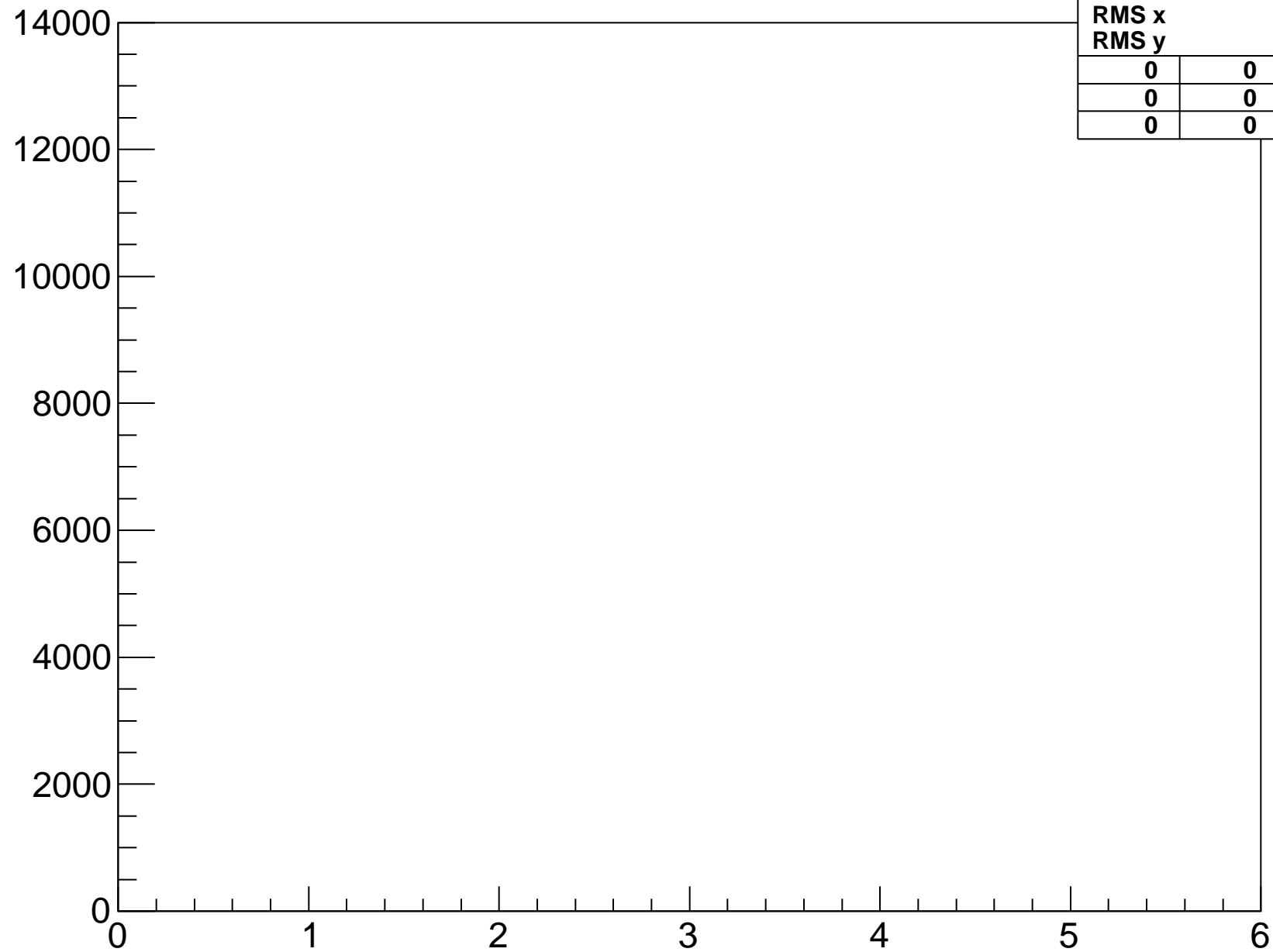
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

samples-fpga-8-hyb-3



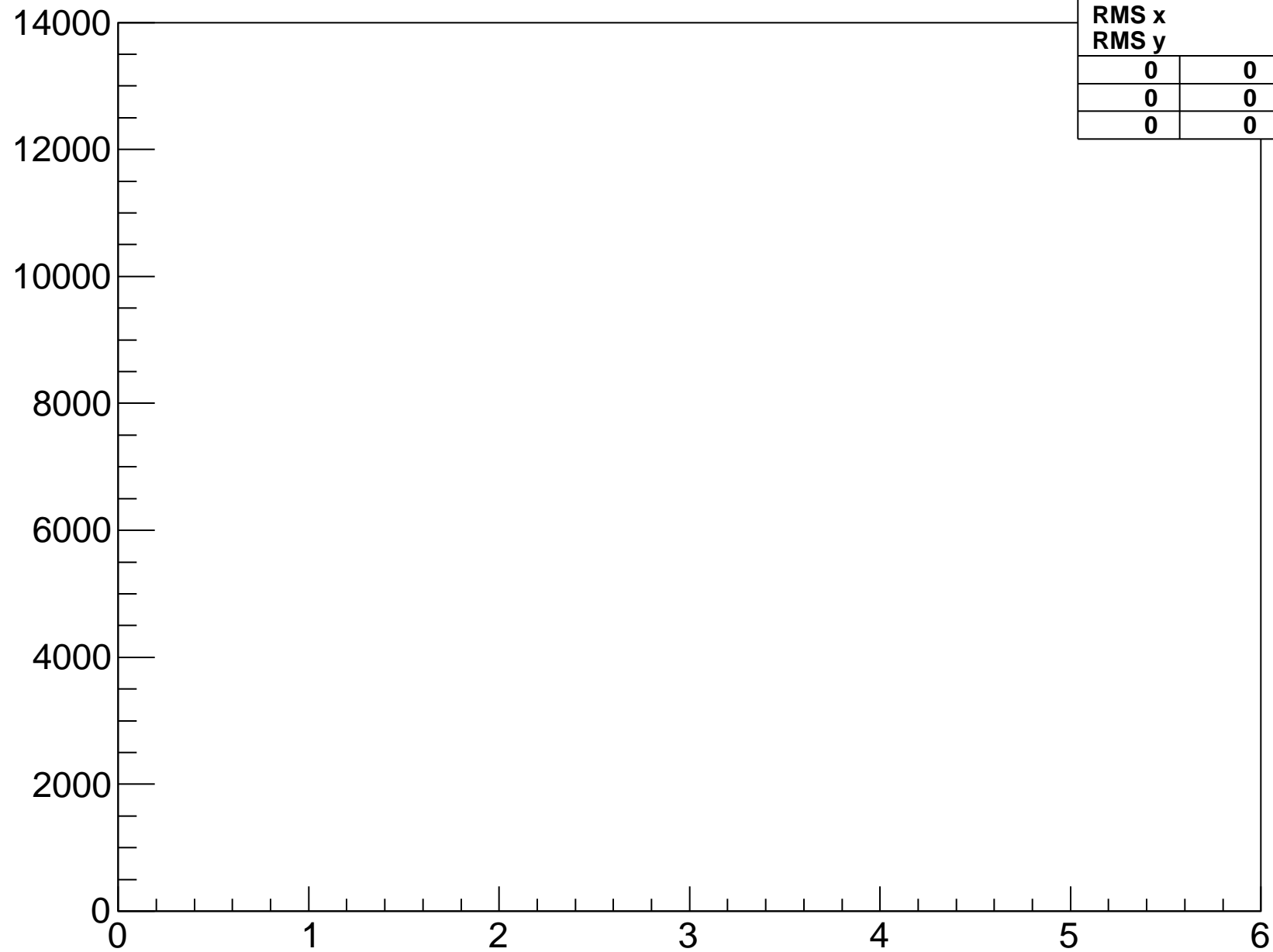
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

samples-fpga-9-hyb-0



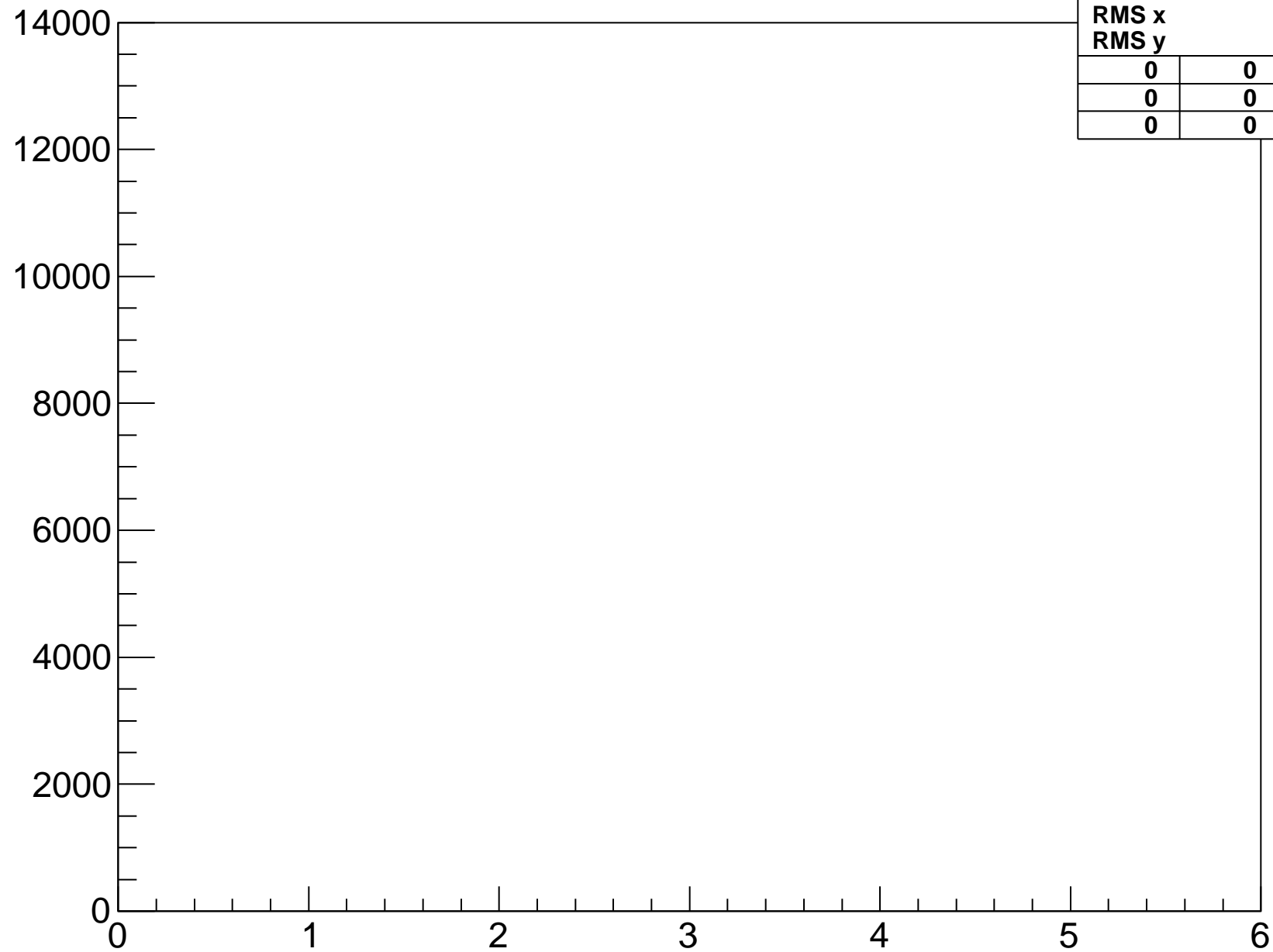
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

samples-fpga-9-hyb-1



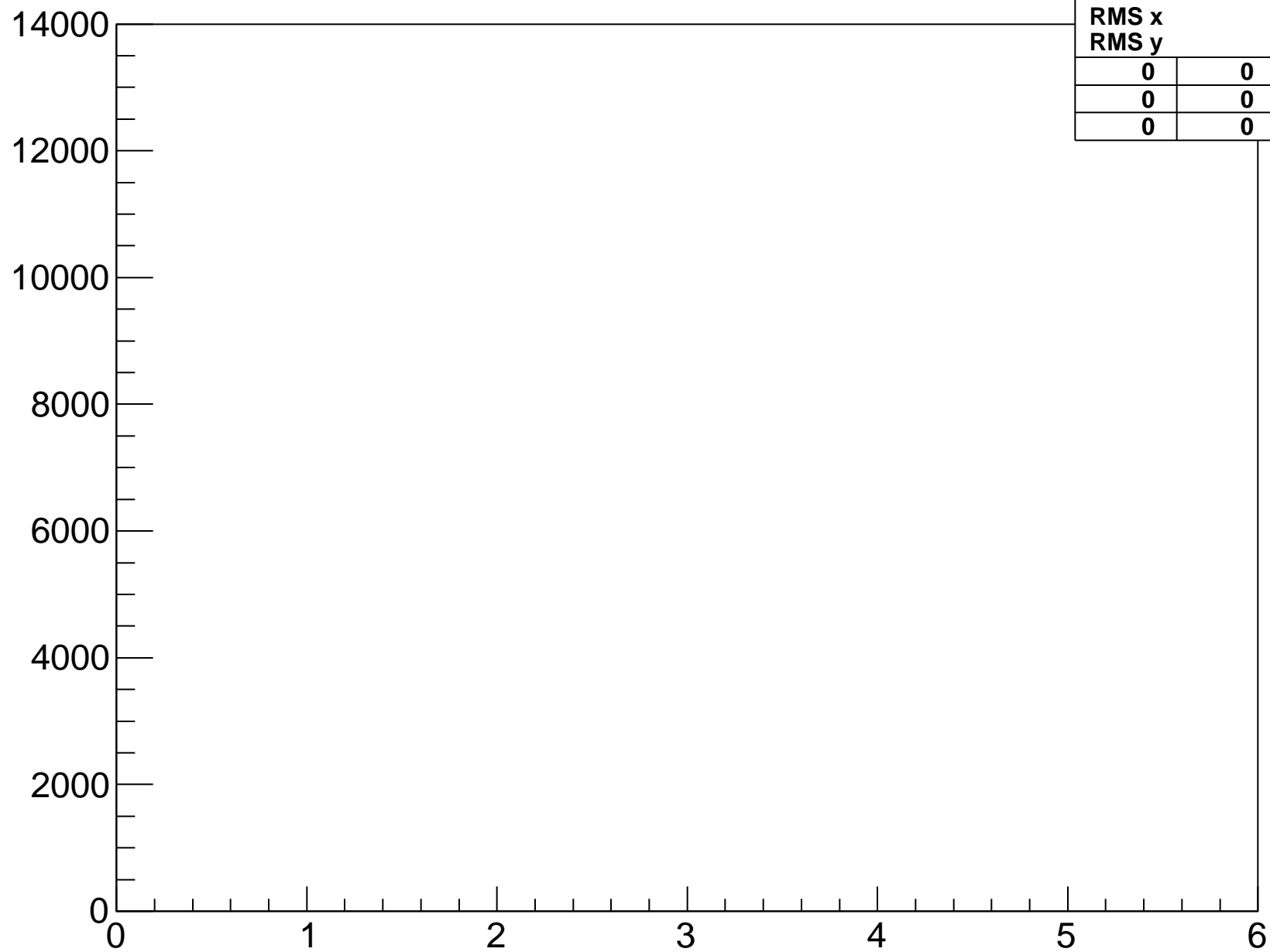
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

samples-fpga-9-hyb-2



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

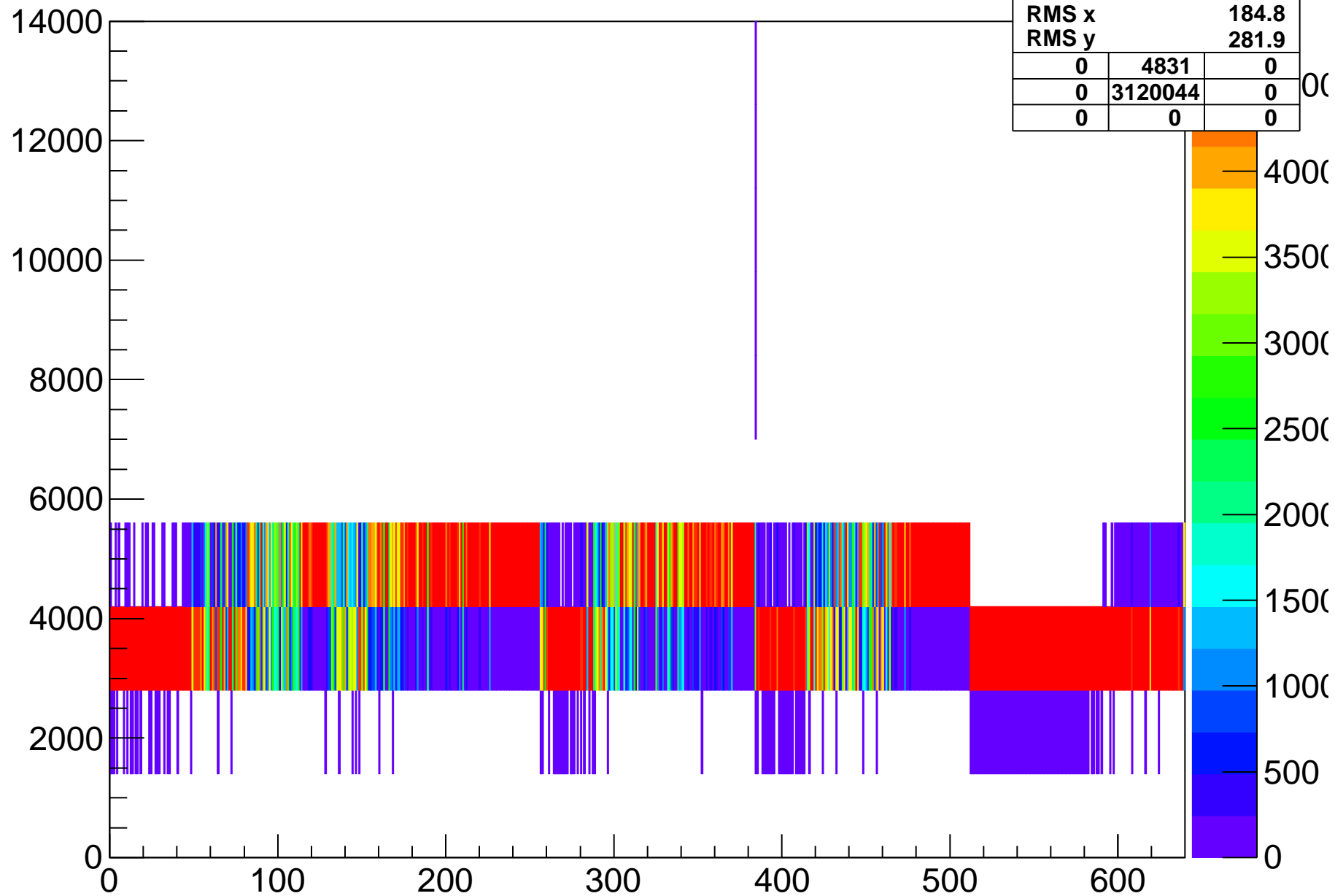
samples-fpga-9-hyb-3



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

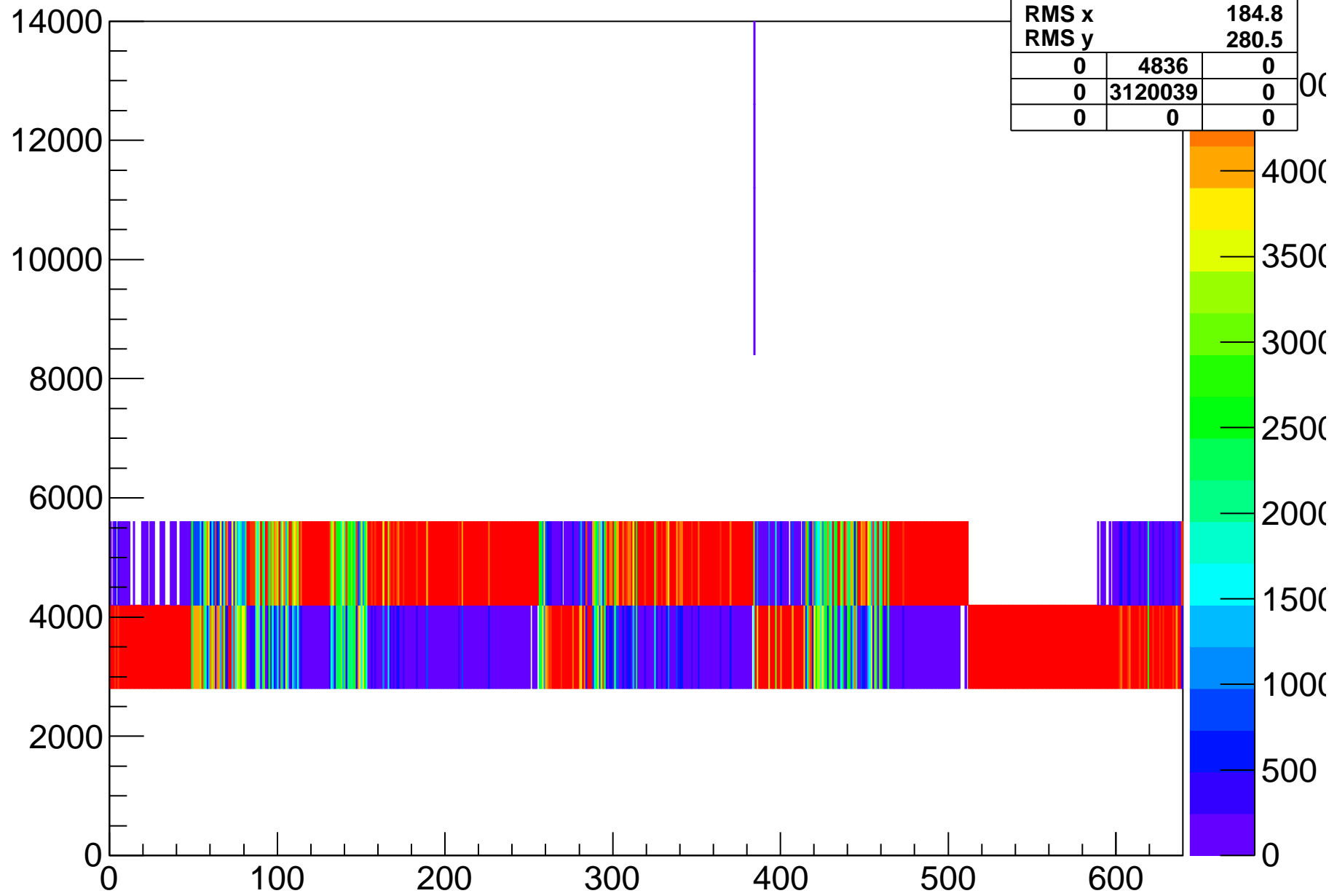
baselinesamples-fpga-0-hyb-0-sample-0

Entries	3124875	
Mean x	319.5	
Mean y	4149	
RMS x	184.8	
RMS y	281.9	
0	4831	0
0	3120044	0
0	0	0



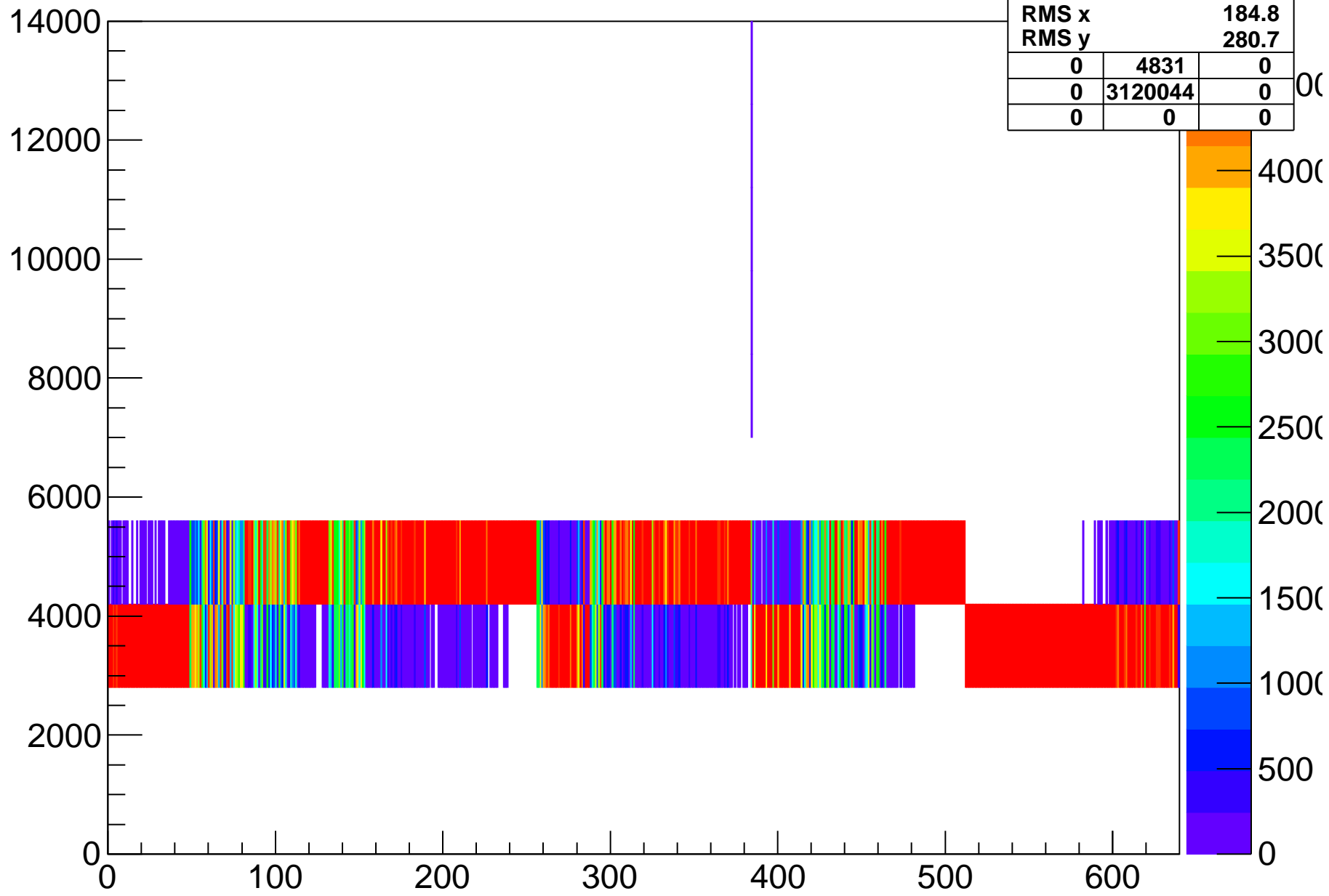
baselinesamples-fpga-0-hyb-0-sample-1

Entries			3124875
Mean x			319.5
Mean y			4187
RMS x			184.8
RMS y			280.5
0	4836	0	0
0	3120039	0	0
0	0	0	0



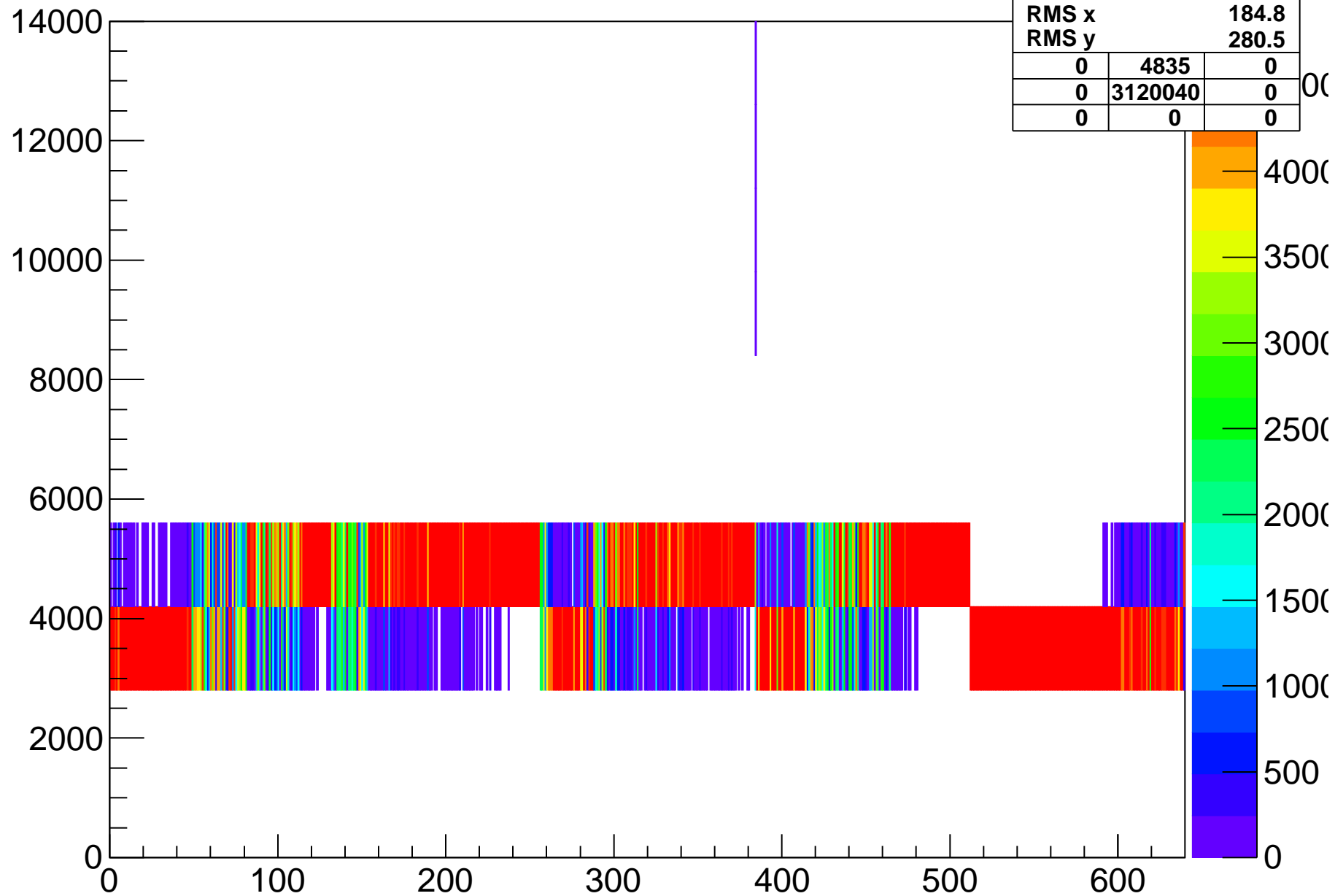
baselinesamples-fpga-0-hyb-0-sample-2

Entries	3124875	
Mean x	319.5	
Mean y	4188	
RMS x	184.8	
RMS y	280.7	
0	4831	0
0	3120044	0
0	0	0



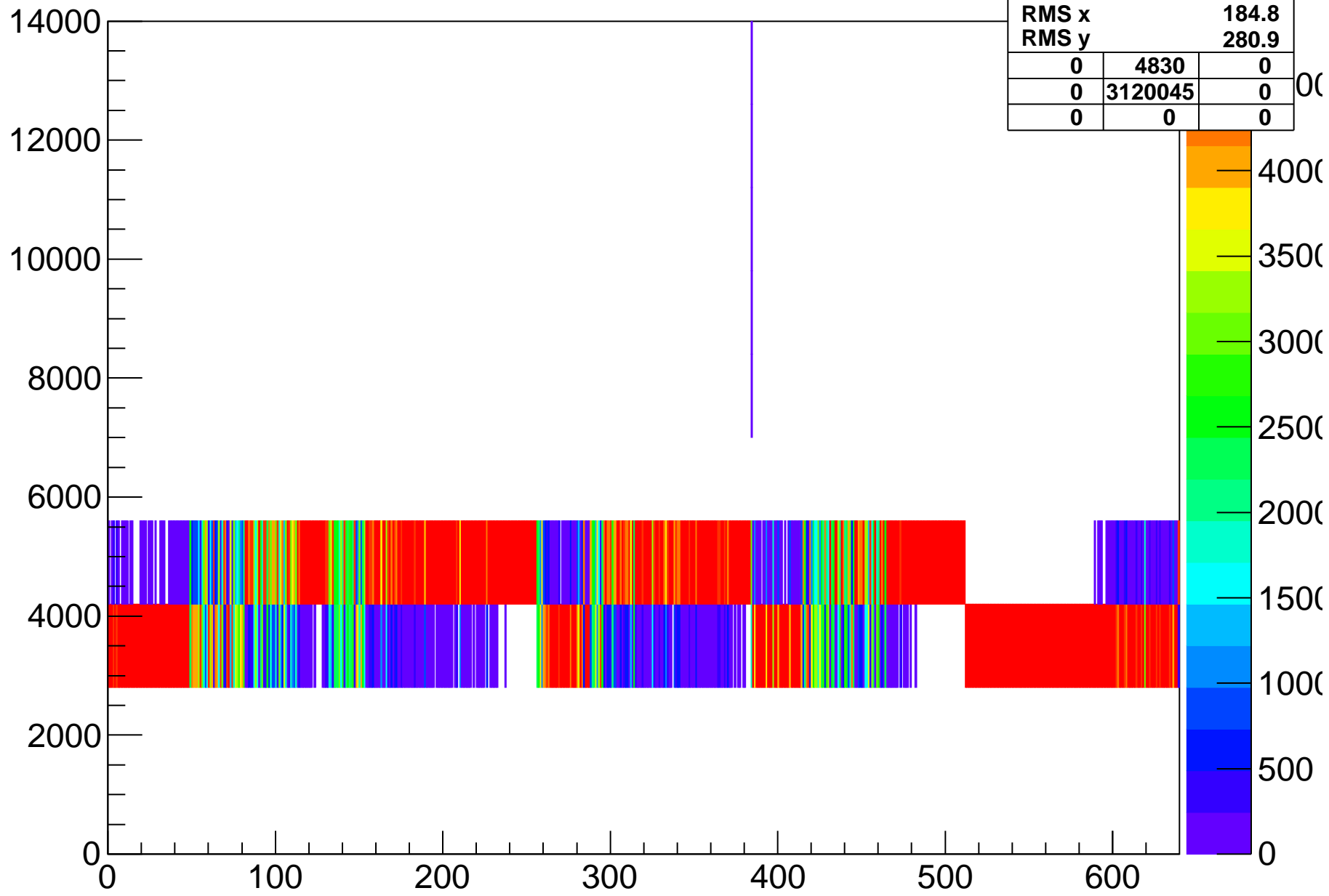
baselinesamples-fpga-0-hyb-0-sample-3

Entries	3124875	
Mean x	319.5	
Mean y	4191	
RMS x	184.8	
RMS y	280.5	
0	4835	0
0	3120040	0
0	0	0



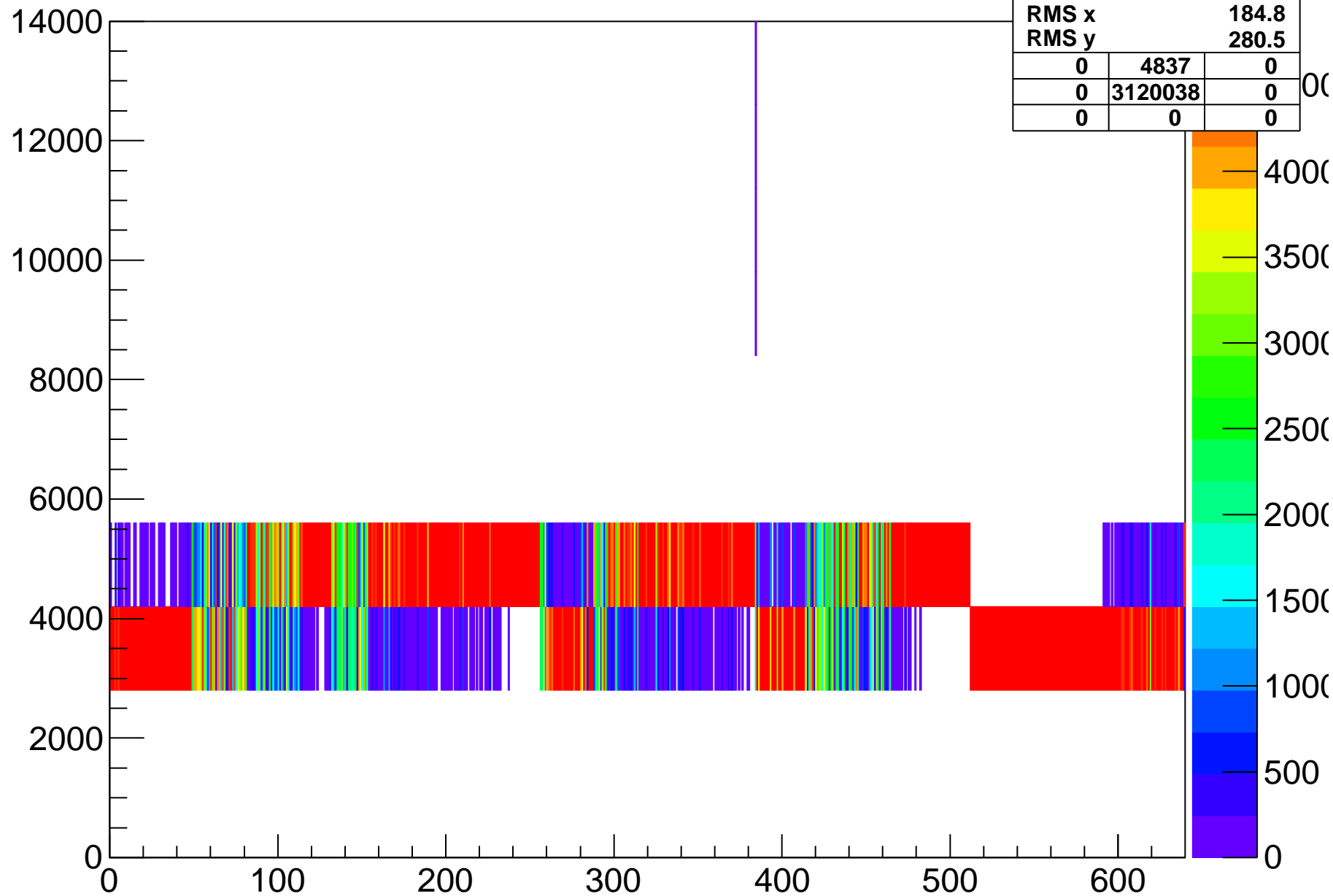
baselinesamples-fpga-0-hyb-0-sample-4

Entries		3124875
Mean x		319.5
Mean y		4185
RMS x		184.8
RMS y		280.9
0	4830	0
0	3120045	0
0	0	0



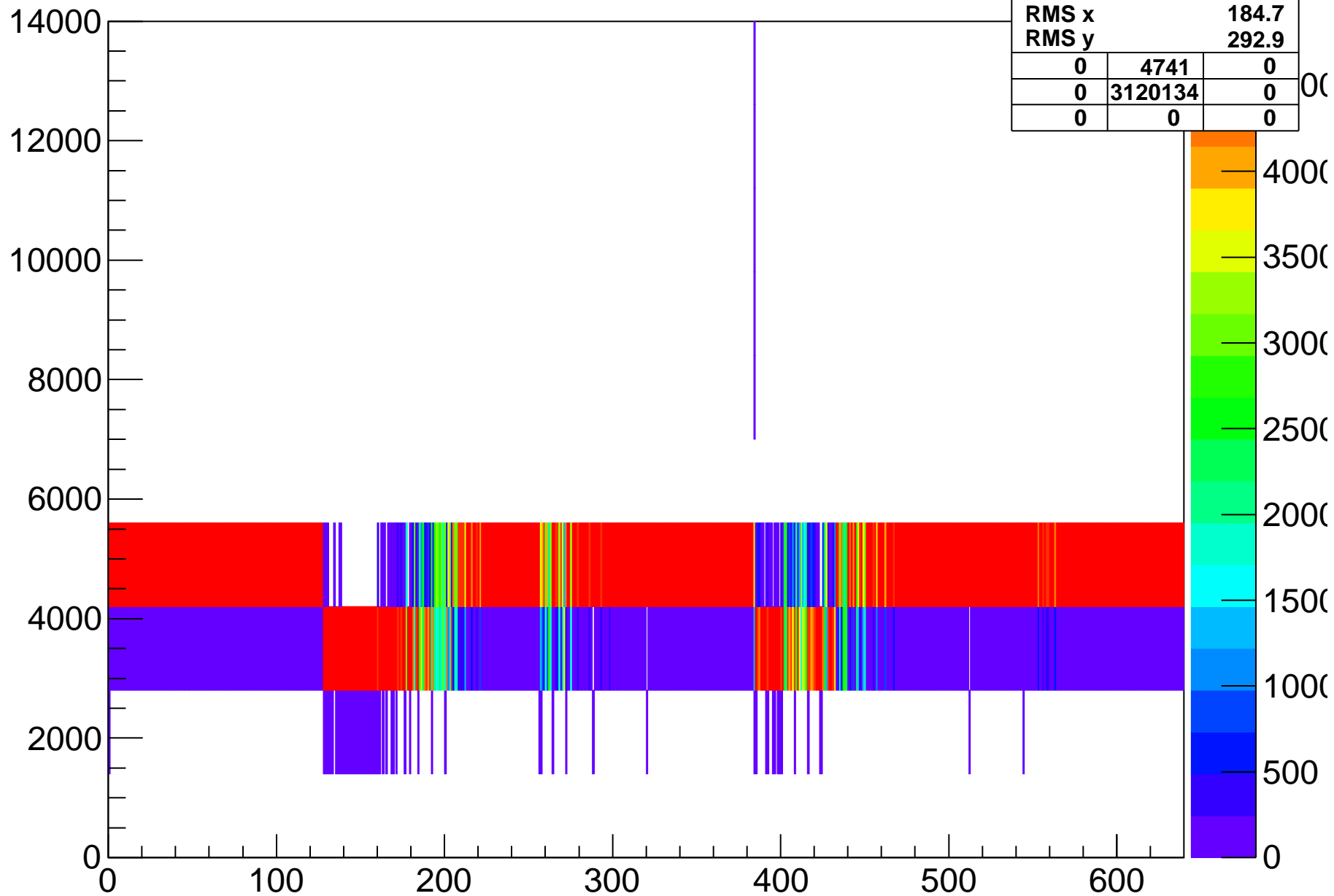
baselinesamples-fpga-0-hyb-0-sample-5

Entries		3124875
Mean x		319.5
Mean y		4187
RMS x		184.8
RMS y		280.5
0	4837	0
0	3120038	0
0	0	0



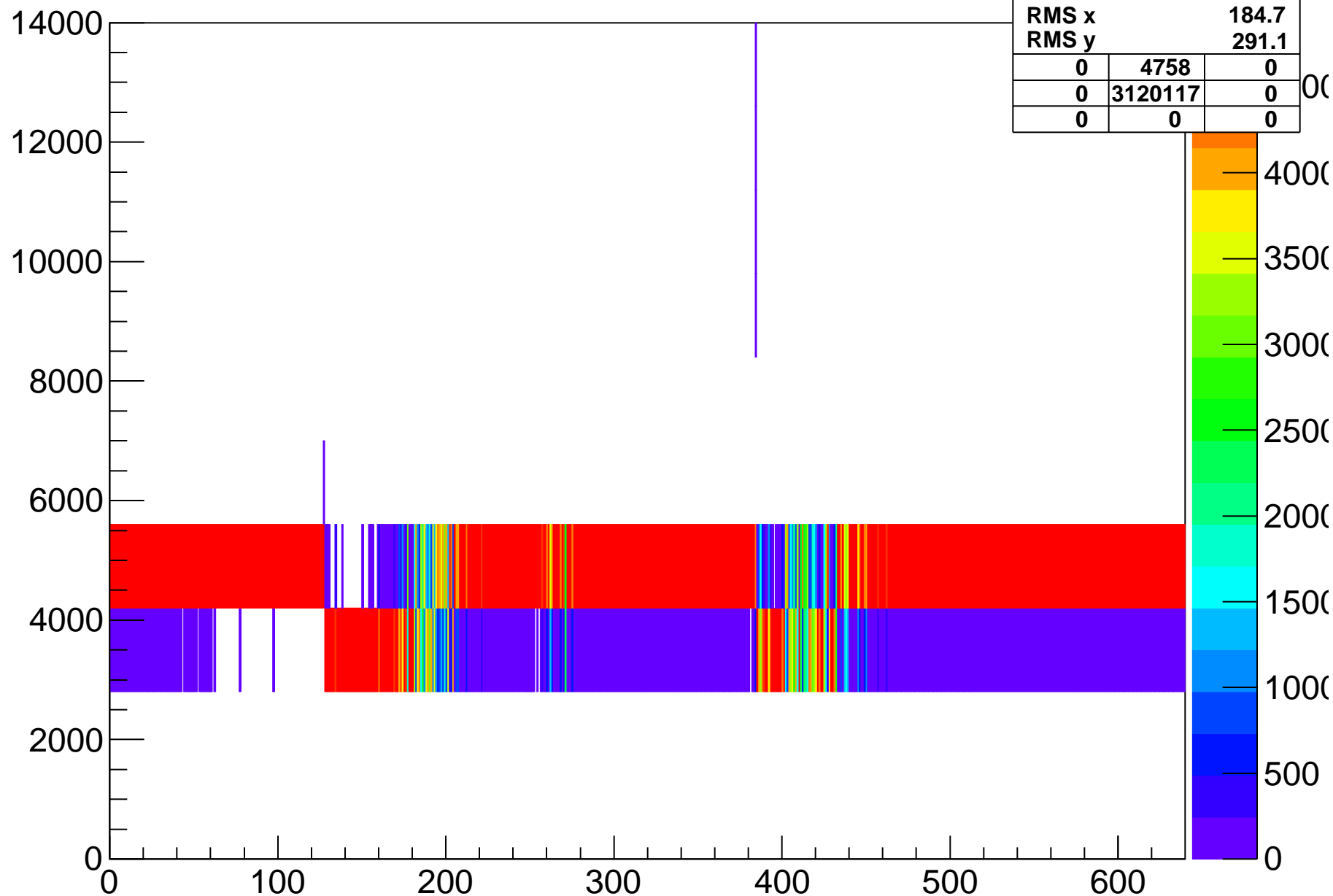
baselinesamples-fpga-0-hyb-1-sample-0

Entries	3124875	
Mean x	319.5	
Mean y	4449	
RMS x	184.7	
RMS y	292.9	
0	4741	0
0	3120134	0
0	0	0



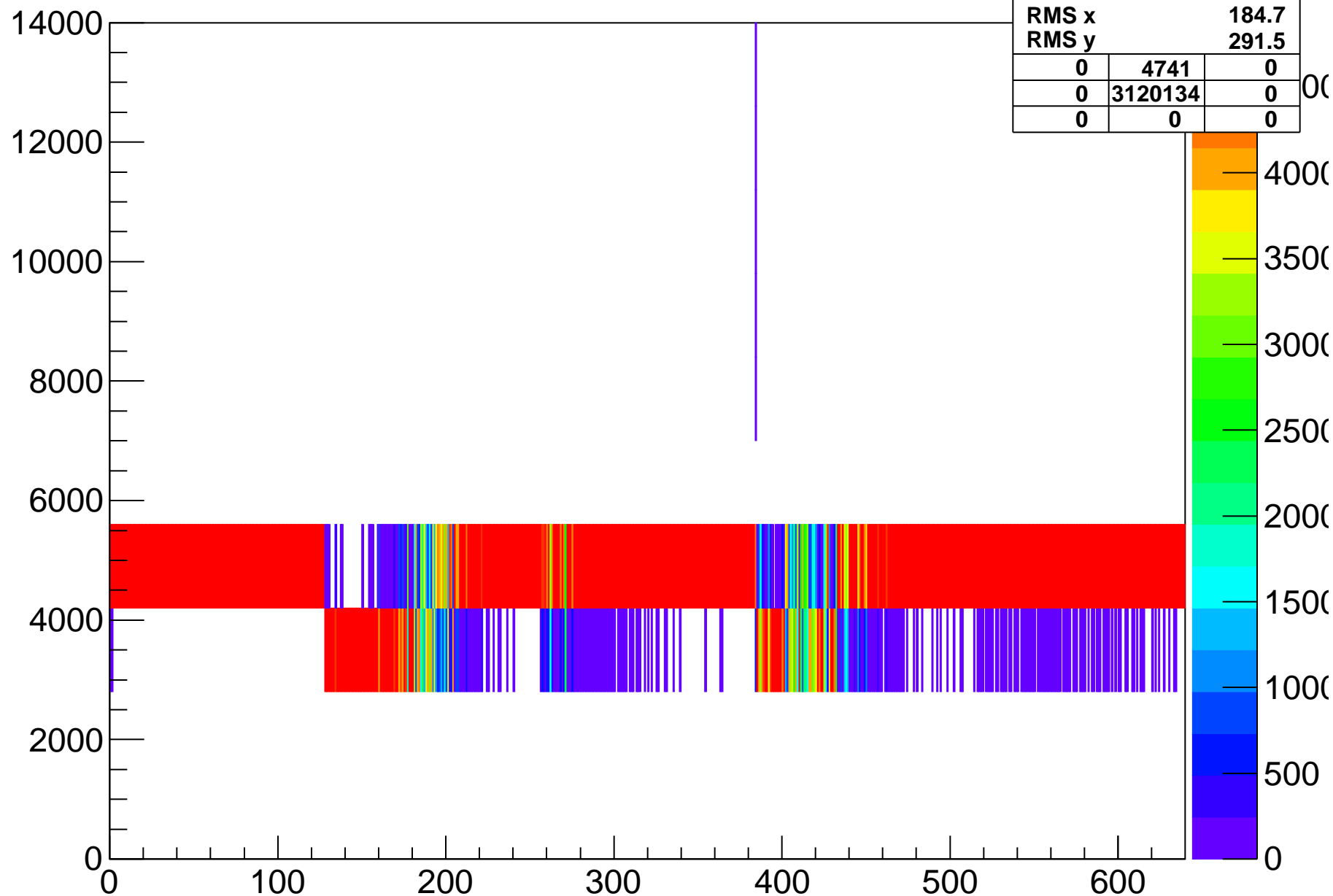
baselinesamples-fpga-0-hyb-1-sample-1

Entries	3124875	
Mean x	319.5	
Mean y	4485	
RMS x	184.7	
RMS y	291.1	
0	4758	0
0	3120117	0
0	0	0



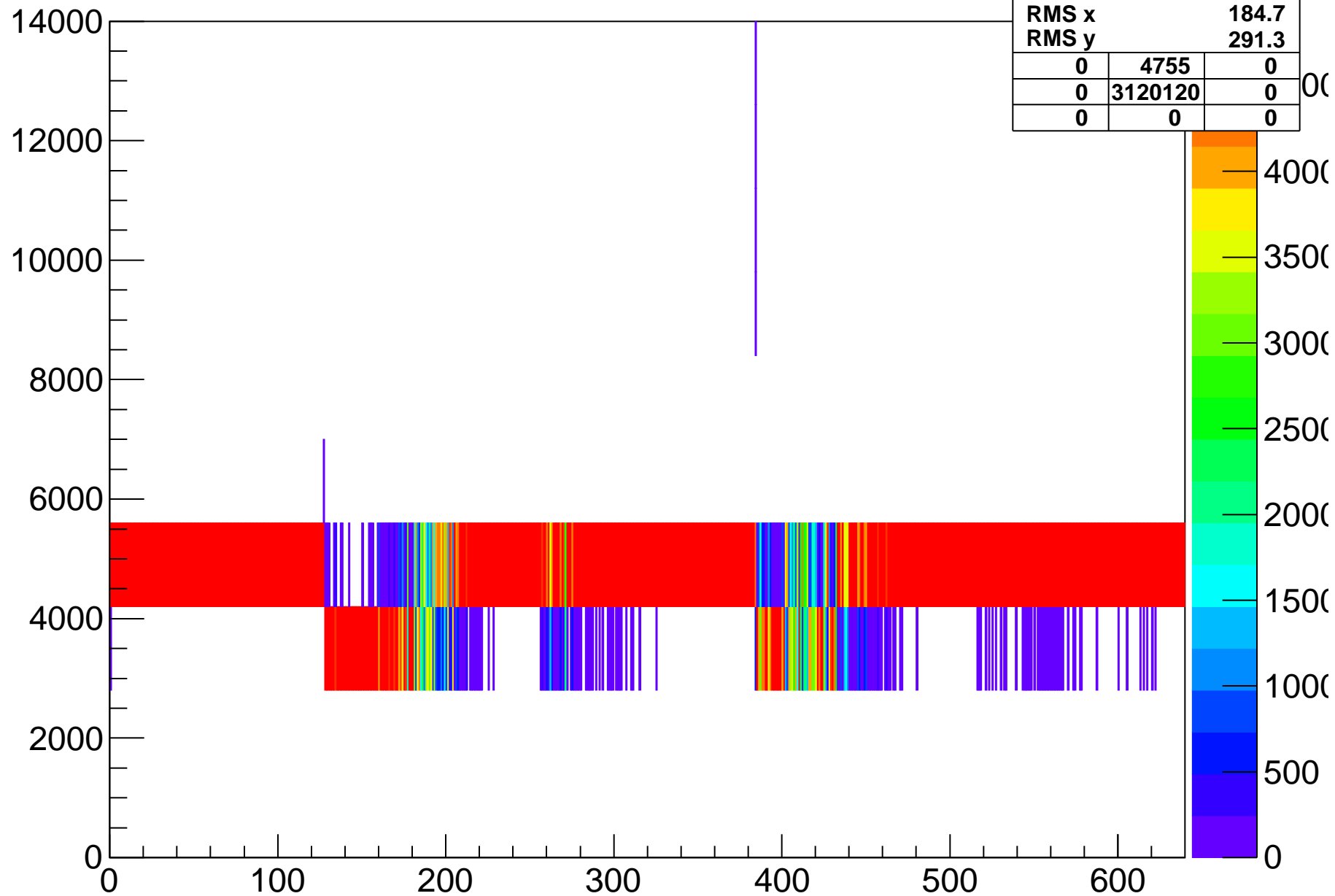
baselinesamples-fpga-0-hyb-1-sample-2

Entries	3124875	
Mean x	319.5	
Mean y	4484	
RMS x	184.7	
RMS y	291.5	
0	4741	0
0	3120134	0
0	0	0



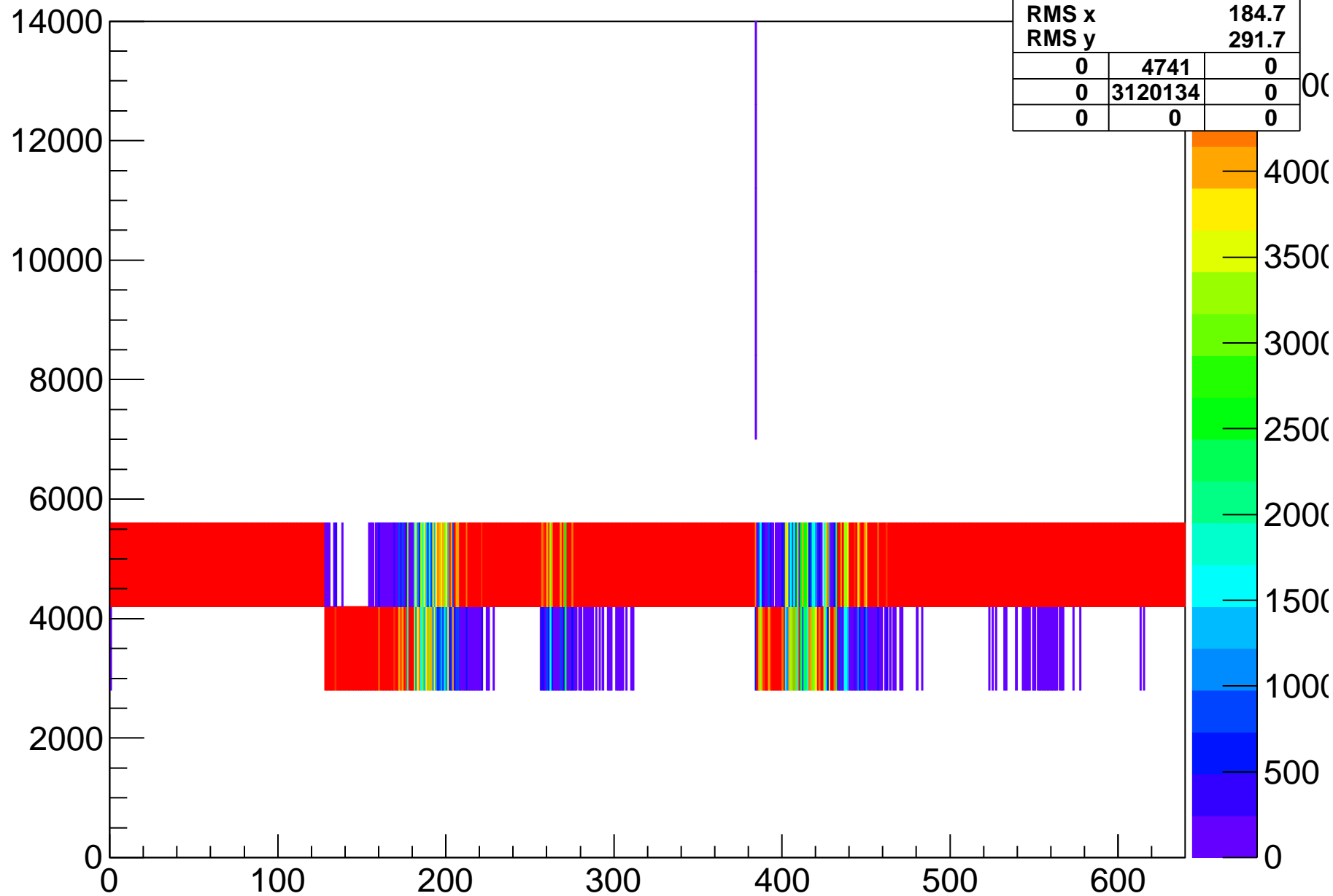
baselinesamples-fpga-0-hyb-1-sample-3

Entries	3124875	
Mean x	319.5	
Mean y	4488	
RMS x	184.7	
RMS y	291.3	
0	4755	0
0	3120120	0
0	0	0



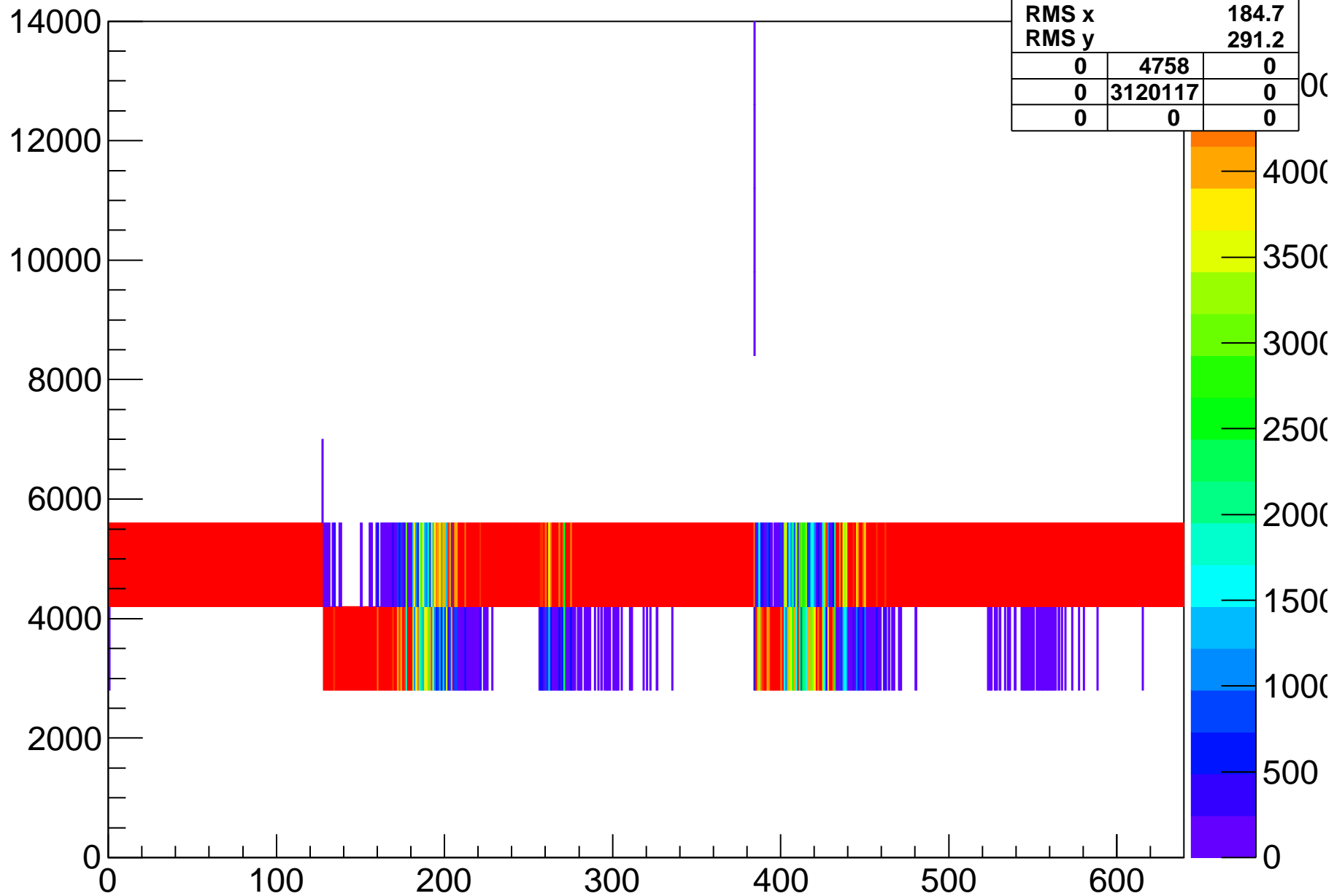
baselinesamples-fpga-0-hyb-1-sample-4

Entries	3124875	
Mean x	319.5	
Mean y	4482	
RMS x	184.7	
RMS y	291.7	
0	4741	0
0	3120134	0
0	0	0



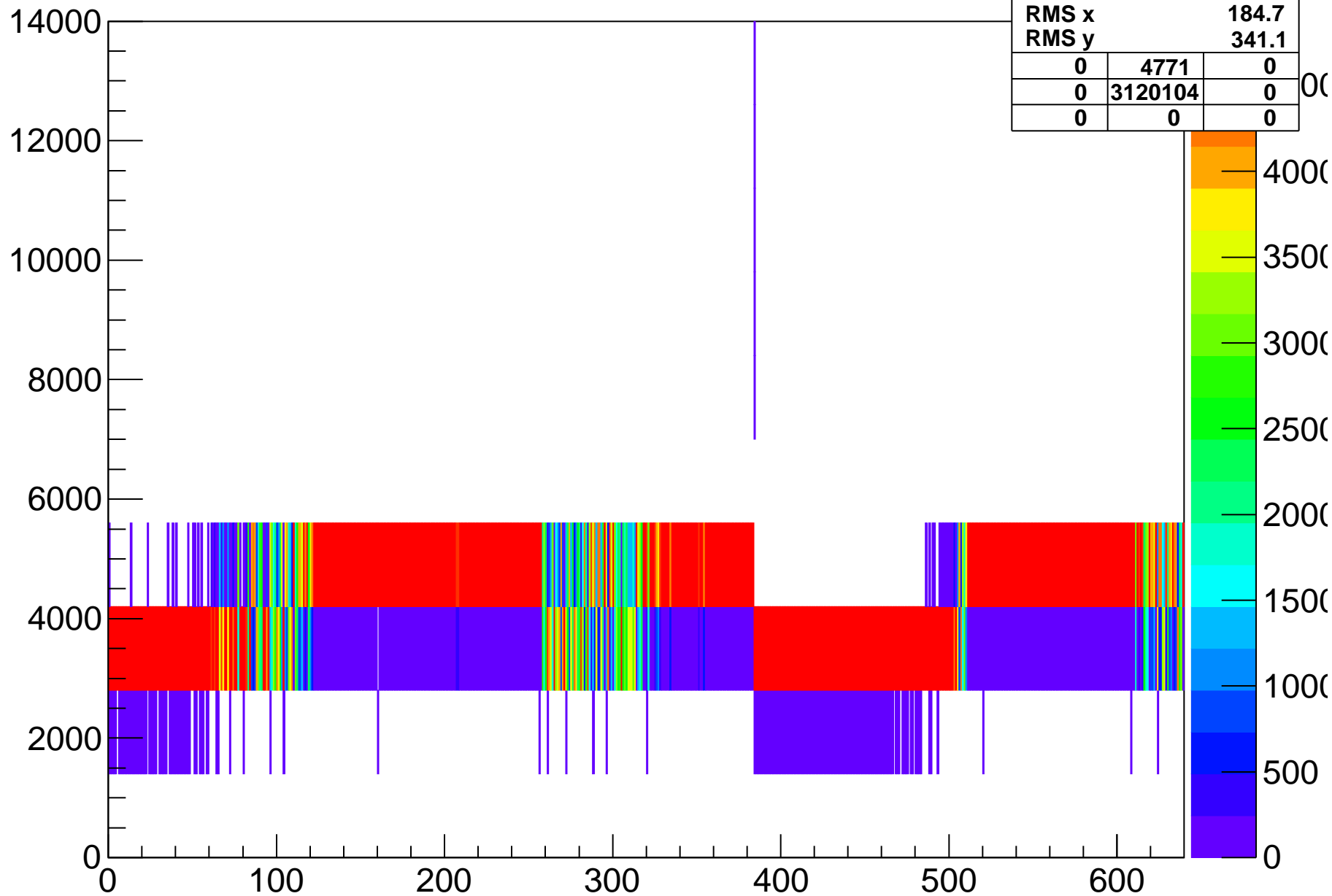
baselinesamples-fpga-0-hyb-1-sample-5

Entries	3124875	
Mean x	319.5	
Mean y	4484	
RMS x	184.7	
RMS y	291.2	
0	4758	0
0	3120117	0
0	0	0



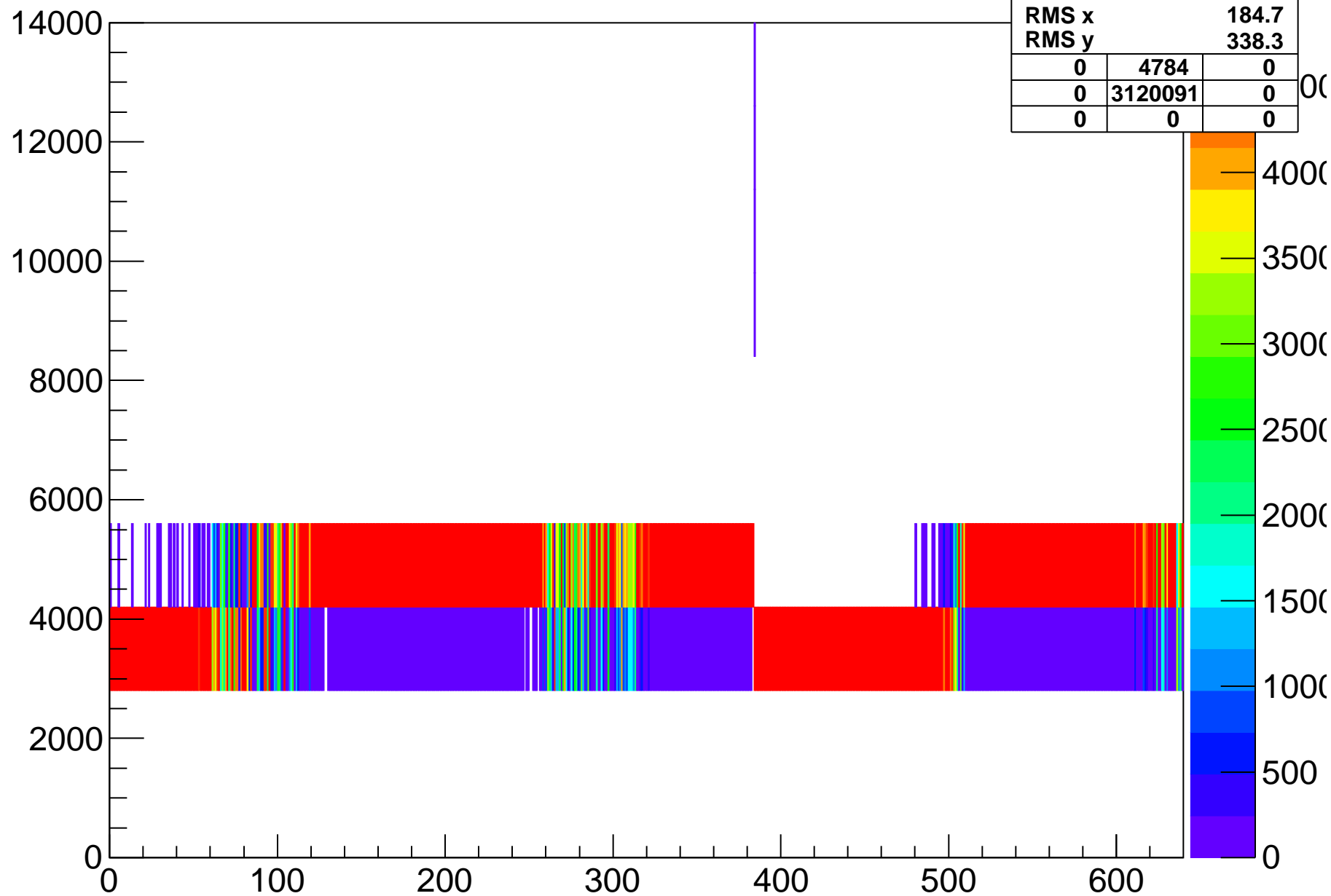
baselinesamples-fpga-0-hyb-2-sample-0

Entries	3124875	
Mean x	319.5	
Mean y	4210	
RMS x	184.7	
RMS y	341.1	
0	4771	0
0	3120104	0
0	0	0



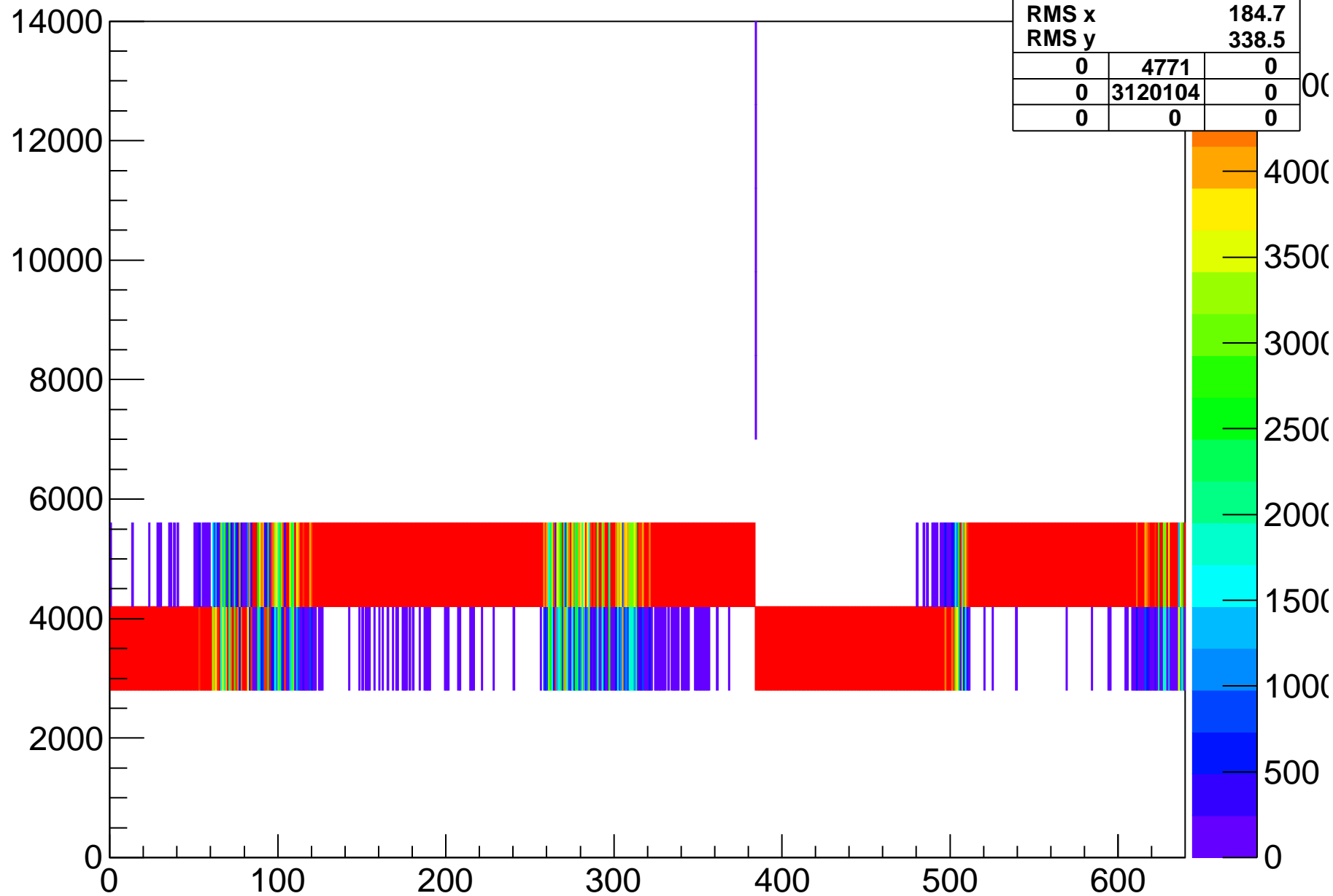
baselinesamples-fpga-0-hyb-2-sample-1

Entries	3124875	
Mean x	319.5	
Mean y	4272	
RMS x	184.7	
RMS y	338.3	
0	4784	0
0	3120091	0
0	0	0



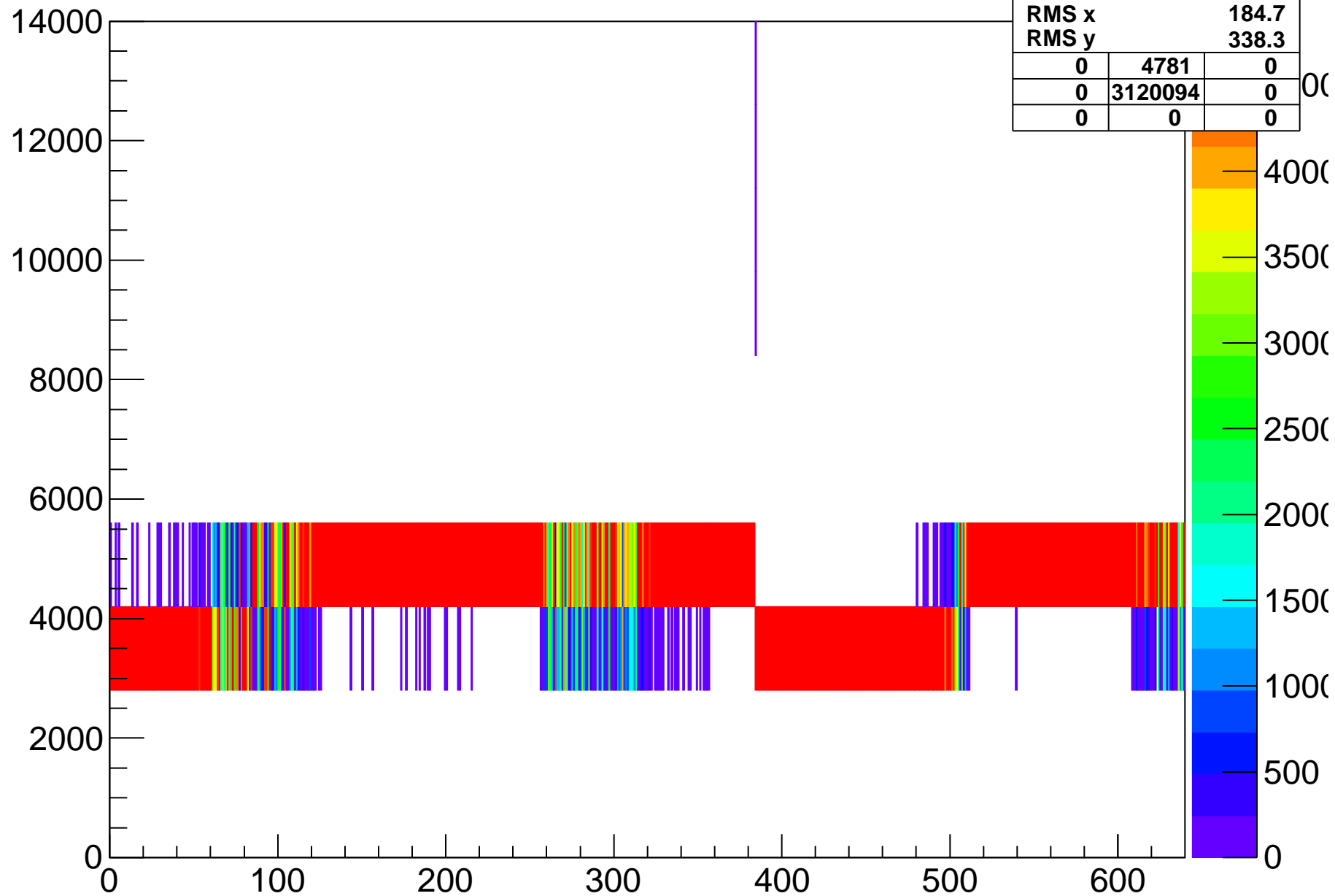
baselinesamples-fpga-0-hyb-2-sample-2

Entries	3124875	
Mean x	319.5	
Mean y	4268	
RMS x	184.7	
RMS y	338.5	
0	4771	0
0	3120104	0
0	0	0



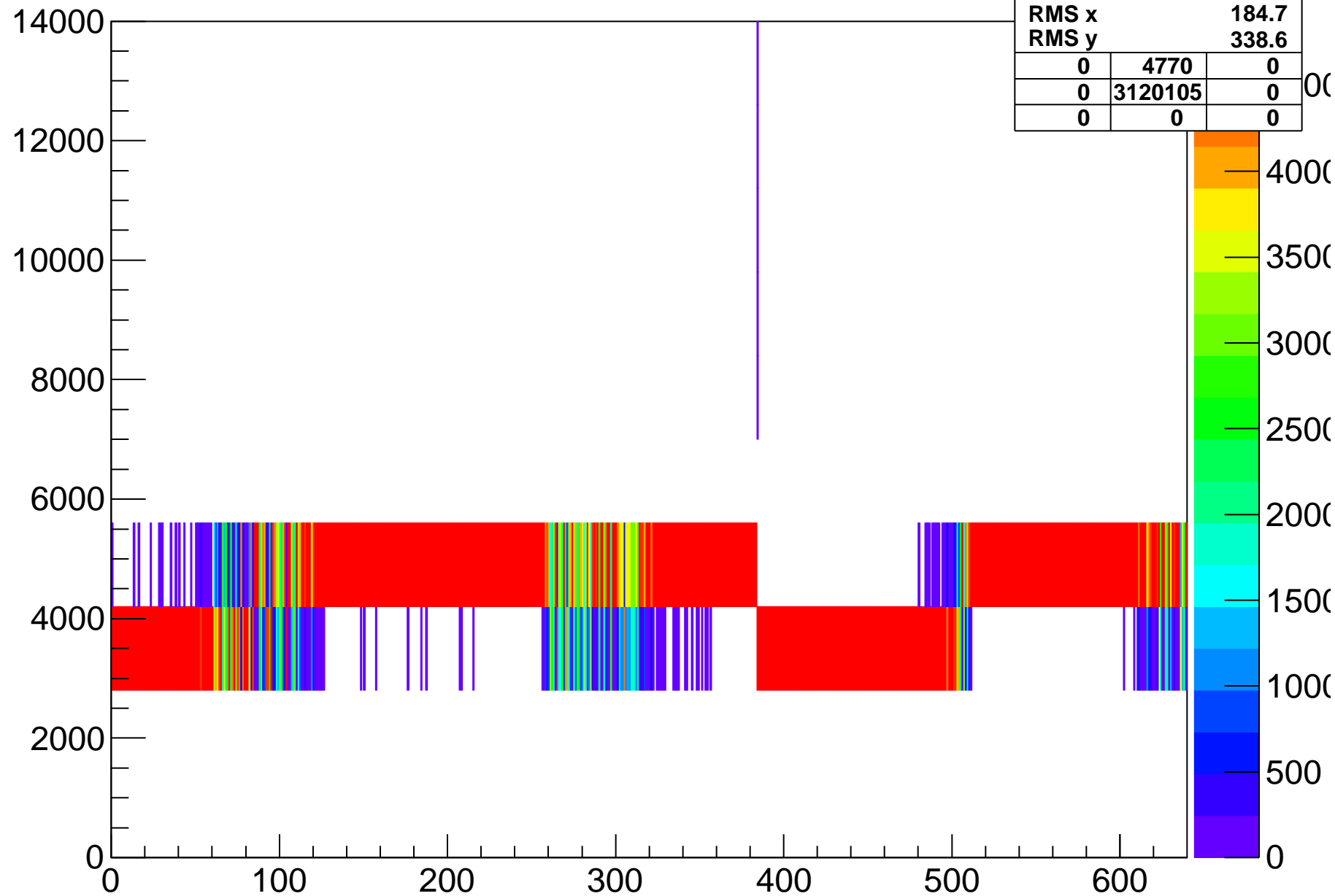
baselinesamples-fpga-0-hyb-2-sample-3

Entries	3124875	
Mean x	319.5	
Mean y	4272	
RMS x	184.7	
RMS y	338.3	
0	4781	0
0	3120094	0
0	0	0



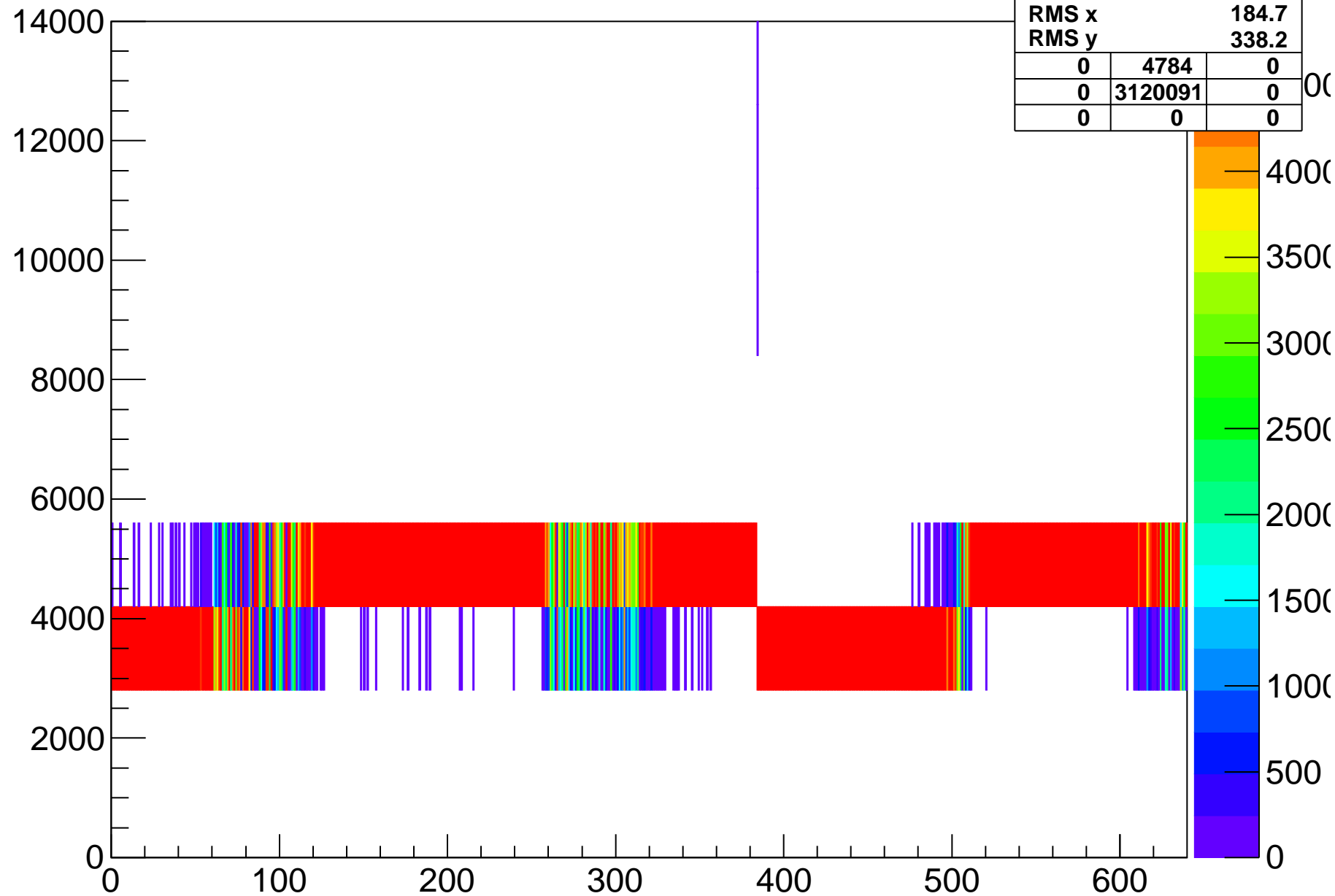
baselinesamples-fpga-0-hyb-2-sample-4

Entries	3124875	
Mean x	319.5	
Mean y	4266	
RMS x	184.7	
RMS y	338.6	
0	4770	0
0	3120105	0
0	0	0



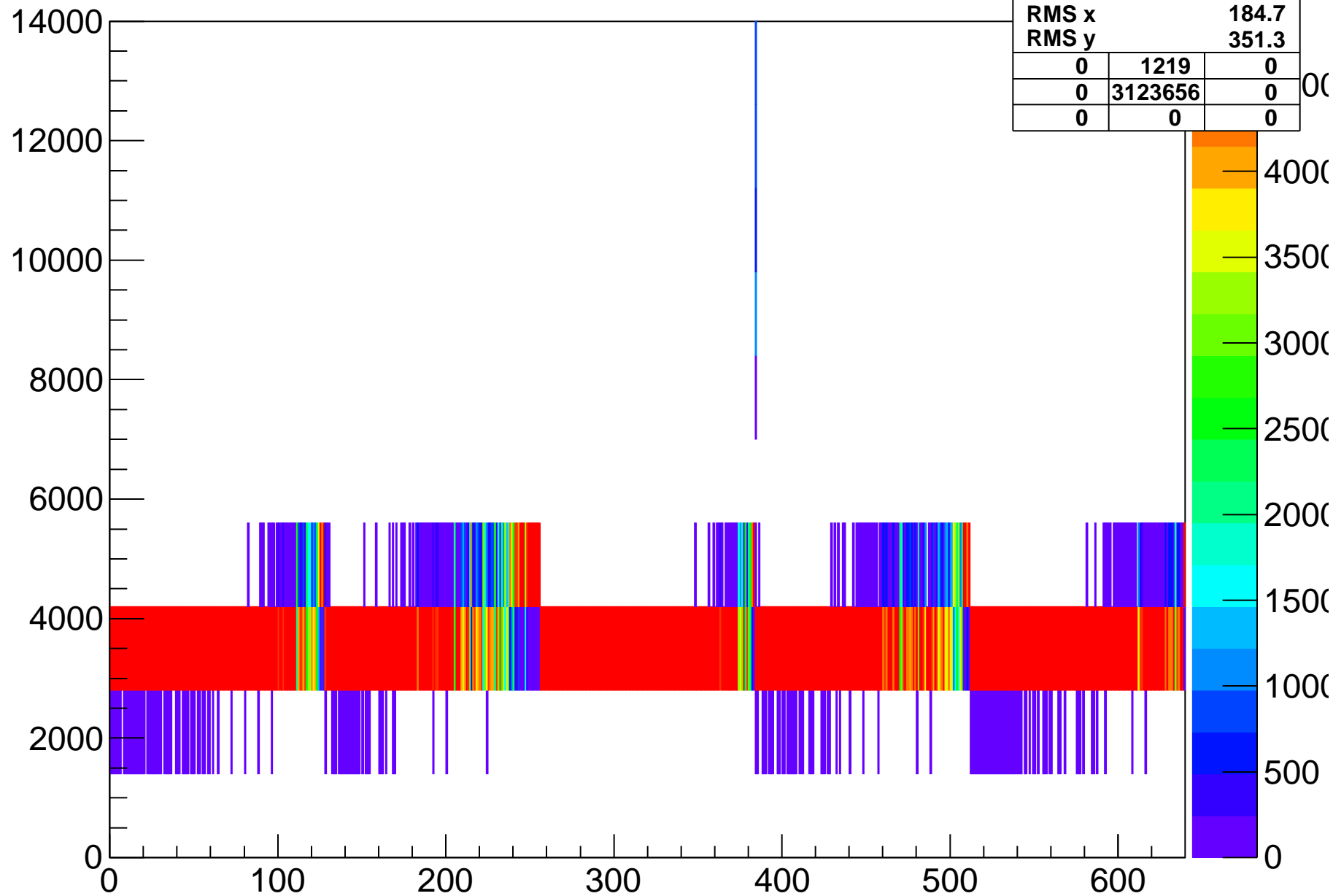
baselinesamples-fpga-0-hyb-2-sample-5

Entries	3124875	
Mean x	319.5	
Mean y	4268	
RMS x	184.7	
RMS y	338.2	
0	4784	0
0	3120091	0
0	0	0



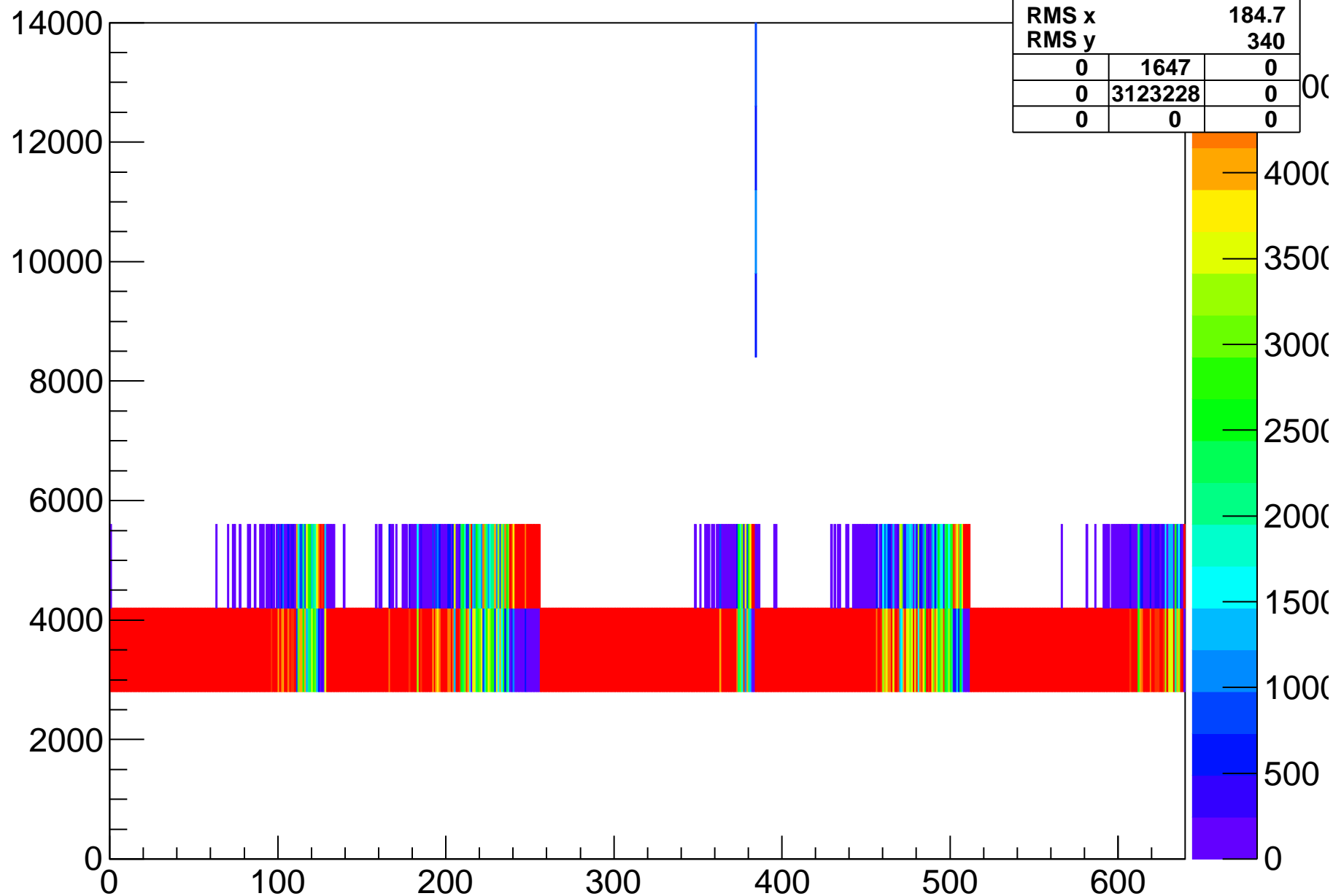
baselinesamples-fpga-0-hyb-3-sample-0

Entries	3124875	
Mean x	319.6	
Mean y	3891	
RMS x	184.7	
RMS y	351.3	
0	1219	0
0	3123656	0
0	0	0



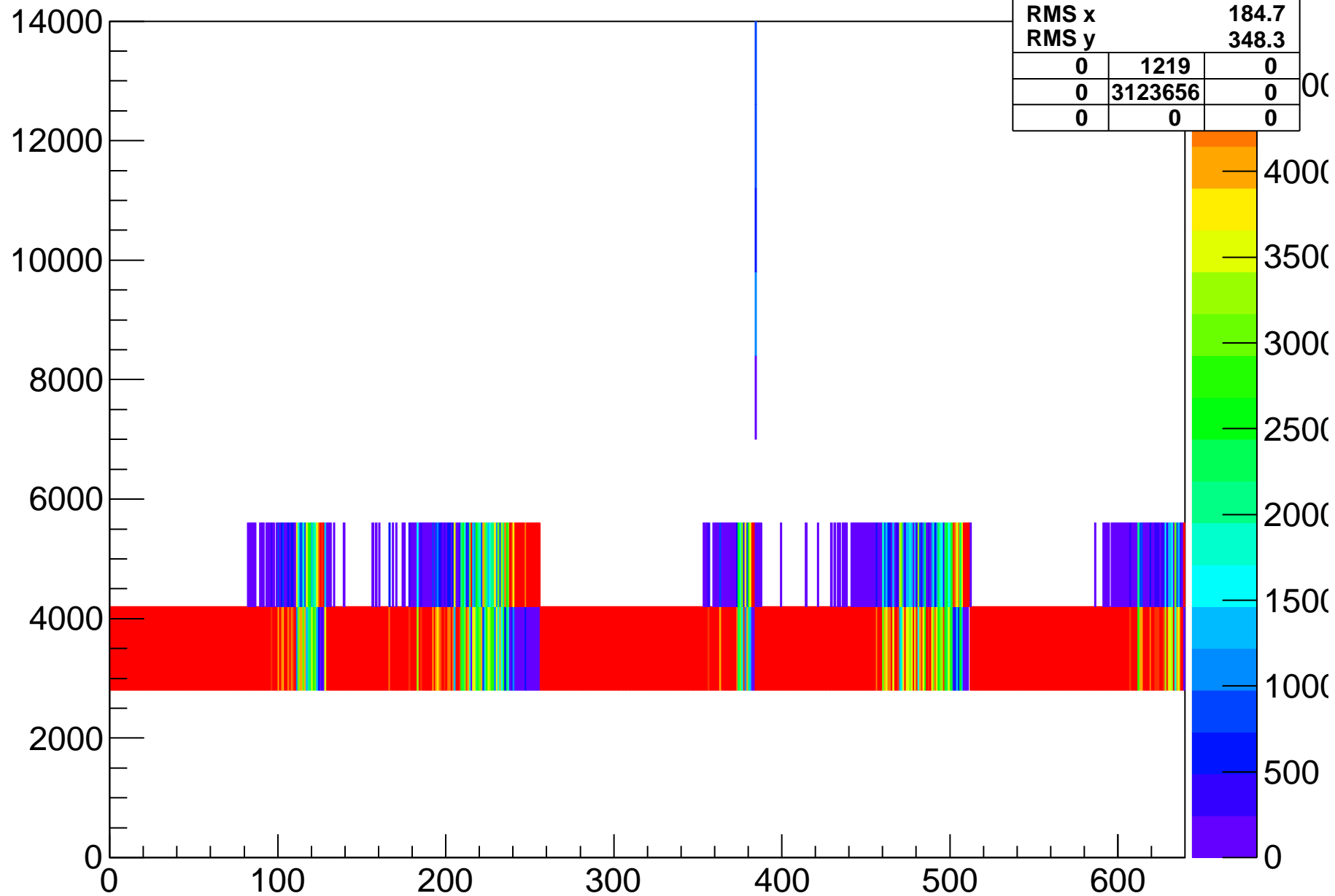
baselinesamples-fpga-0-hyb-3-sample-1

Entries	3124875	
Mean x	319.6	
Mean y	3938	
RMS x	184.7	
RMS y	340	
0	1647	0
0	3123228	0
0	0	0



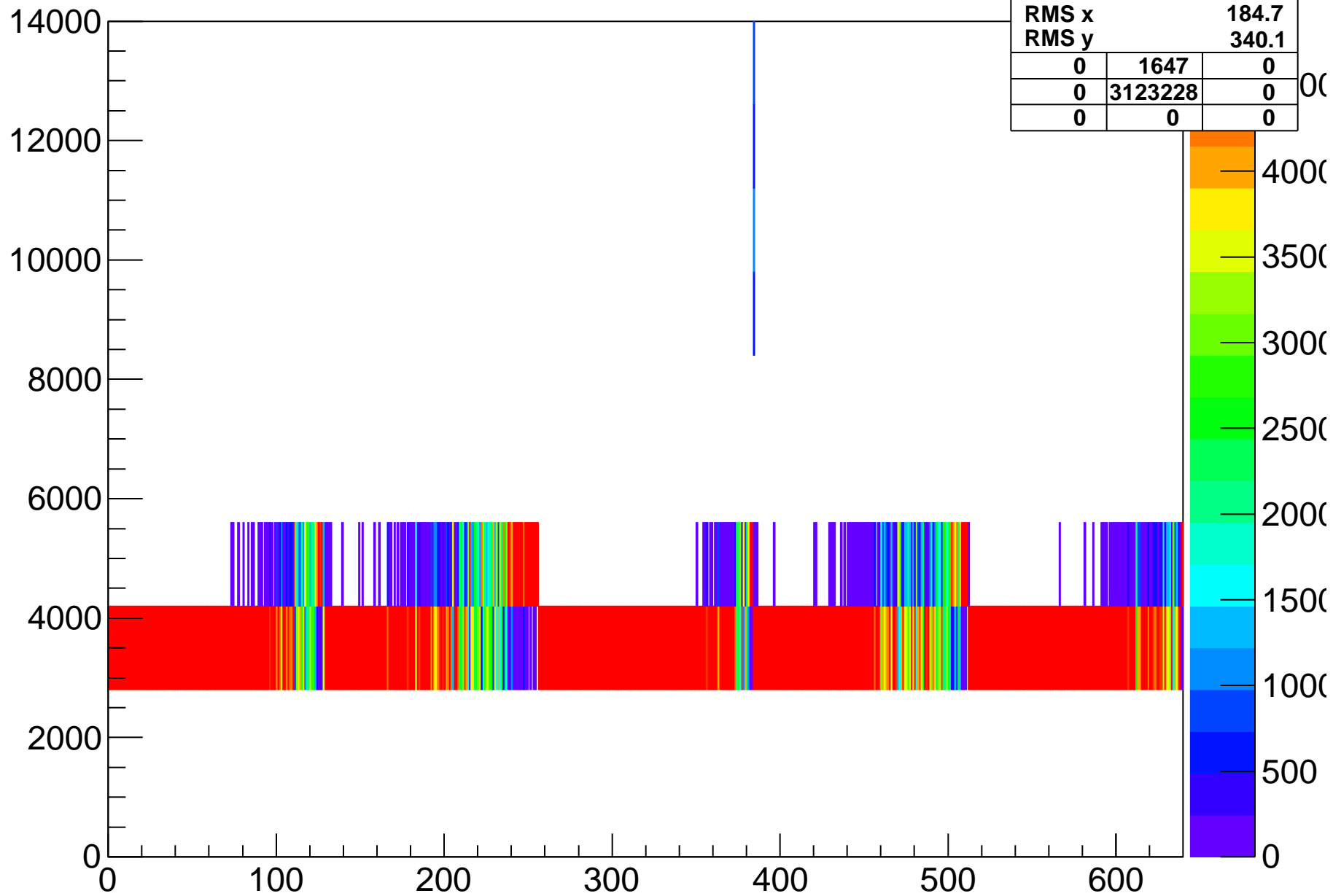
baselinesamples-fpga-0-hyb-3-sample-2

Entries	3124875	
Mean x	319.6	
Mean y	3938	
RMS x	184.7	
RMS y	348.3	
0	1219	0
0	3123656	0
0	0	0



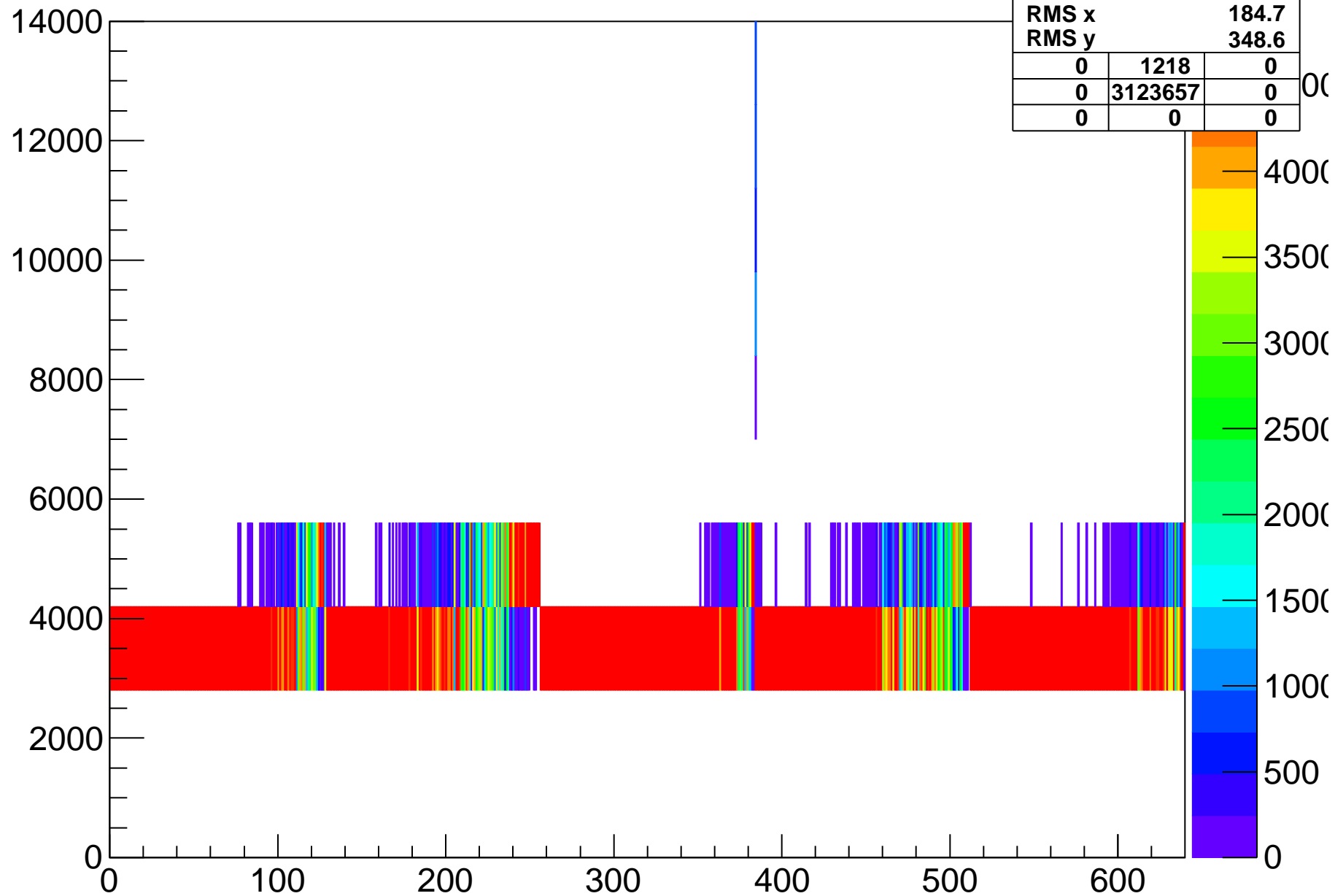
baselinesamples-fpga-0-hyb-3-sample-3

Entries	3124875	
Mean x	319.6	
Mean y	3940	
RMS x	184.7	
RMS y	340.1	
0	1647	0
0	3123228	0
0	0	0



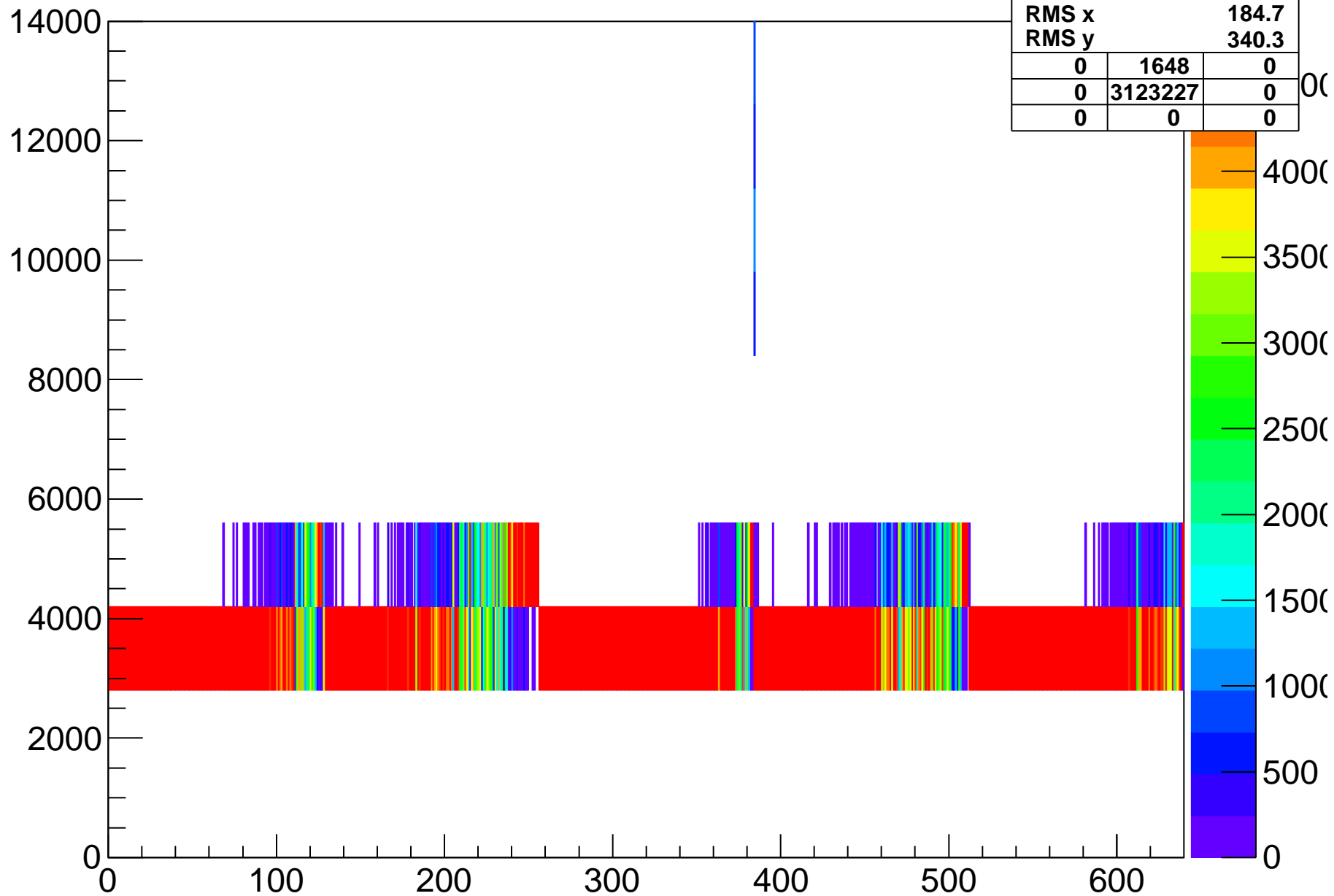
baselinesamples-fpga-0-hyb-3-sample-4

Entries	3124875	
Mean x	319.6	
Mean y	3934	
RMS x	184.7	
RMS y	348.6	
0	1218	0
0	3123657	0
0	0	0



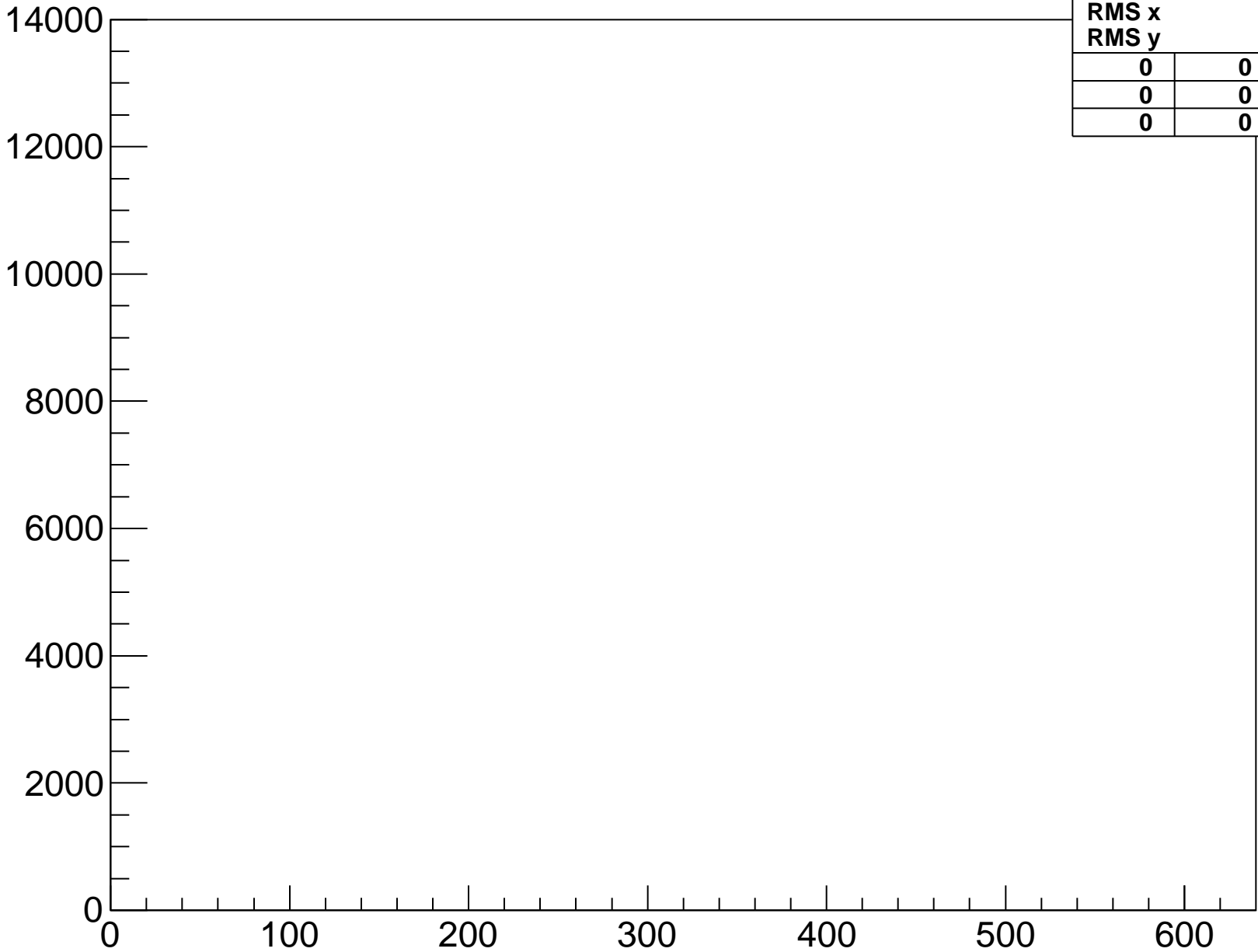
baselinesamples-fpga-0-hyb-3-sample-5

Entries	3124875	
Mean x	319.6	
Mean y	3936	
RMS x	184.7	
RMS y	340.3	
0	1648	0
0	3123227	0
0	0	0



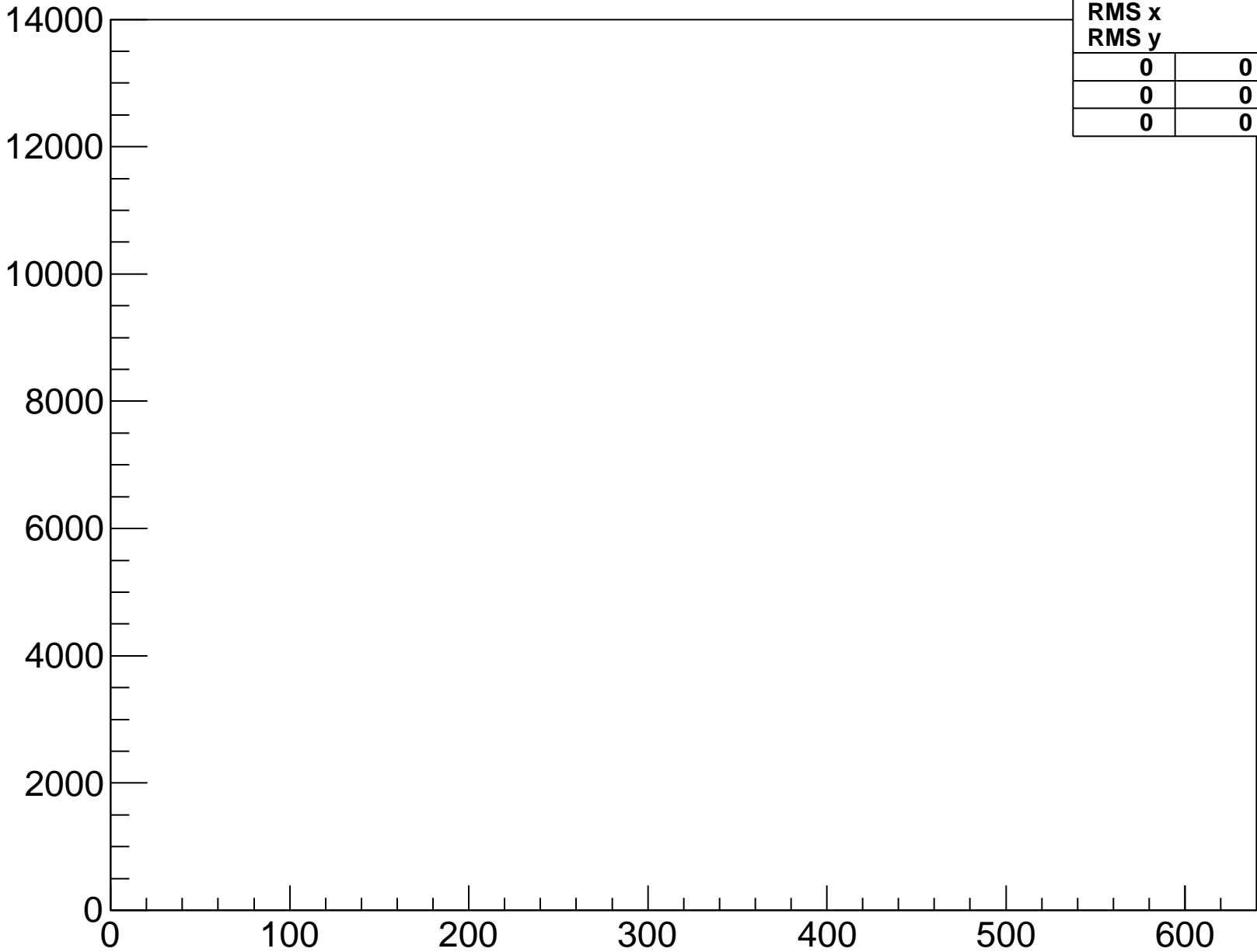
baselinesamples-fpga-1-hyb-0-sample-0

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

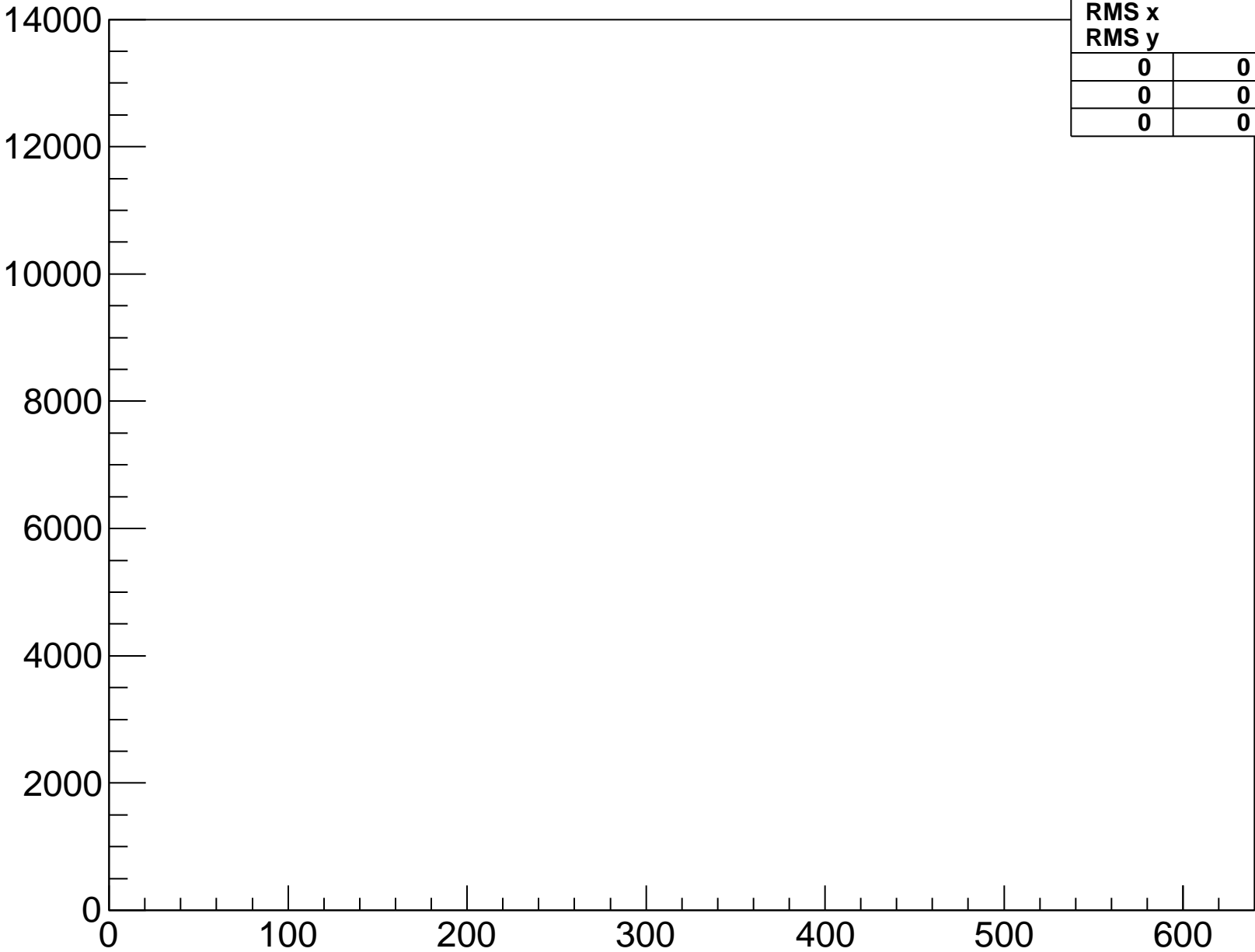


baselinesamples-fpga-1-hyb-0-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	



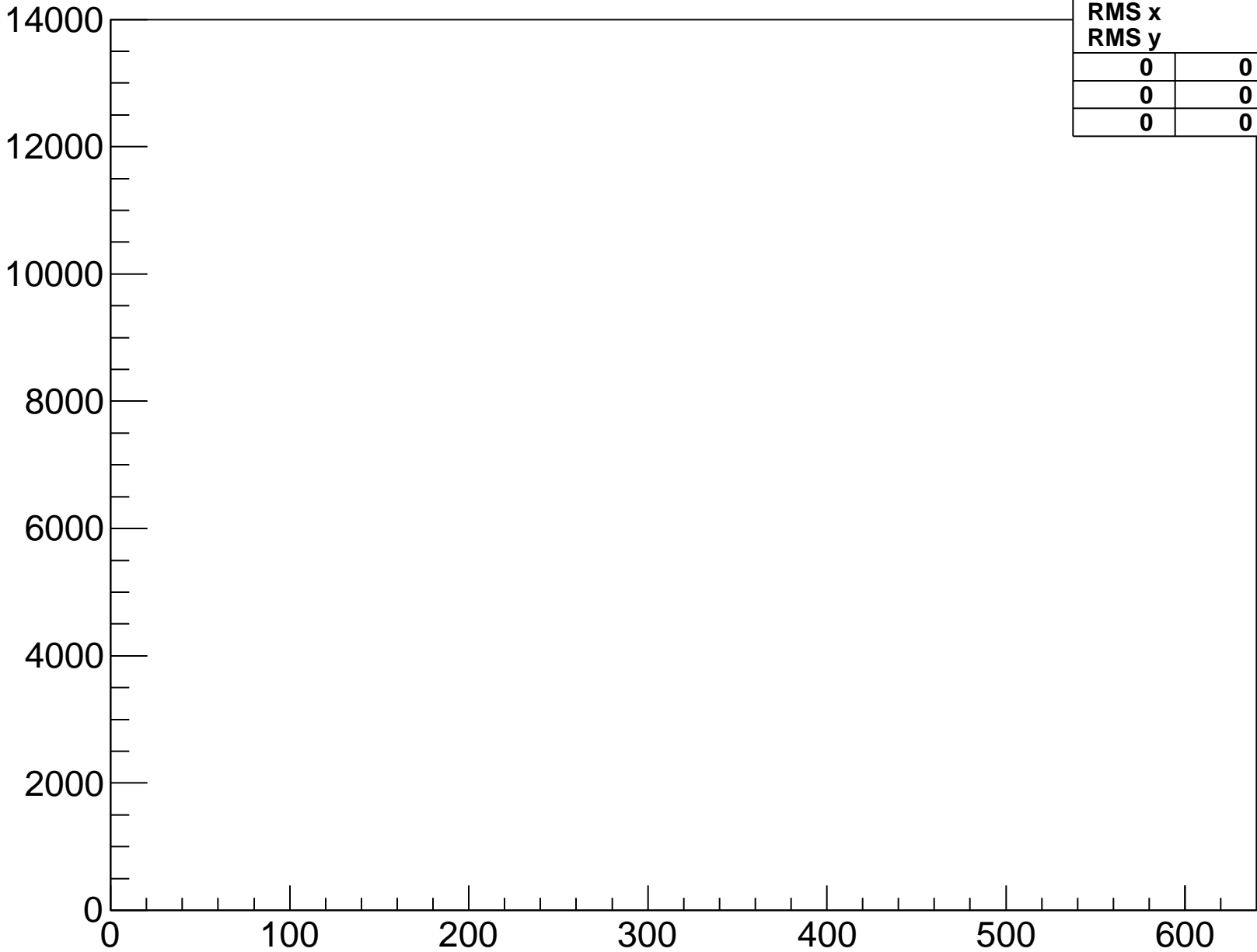
baselinesamples-fpga-1-hyb-0-sample-2



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

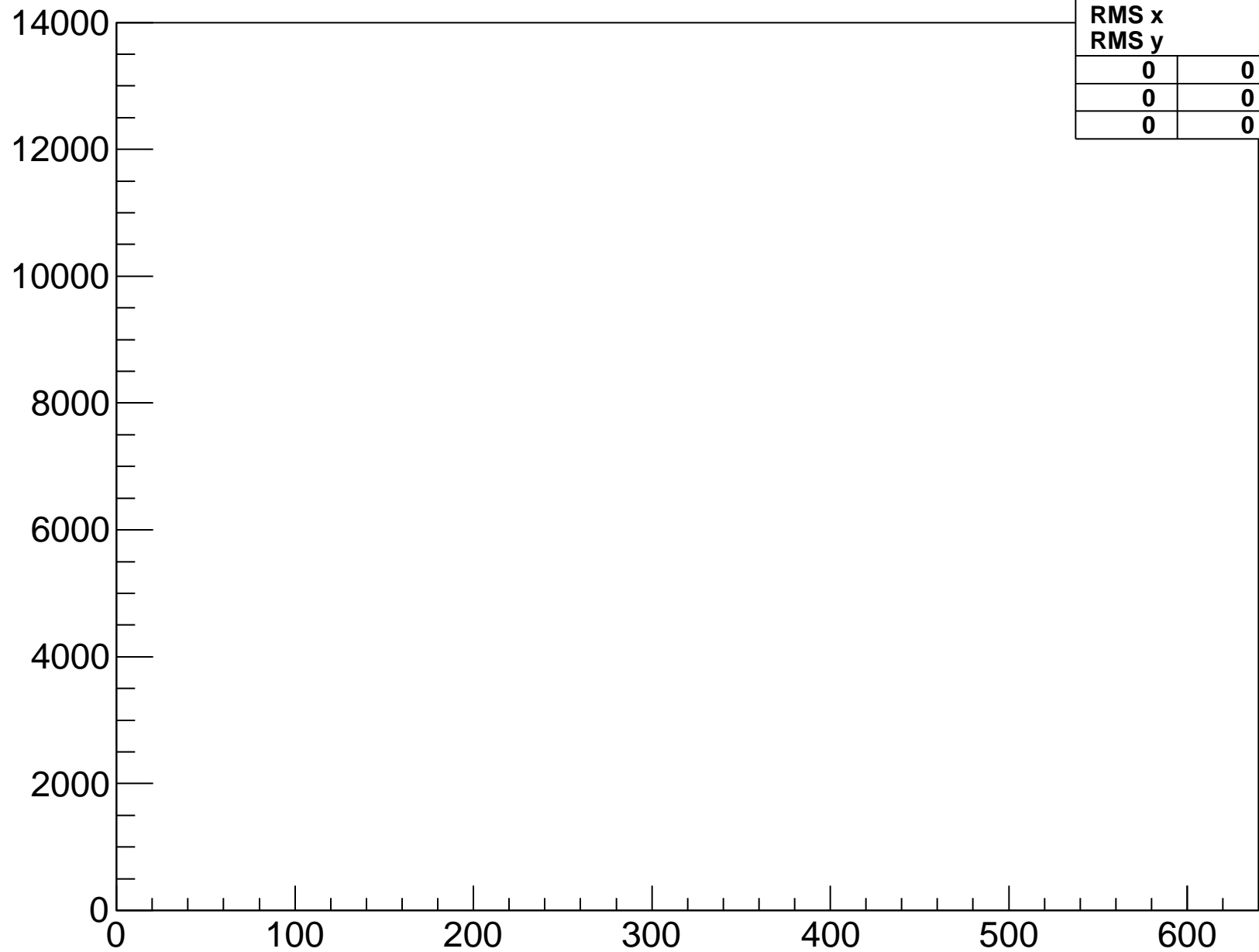
baselinesamples-fpga-1-hyb-0-sample-3

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



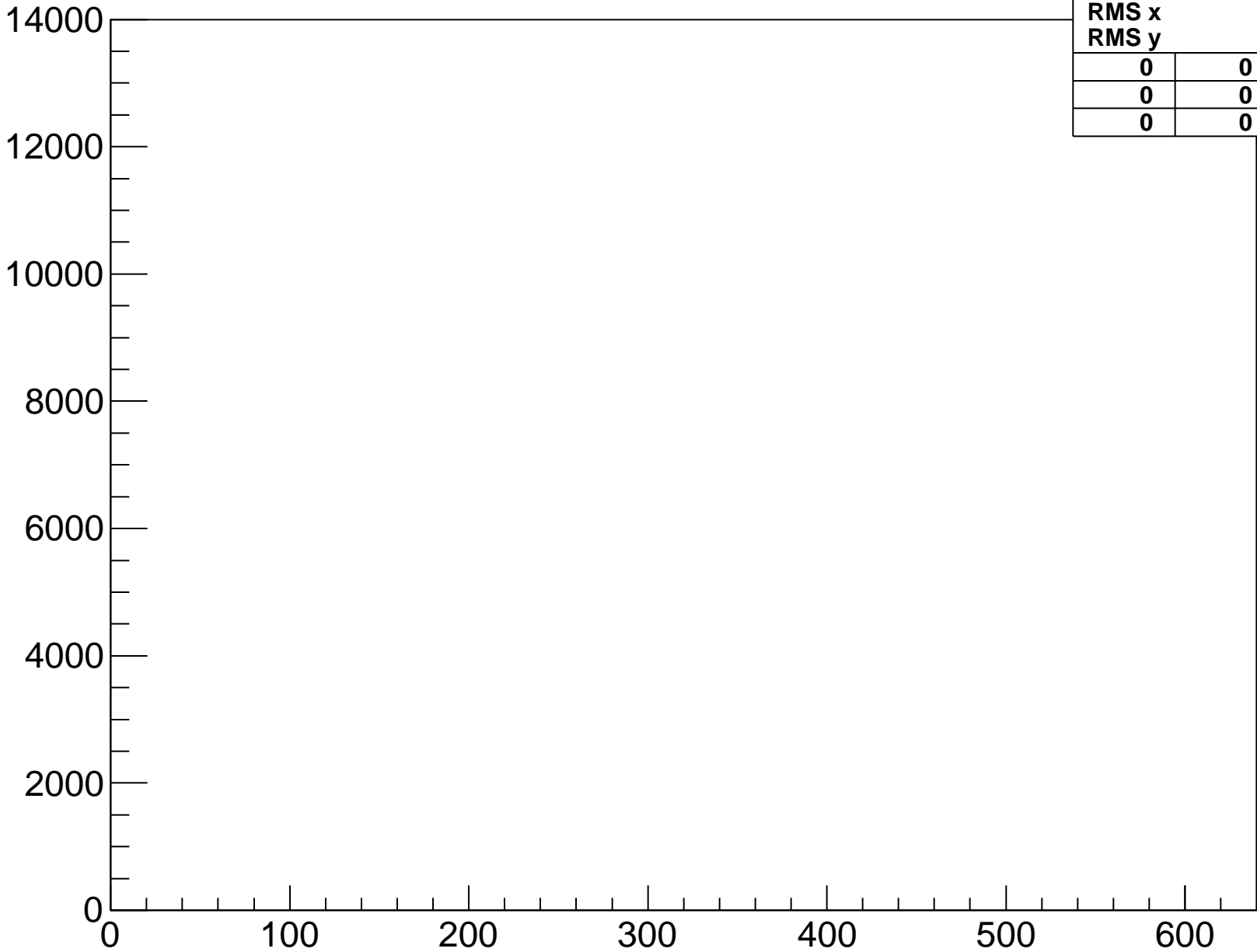
baselinesamples-fpga-1-hyb-0-sample-4

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



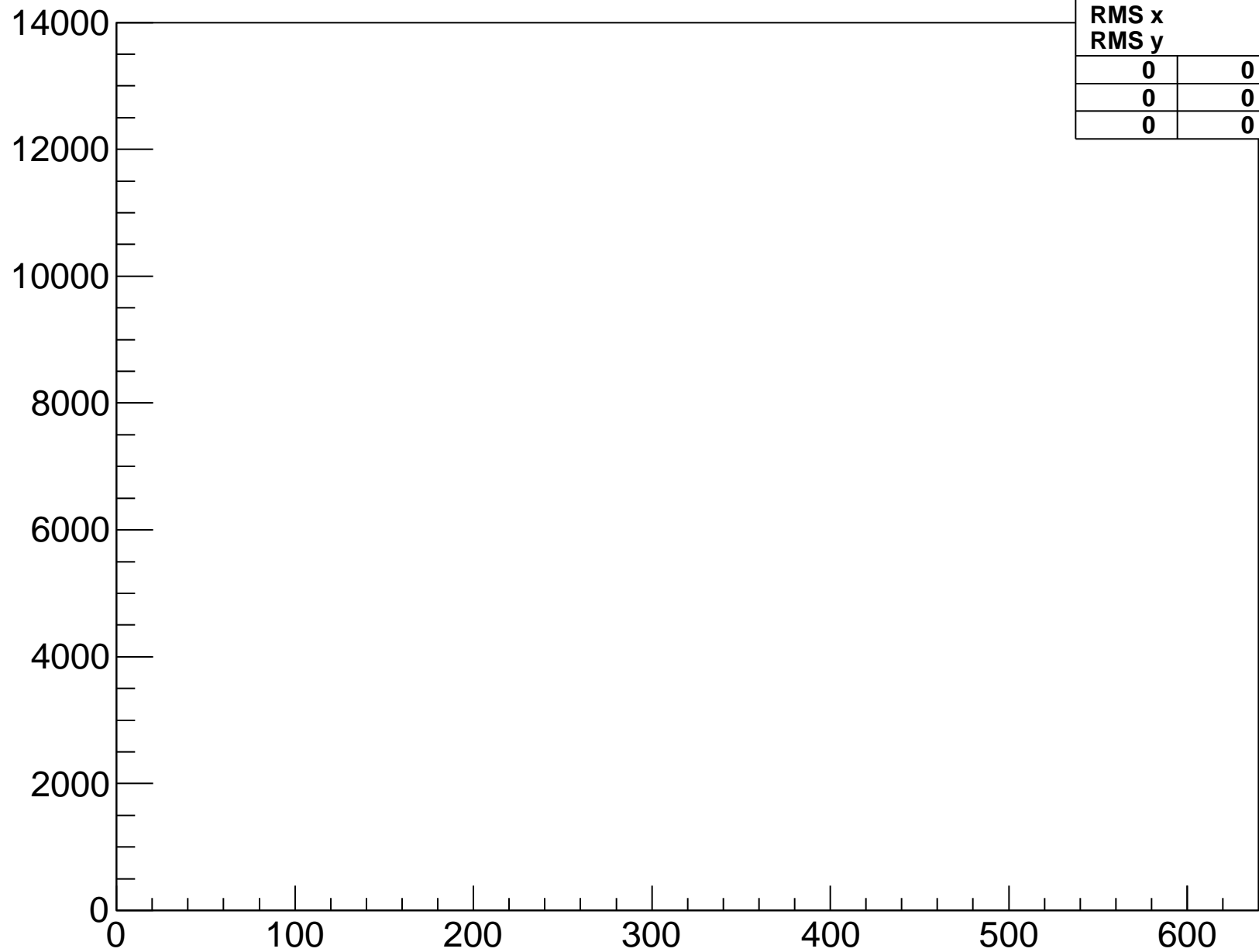
baselinesamples-fpga-1-hyb-0-sample-5

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



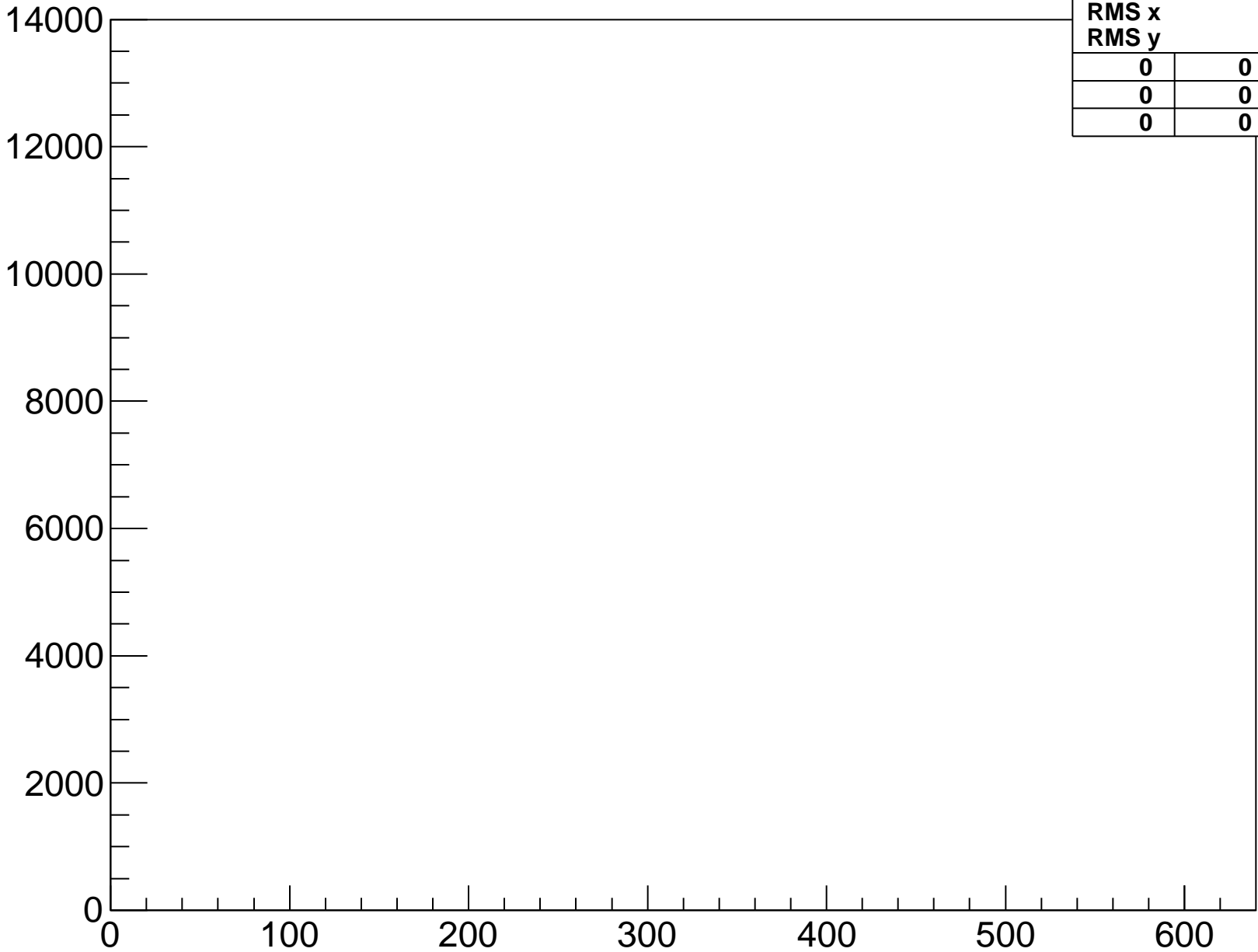
baselinesamples-fpga-1-hyb-1-sample-0

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

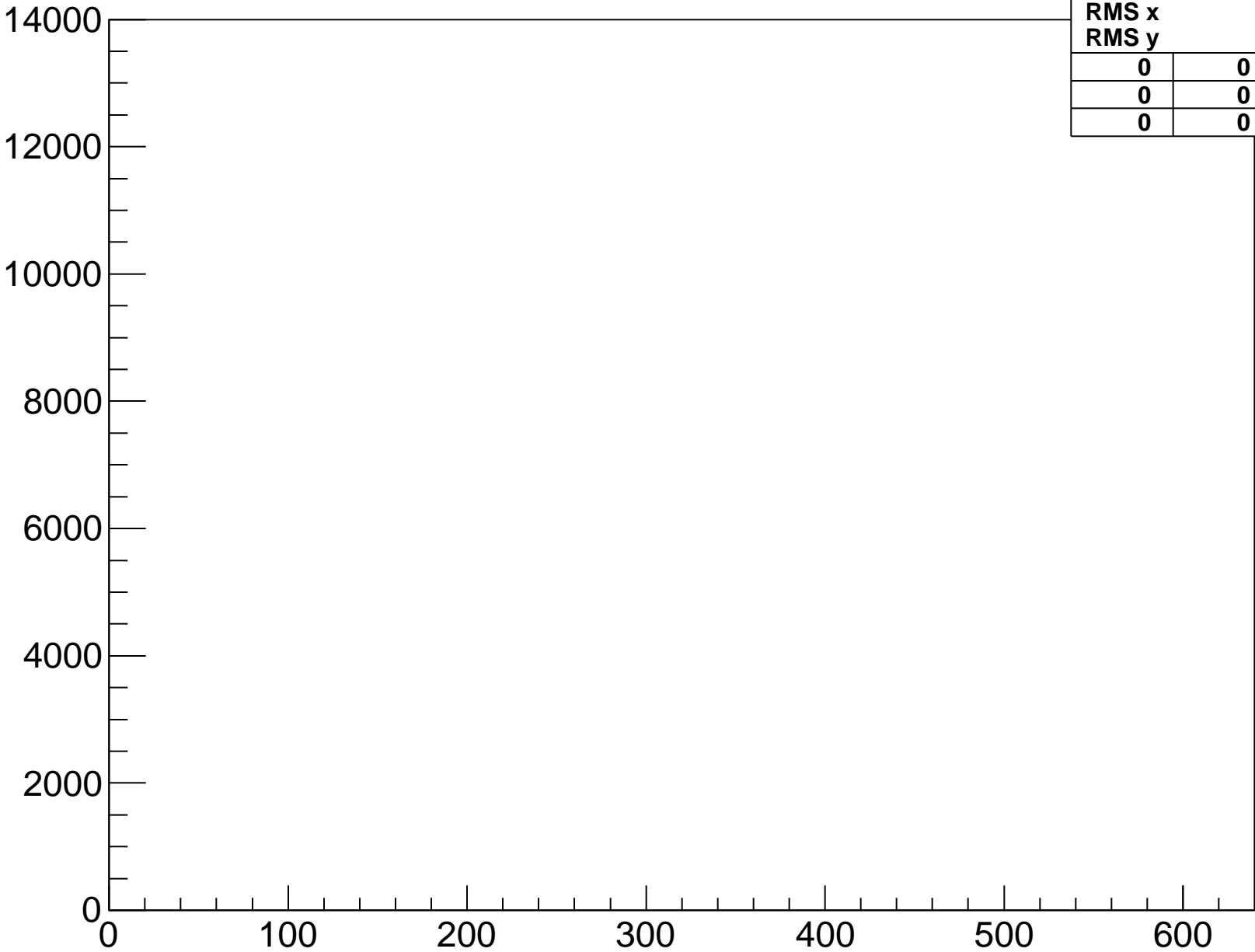


baselinesamples-fpga-1-hyb-1-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

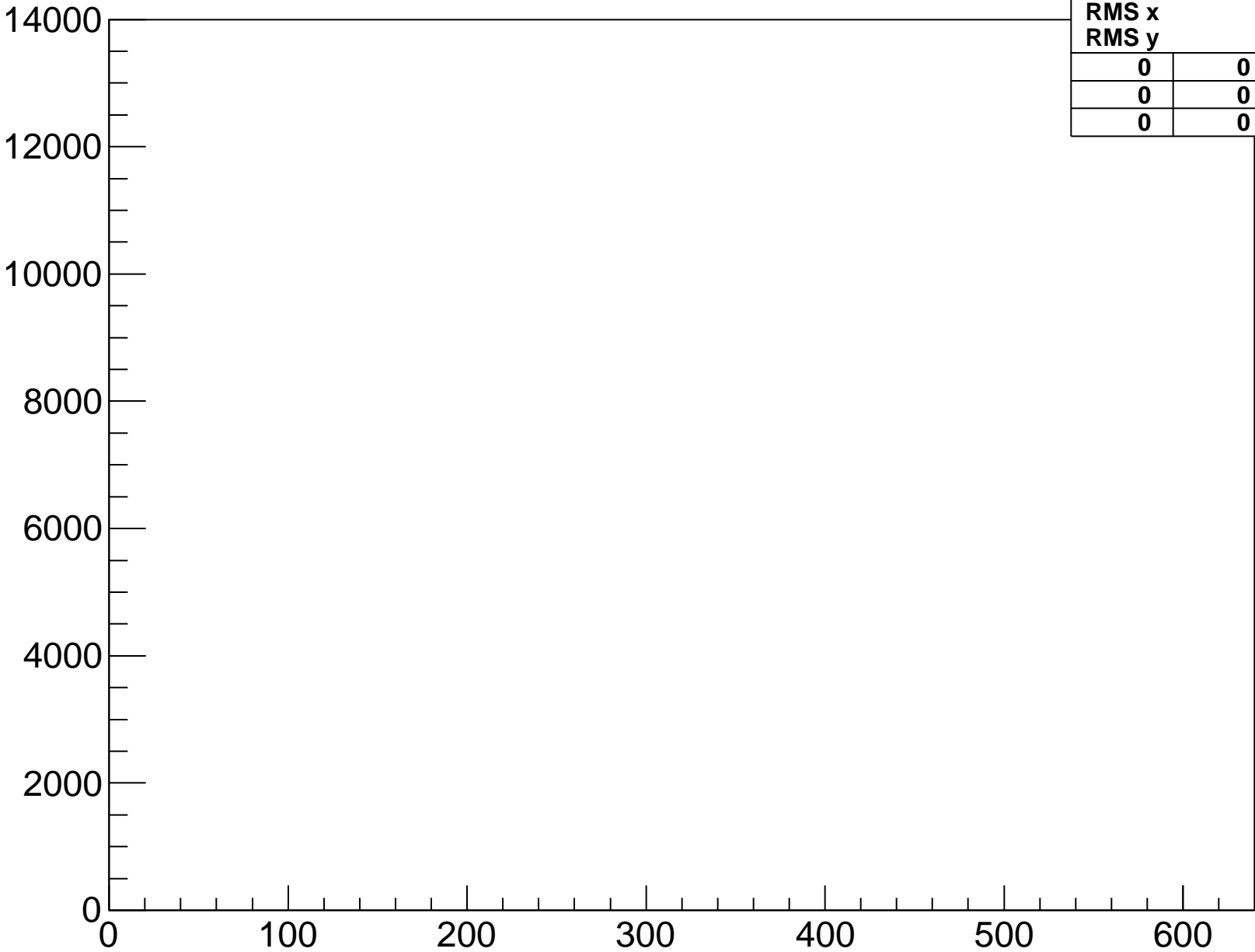


baselinesamples-fpga-1-hyb-1-sample-2



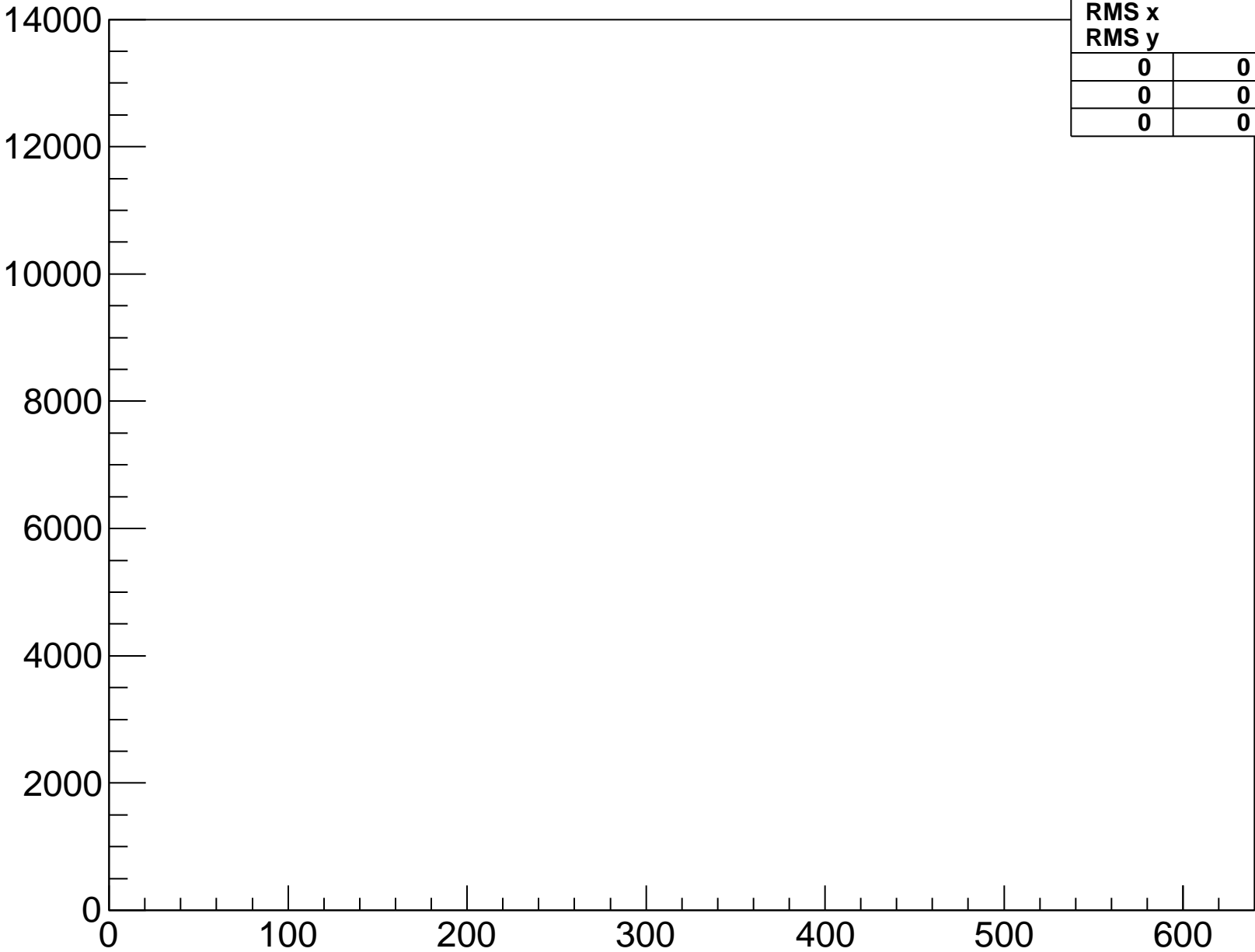
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-1-hyb-1-sample-3



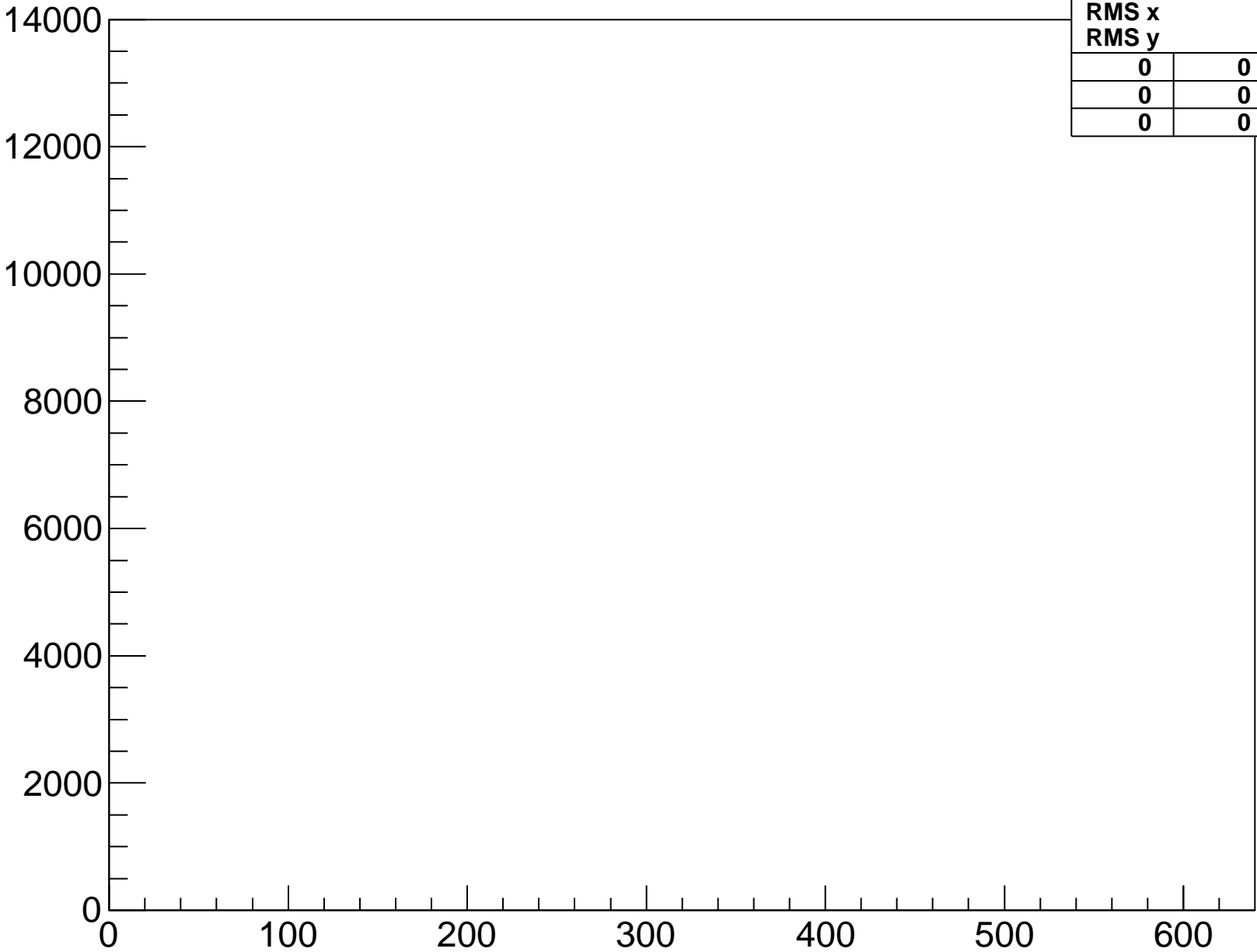
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-1-hyb-1-sample-4



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

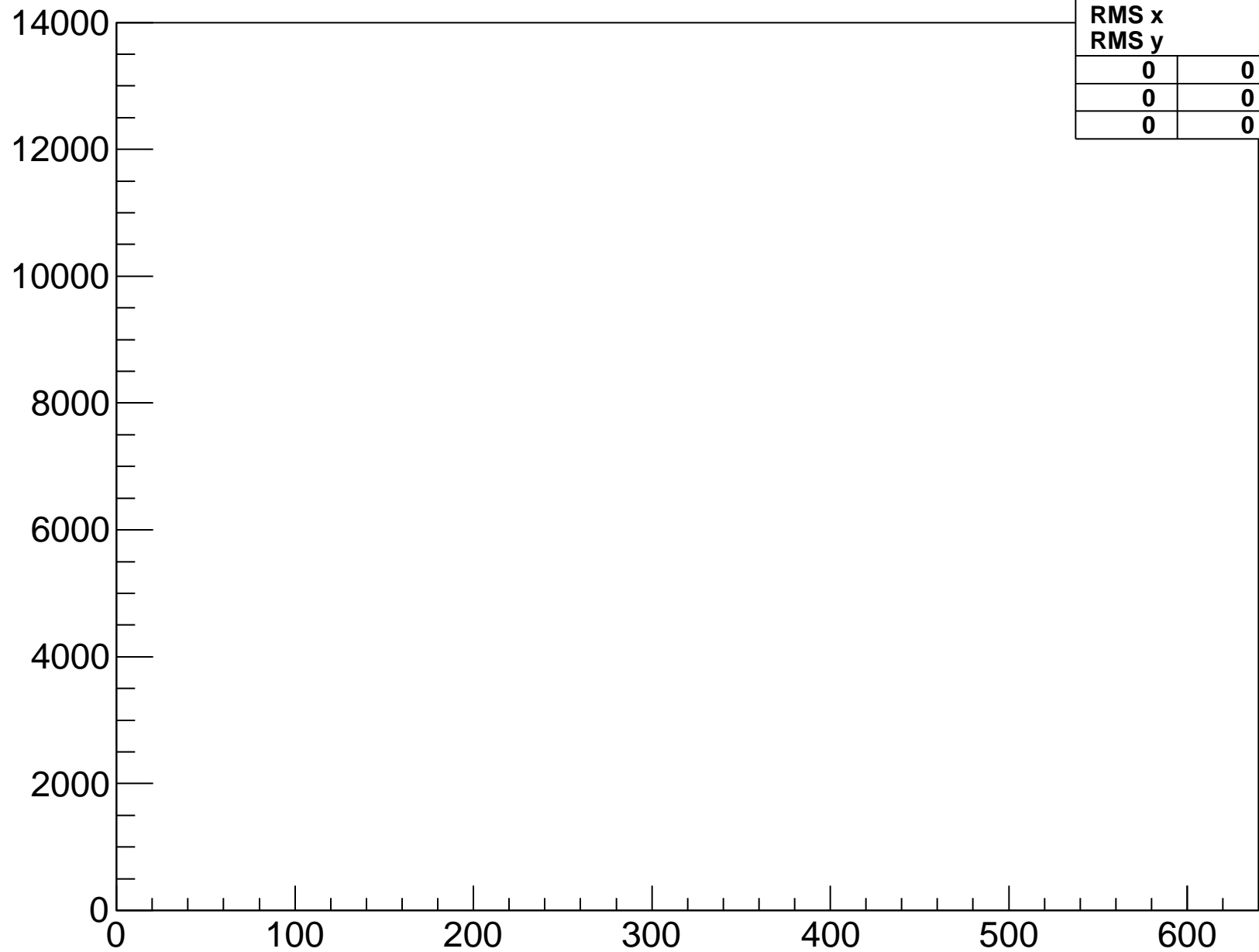
baselinesamples-fpga-1-hyb-1-sample-5



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

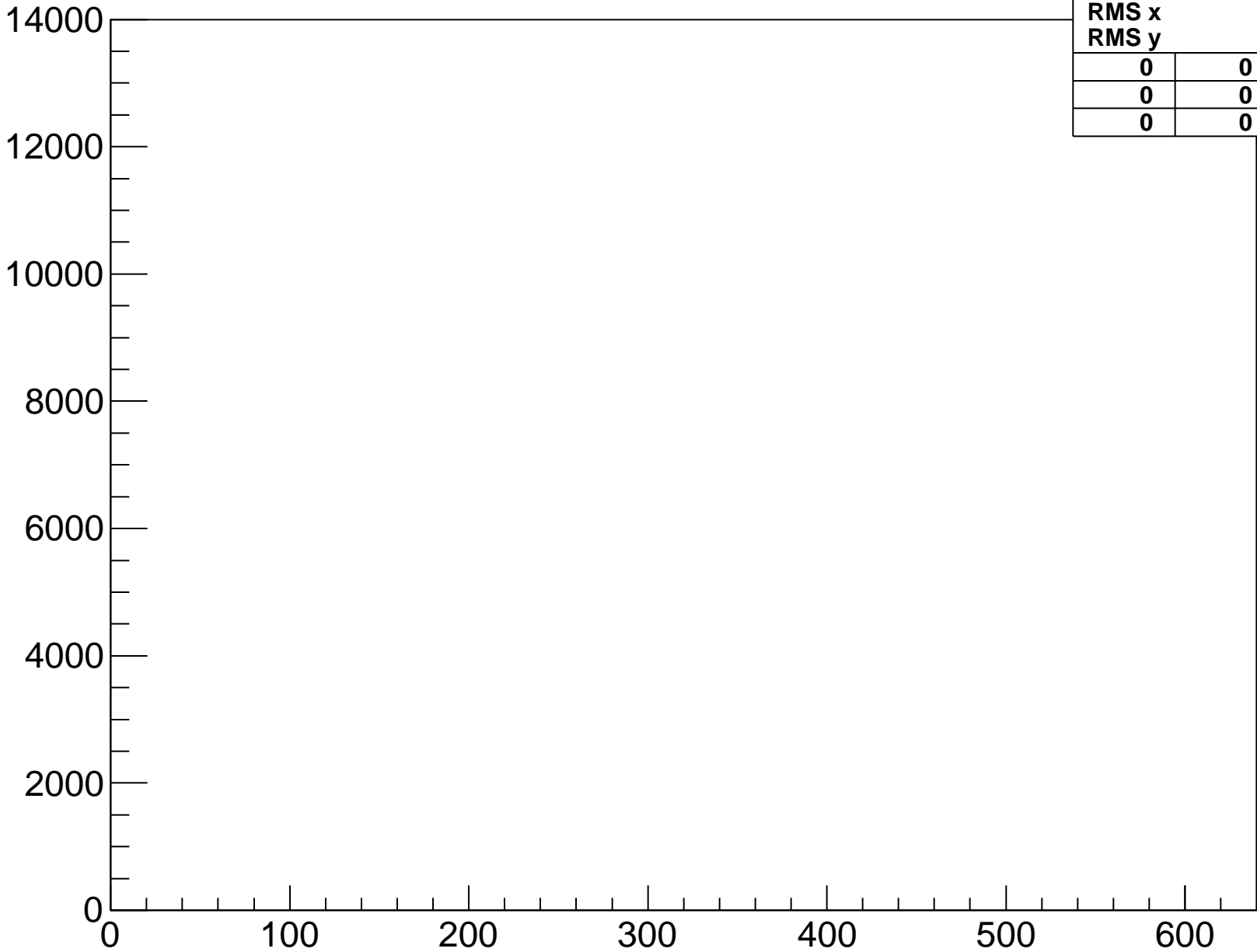
baselinesamples-fpga-1-hyb-2-sample-0

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

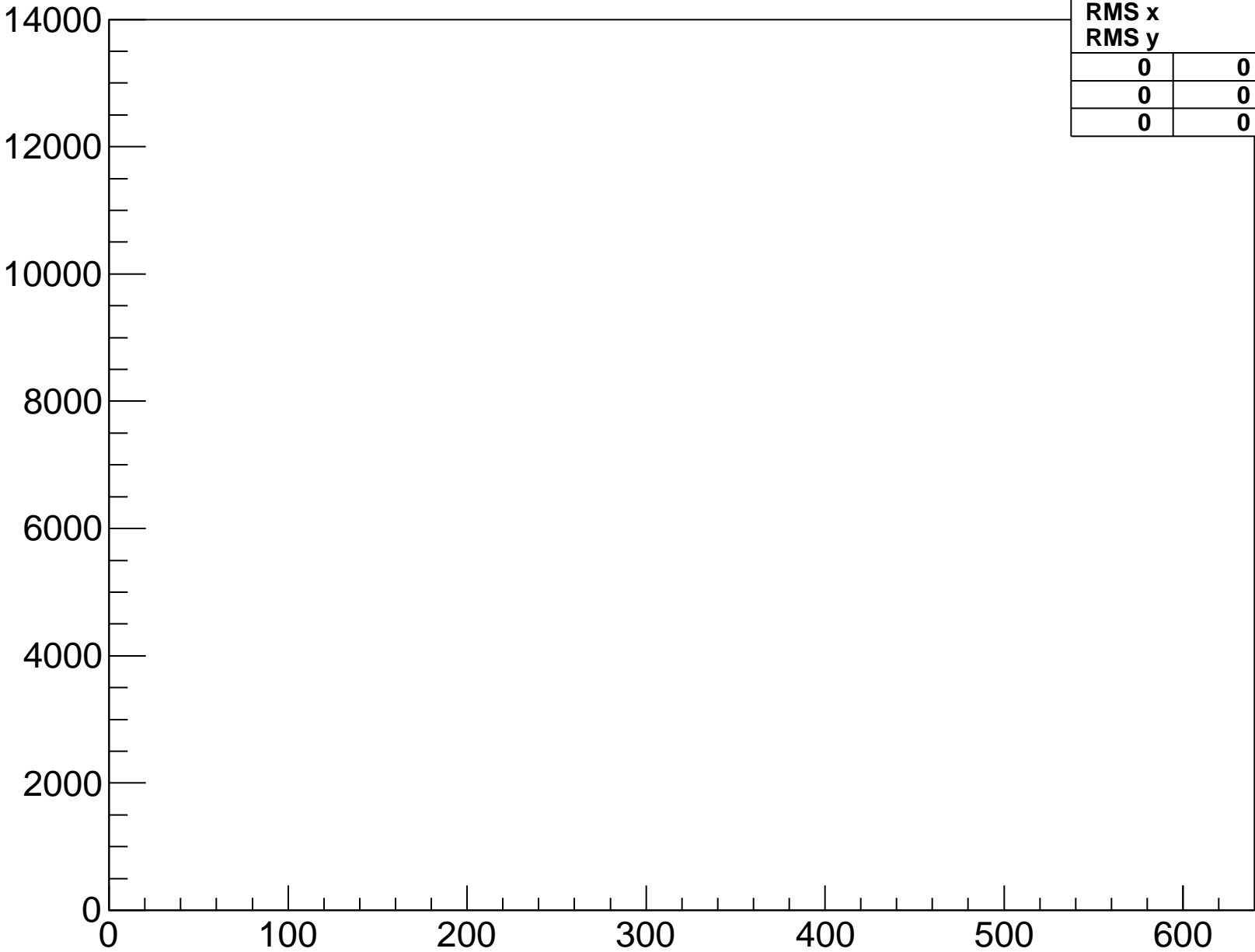


baselinesamples-fpga-1-hyb-2-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



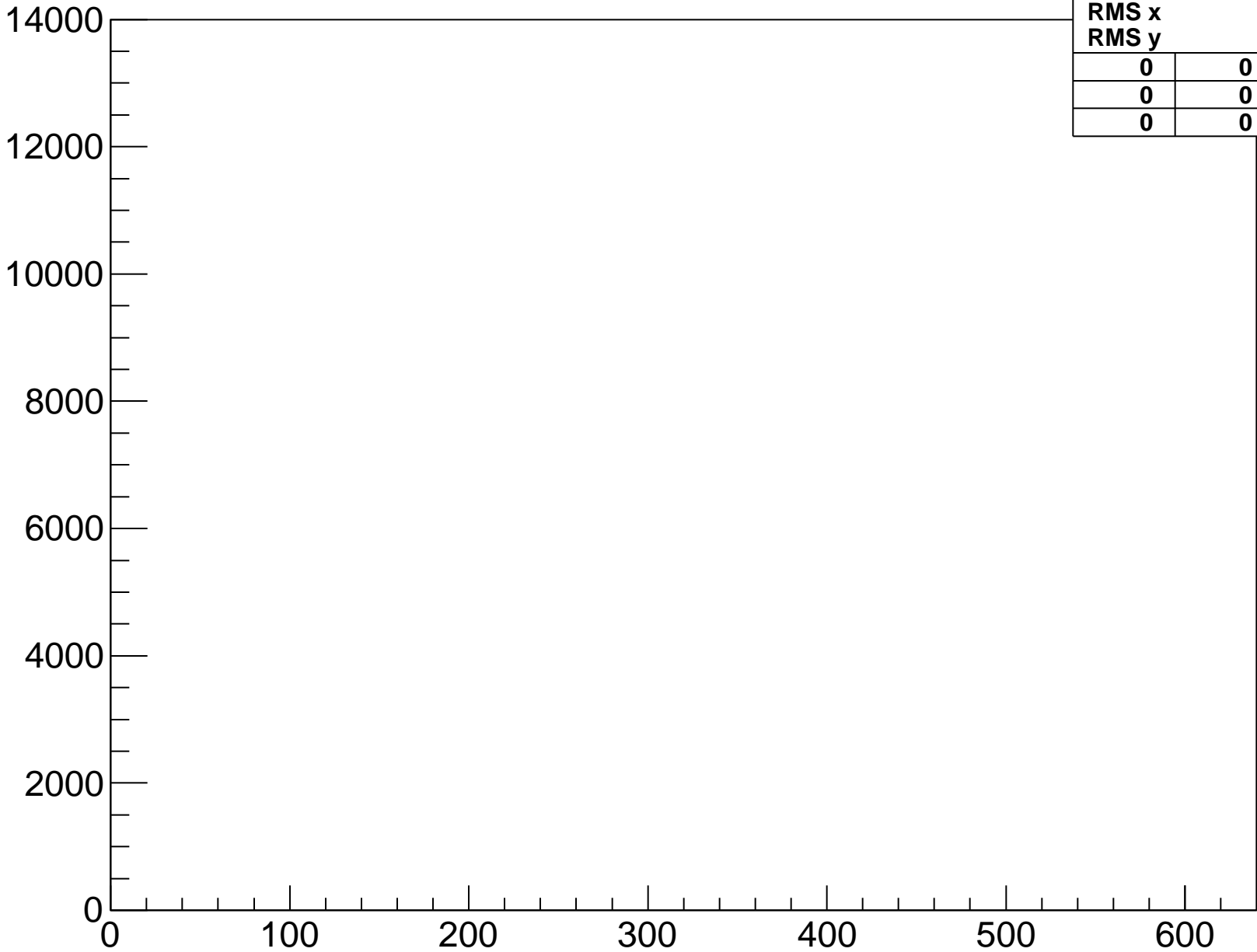
baselinesamples-fpga-1-hyb-2-sample-2



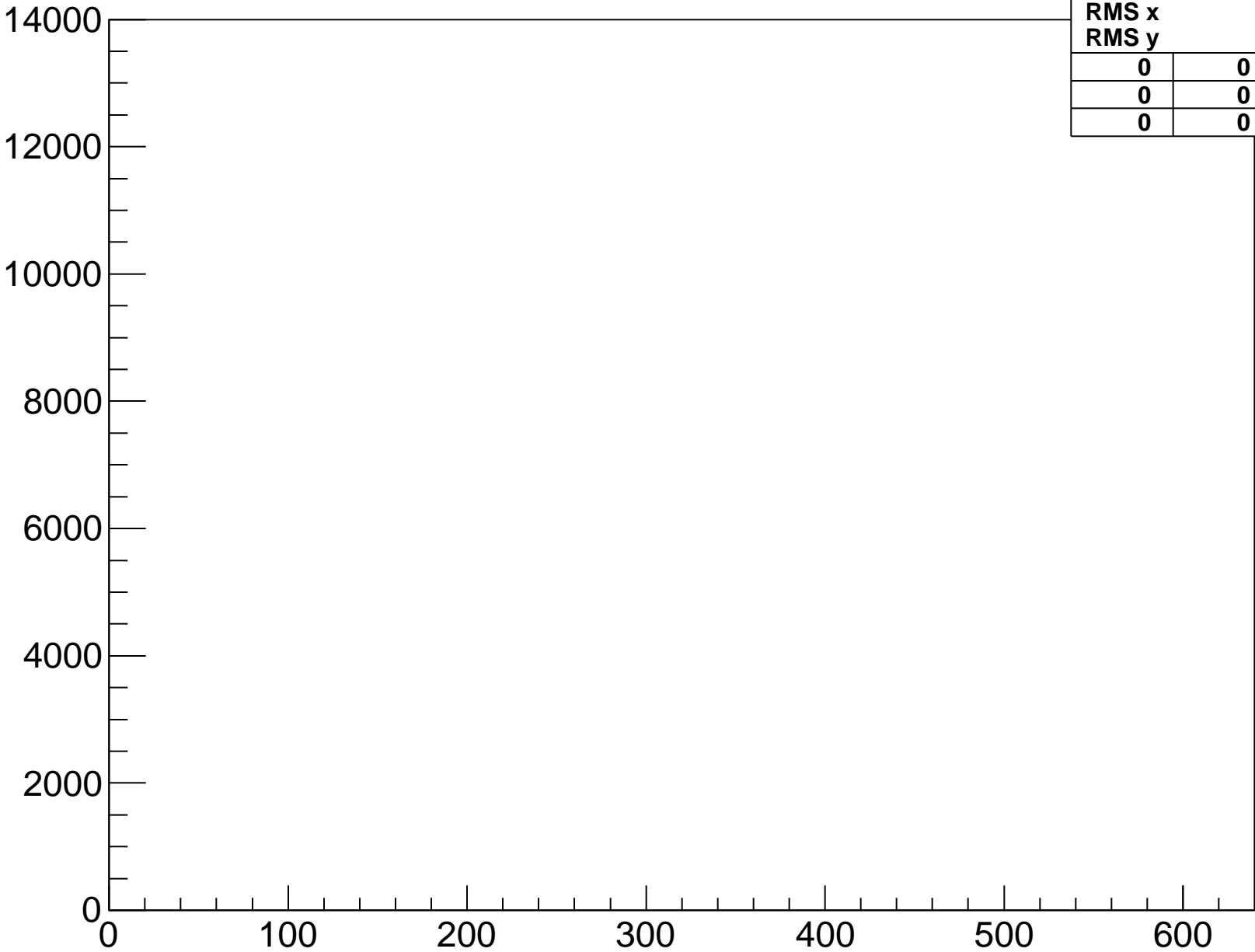
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-1-hyb-2-sample-3

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

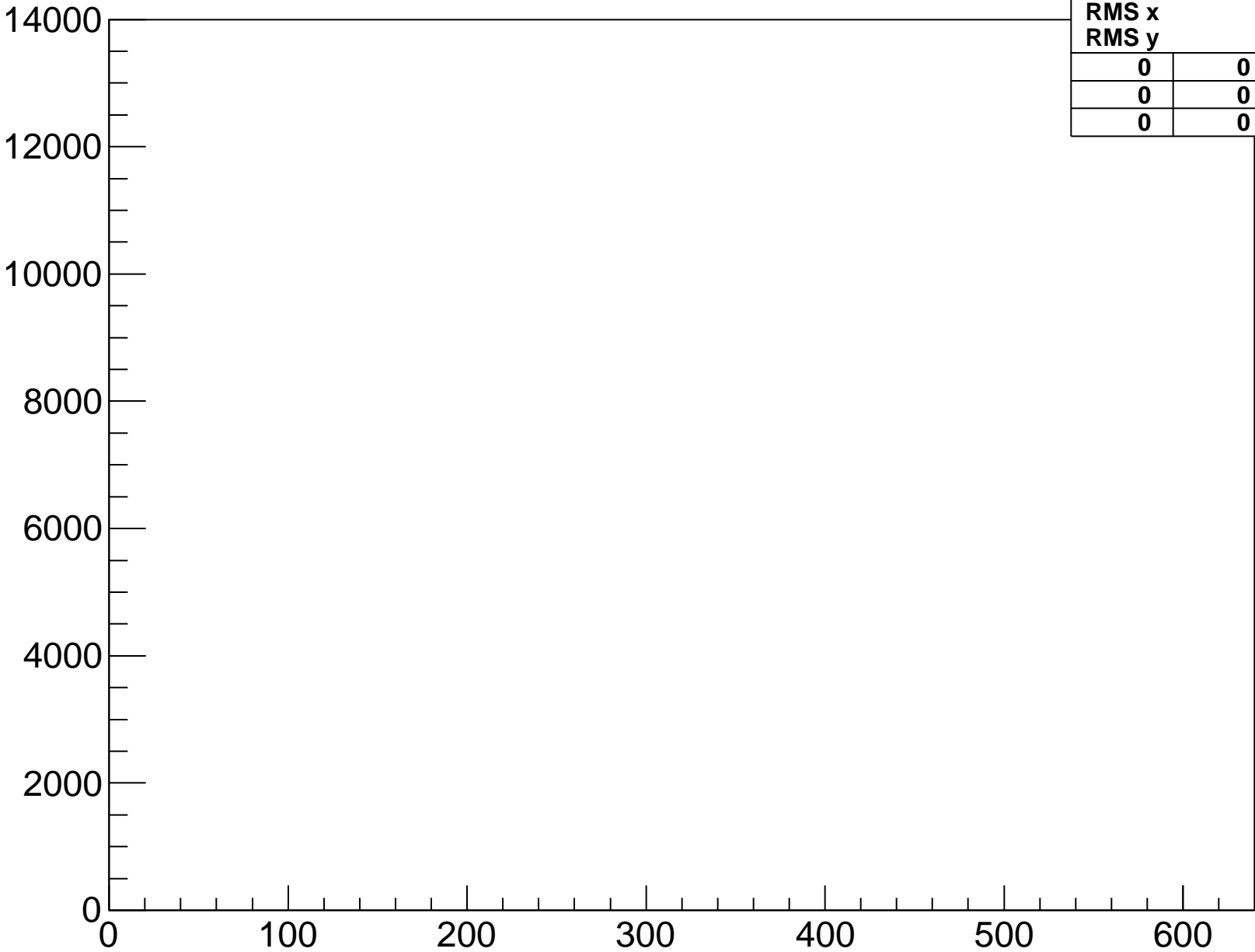


baselinesamples-fpga-1-hyb-2-sample-4



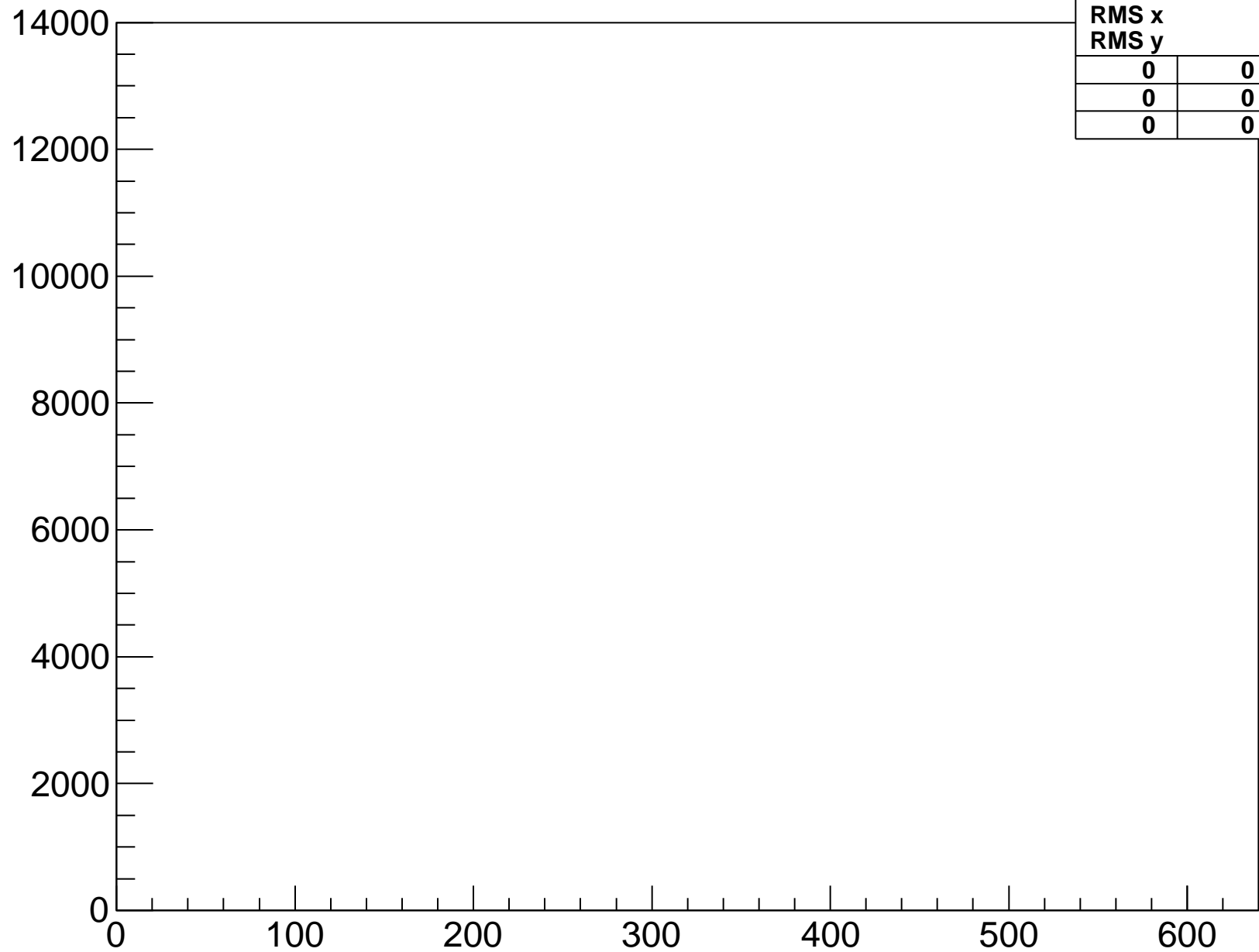
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-1-hyb-2-sample-5



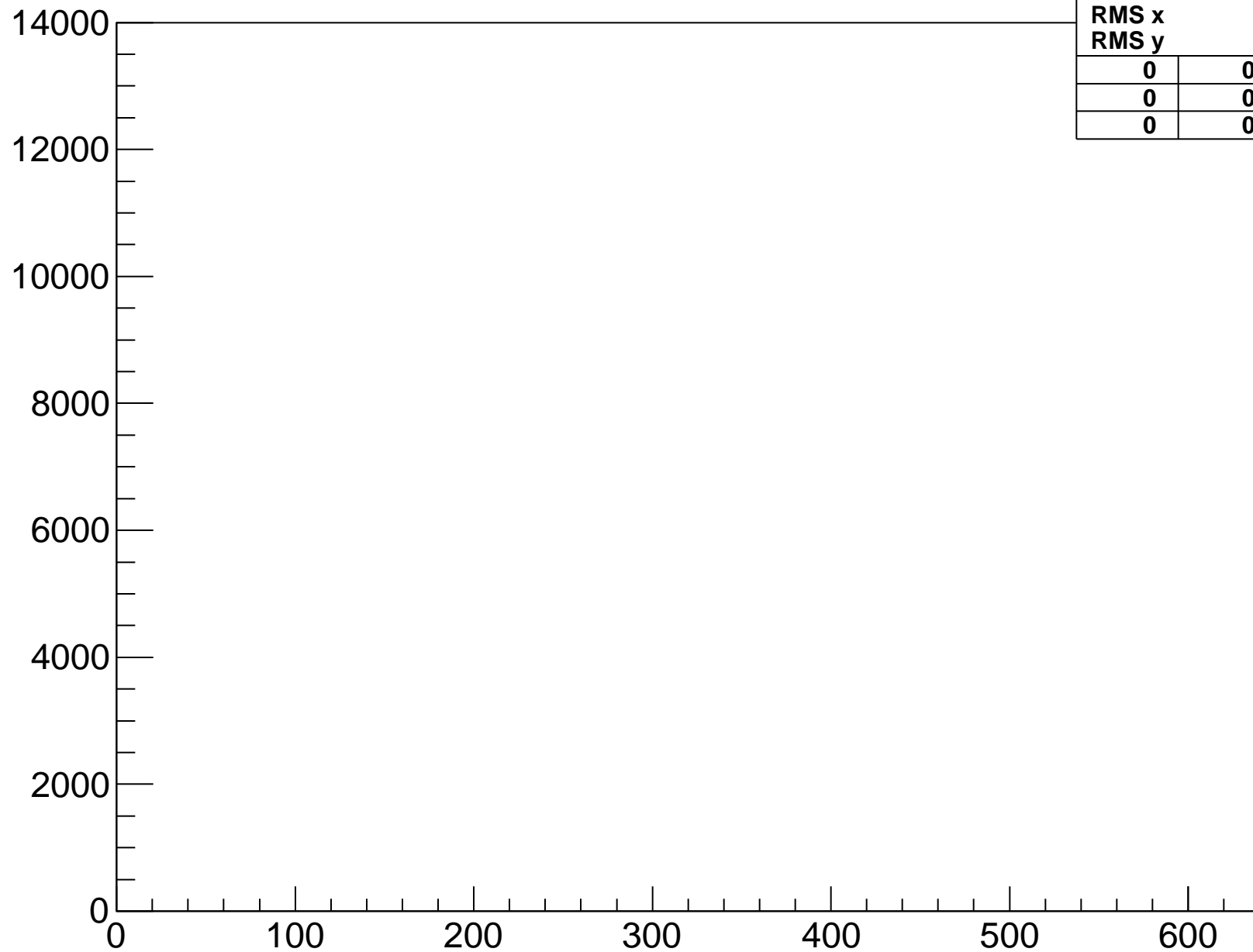
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-1-hyb-3-sample-0



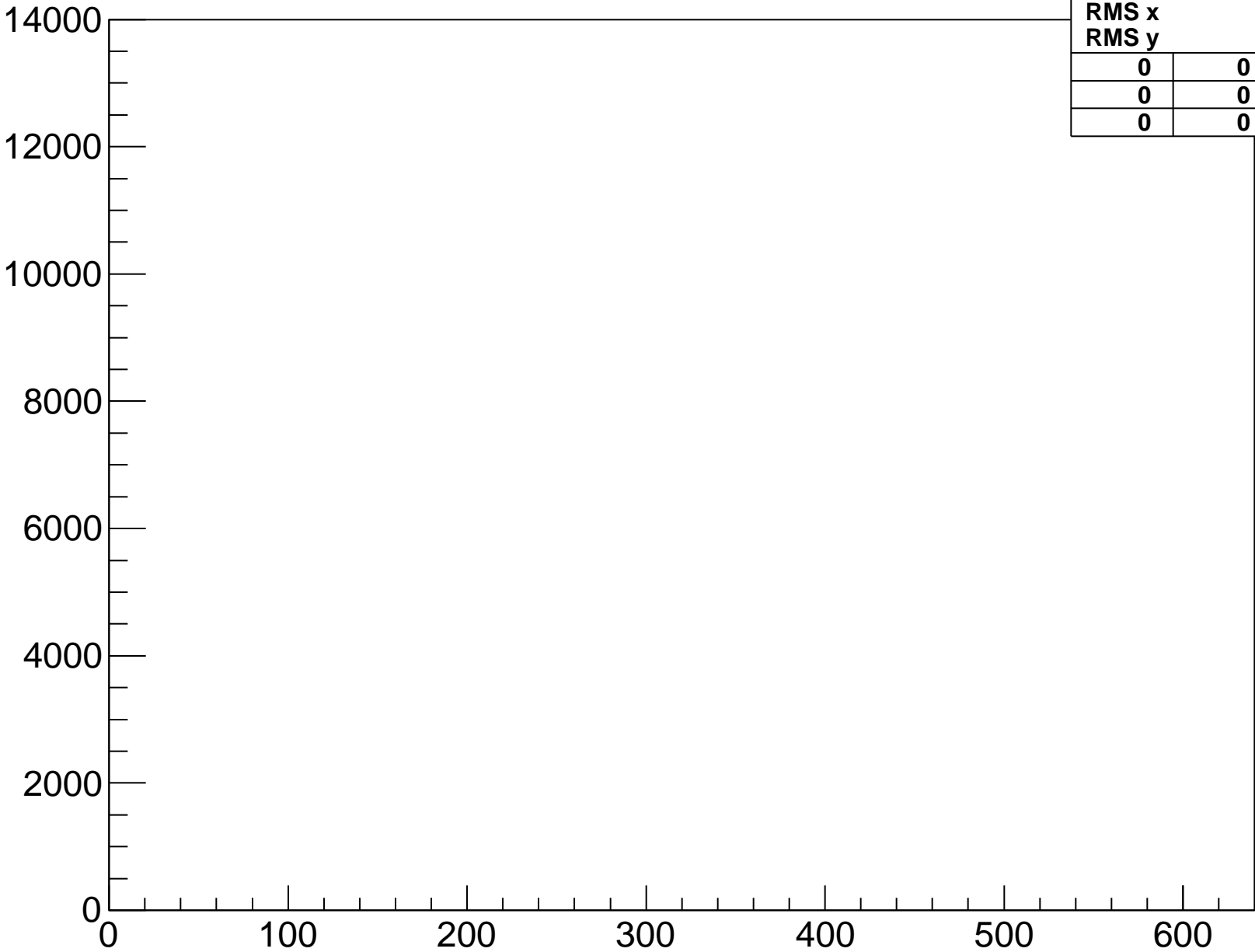
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-1-hyb-3-sample-1



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

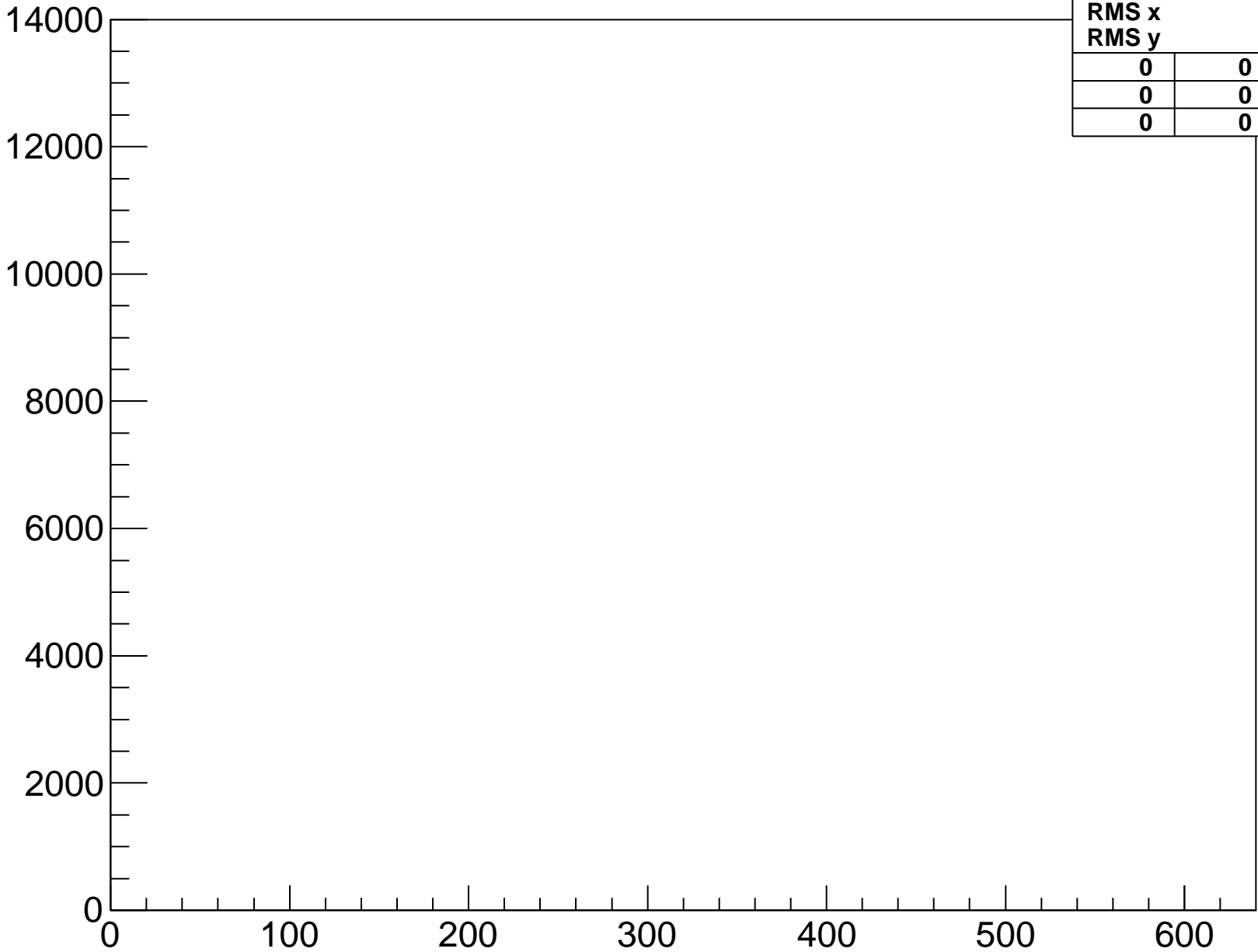
baselinesamples-fpga-1-hyb-3-sample-2



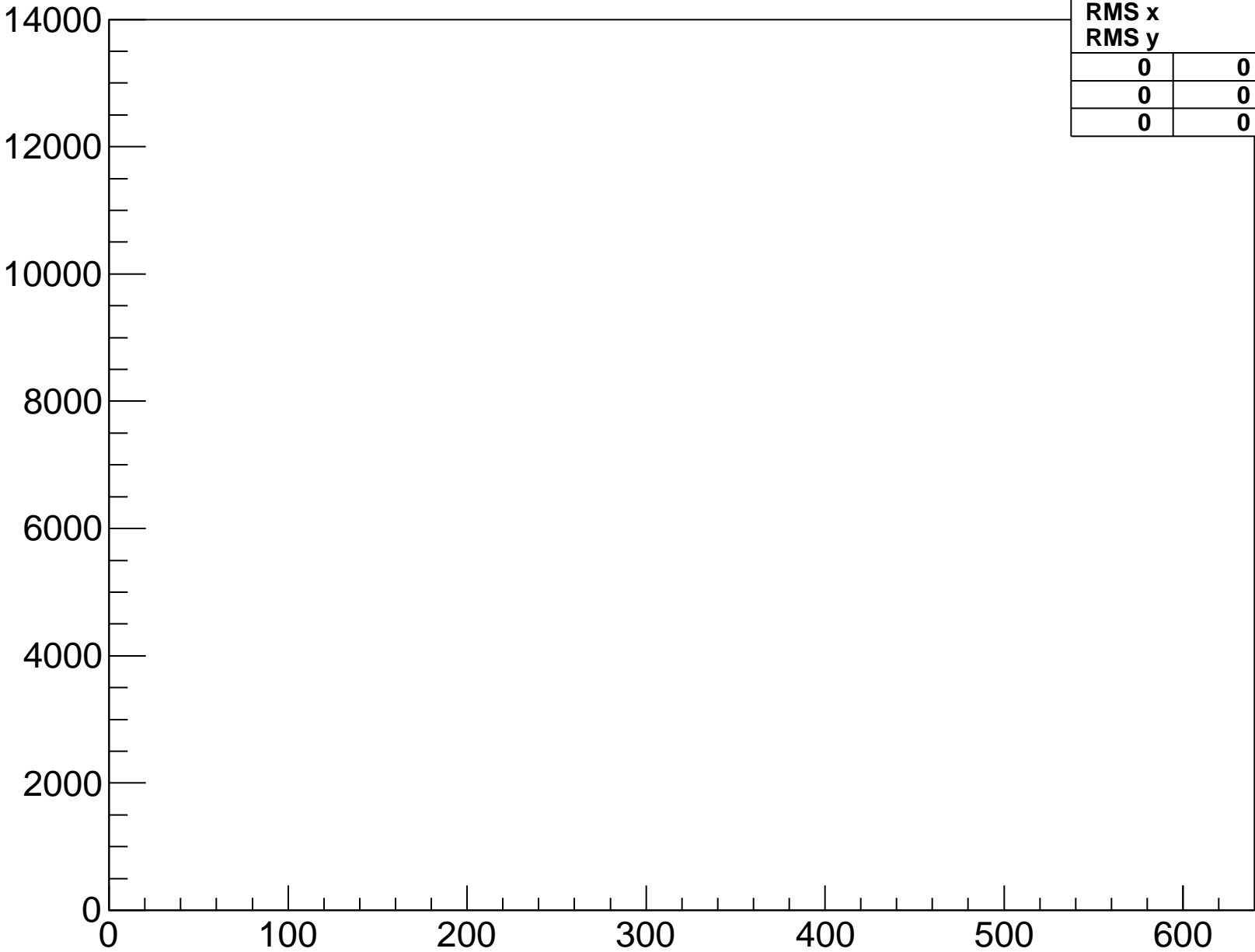
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-1-hyb-3-sample-3

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

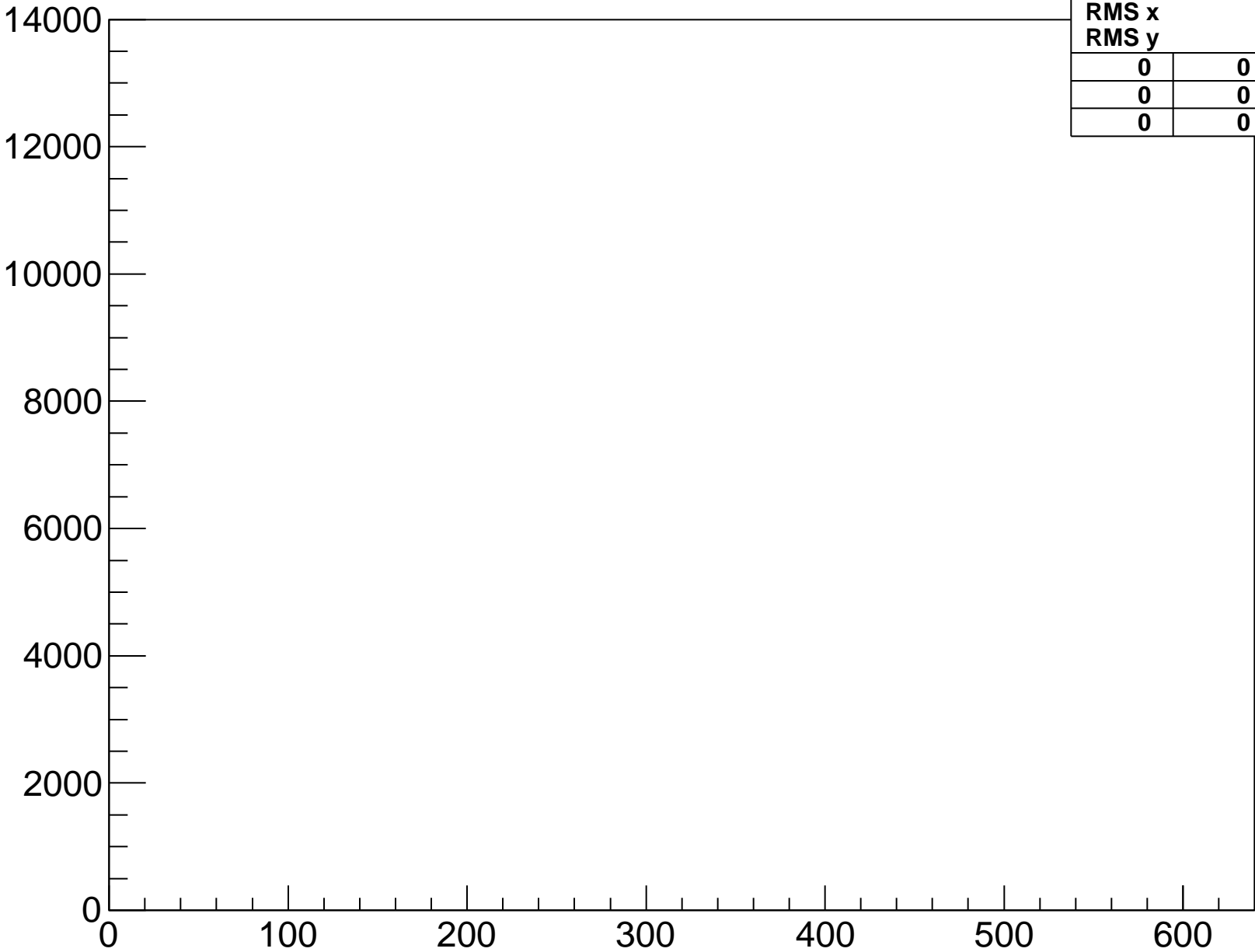


baselinesamples-fpga-1-hyb-3-sample-4



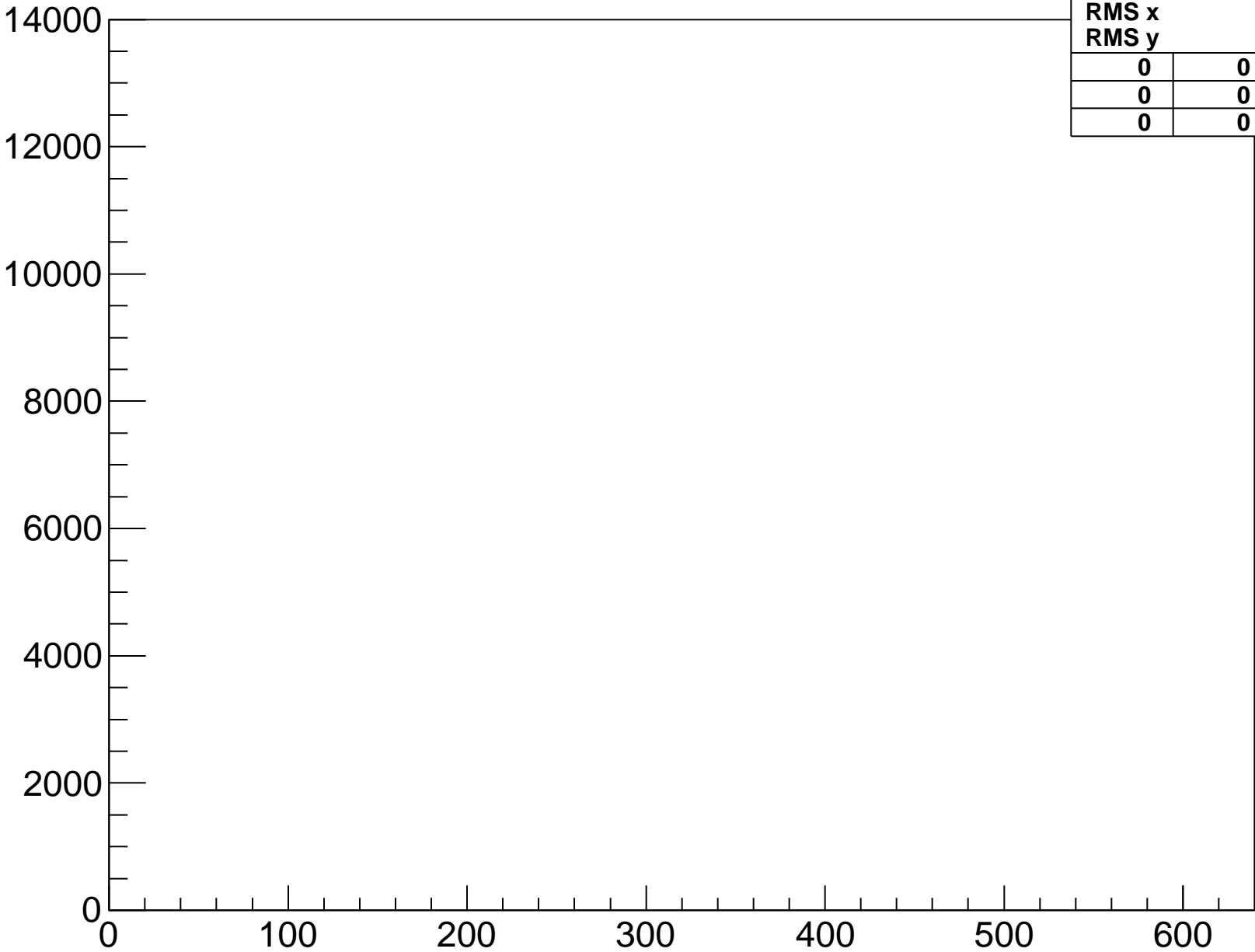
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-1-hyb-3-sample-5



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

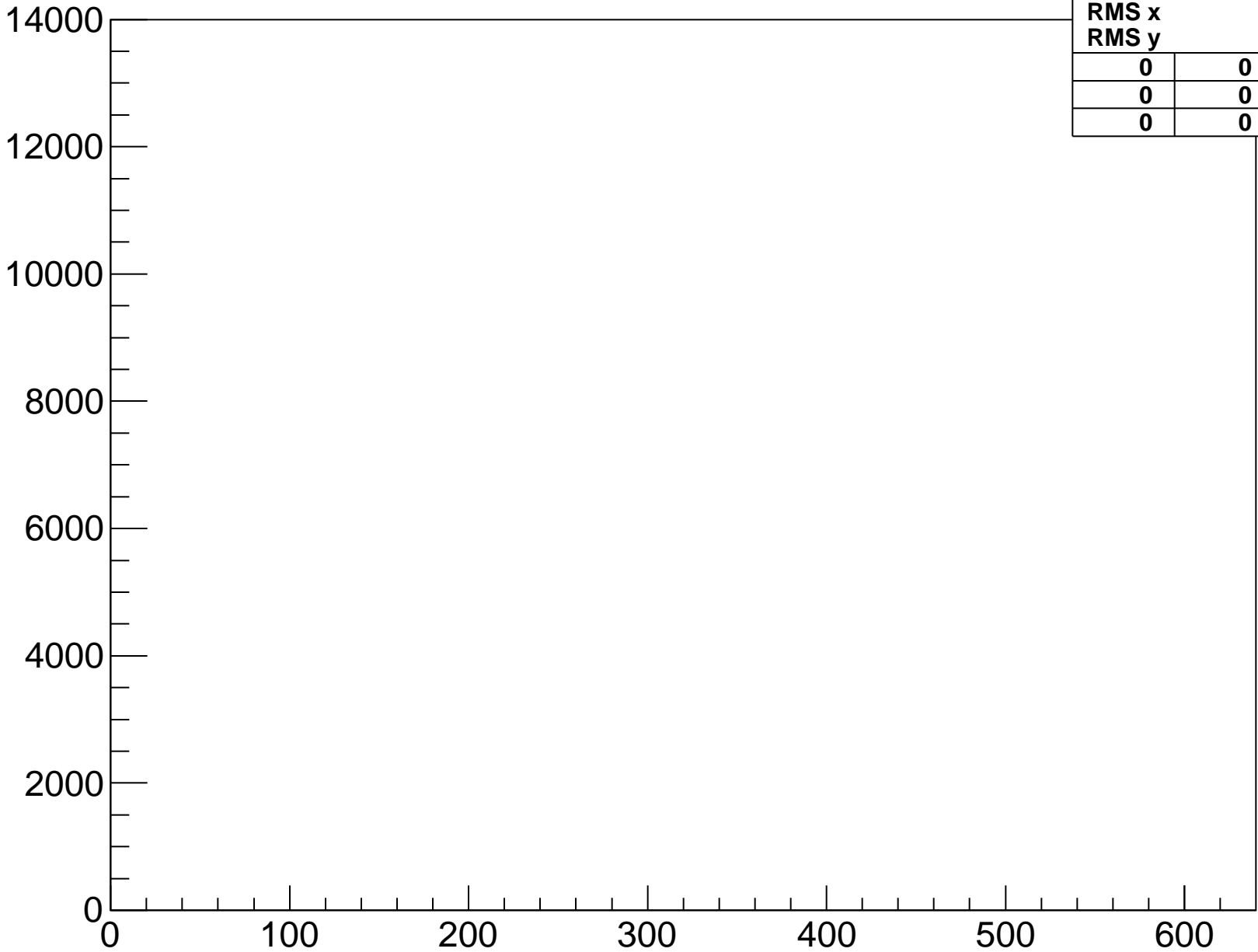
baselinesamples-fpga-2-hyb-0-sample-0



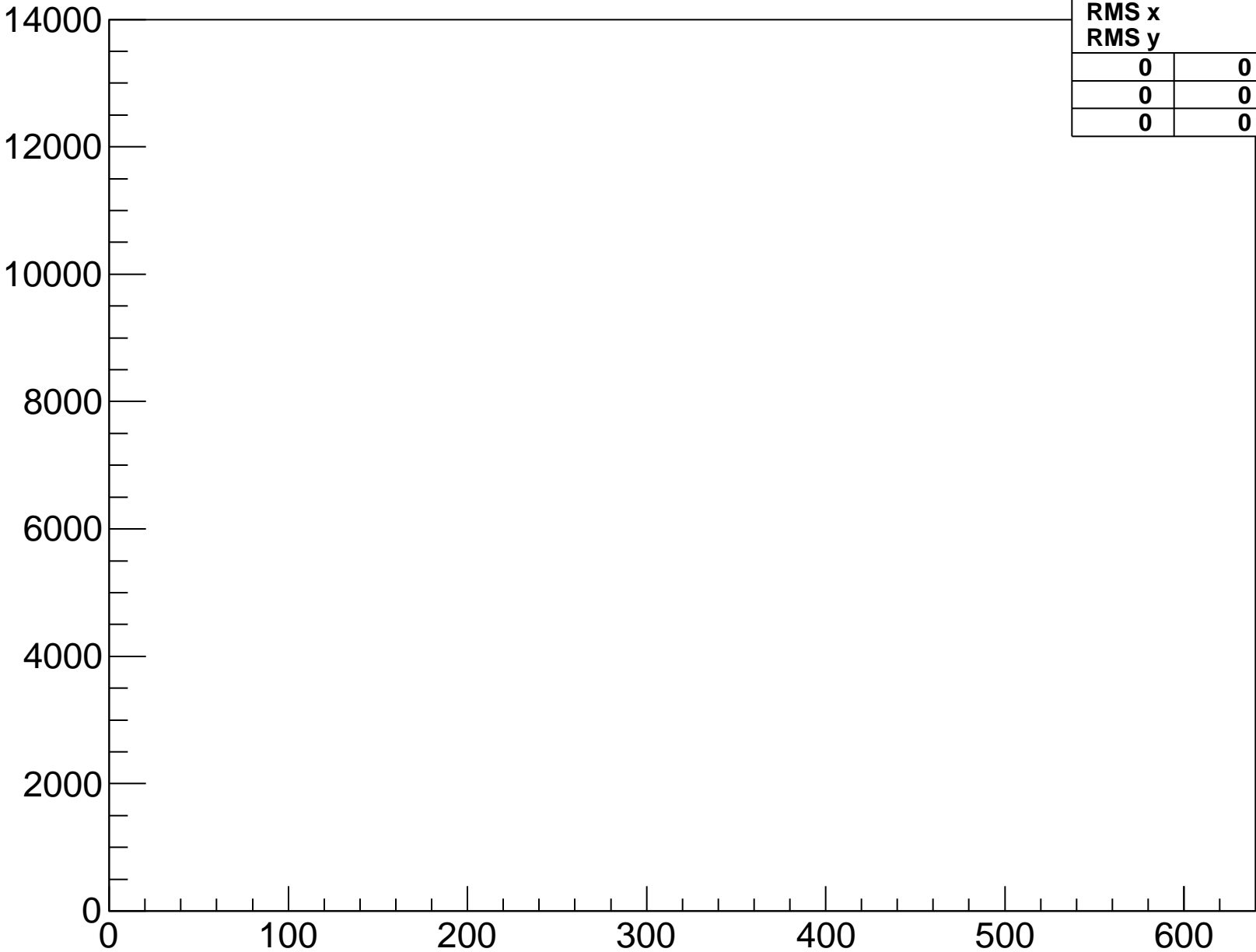
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-2-hyb-0-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

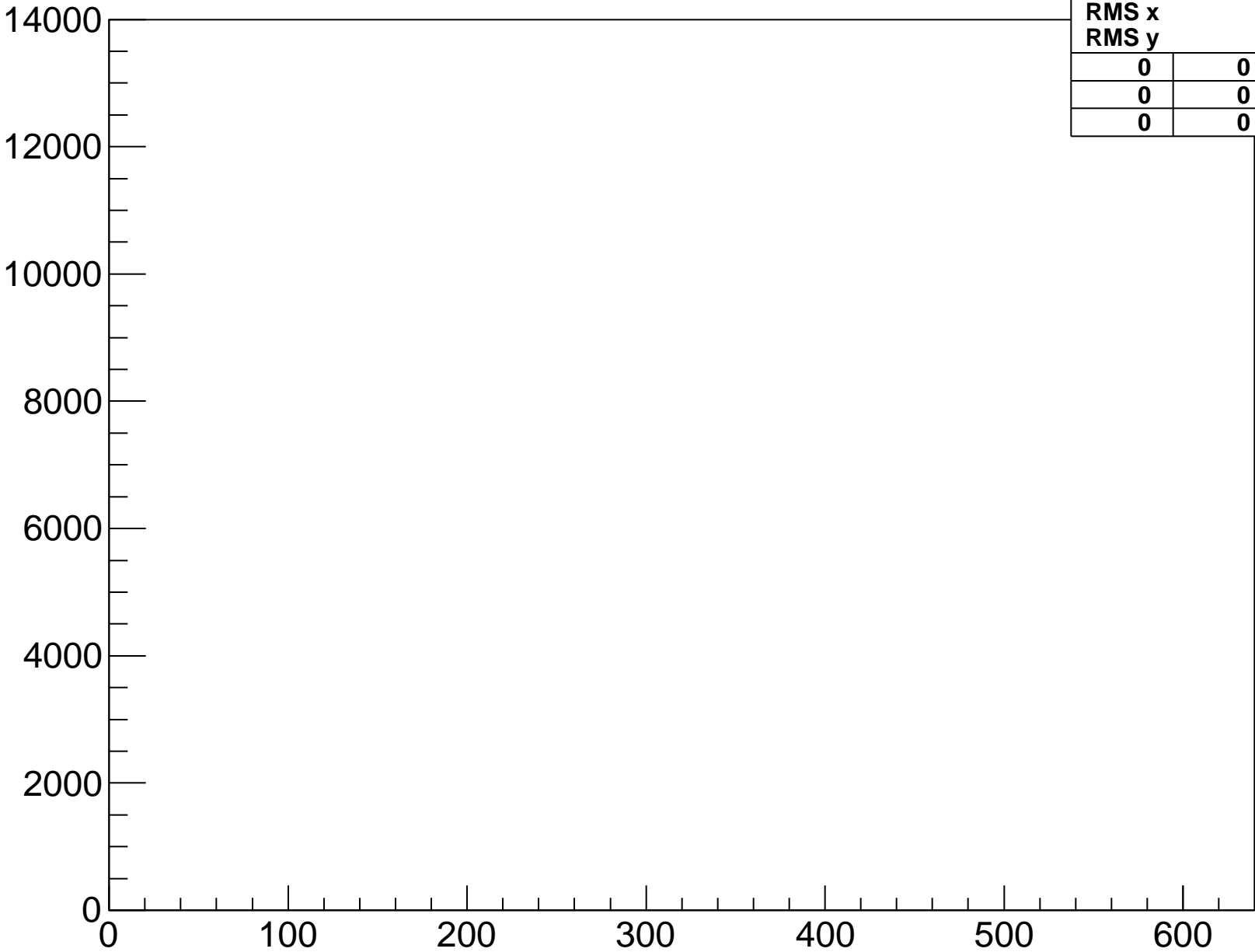


baselinesamples-fpga-2-hyb-0-sample-2



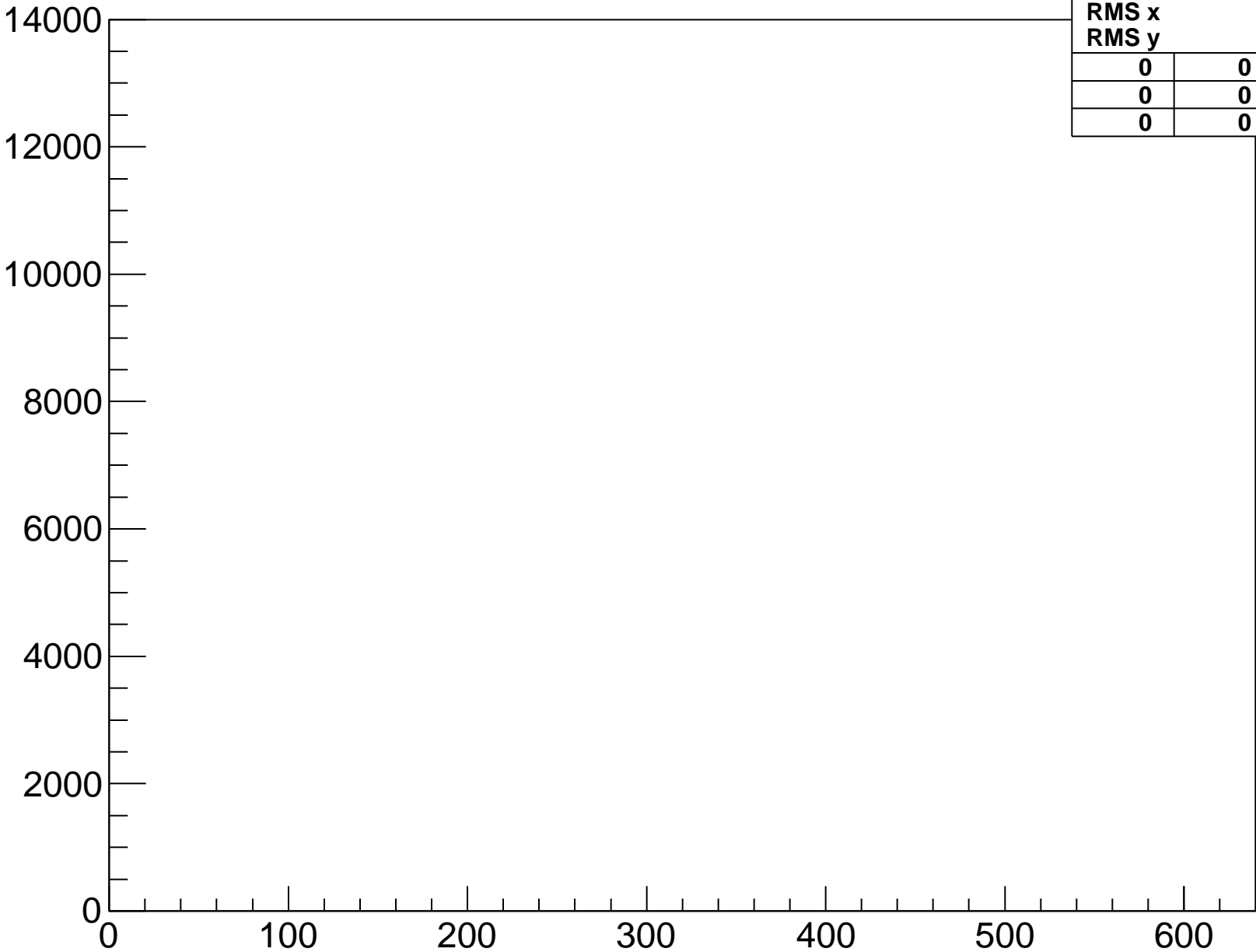
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-2-hyb-0-sample-3



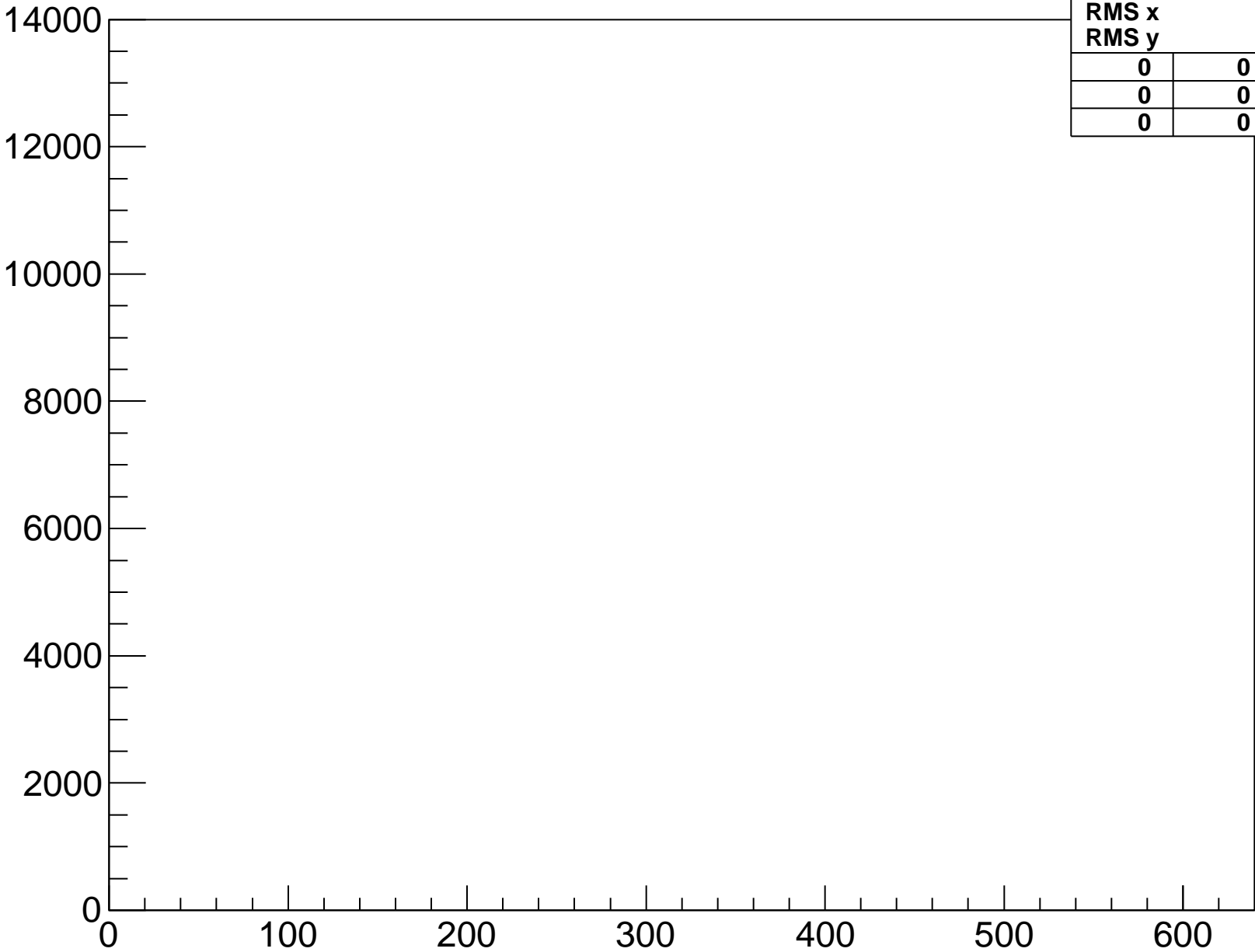
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-2-hyb-0-sample-4



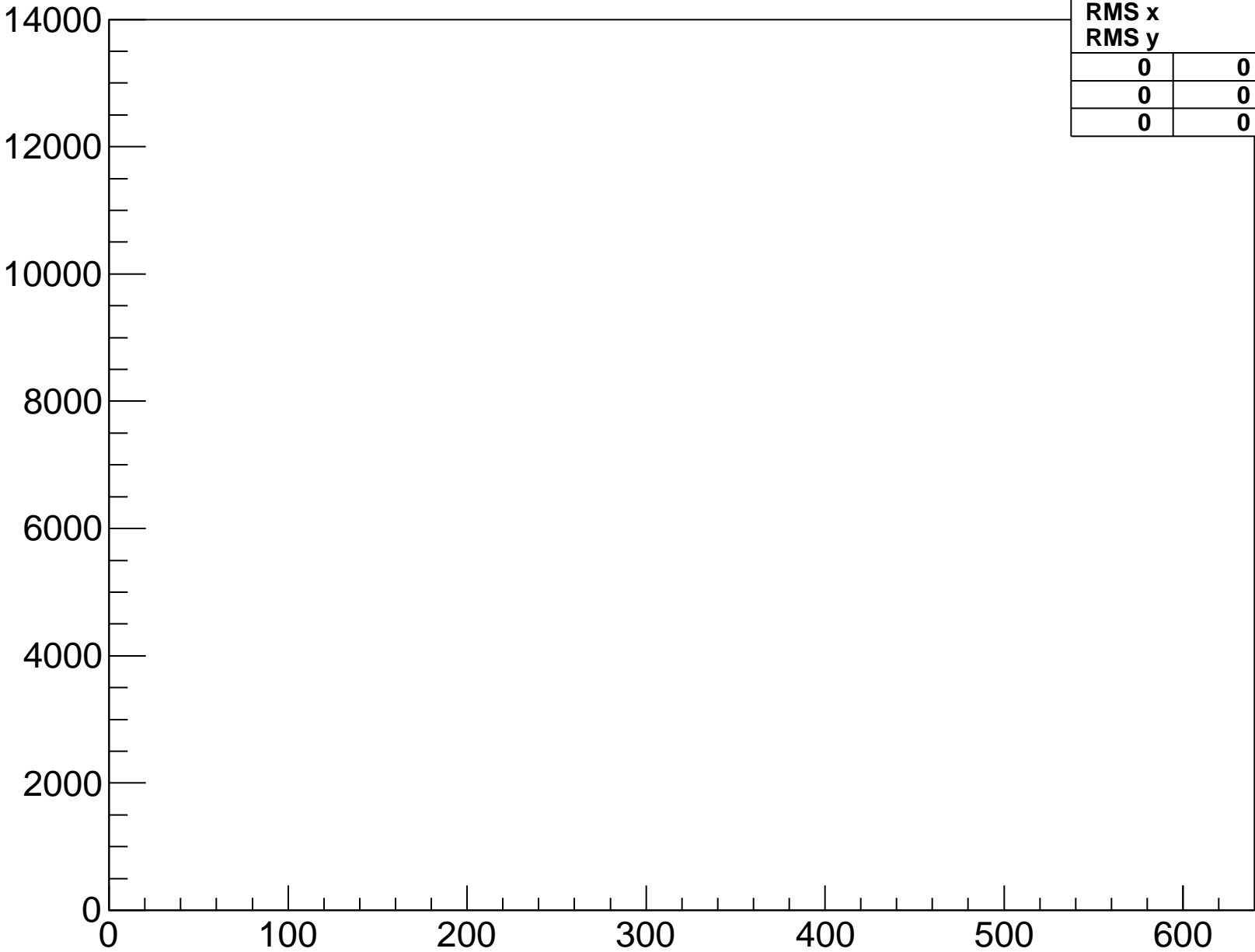
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-2-hyb-0-sample-5



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

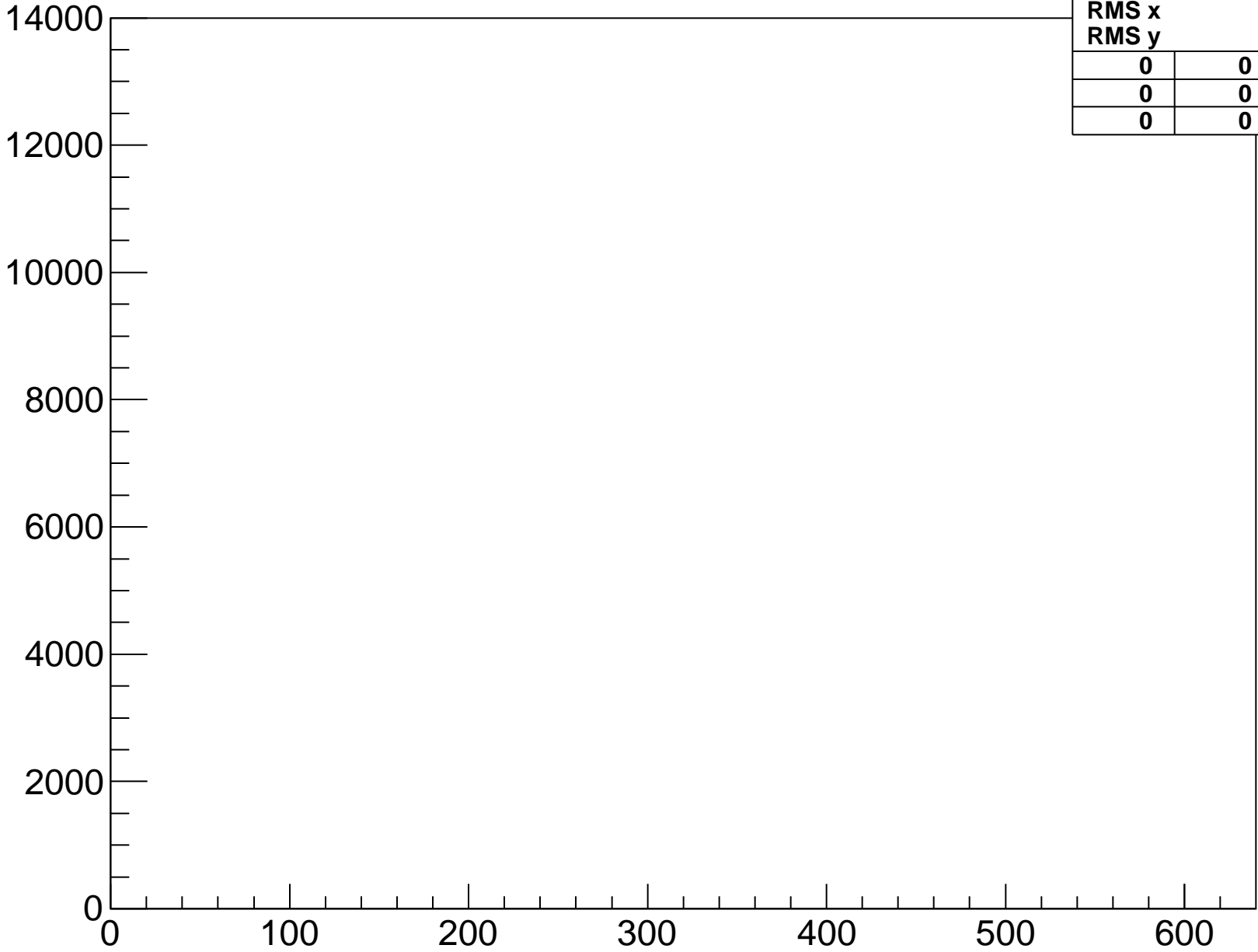
baselinesamples-fpga-2-hyb-1-sample-0



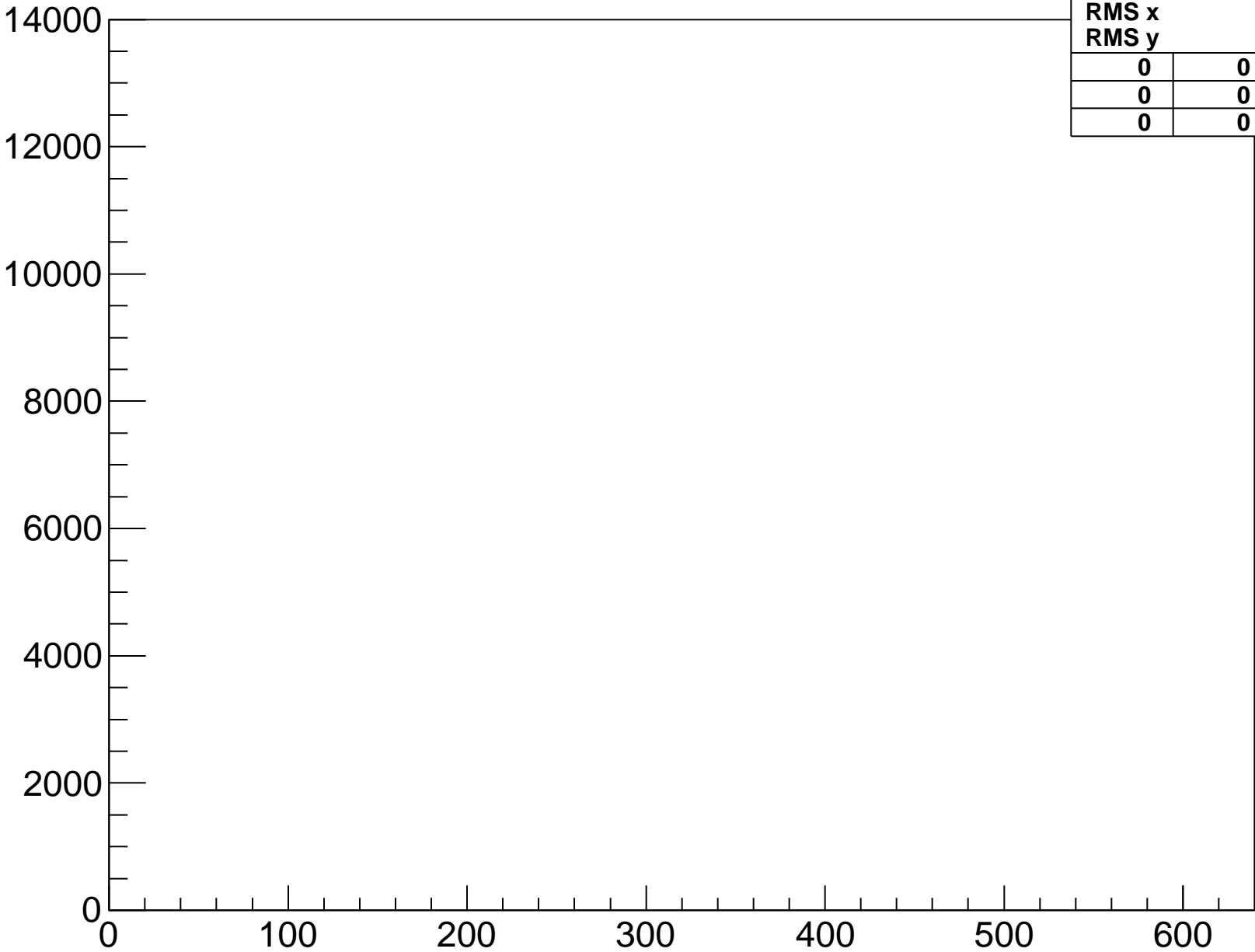
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-2-hyb-1-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

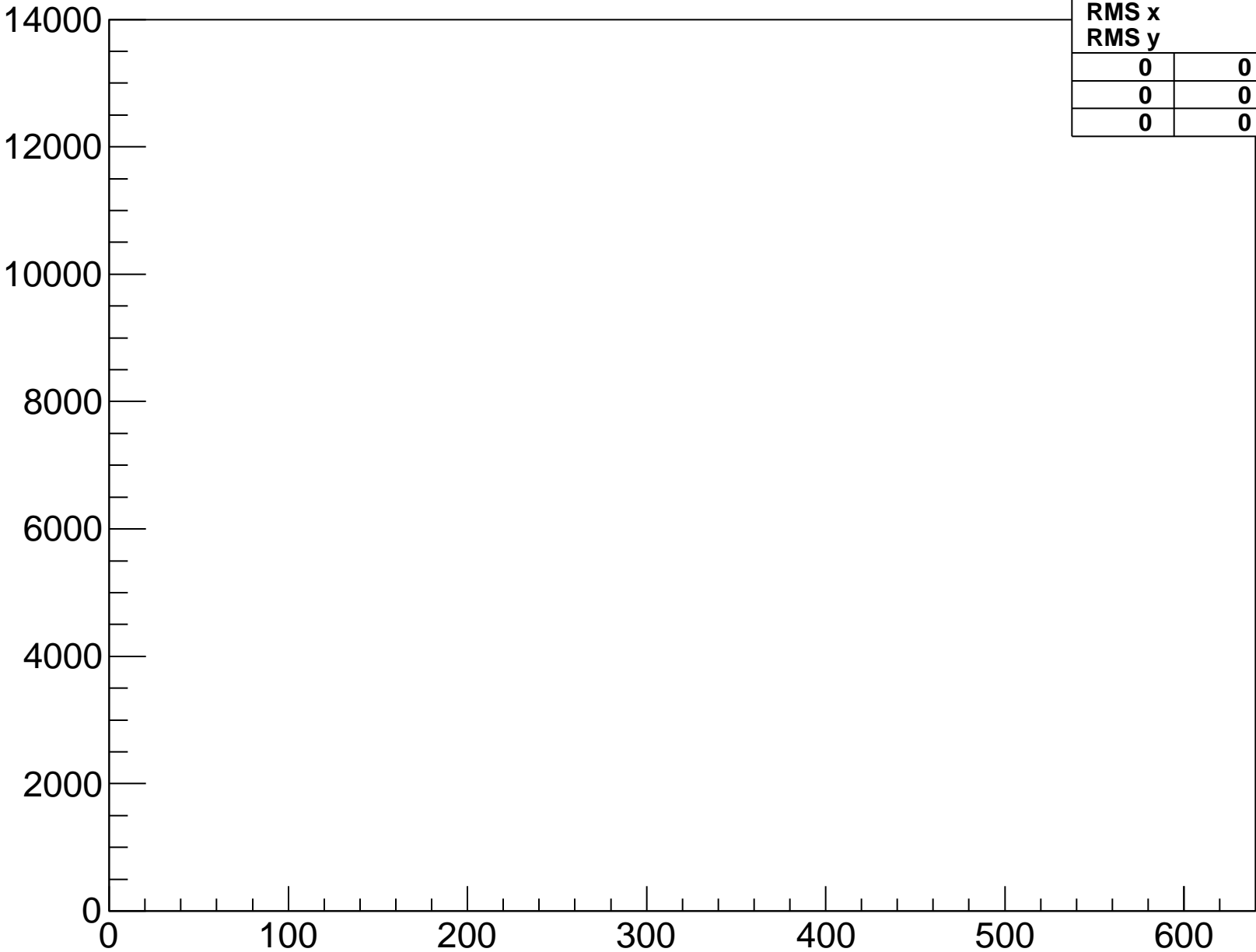


baselinesamples-fpga-2-hyb-1-sample-2



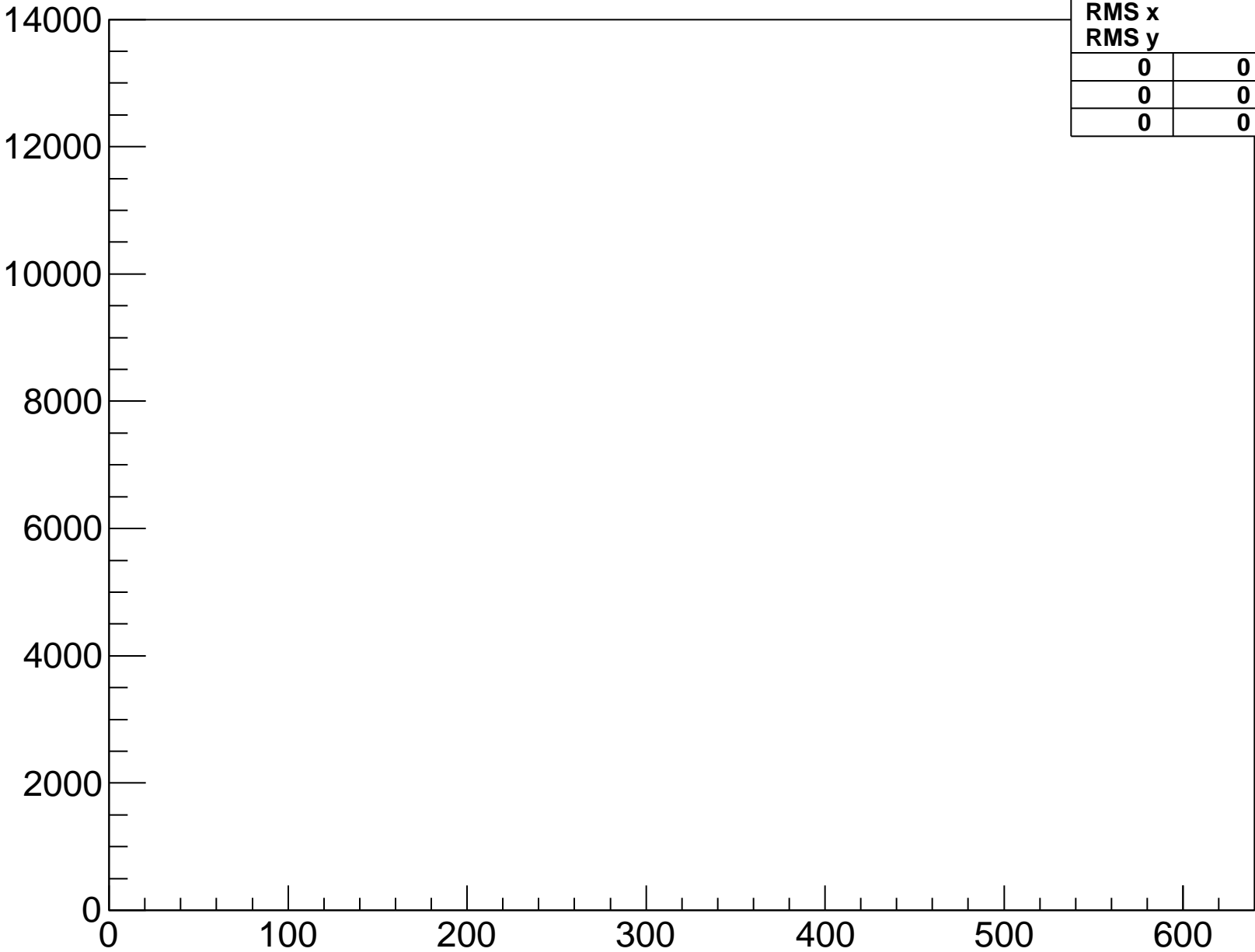
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-2-hyb-1-sample-3



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

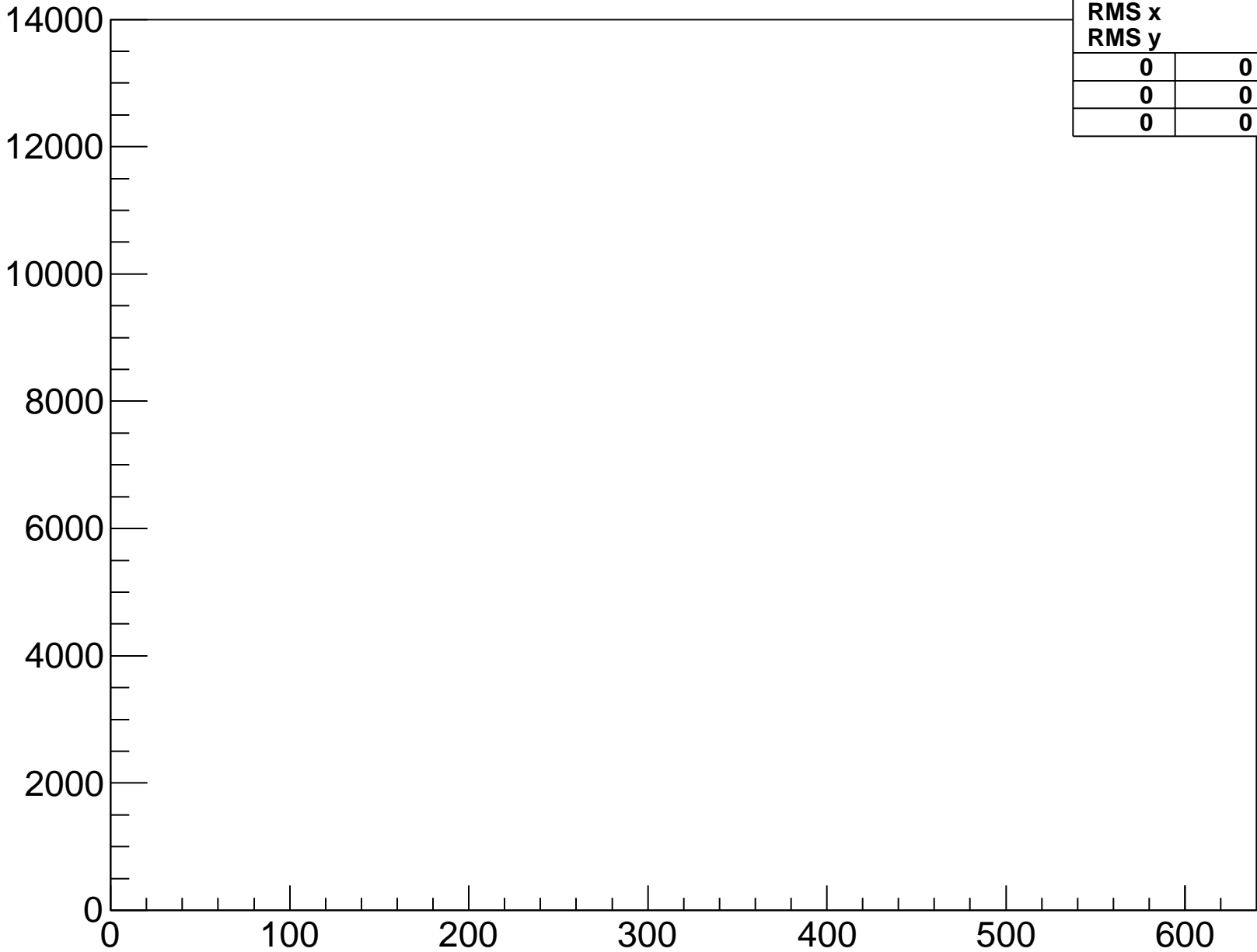
baselinesamples-fpga-2-hyb-1-sample-4



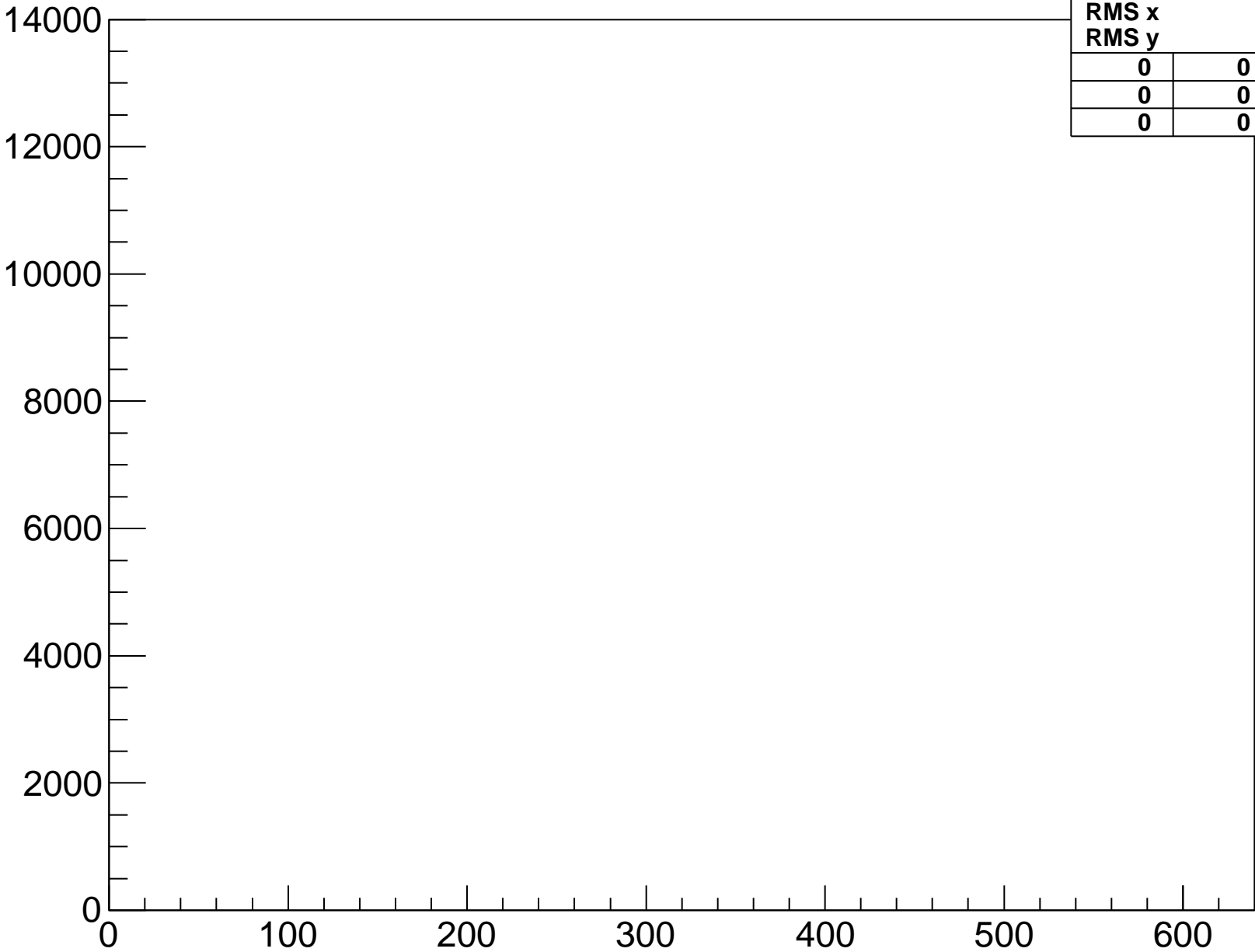
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-2-hyb-1-sample-5

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



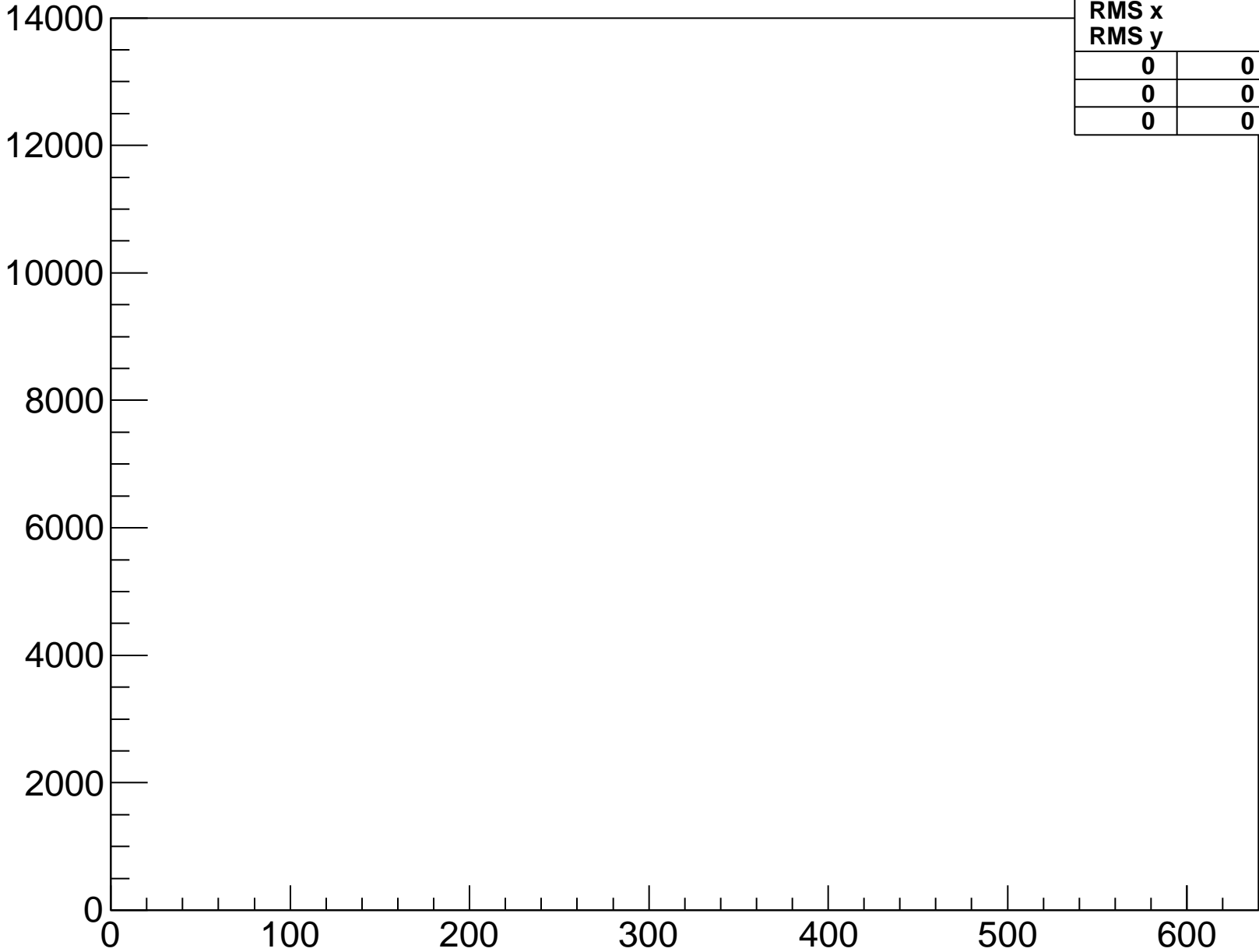
baselinesamples-fpga-2-hyb-2-sample-0



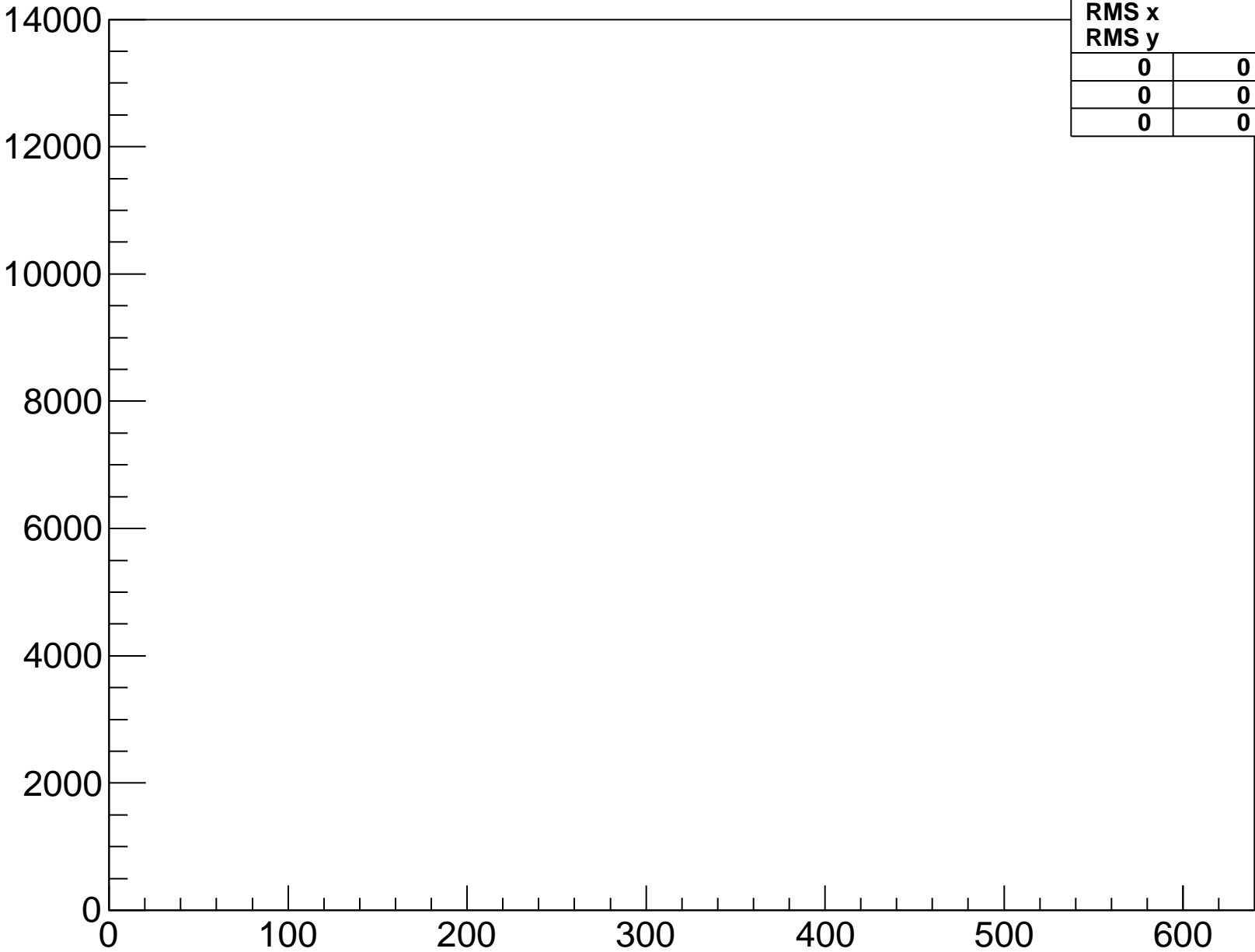
Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	
0	0	0	
0	0	0	

baselinesamples-fpga-2-hyb-2-sample-1

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

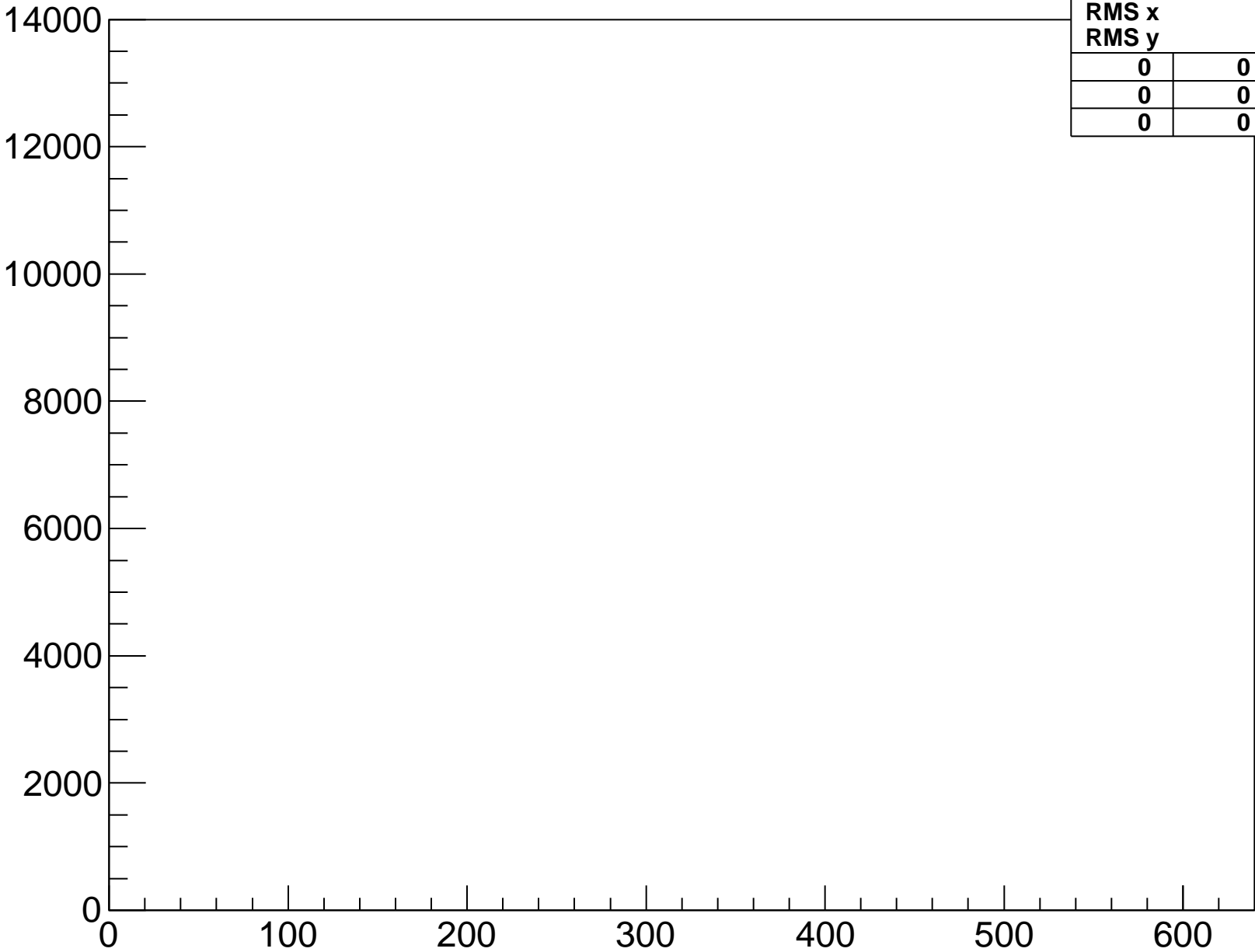


baselinesamples-fpga-2-hyb-2-sample-2



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

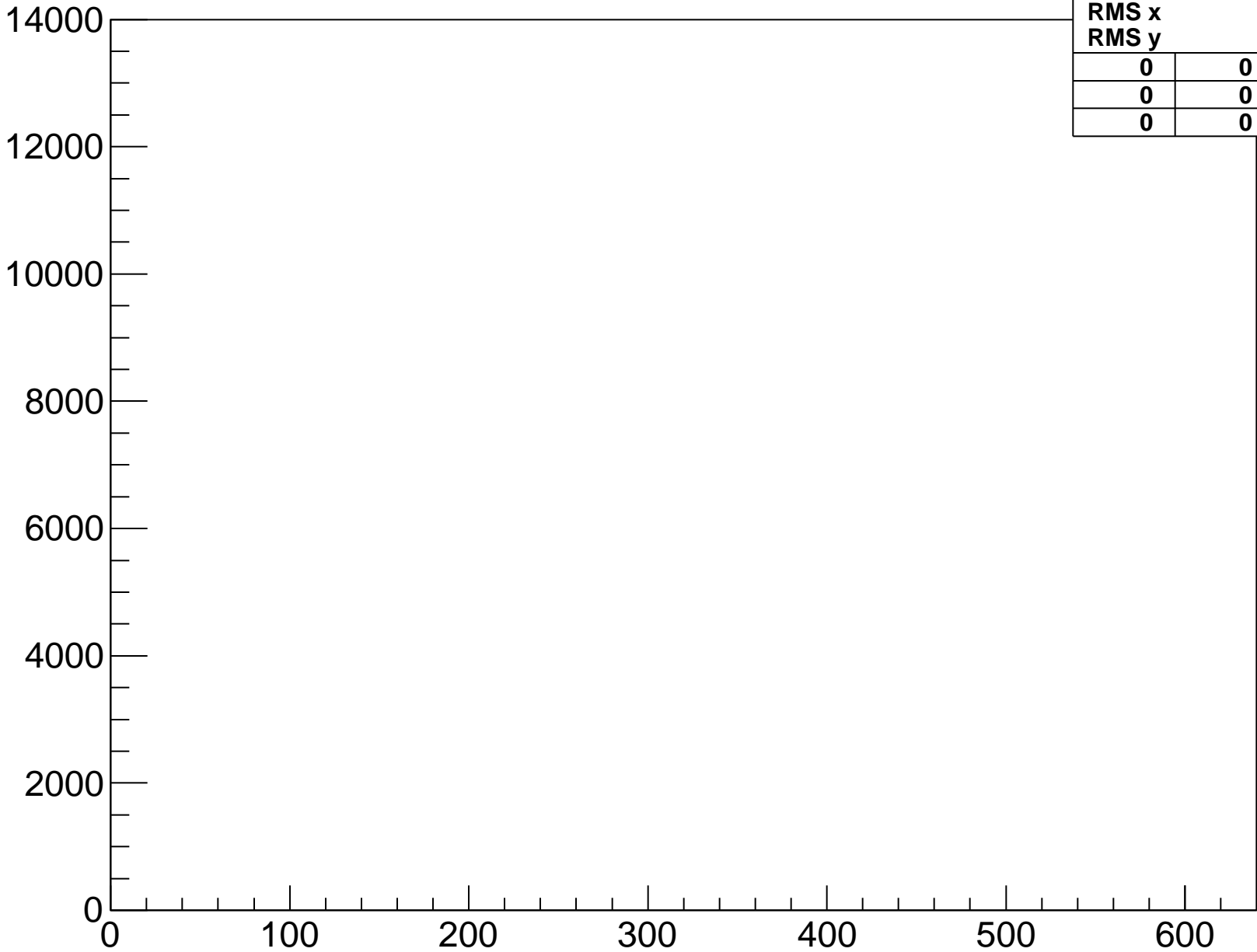
baselinesamples-fpga-2-hyb-2-sample-3



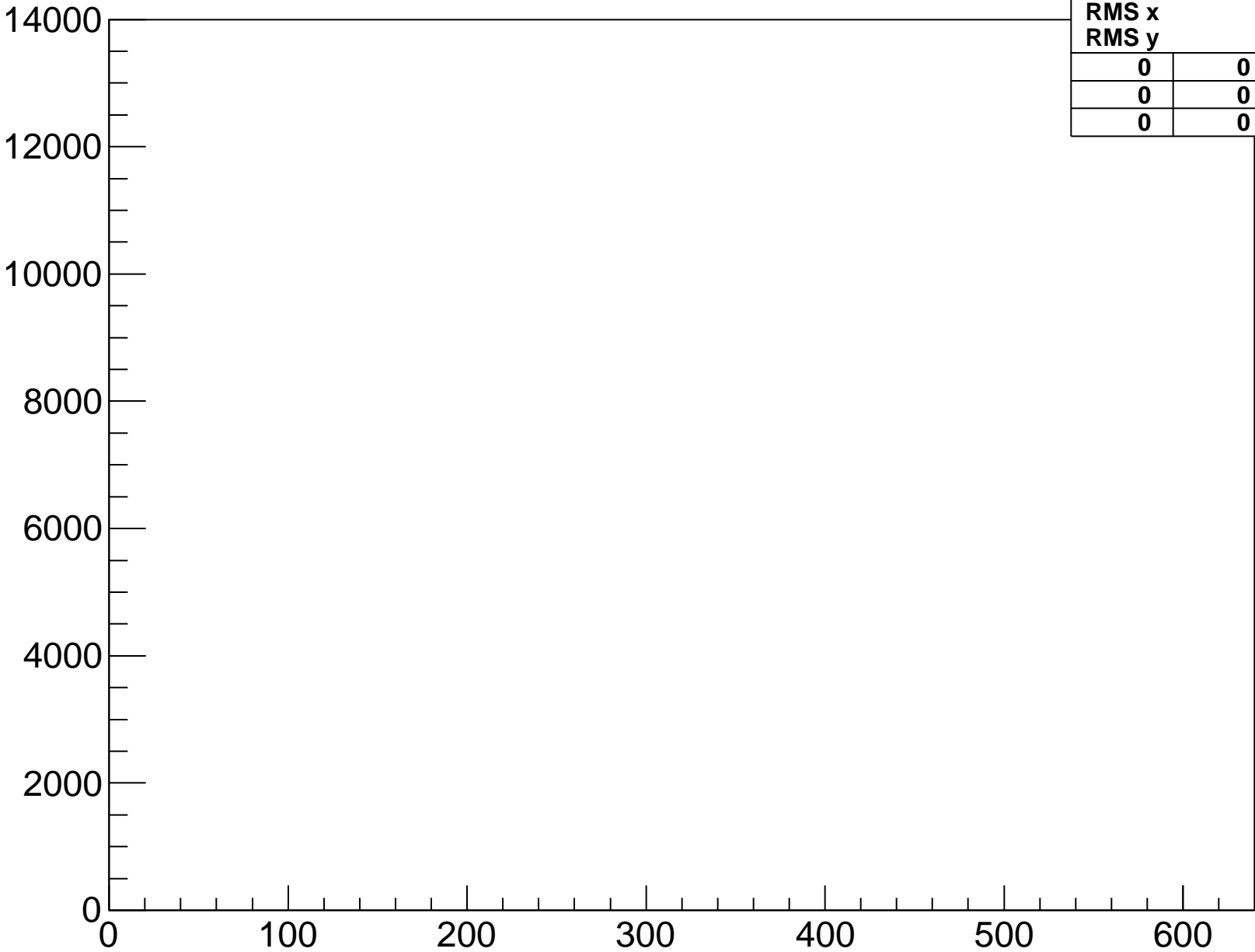
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-2-hyb-2-sample-4

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



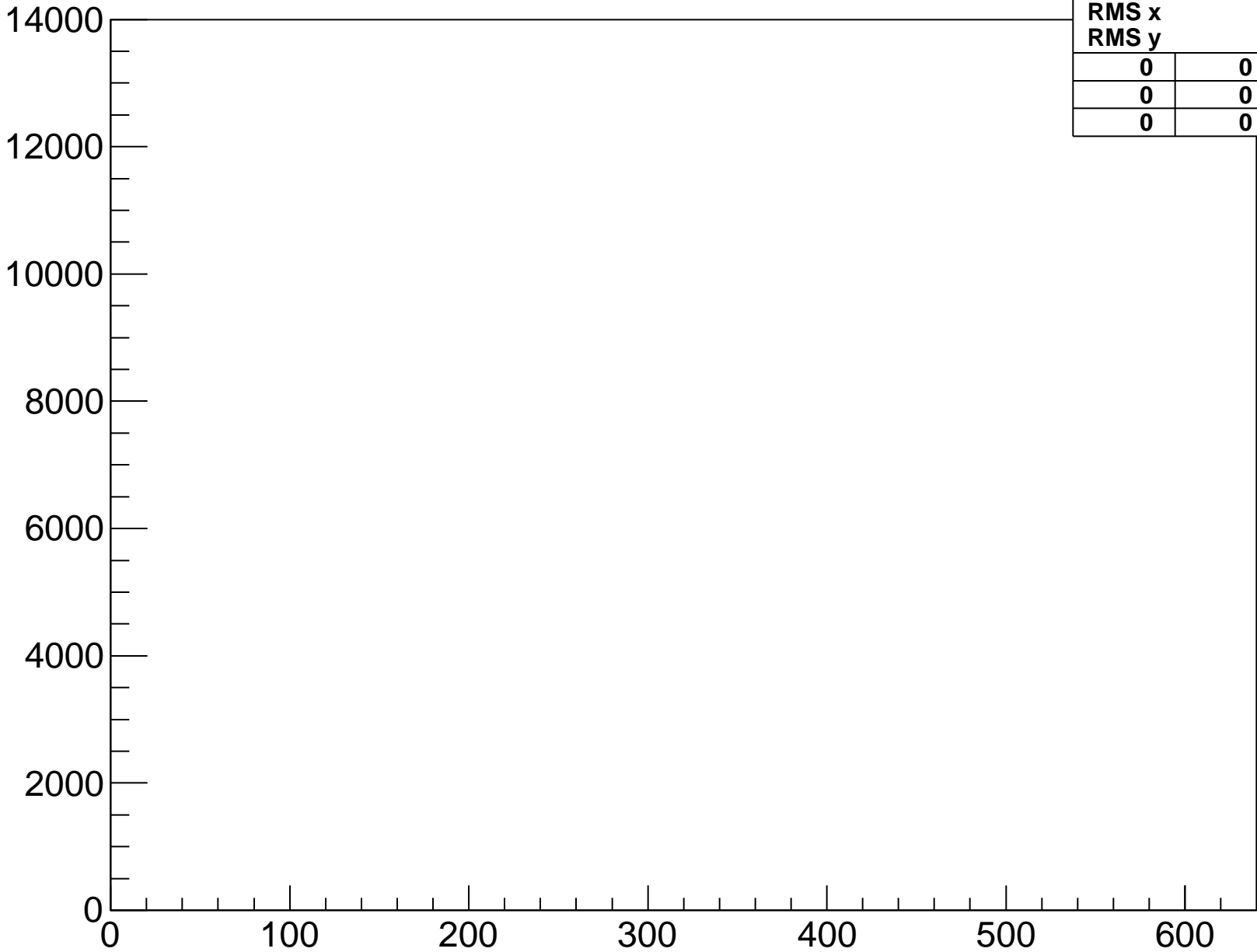
baselinesamples-fpga-2-hyb-2-sample-5



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

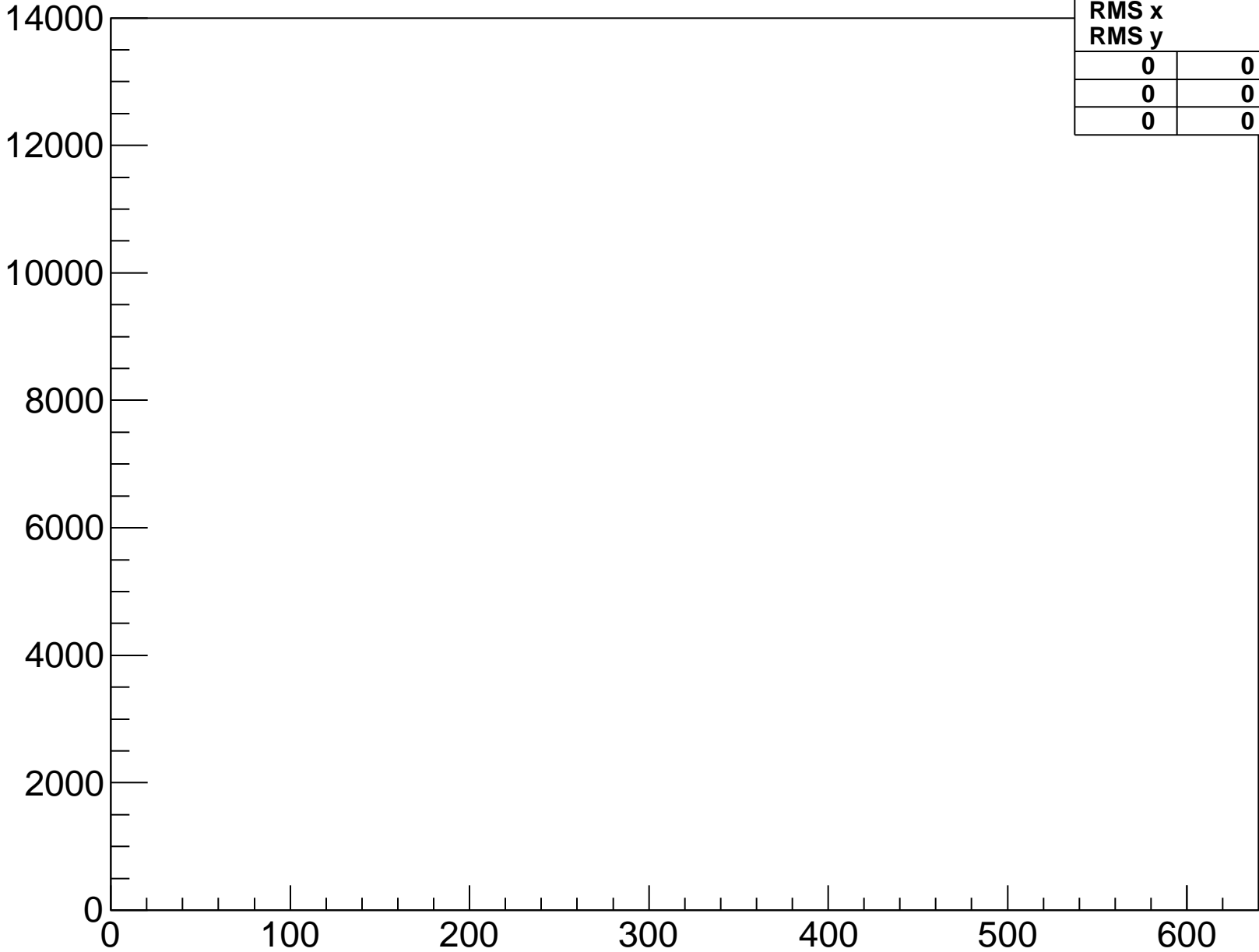
baselinesamples-fpga-2-hyb-3-sample-0

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

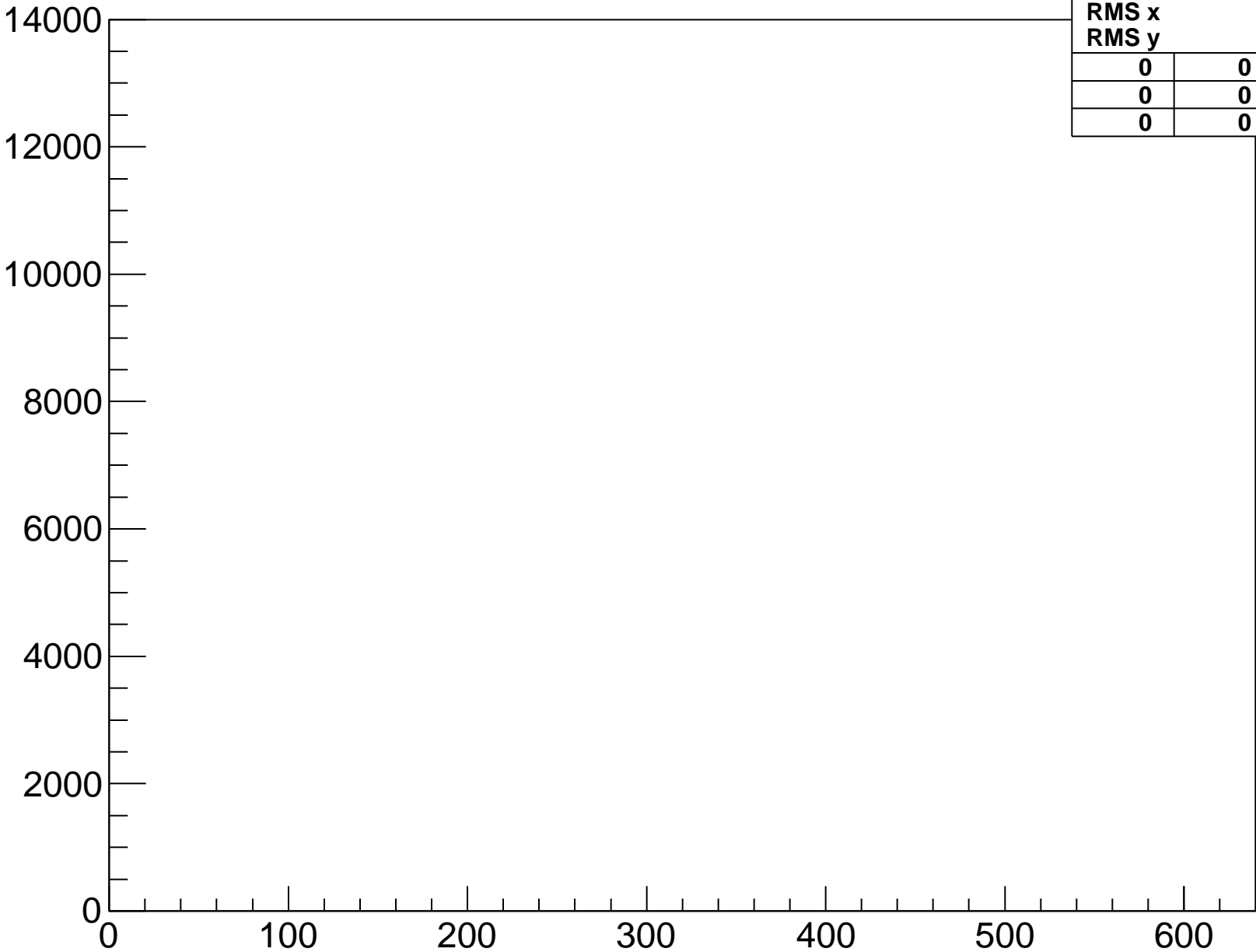


baselinesamples-fpga-2-hyb-3-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

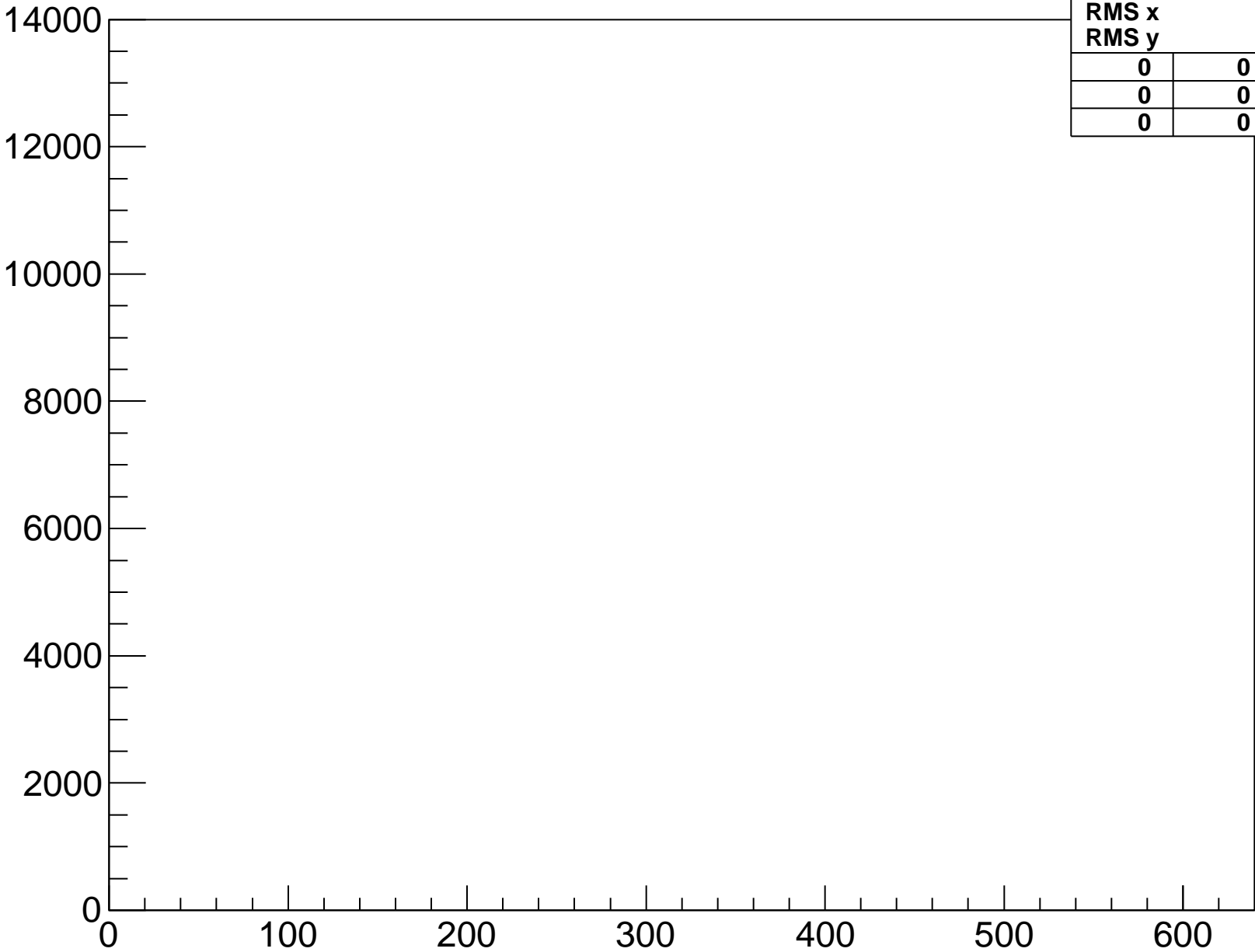


baselinesamples-fpga-2-hyb-3-sample-2



Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	0
0	0	0	0
0	0	0	0

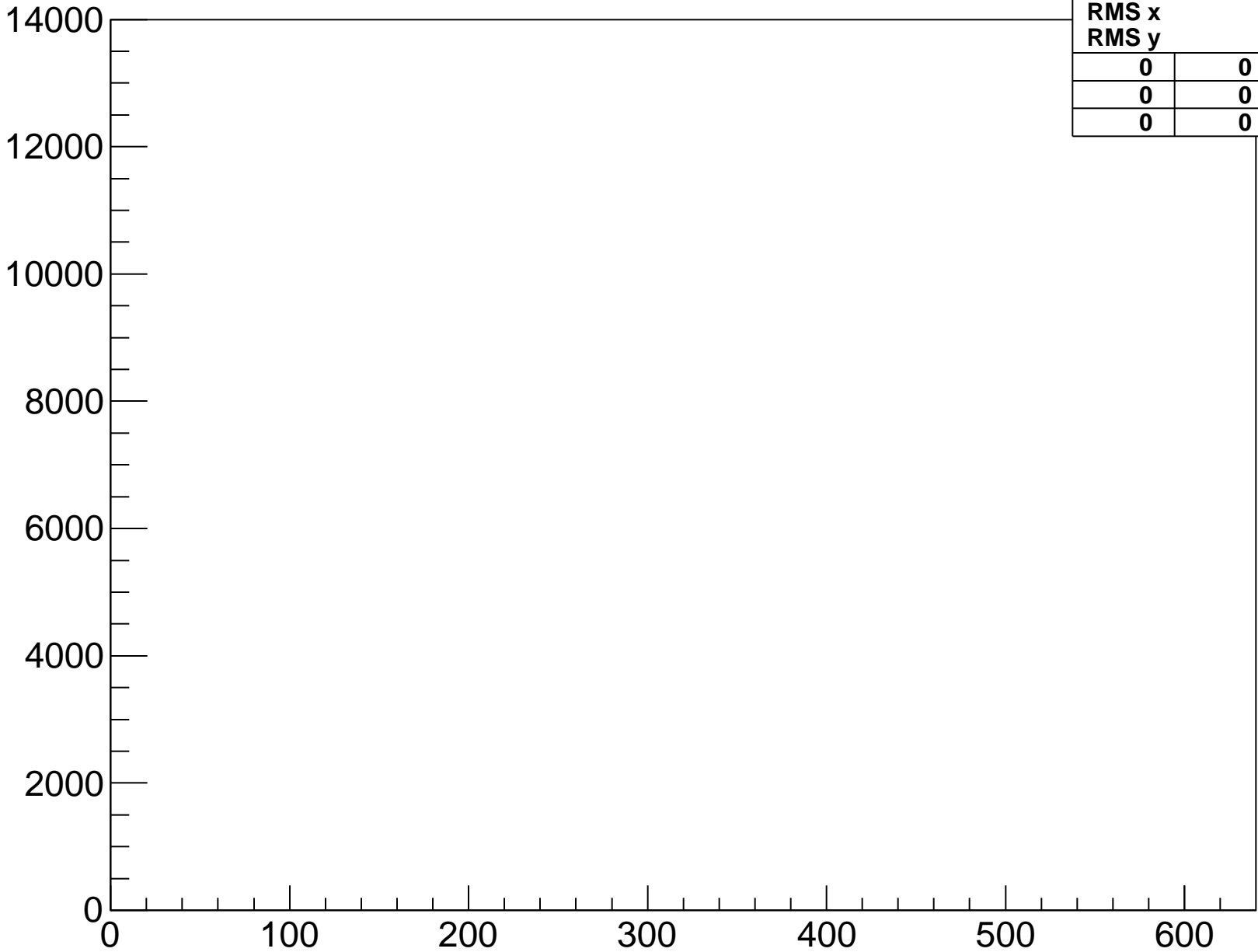
baselinesamples-fpga-2-hyb-3-sample-3



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

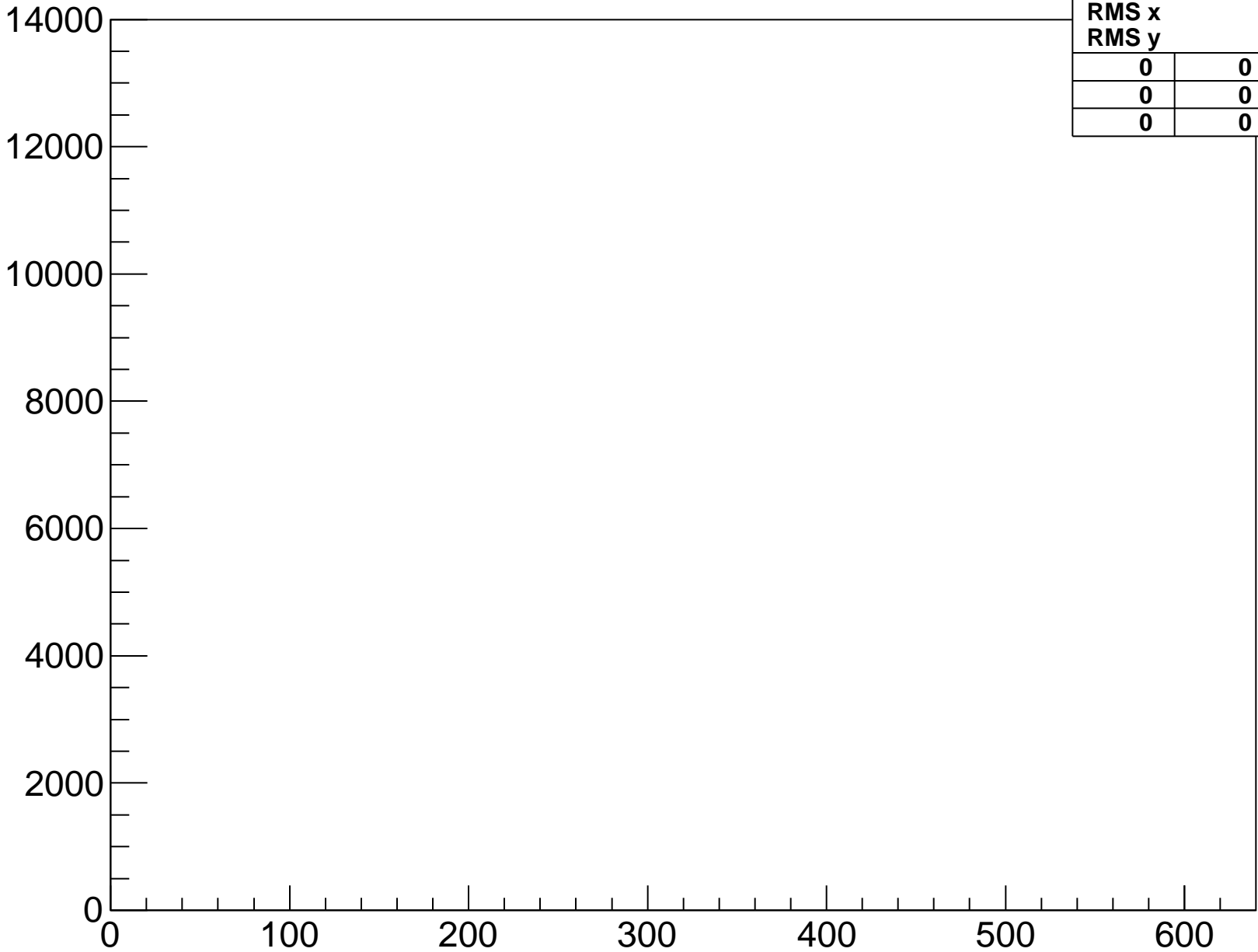
baselinesamples-fpga-2-hyb-3-sample-4

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



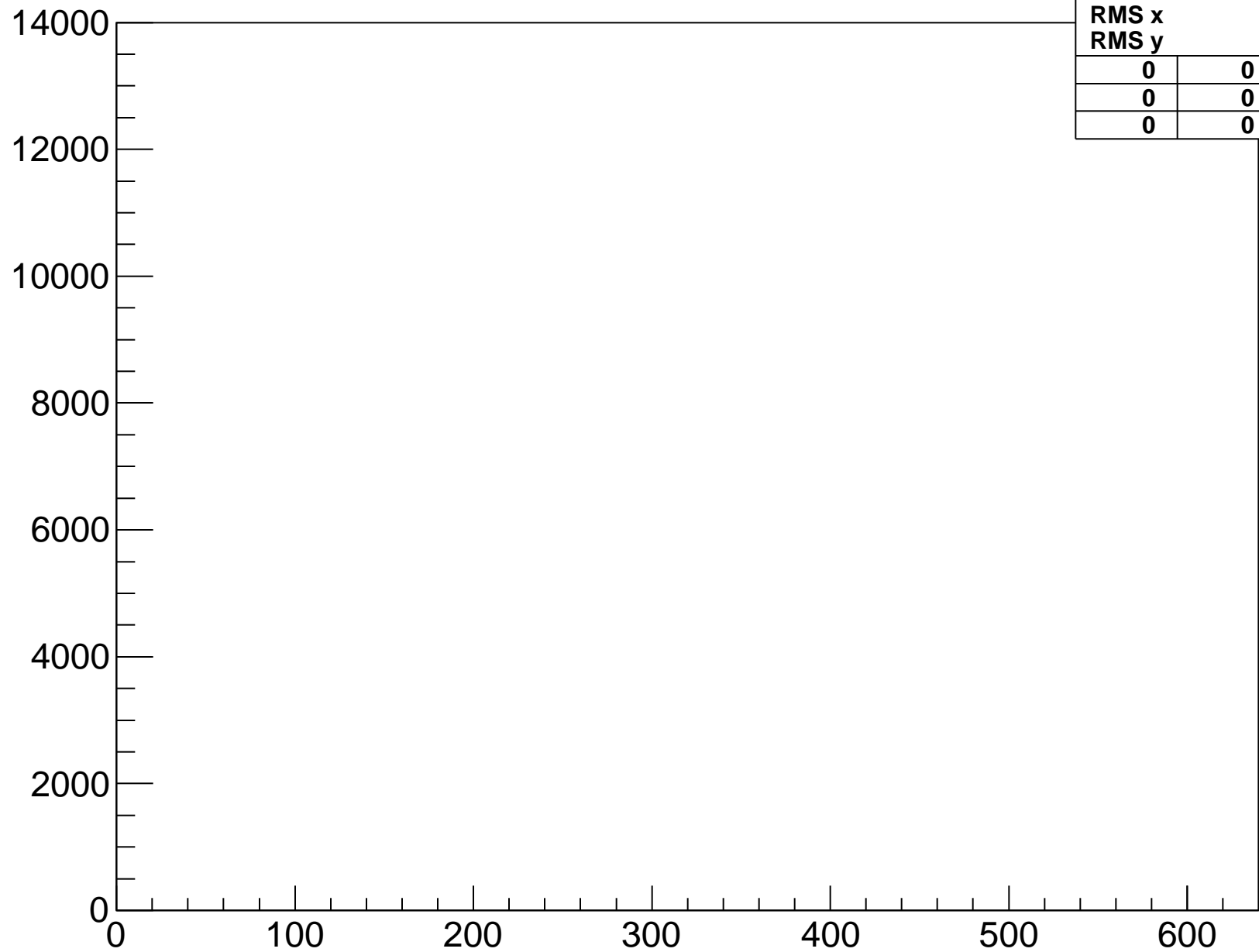
baselinesamples-fpga-2-hyb-3-sample-5

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

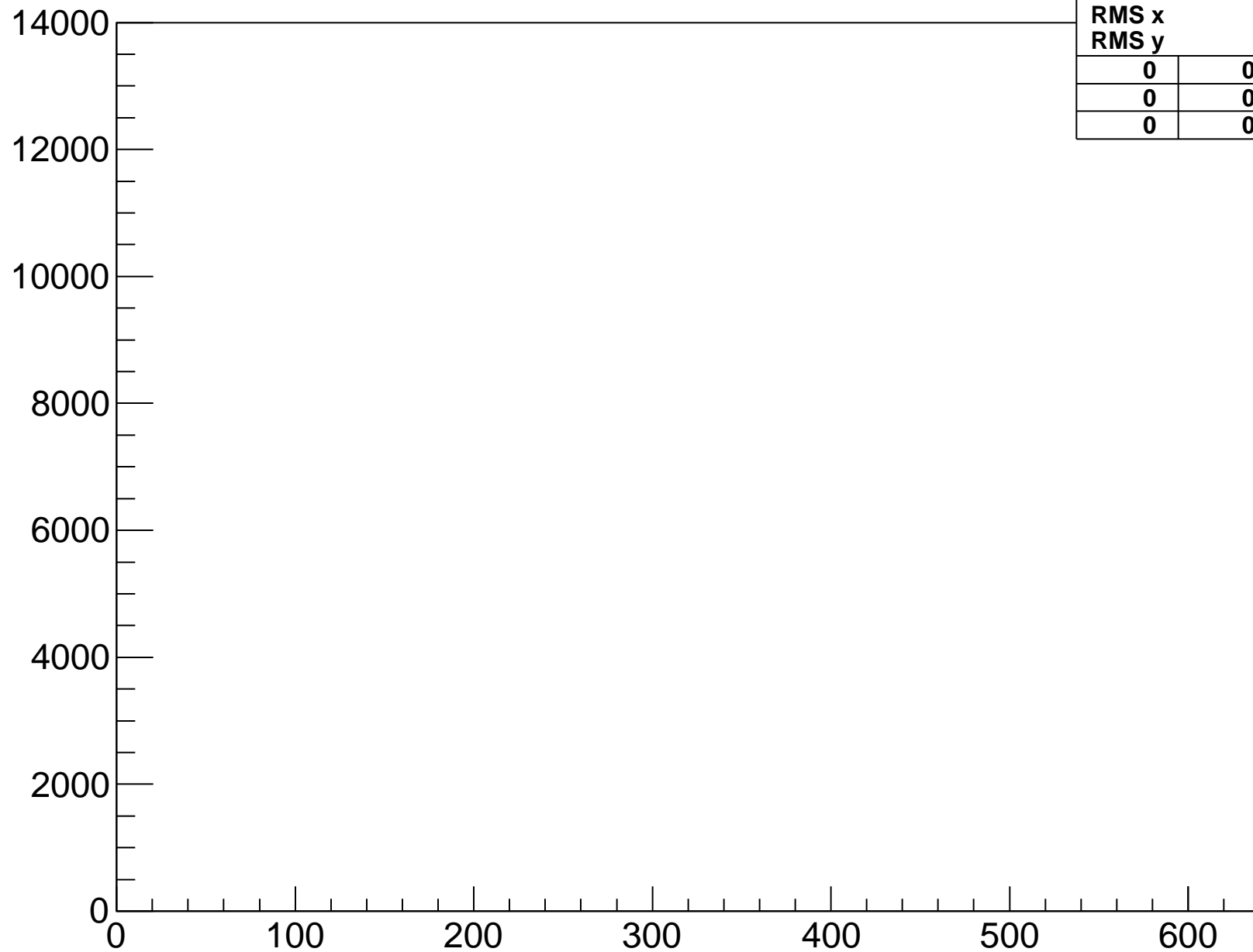


baselinesamples-fpga-3-hyb-0-sample-0

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

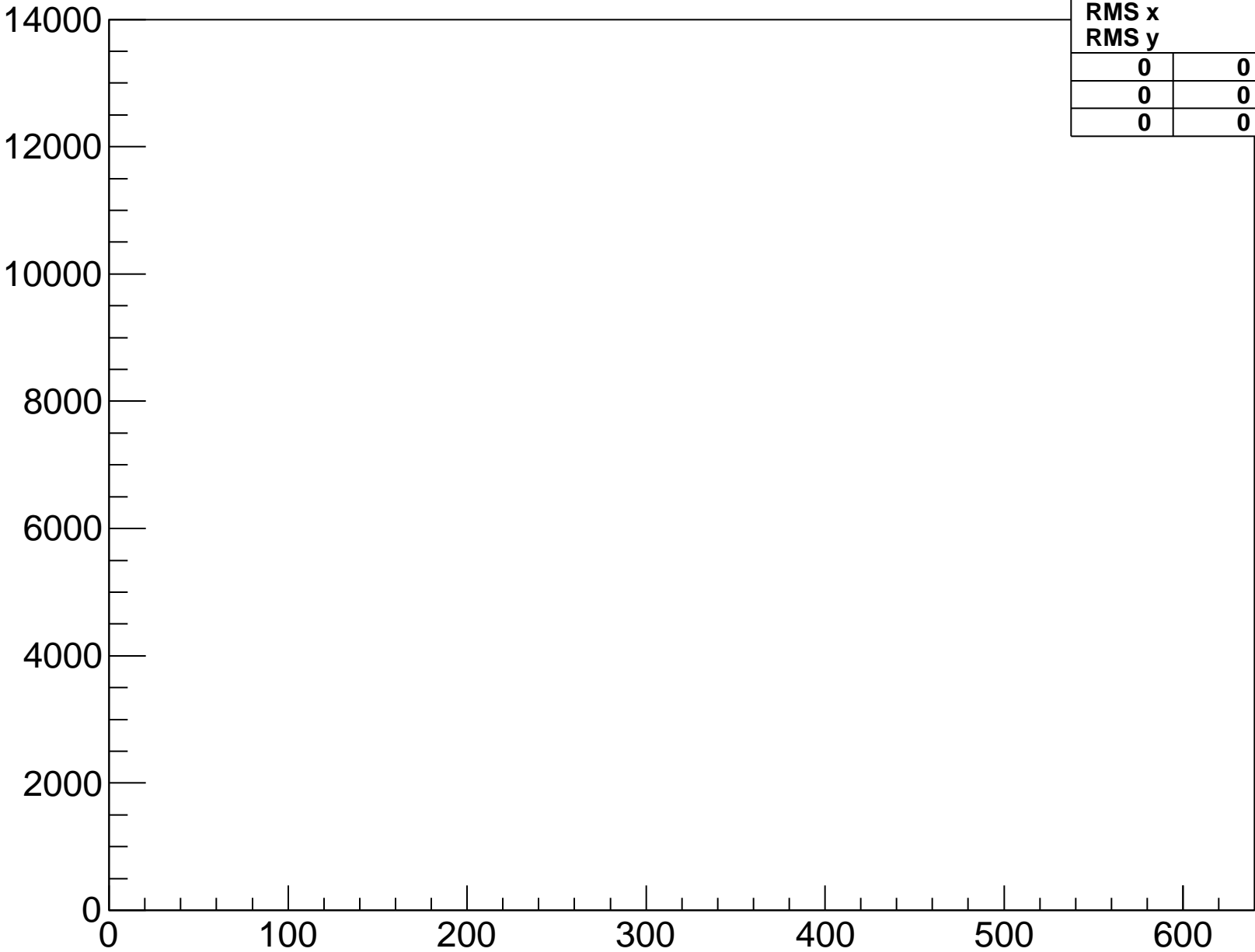


baselinesamples-fpga-3-hyb-0-sample-1



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

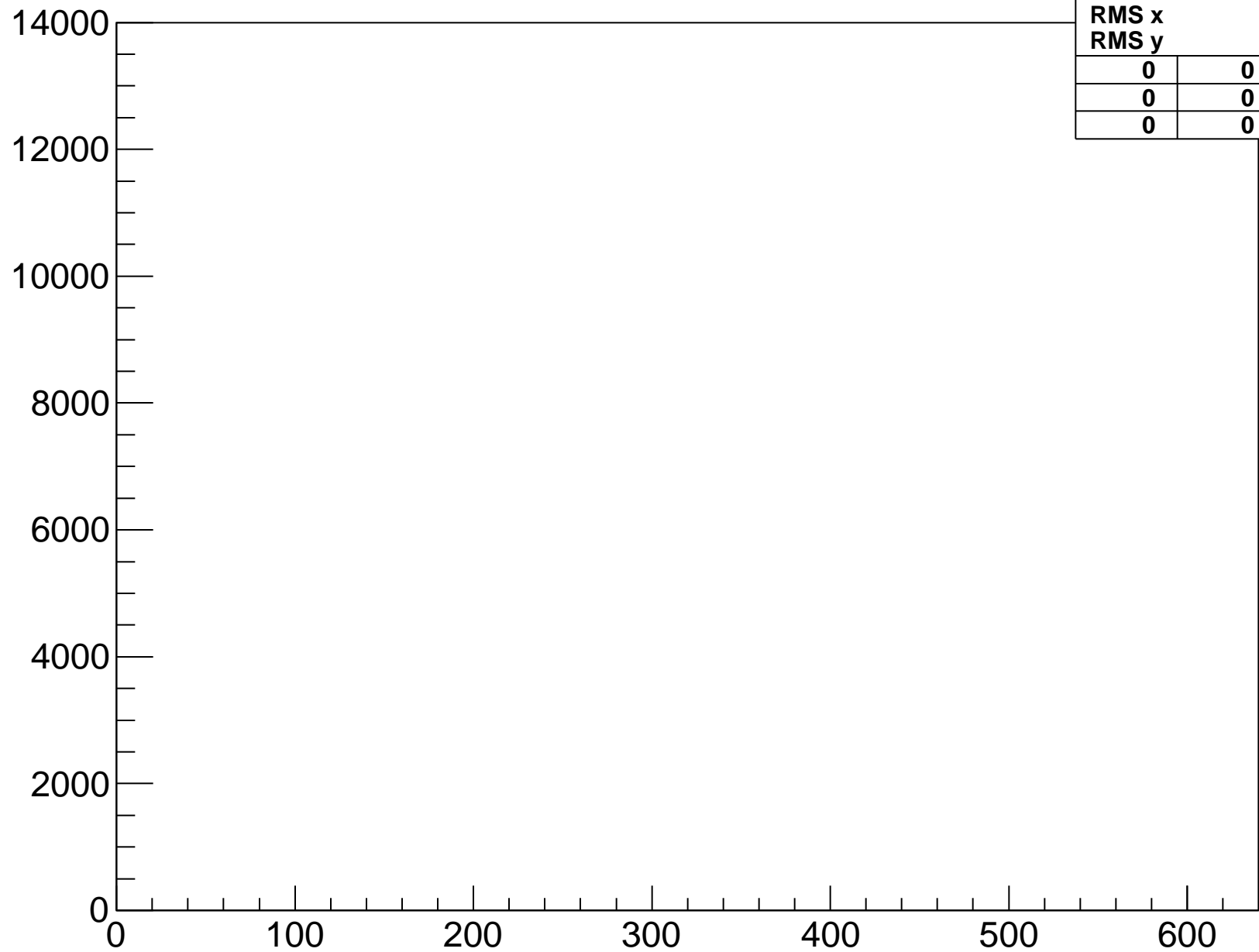
baselinesamples-fpga-3-hyb-0-sample-2



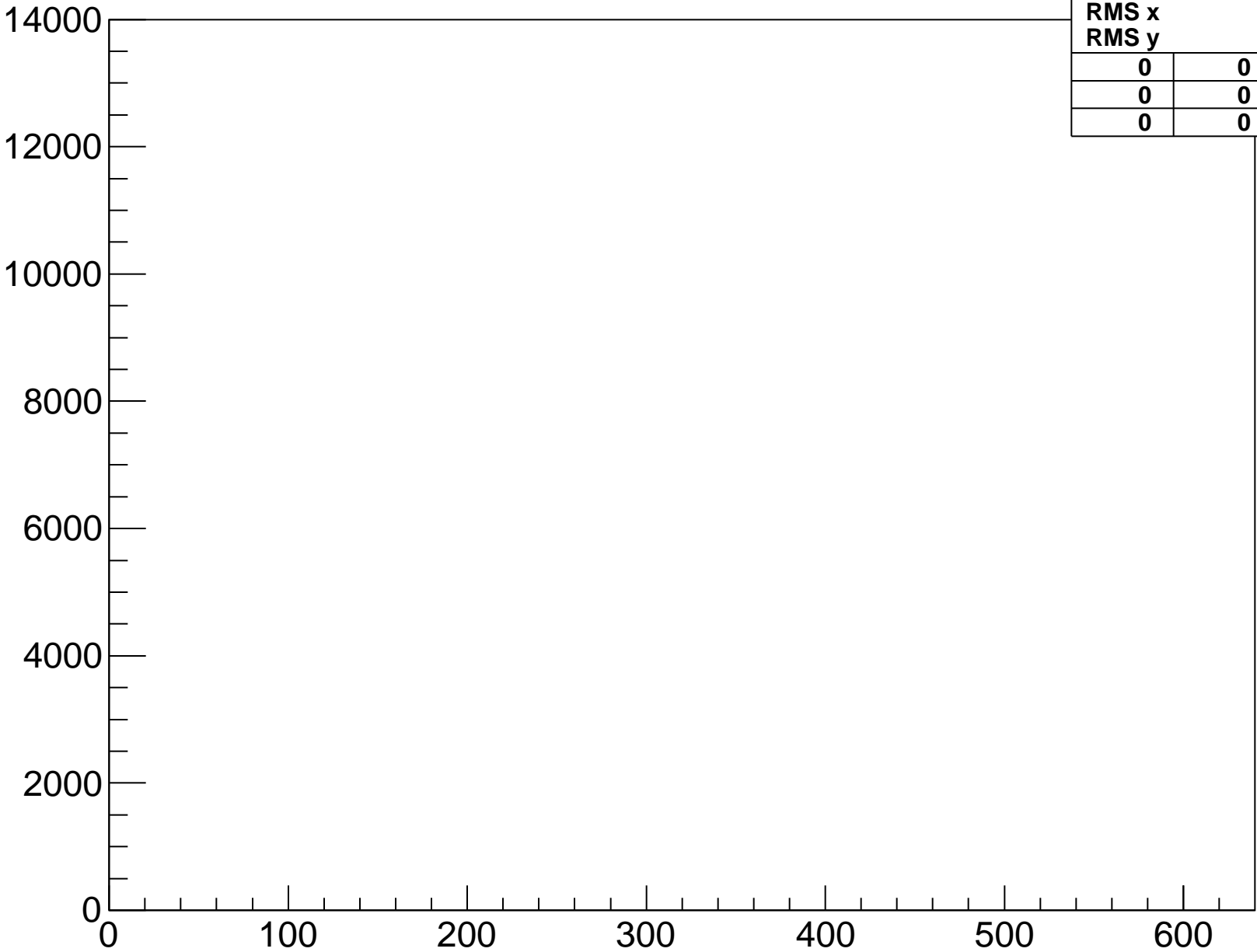
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-3-hyb-0-sample-3

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



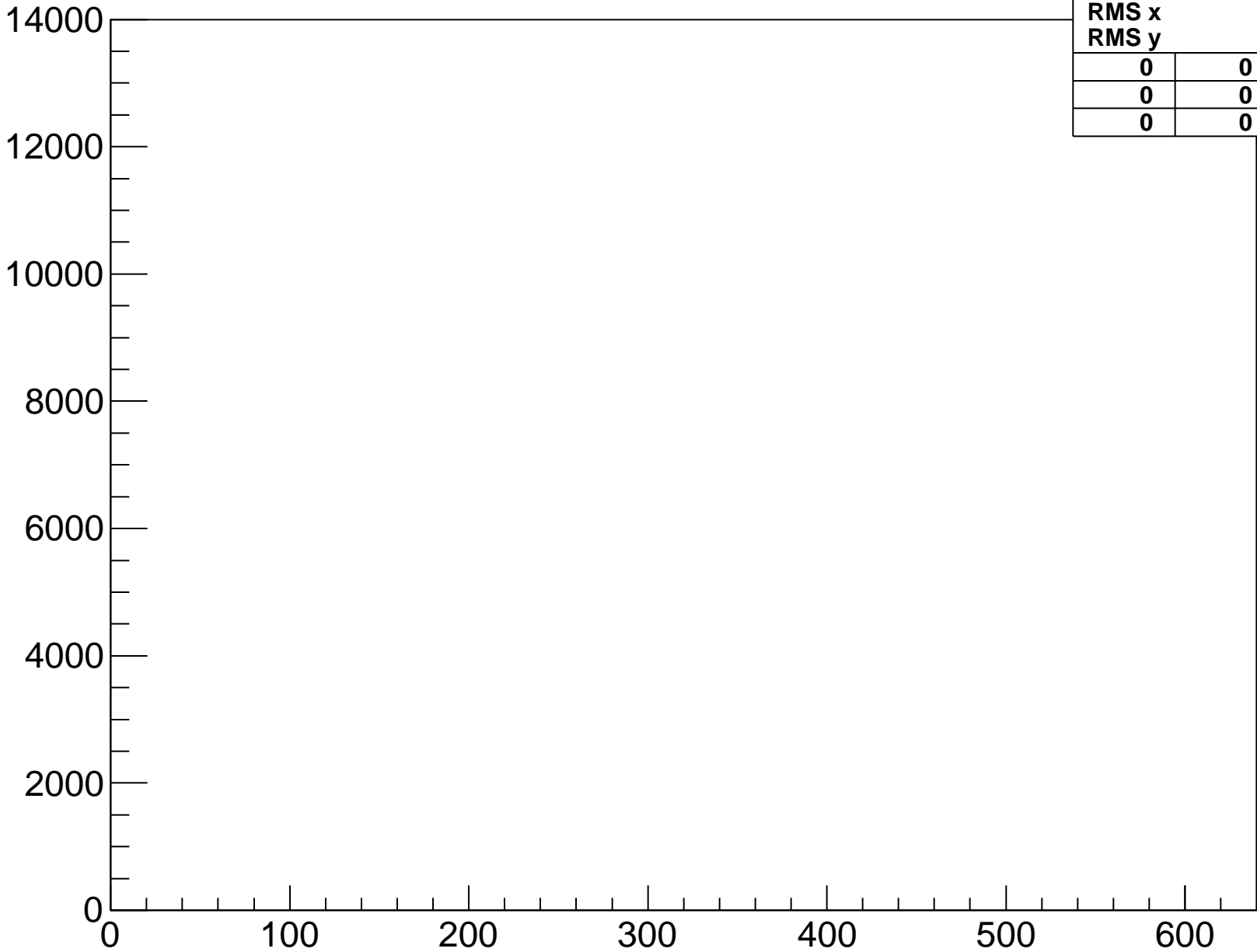
baselinesamples-fpga-3-hyb-0-sample-4



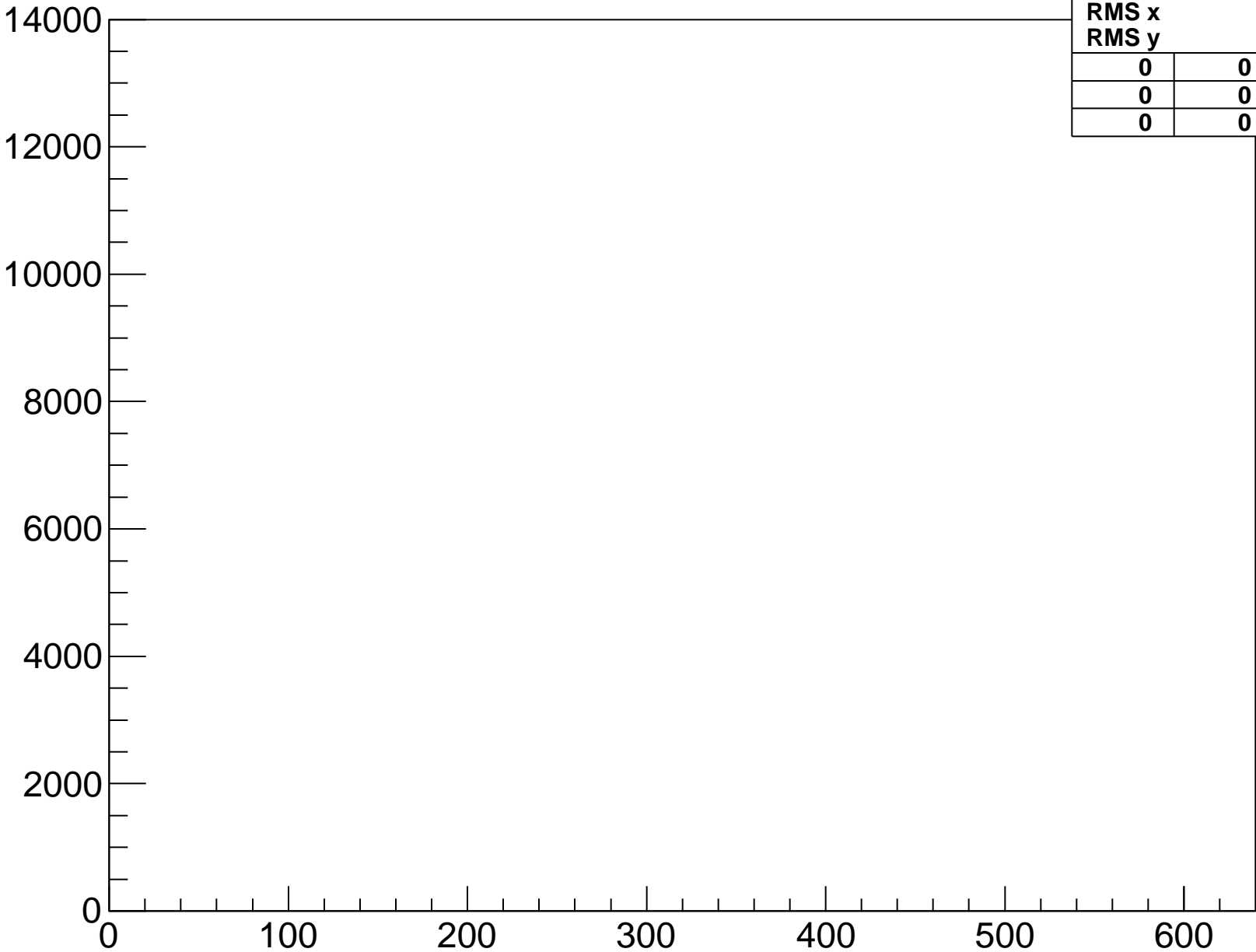
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-3-hyb-0-sample-5

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

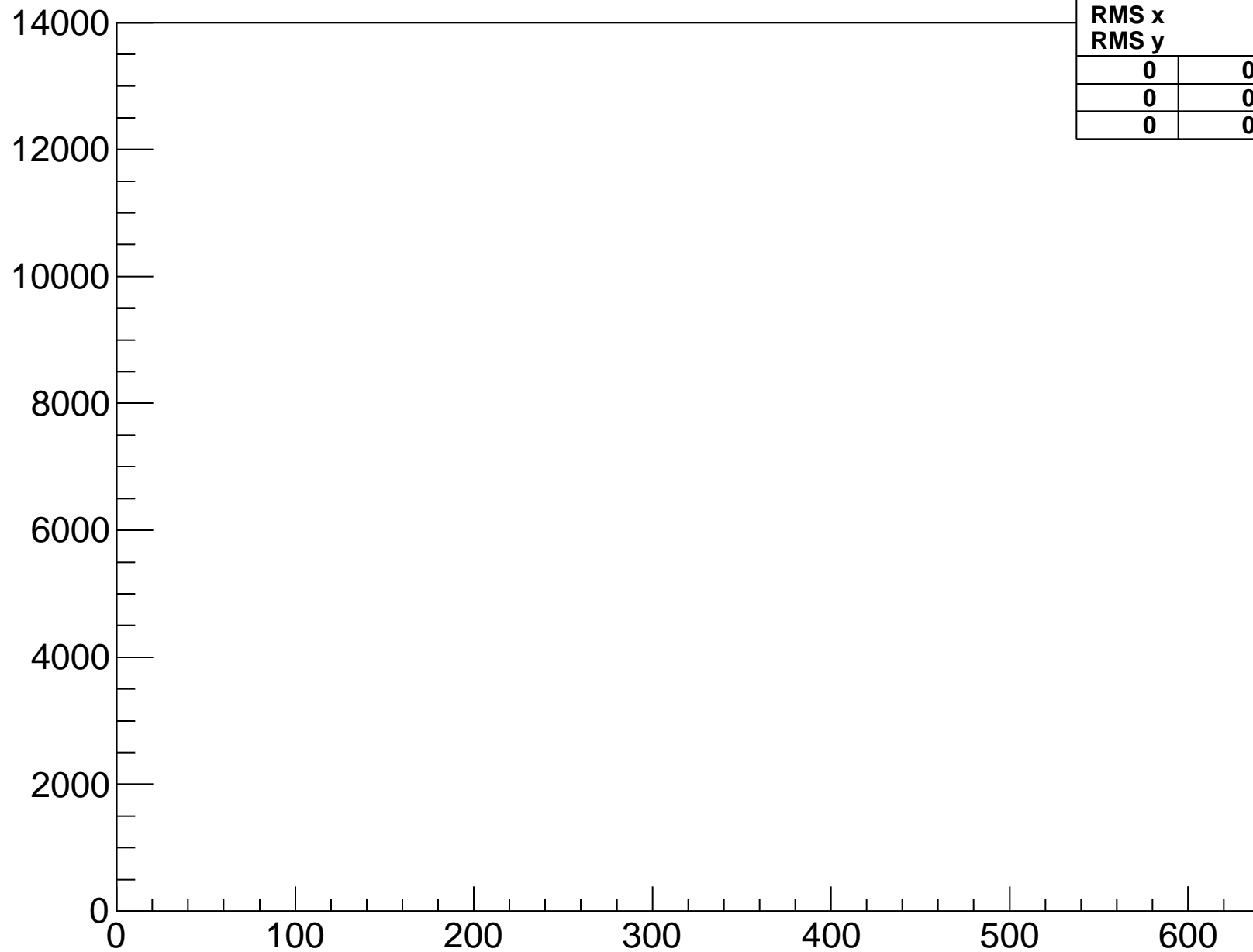


baselinesamples-fpga-3-hyb-1-sample-0



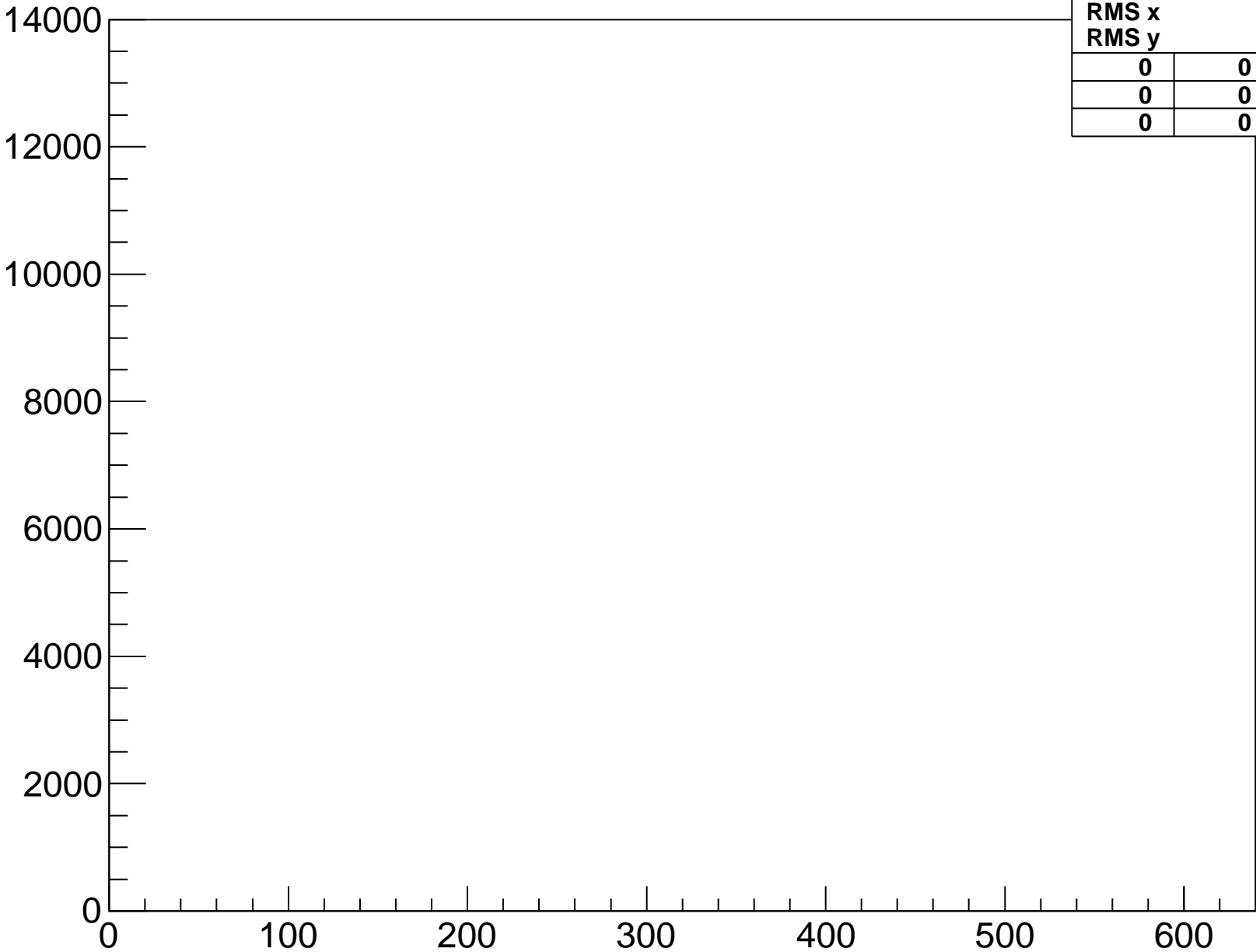
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-3-hyb-1-sample-1



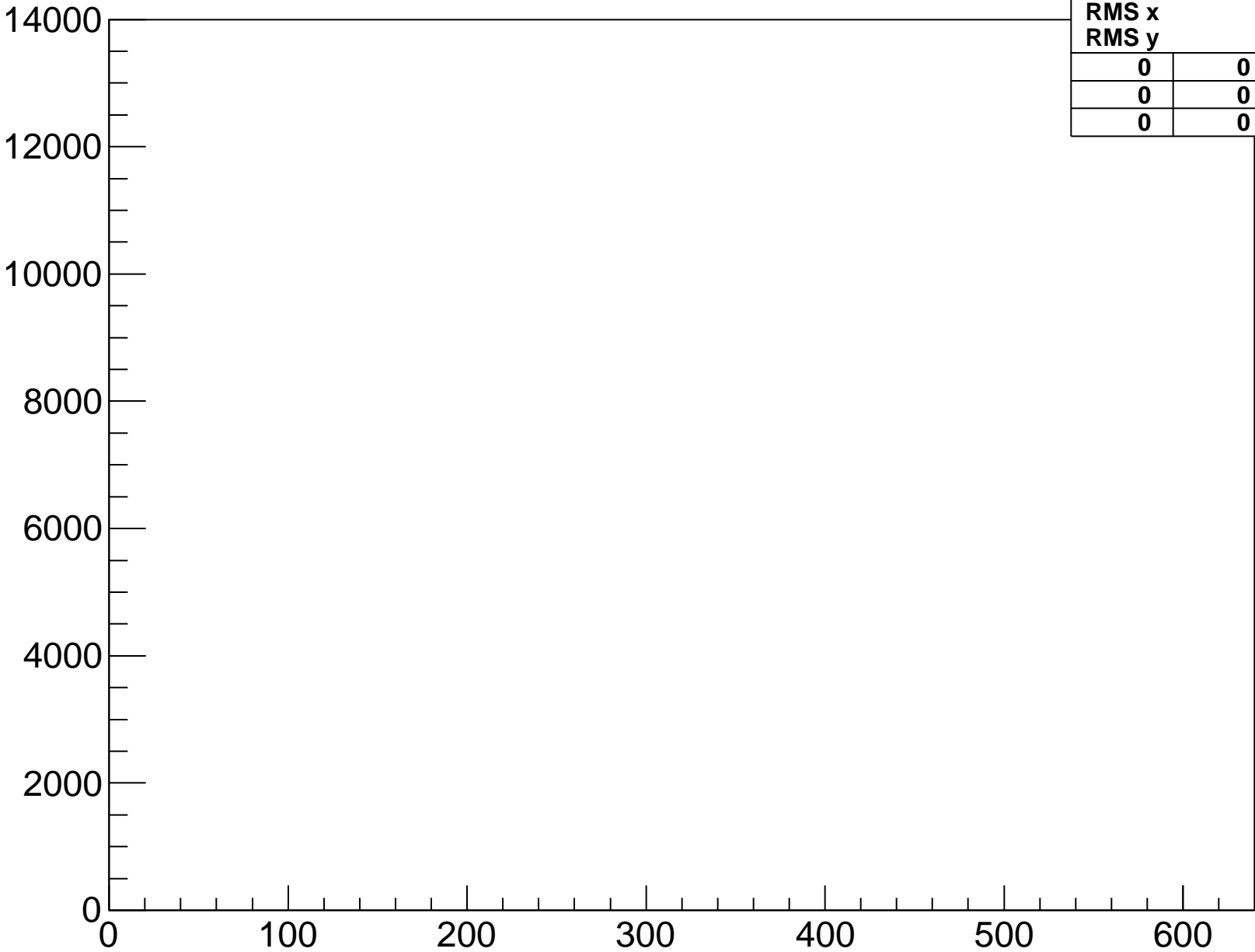
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-3-hyb-1-sample-2



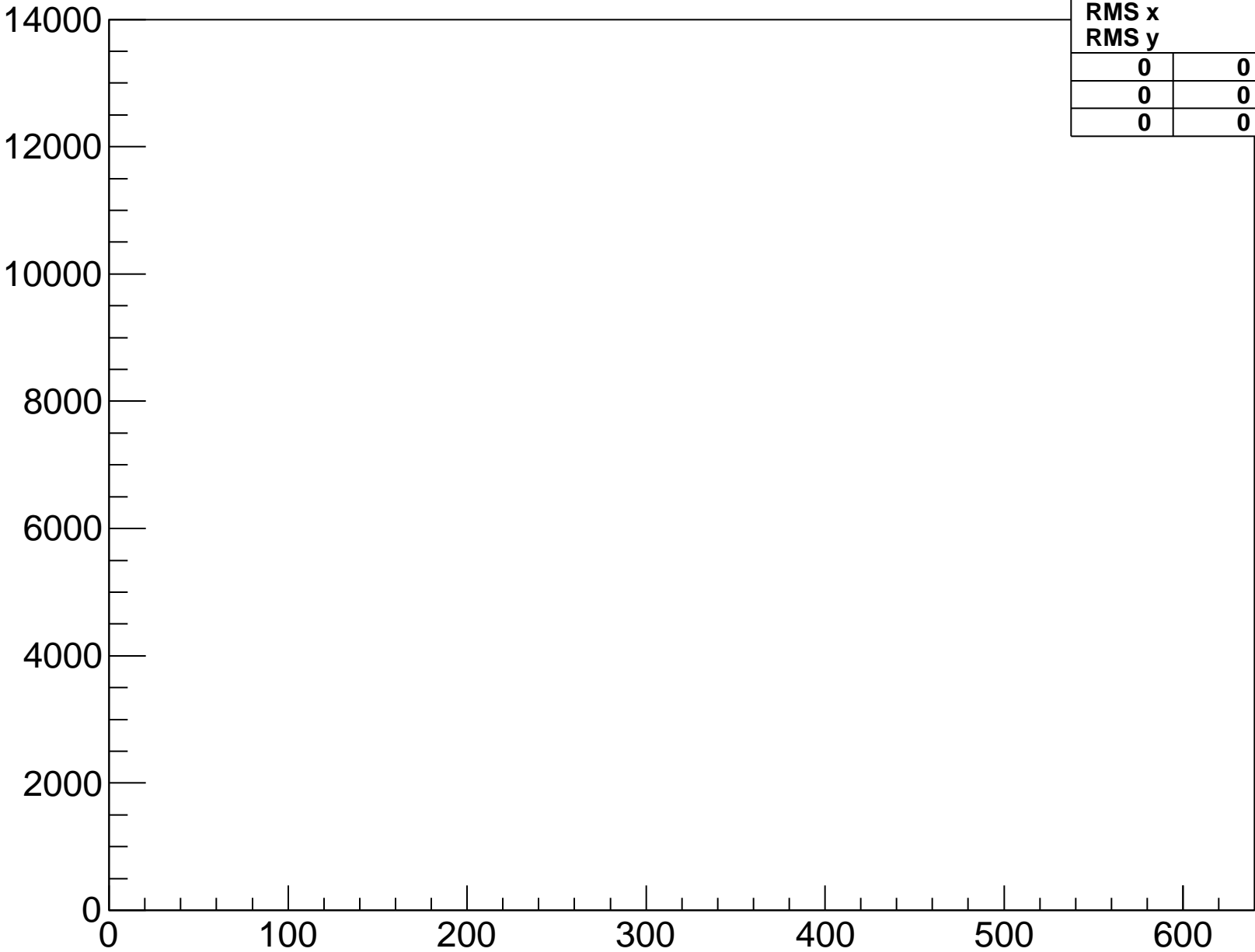
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-3-hyb-1-sample-3



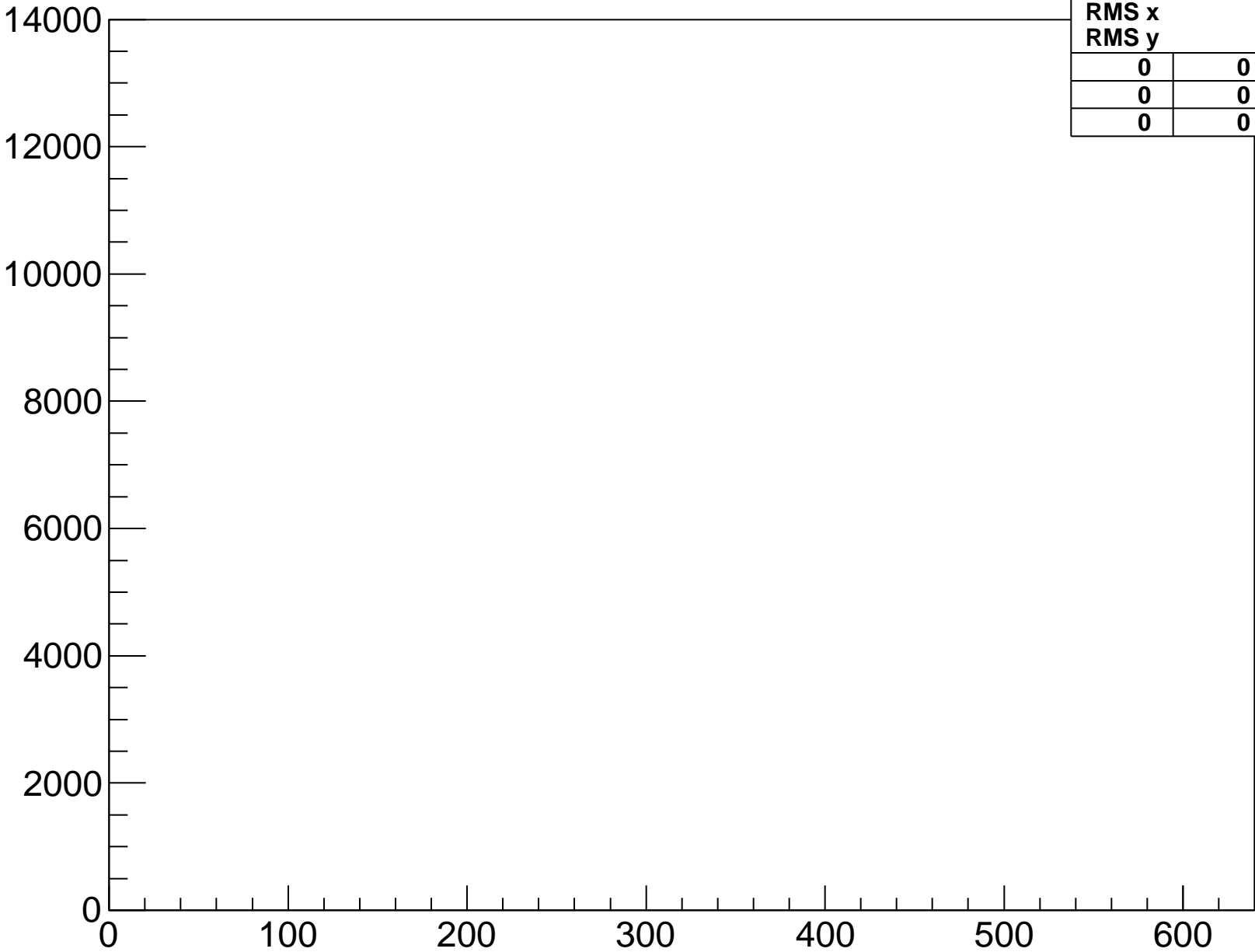
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-3-hyb-1-sample-4



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

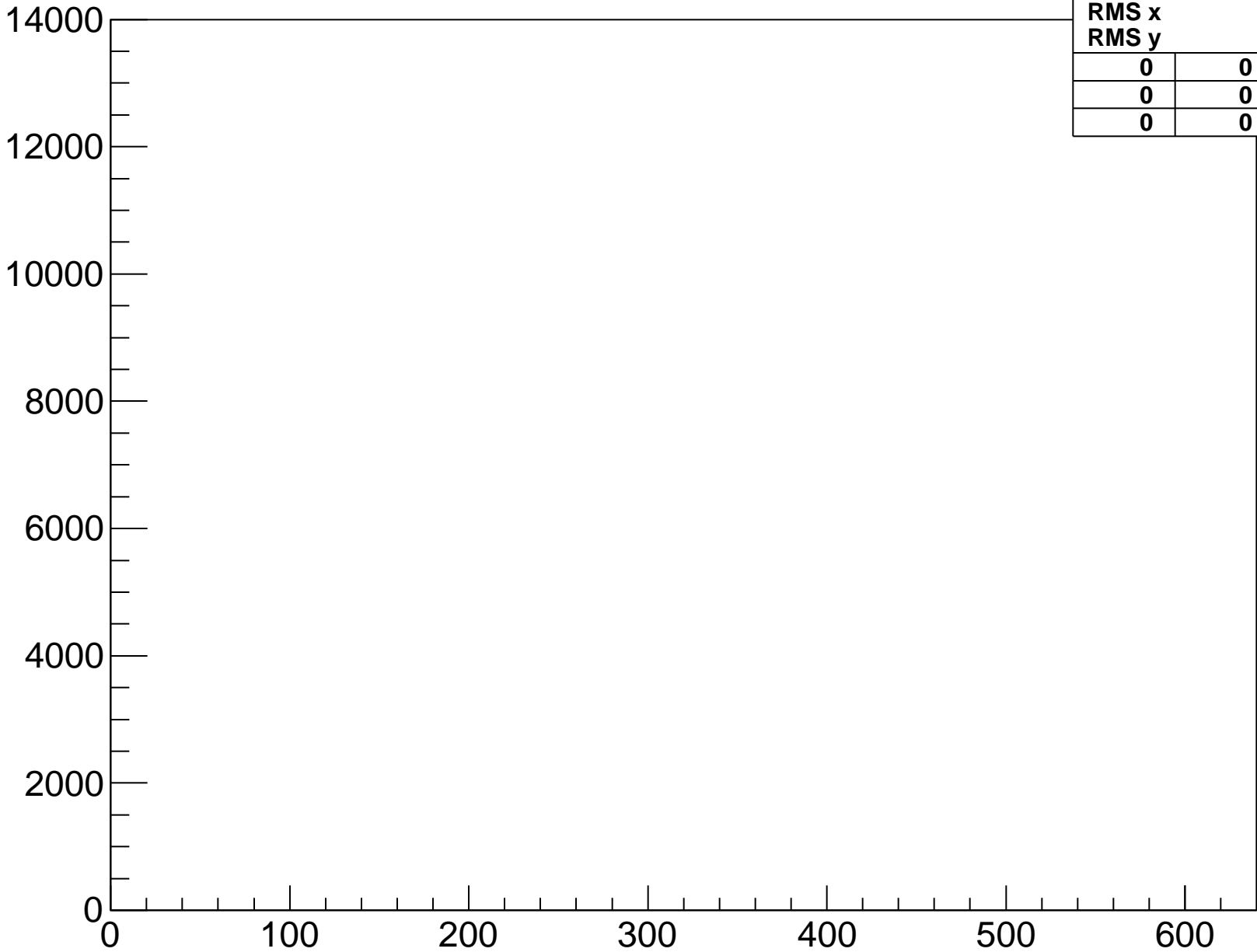
baselinesamples-fpga-3-hyb-1-sample-5



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

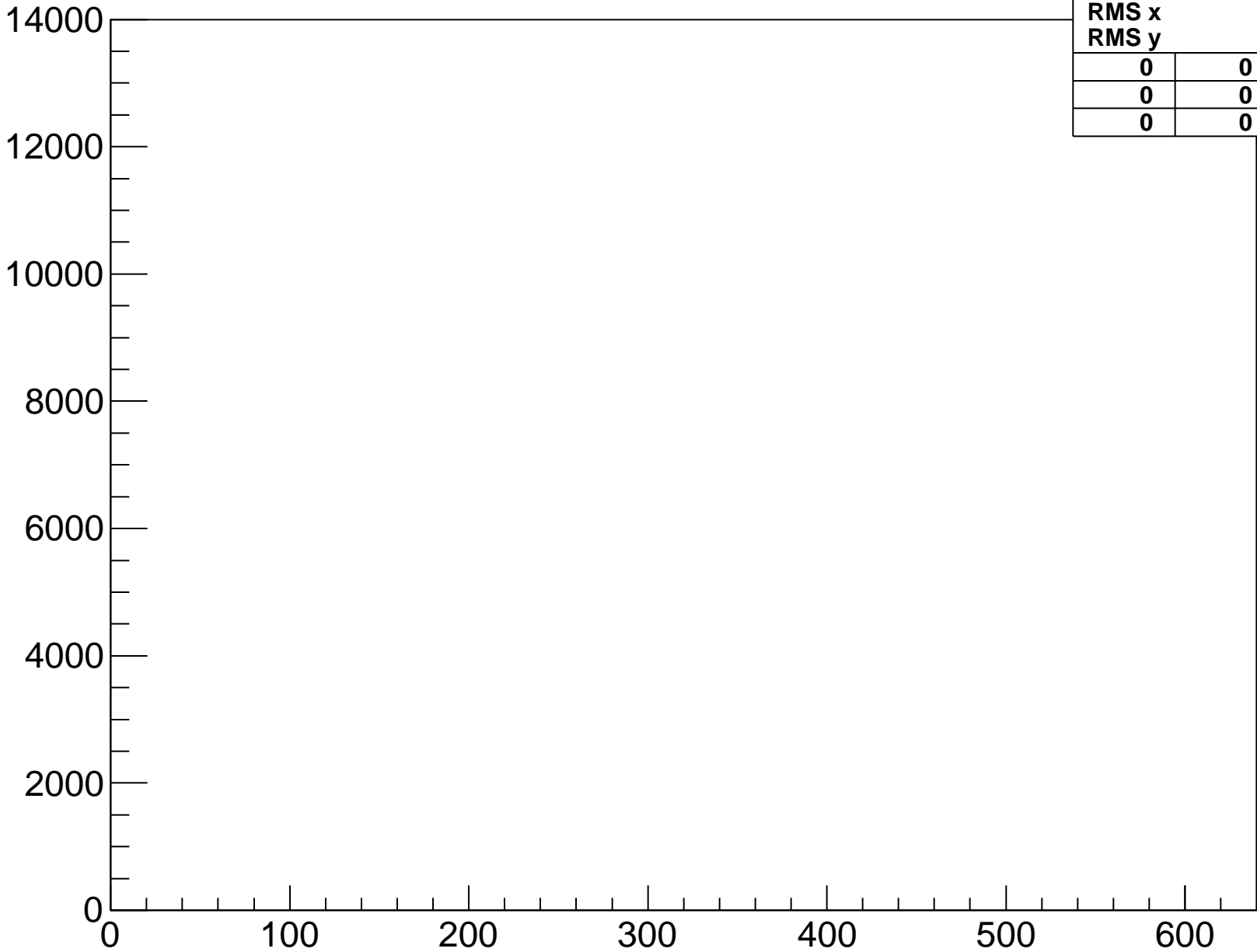
baselinesamples-fpga-3-hyb-2-sample-0

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

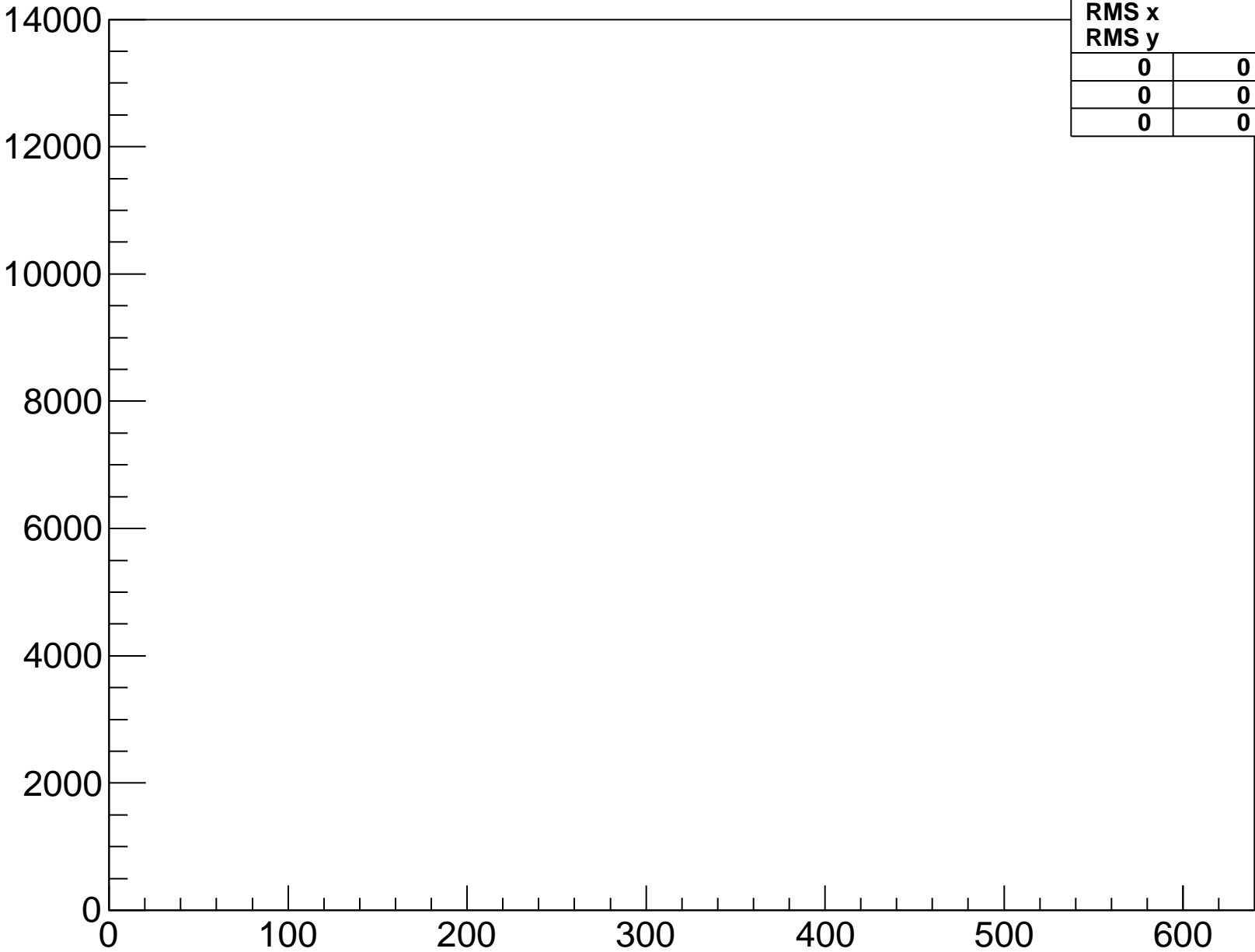


baselinesamples-fpga-3-hyb-2-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



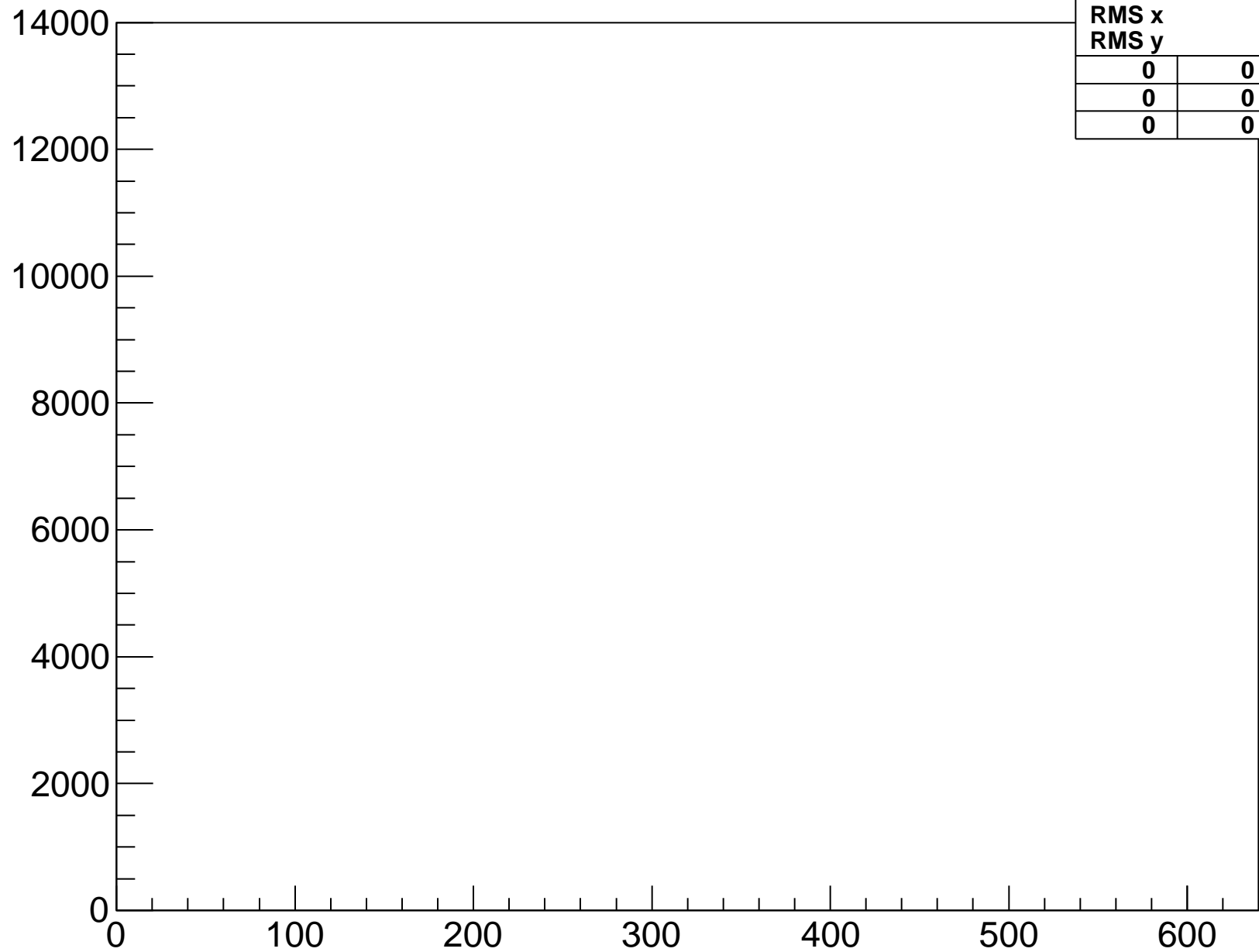
baselinesamples-fpga-3-hyb-2-sample-2



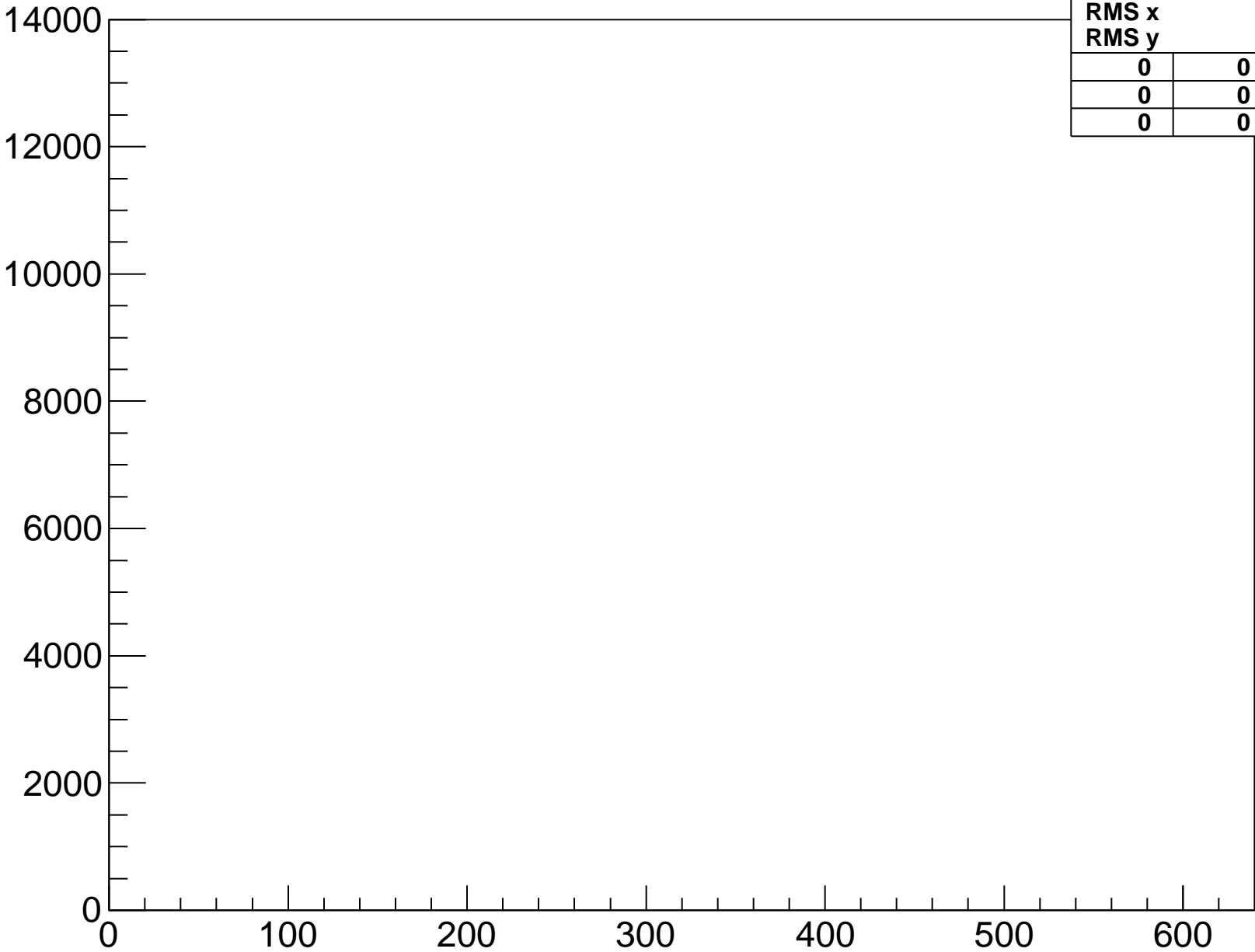
Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	
0	0	0	
0	0	0	

baselinesamples-fpga-3-hyb-2-sample-3

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

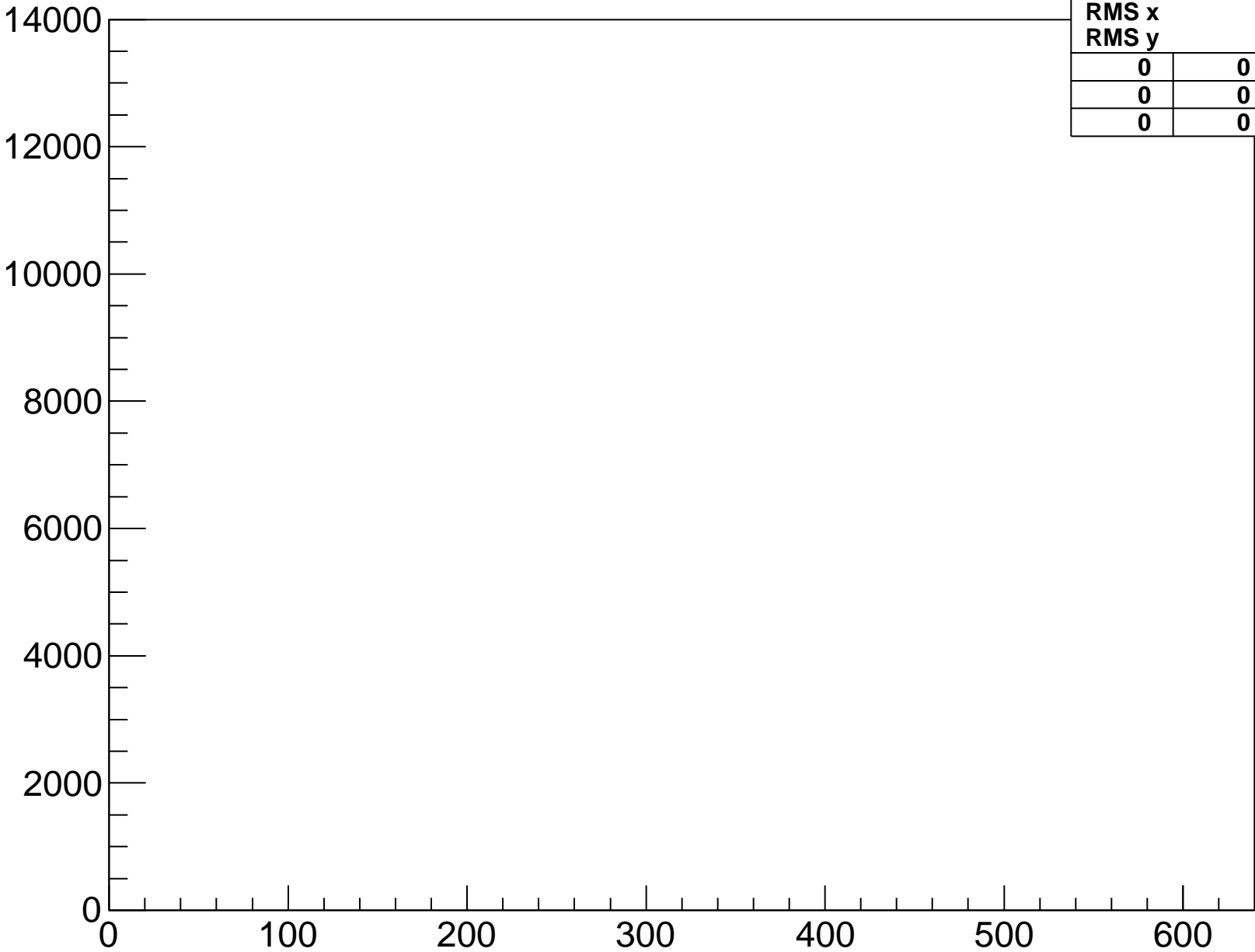


baselinesamples-fpga-3-hyb-2-sample-4



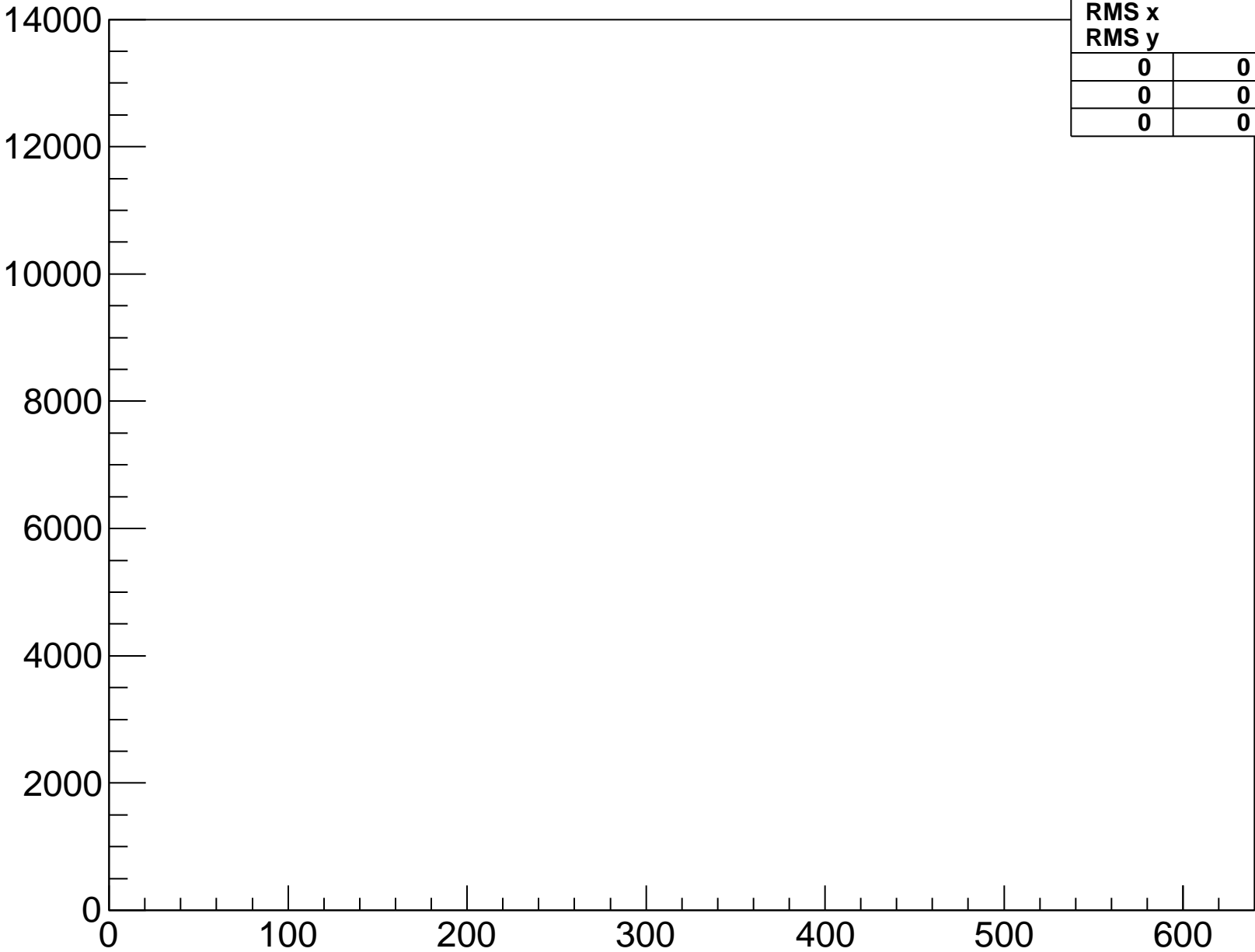
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-3-hyb-2-sample-5



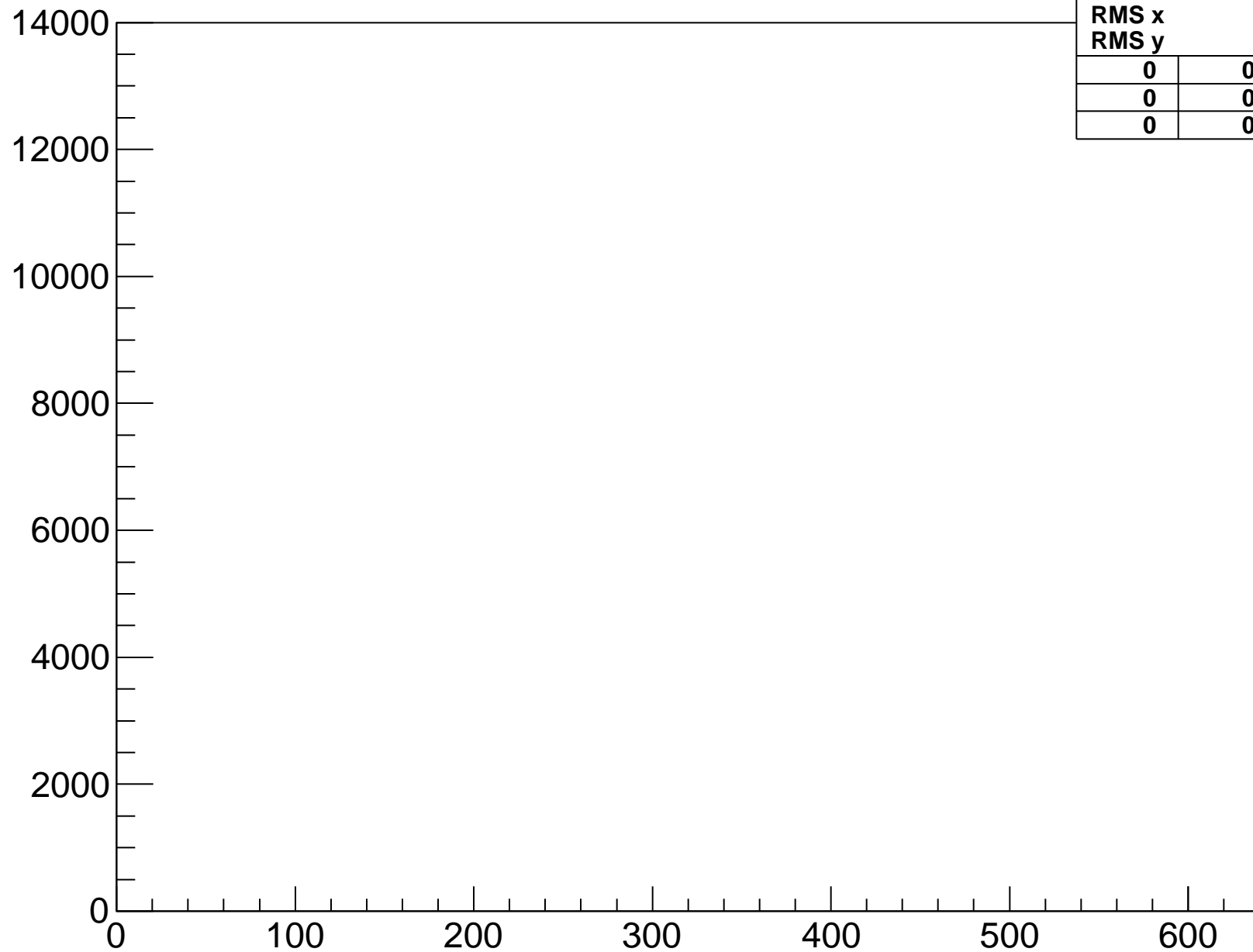
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-3-hyb-3-sample-0



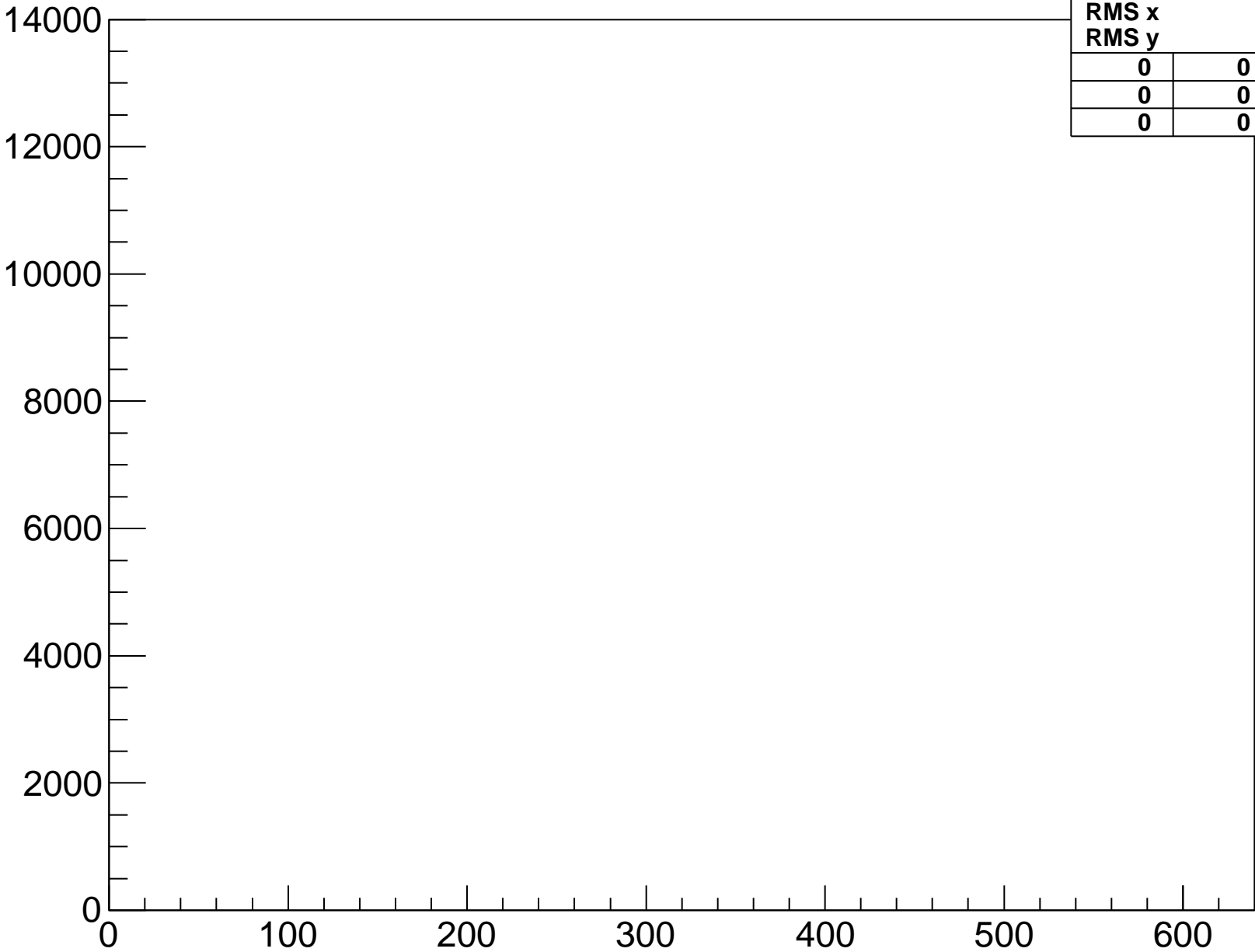
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-3-hyb-3-sample-1



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

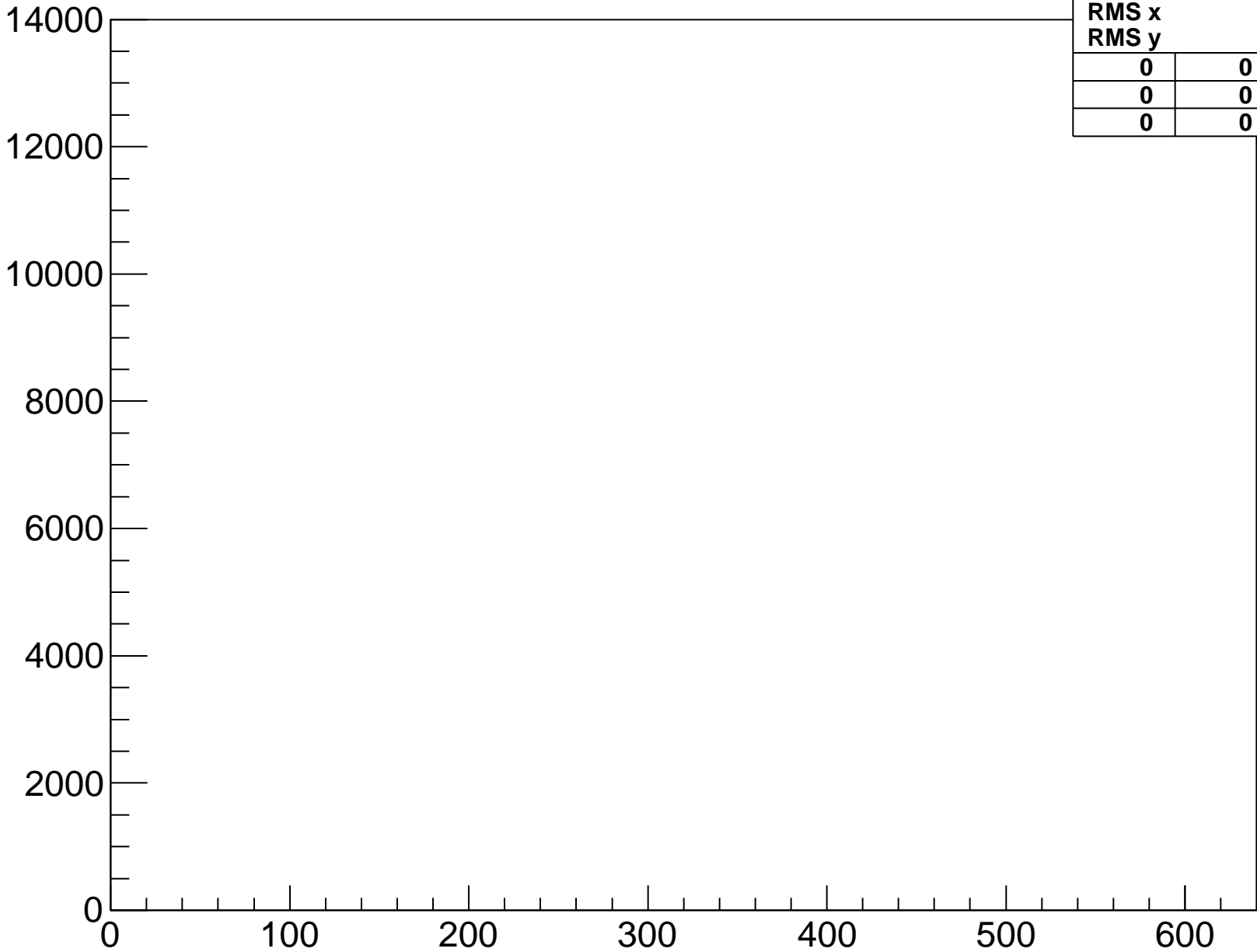
baselinesamples-fpga-3-hyb-3-sample-2



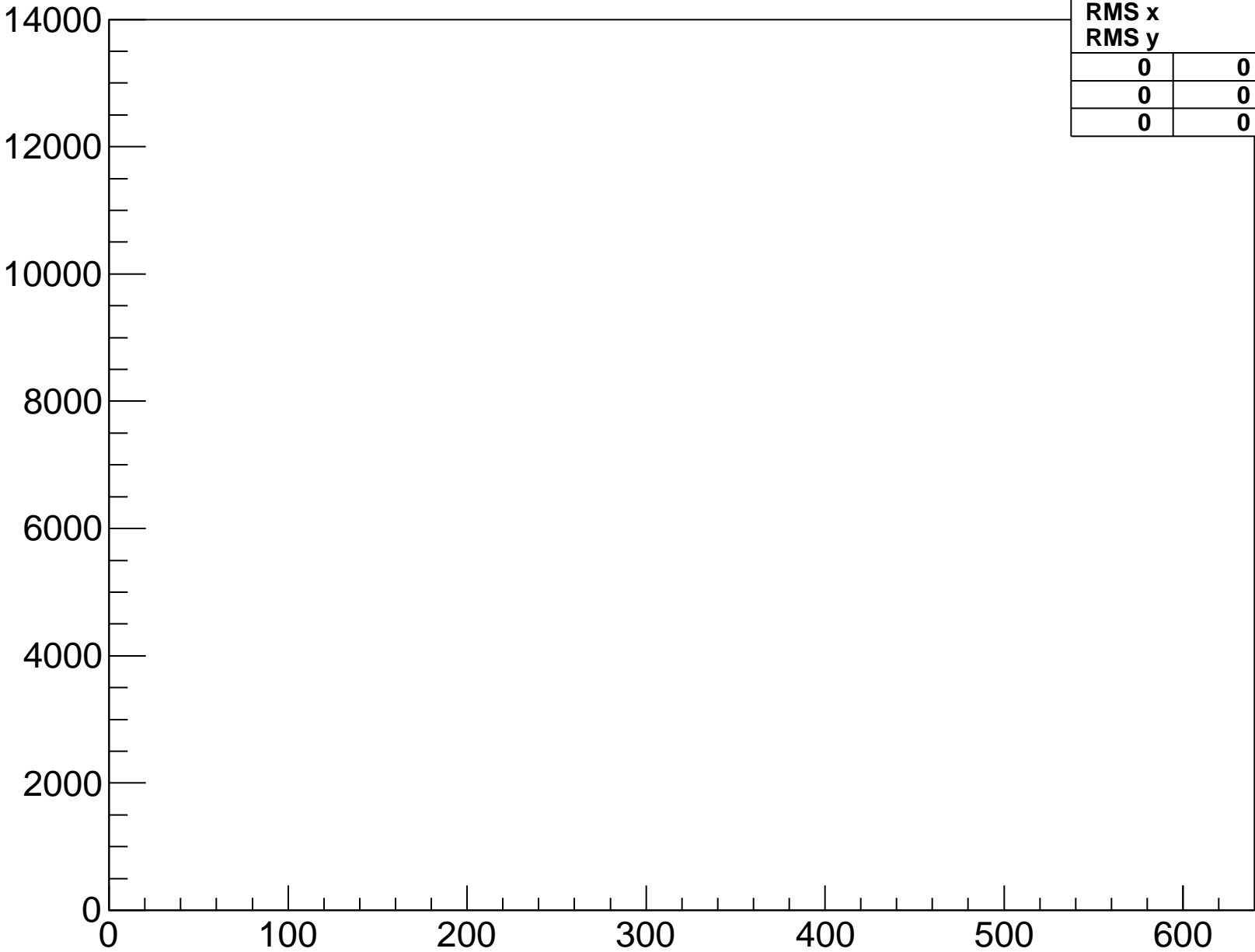
Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-3-hyb-3-sample-3

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



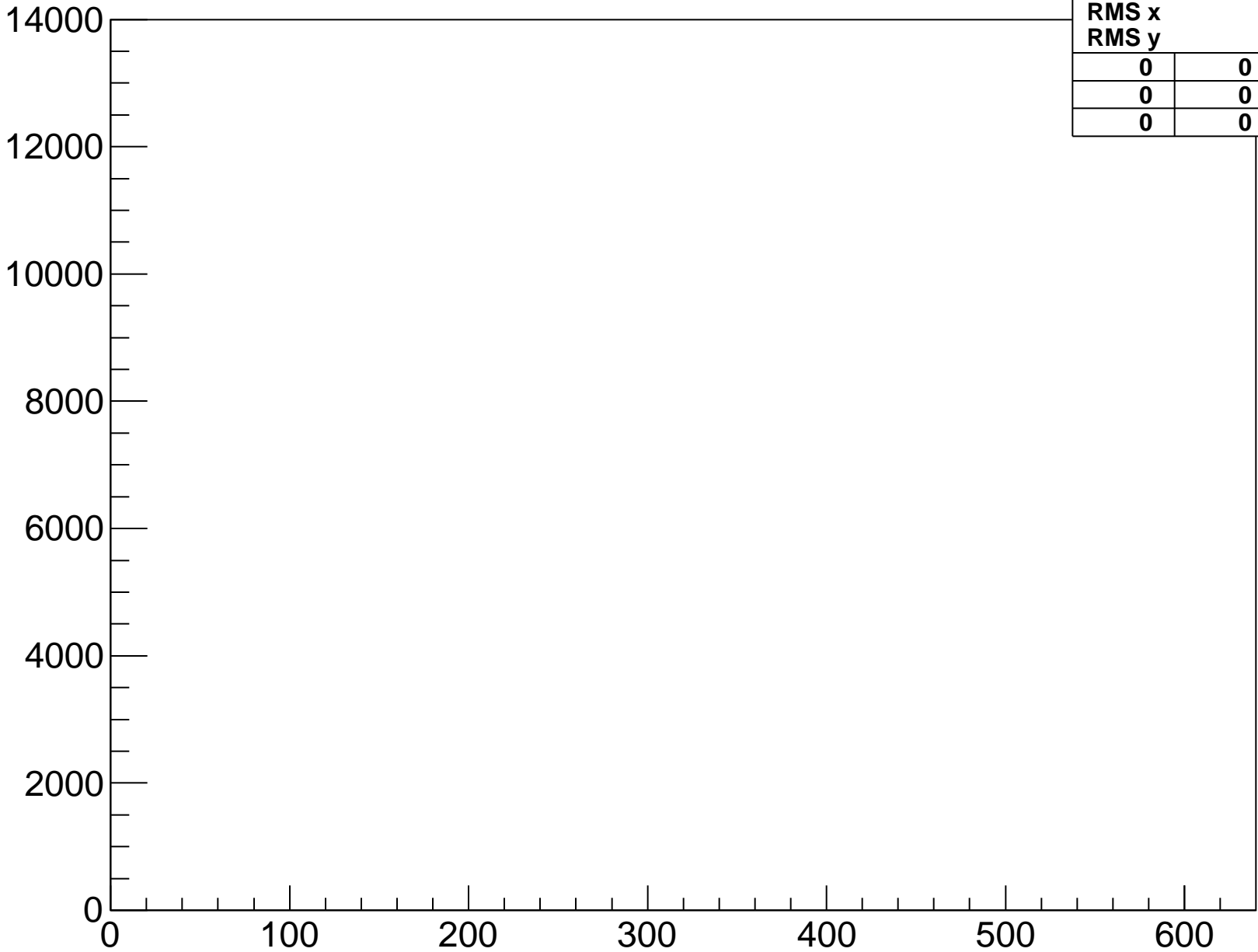
baselinesamples-fpga-3-hyb-3-sample-4



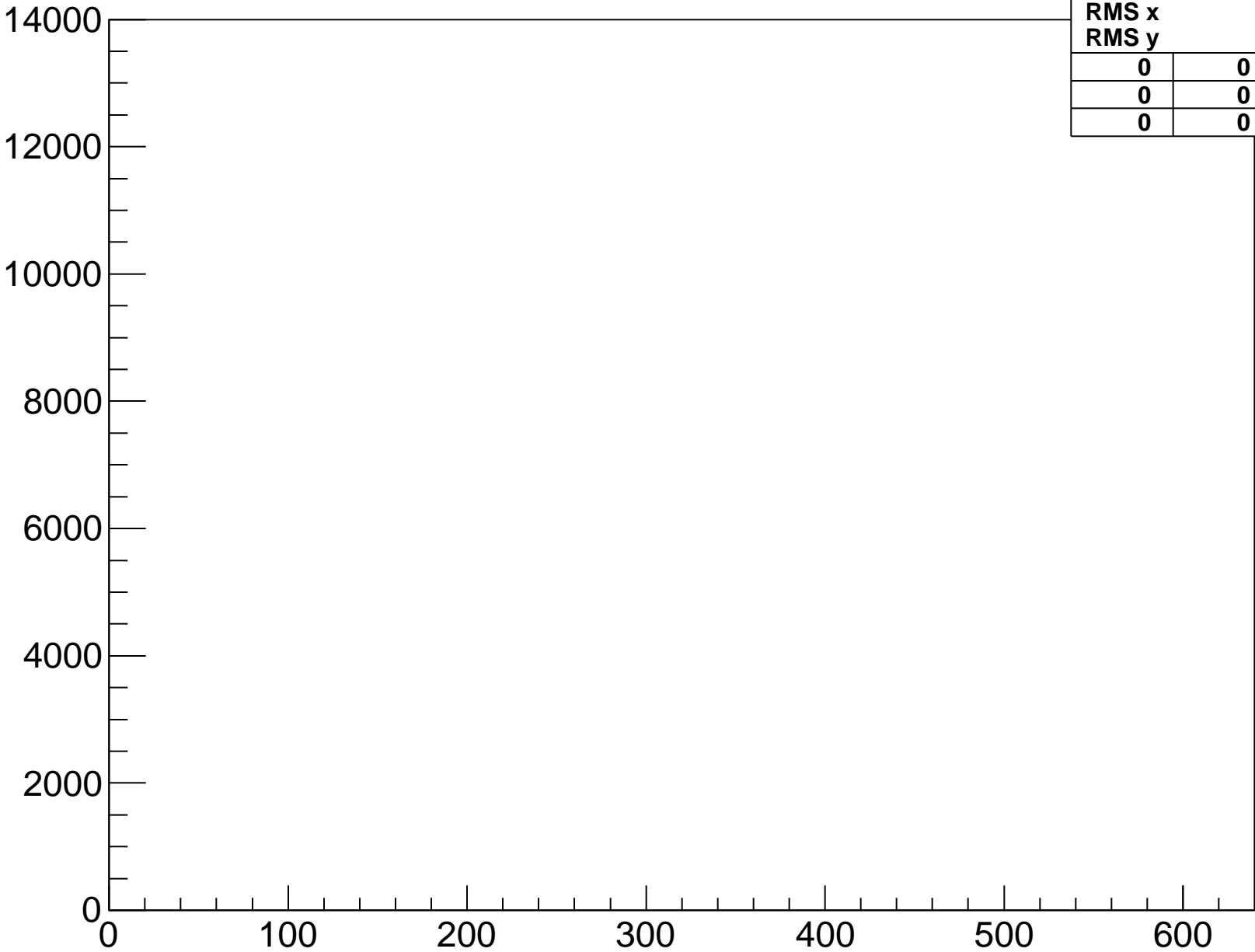
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-3-hyb-3-sample-5

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



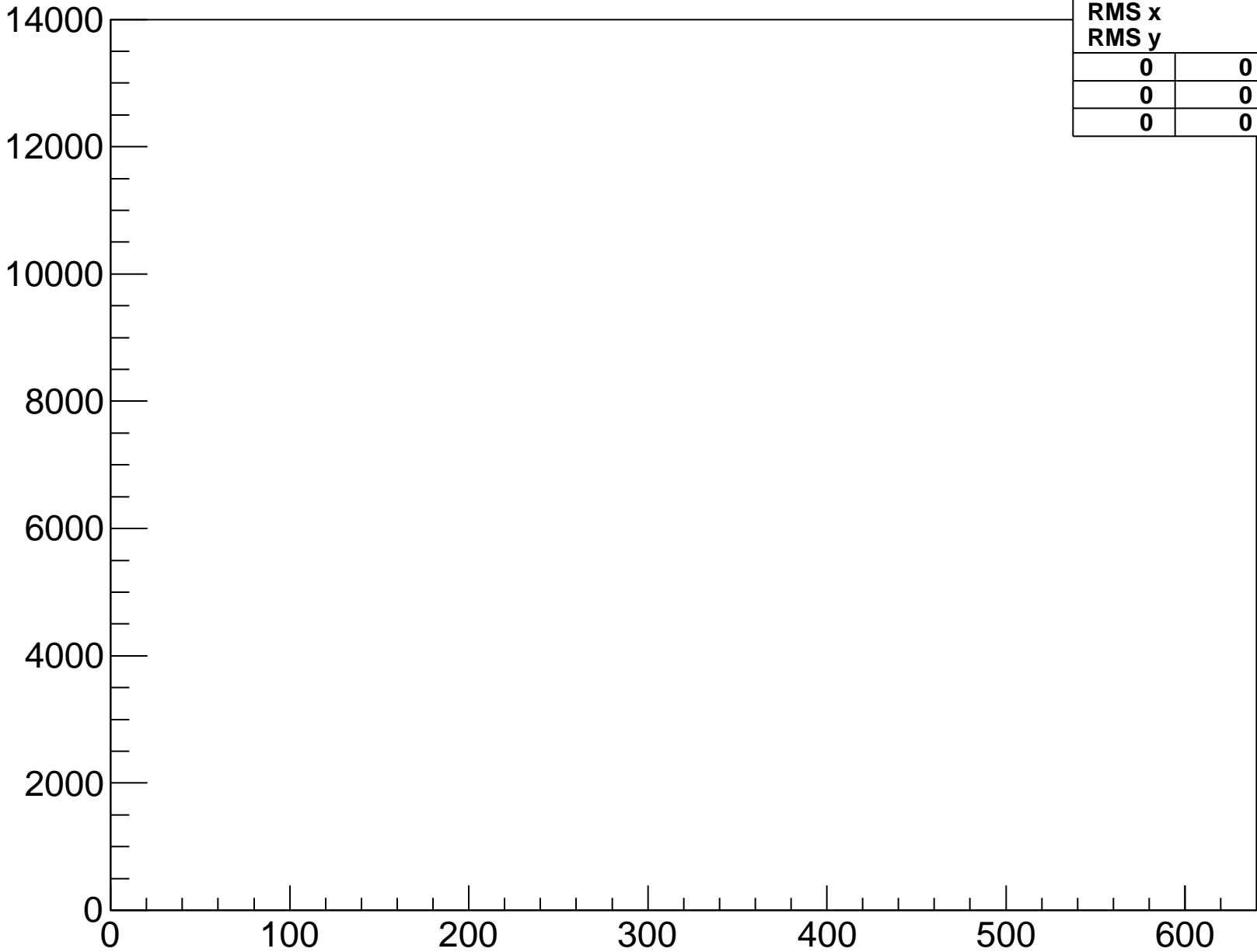
baselinesamples-fpga-4-hyb-0-sample-0



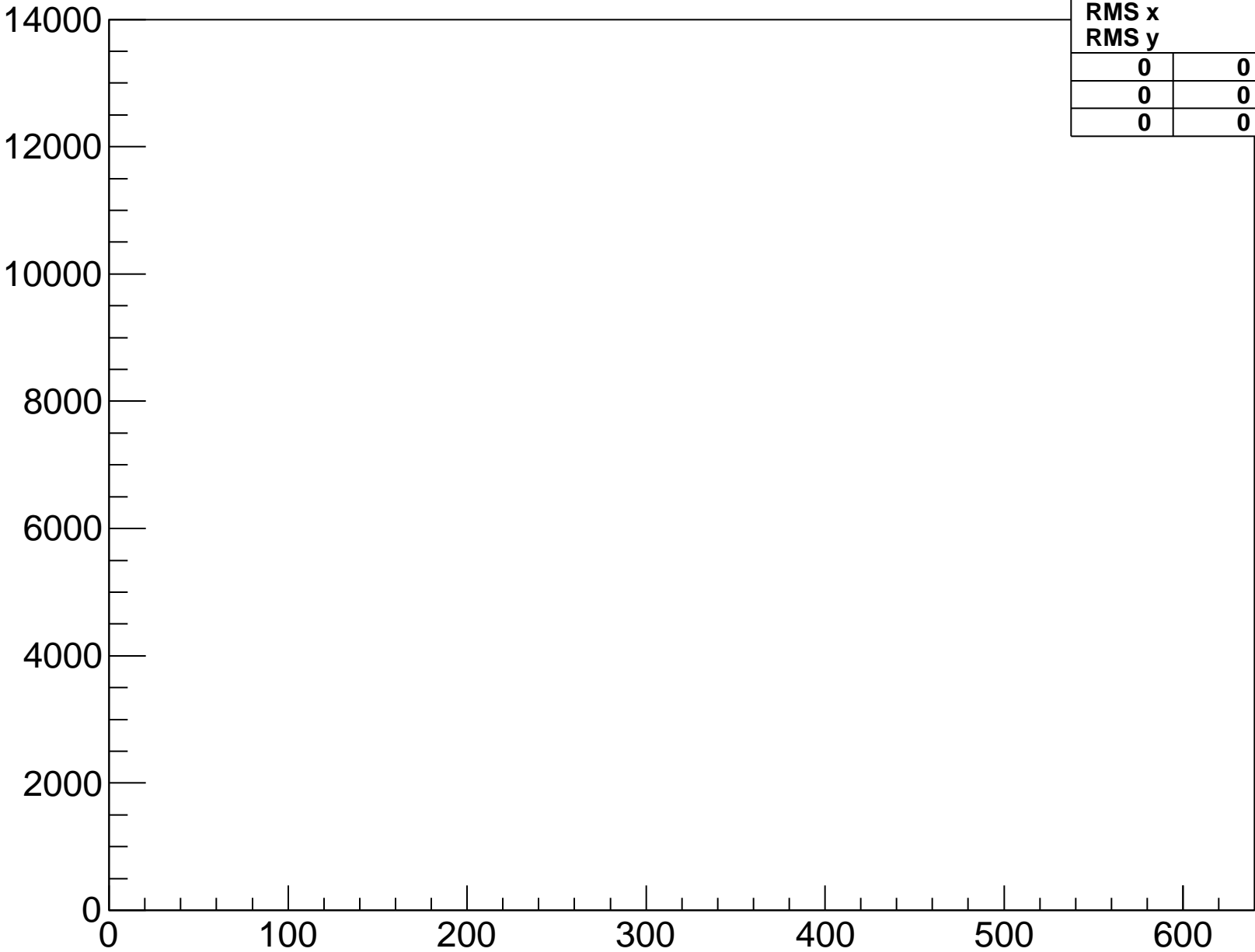
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-4-hyb-0-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



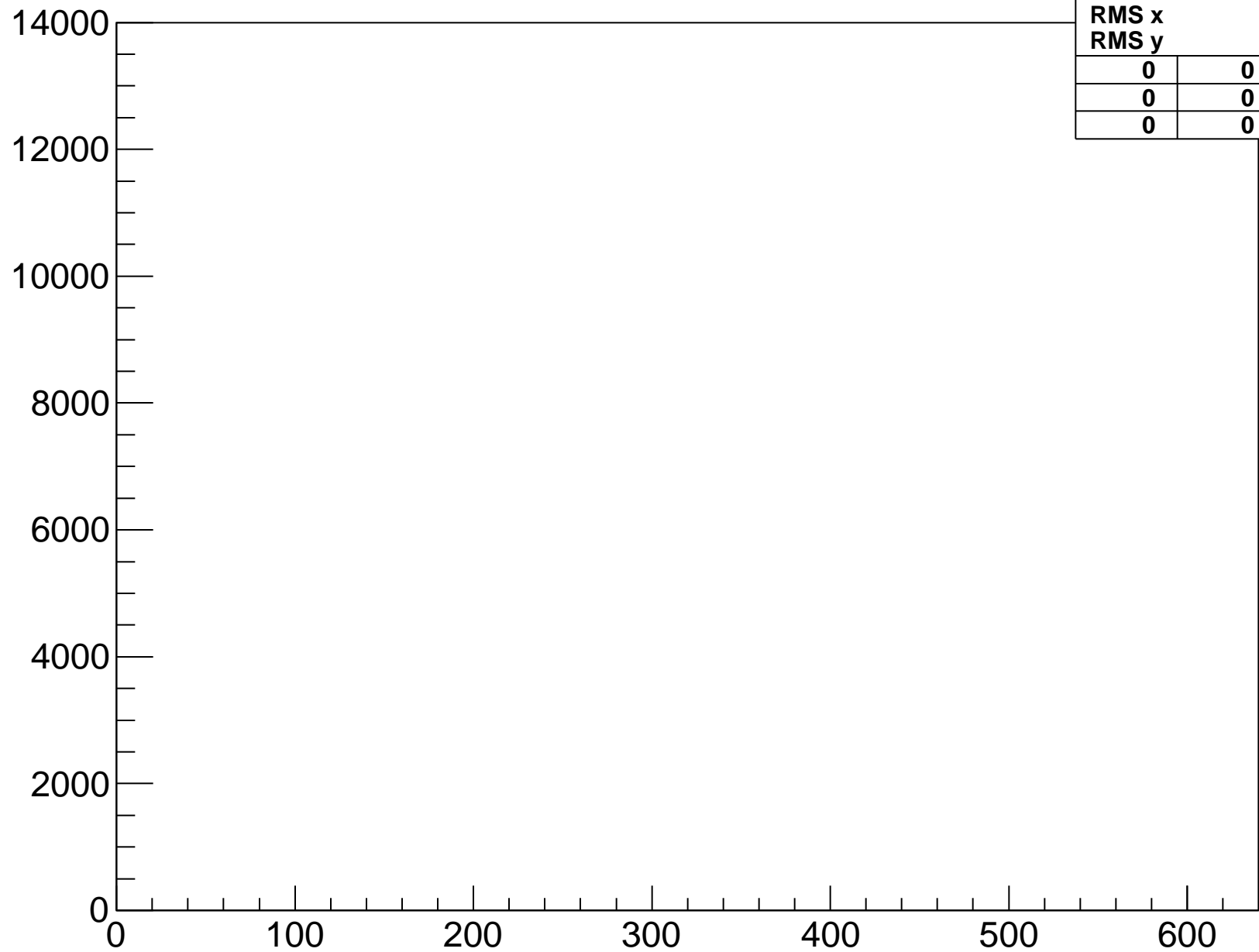
baselinesamples-fpga-4-hyb-0-sample-2



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

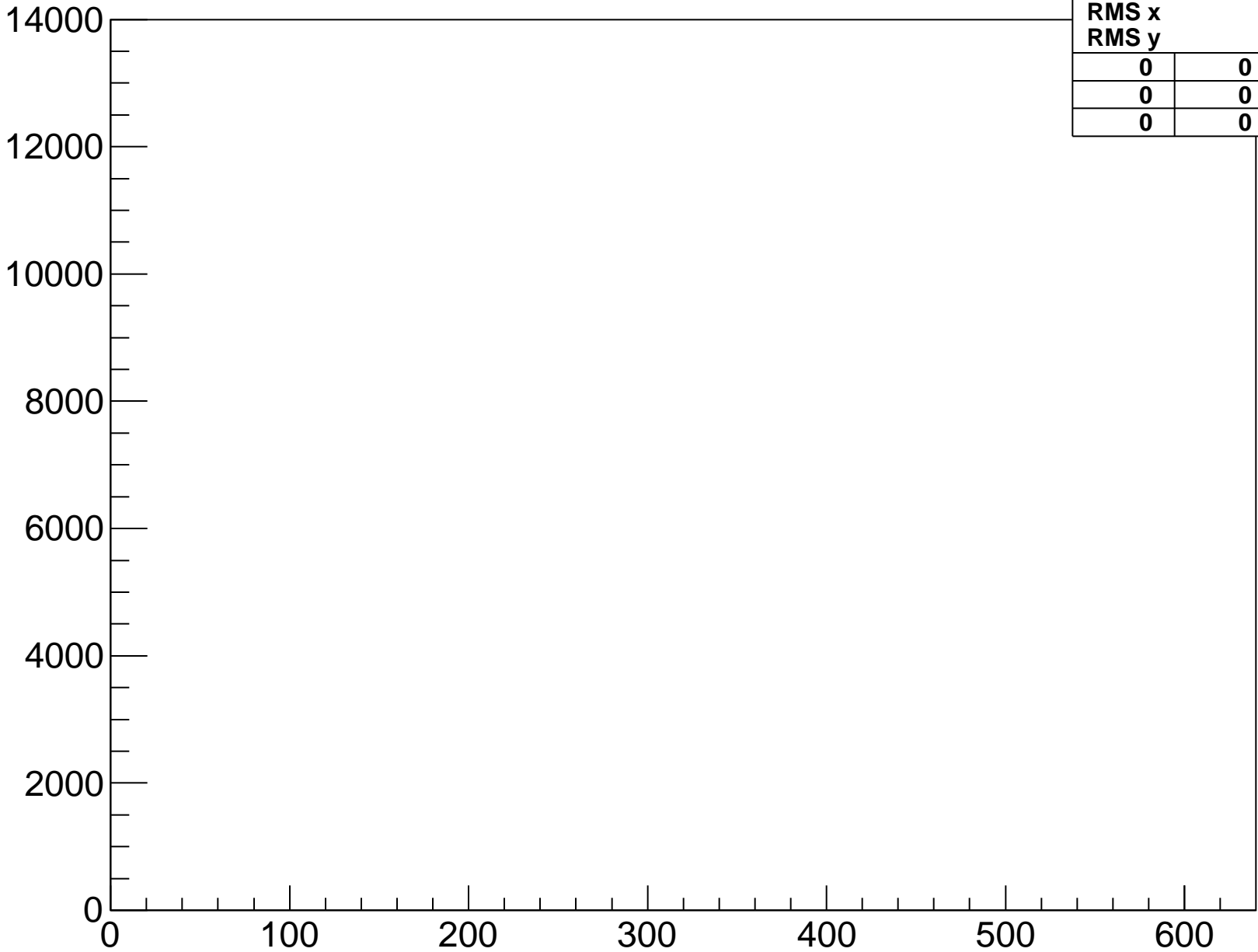
baselinesamples-fpga-4-hyb-0-sample-3

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



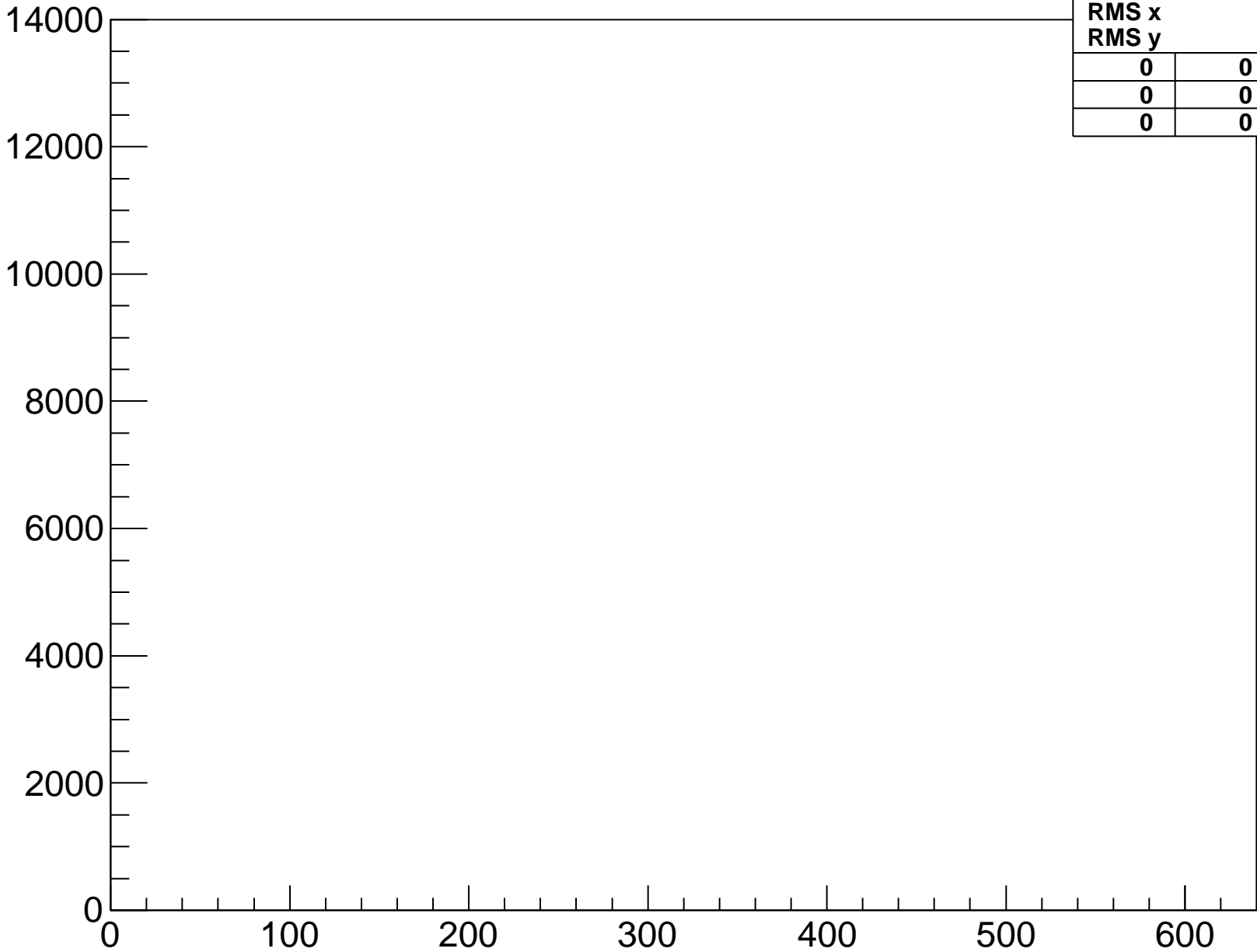
baselinesamples-fpga-4-hyb-0-sample-4

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

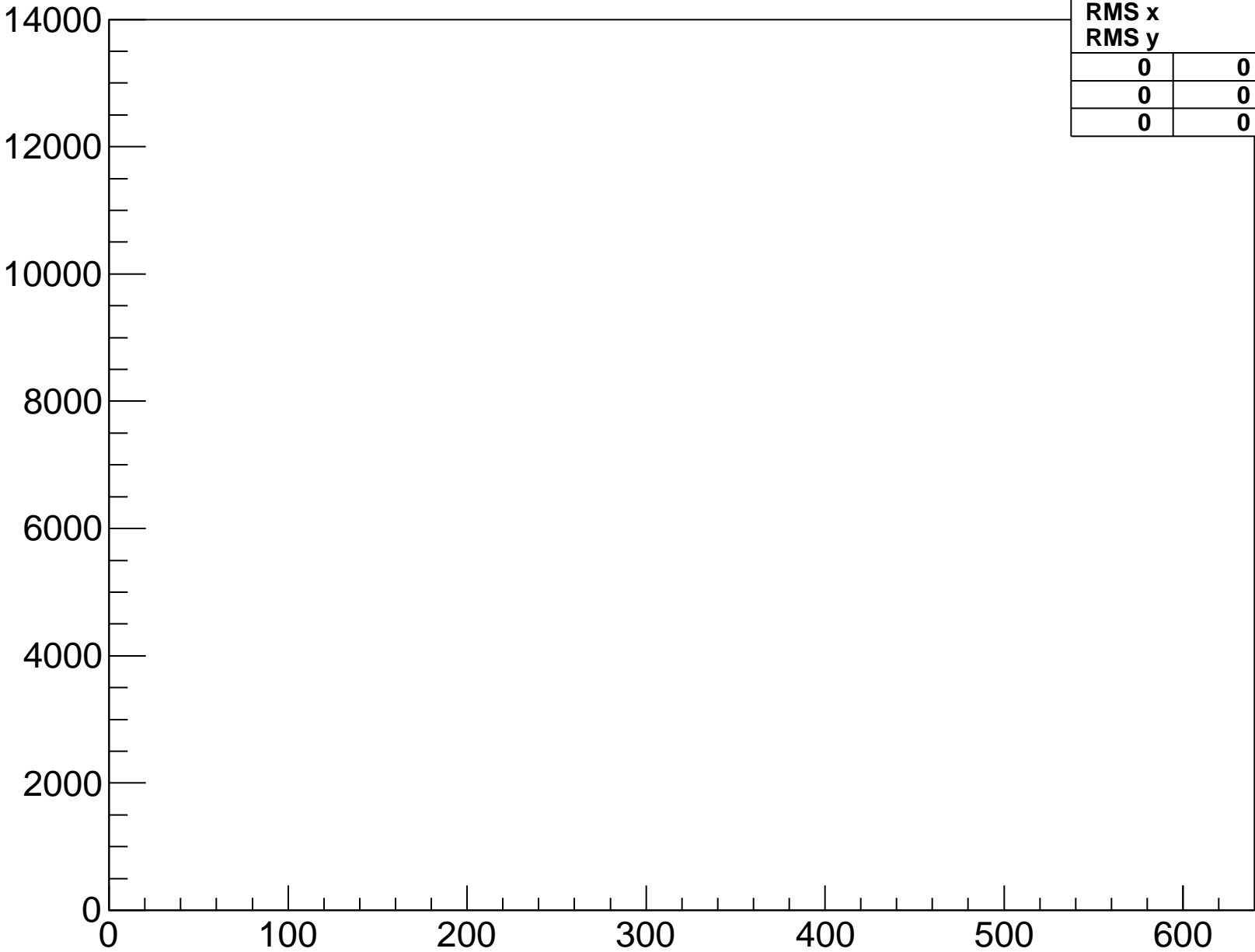


baselinesamples-fpga-4-hyb-0-sample-5

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



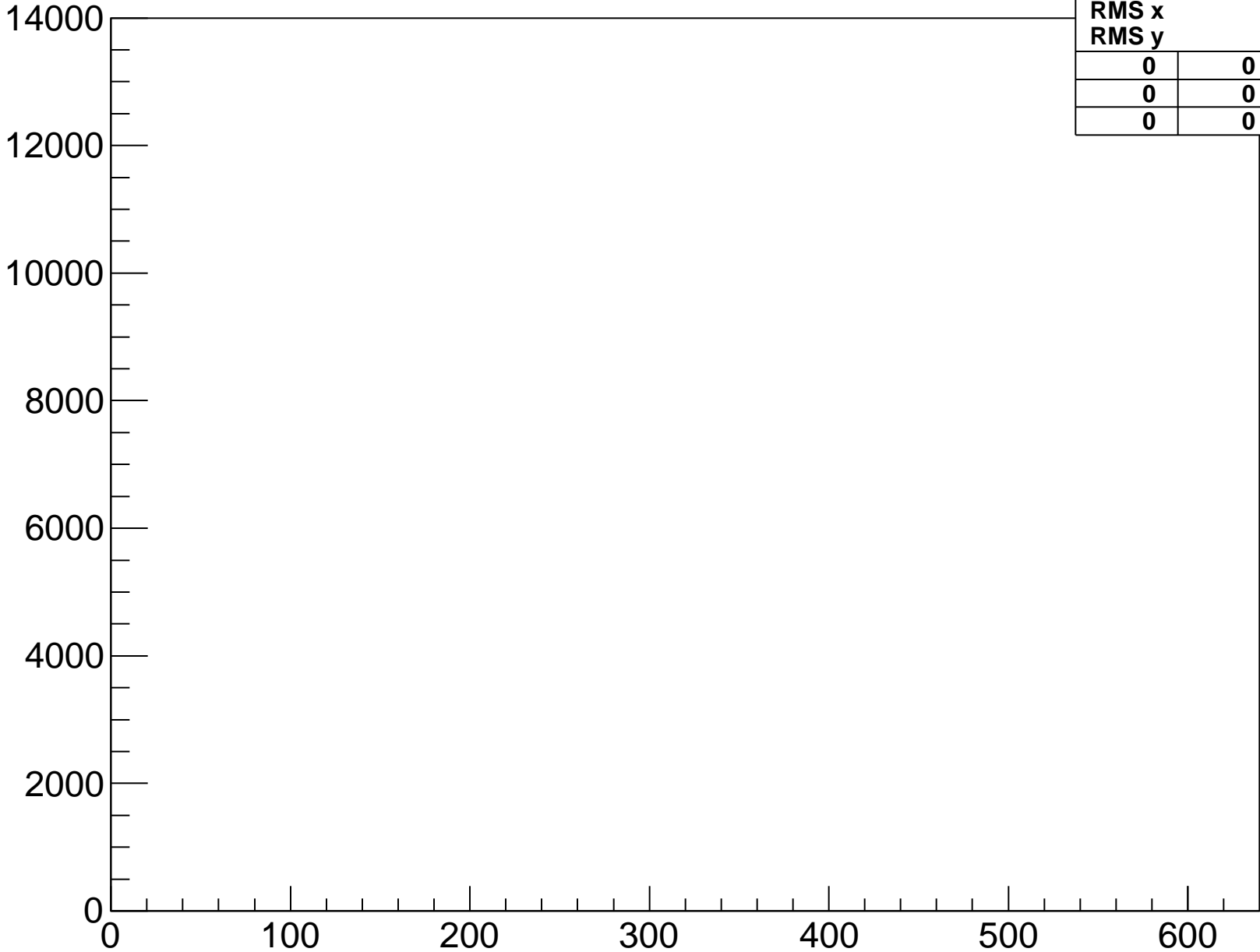
baselinesamples-fpga-4-hyb-1-sample-0



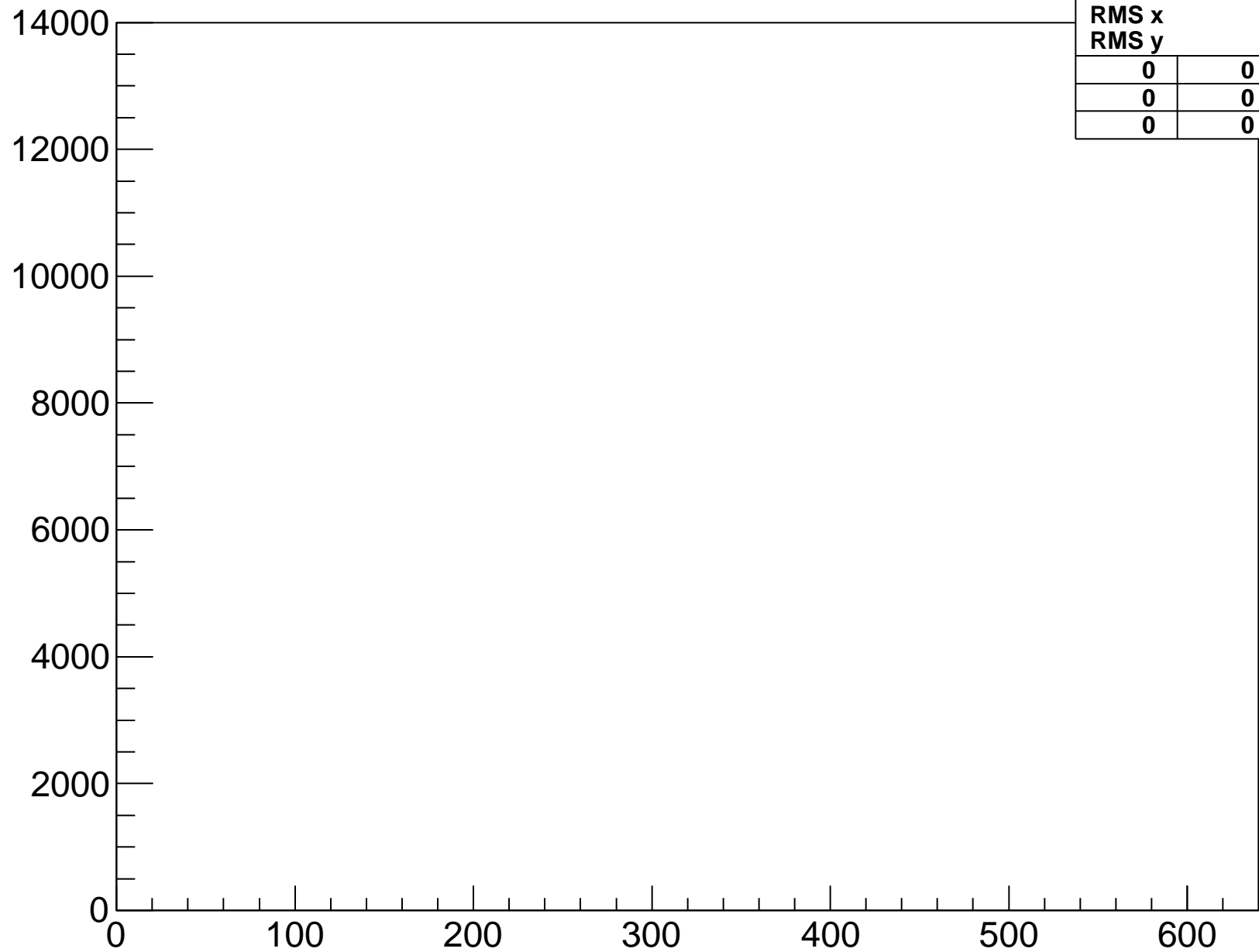
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-4-hyb-1-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

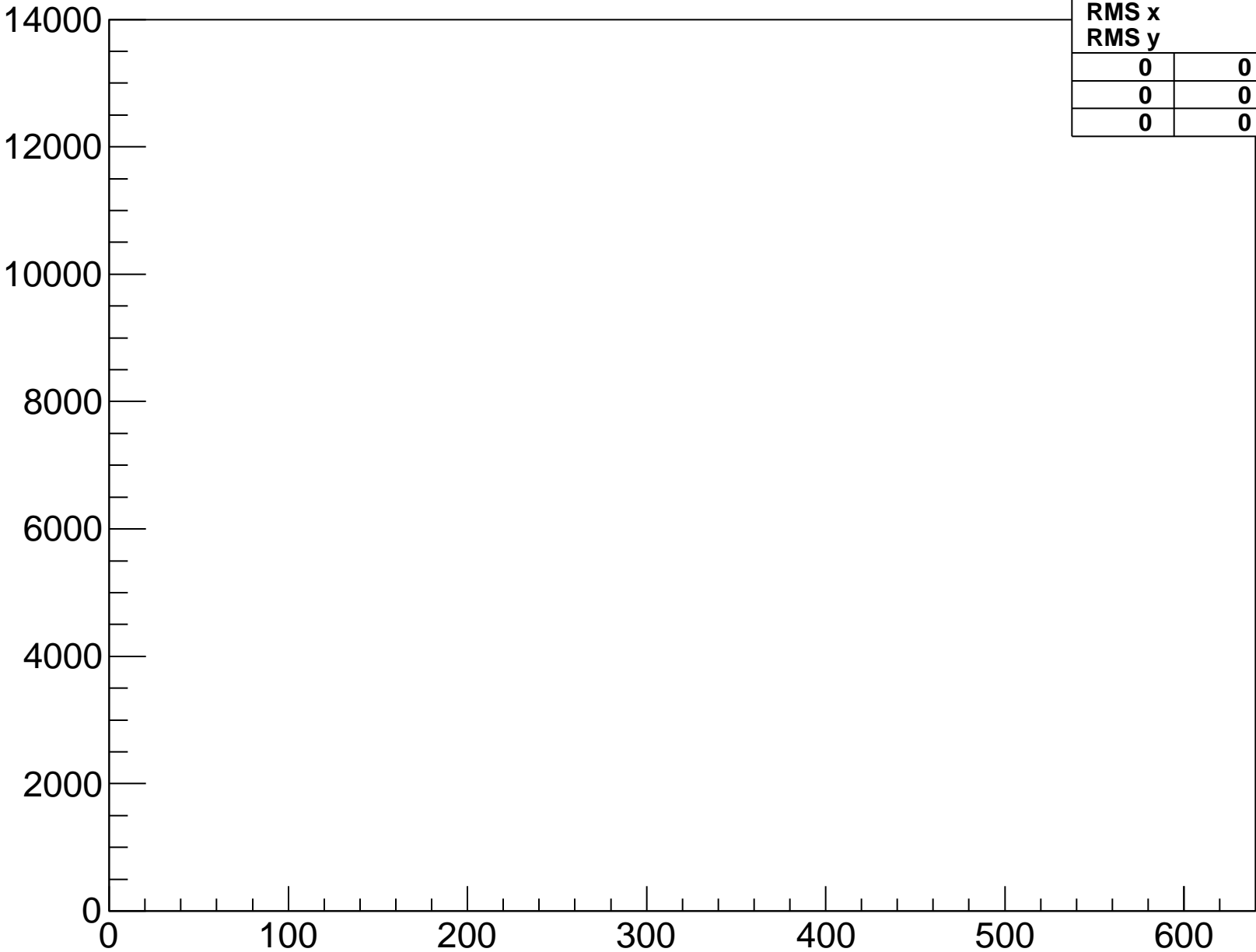


baselinesamples-fpga-4-hyb-1-sample-2



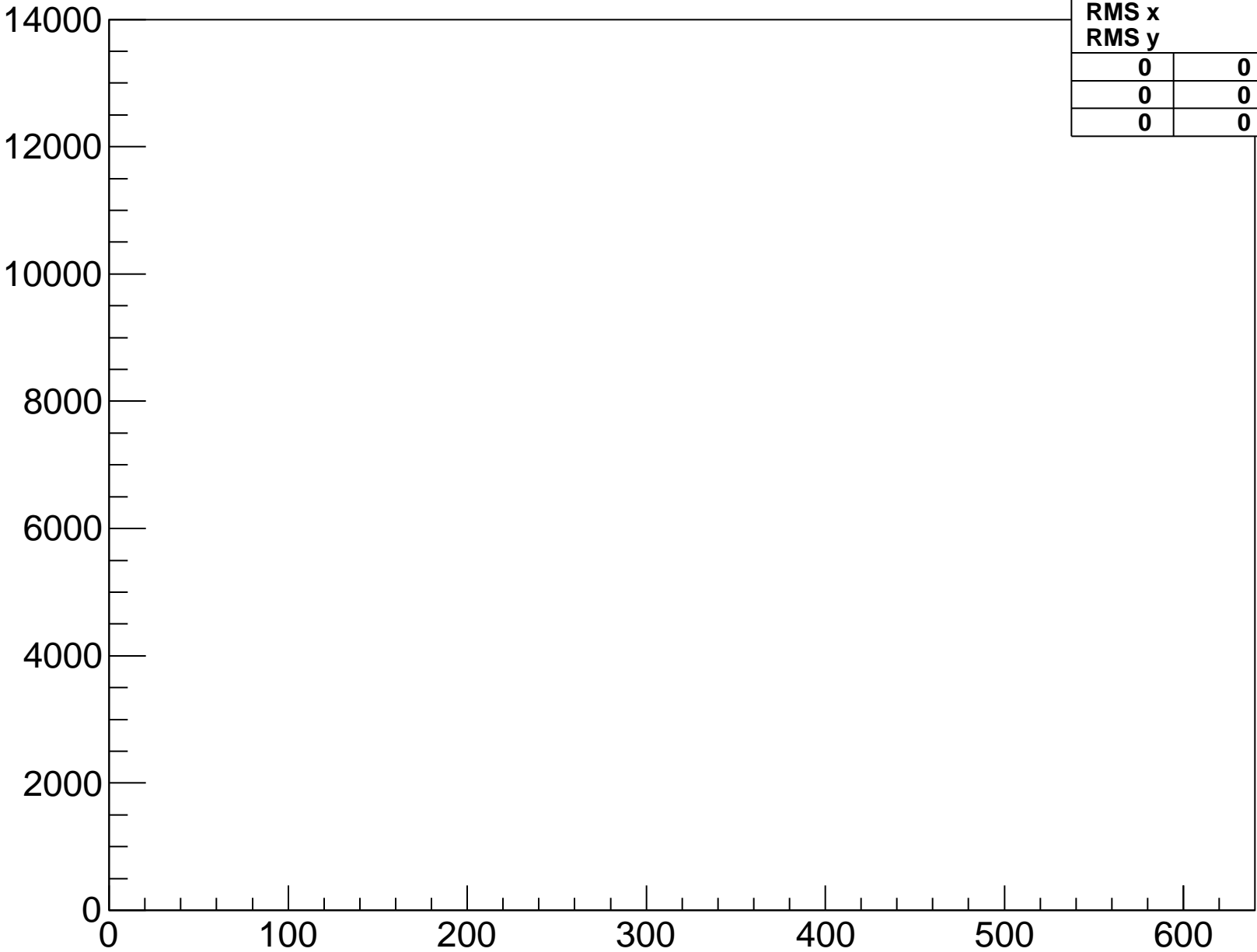
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-4-hyb-1-sample-3



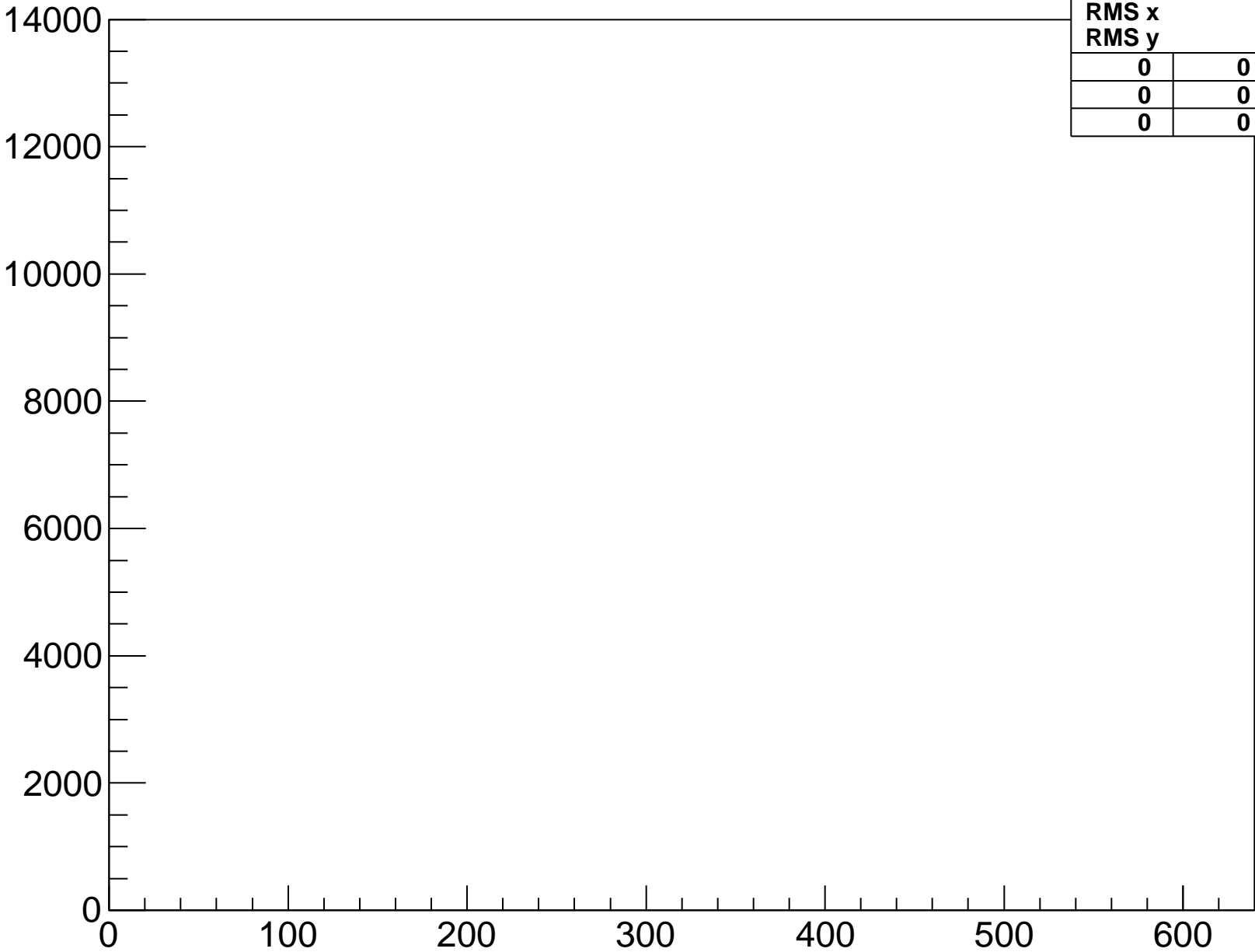
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-4-hyb-1-sample-4



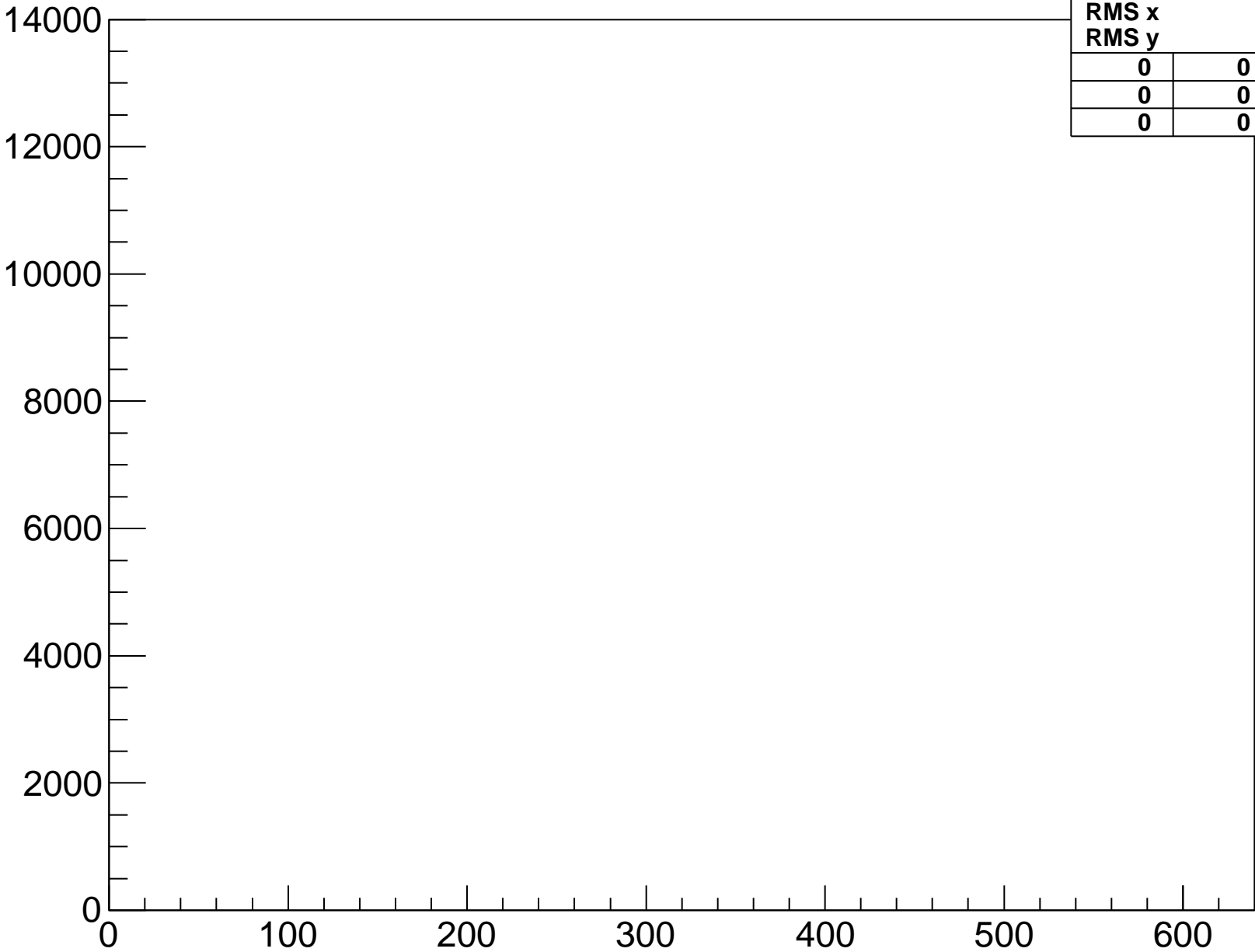
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-4-hyb-1-sample-5



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

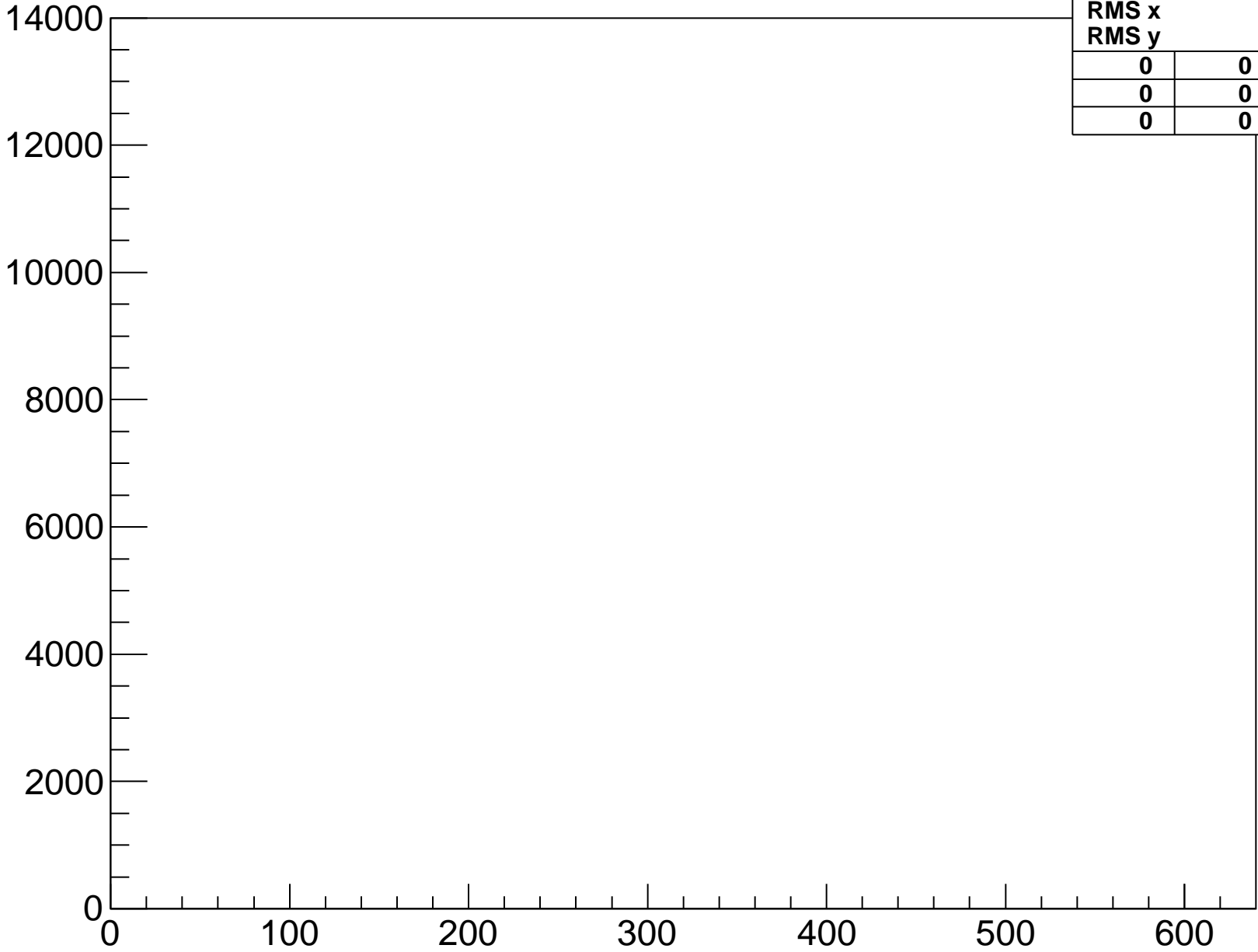
baselinesamples-fpga-4-hyb-2-sample-0



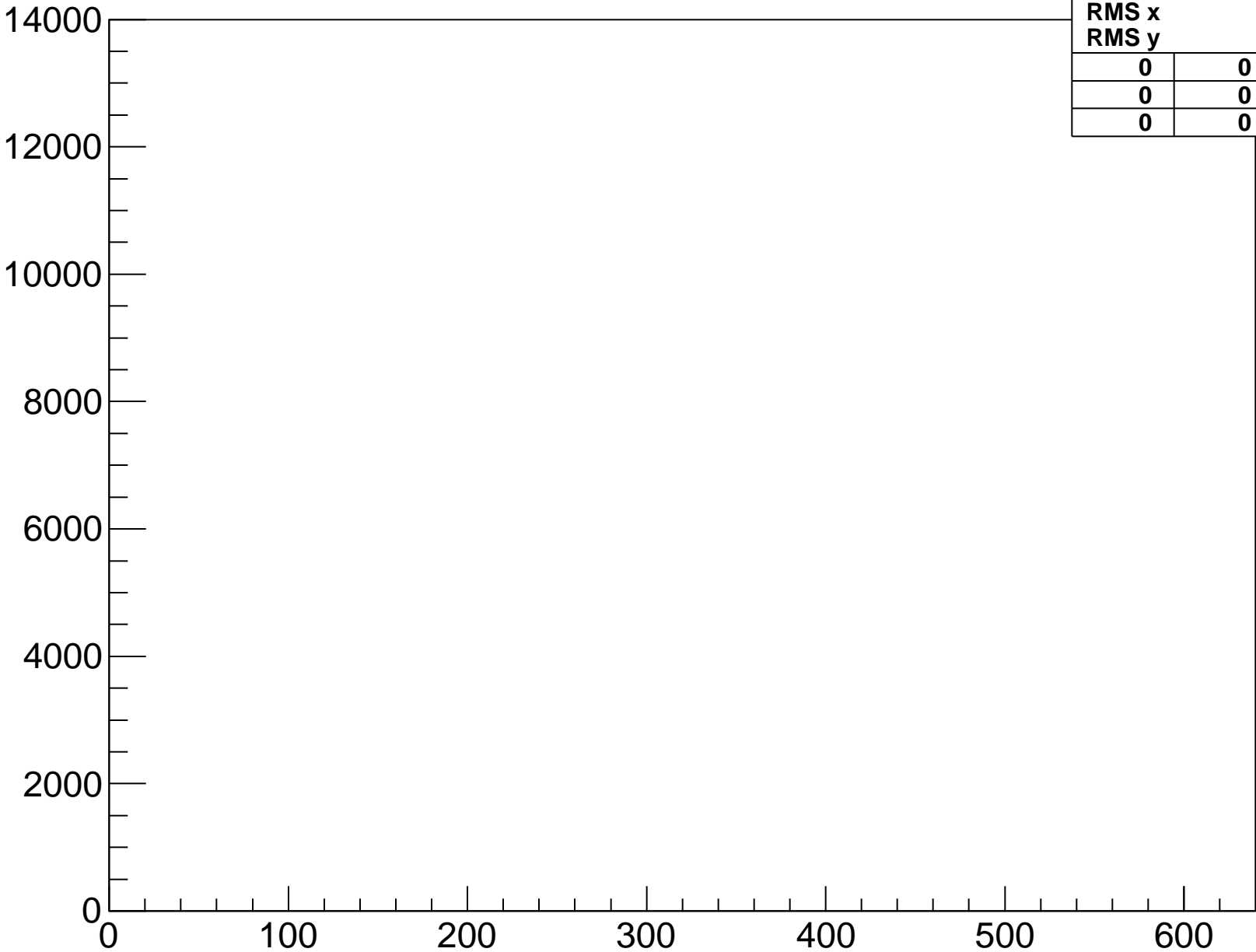
Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	
0	0	0	
0	0	0	

baselinesamples-fpga-4-hyb-2-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

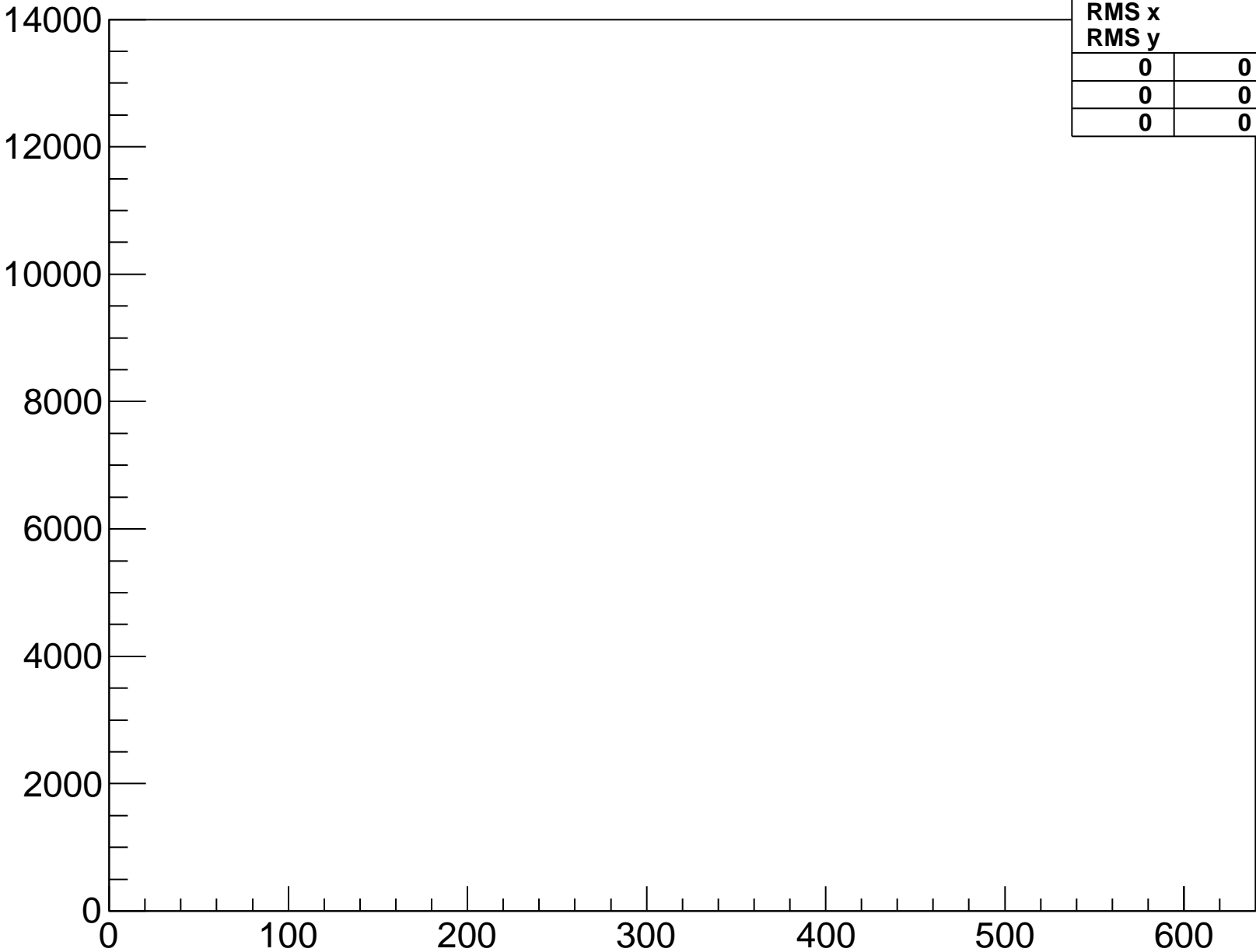


baselinesamples-fpga-4-hyb-2-sample-2



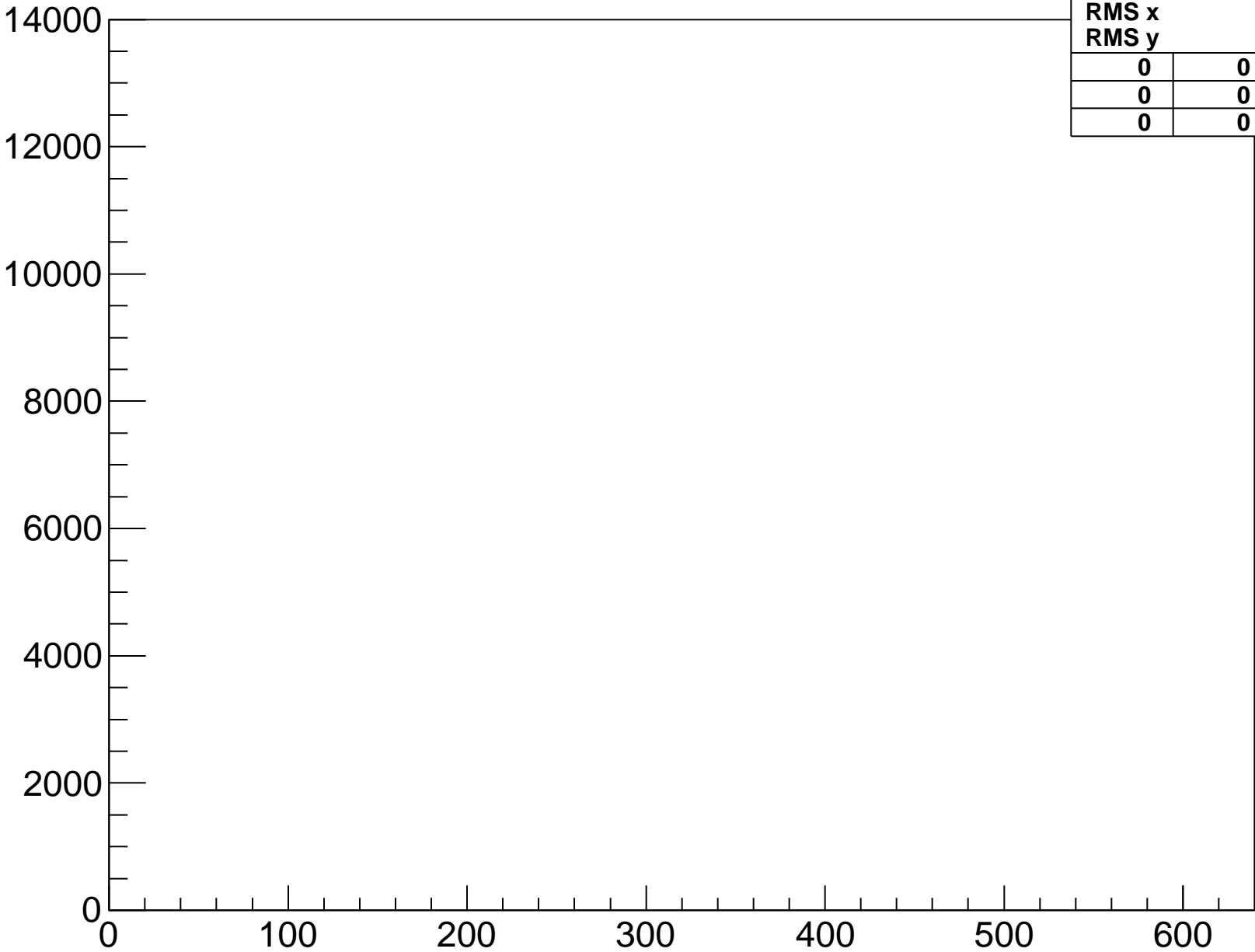
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-4-hyb-2-sample-3



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

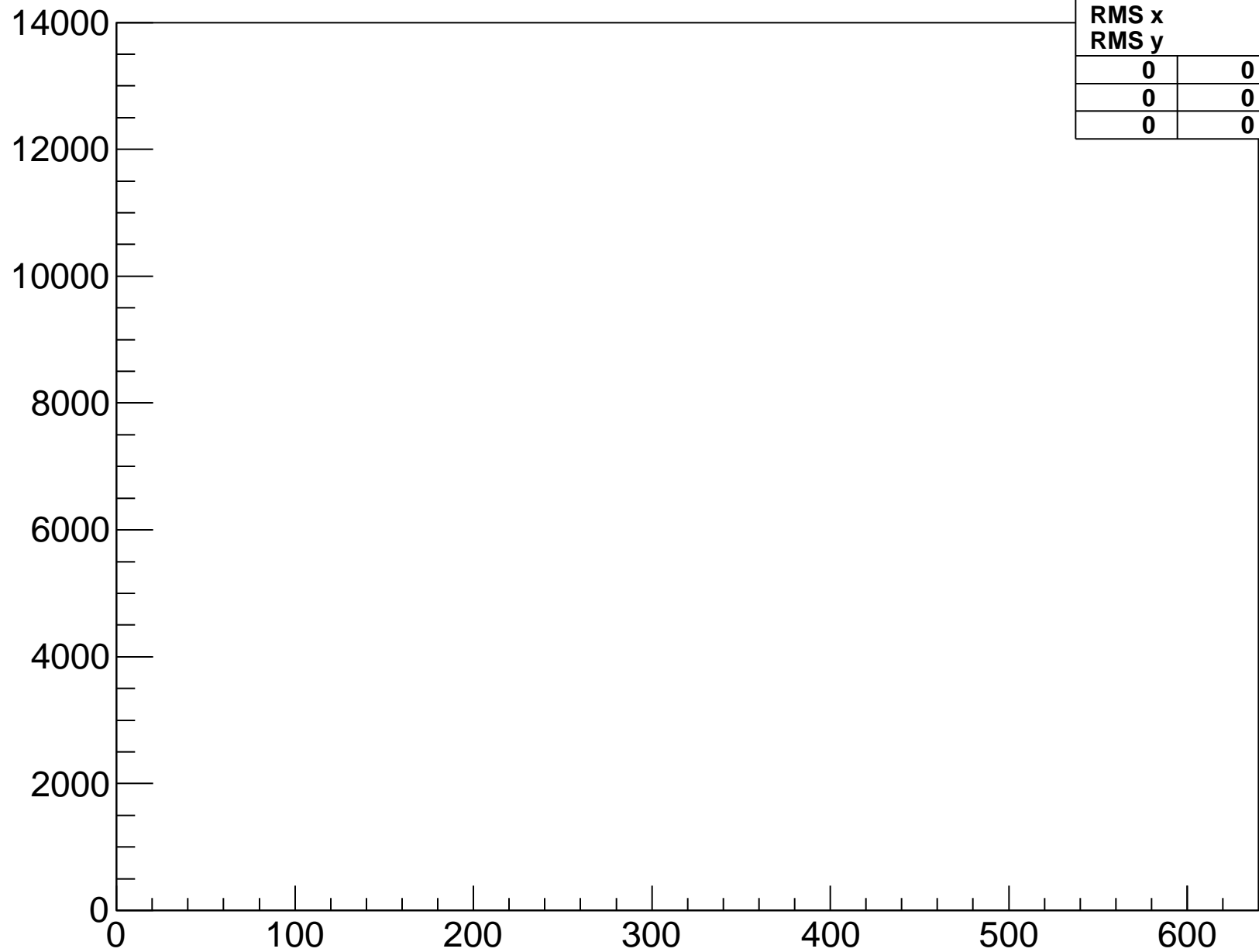
baselinesamples-fpga-4-hyb-2-sample-4



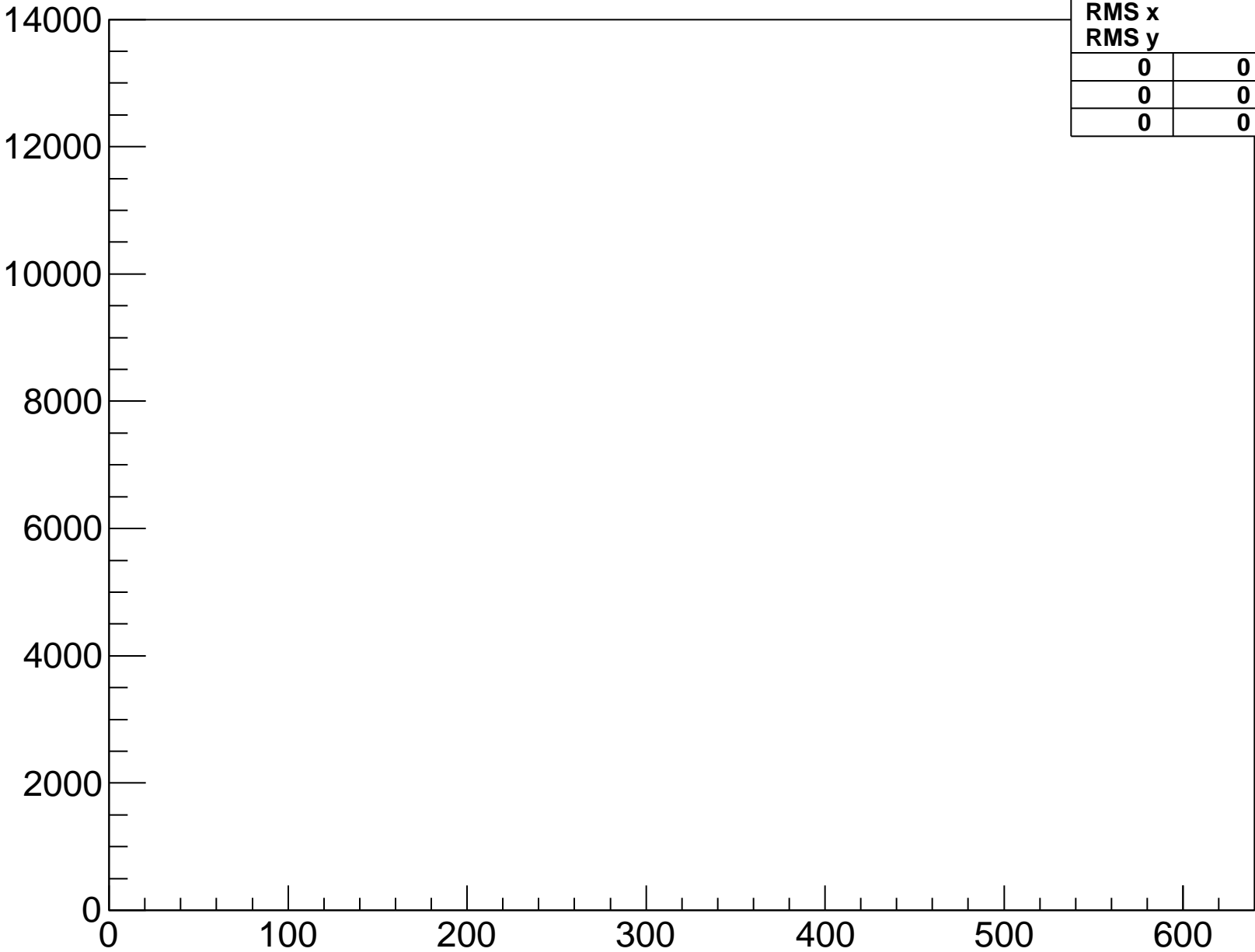
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-4-hyb-2-sample-5

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



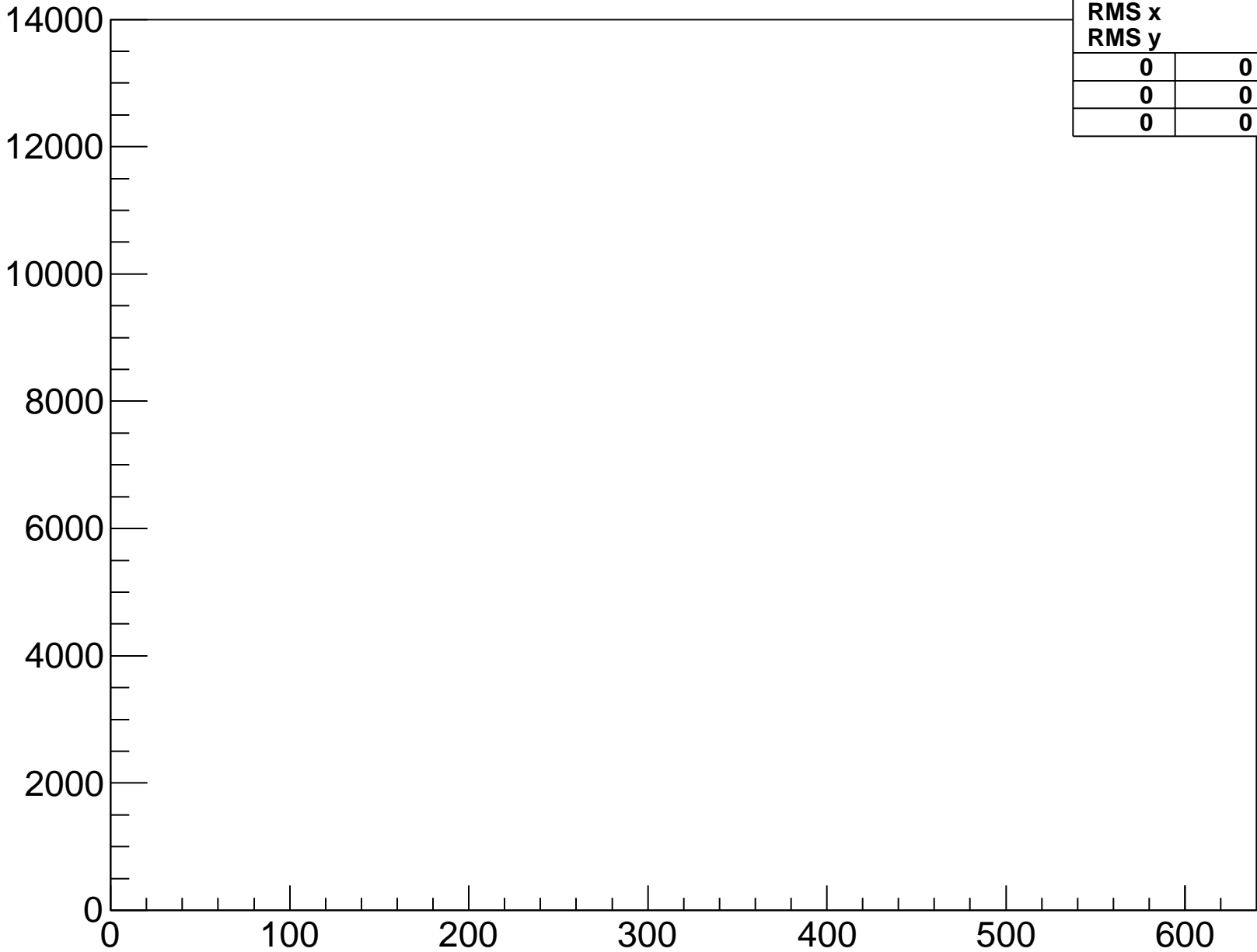
baselinesamples-fpga-4-hyb-3-sample-0



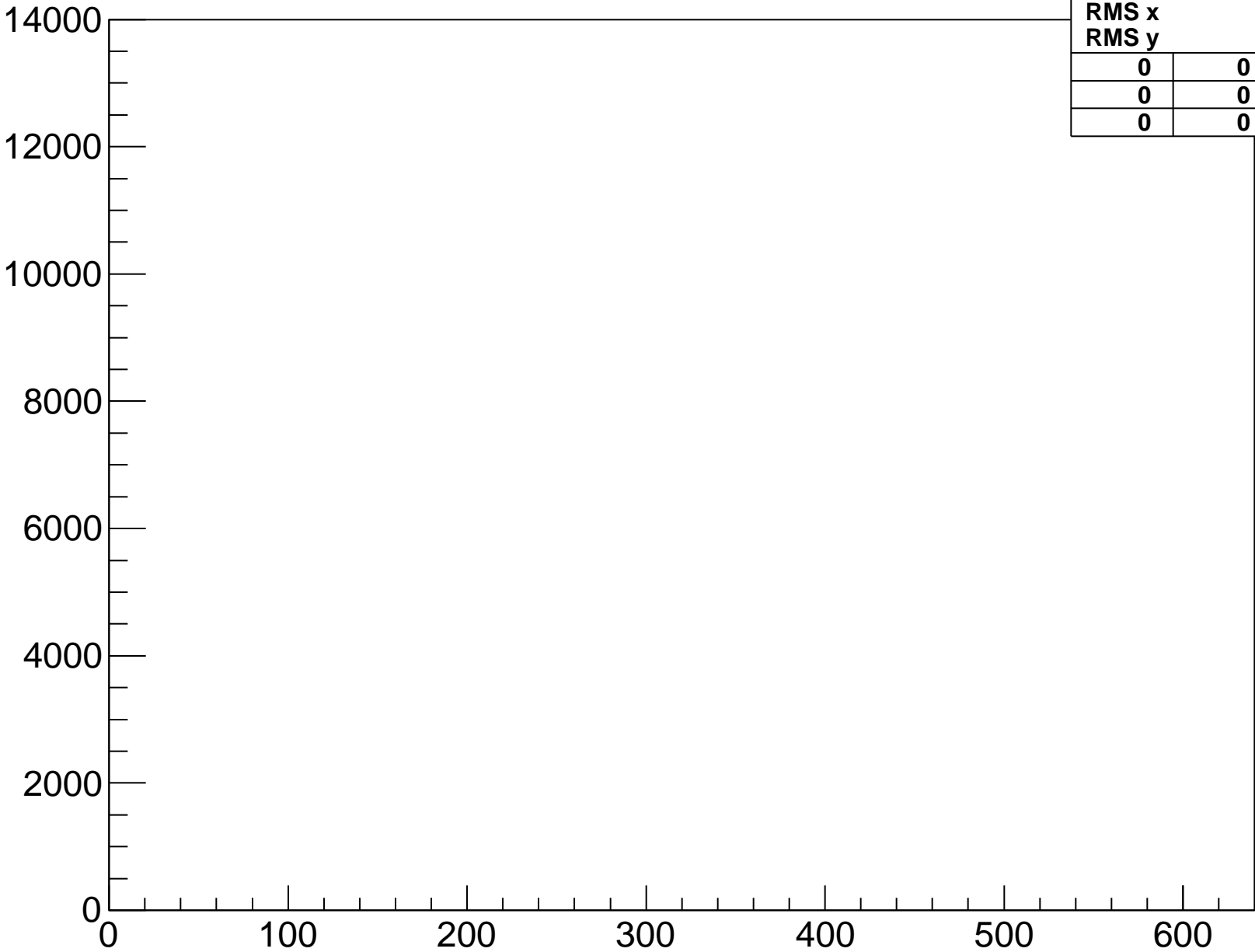
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-4-hyb-3-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	



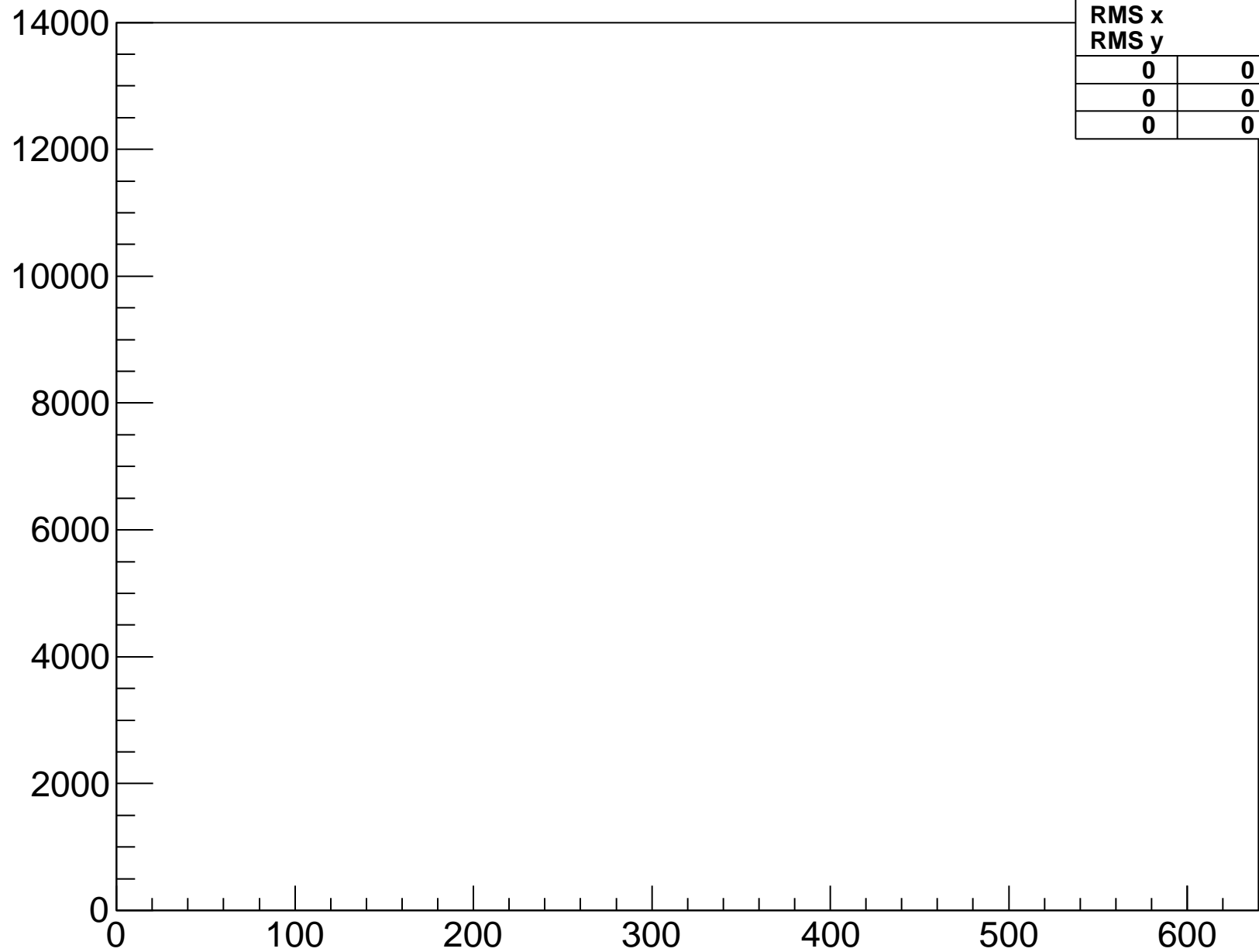
baselinesamples-fpga-4-hyb-3-sample-2



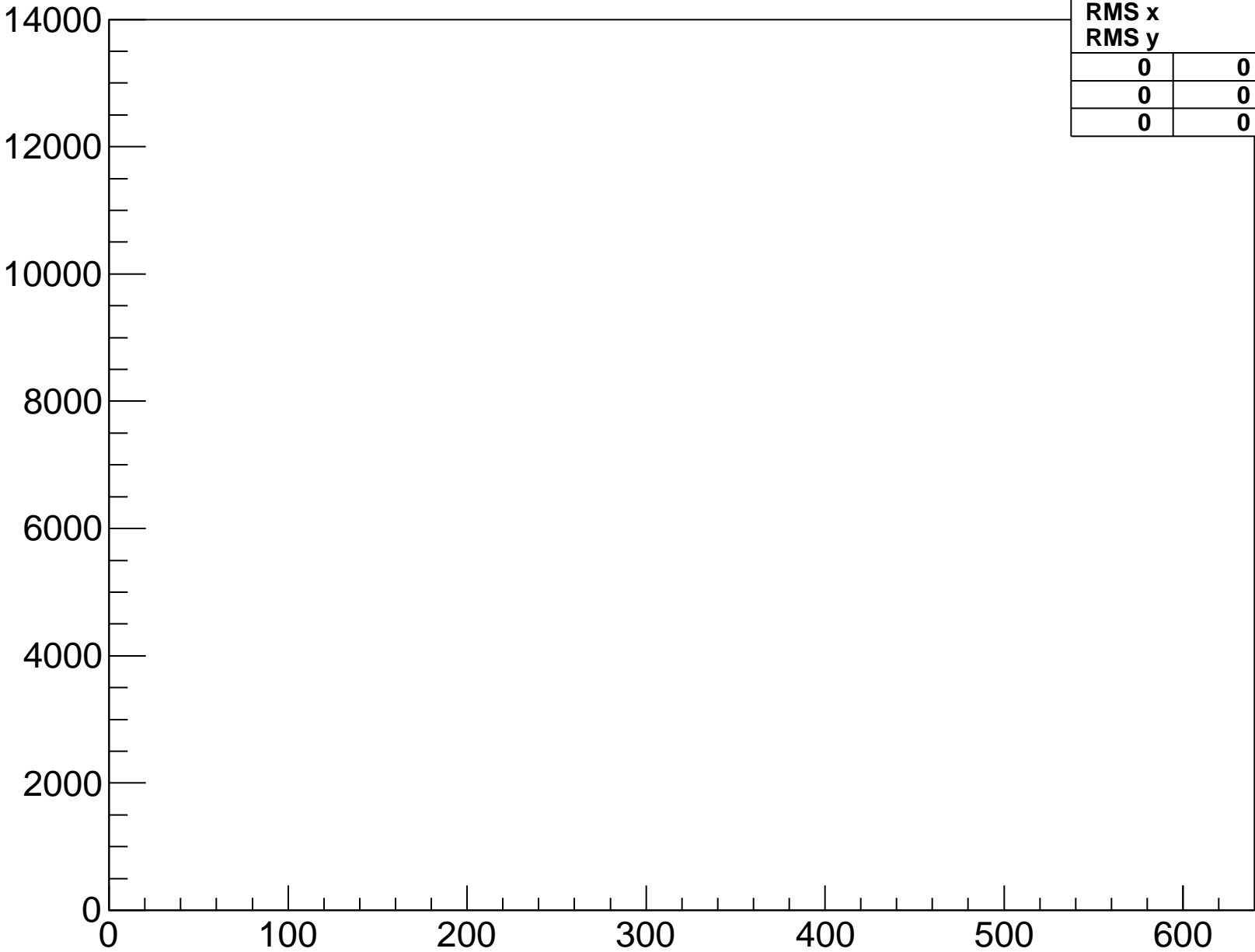
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-4-hyb-3-sample-3

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

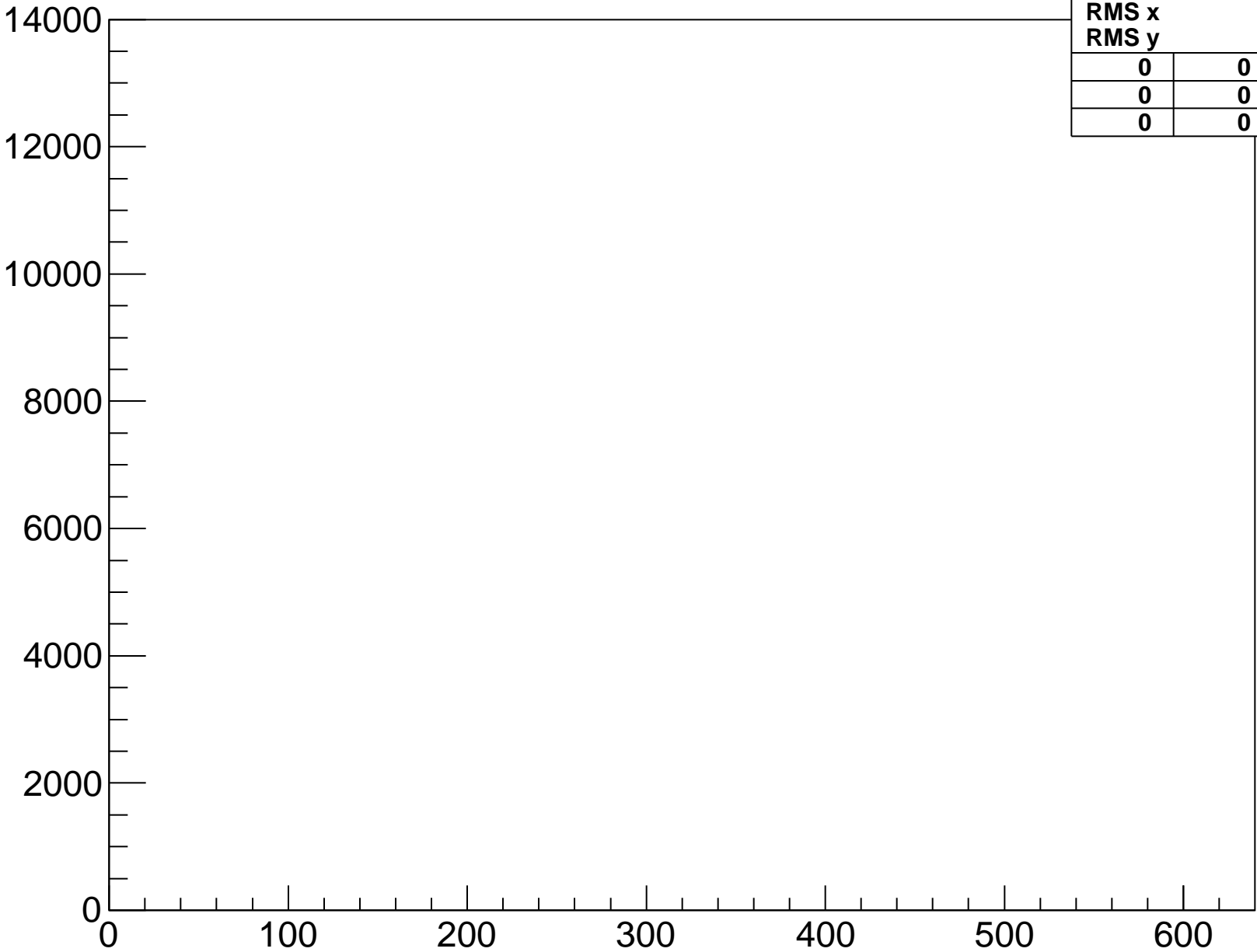


baselinesamples-fpga-4-hyb-3-sample-4



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

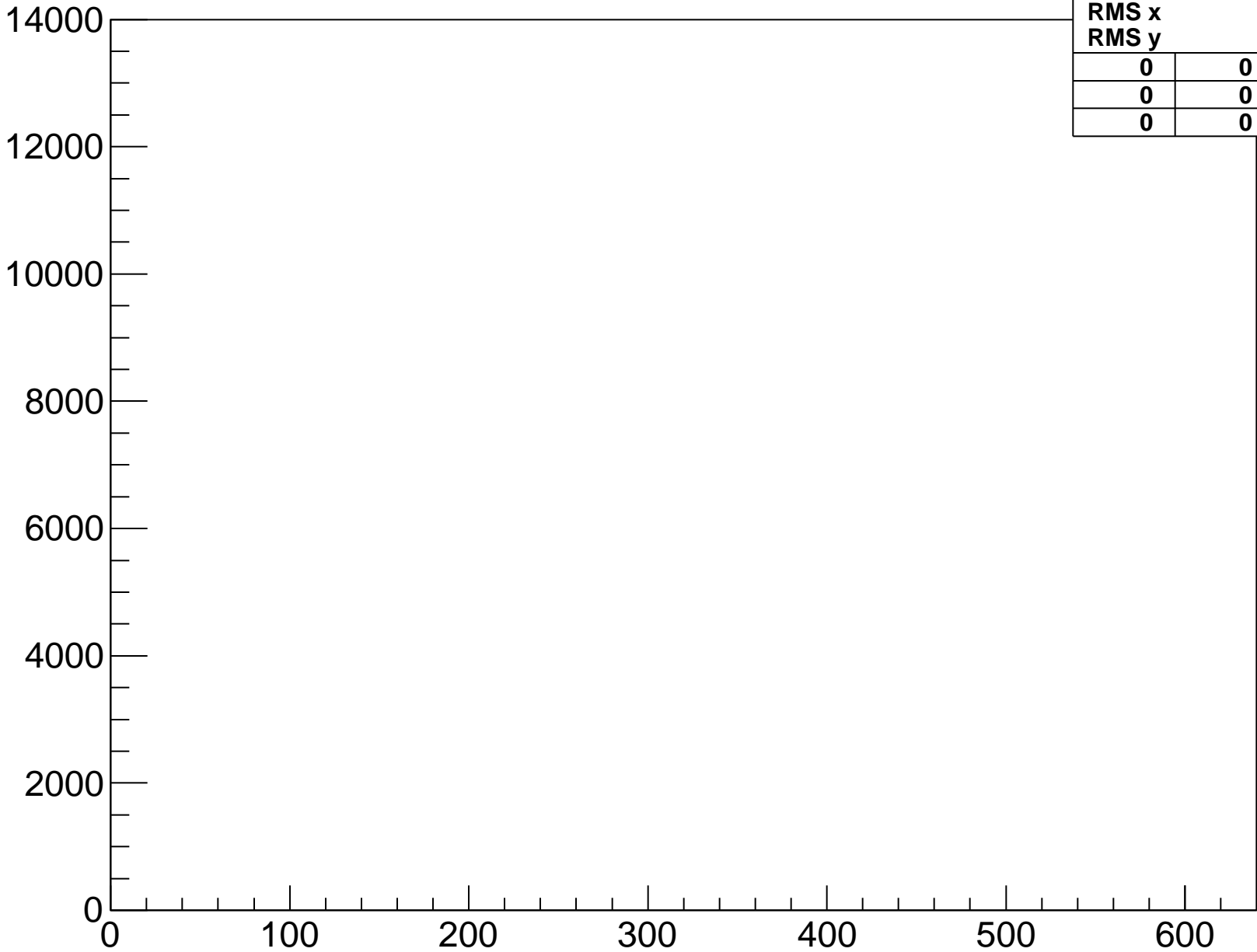
baselinesamples-fpga-4-hyb-3-sample-5



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

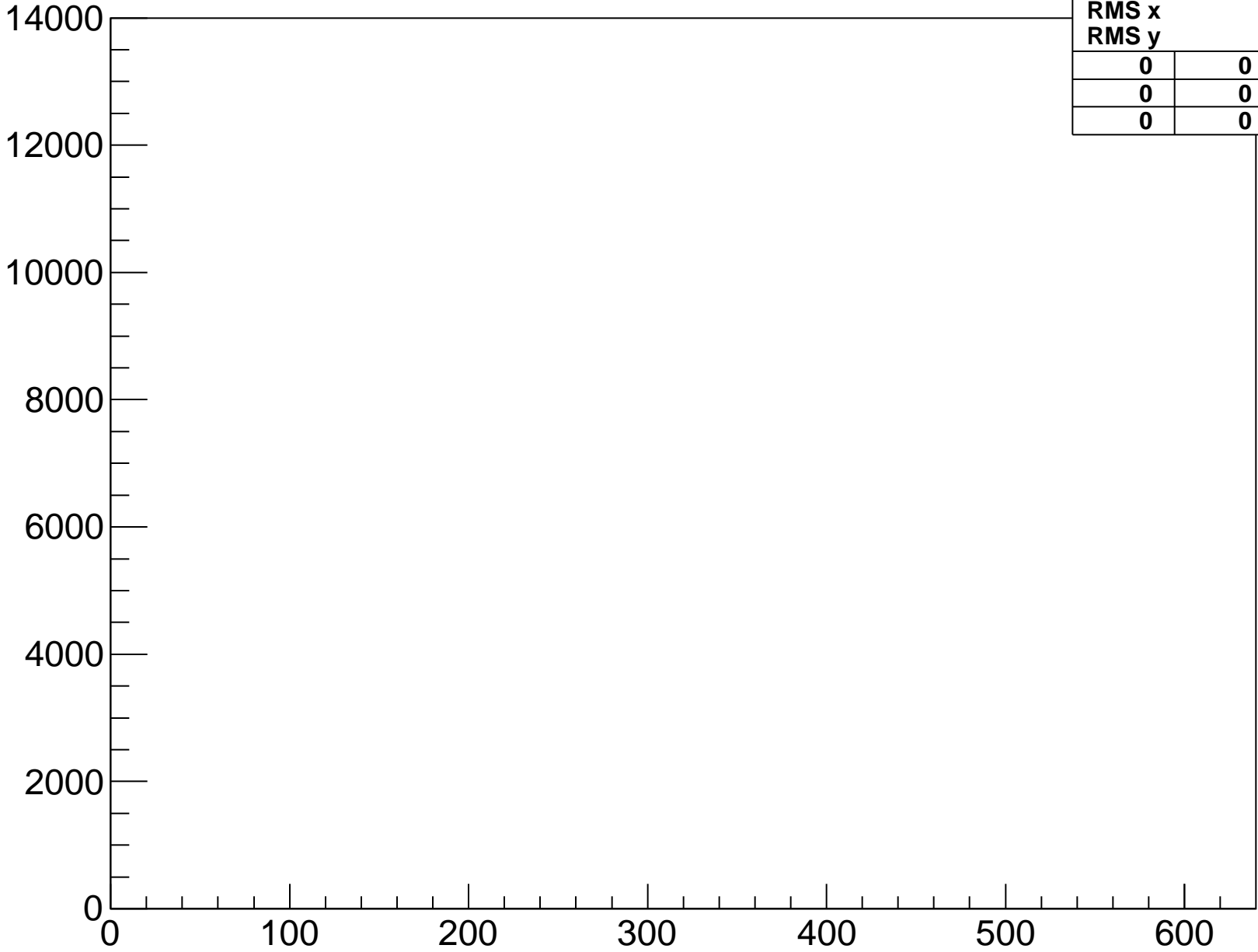
baselinesamples-fpga-5-hyb-0-sample-0

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



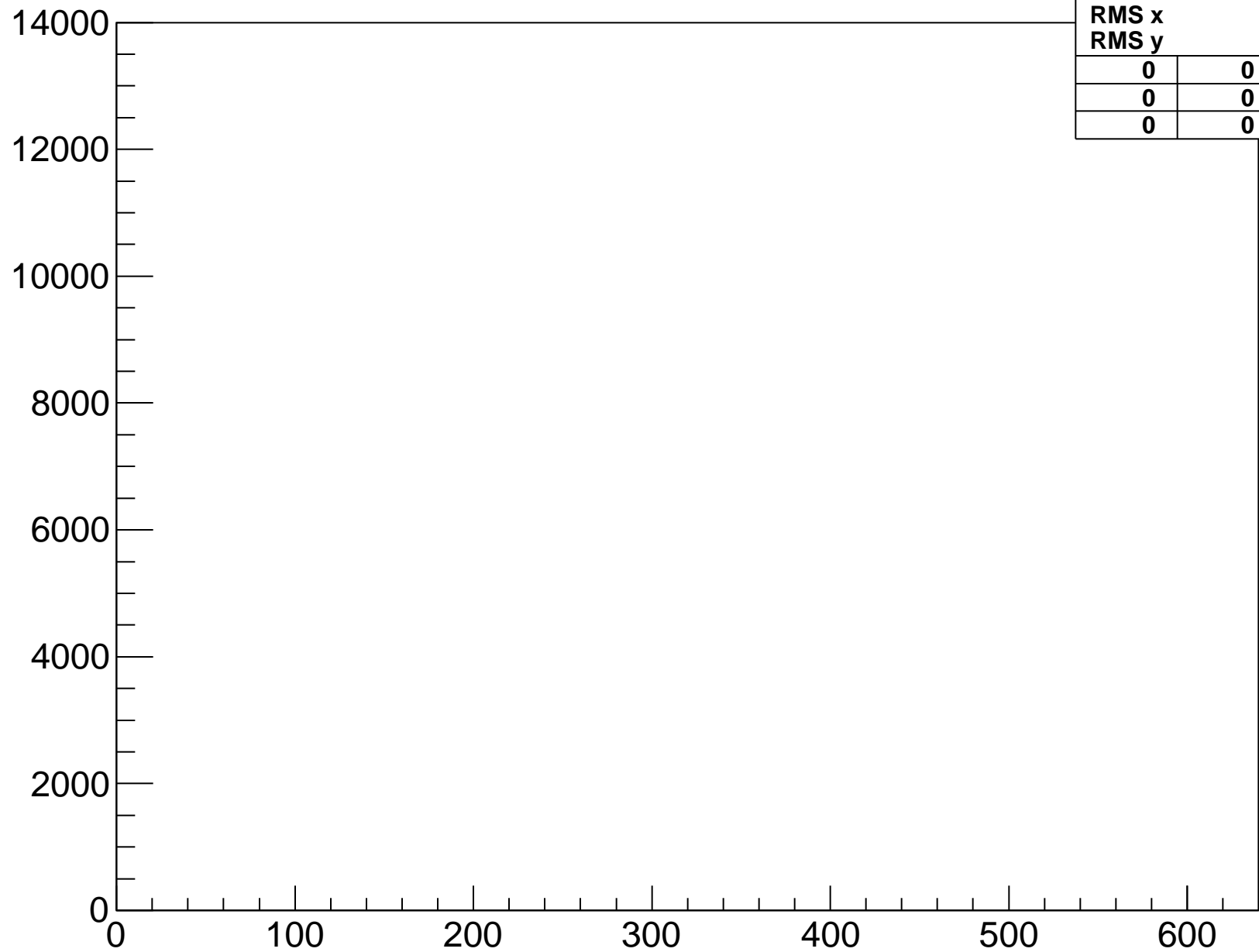
baselinesamples-fpga-5-hyb-0-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

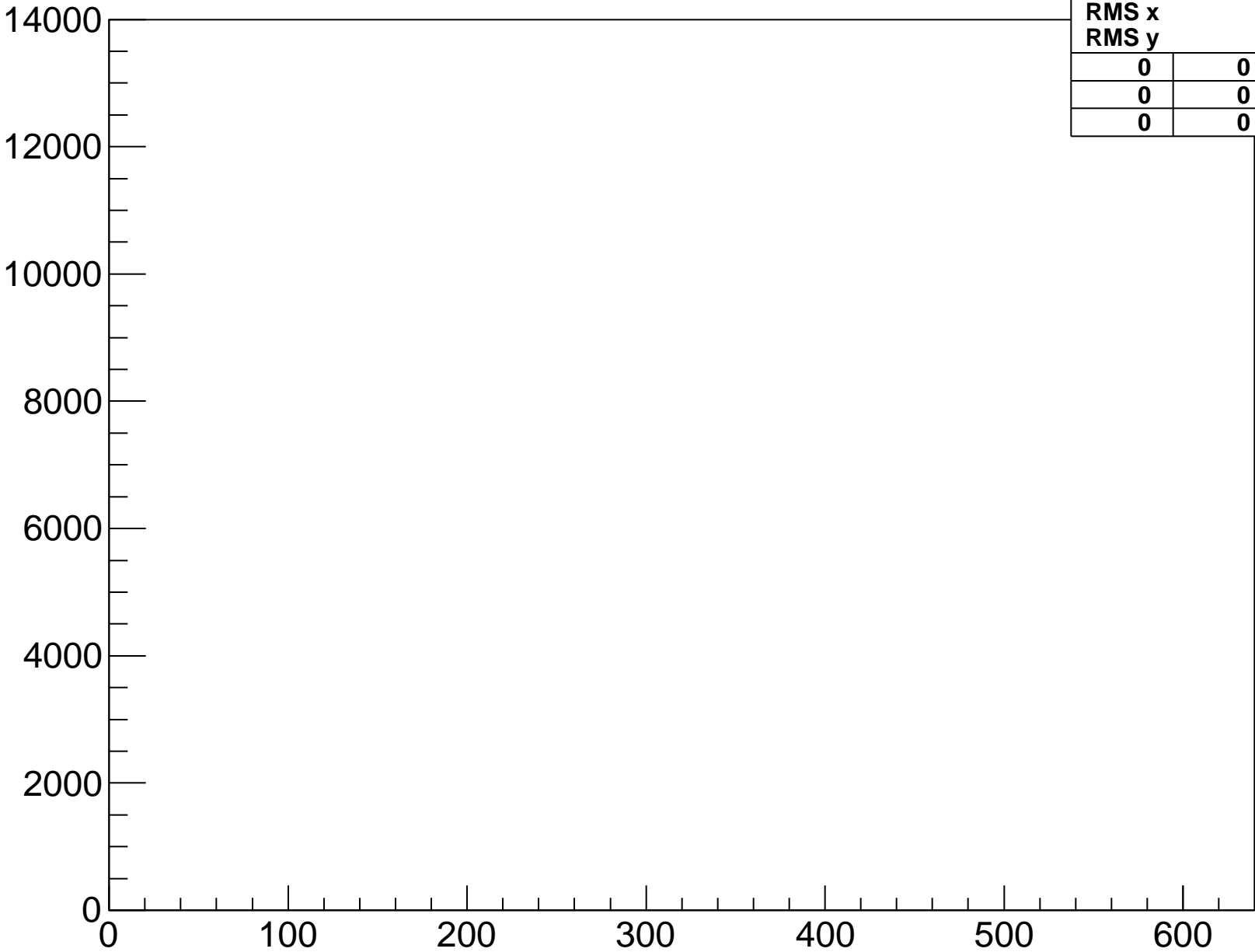


baselinesamples-fpga-5-hyb-0-sample-2

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



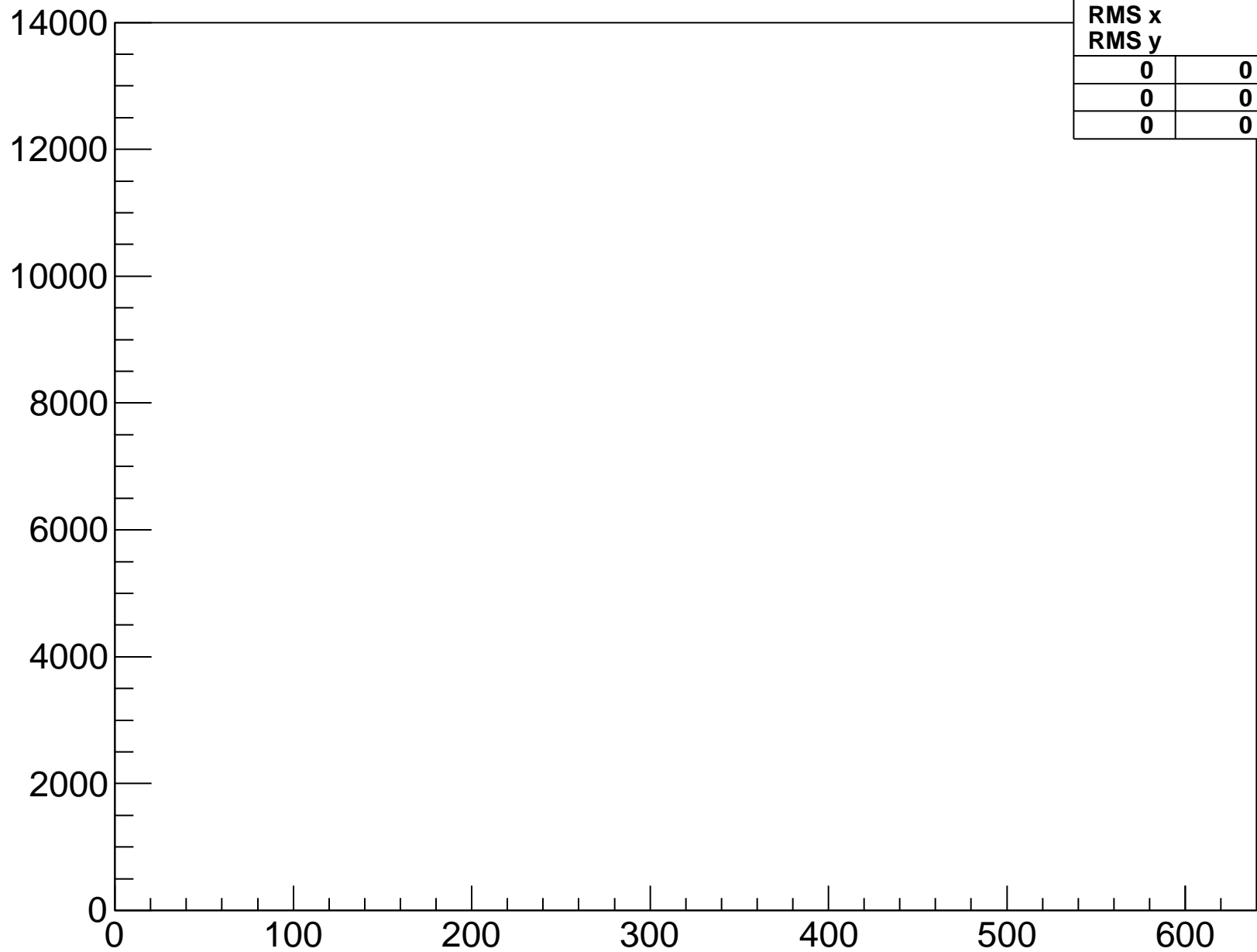
baselinesamples-fpga-5-hyb-0-sample-3



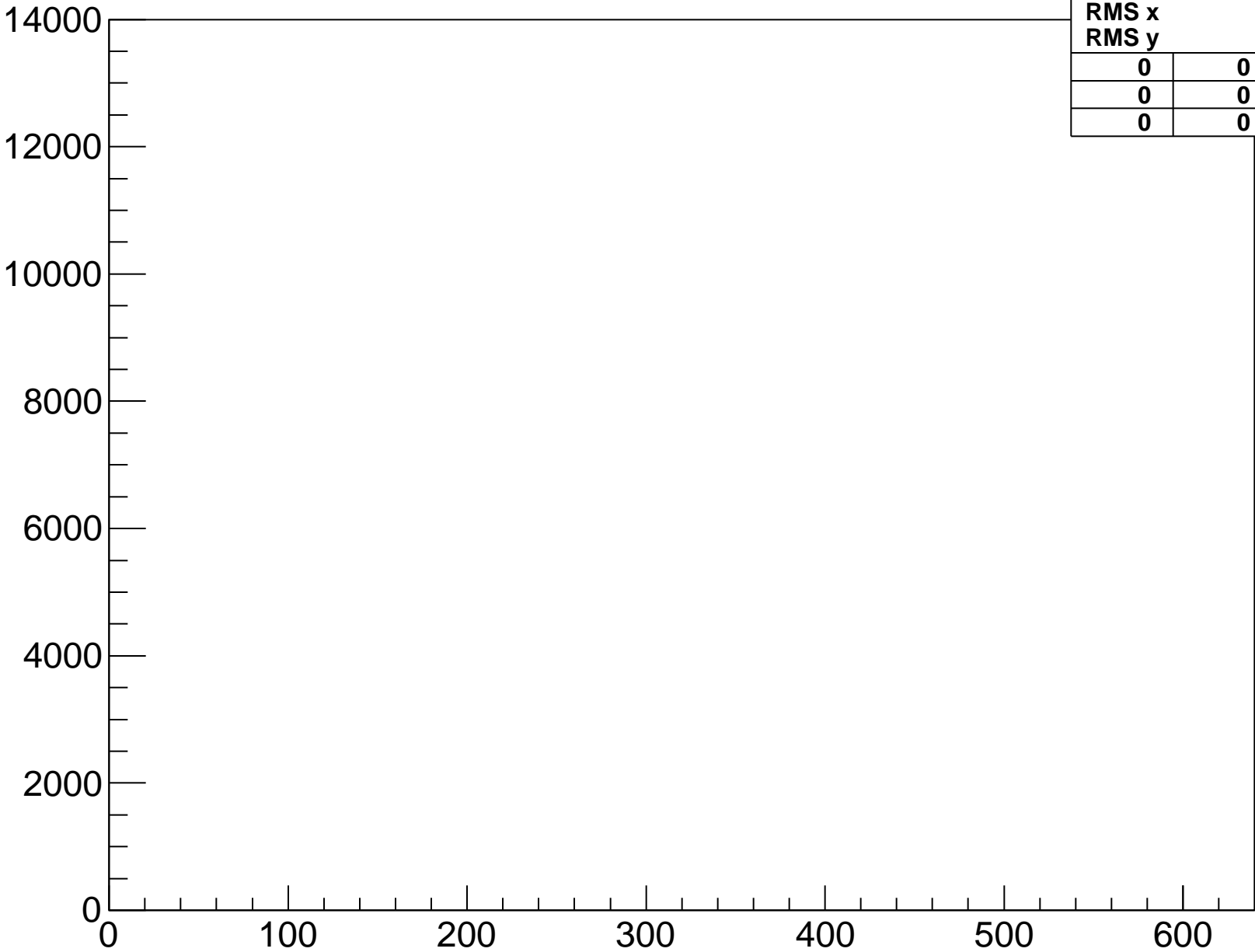
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-5-hyb-0-sample-4

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

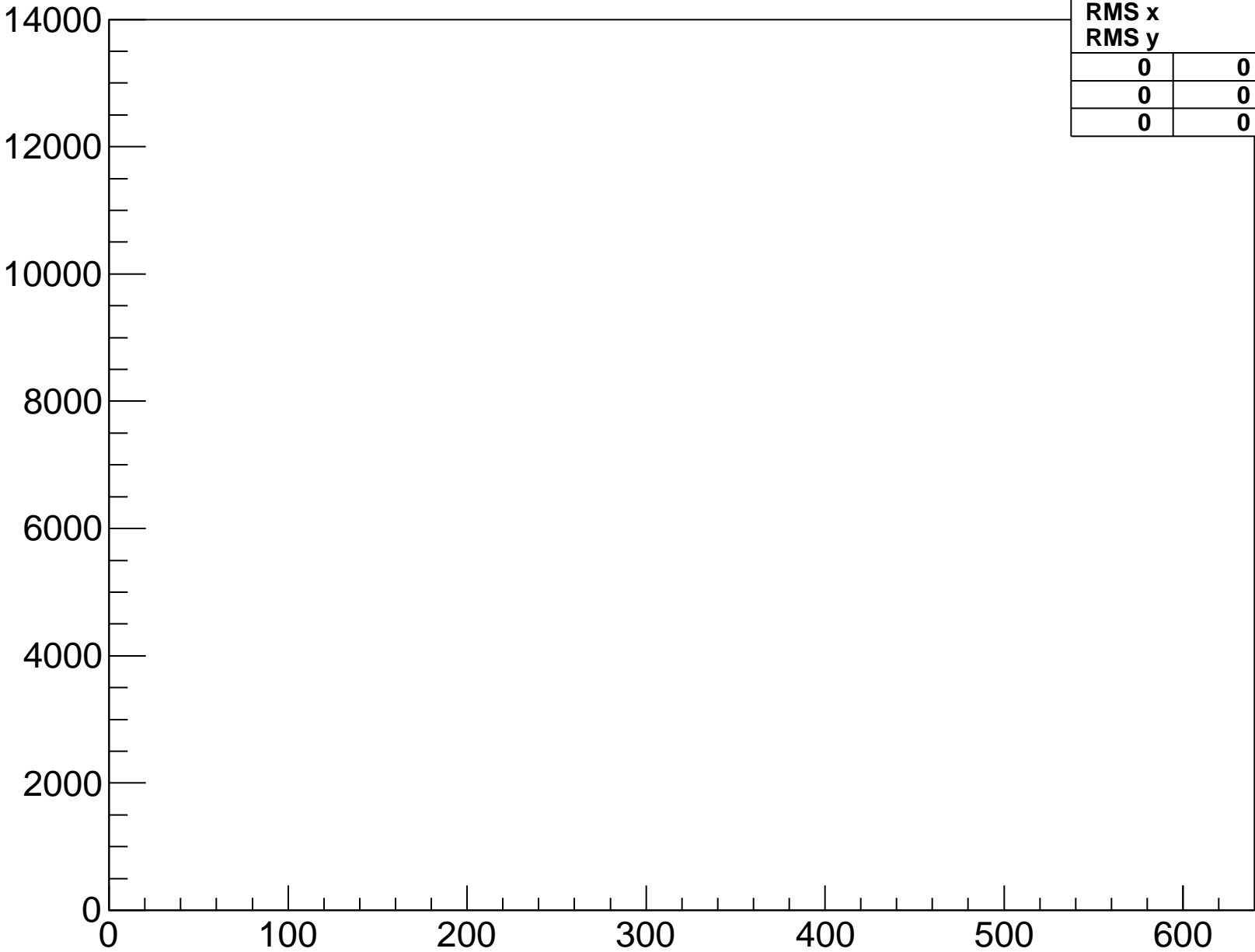


baselinesamples-fpga-5-hyb-0-sample-5



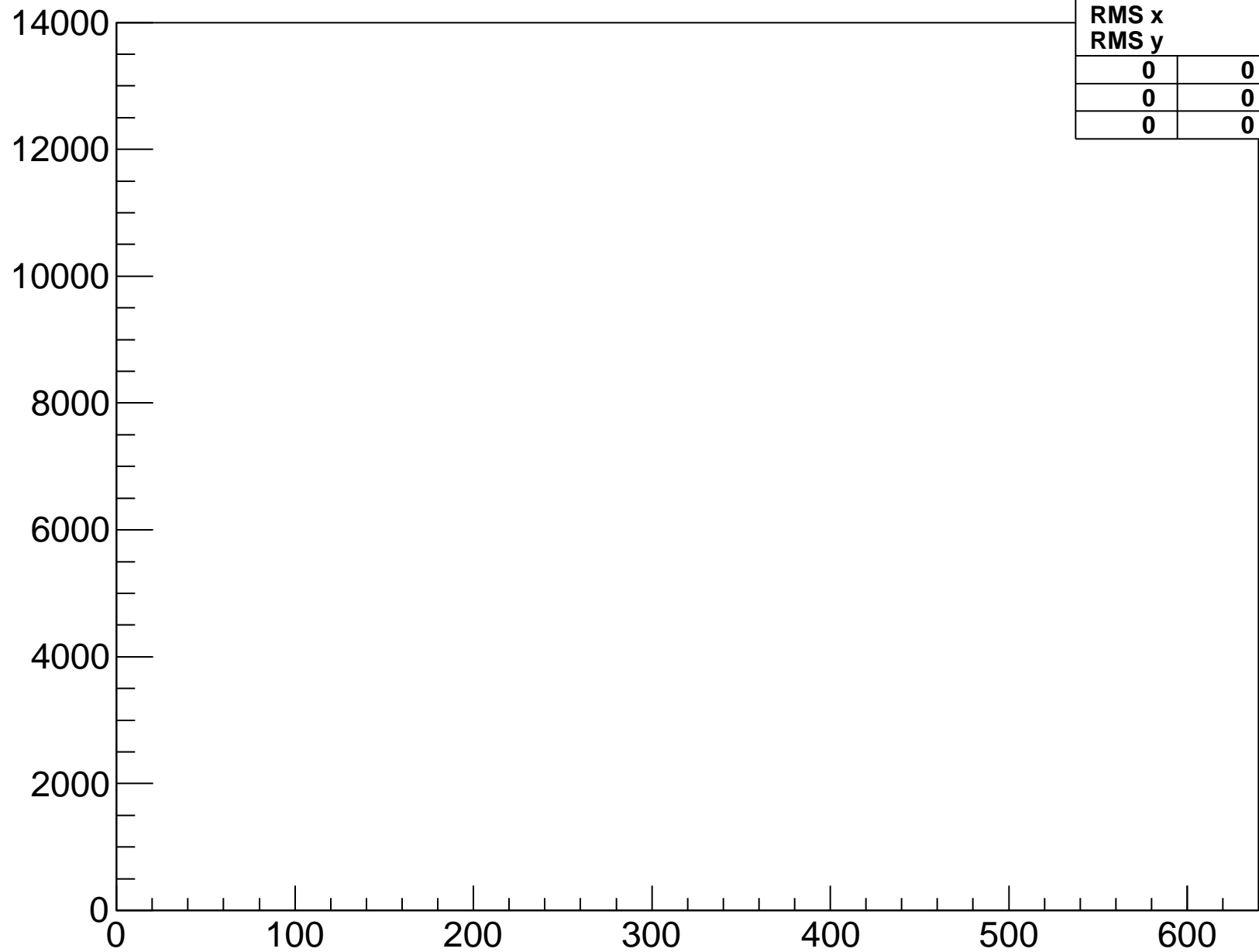
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-5-hyb-1-sample-0



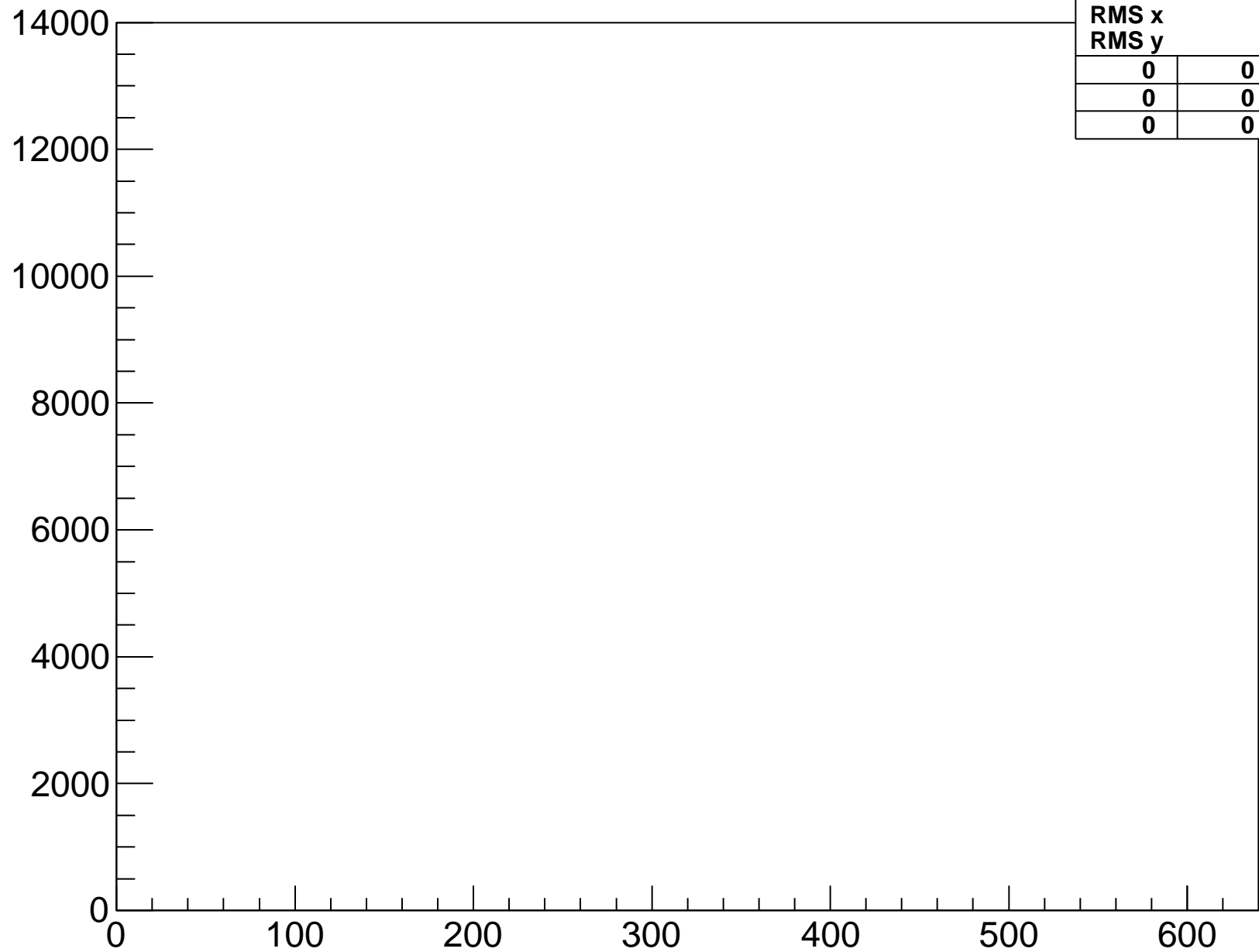
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-5-hyb-1-sample-1



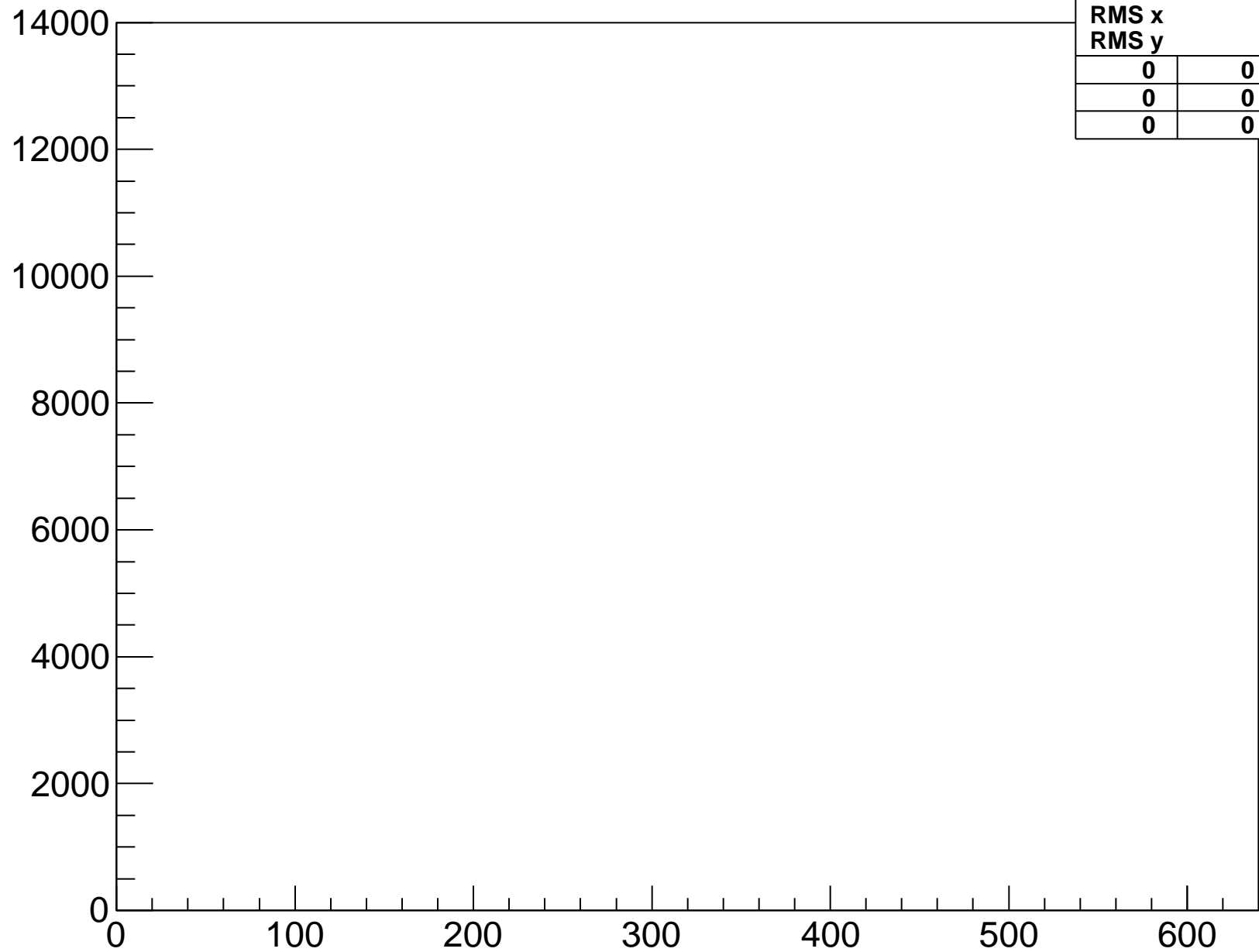
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-5-hyb-1-sample-2



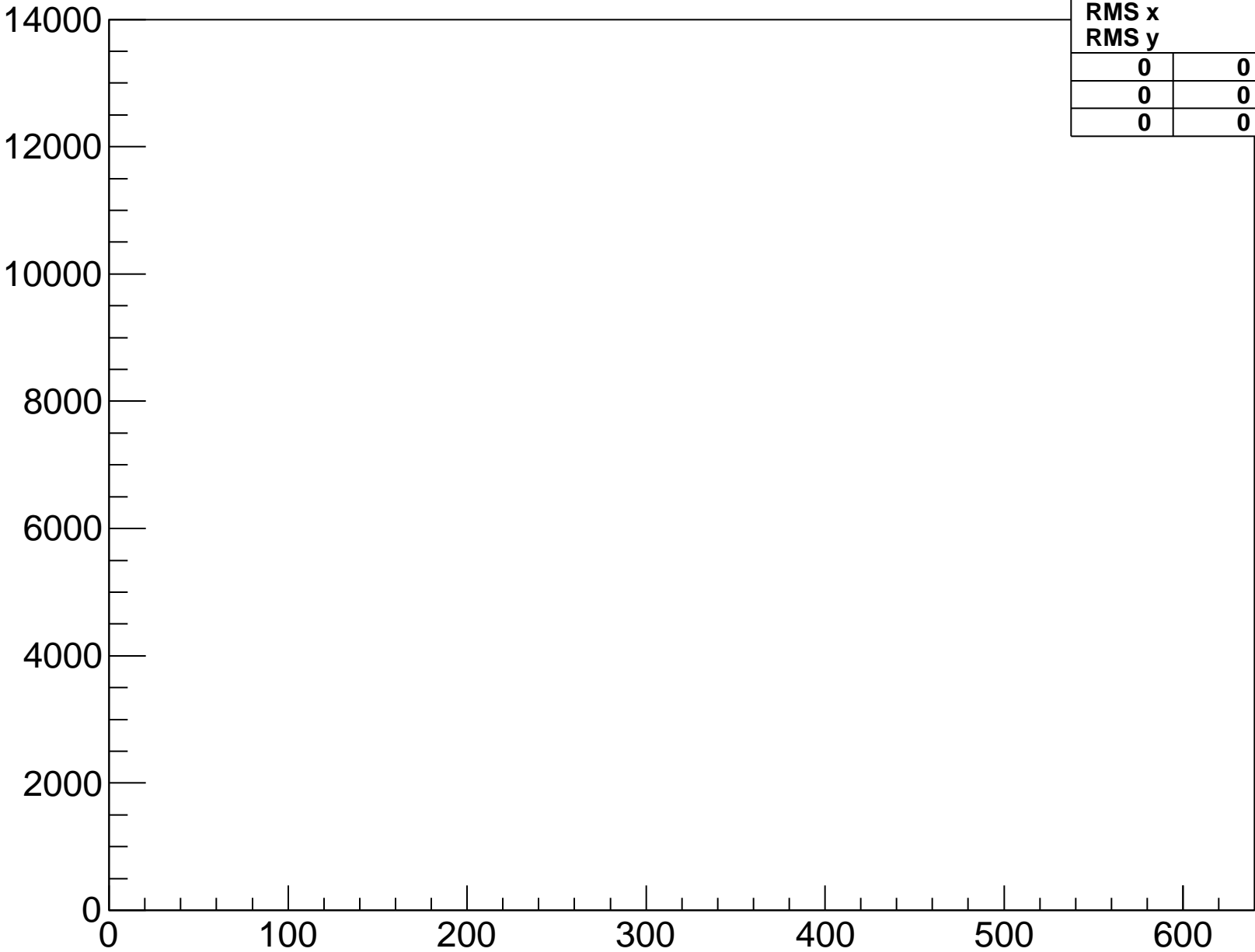
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-5-hyb-1-sample-3



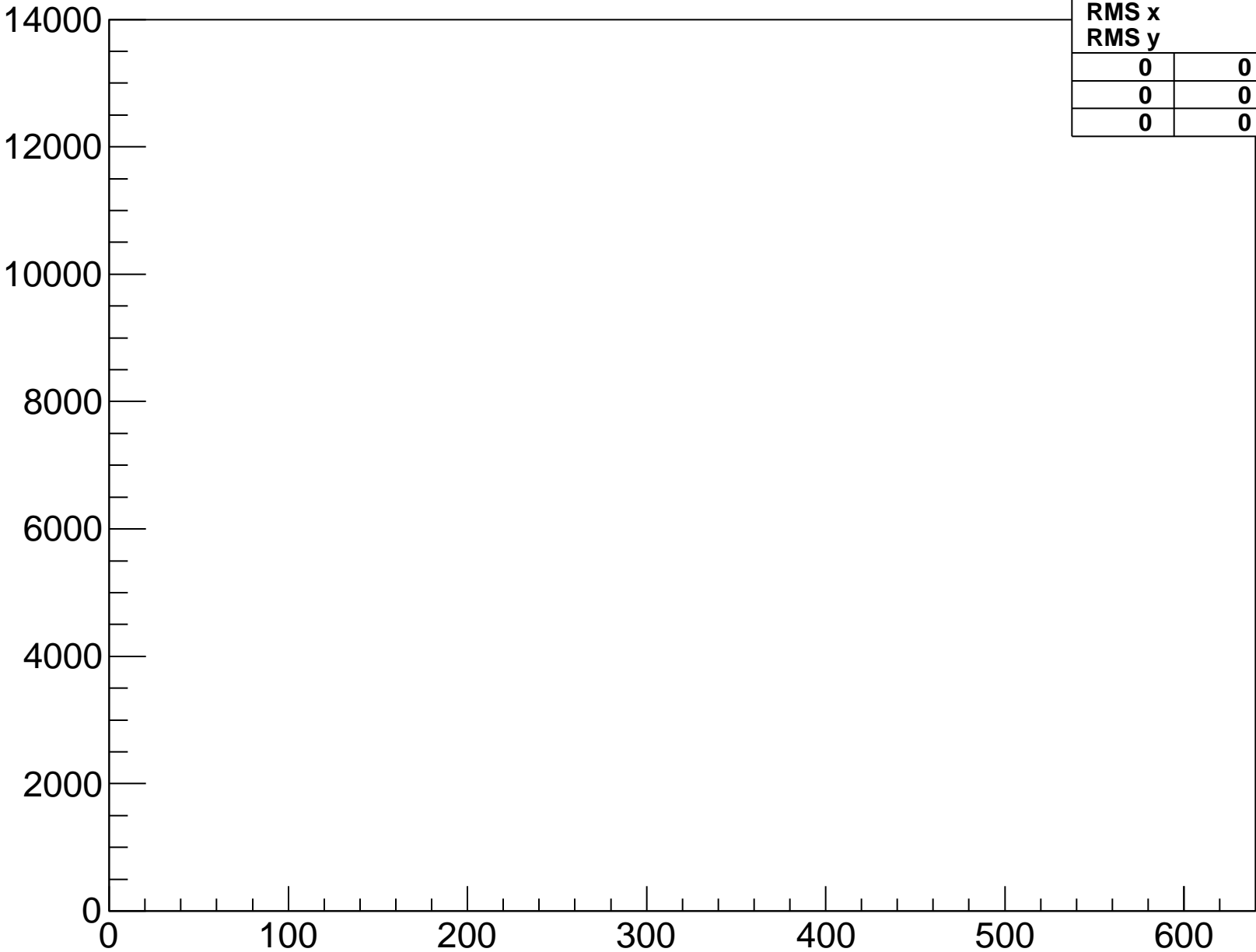
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-5-hyb-1-sample-4



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

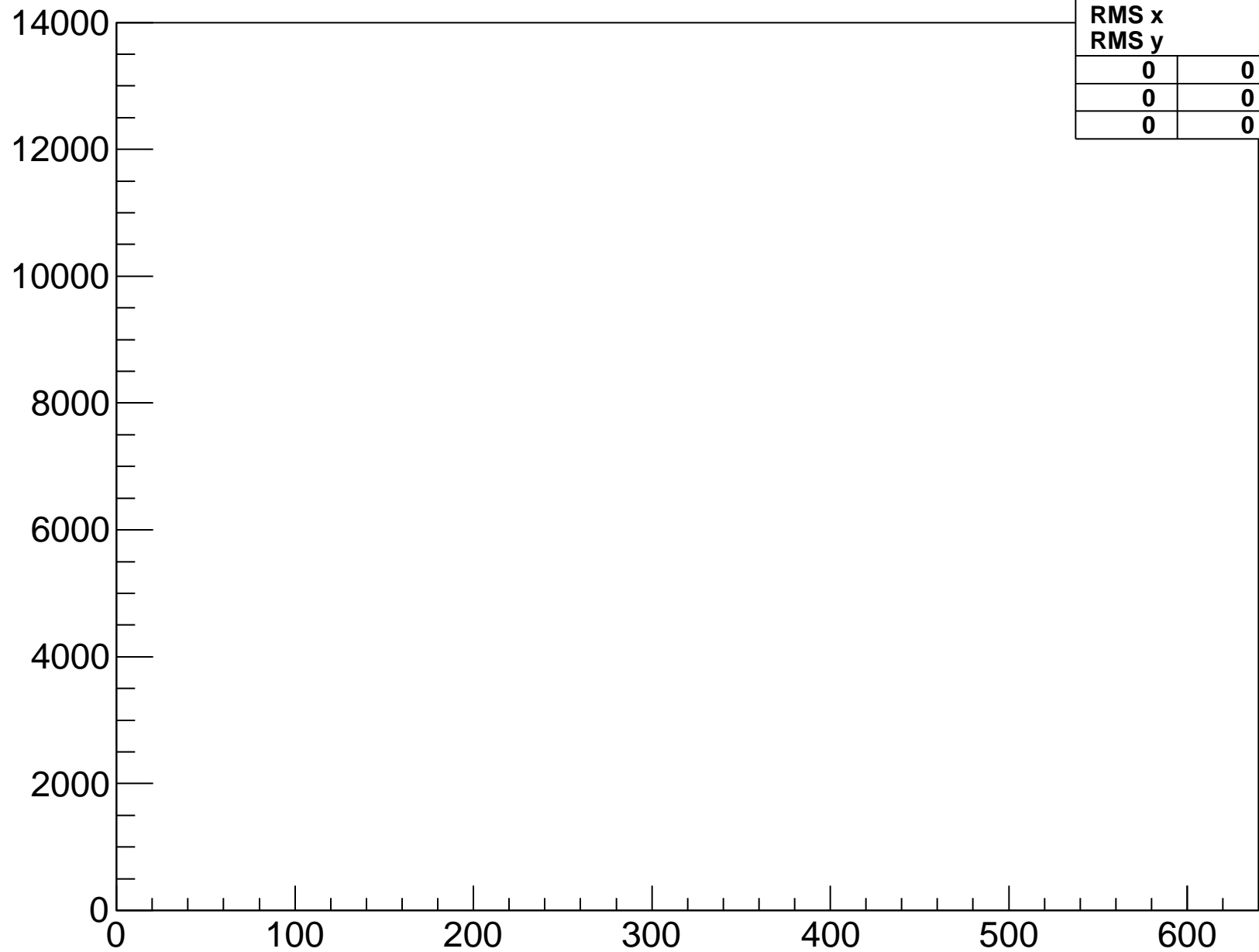
baselinesamples-fpga-5-hyb-1-sample-5



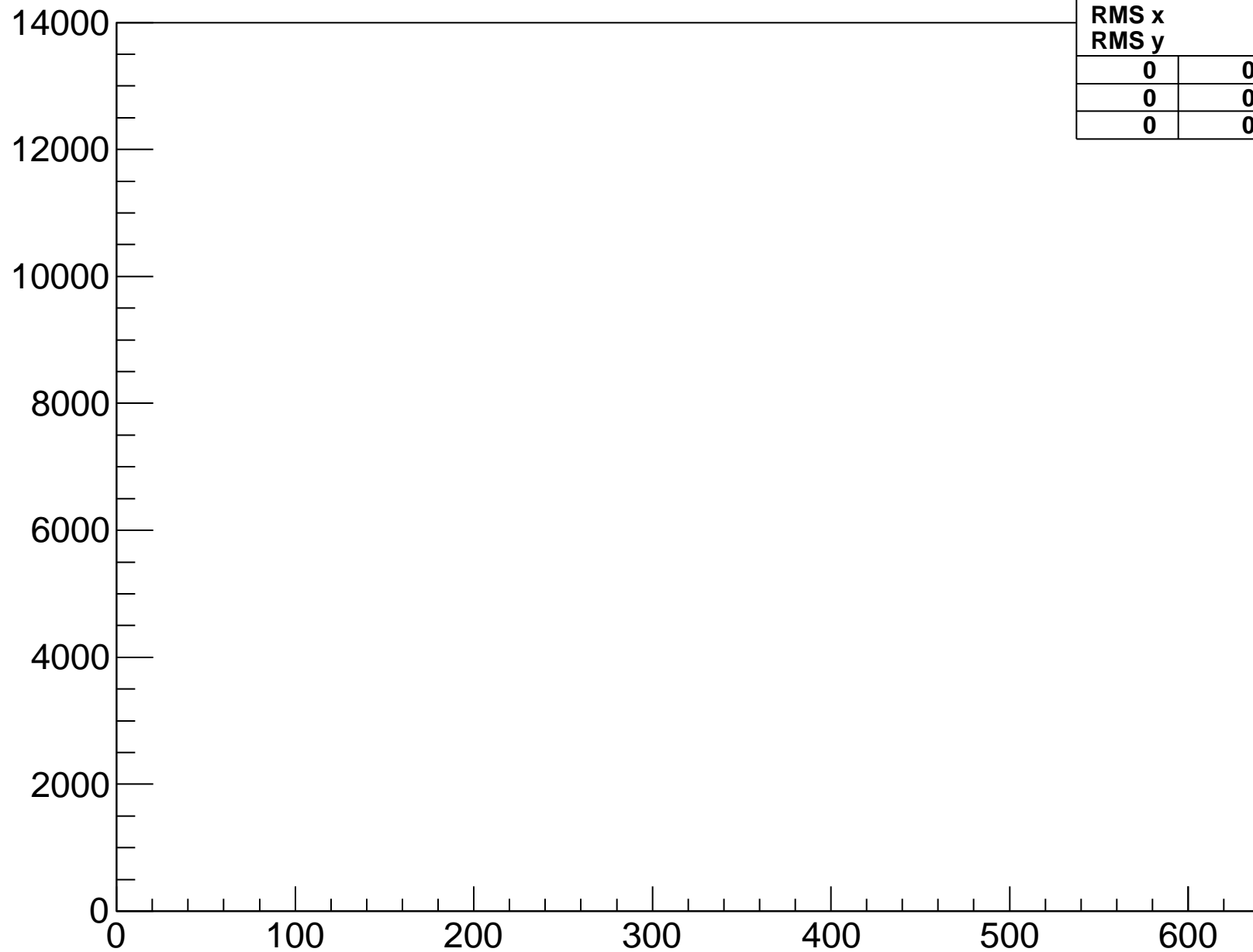
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-5-hyb-2-sample-0

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

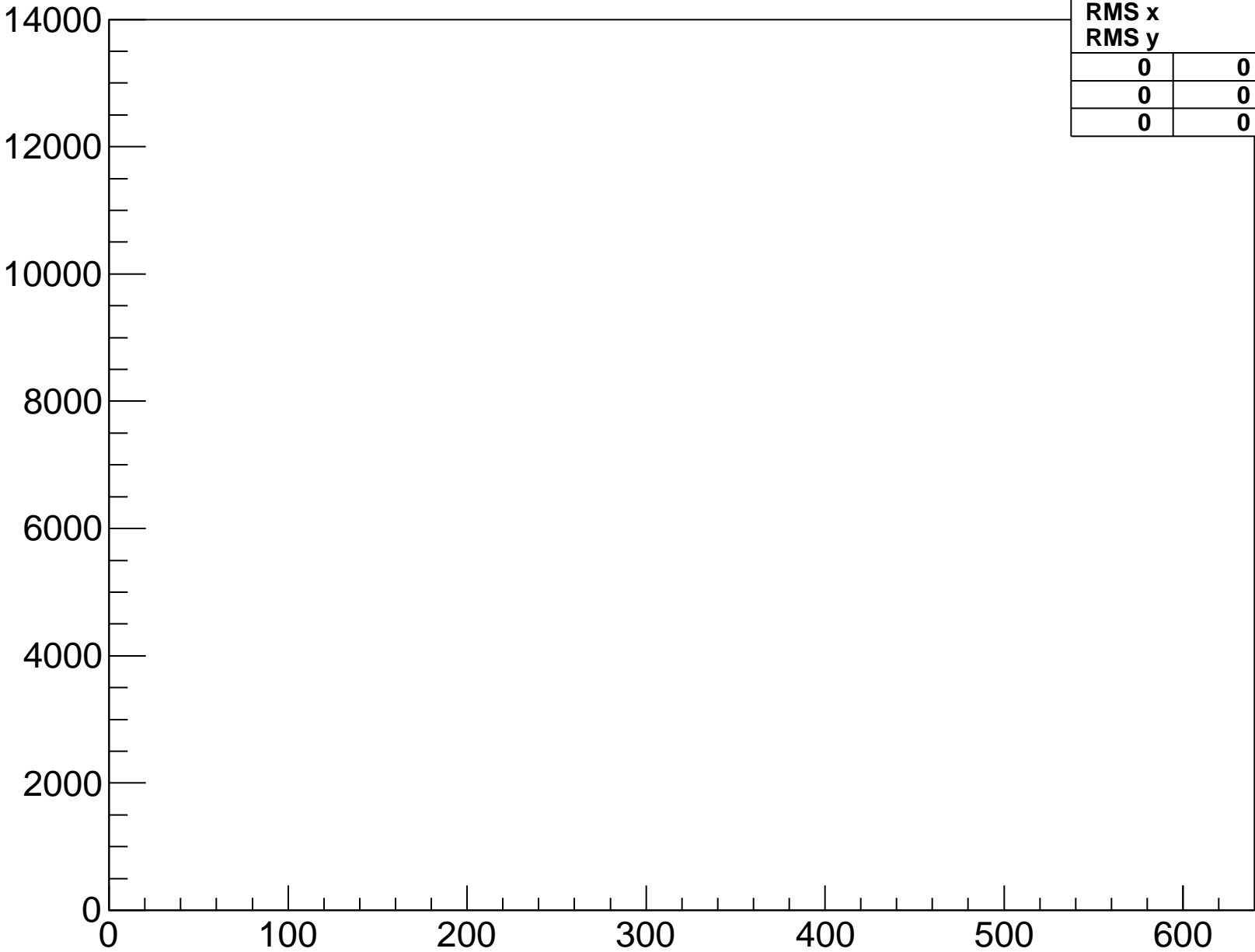


baselinesamples-fpga-5-hyb-2-sample-1



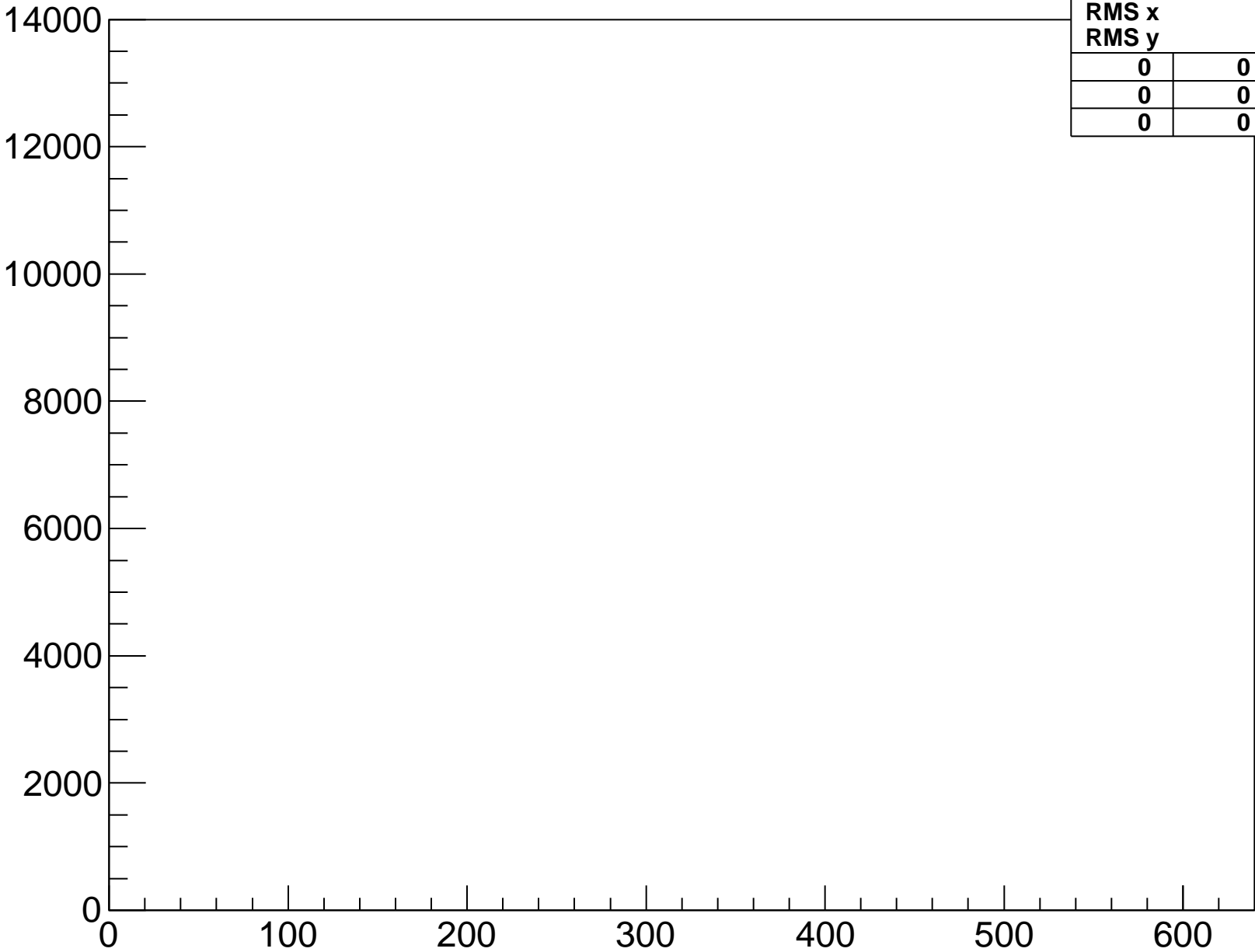
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-5-hyb-2-sample-2



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

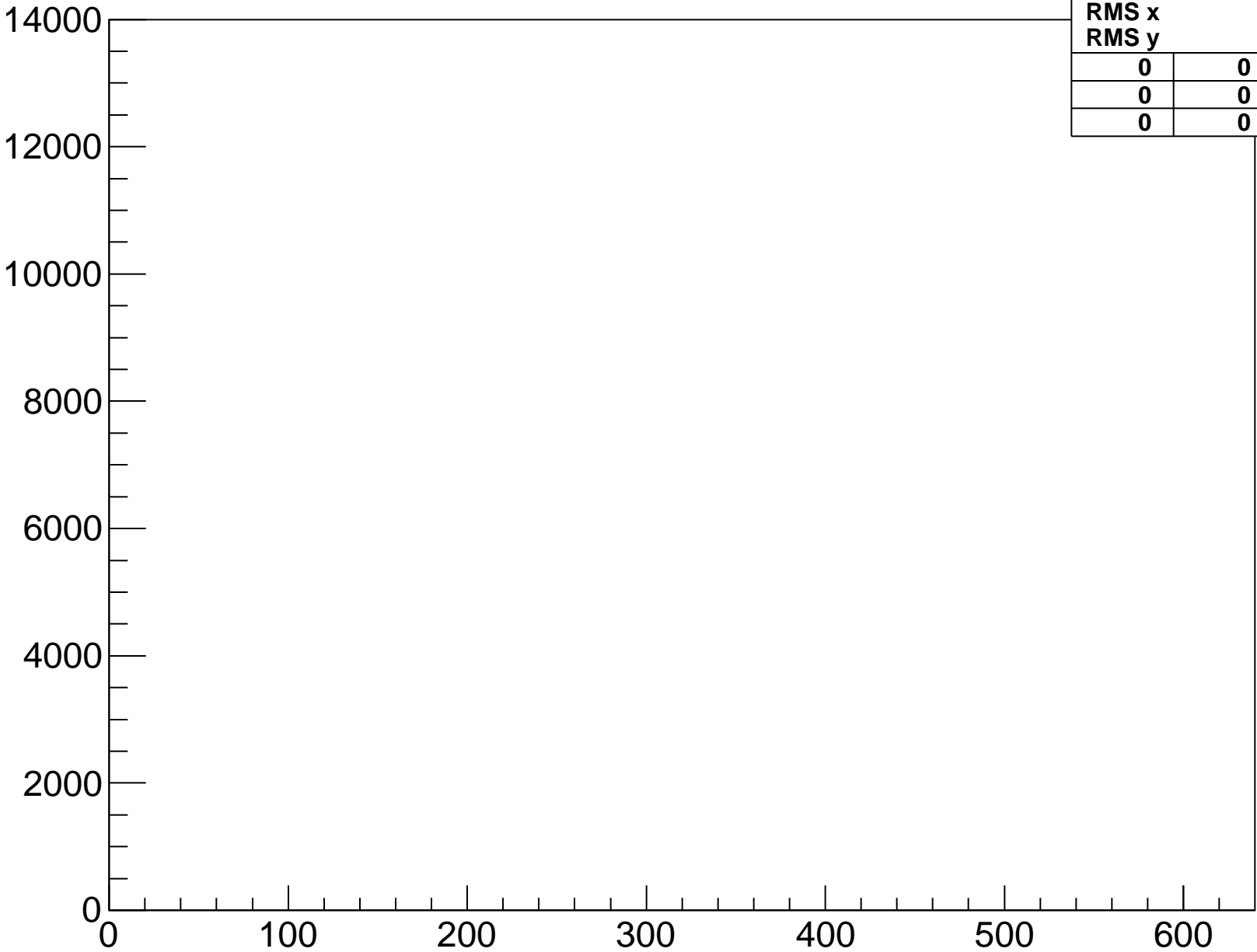
baselinesamples-fpga-5-hyb-2-sample-3



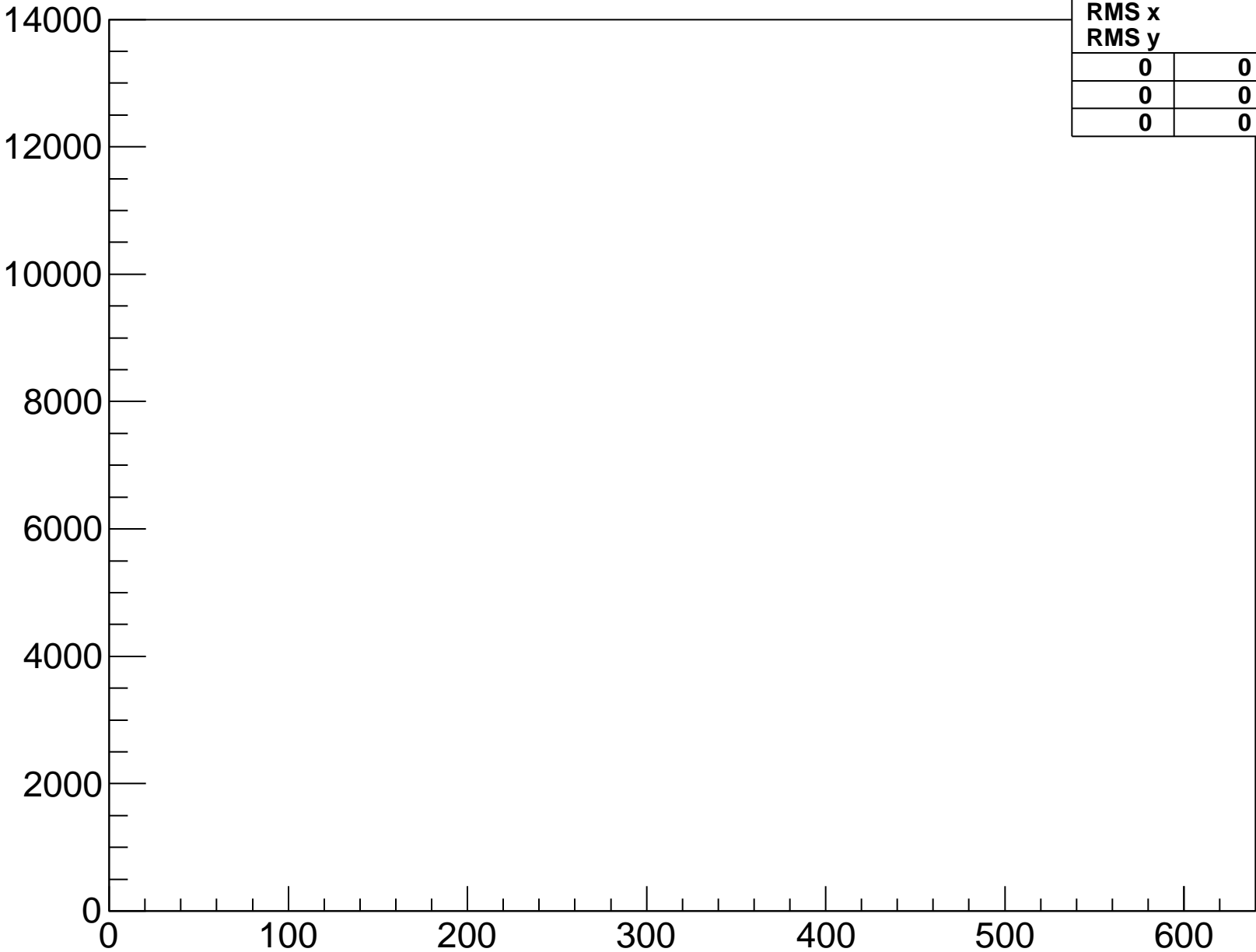
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-5-hyb-2-sample-4

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

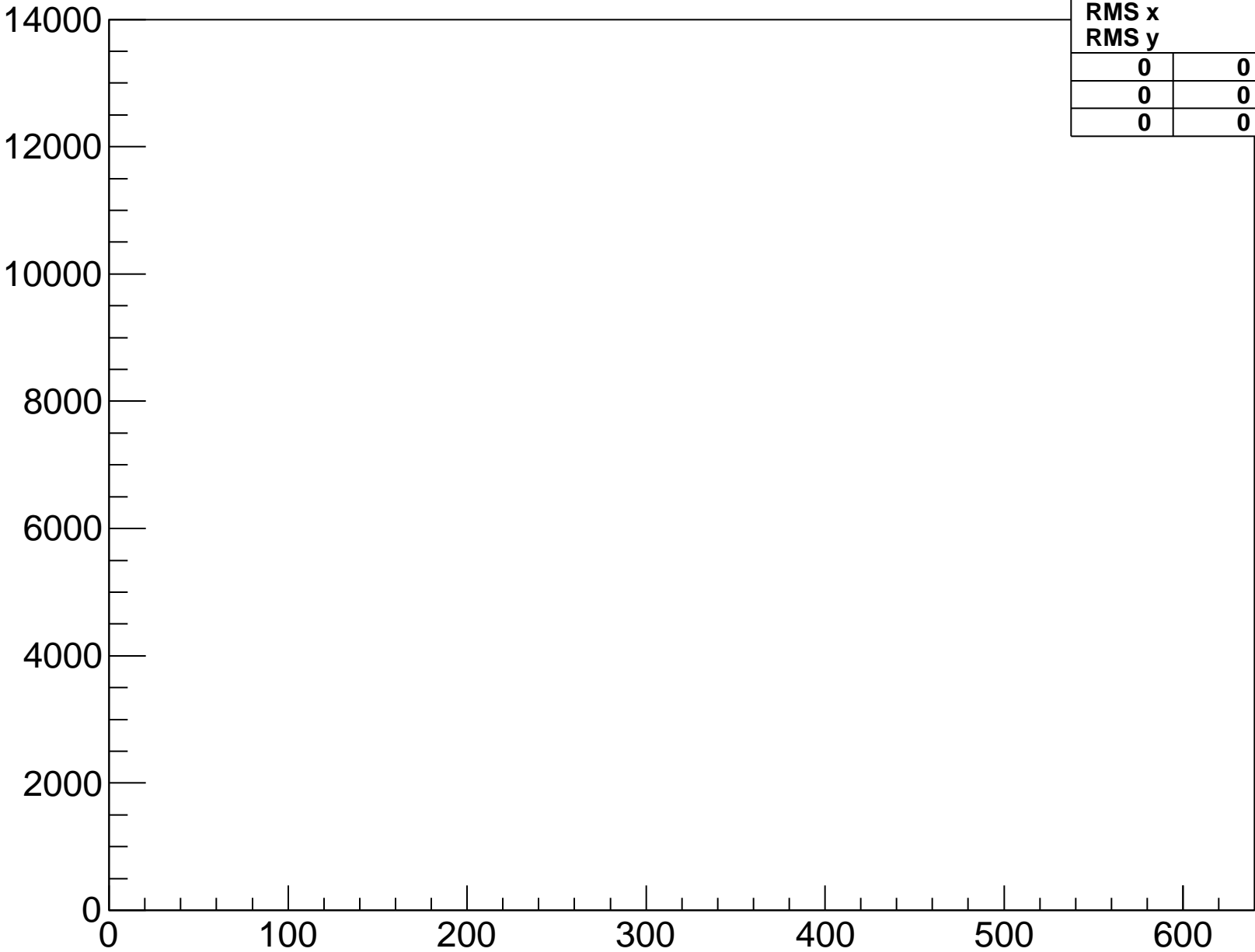


baselinesamples-fpga-5-hyb-2-sample-5



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

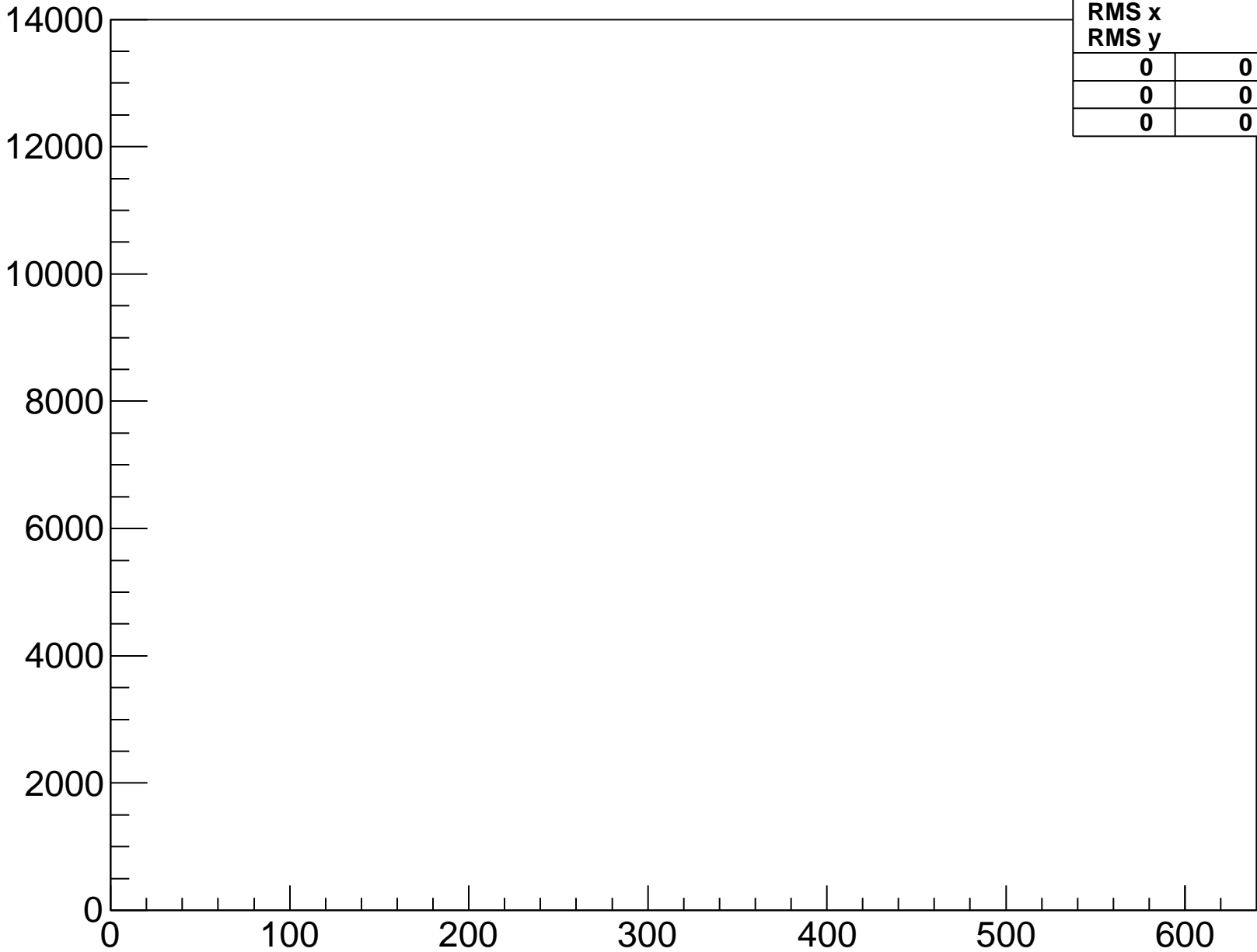
baselinesamples-fpga-5-hyb-3-sample-0



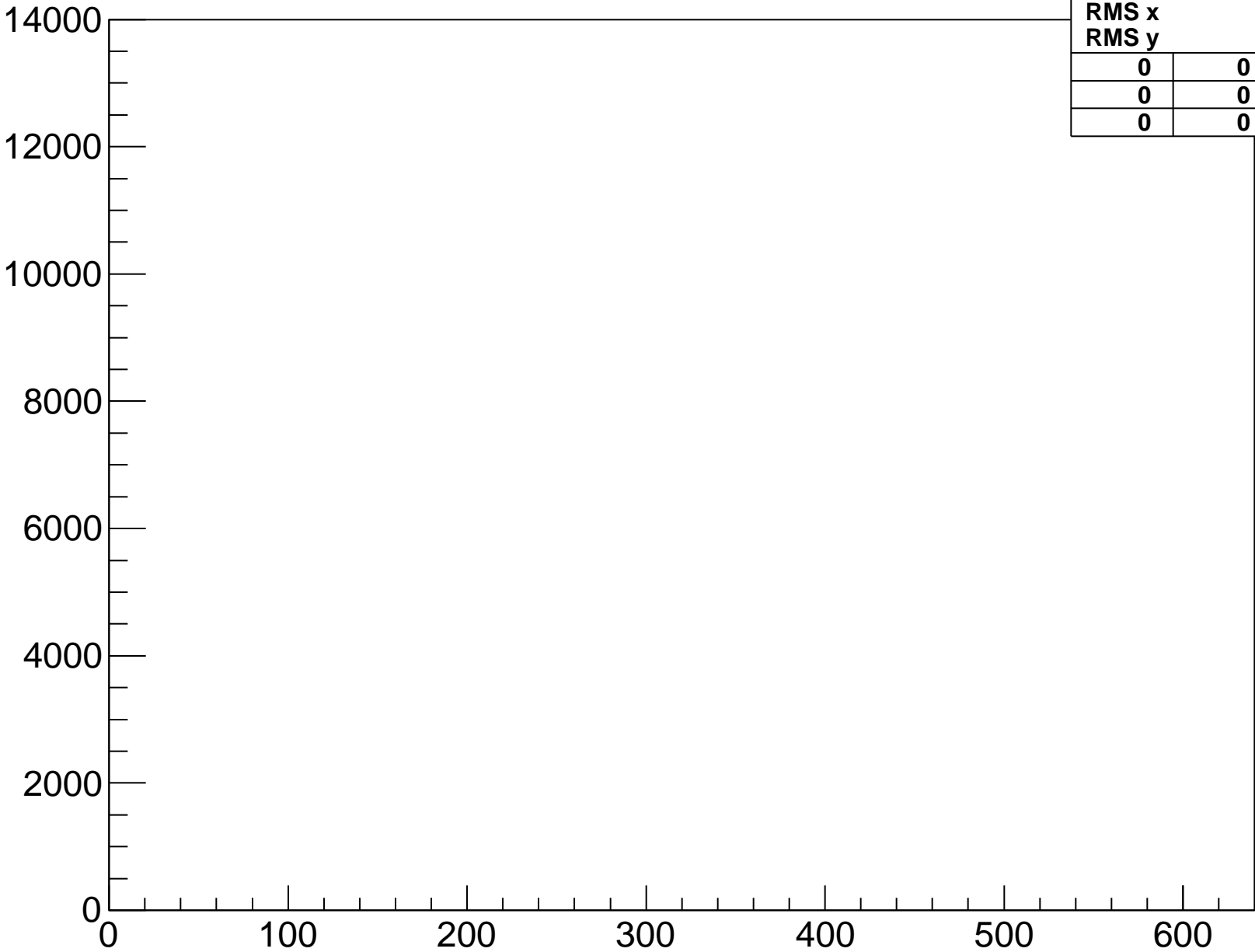
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-5-hyb-3-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

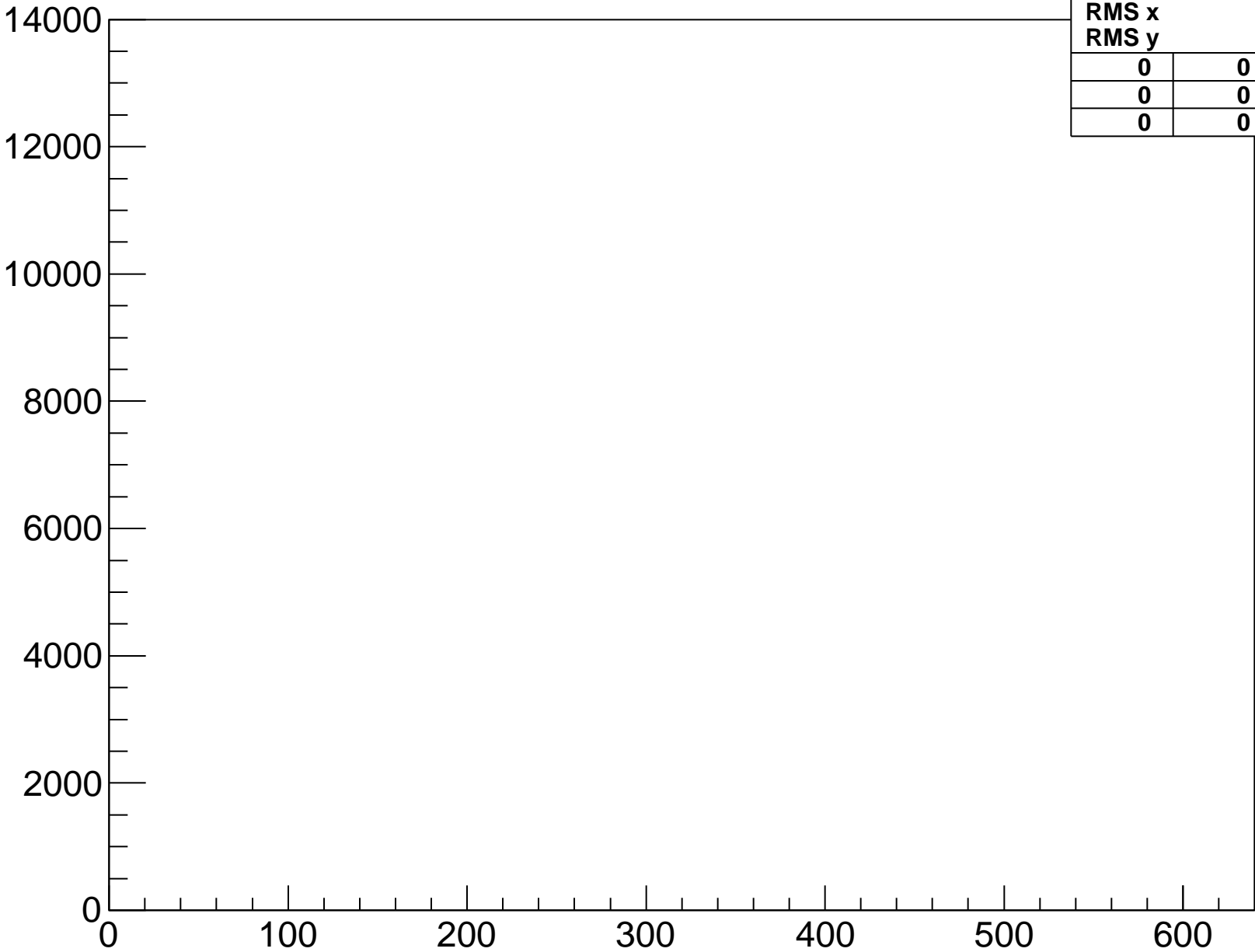


baselinesamples-fpga-5-hyb-3-sample-2



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

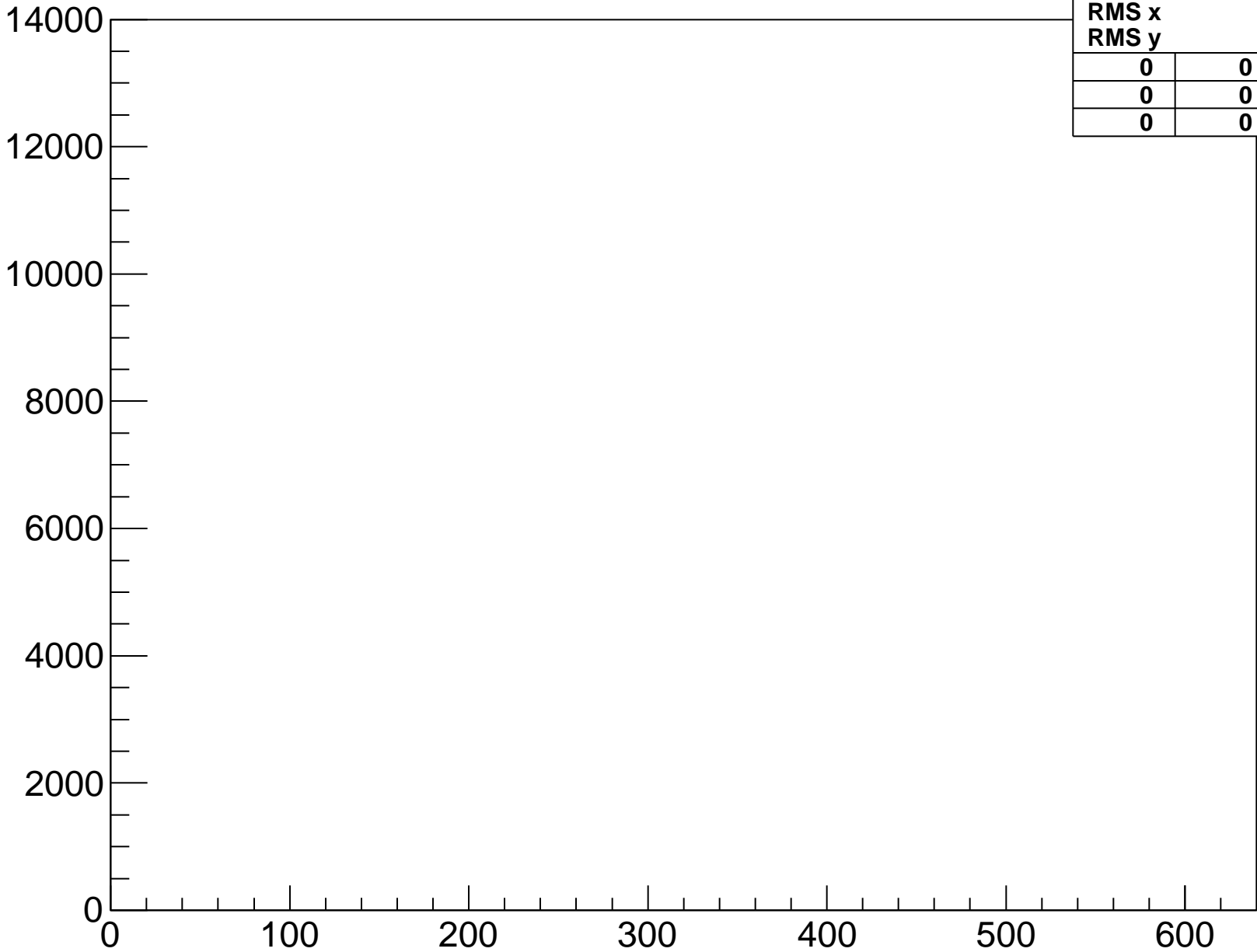
baselinesamples-fpga-5-hyb-3-sample-3



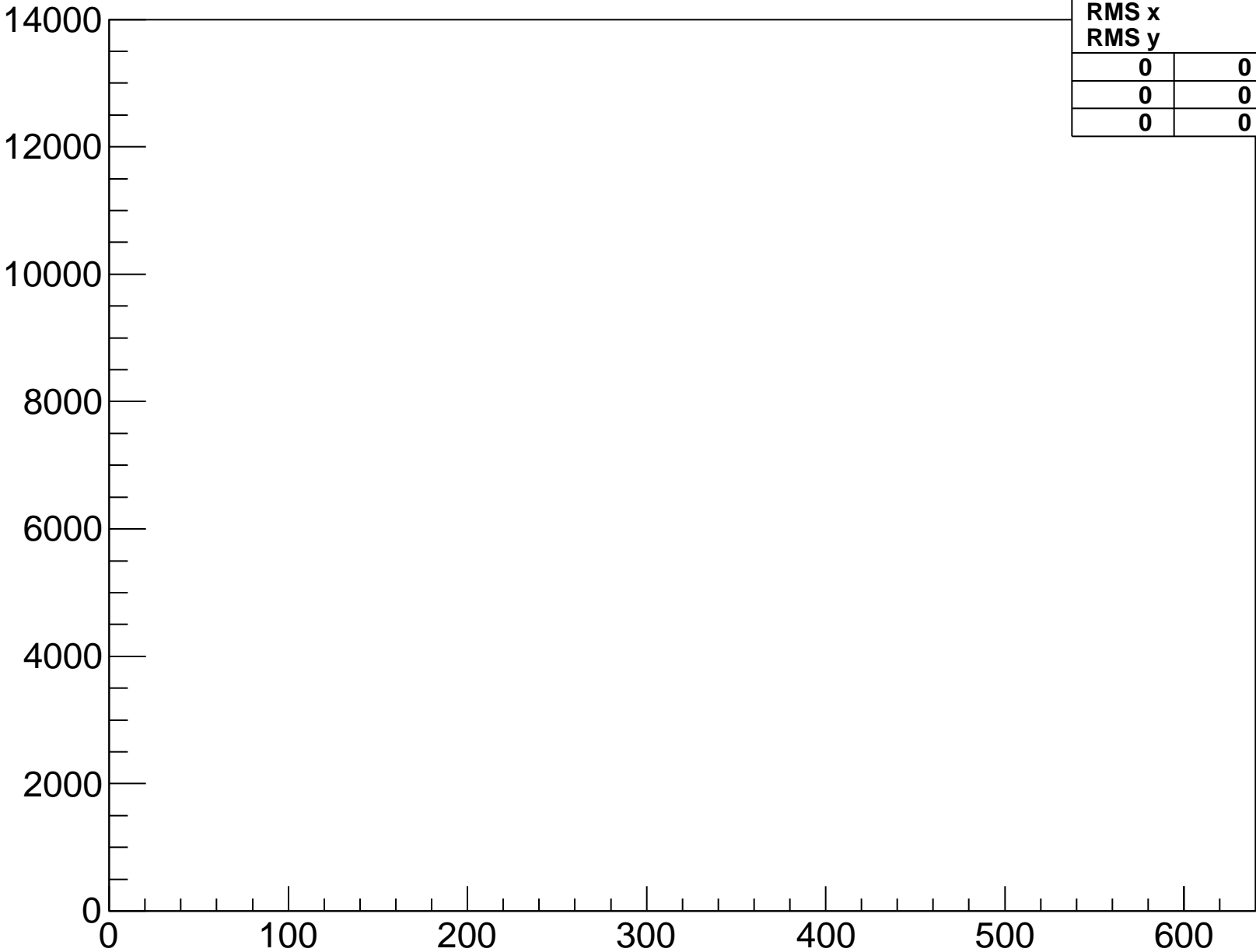
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-5-hyb-3-sample-4

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



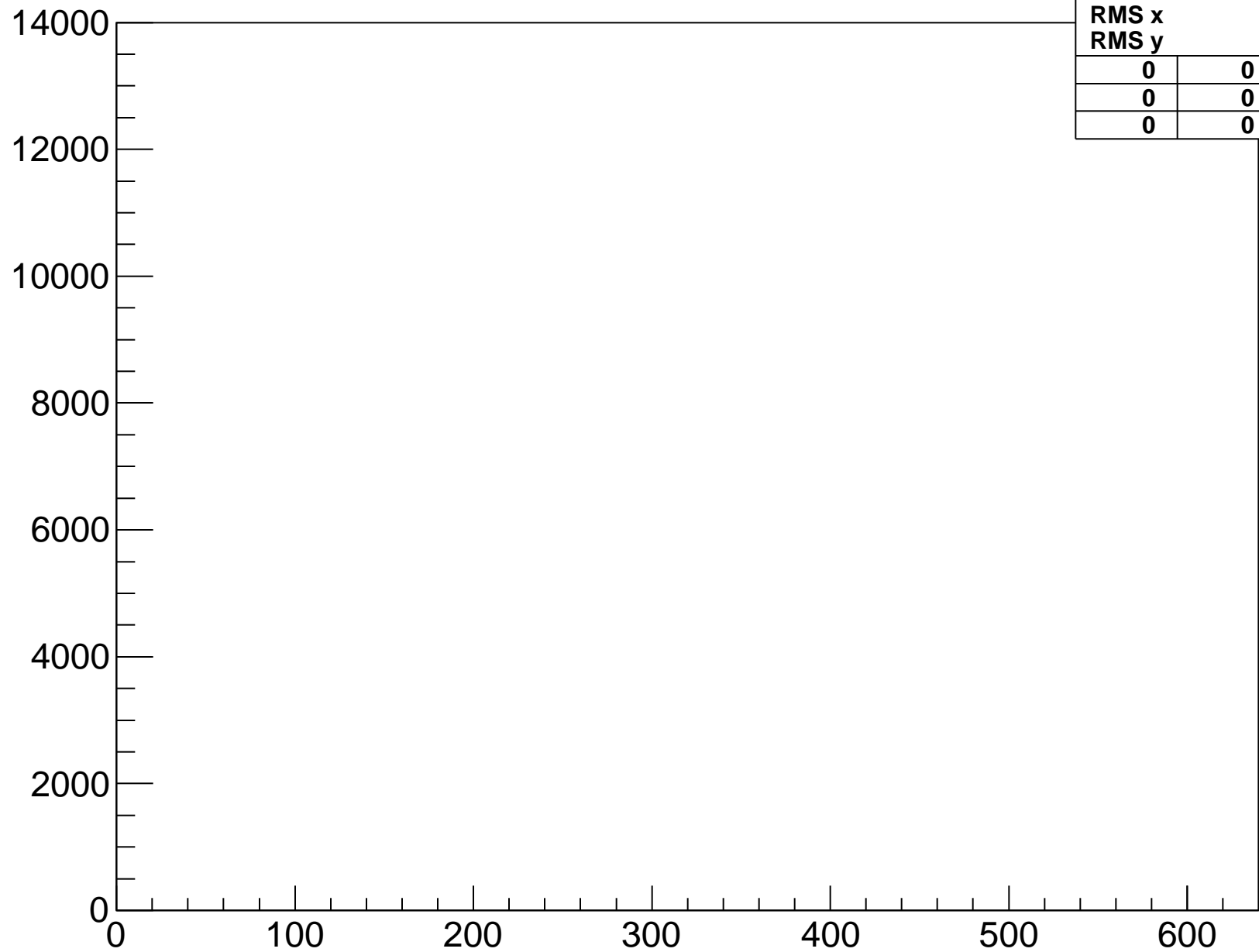
baselinesamples-fpga-5-hyb-3-sample-5



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

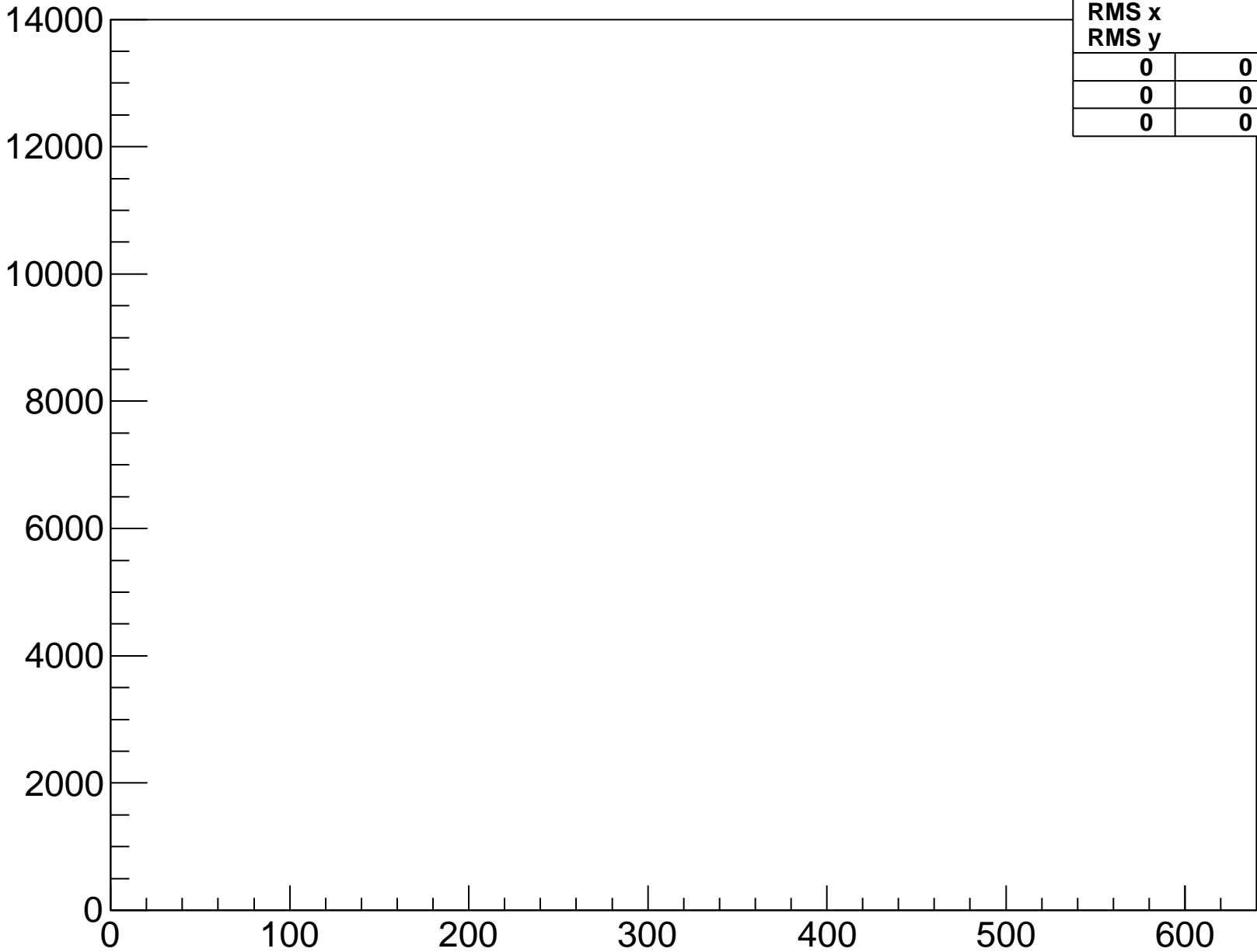
baselinesamples-fpga-6-hyb-0-sample-0

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

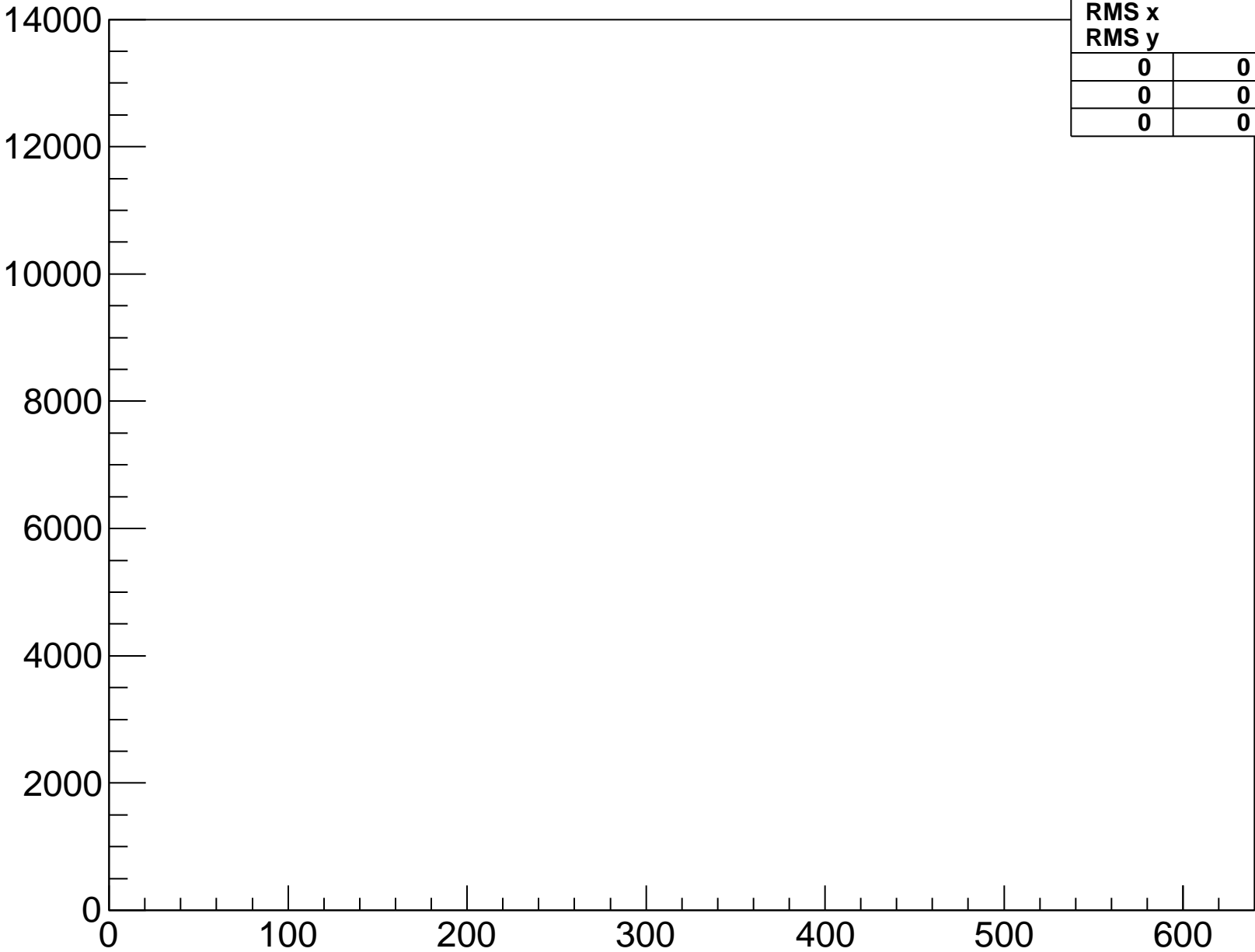


baselinesamples-fpga-6-hyb-0-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	



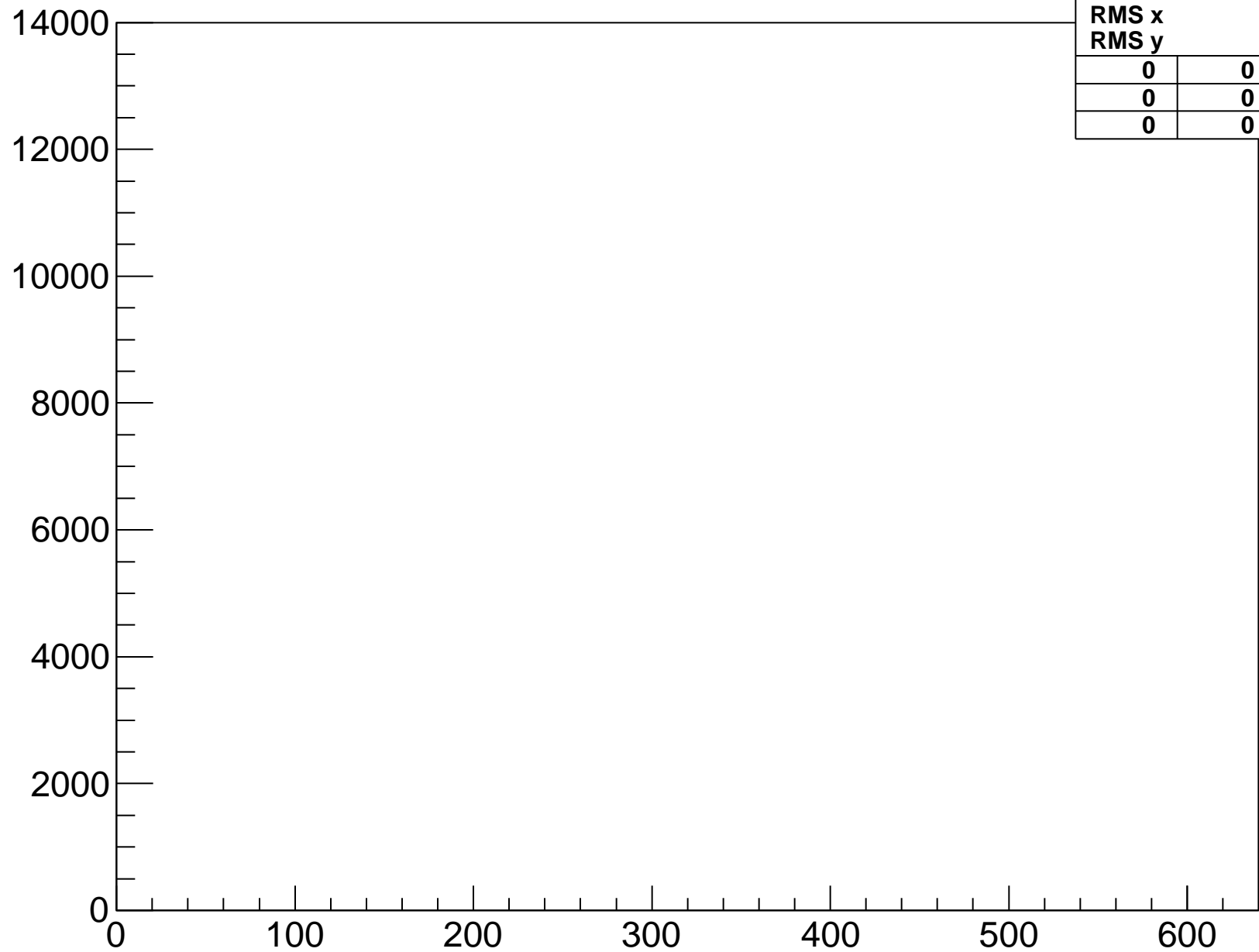
baselinesamples-fpga-6-hyb-0-sample-2



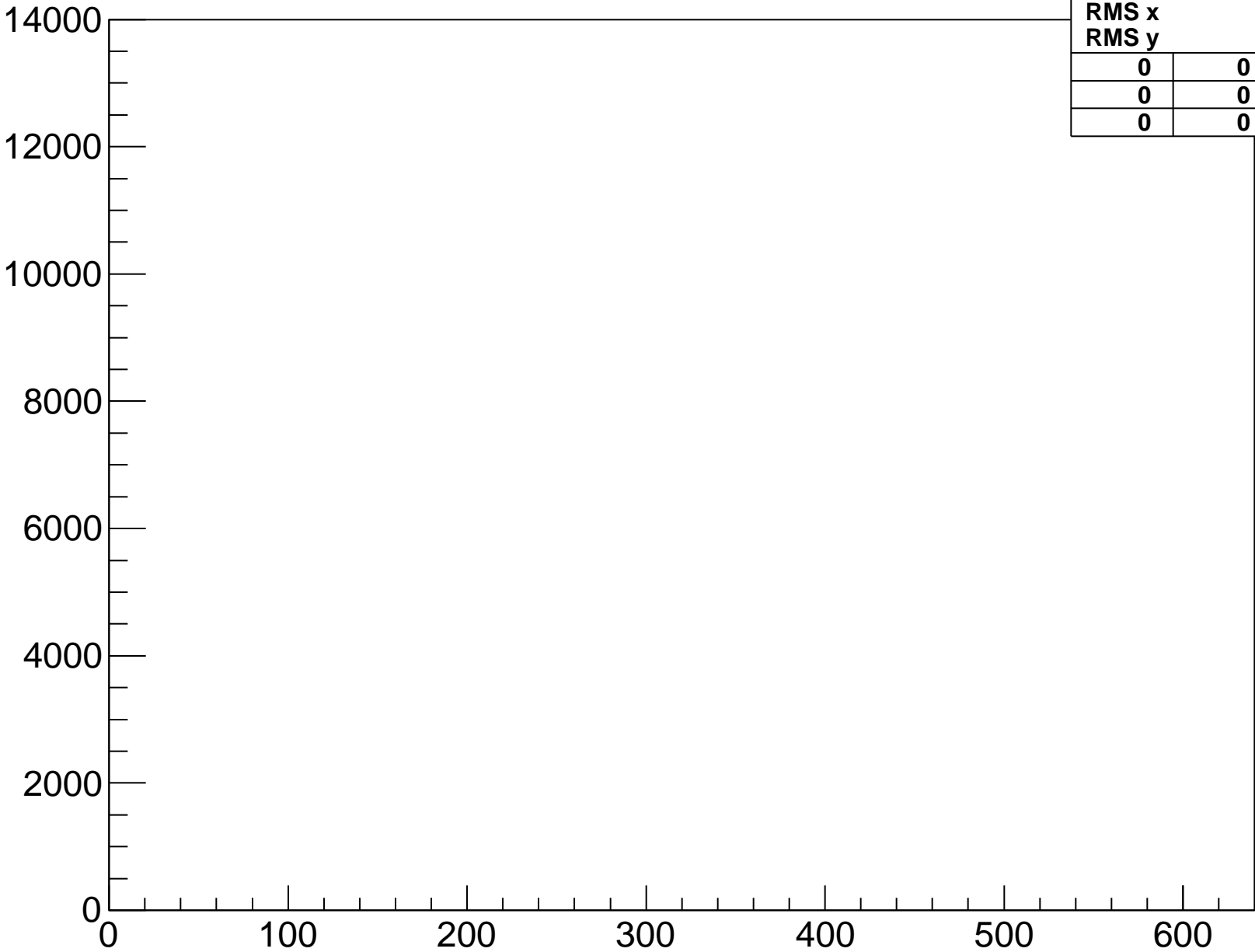
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-6-hyb-0-sample-3

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



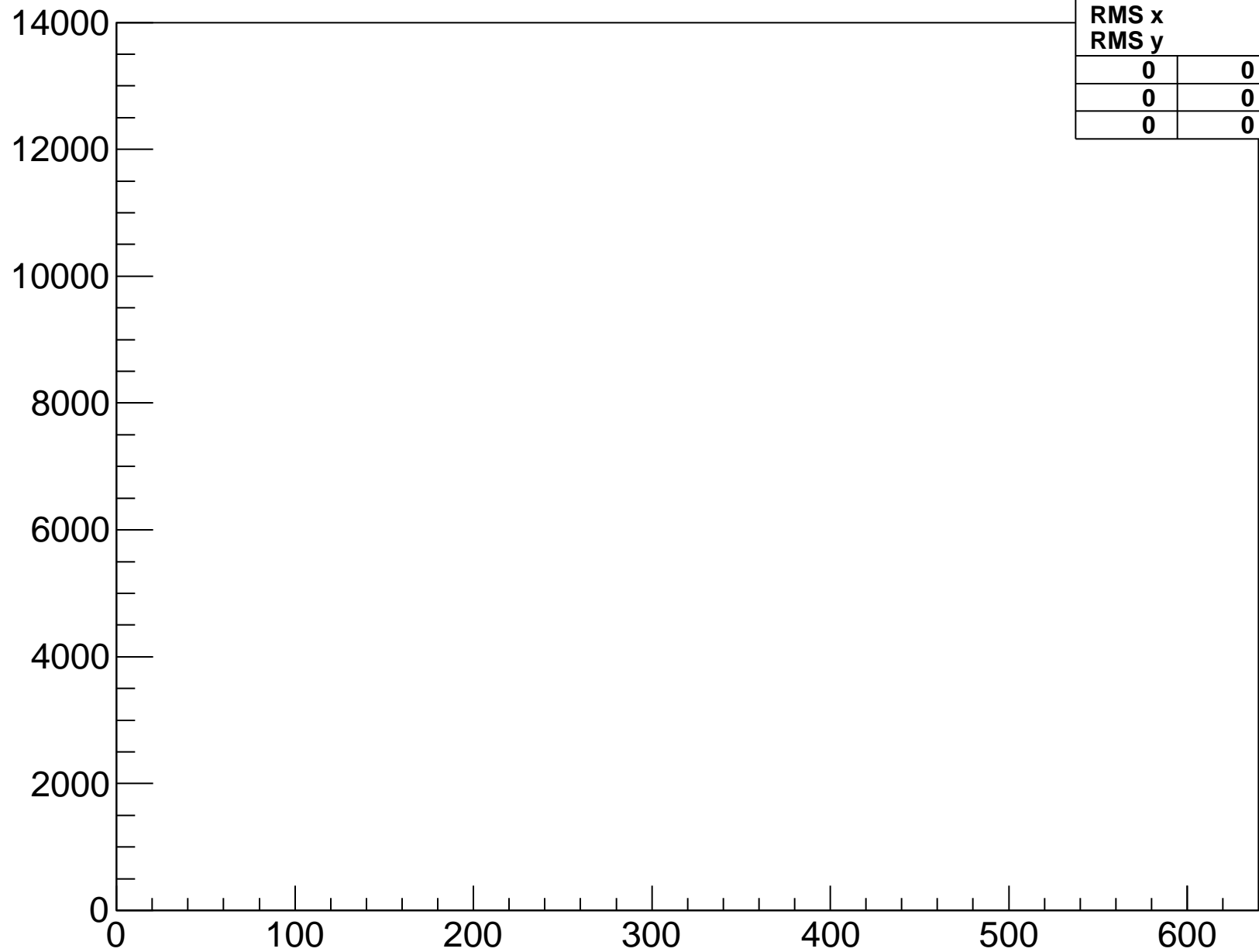
baselinesamples-fpga-6-hyb-0-sample-4



Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	0
0	0	0	0
0	0	0	0

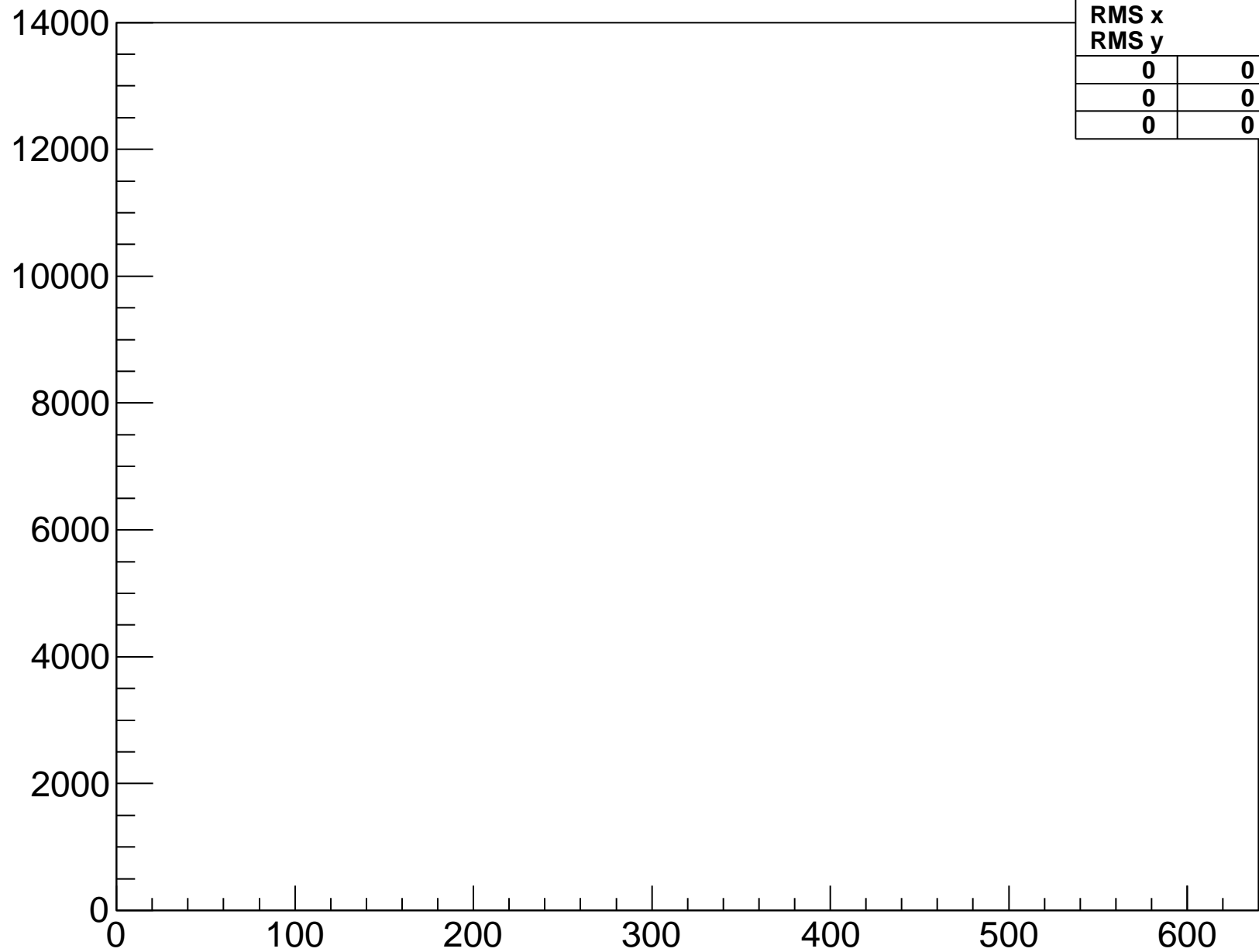
baselinesamples-fpga-6-hyb-0-sample-5

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



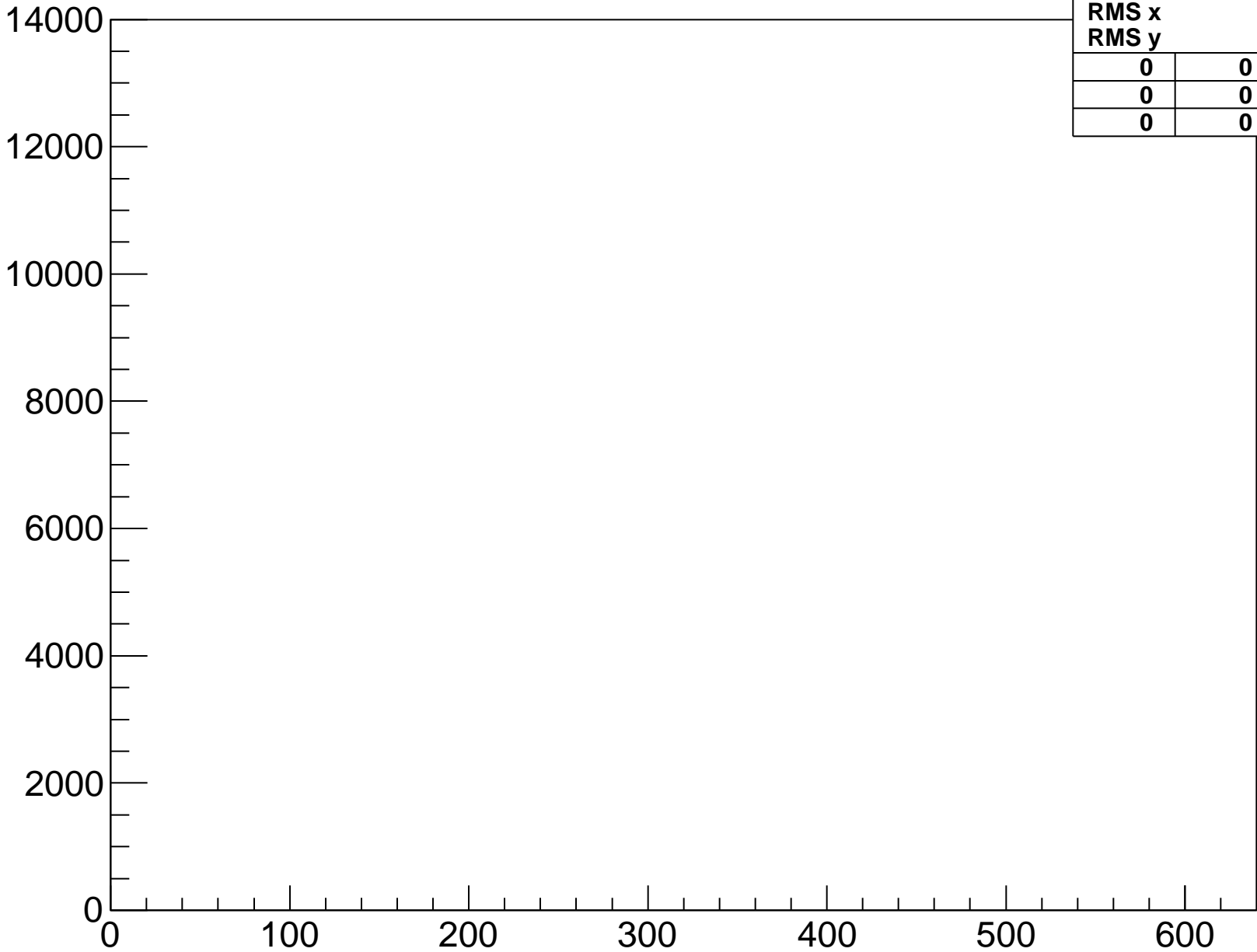
baselinesamples-fpga-6-hyb-1-sample-0

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

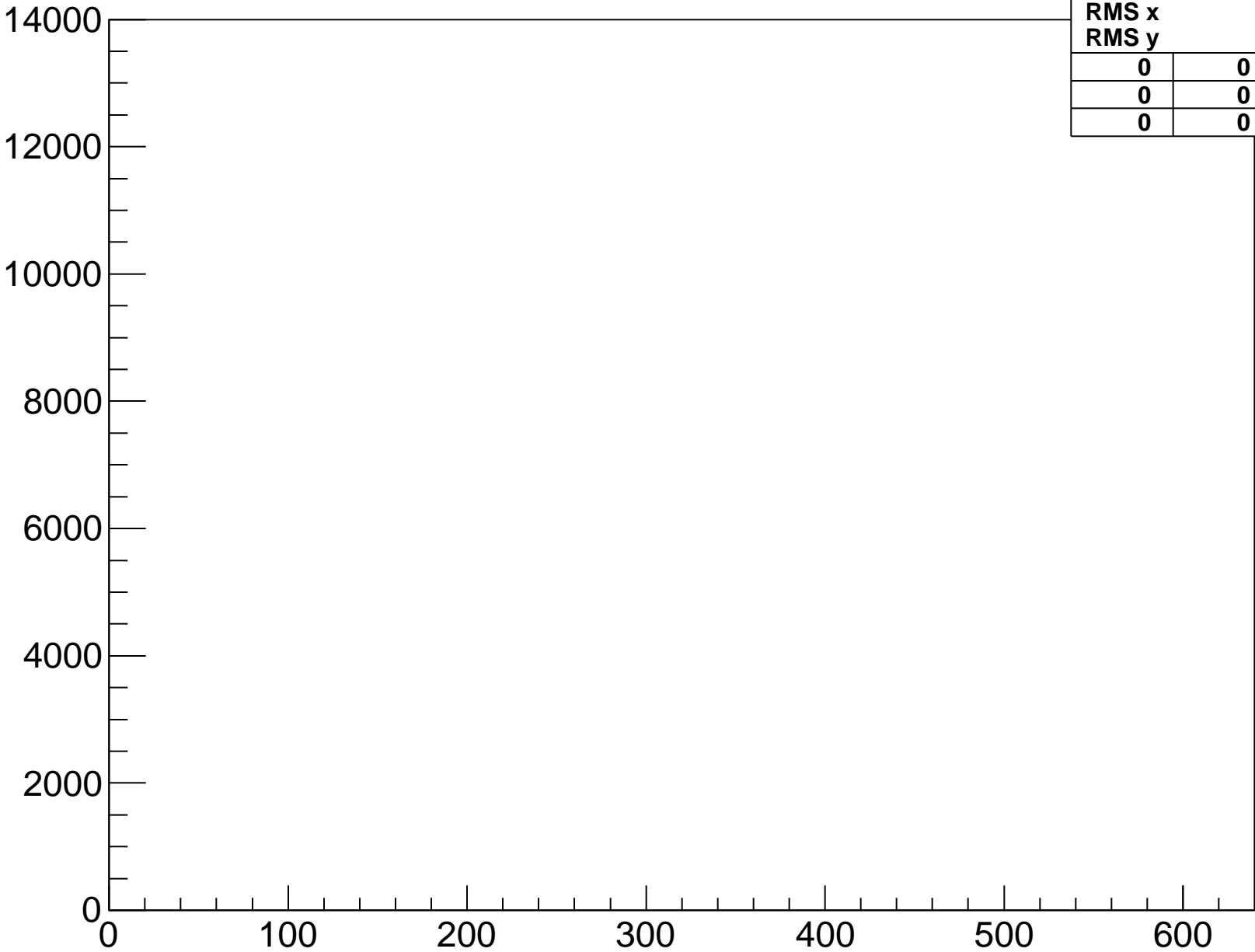


baselinesamples-fpga-6-hyb-1-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

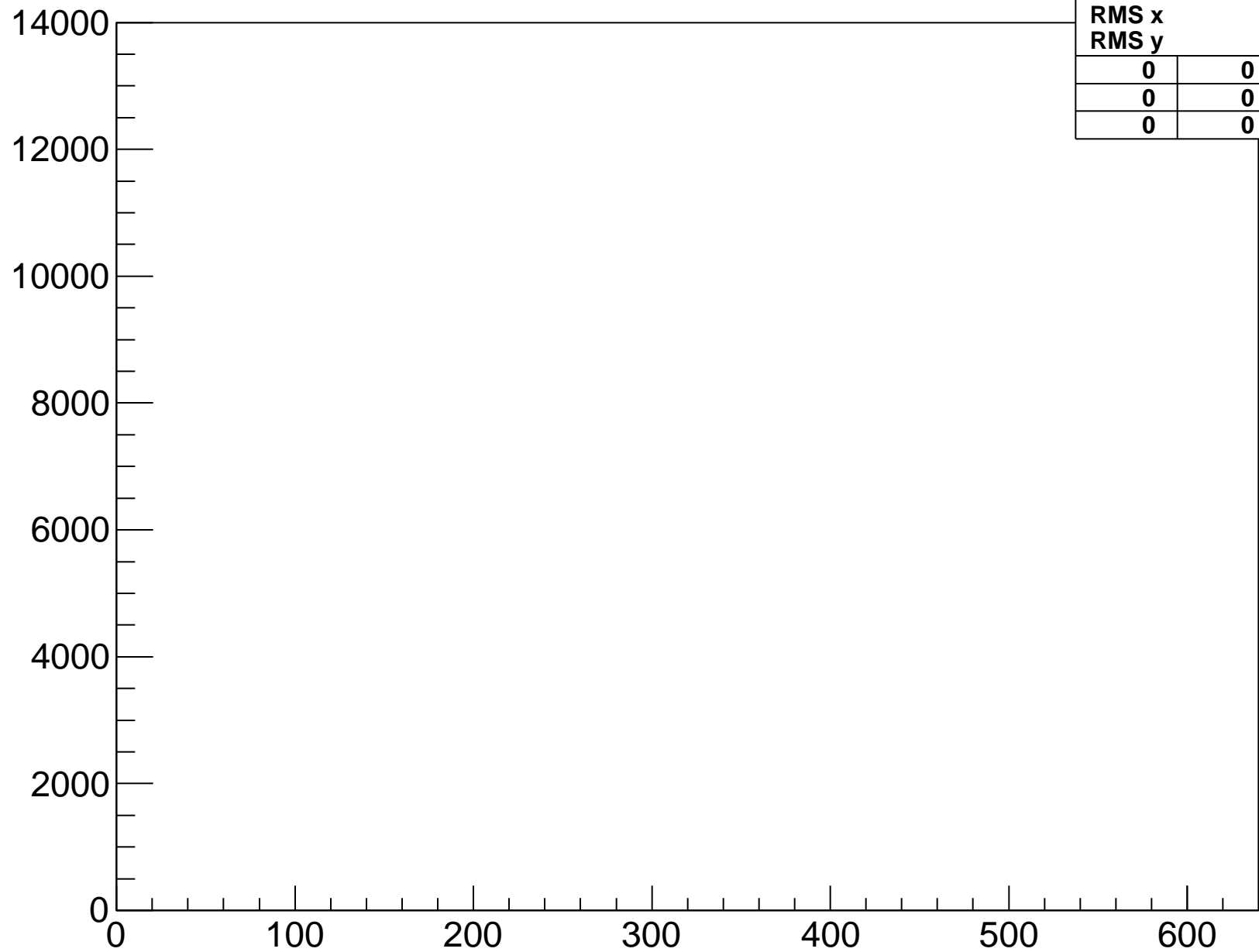


baselinesamples-fpga-6-hyb-1-sample-2



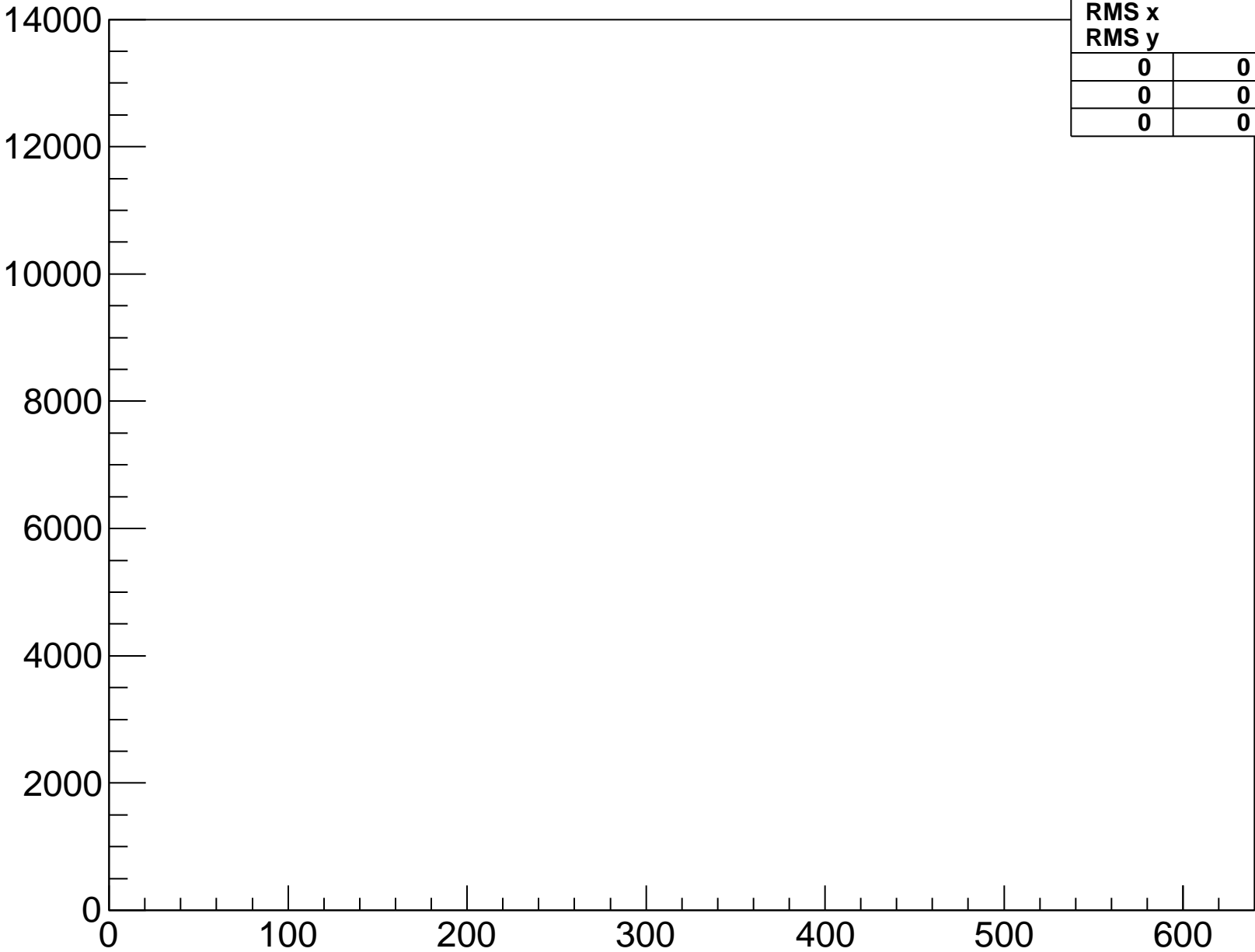
Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-6-hyb-1-sample-3



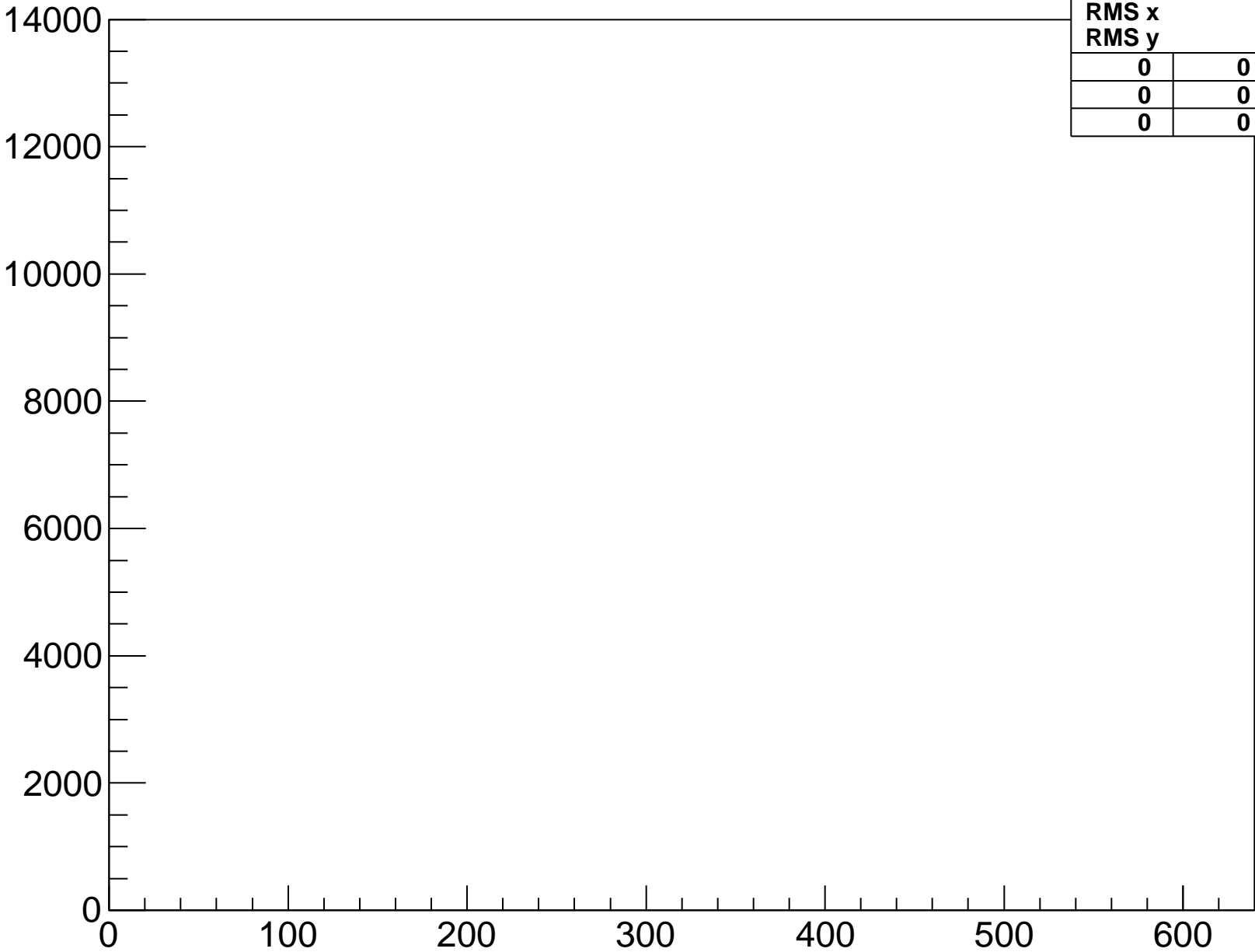
Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	
0	0	0	
0	0	0	

baselinesamples-fpga-6-hyb-1-sample-4



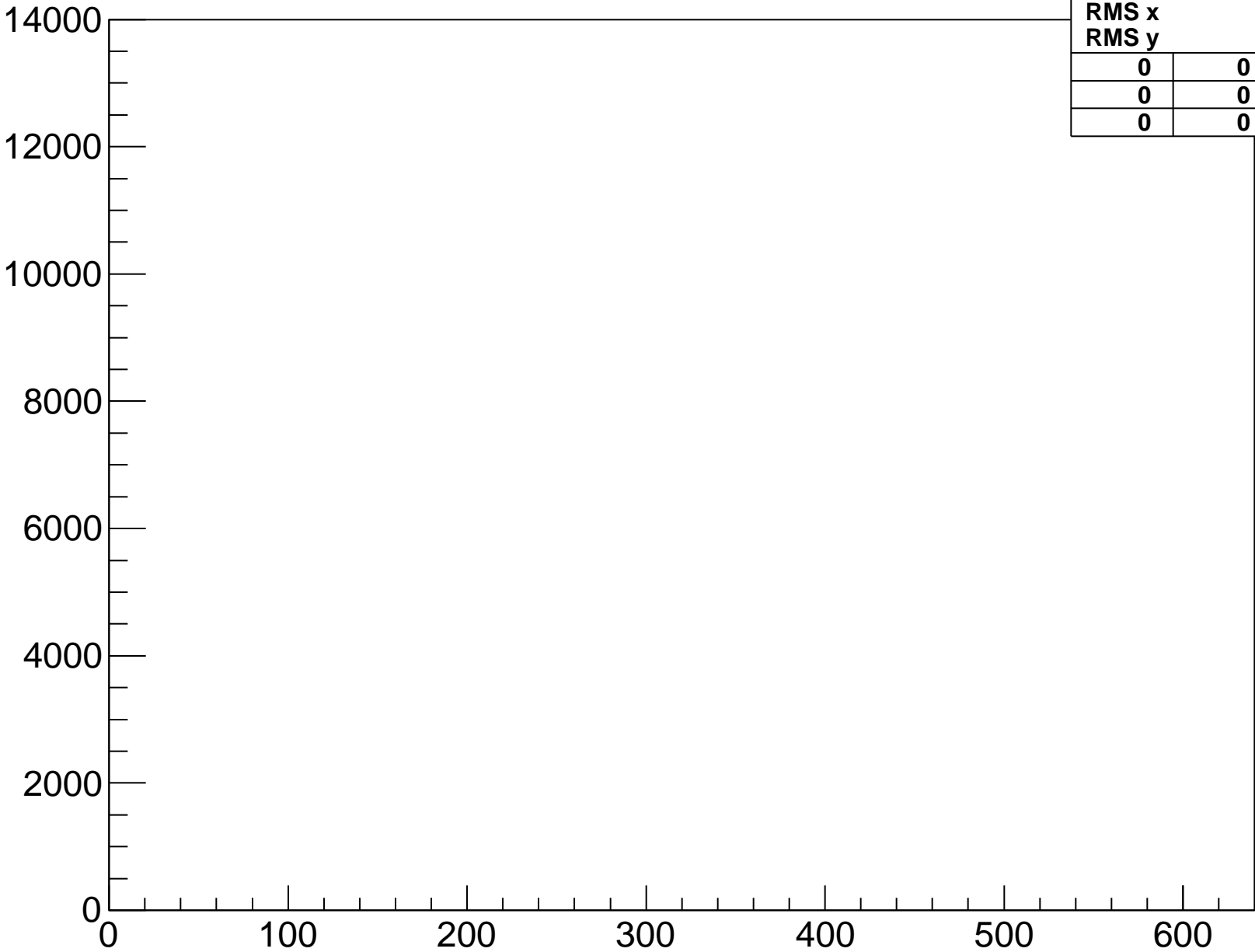
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-6-hyb-1-sample-5



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

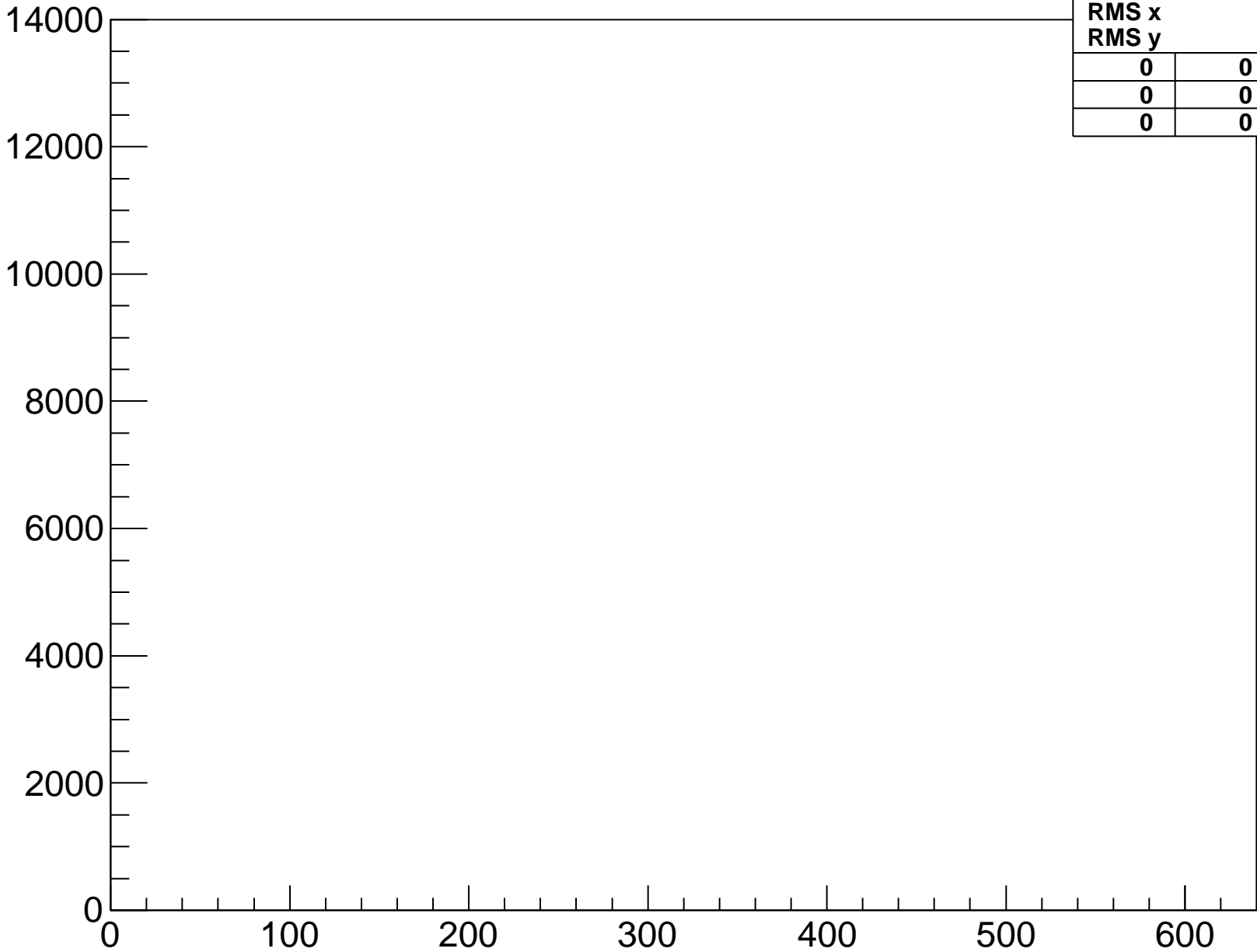
baselinesamples-fpga-6-hyb-2-sample-0



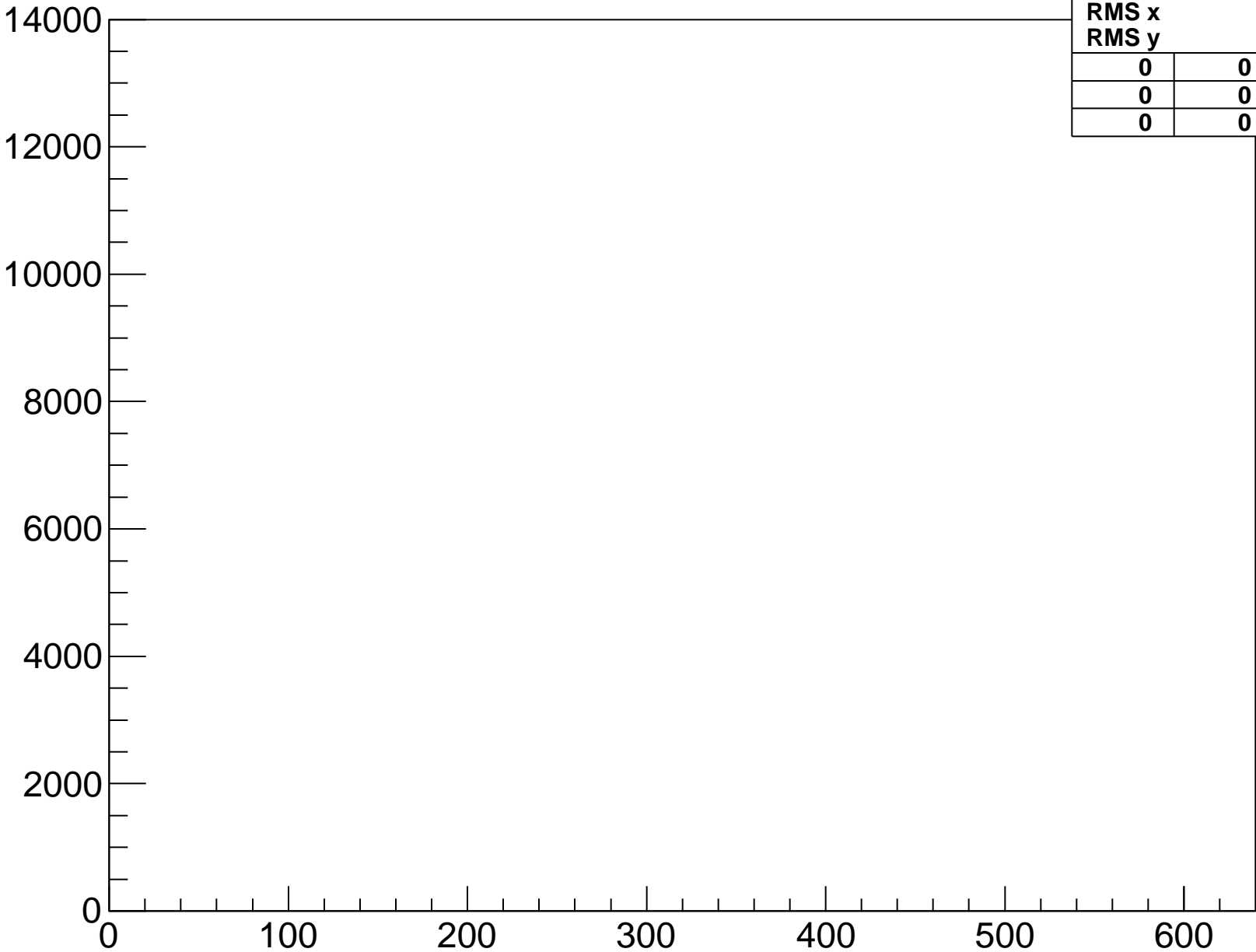
Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	
0	0	0	
0	0	0	

baselinesamples-fpga-6-hyb-2-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

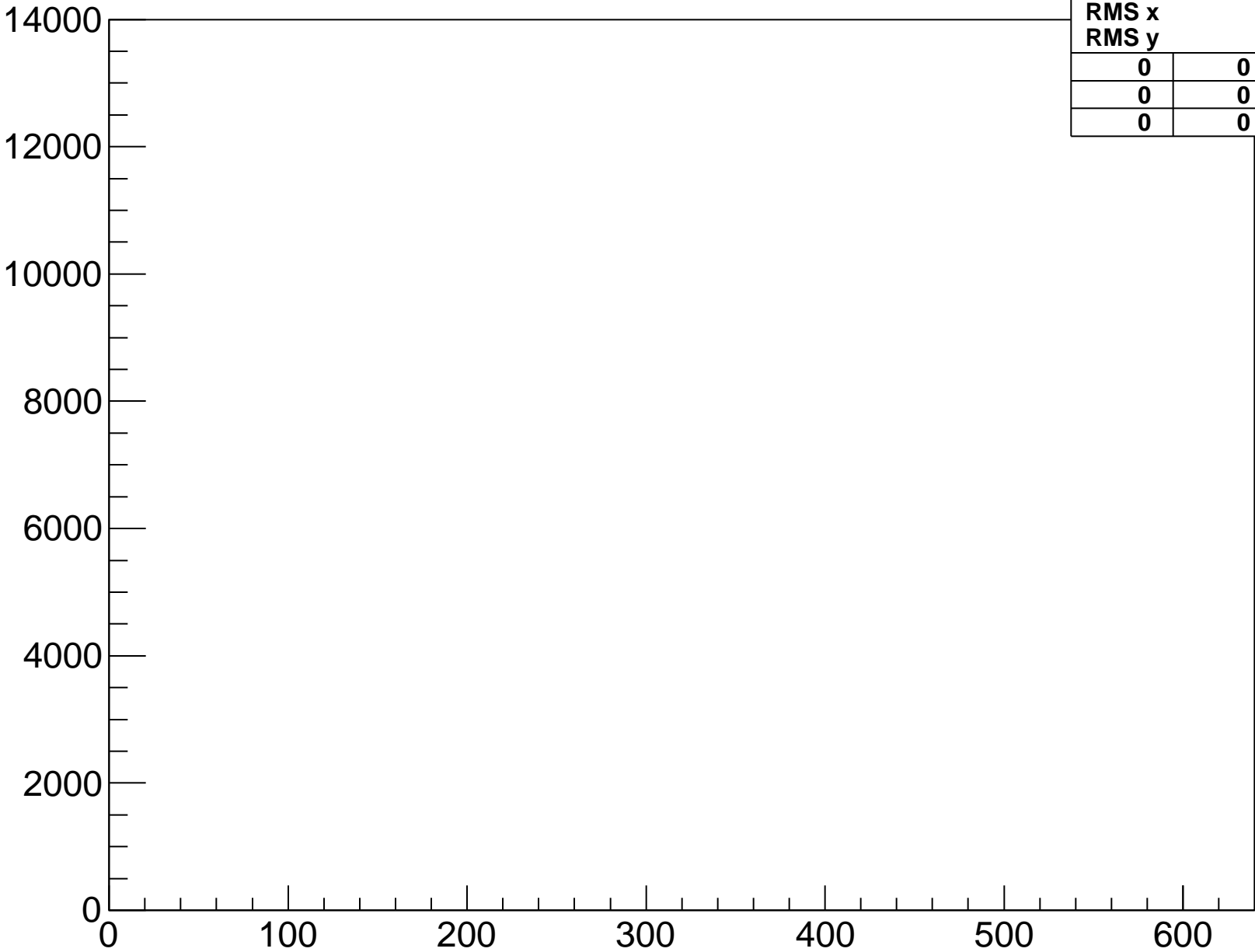


baselinesamples-fpga-6-hyb-2-sample-2



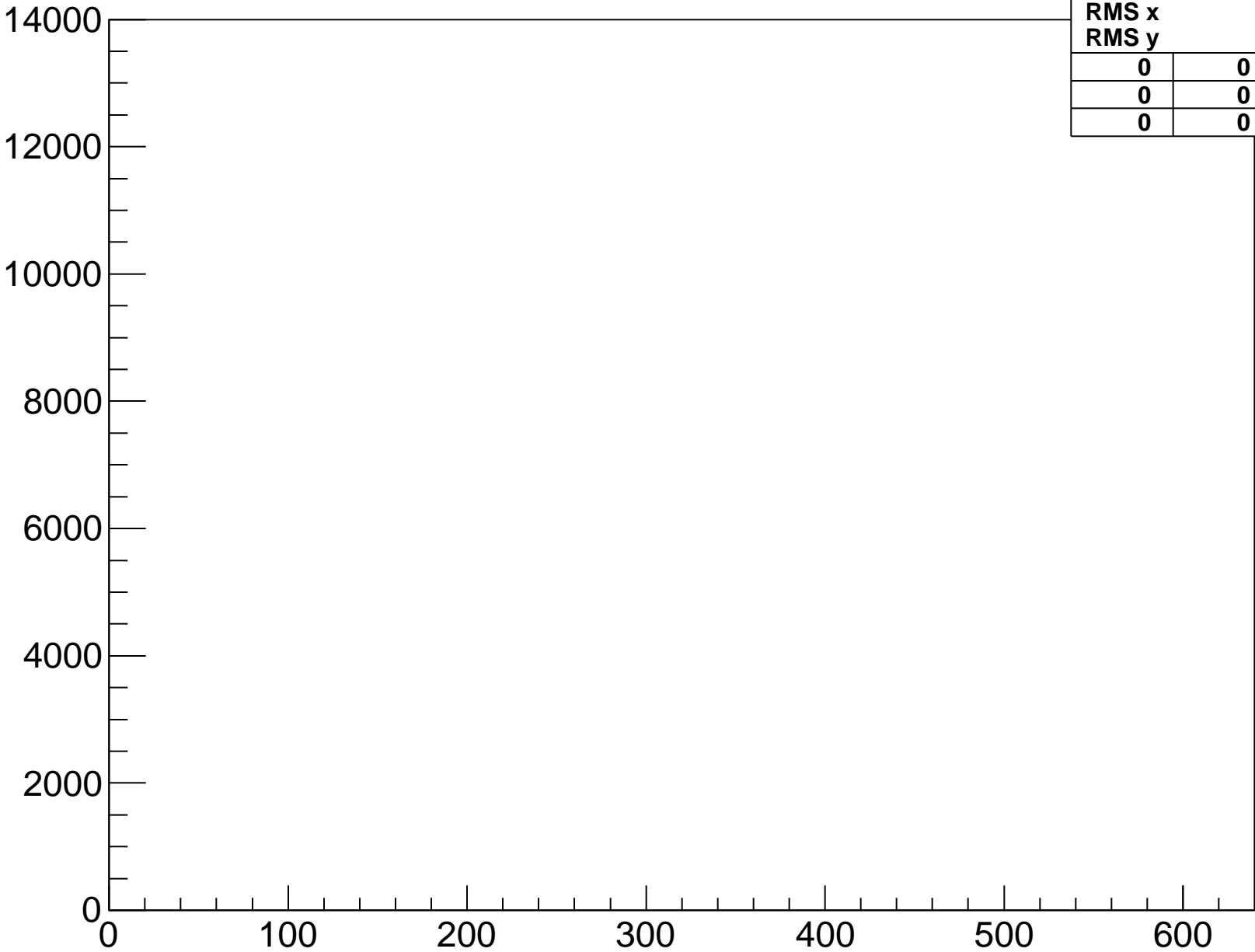
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-6-hyb-2-sample-3



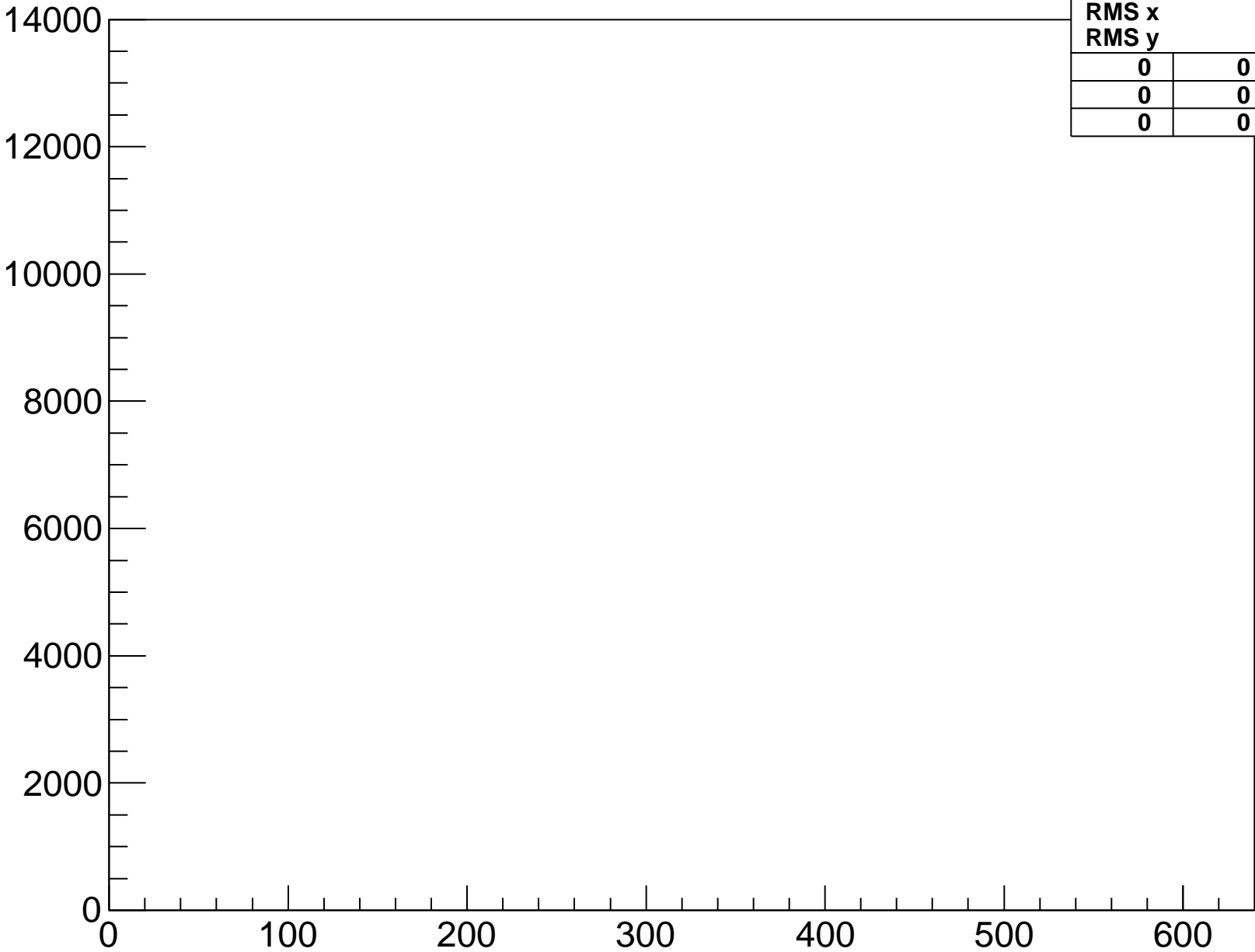
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-6-hyb-2-sample-4



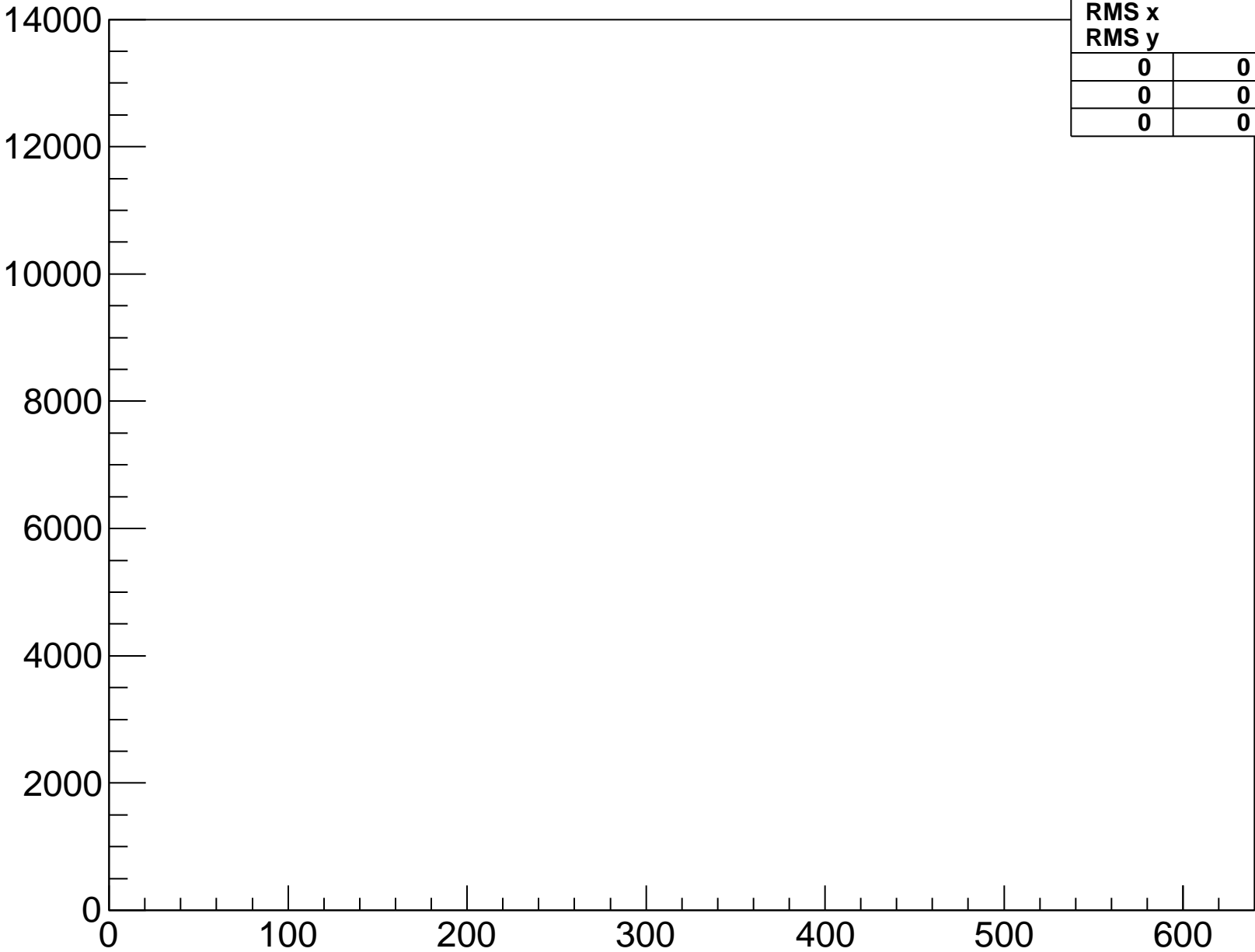
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-6-hyb-2-sample-5



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

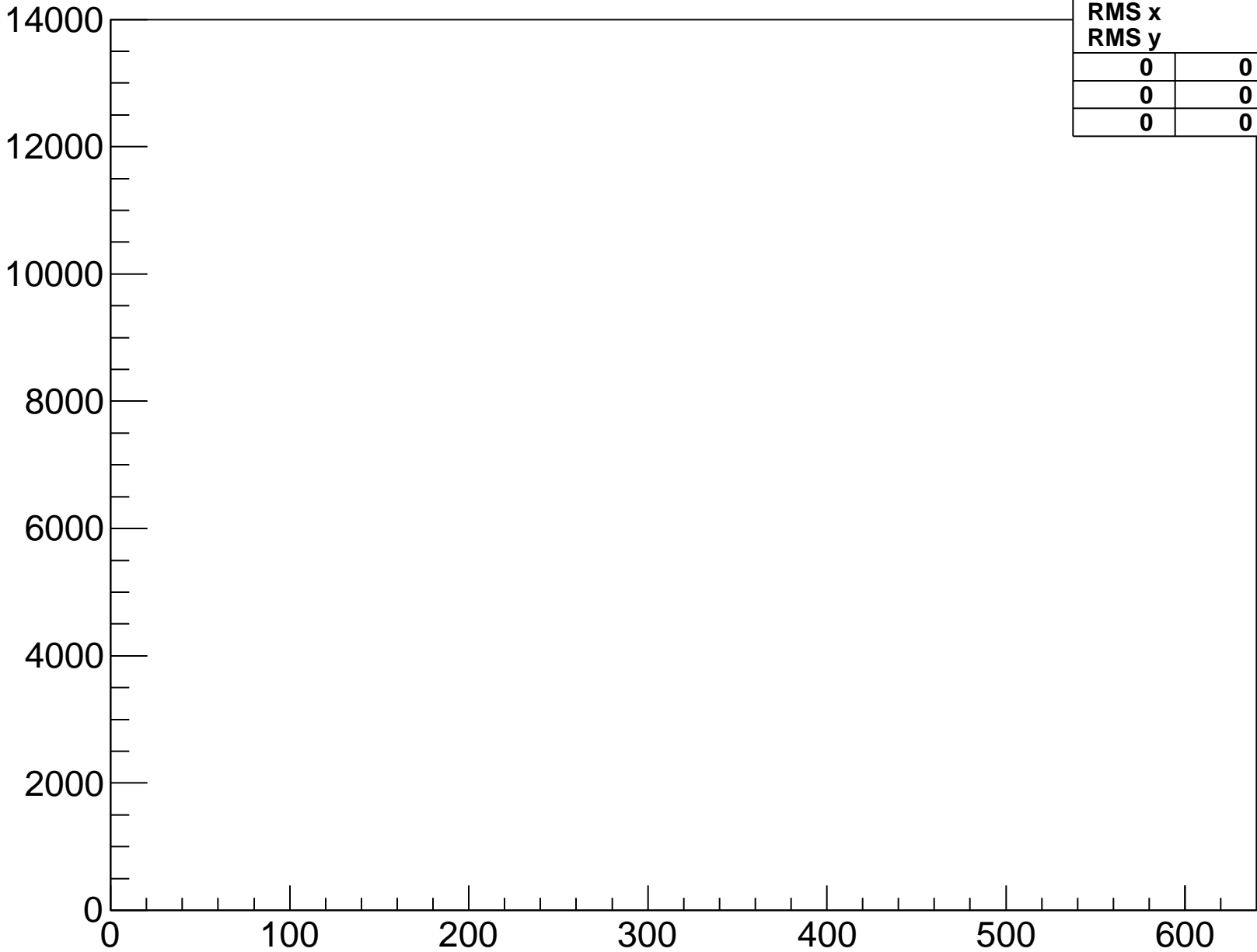
baselinesamples-fpga-6-hyb-3-sample-0



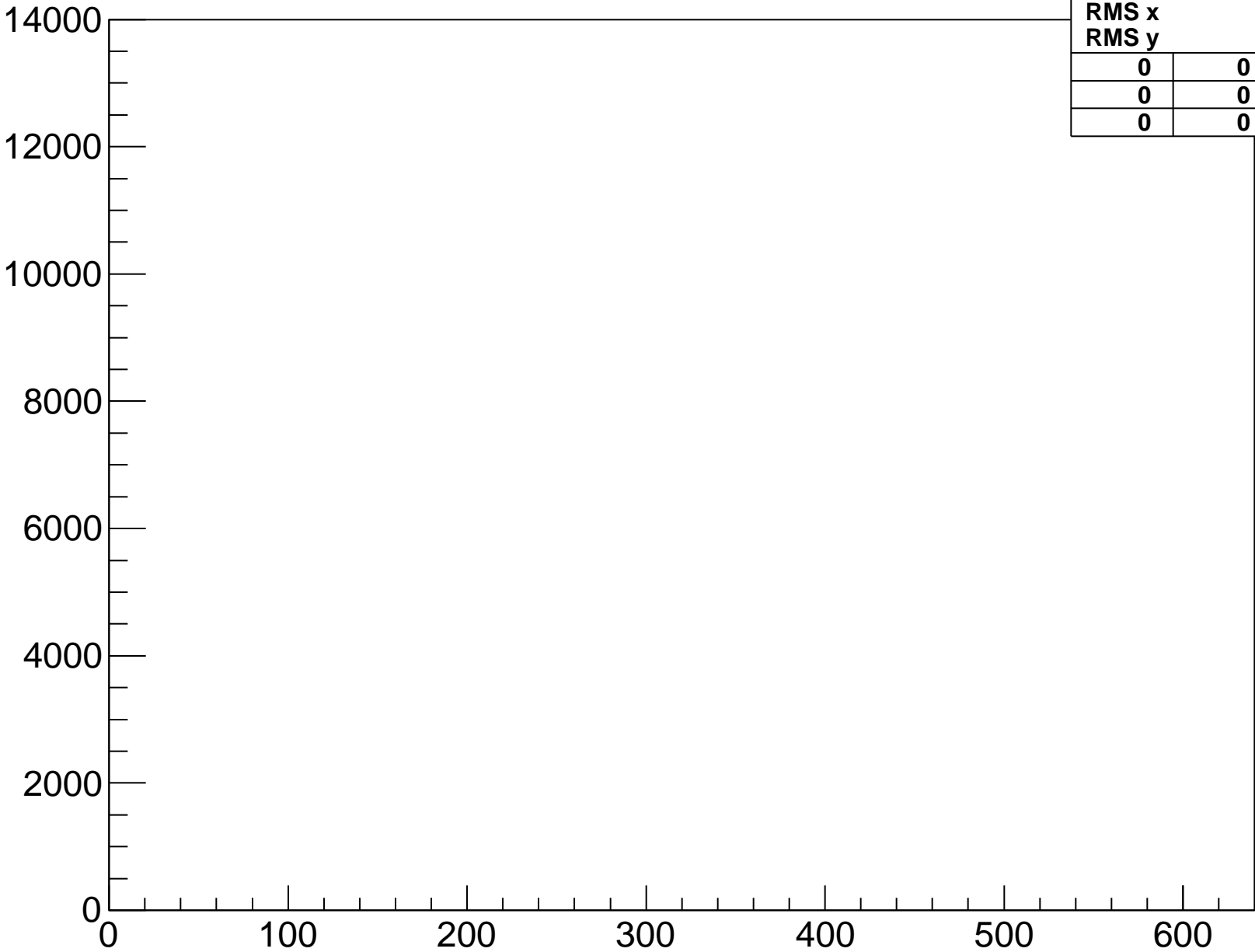
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-6-hyb-3-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

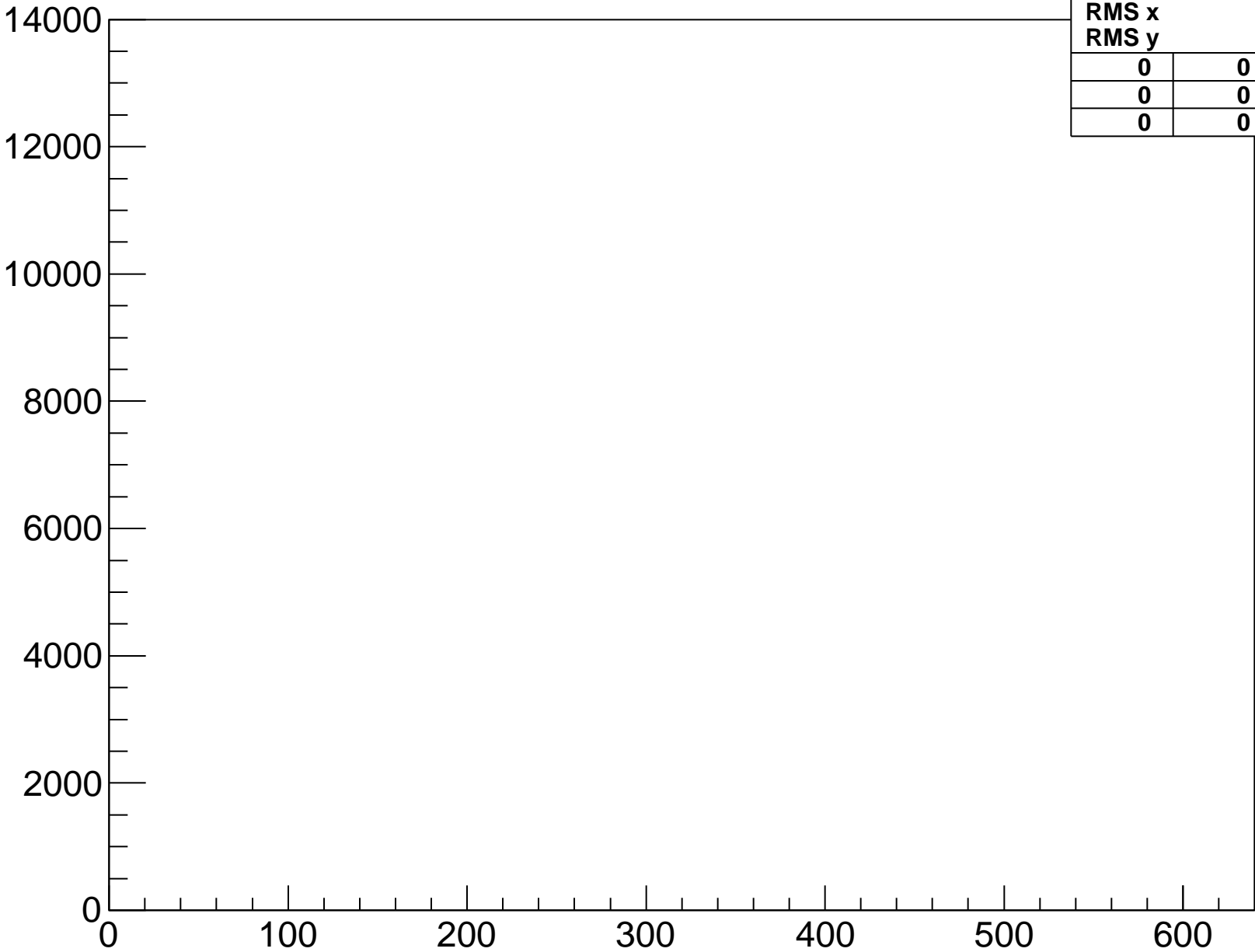


baselinesamples-fpga-6-hyb-3-sample-2



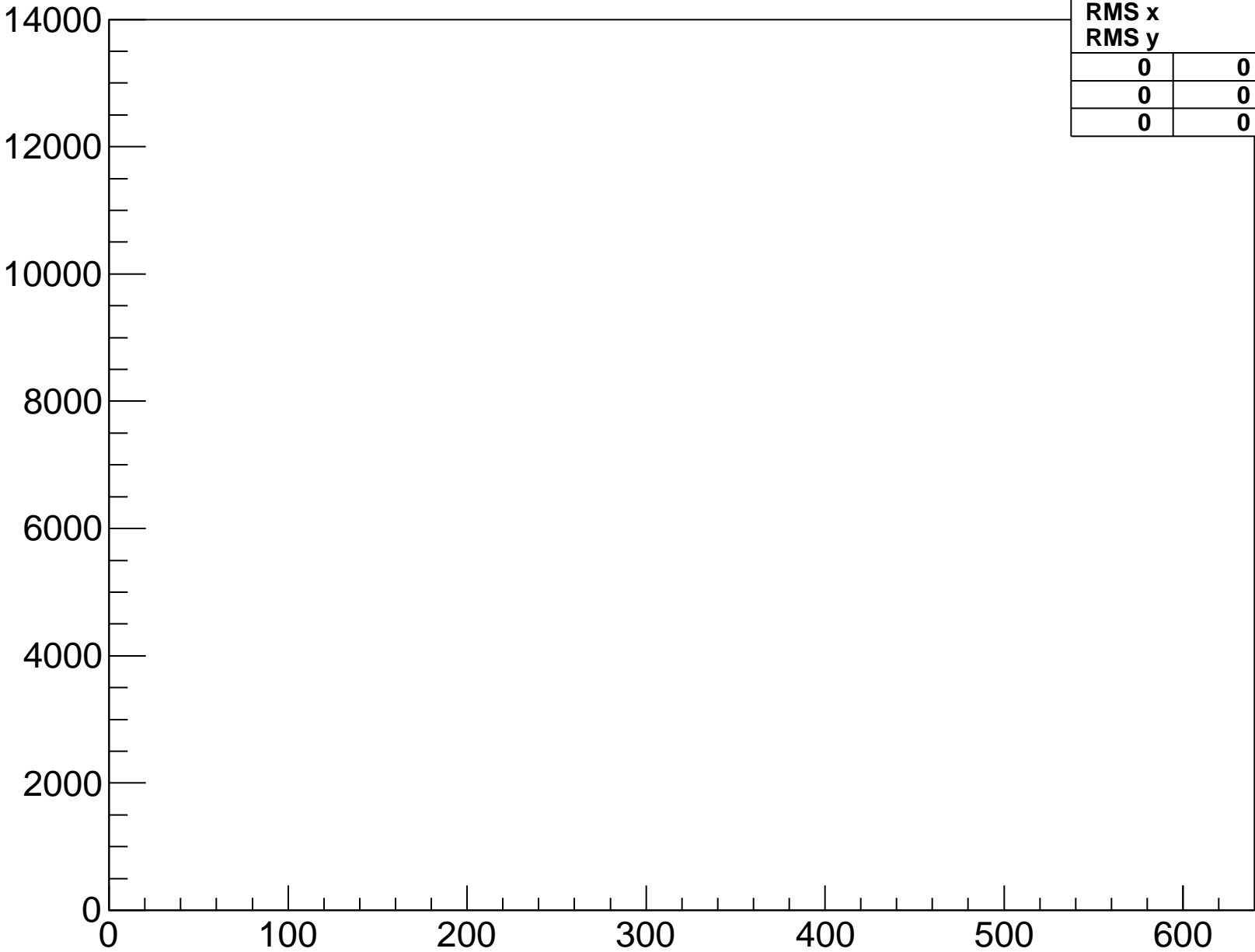
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-6-hyb-3-sample-3



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

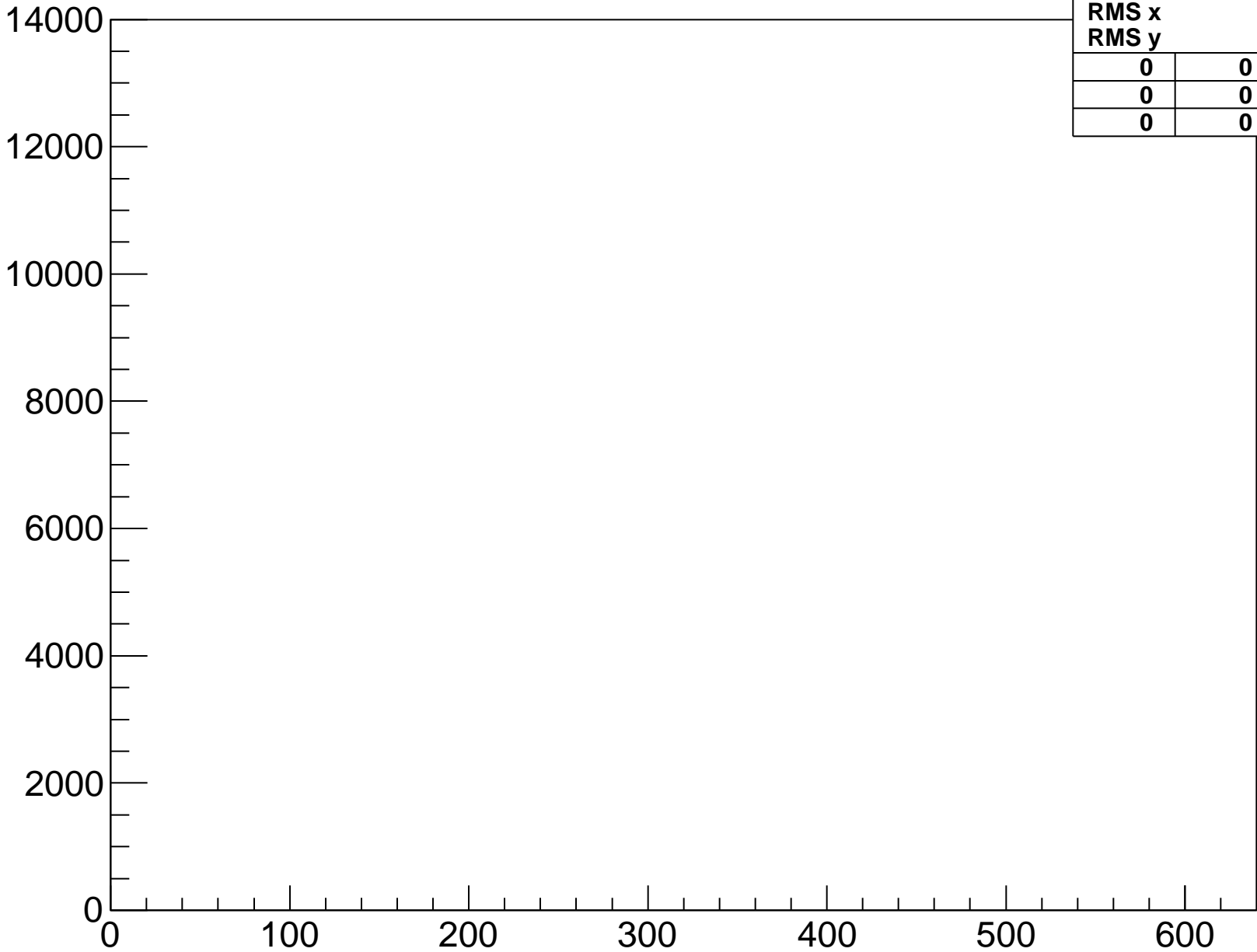
baselinesamples-fpga-6-hyb-3-sample-4



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

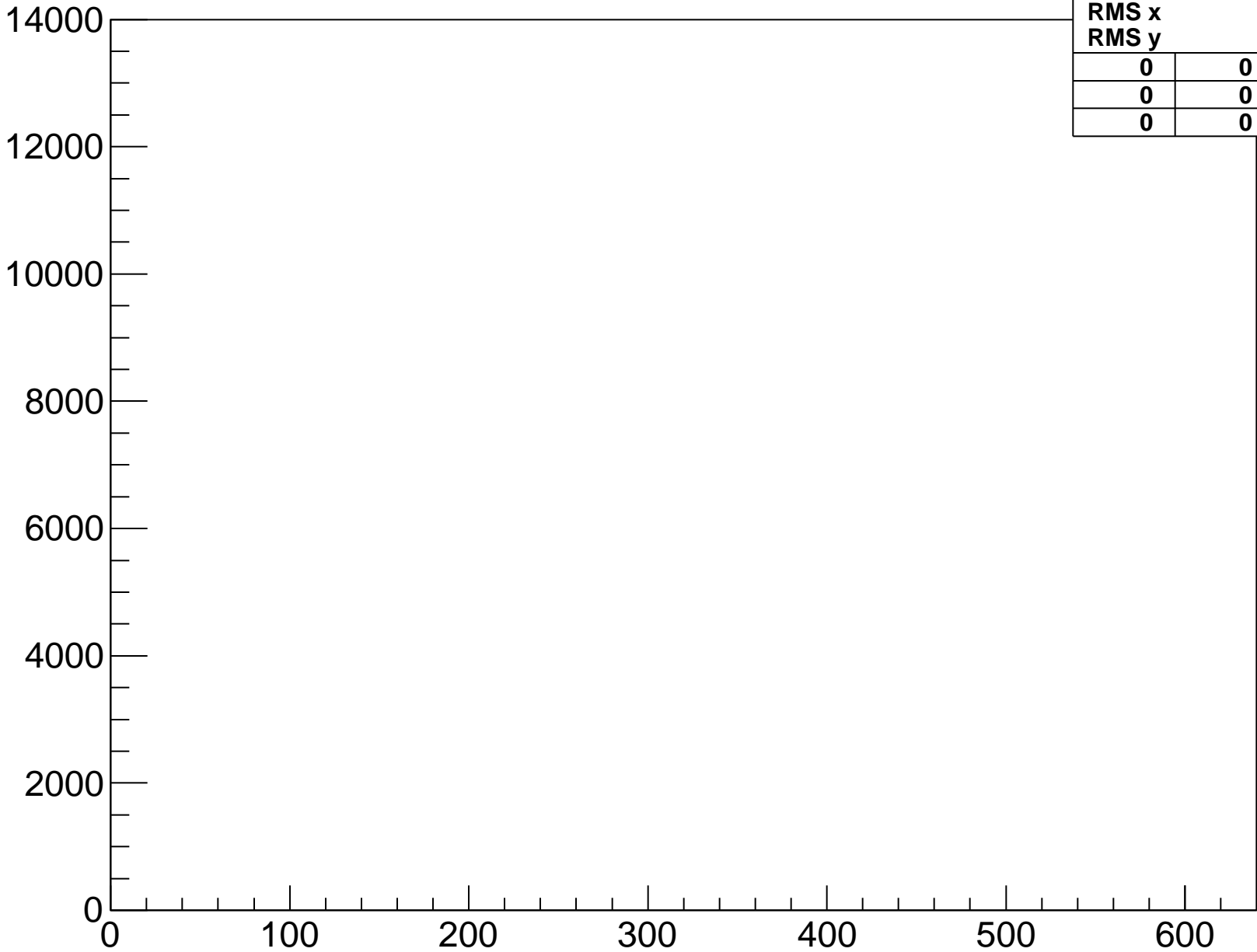
baselinesamples-fpga-6-hyb-3-sample-5

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	



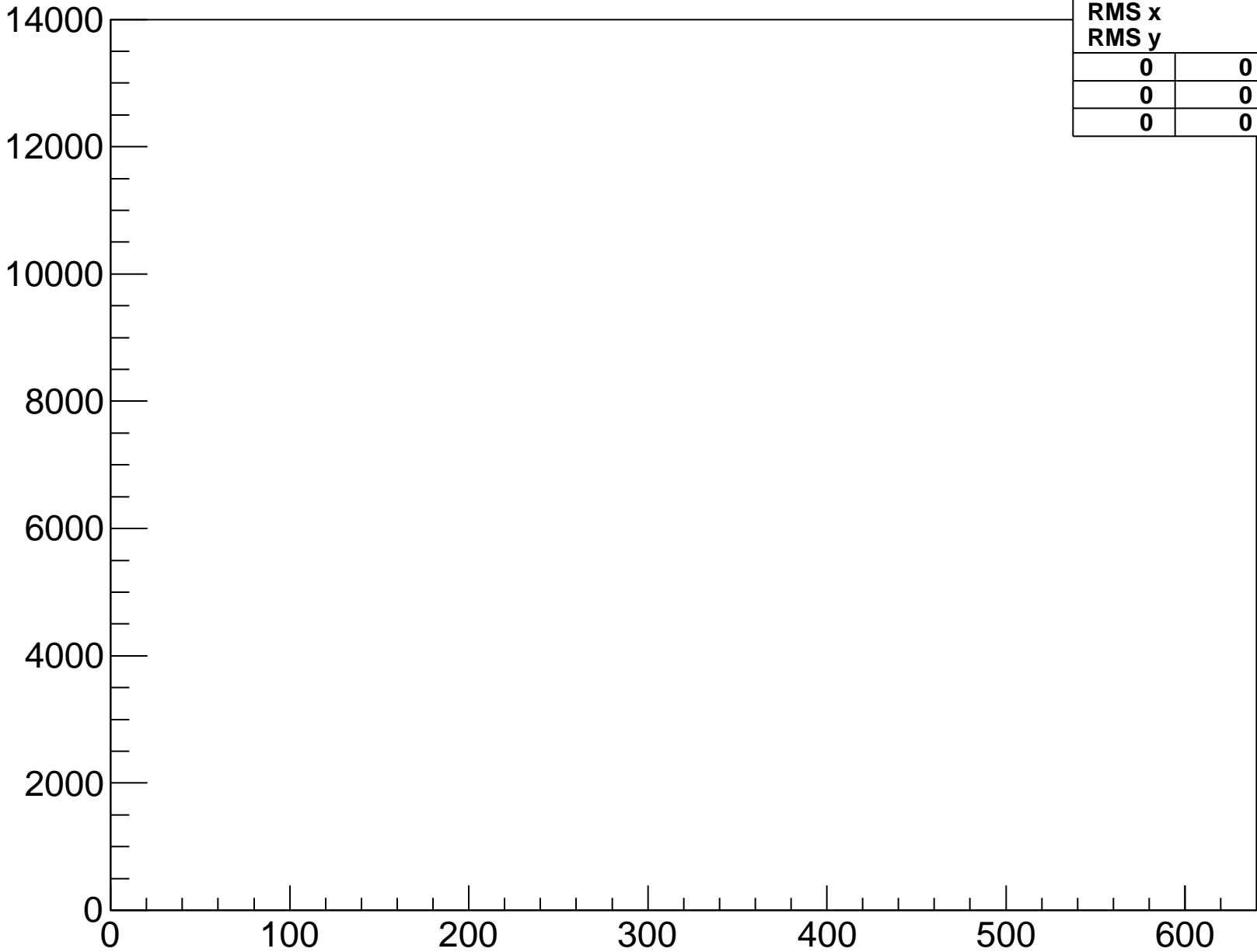
baselinesamples-fpga-7-hyb-0-sample-0

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



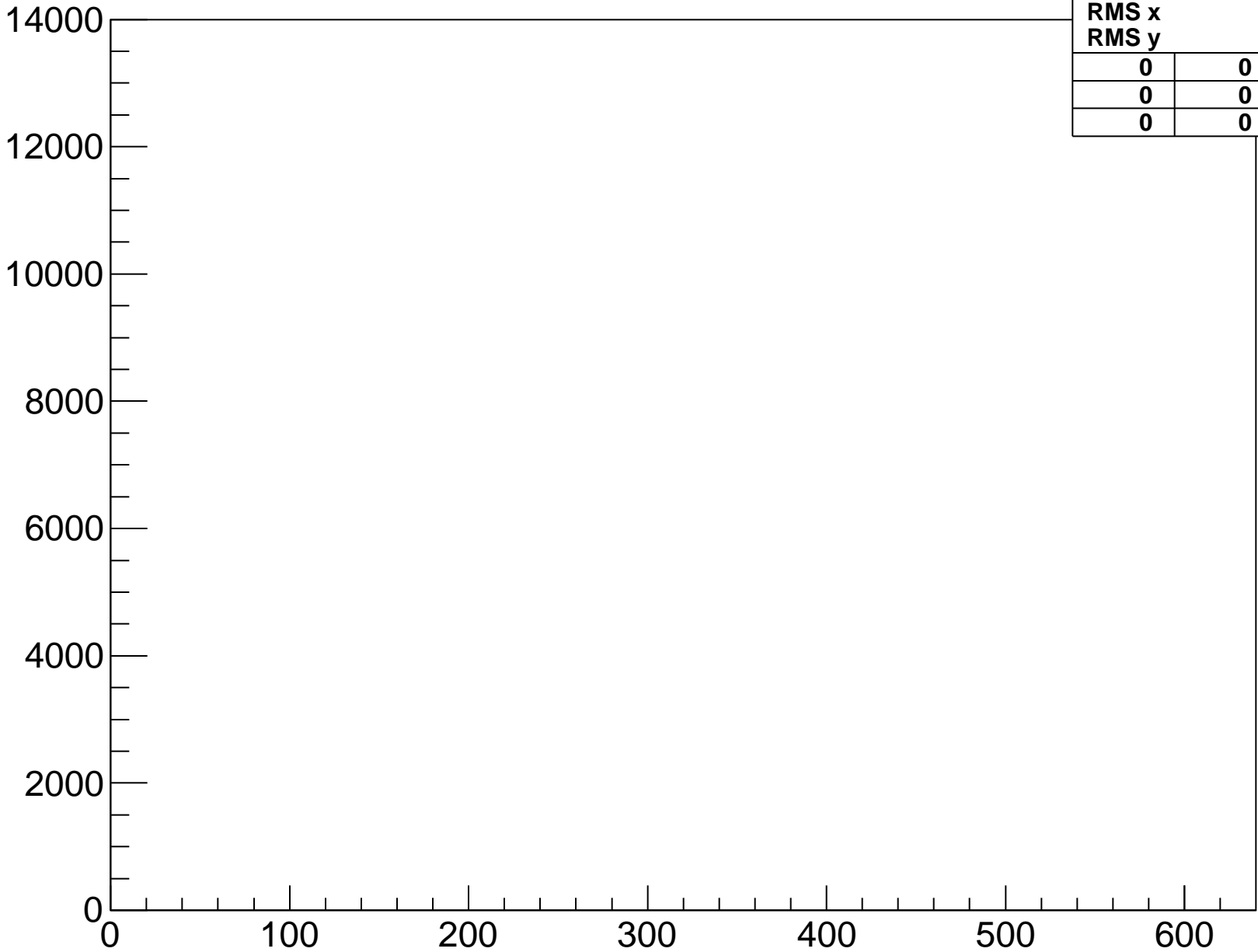
baselinesamples-fpga-7-hyb-0-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

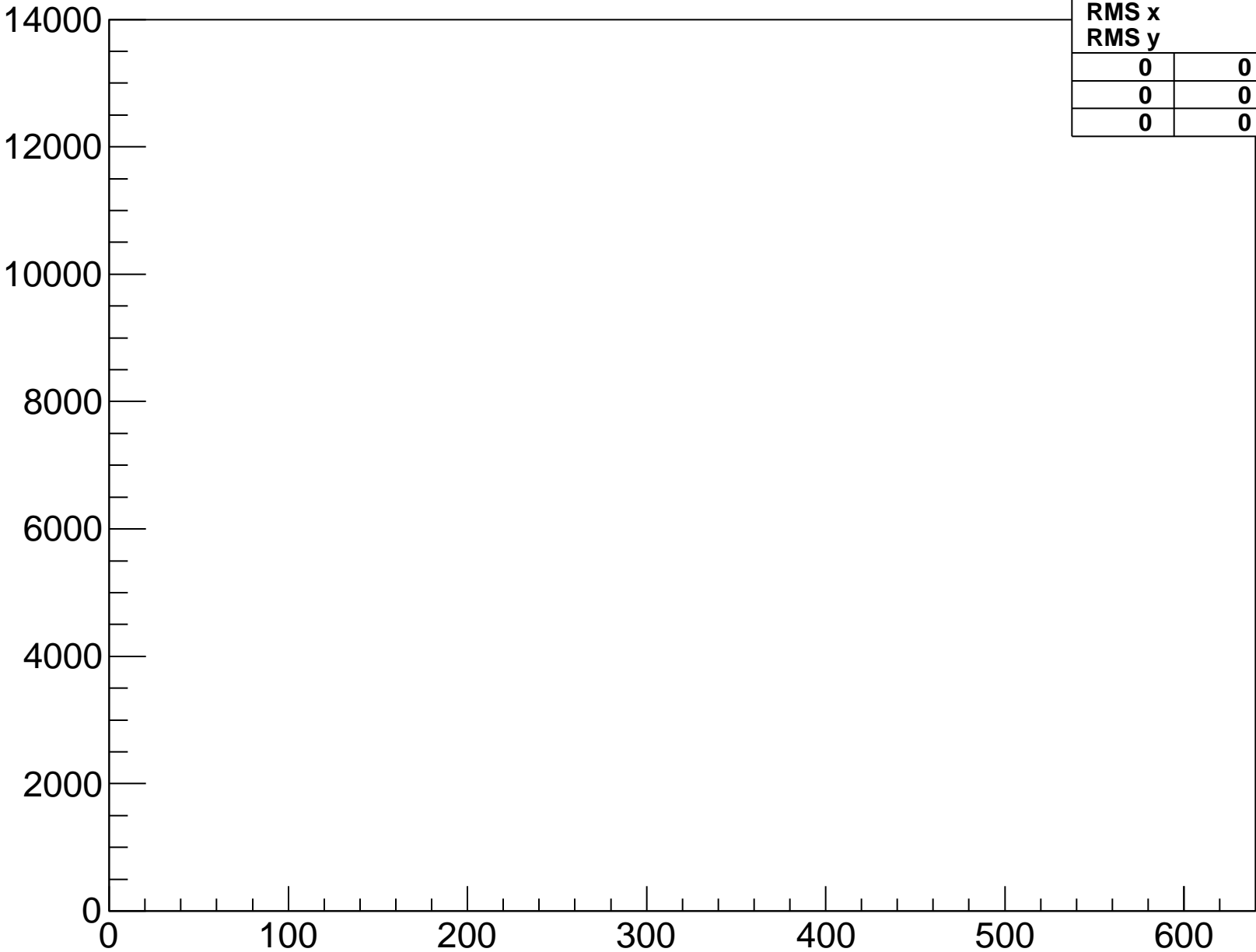


baselinesamples-fpga-7-hyb-0-sample-2

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

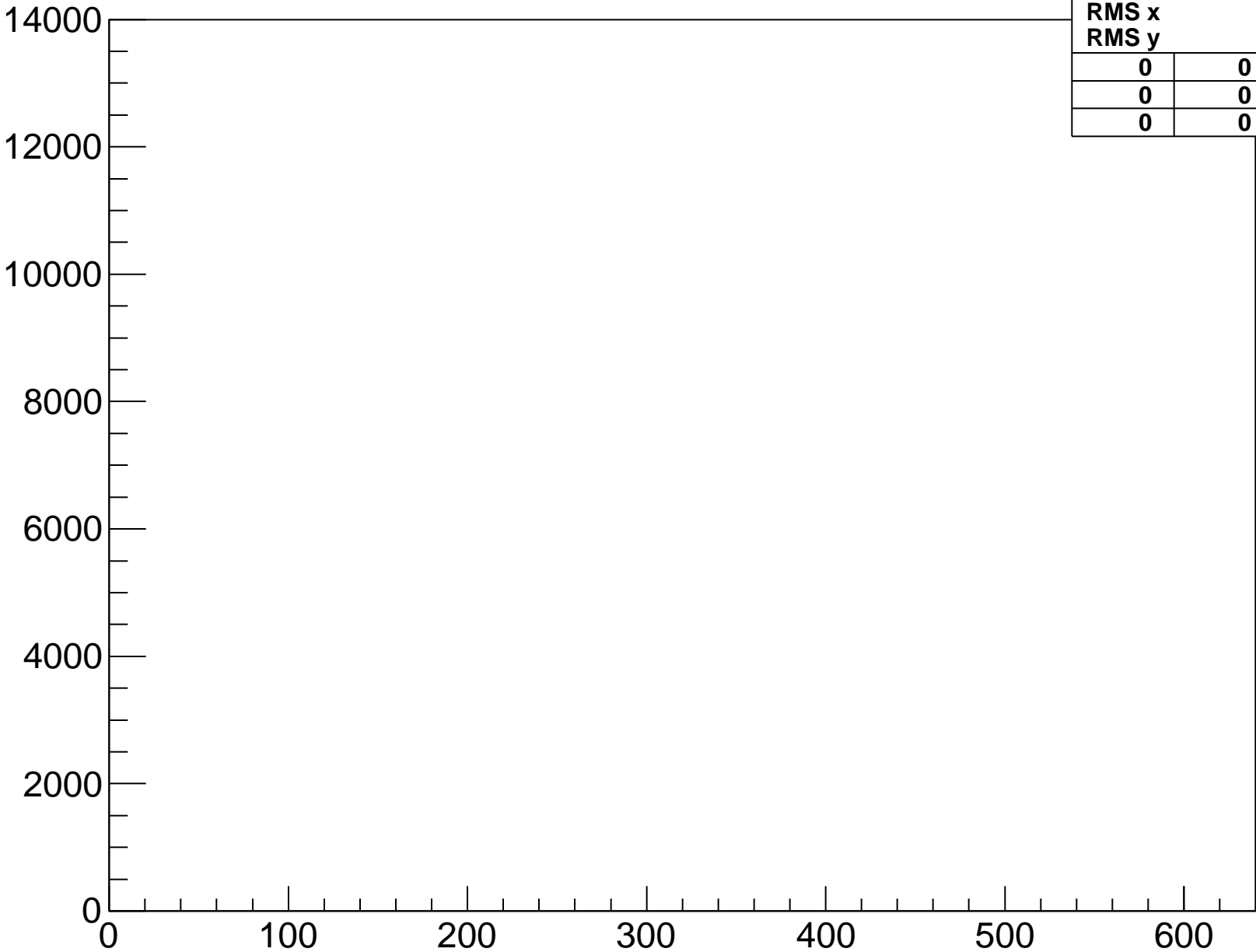


baselinesamples-fpga-7-hyb-0-sample-3



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

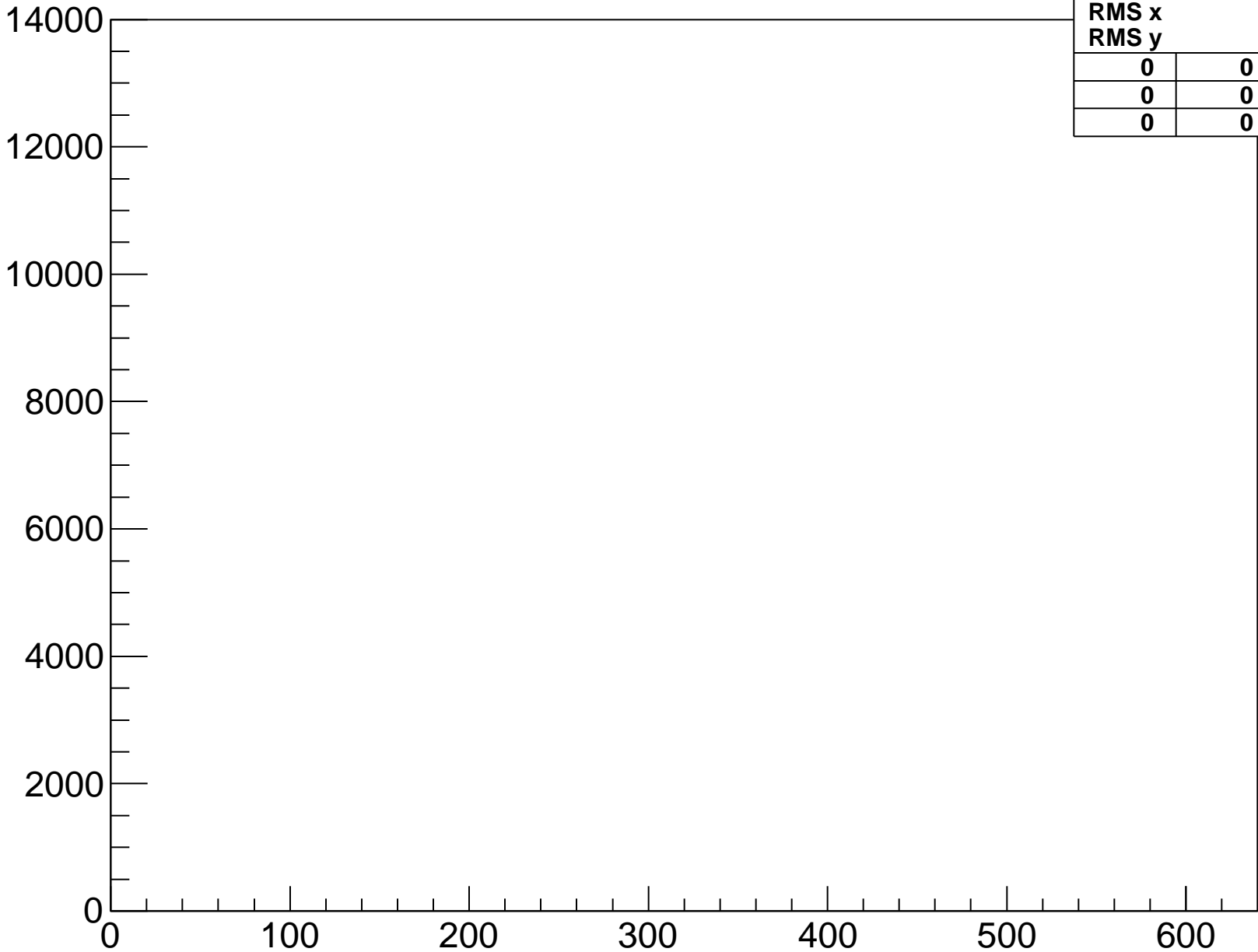
baselinesamples-fpga-7-hyb-0-sample-4



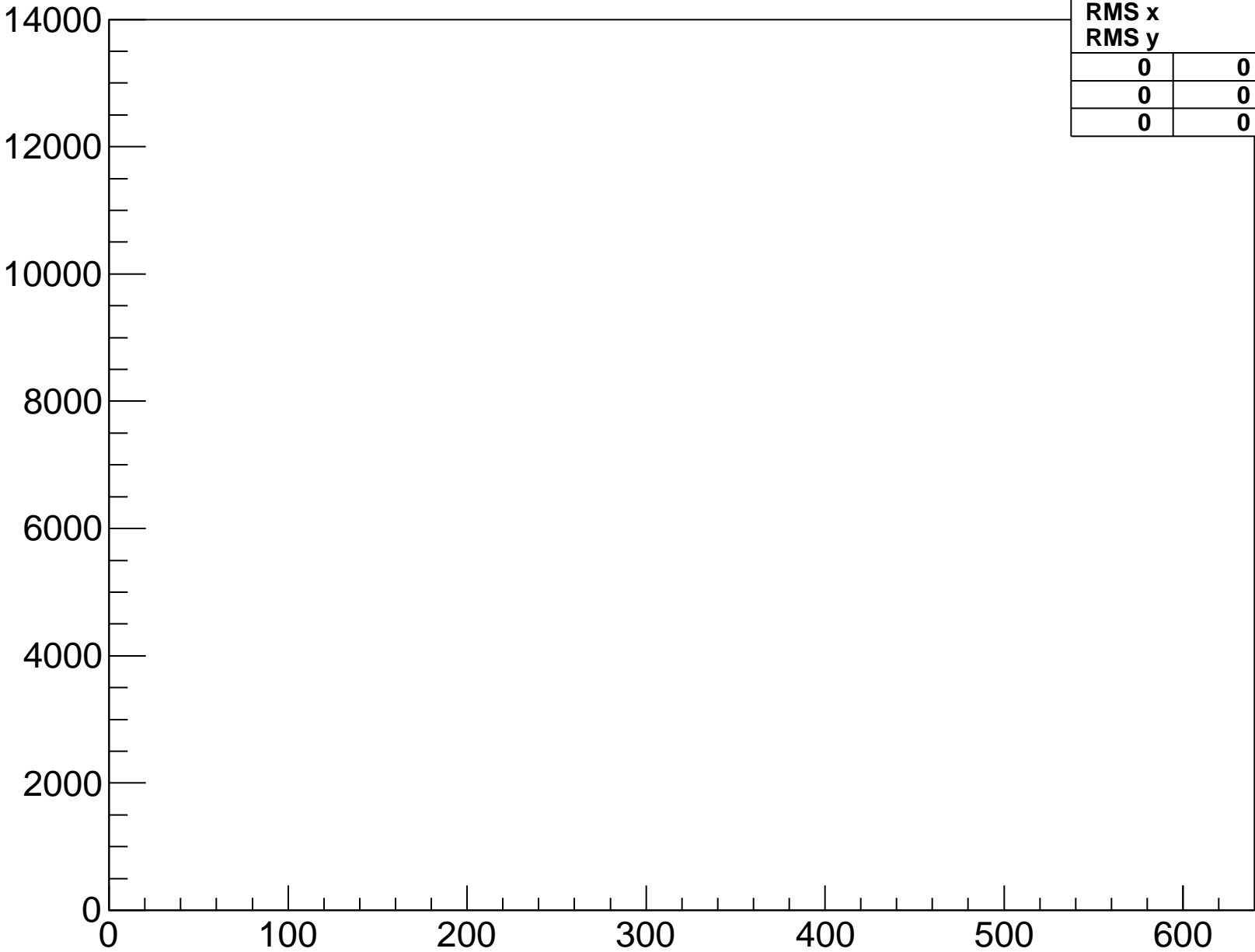
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-7-hyb-0-sample-5

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



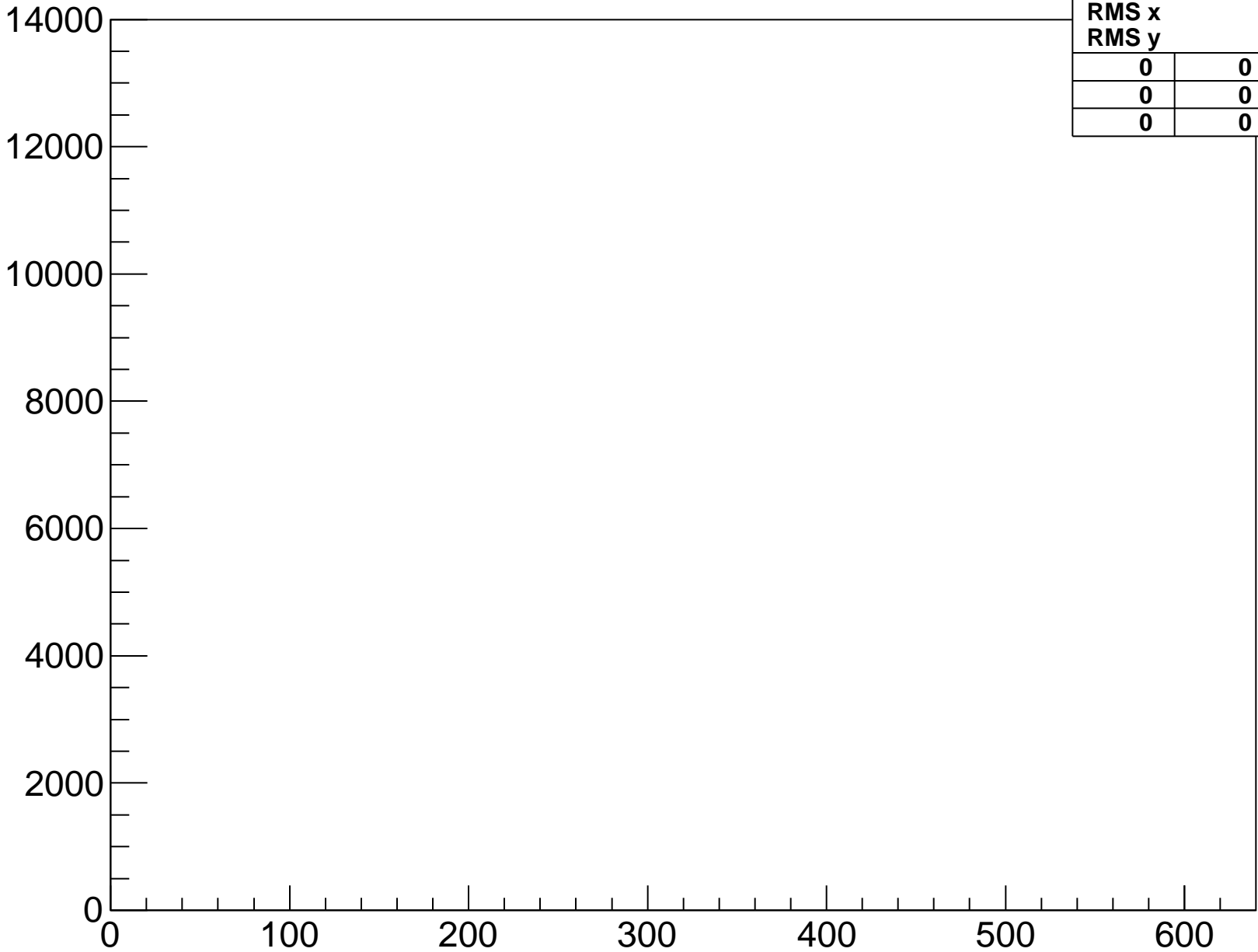
baselinesamples-fpga-7-hyb-1-sample-0



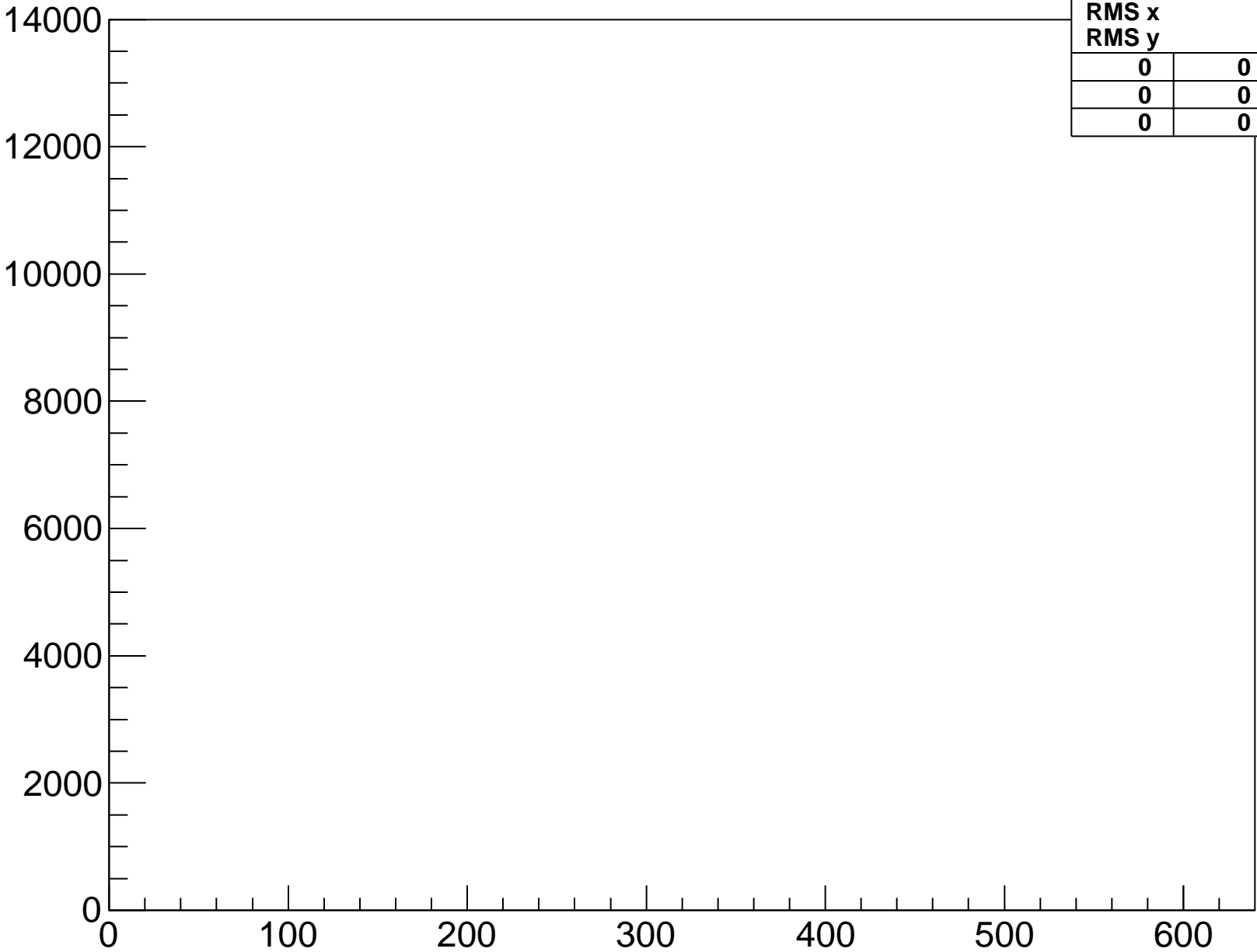
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-7-hyb-1-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

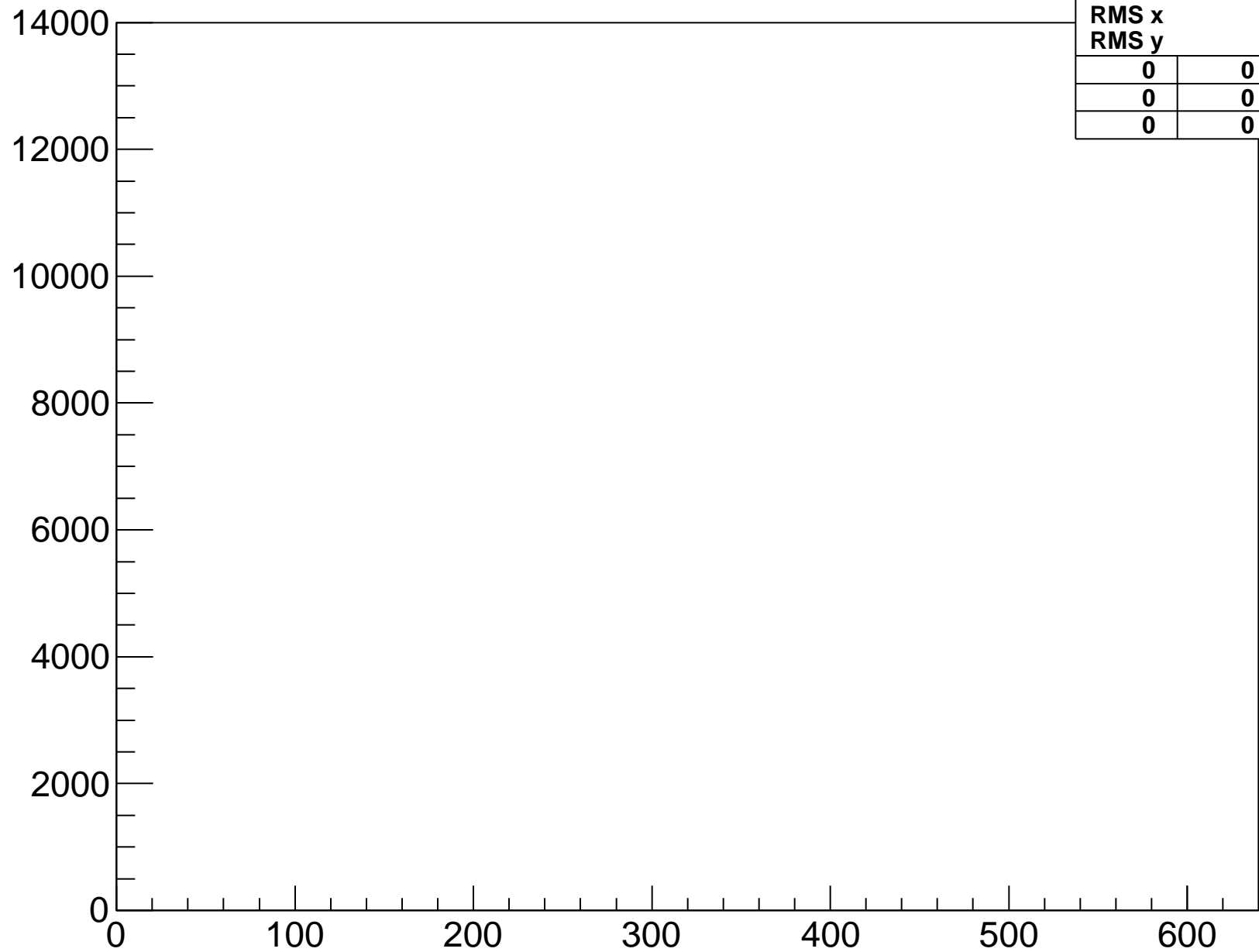


baselinesamples-fpga-7-hyb-1-sample-2



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

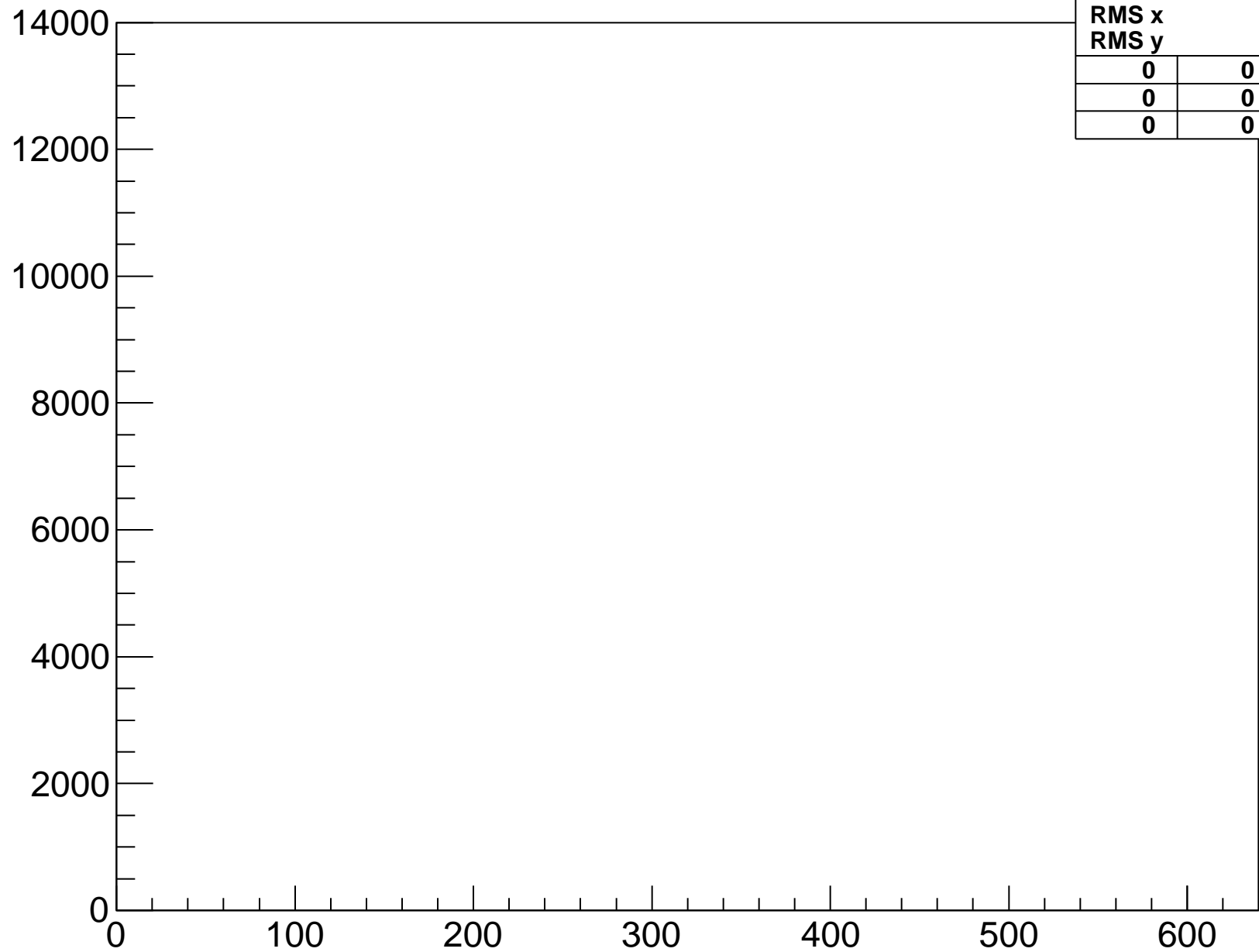
baselinesamples-fpga-7-hyb-1-sample-3



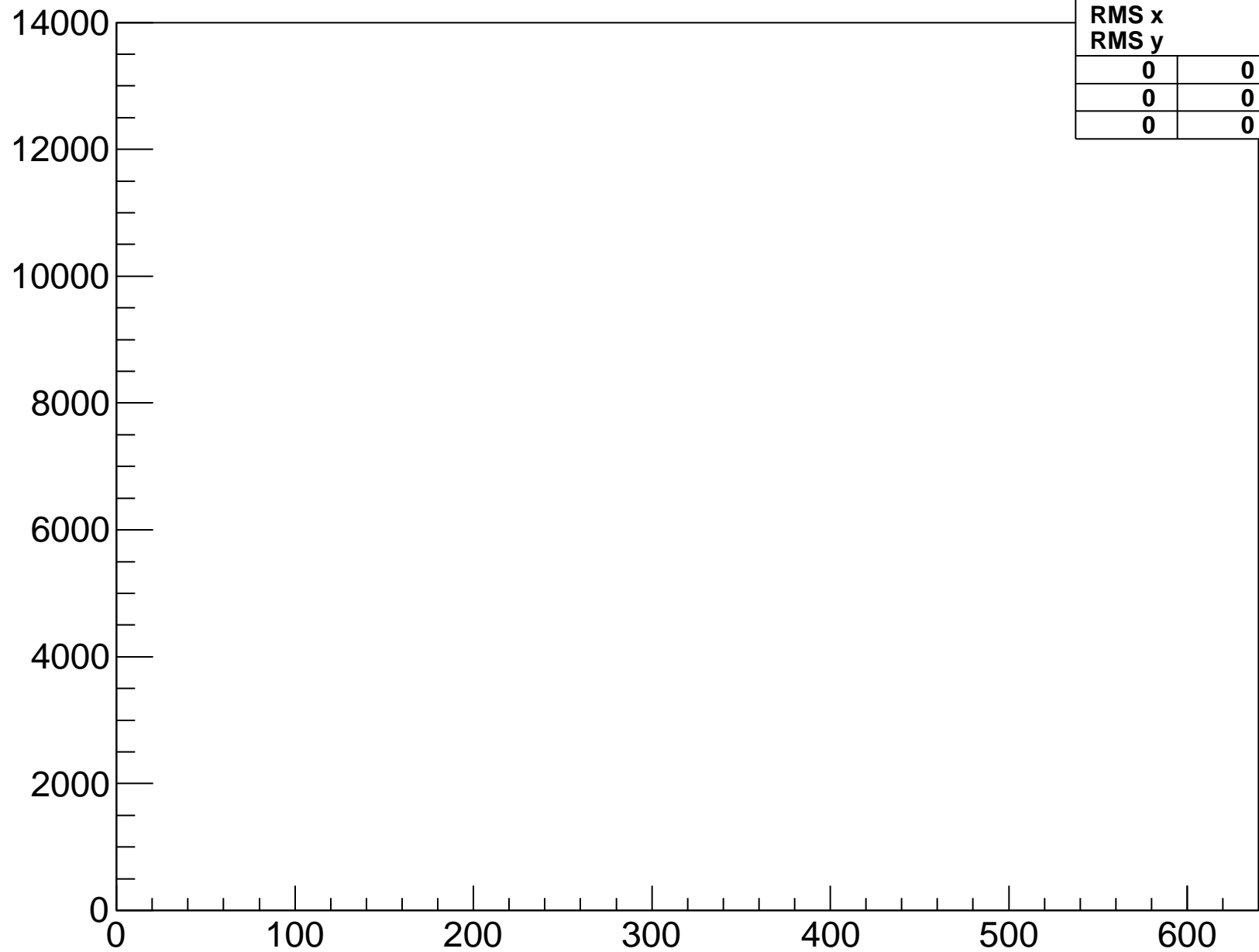
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-7-hyb-1-sample-4

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

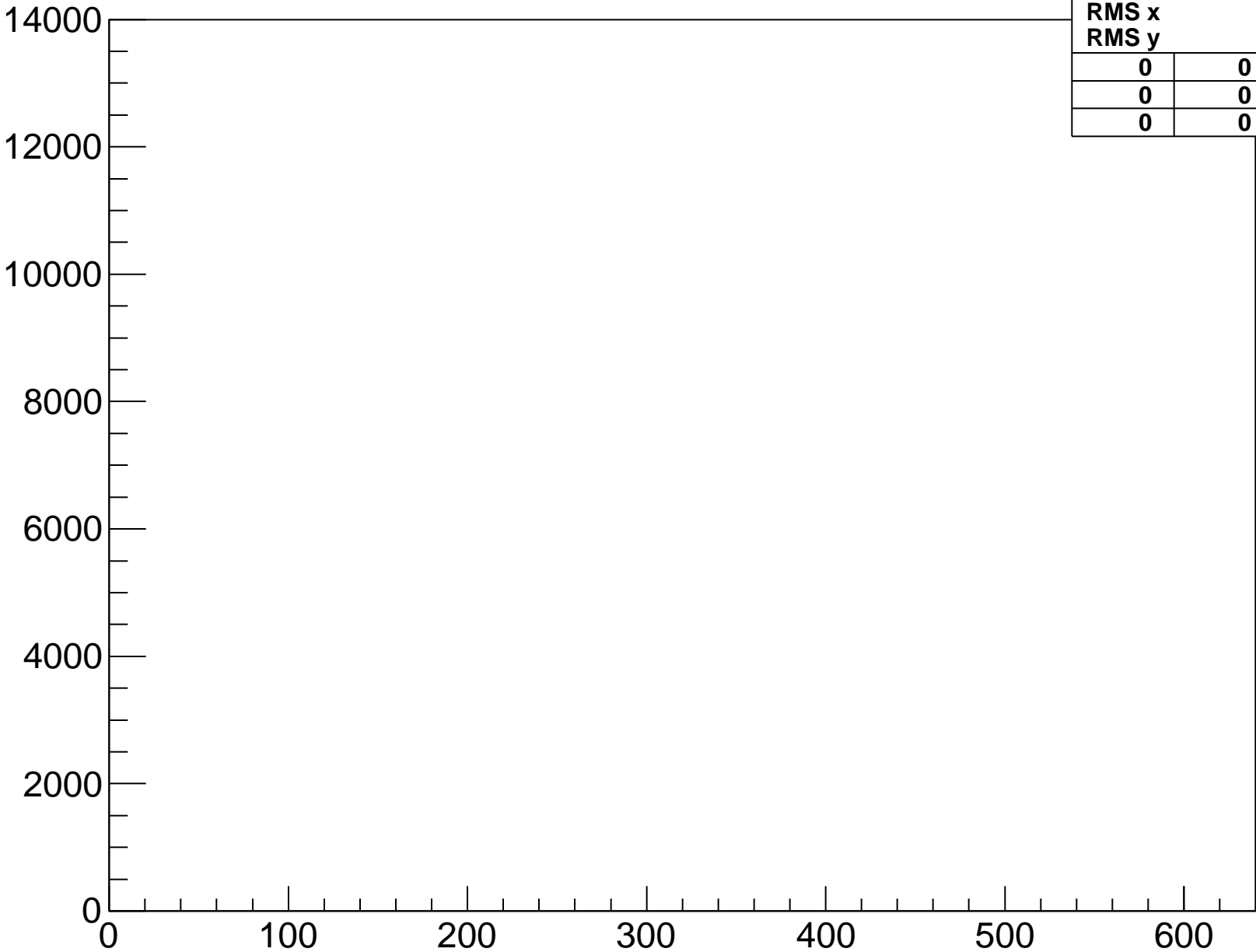


baselinesamples-fpga-7-hyb-1-sample-5



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

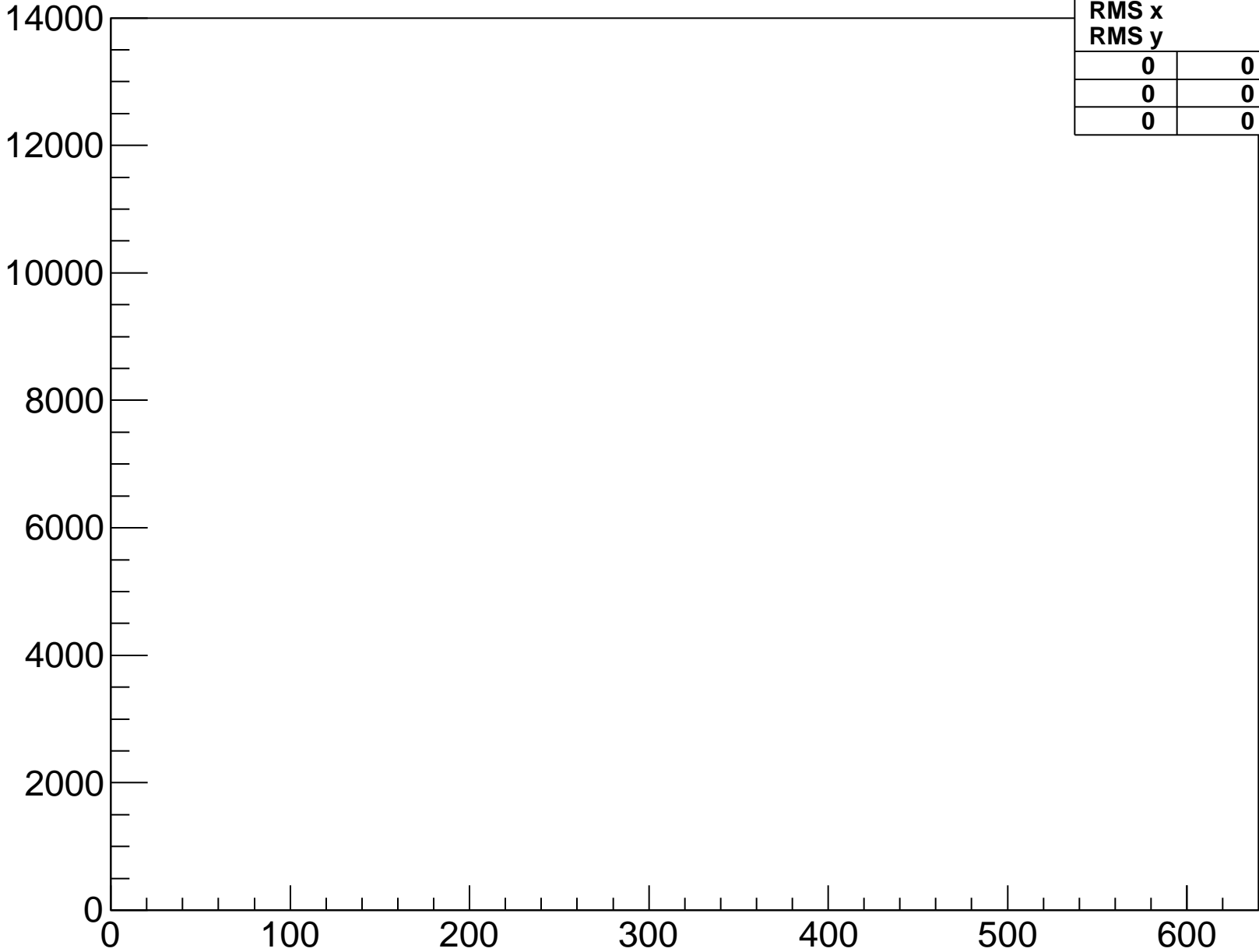
baselinesamples-fpga-7-hyb-2-sample-0



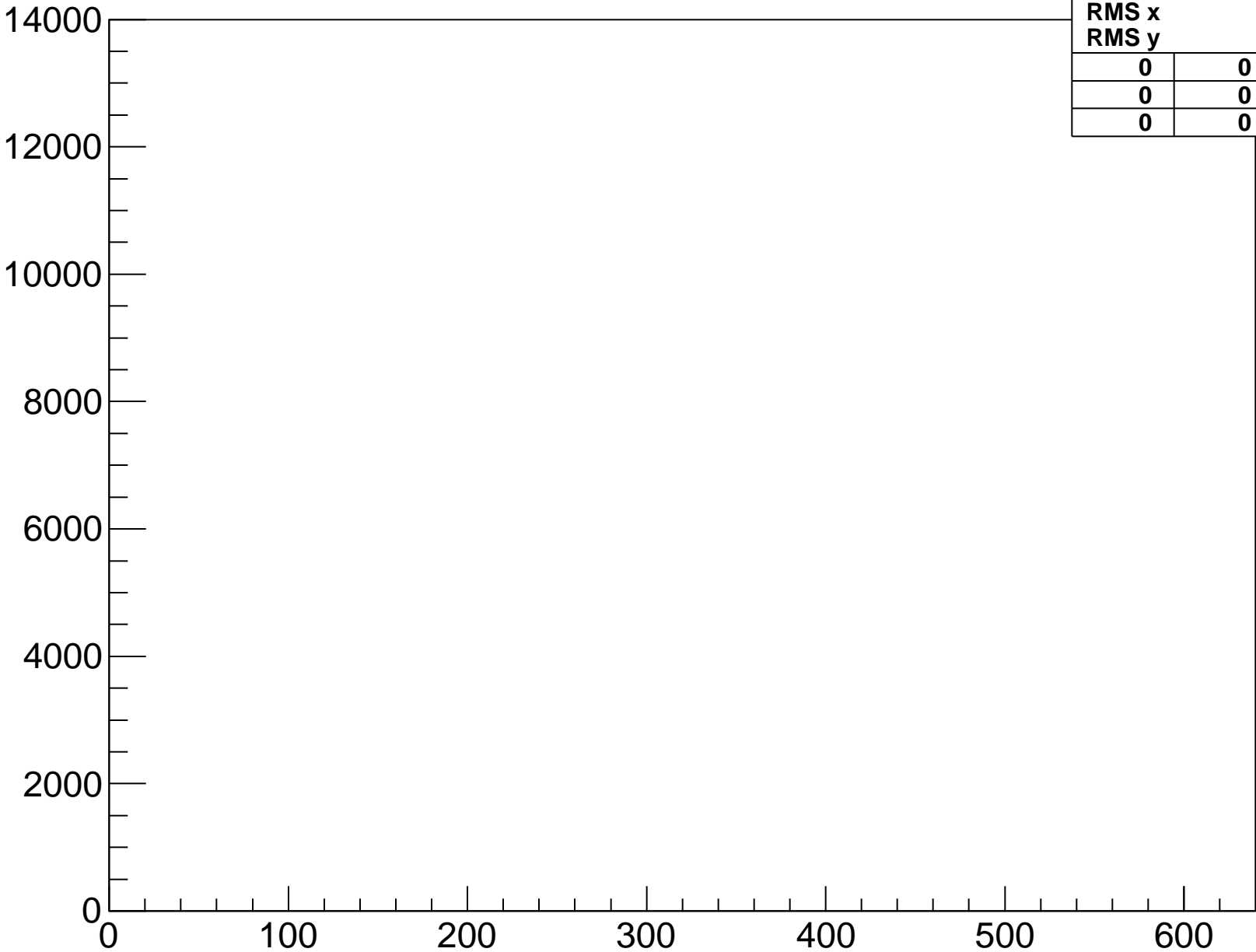
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-7-hyb-2-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

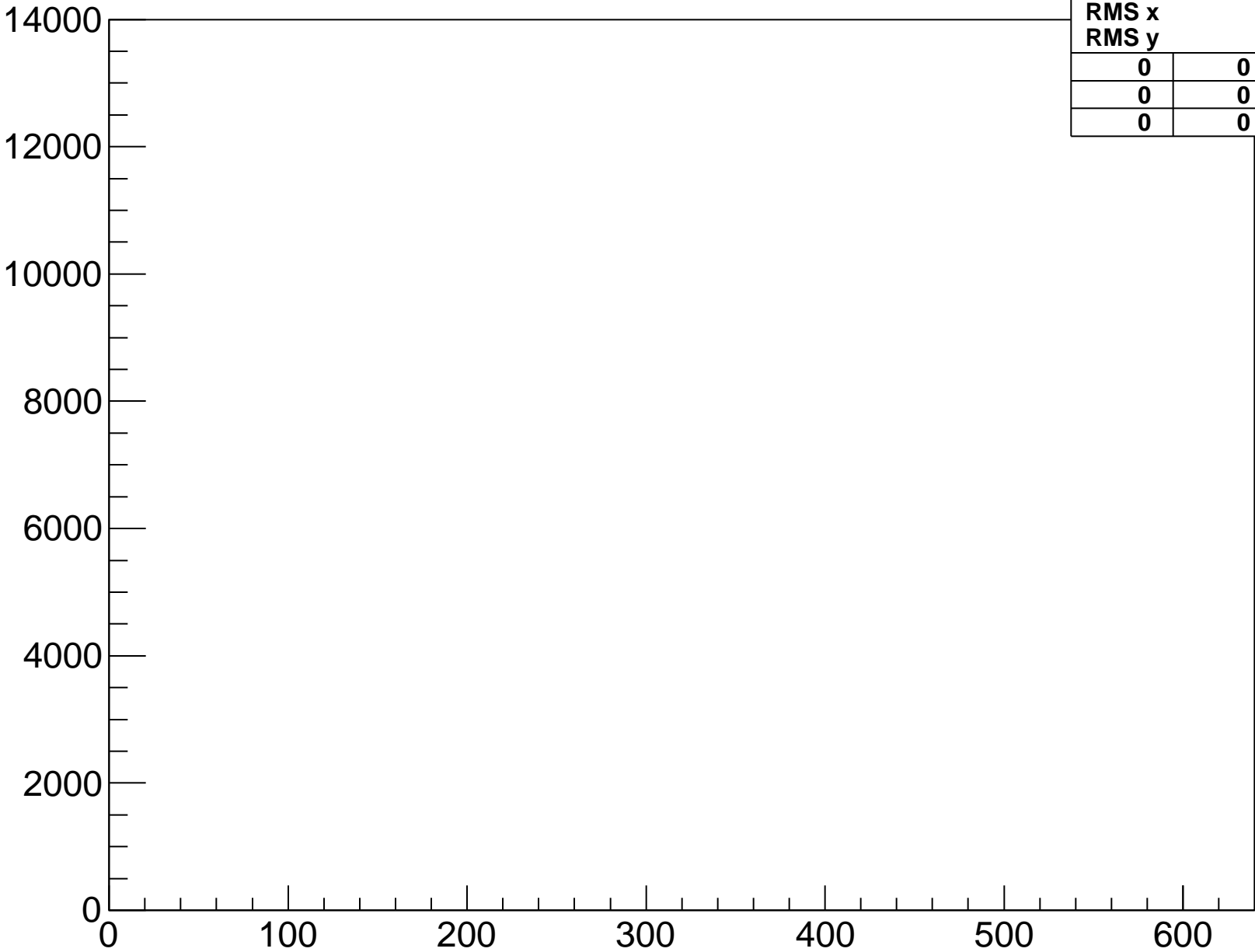


baselinesamples-fpga-7-hyb-2-sample-2



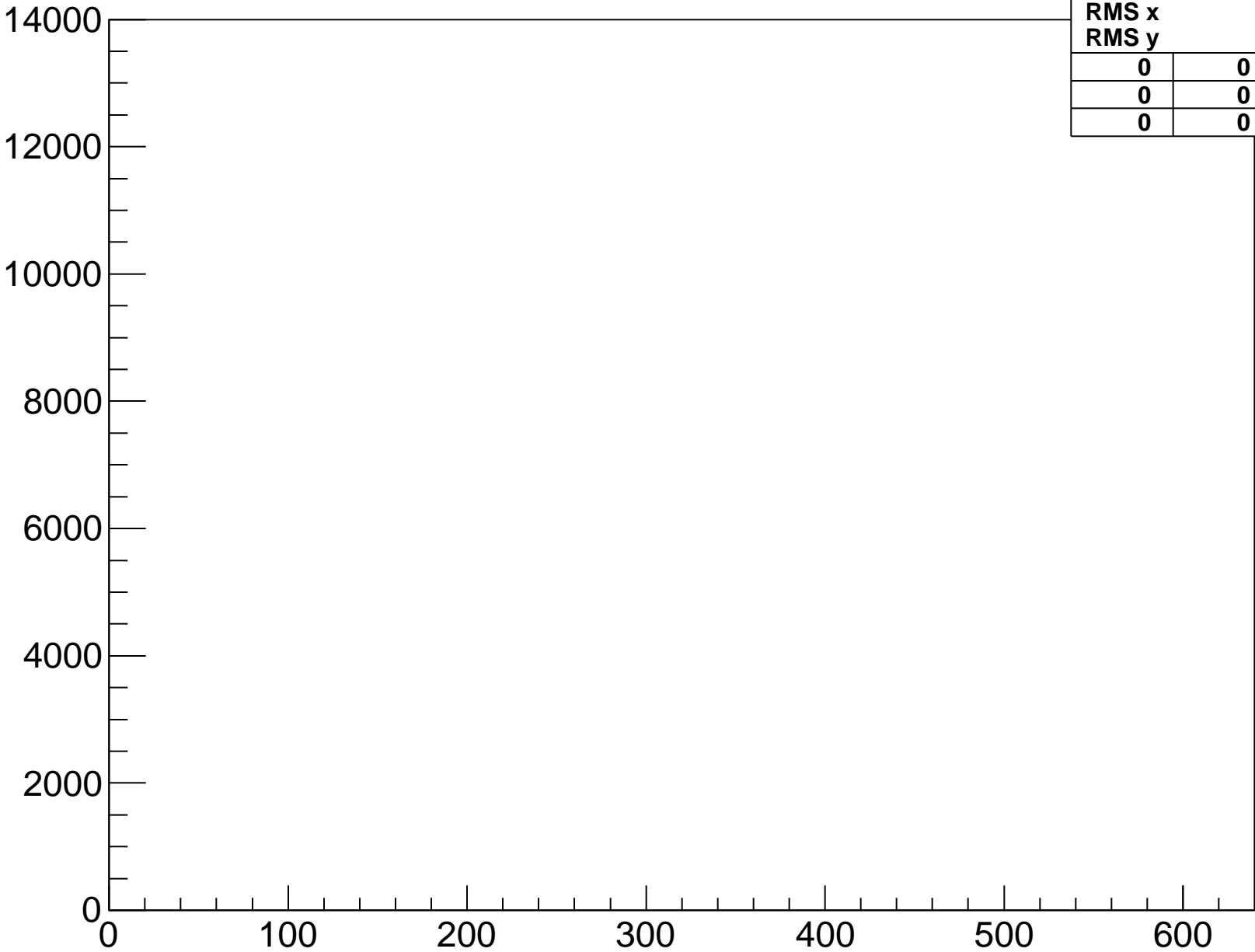
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-7-hyb-2-sample-3



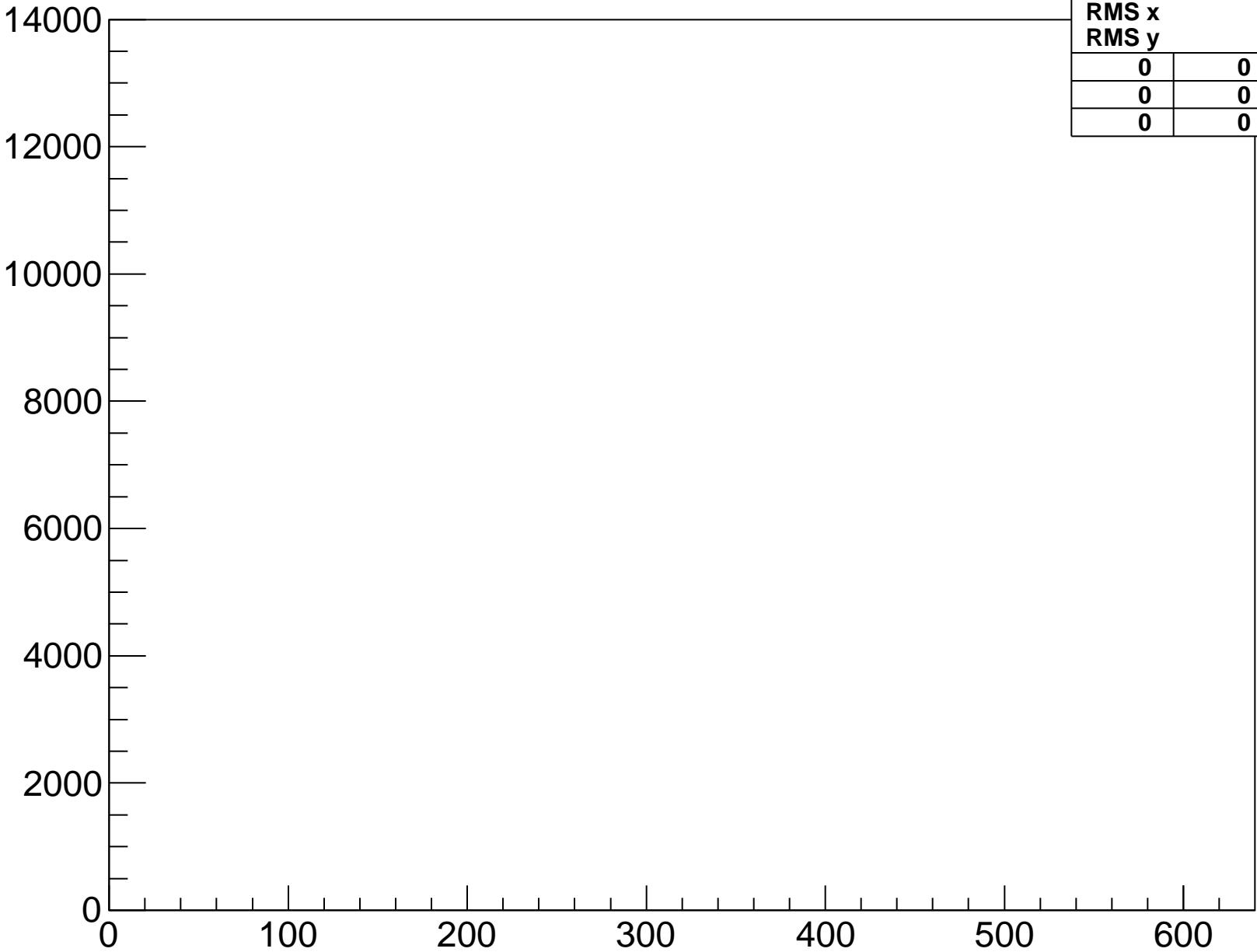
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-7-hyb-2-sample-4



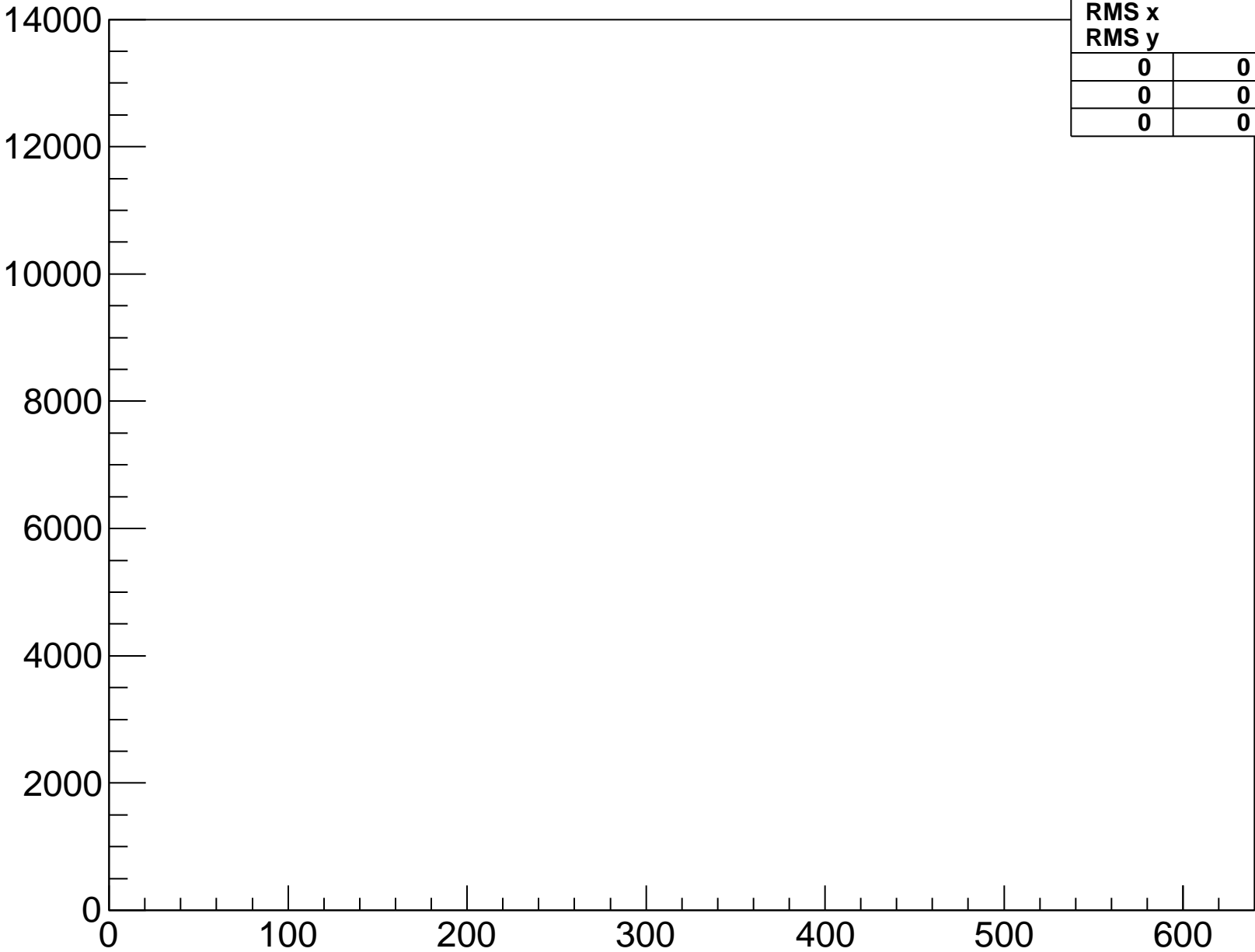
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-7-hyb-2-sample-5



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

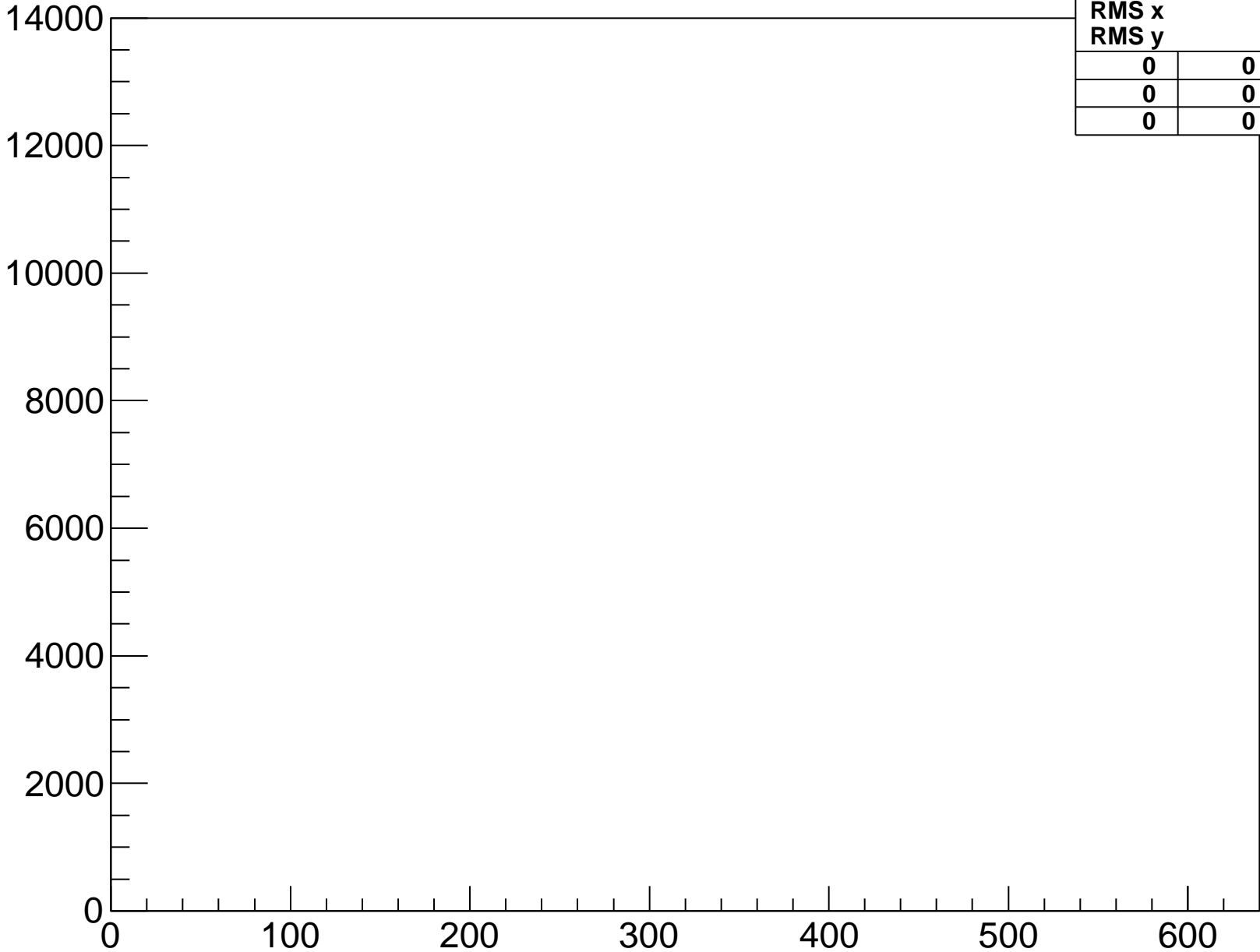
baselinesamples-fpga-7-hyb-3-sample-0



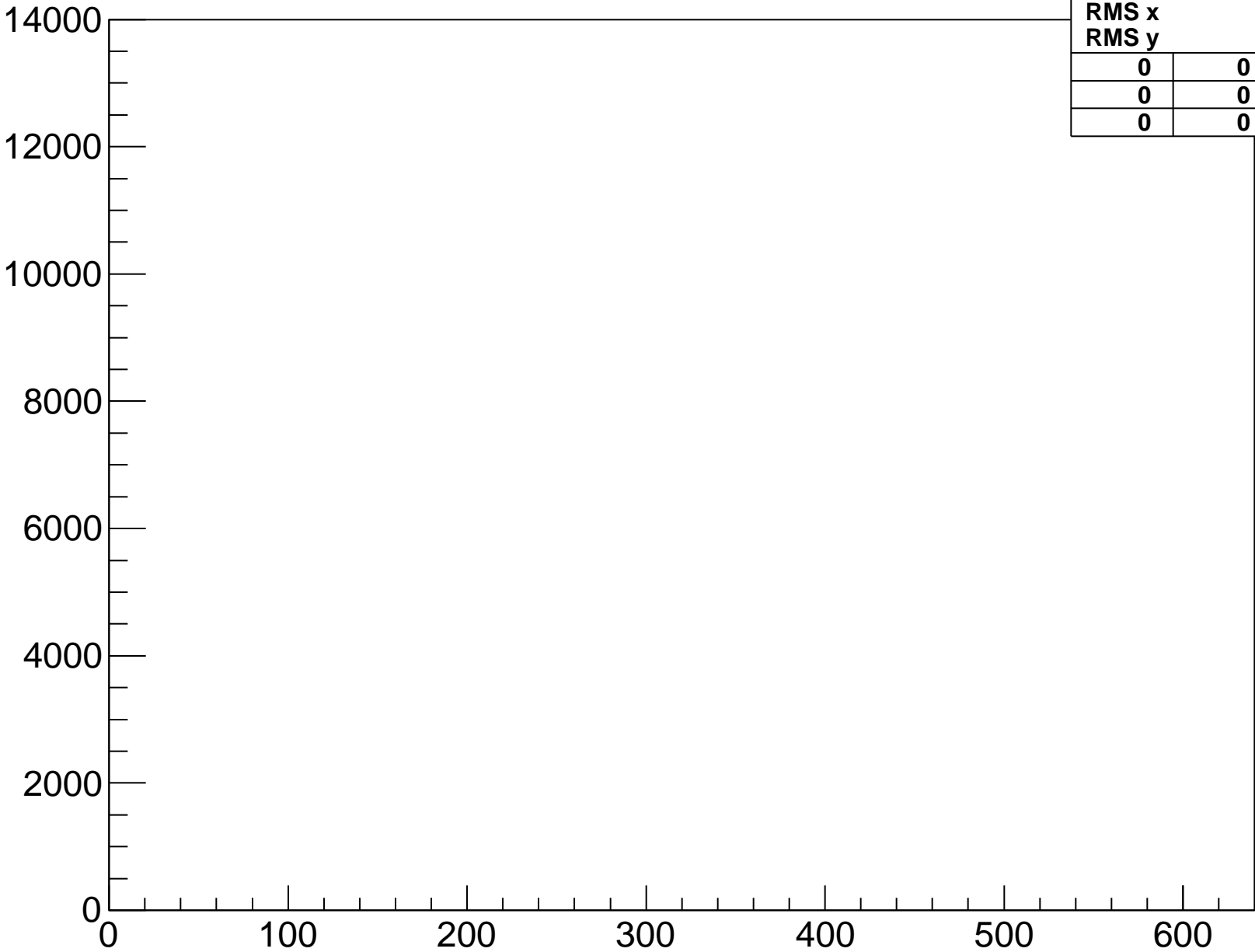
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-7-hyb-3-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

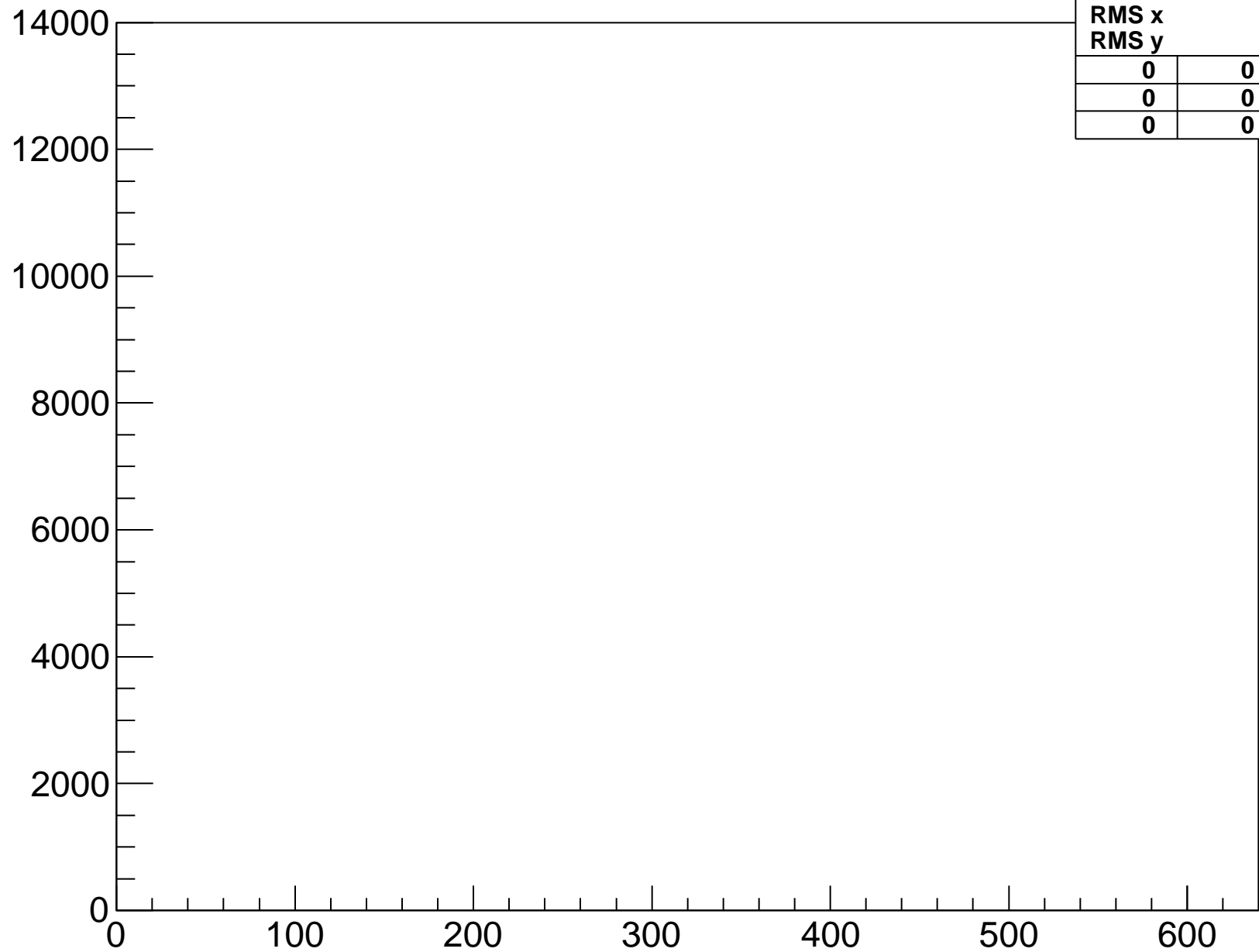


baselinesamples-fpga-7-hyb-3-sample-2



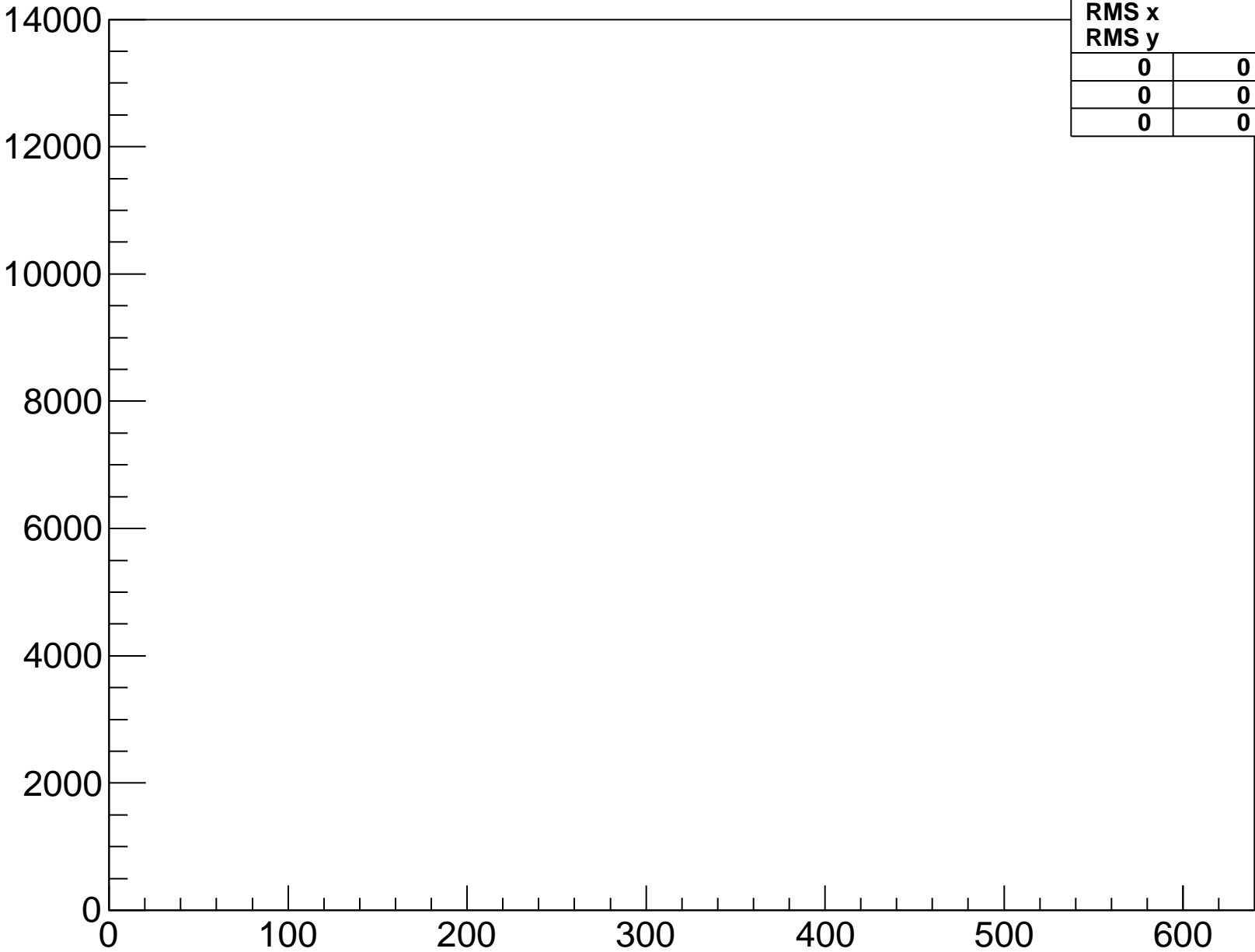
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-7-hyb-3-sample-3



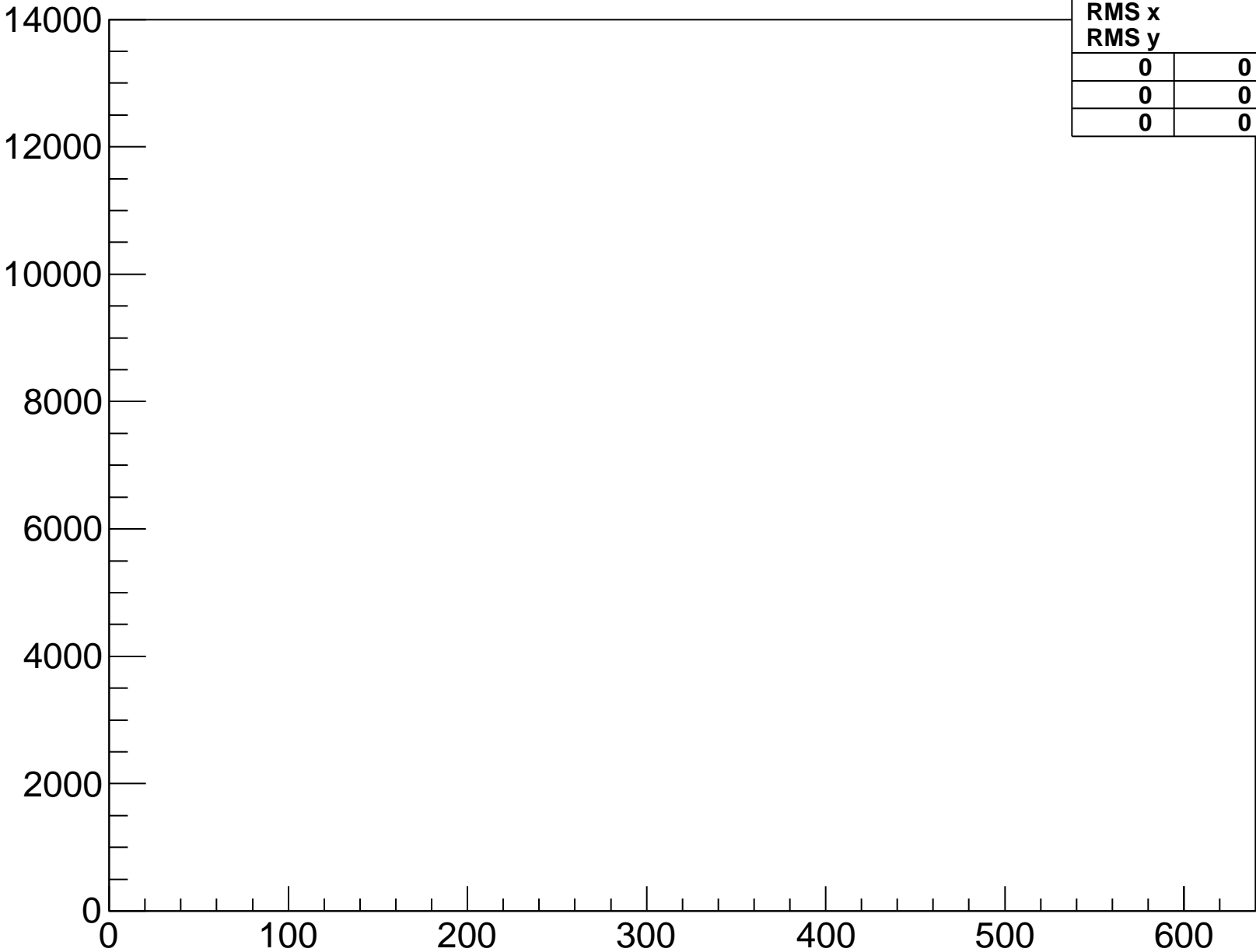
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-7-hyb-3-sample-4



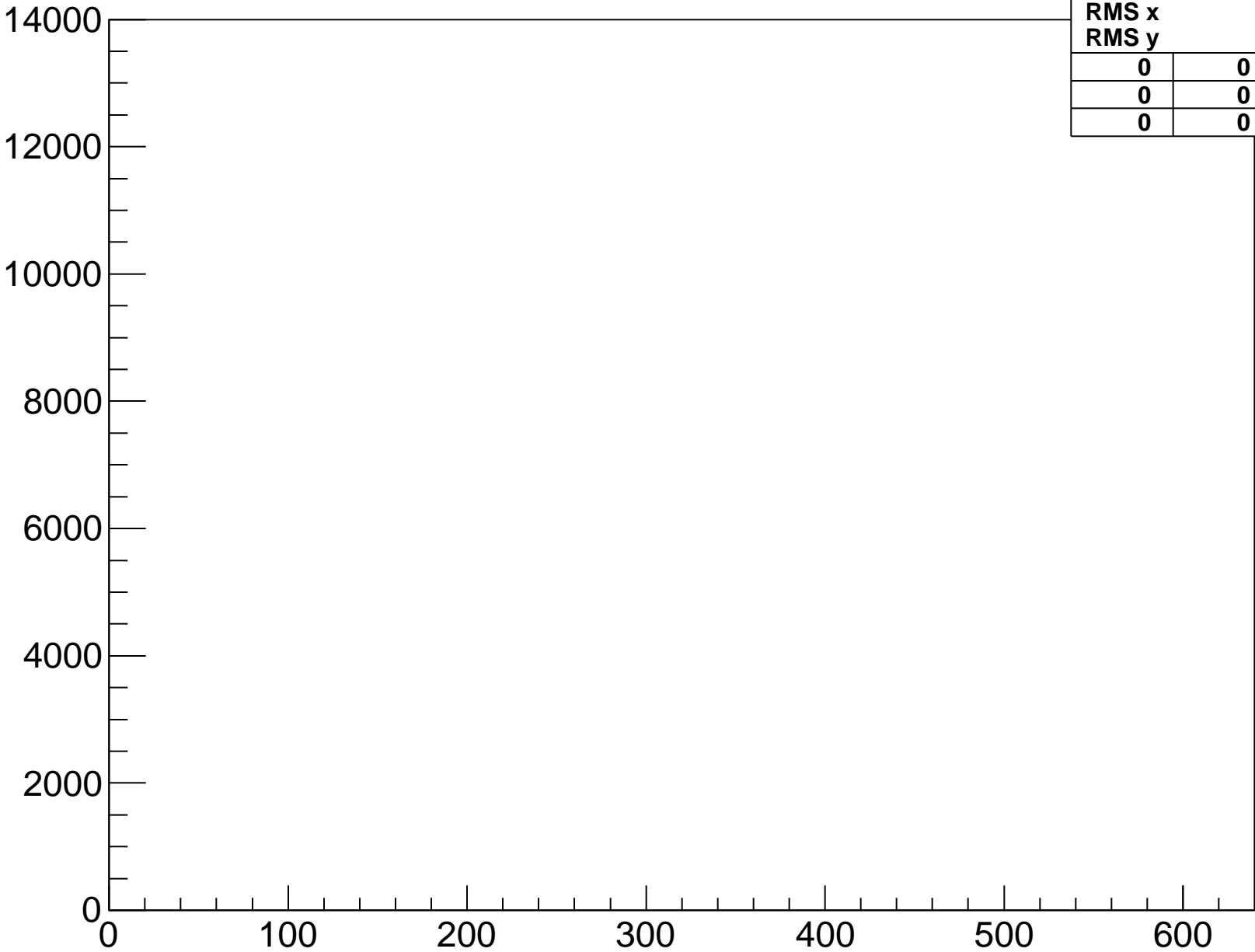
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-7-hyb-3-sample-5



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

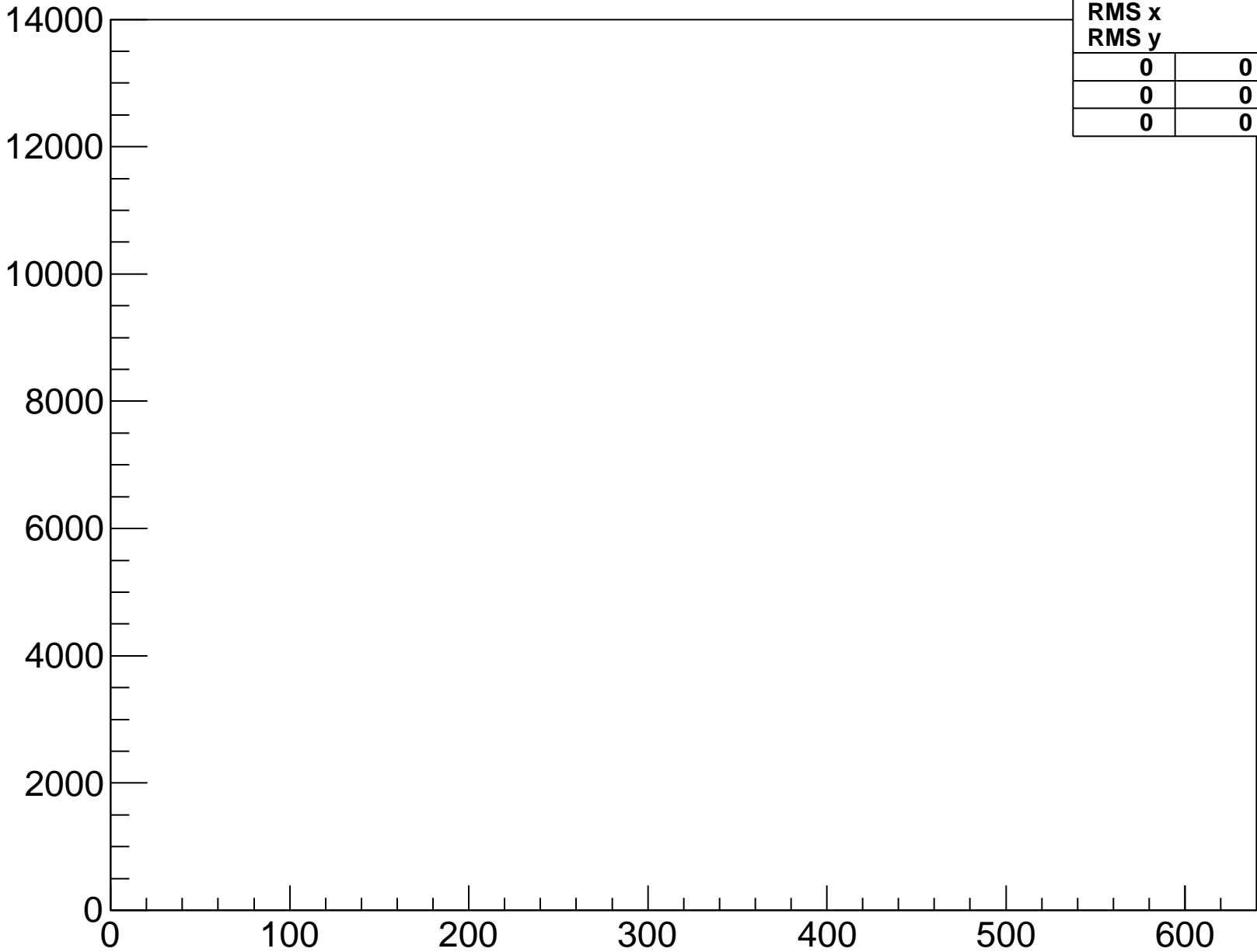
baselinesamples-fpga-8-hyb-0-sample-0



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

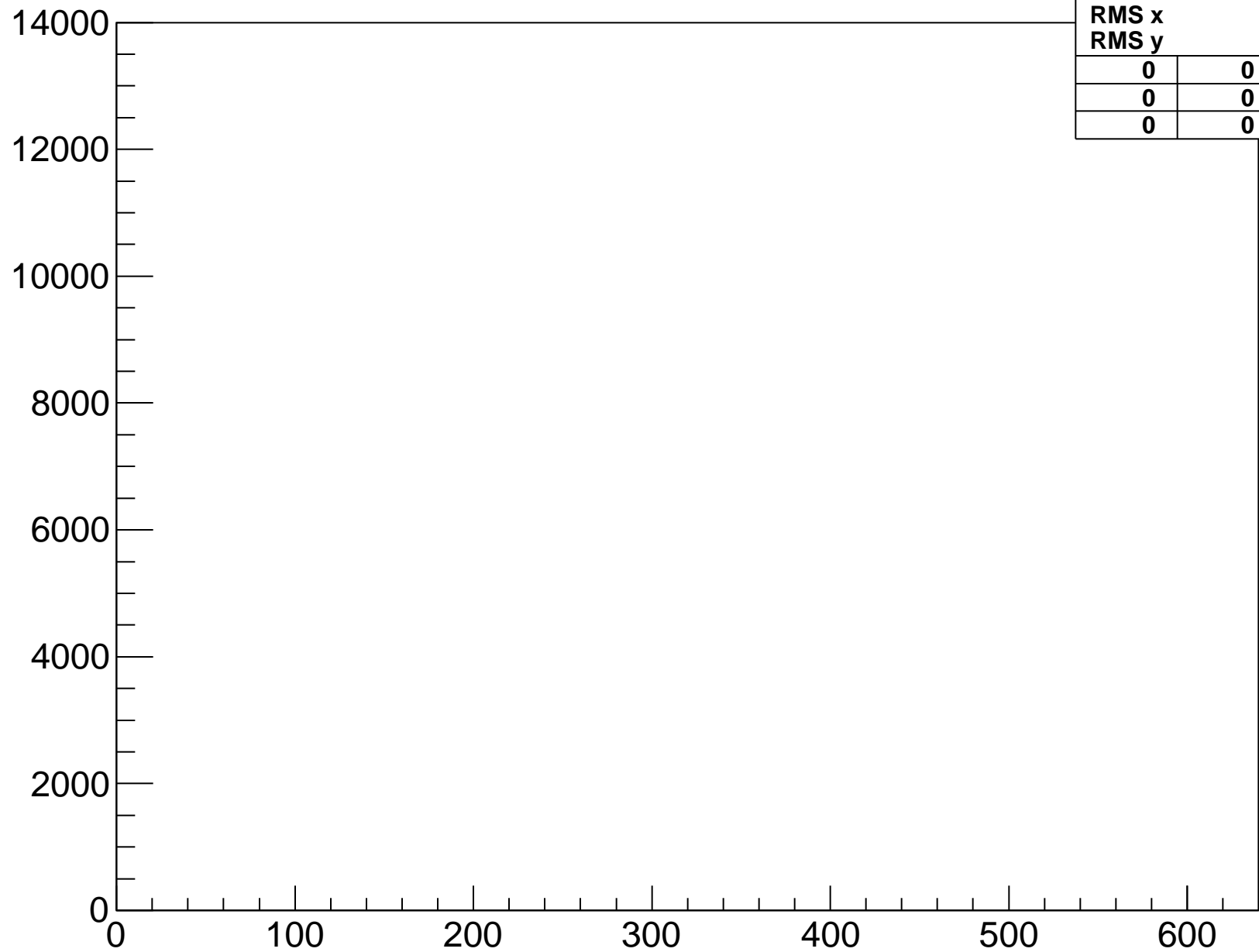
baselinesamples-fpga-8-hyb-0-sample-1

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

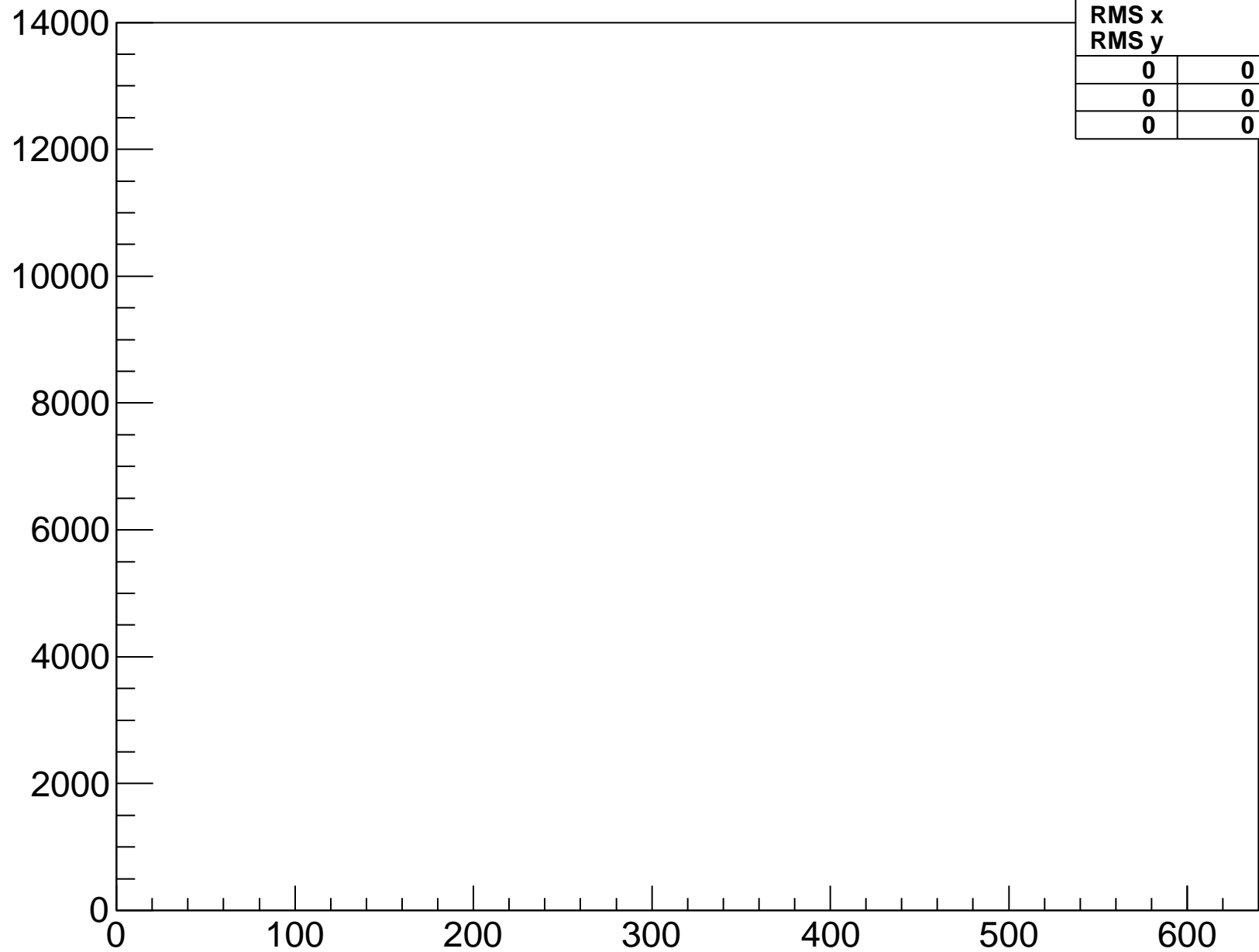


baselinesamples-fpga-8-hyb-0-sample-2

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

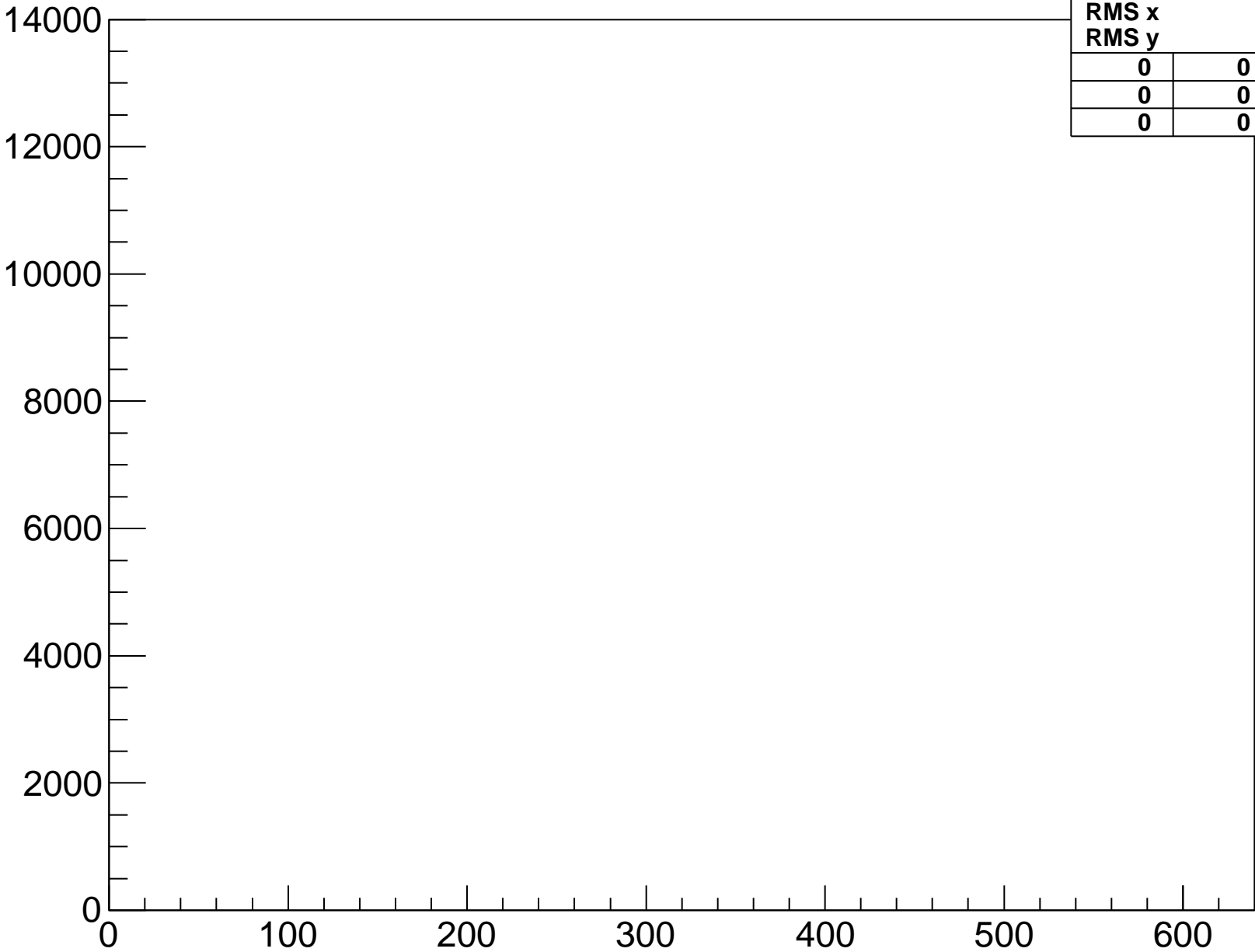


baselinesamples-fpga-8-hyb-0-sample-3



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

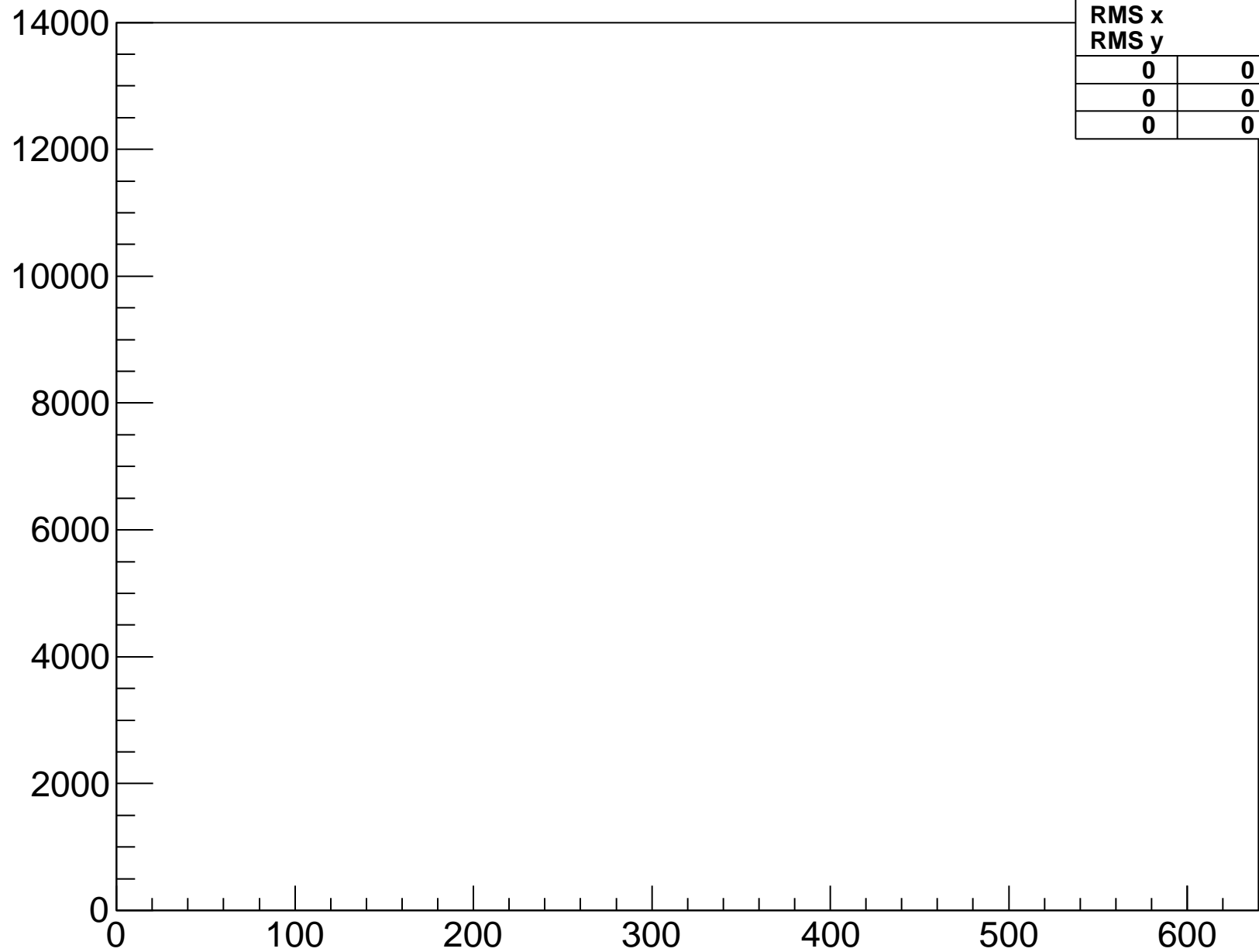
baselinesamples-fpga-8-hyb-0-sample-4



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

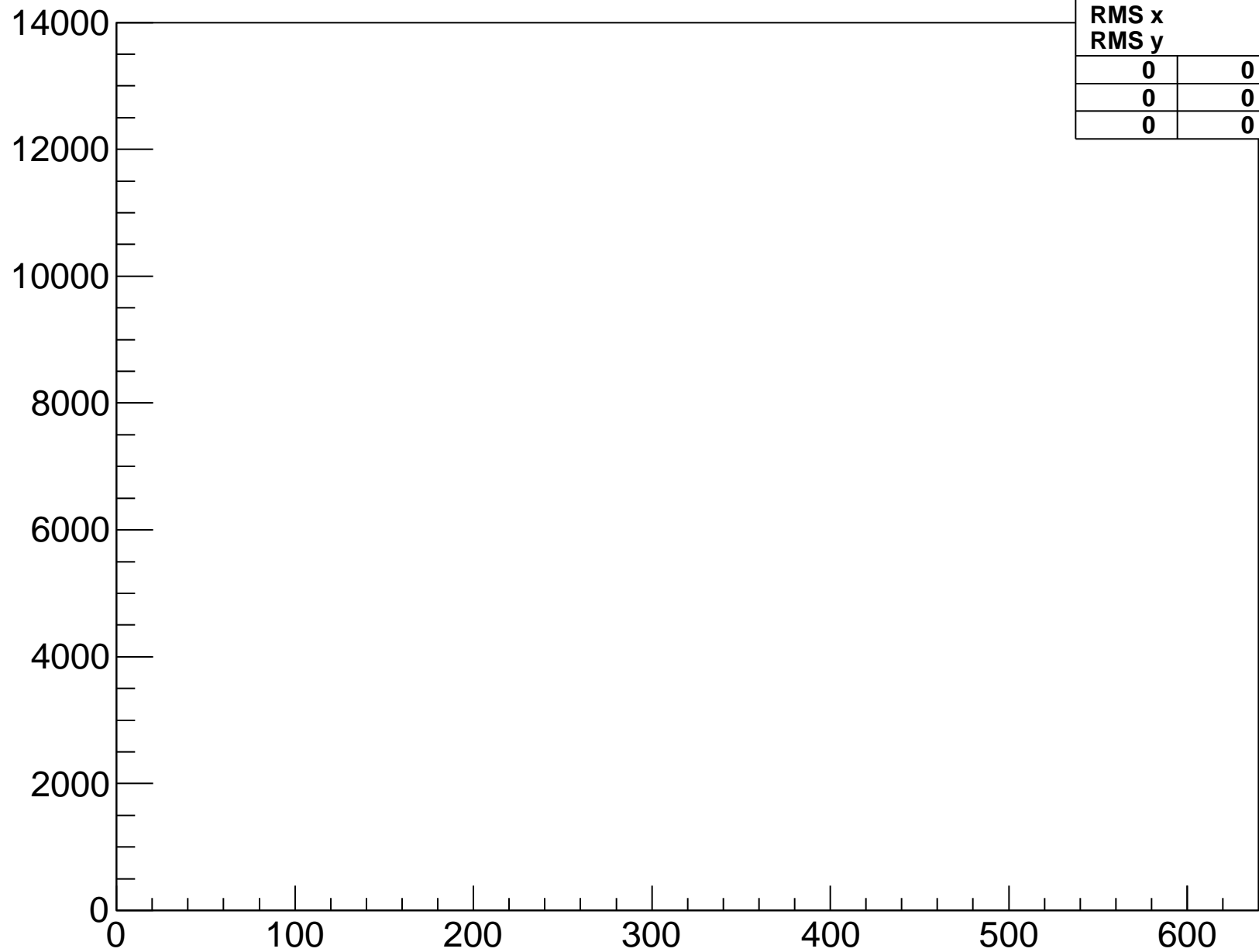
baselinesamples-fpga-8-hyb-0-sample-5

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



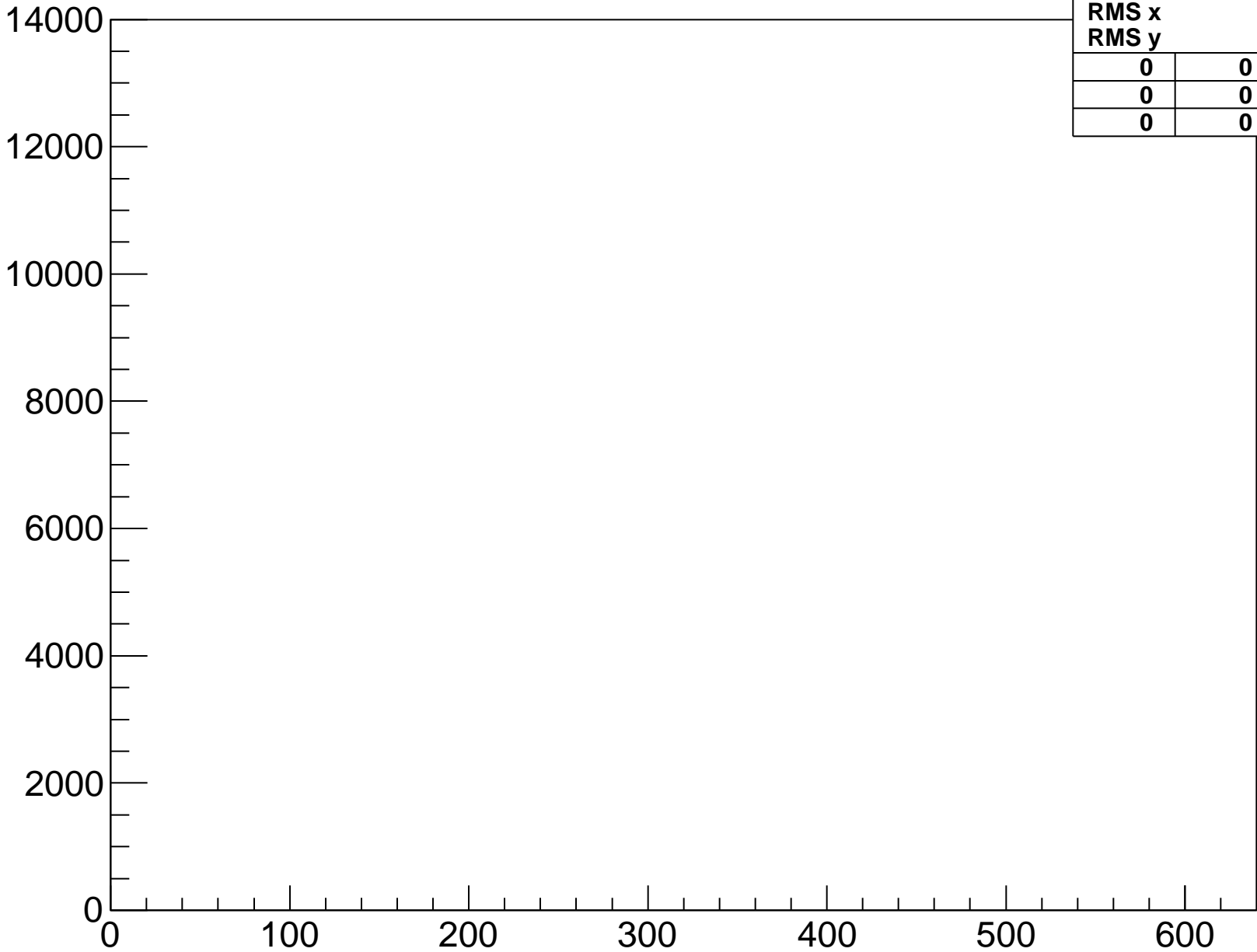
baselinesamples-fpga-8-hyb-1-sample-0

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

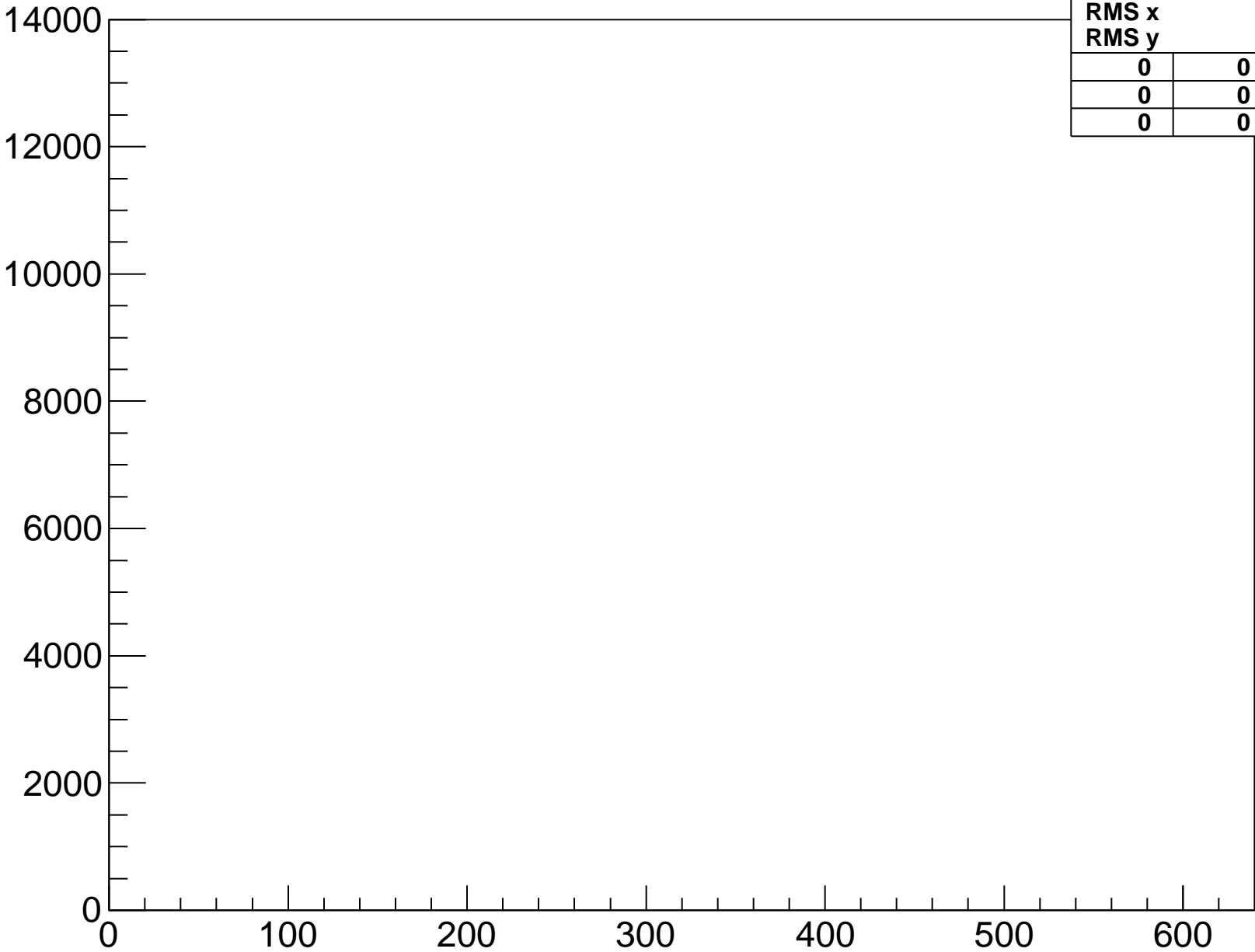


baselinesamples-fpga-8-hyb-1-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

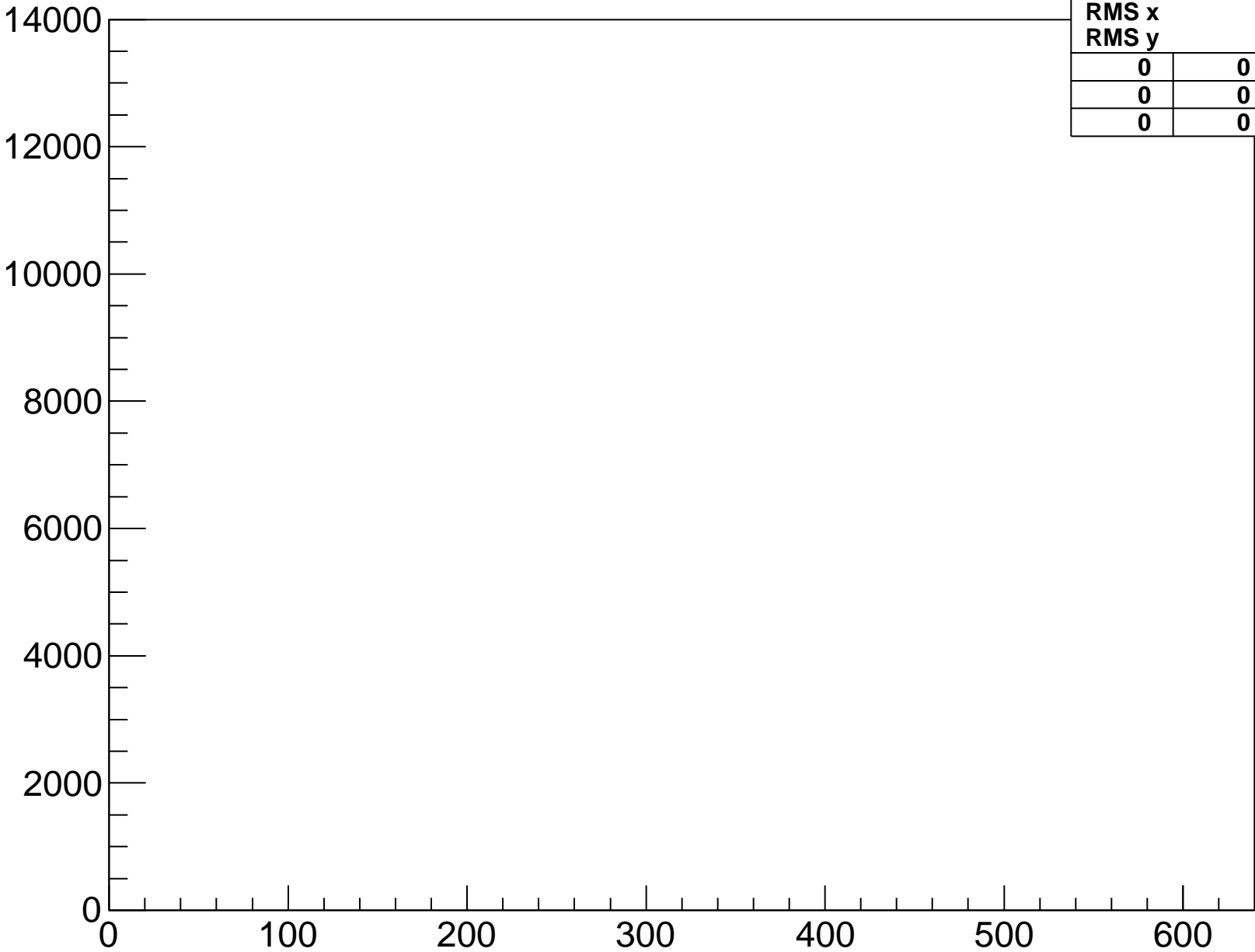


baselinesamples-fpga-8-hyb-1-sample-2



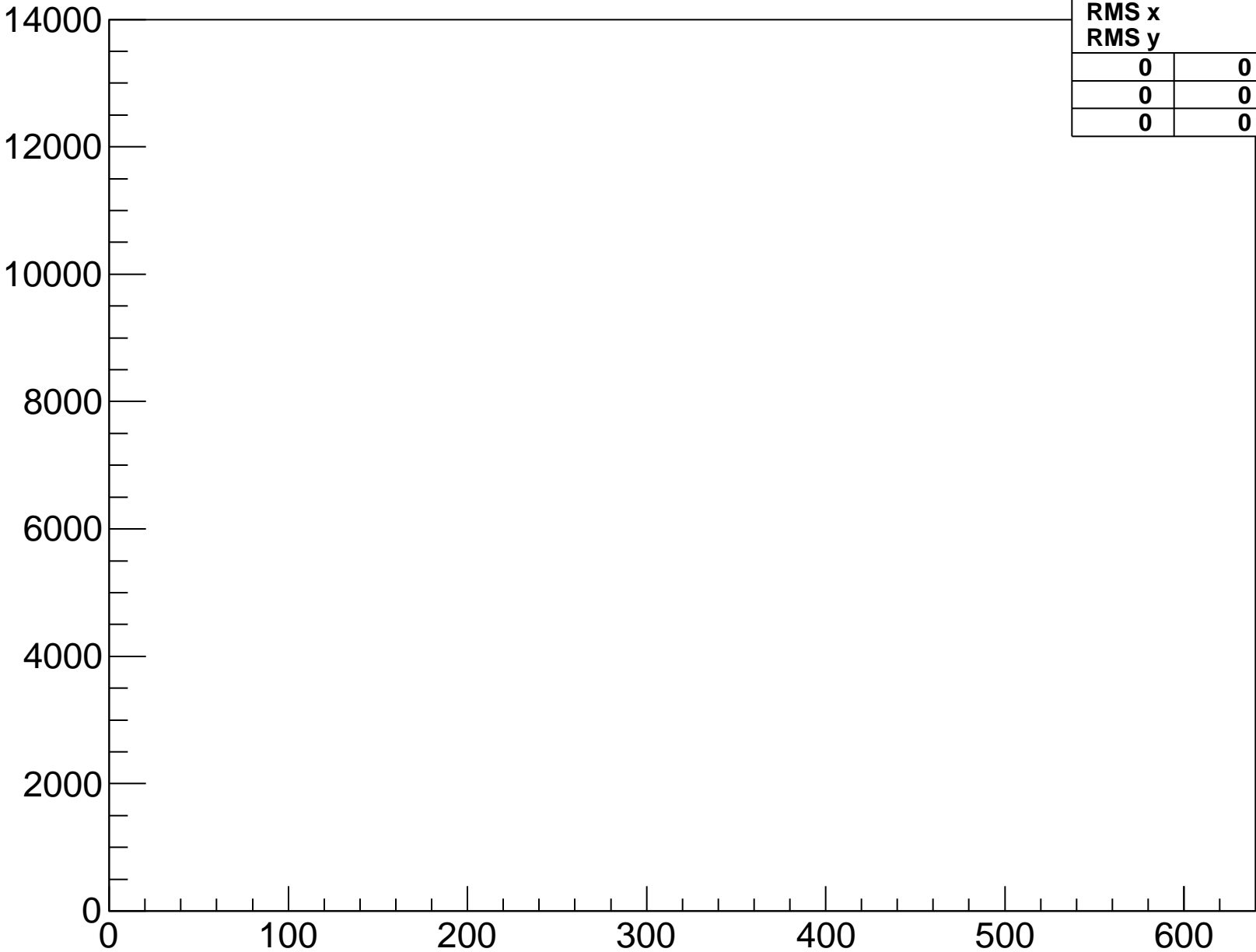
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-8-hyb-1-sample-3



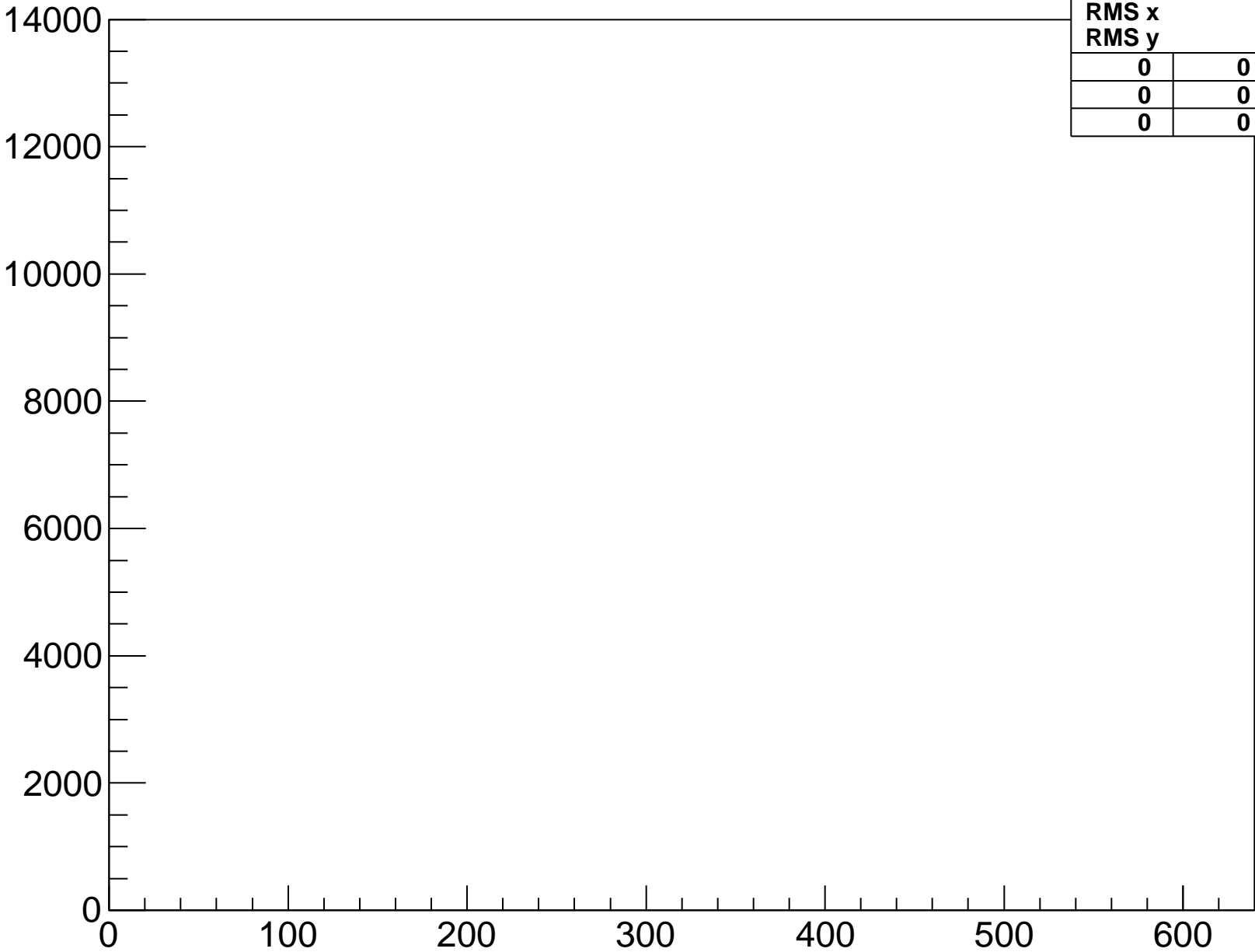
Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-8-hyb-1-sample-4



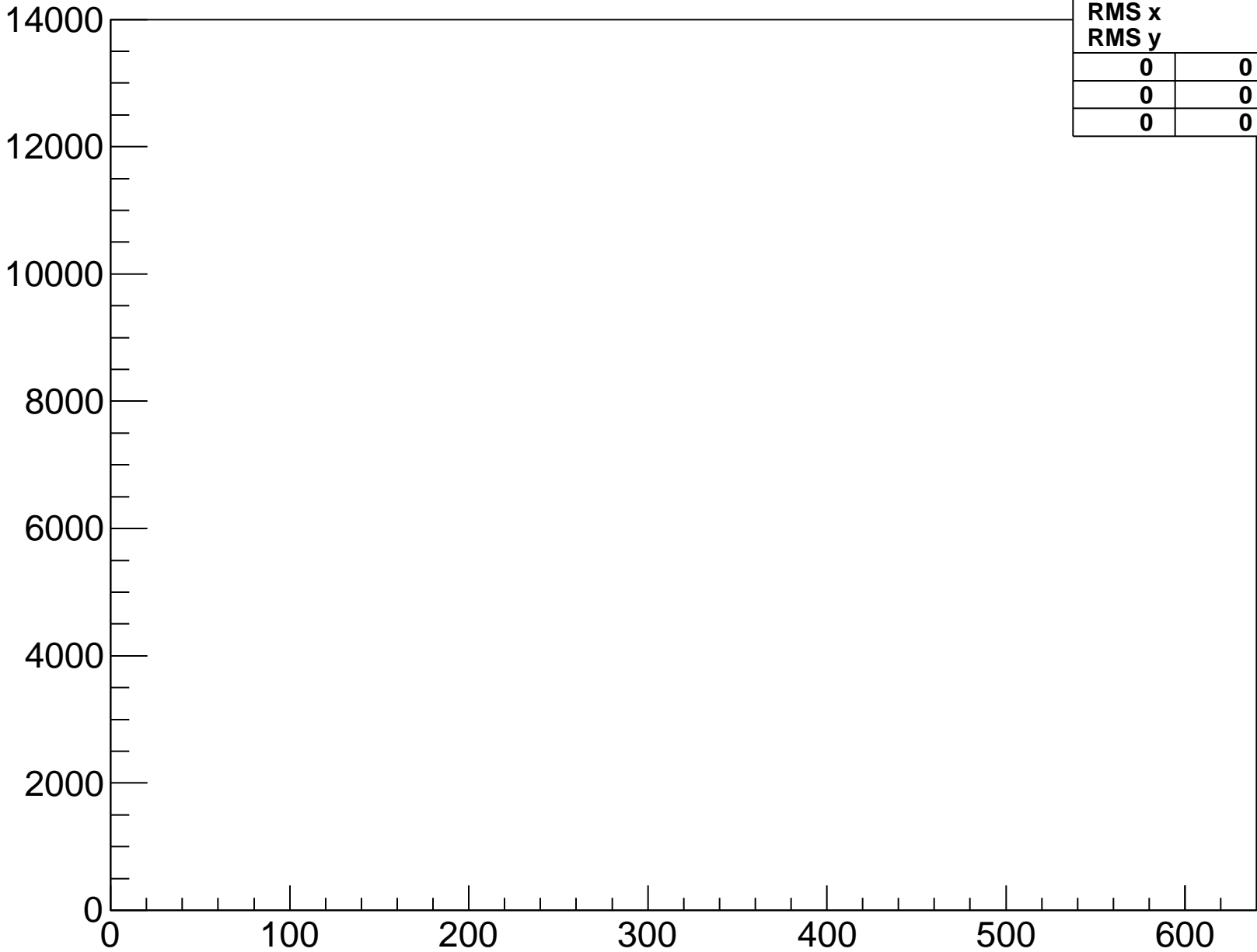
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-8-hyb-1-sample-5



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

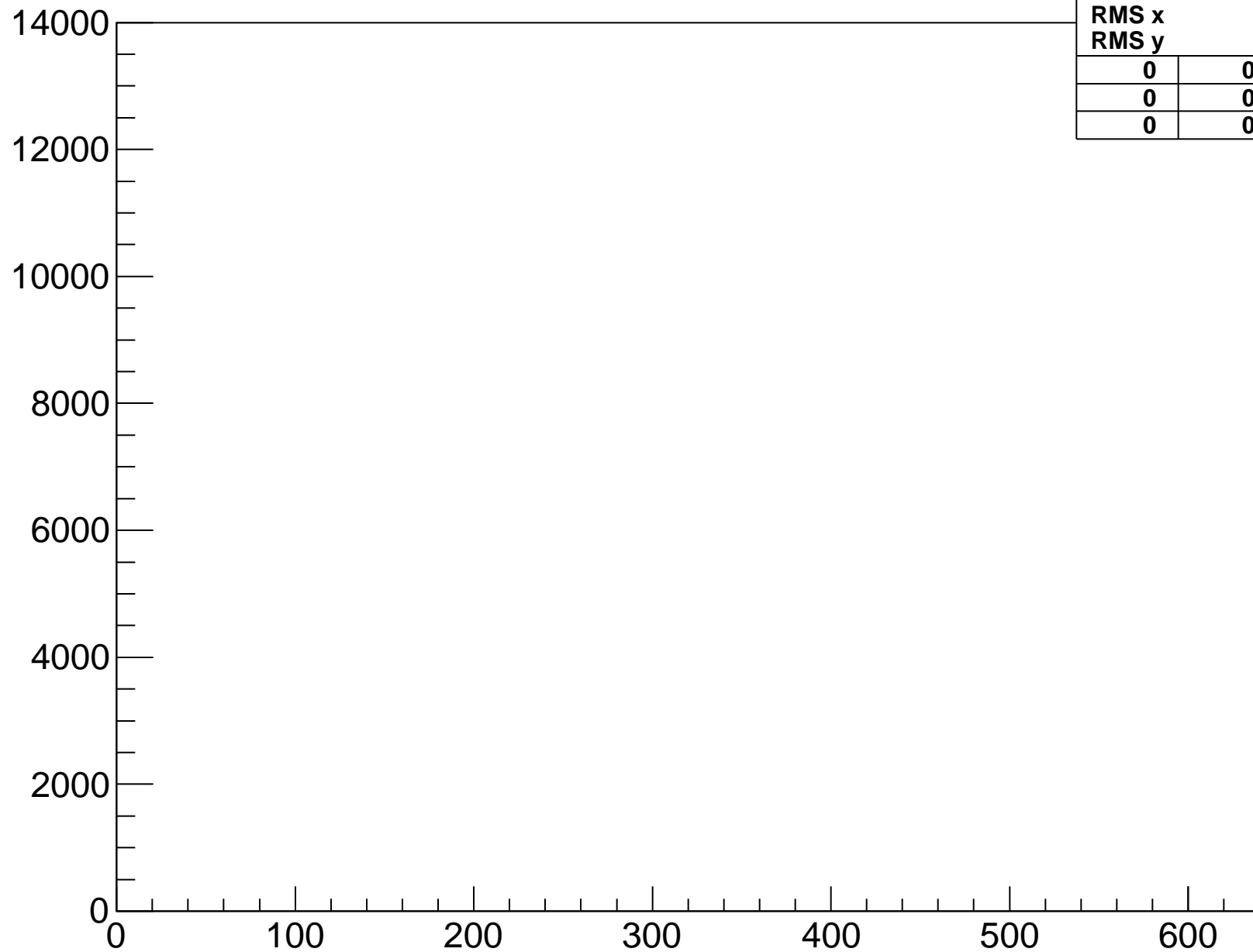
baselinesamples-fpga-8-hyb-2-sample-0



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

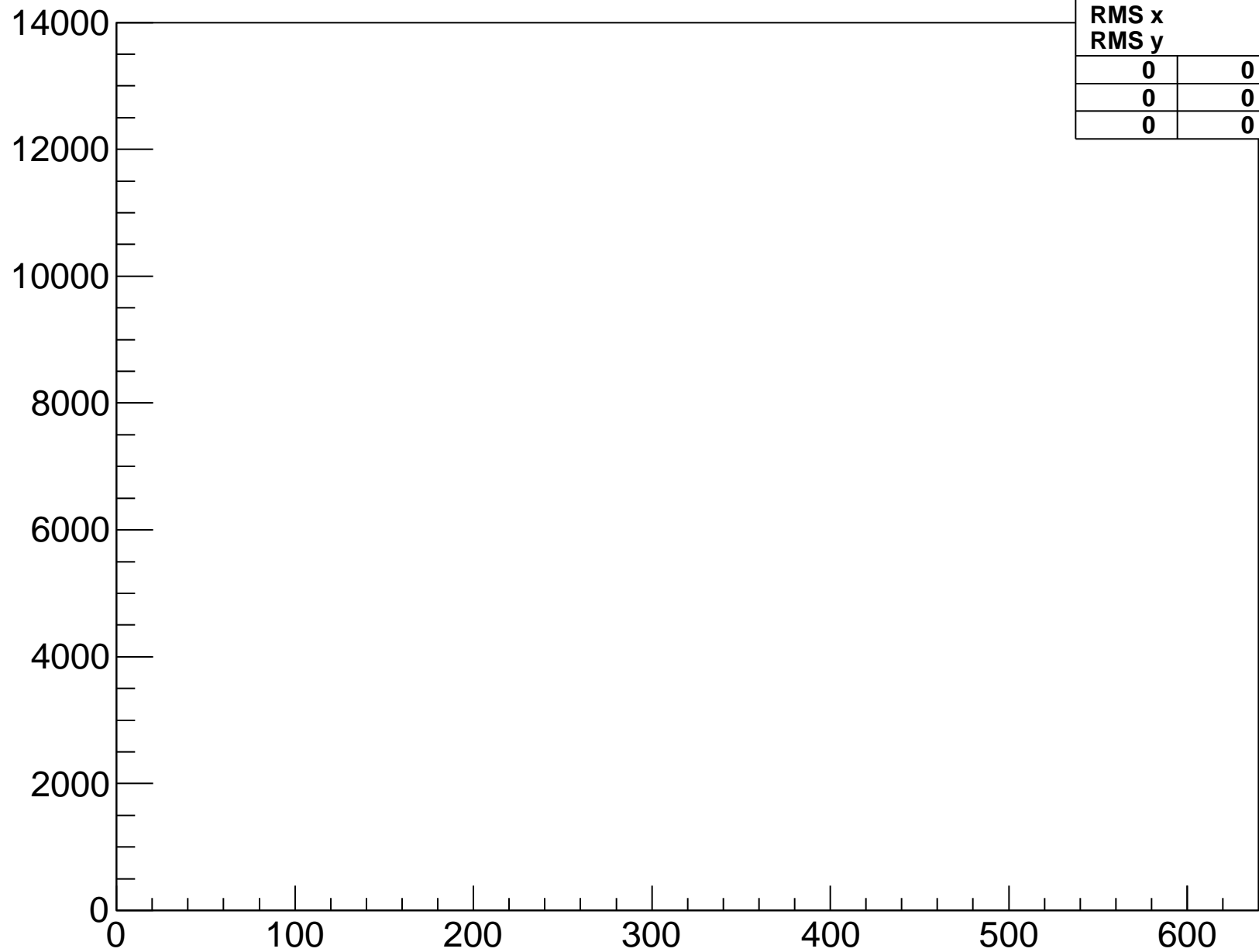
baselinesamples-fpga-8-hyb-2-sample-1

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

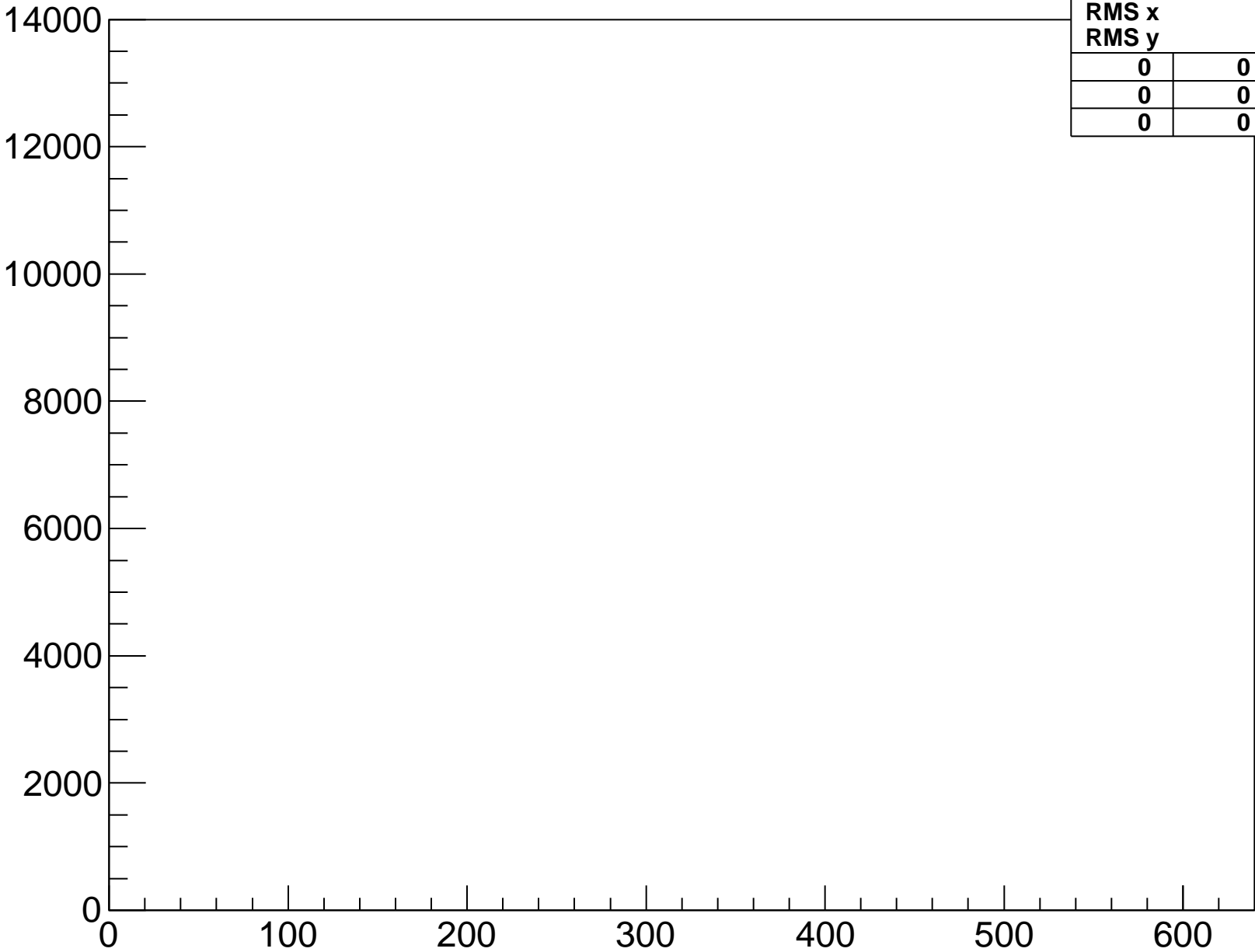


baselinesamples-fpga-8-hyb-2-sample-2

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0



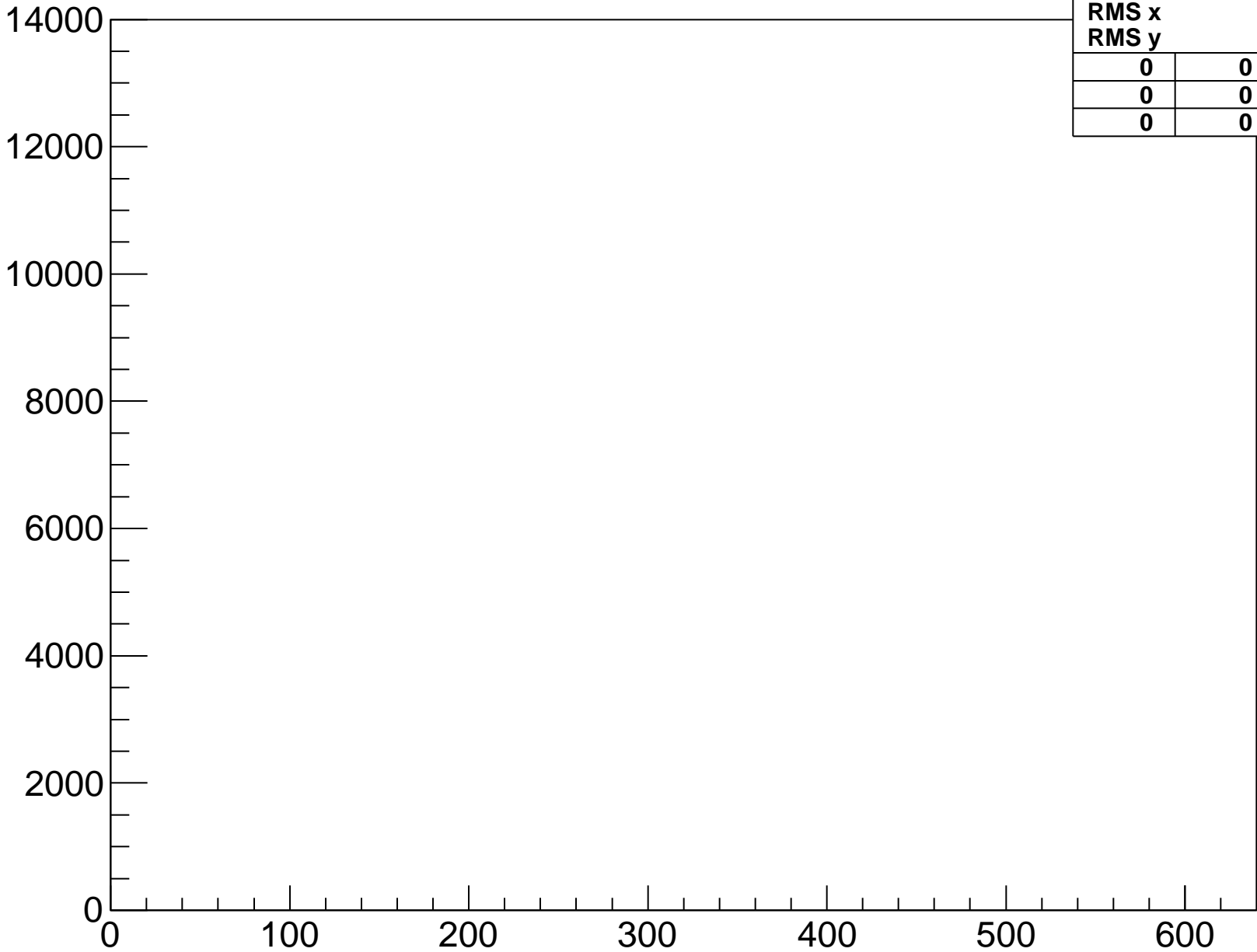
baselinesamples-fpga-8-hyb-2-sample-3



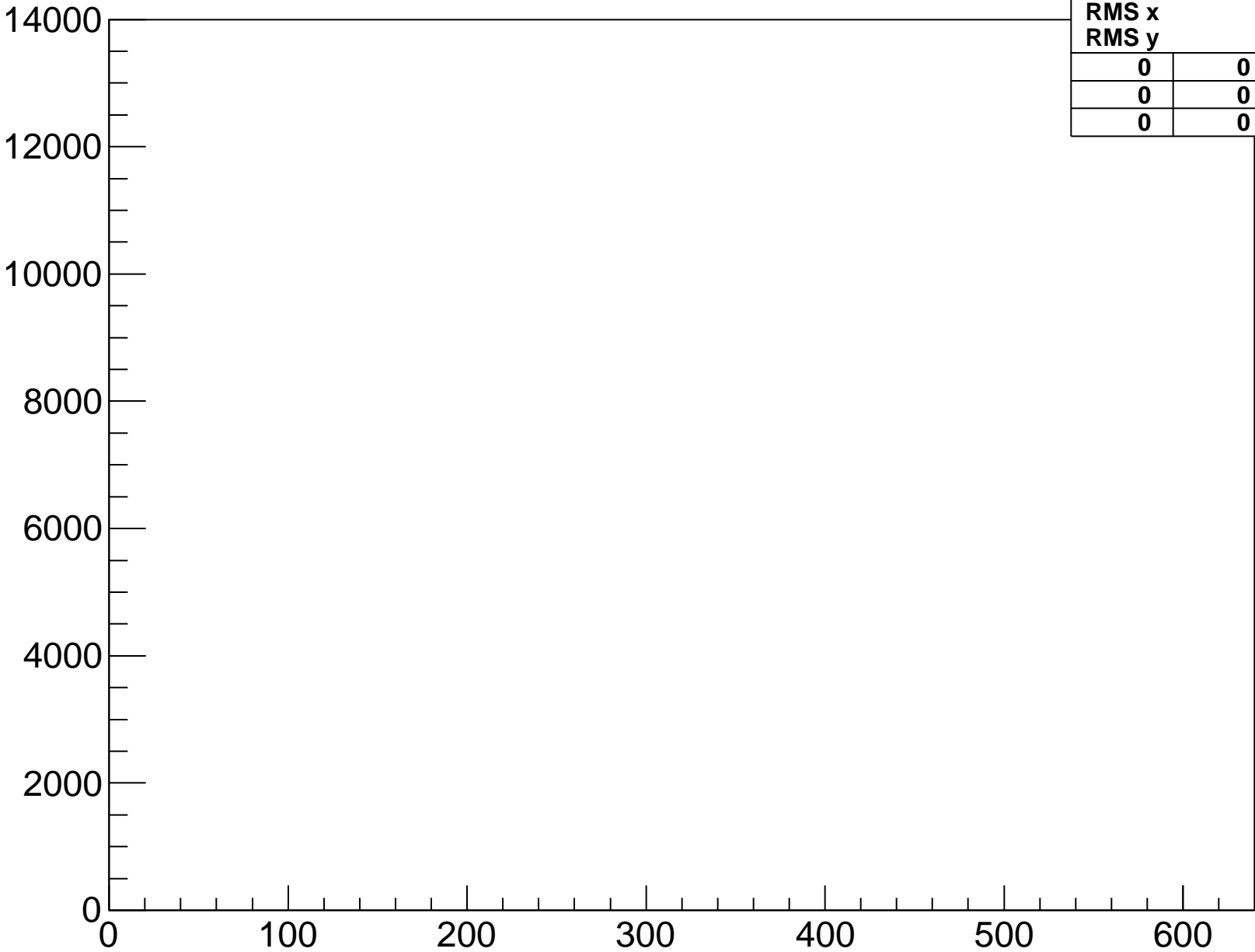
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-8-hyb-2-sample-4

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



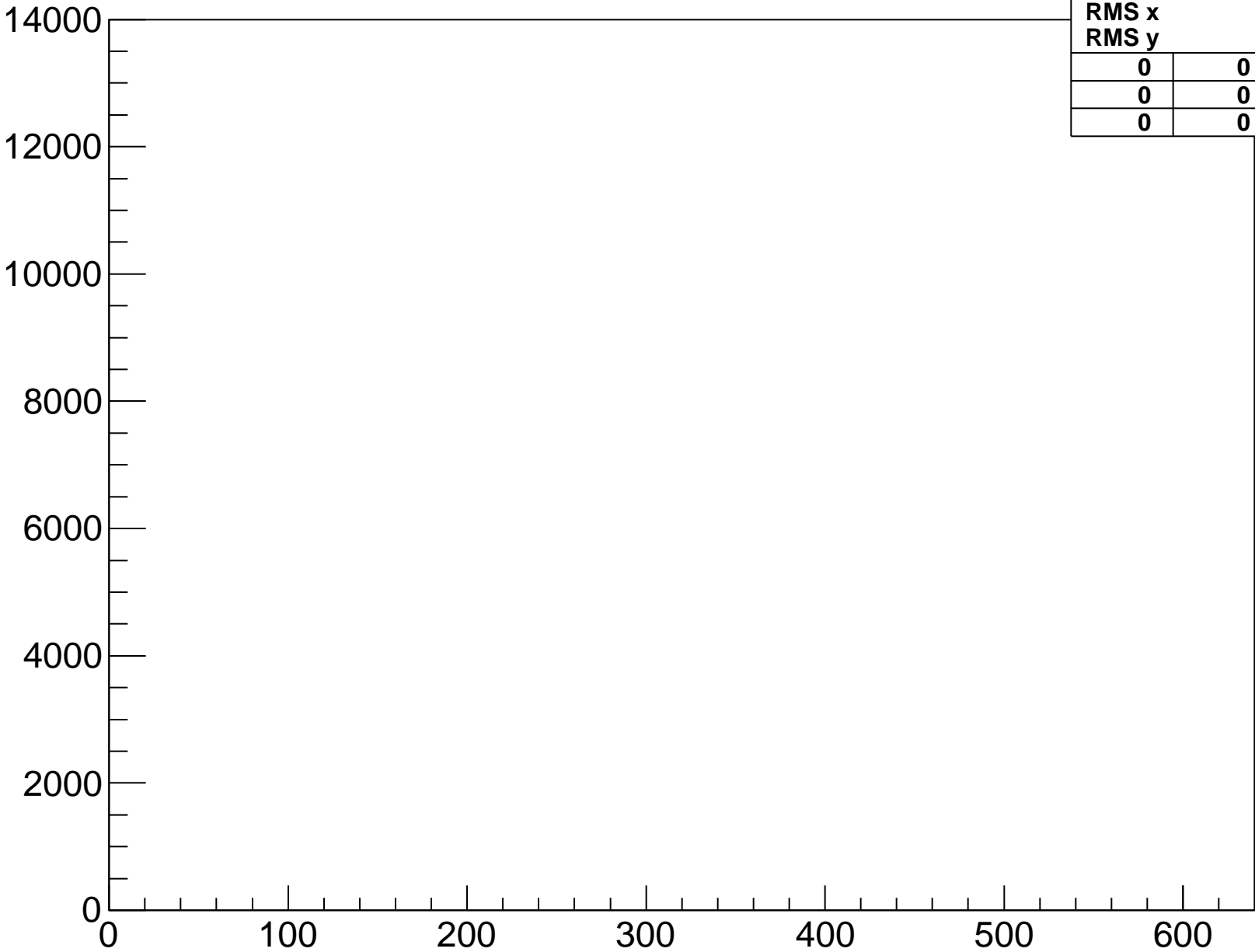
baselinesamples-fpga-8-hyb-2-sample-5



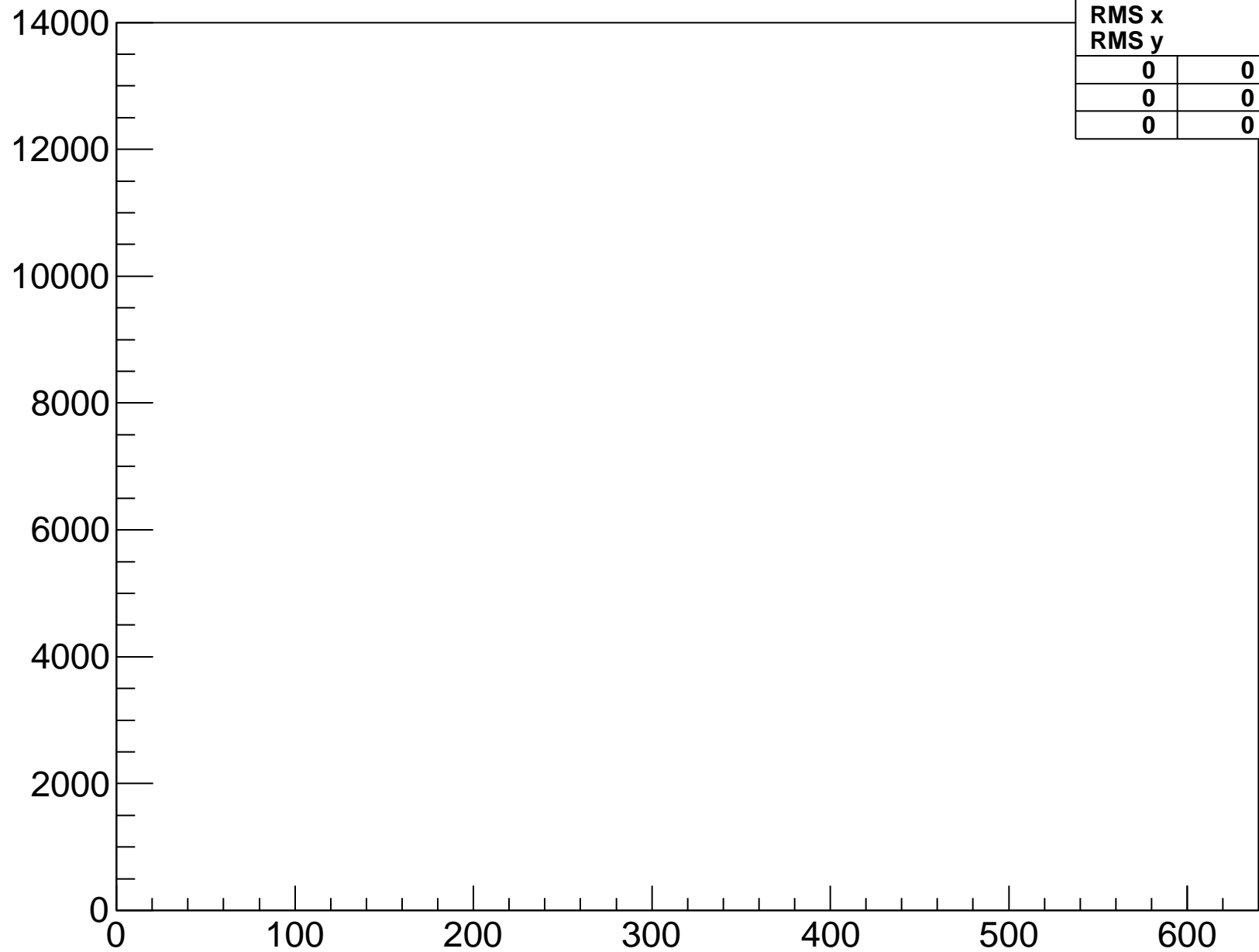
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-8-hyb-3-sample-0

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

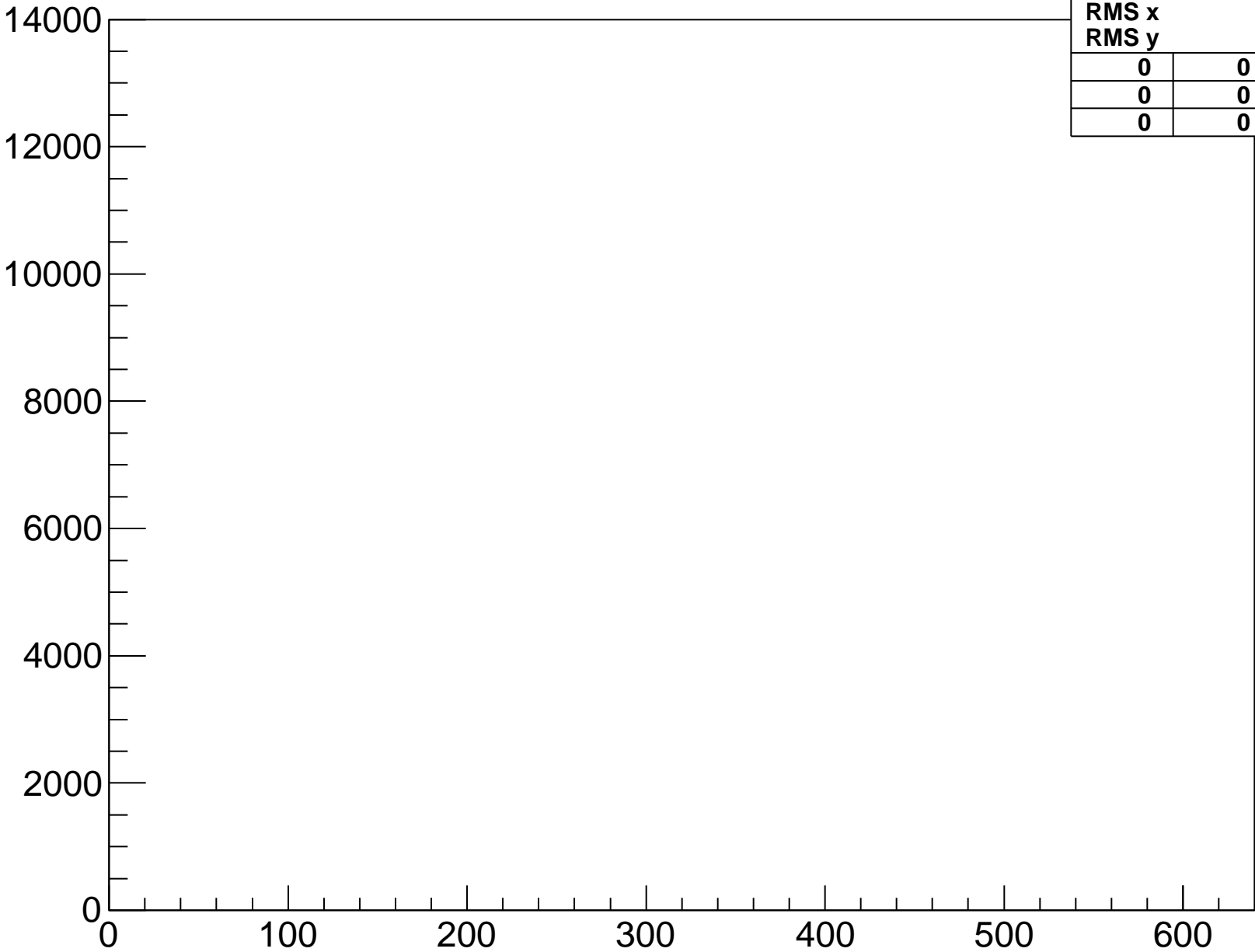


baselinesamples-fpga-8-hyb-3-sample-1



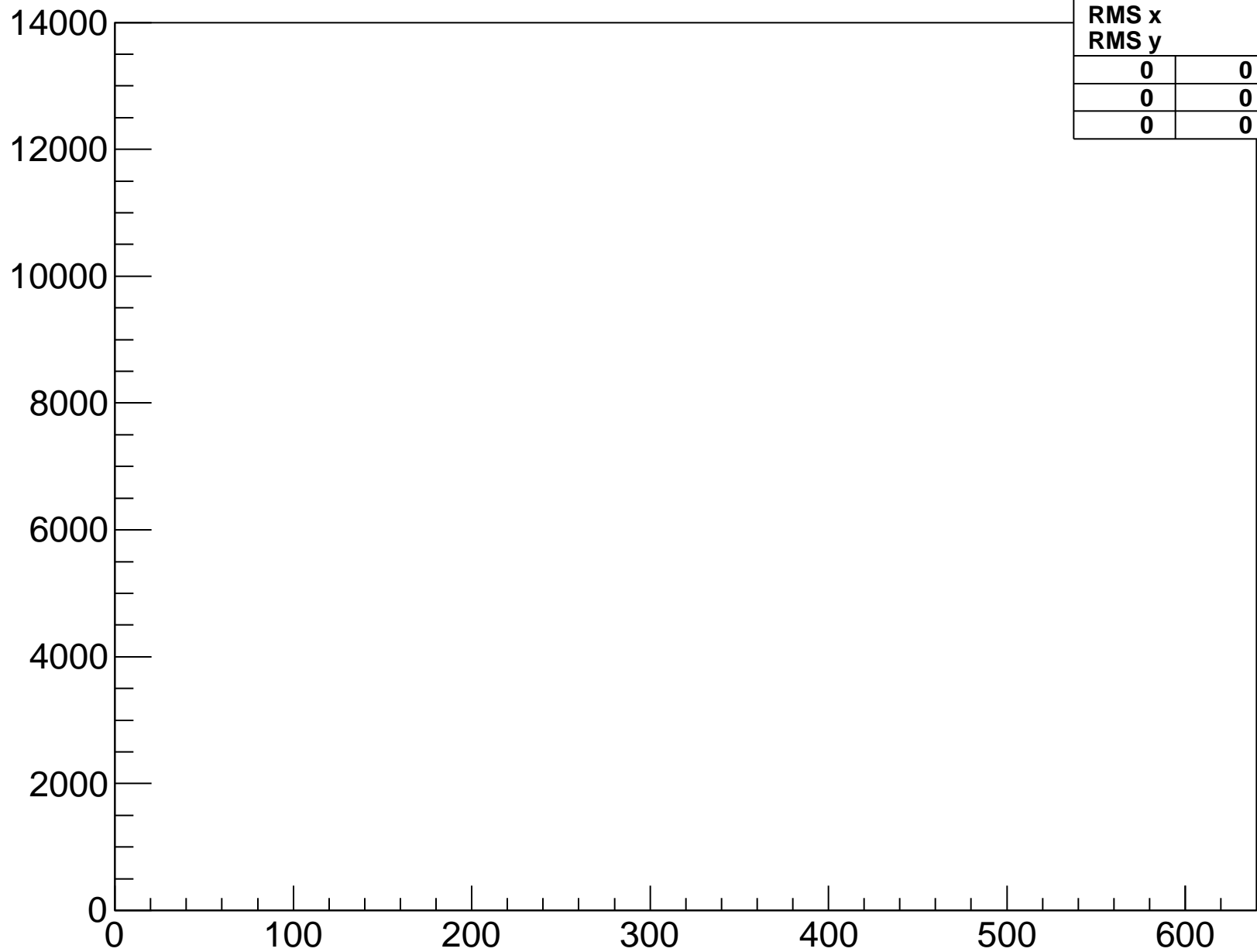
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-8-hyb-3-sample-2



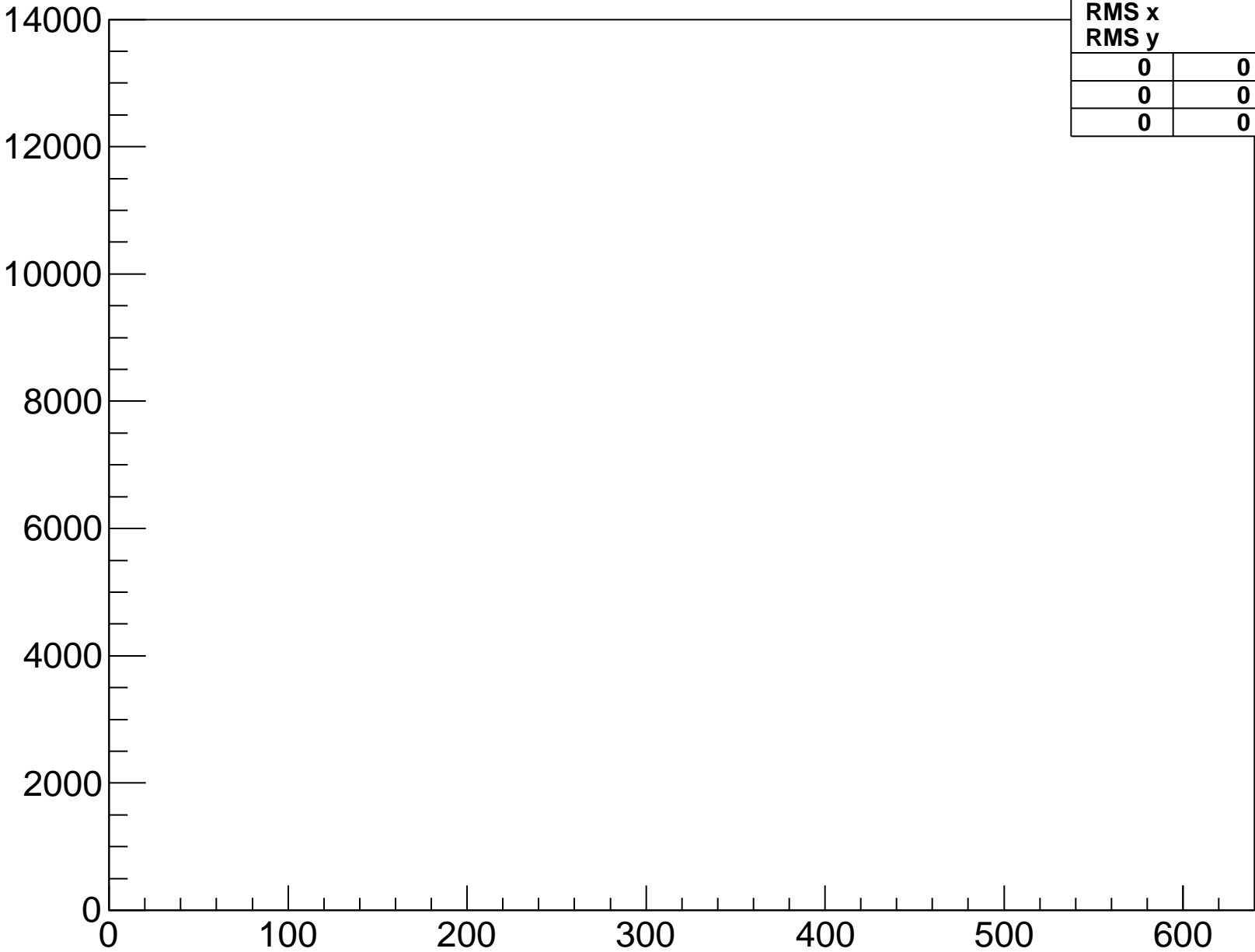
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-8-hyb-3-sample-3



Entries	0		
Mean x	0		
Mean y	0		
RMS x	0		
RMS y	0		
0	0	0	
0	0	0	
0	0	0	

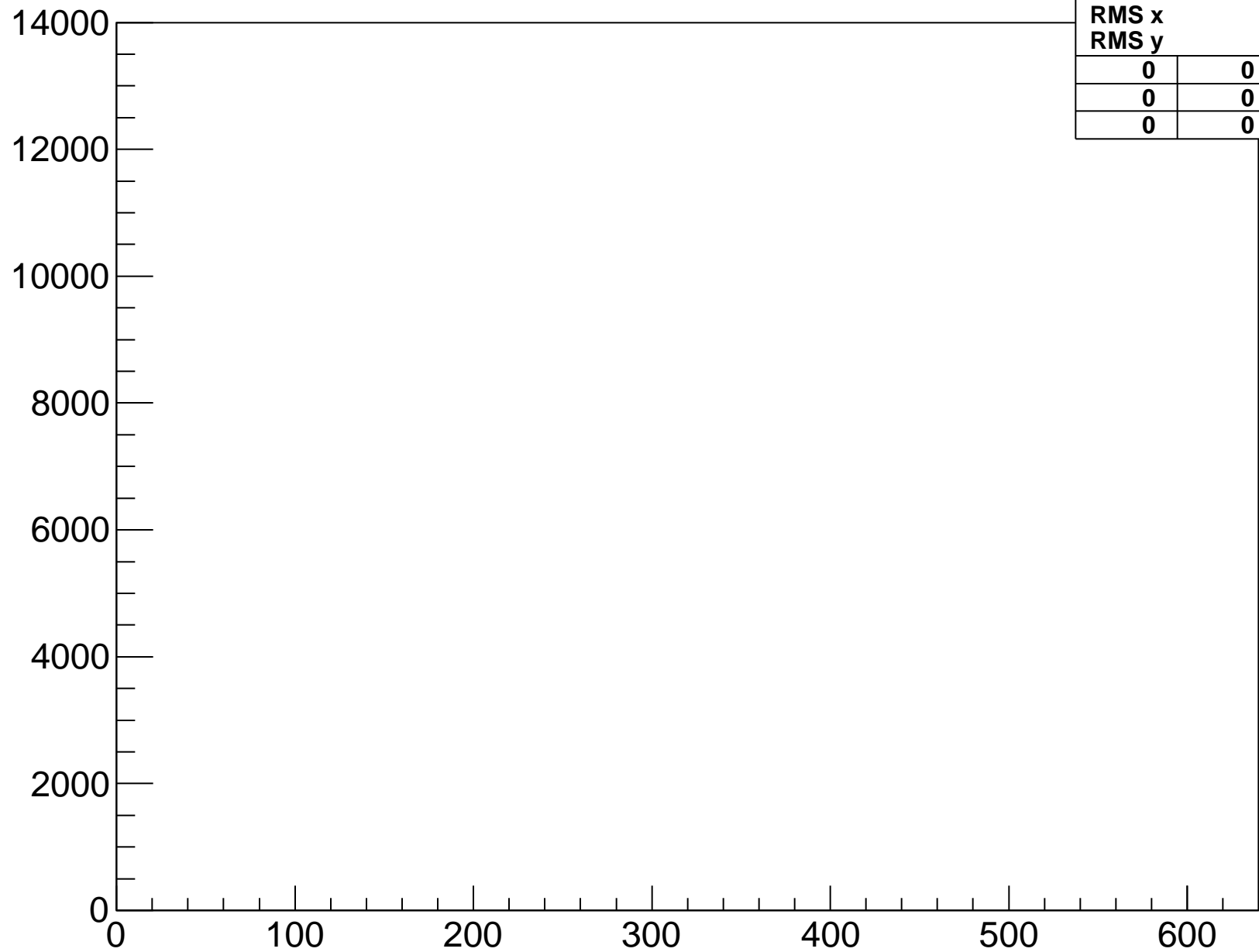
baselinesamples-fpga-8-hyb-3-sample-4



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

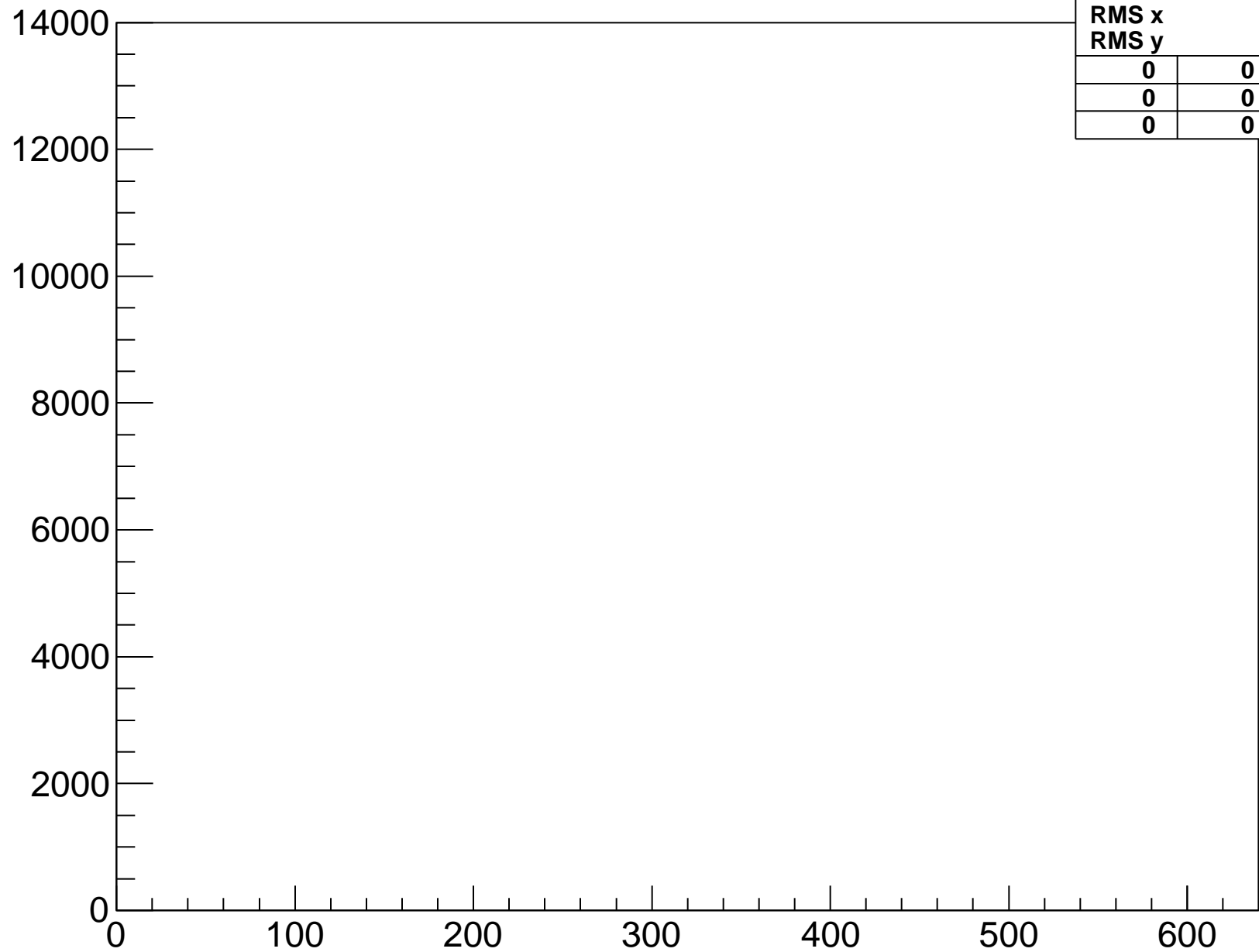
baselinesamples-fpga-8-hyb-3-sample-5

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	



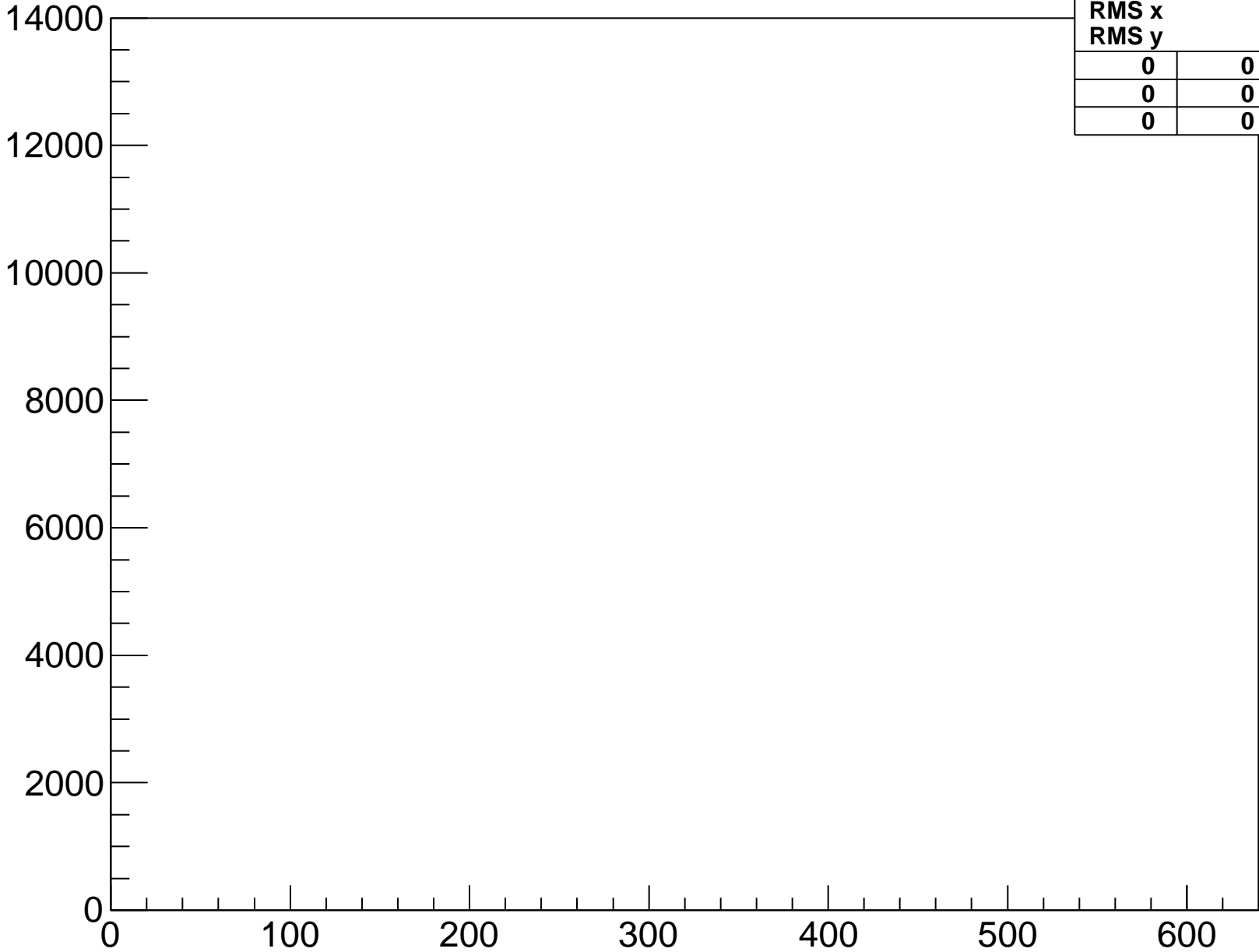
baselinesamples-fpga-9-hyb-0-sample-0

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

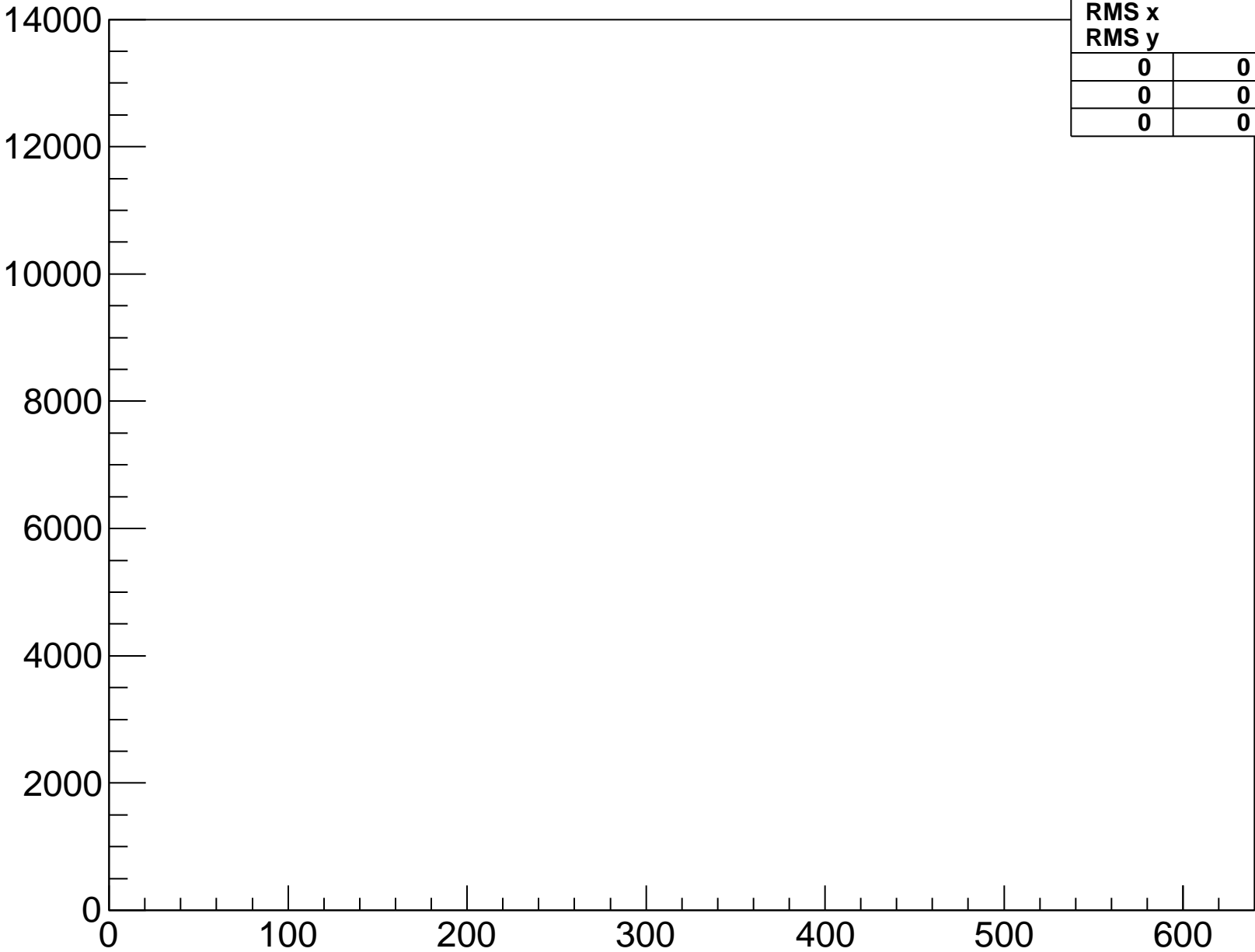


baselinesamples-fpga-9-hyb-0-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

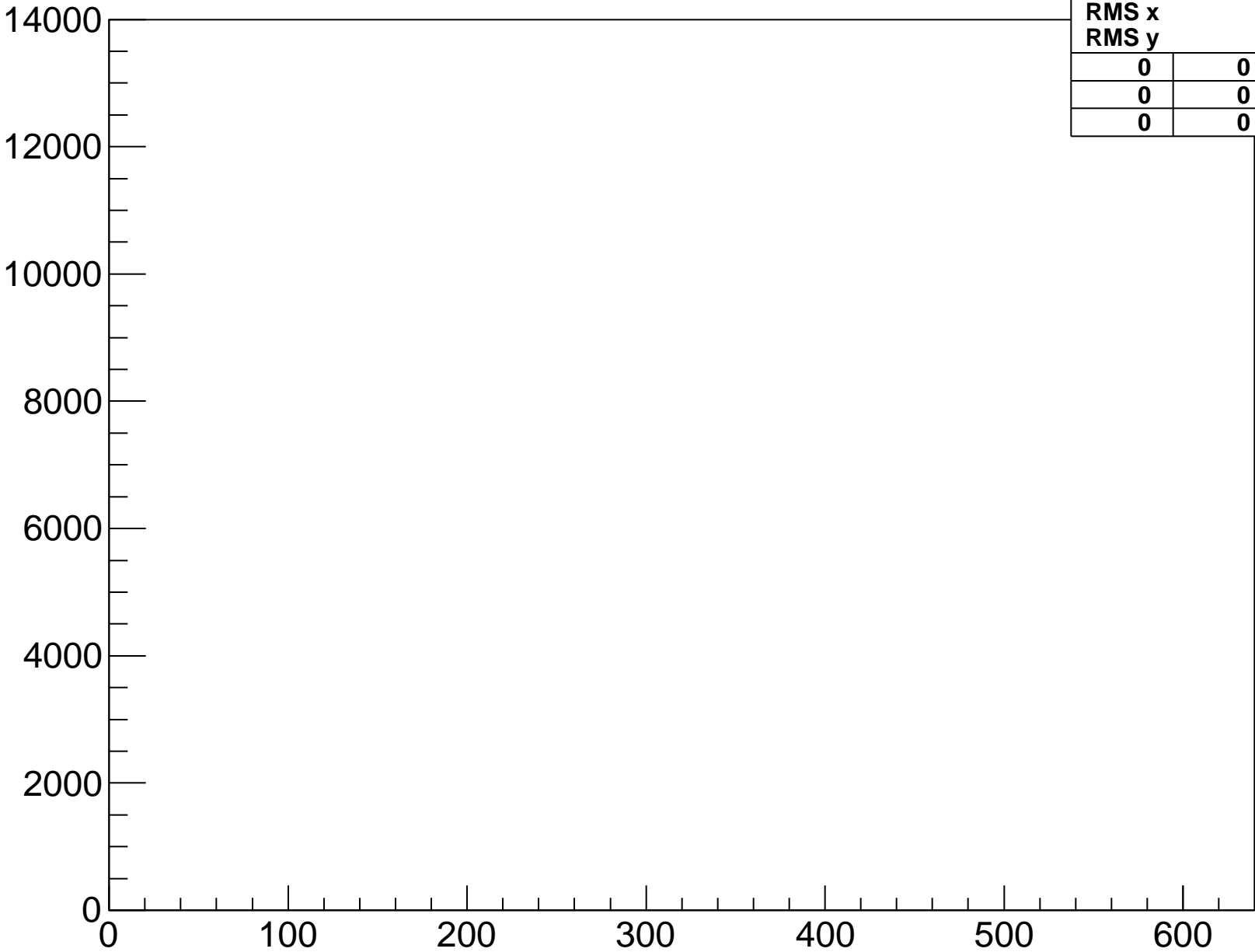


baselinesamples-fpga-9-hyb-0-sample-2



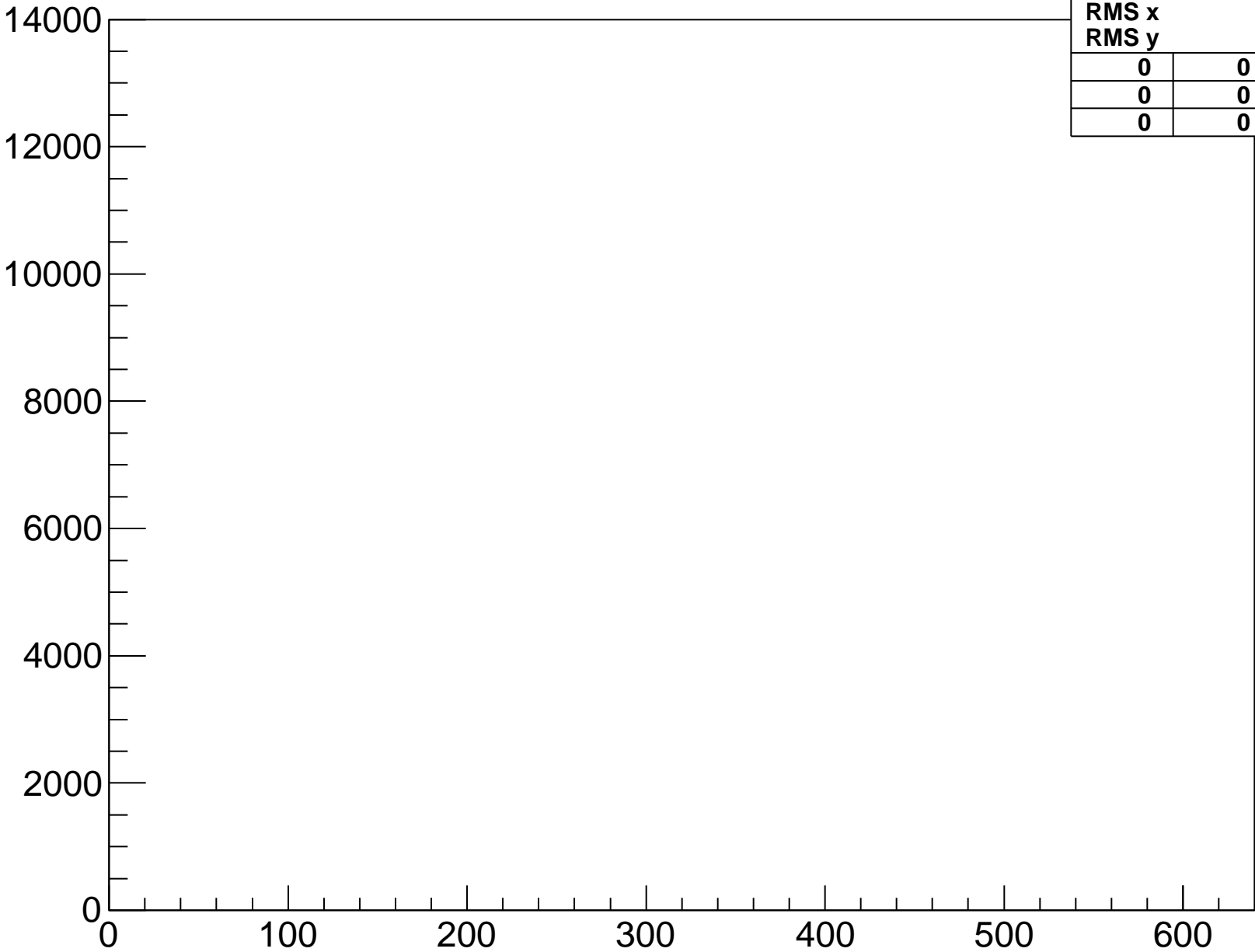
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-9-hyb-0-sample-3



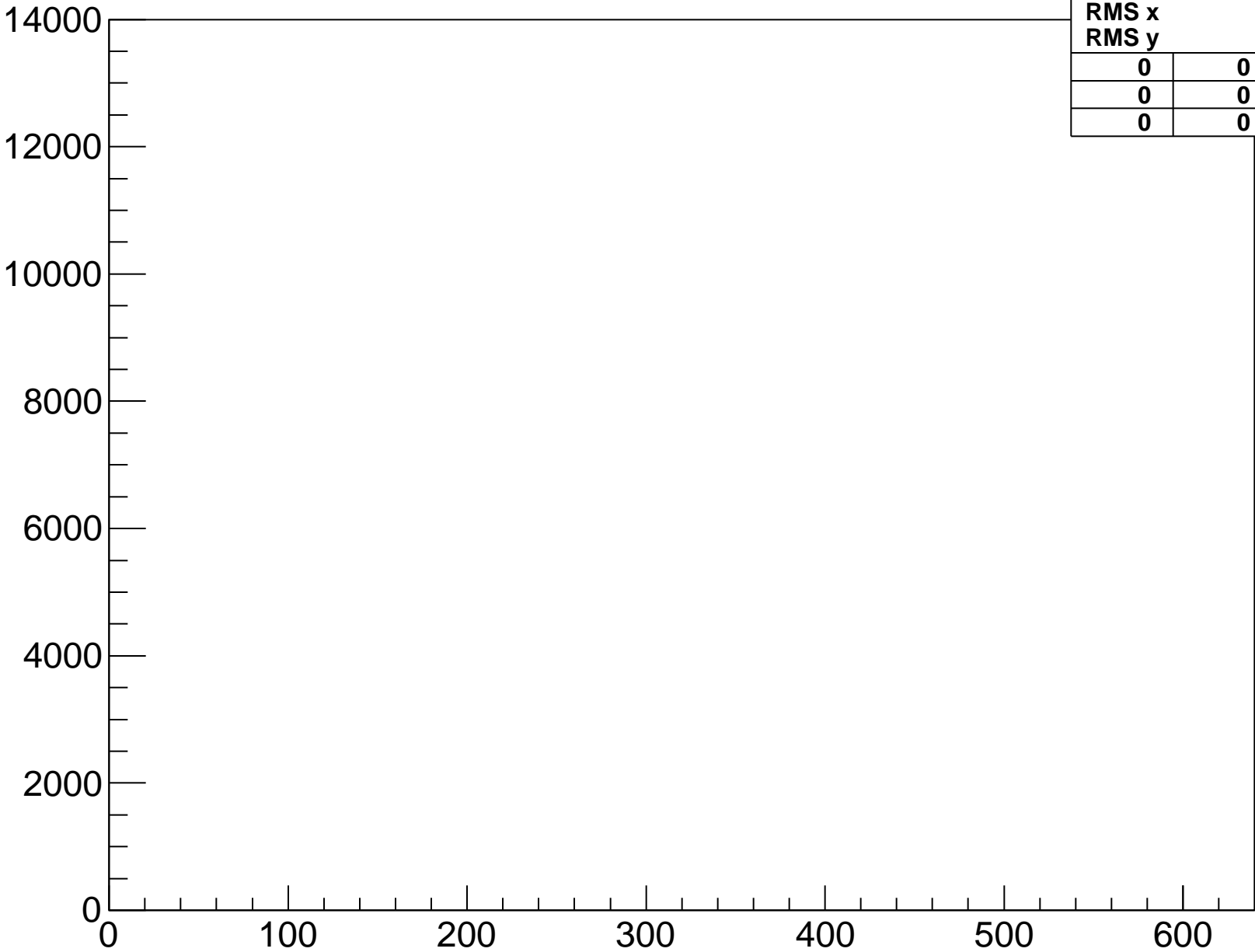
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-9-hyb-0-sample-4



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

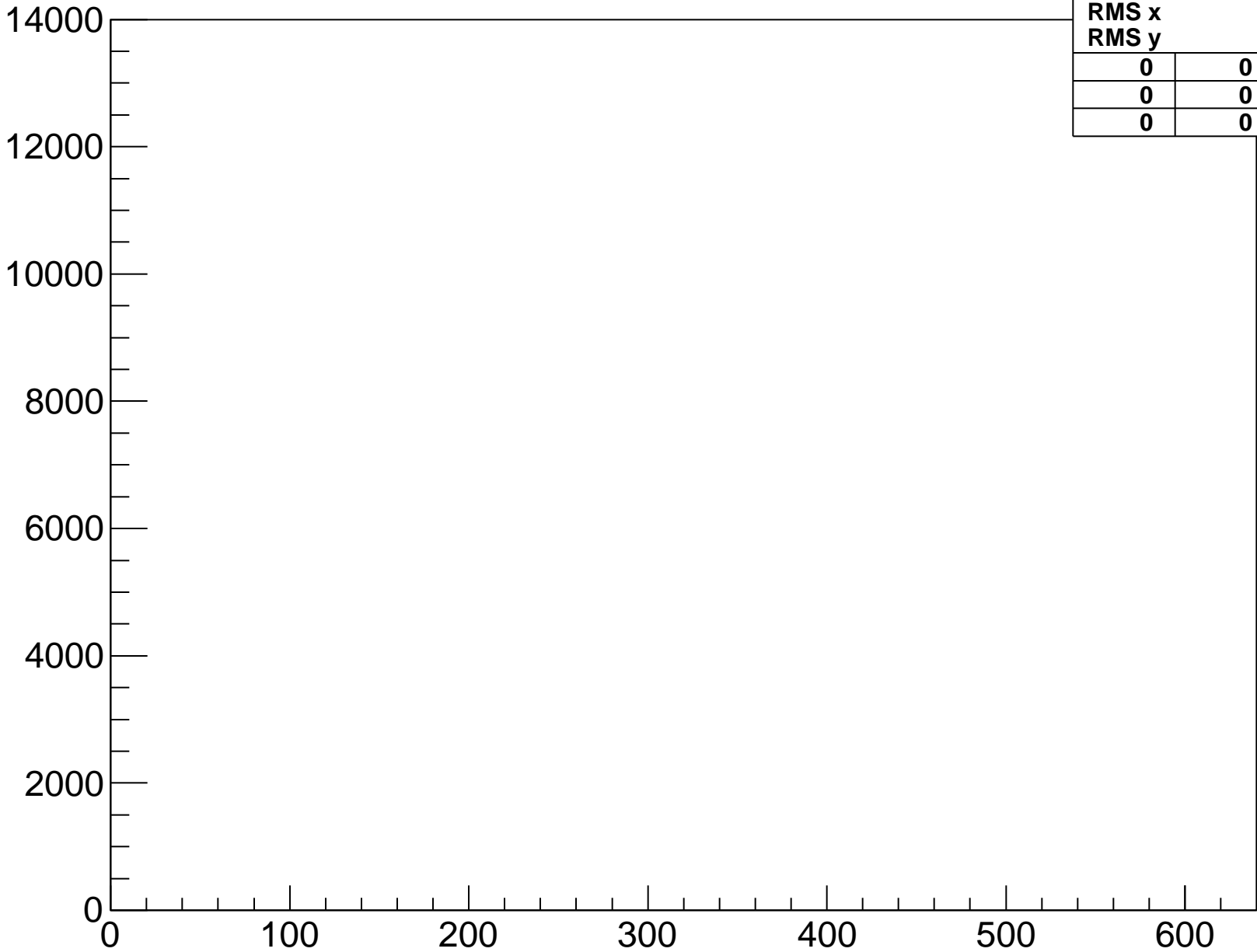
baselinesamples-fpga-9-hyb-0-sample-5



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

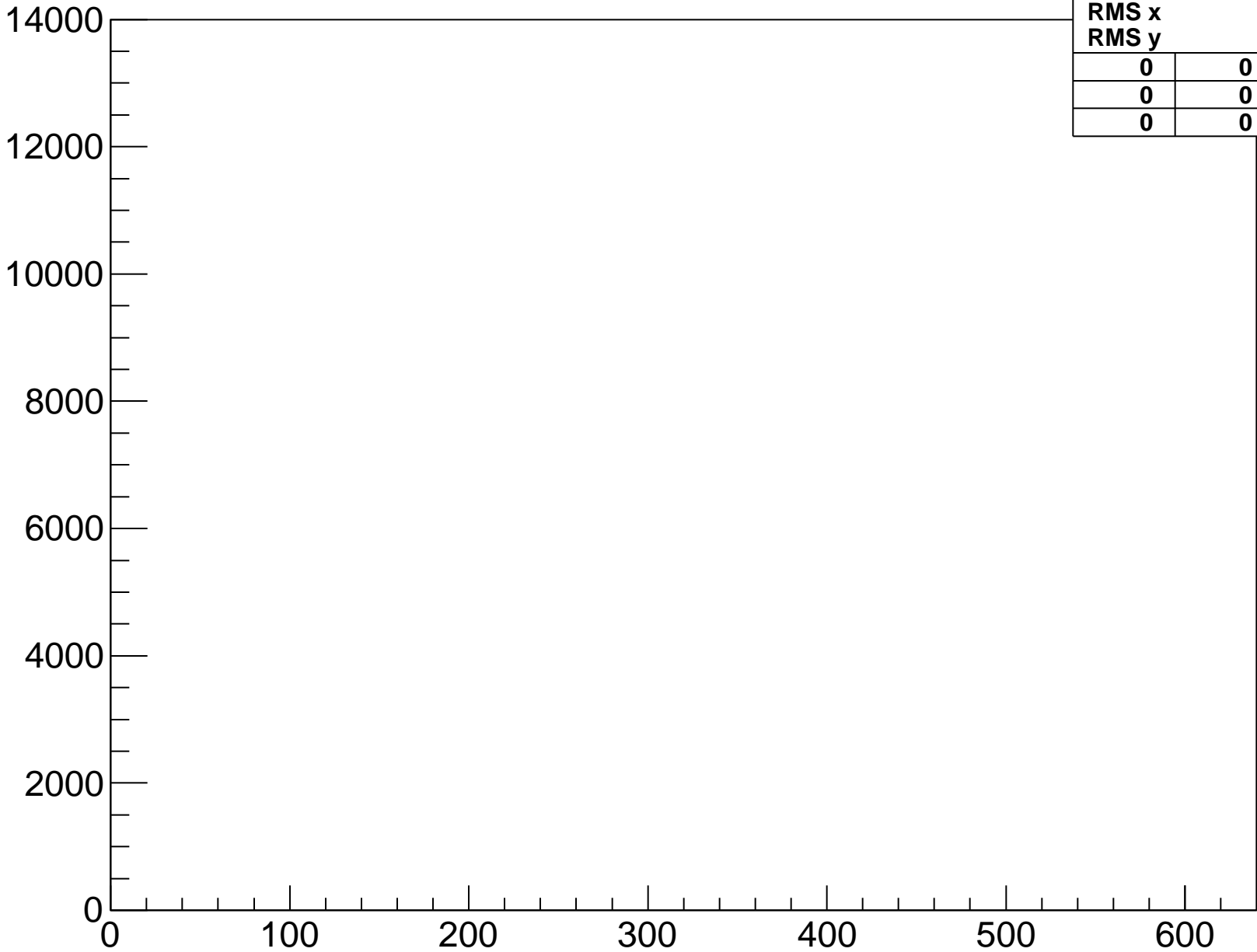
baselinesamples-fpga-9-hyb-1-sample-0

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0



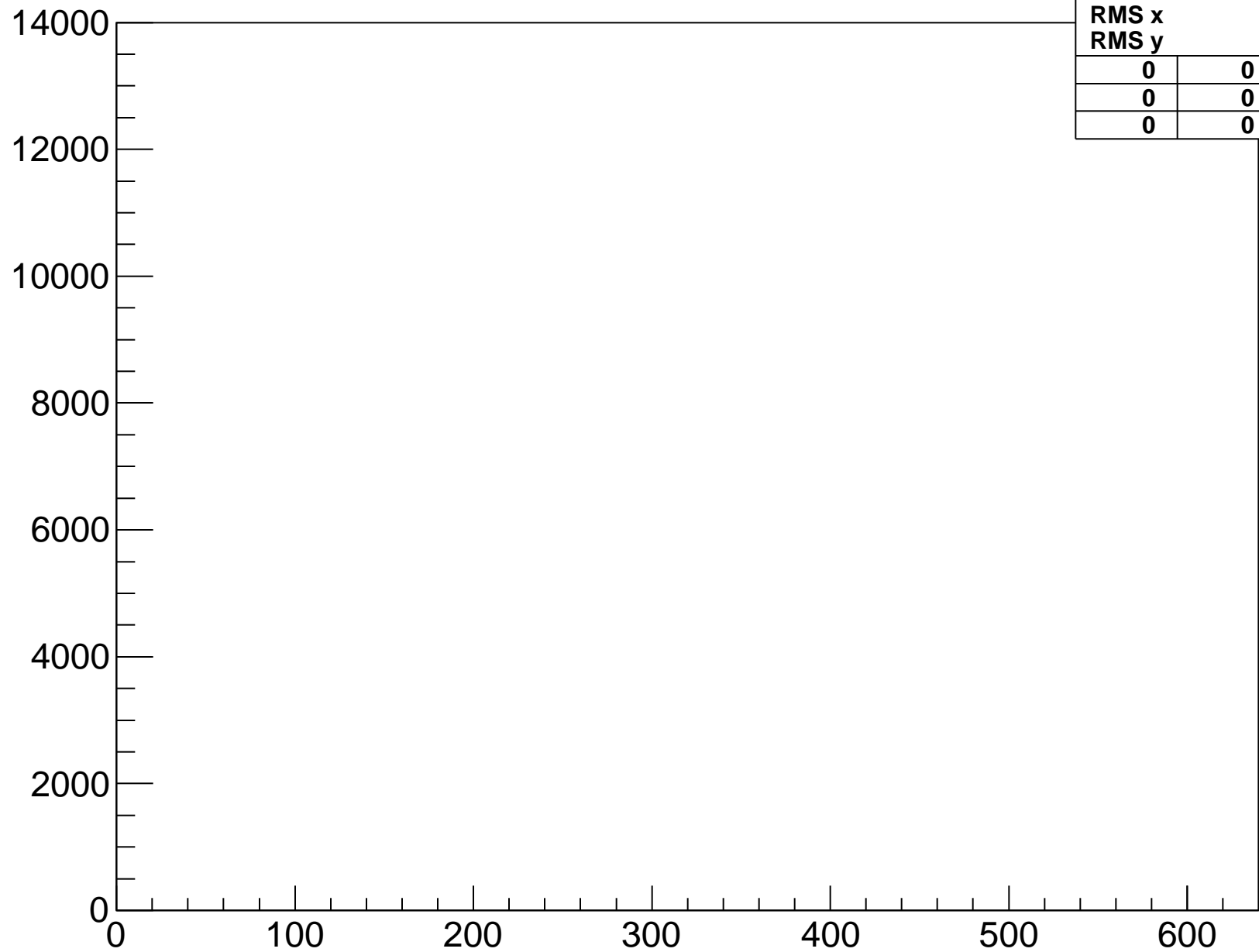
baselinesamples-fpga-9-hyb-1-sample-1

Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	
0	0	0	
0	0	0	

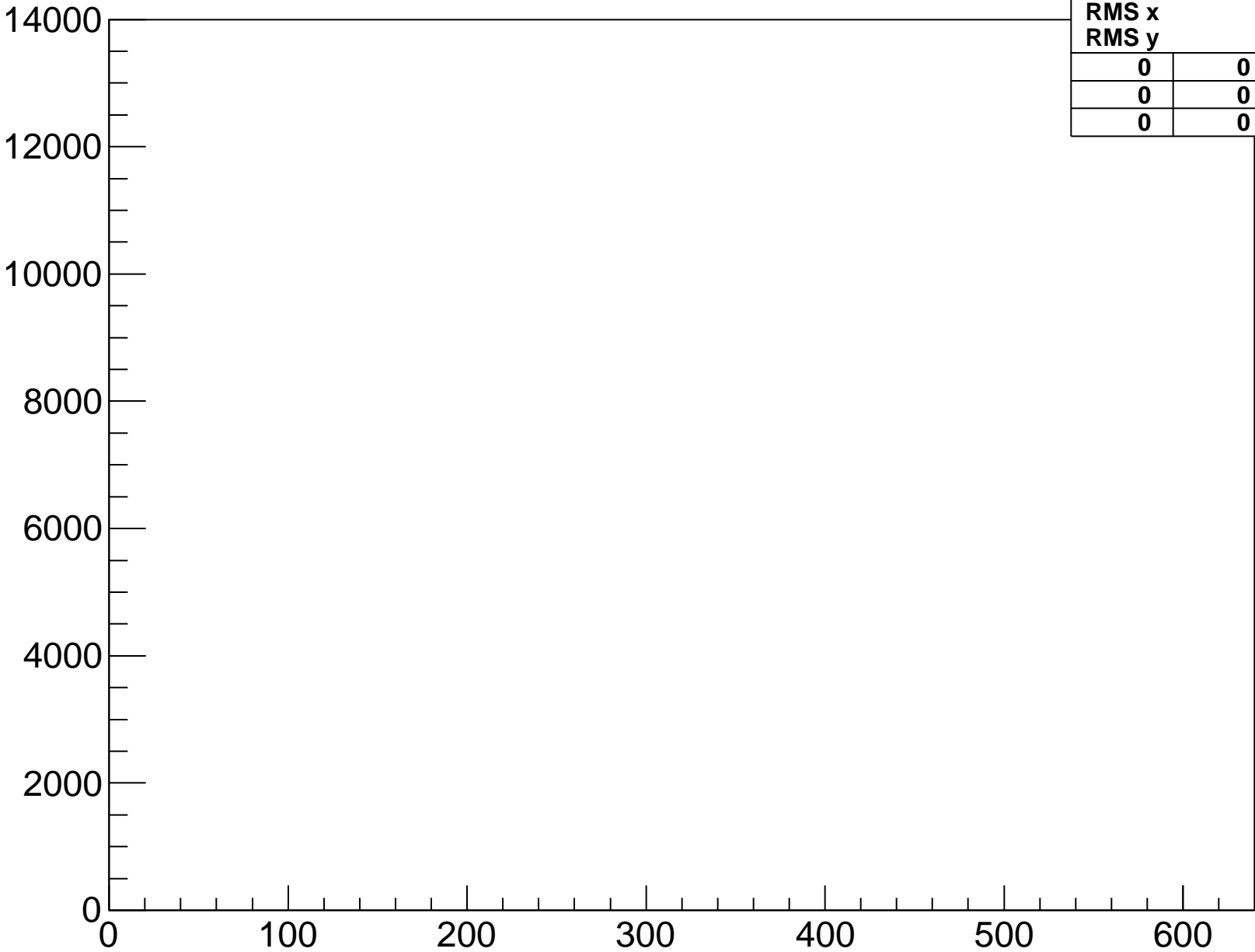


baselinesamples-fpga-9-hyb-1-sample-2

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

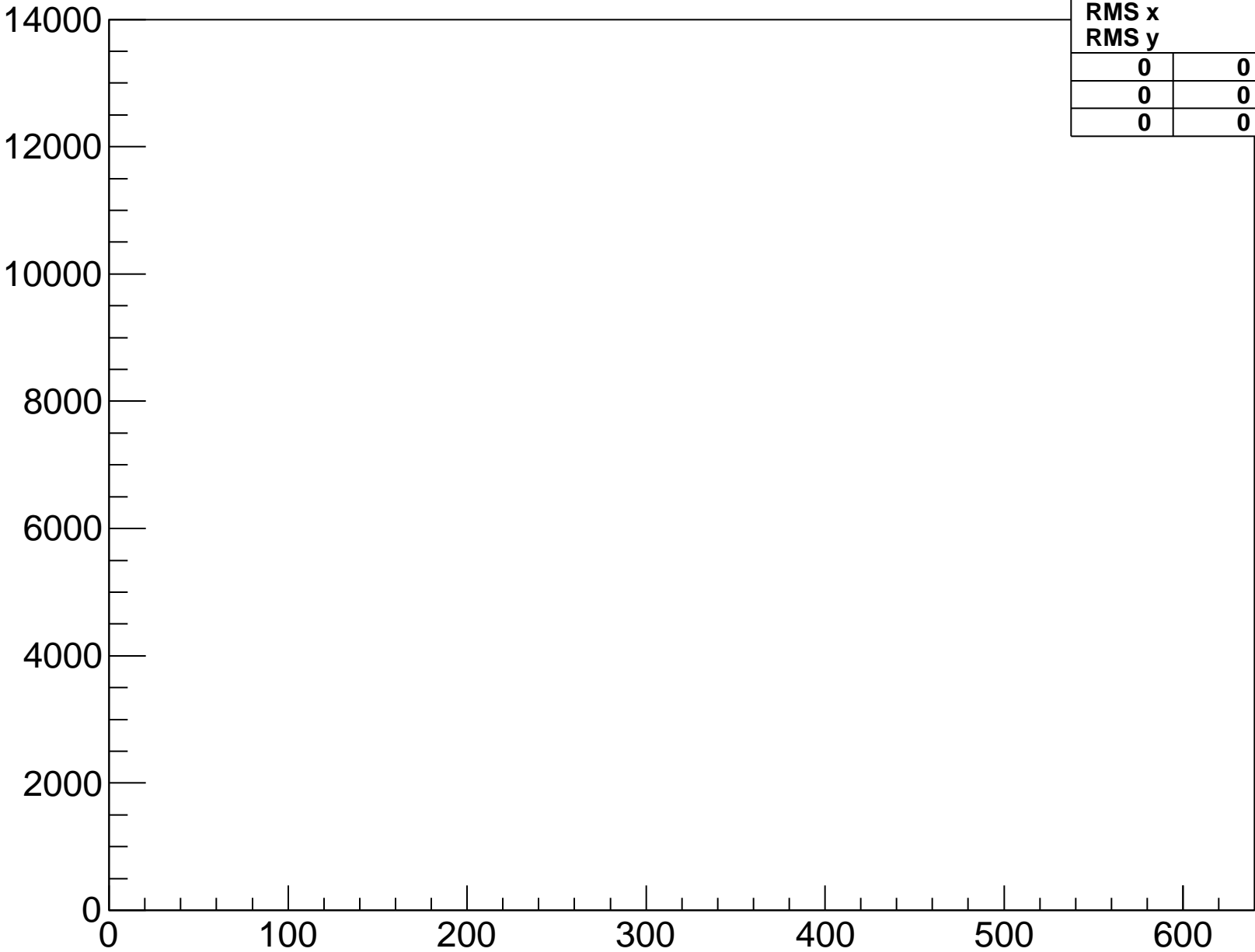


baselinesamples-fpga-9-hyb-1-sample-3



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

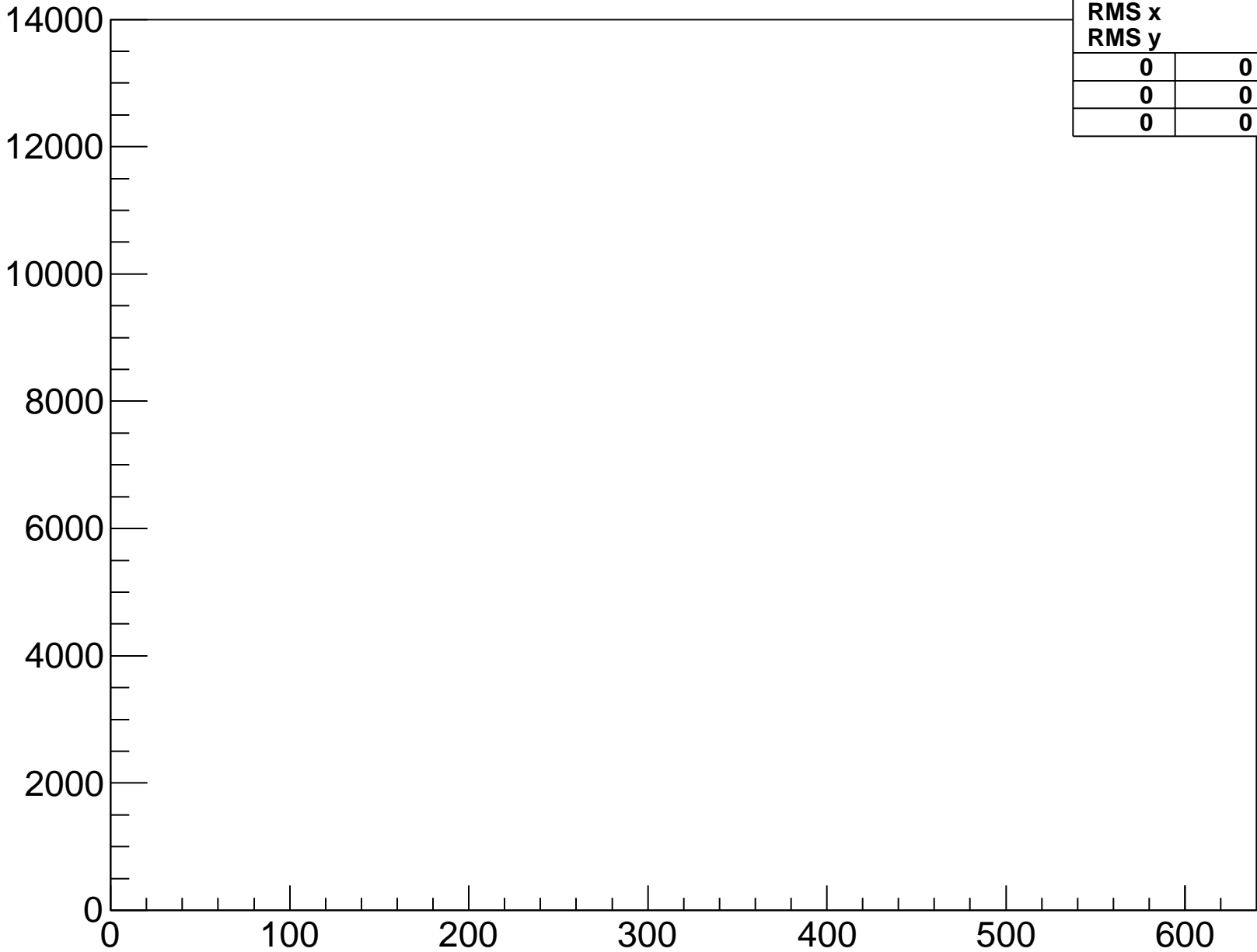
baselinesamples-fpga-9-hyb-1-sample-4



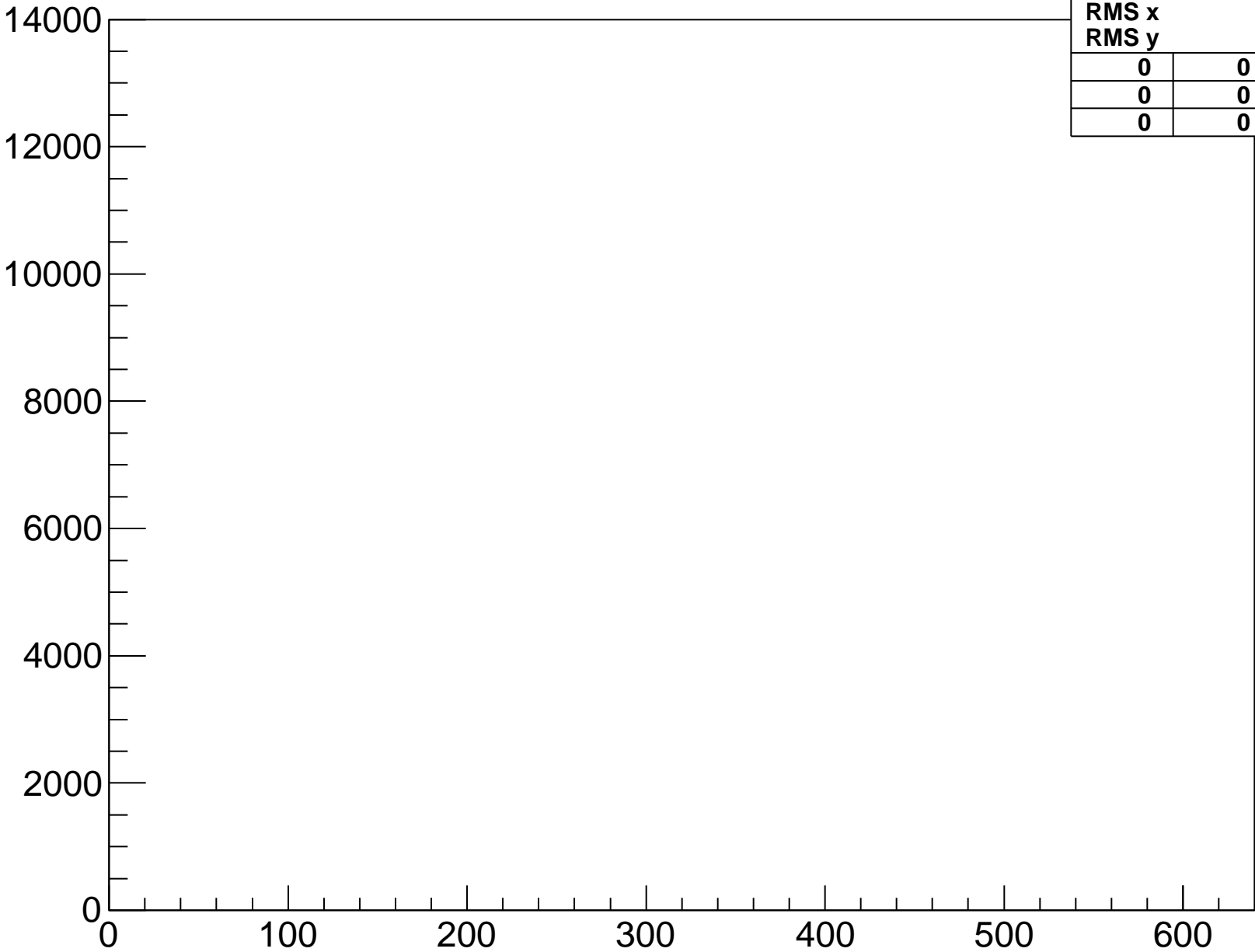
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-9-hyb-1-sample-5

Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

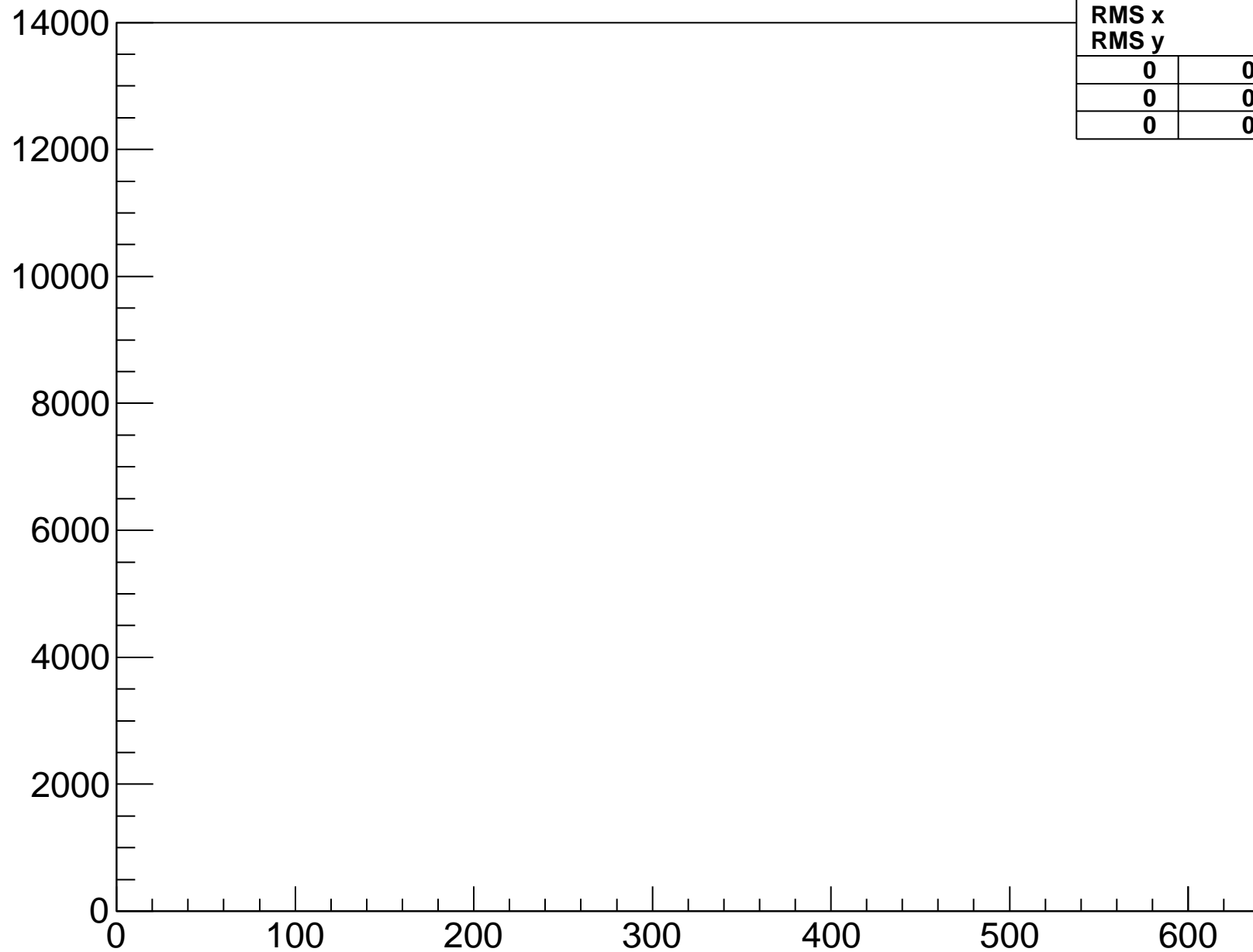


baselinesamples-fpga-9-hyb-2-sample-0



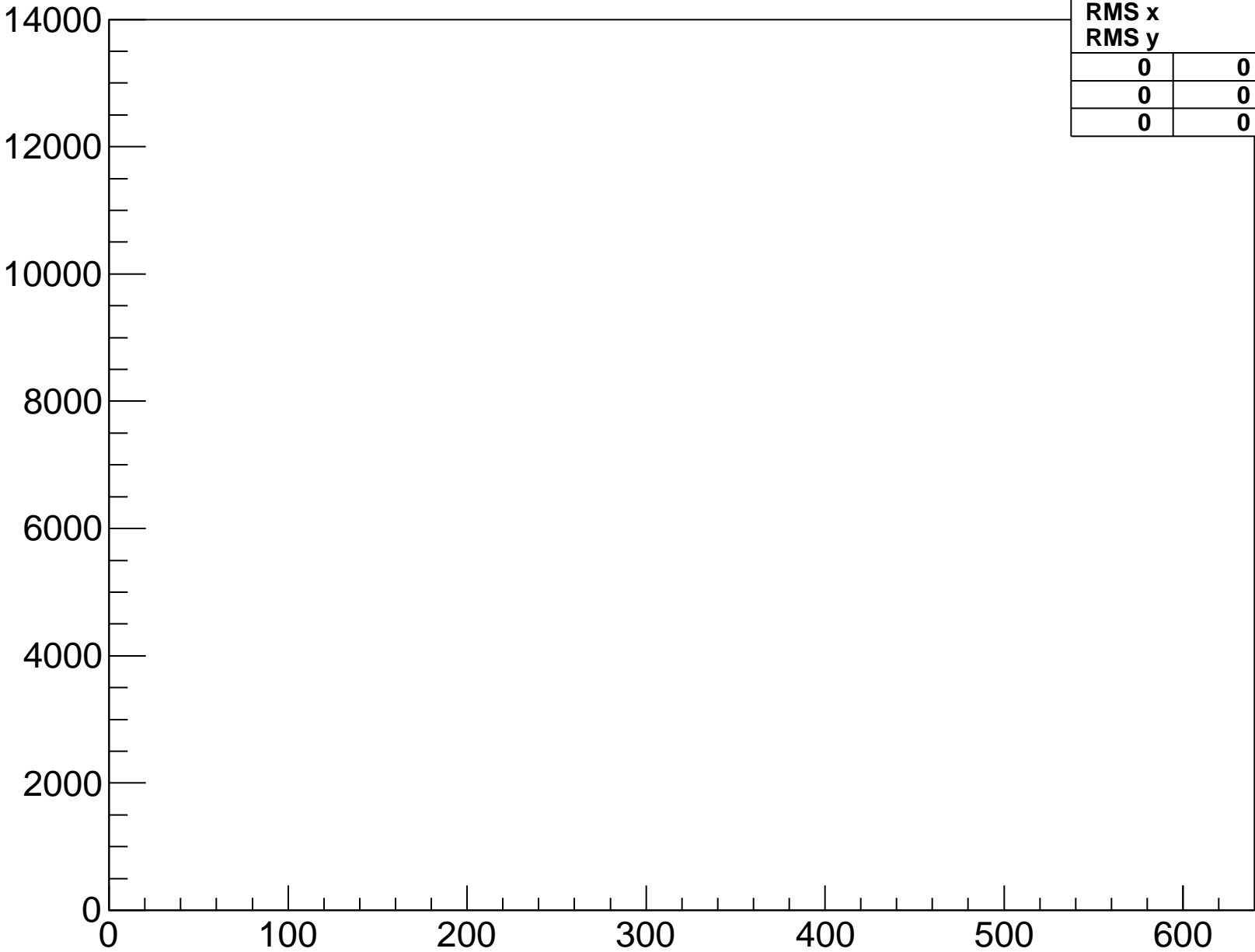
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-9-hyb-2-sample-1



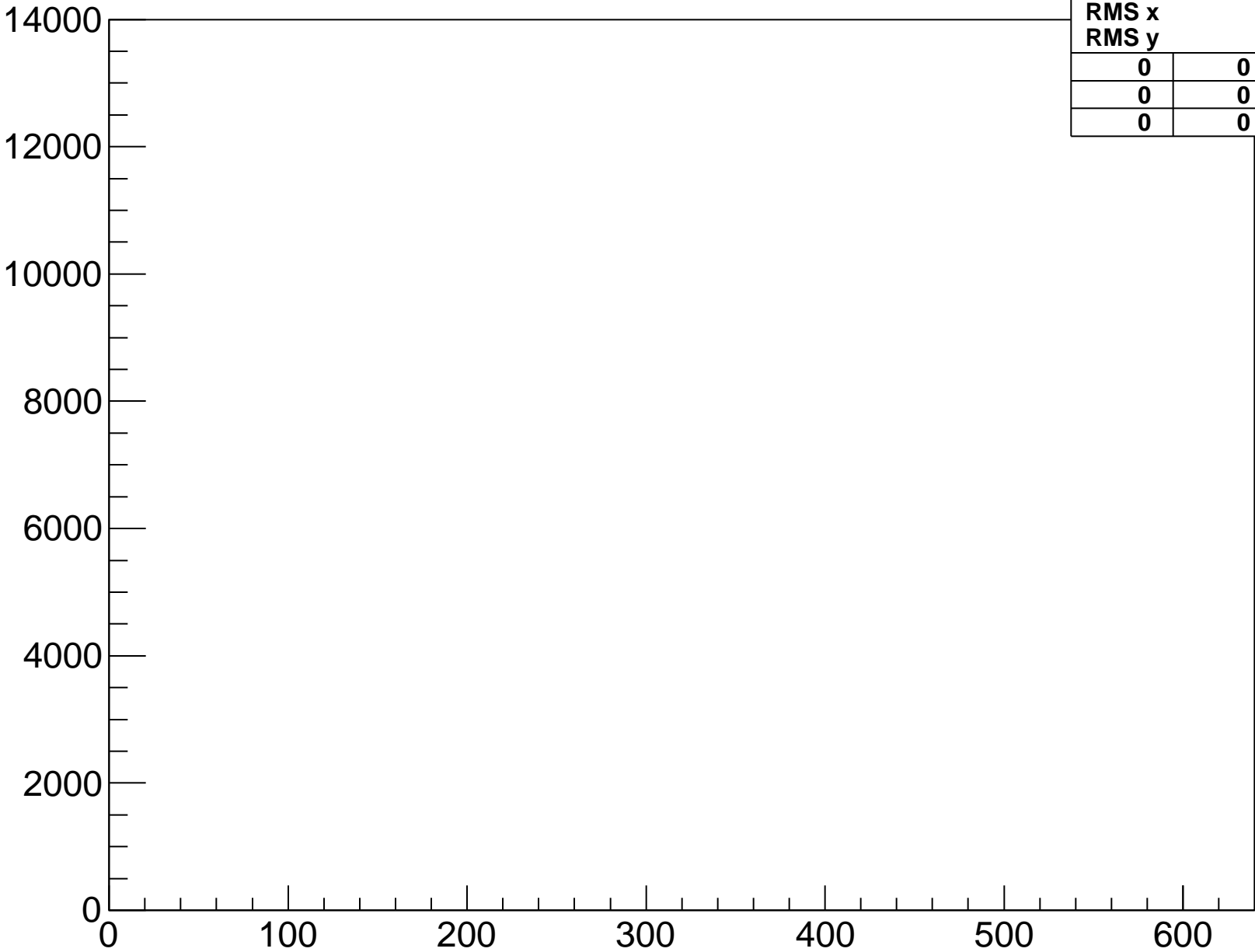
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-9-hyb-2-sample-2



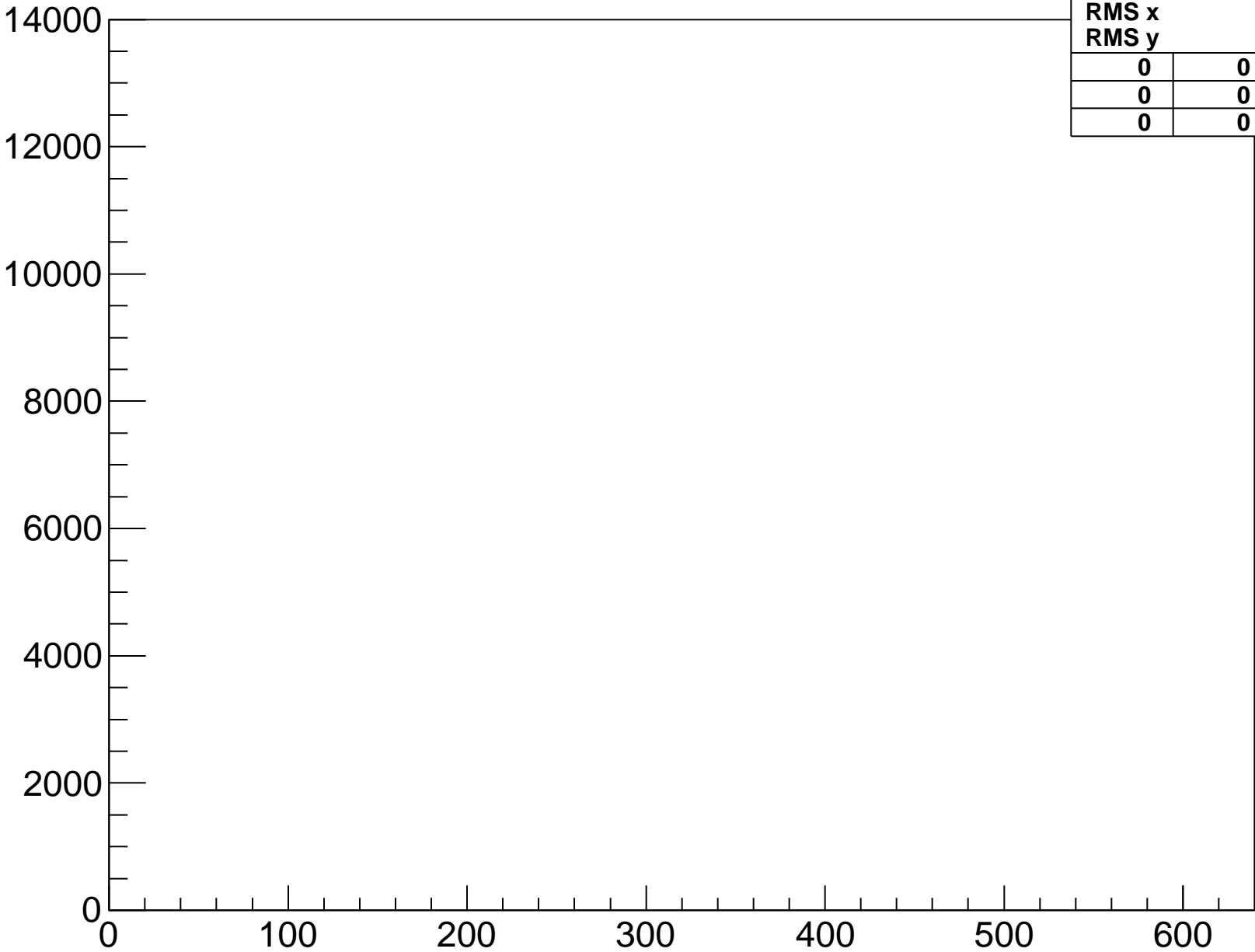
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-9-hyb-2-sample-3



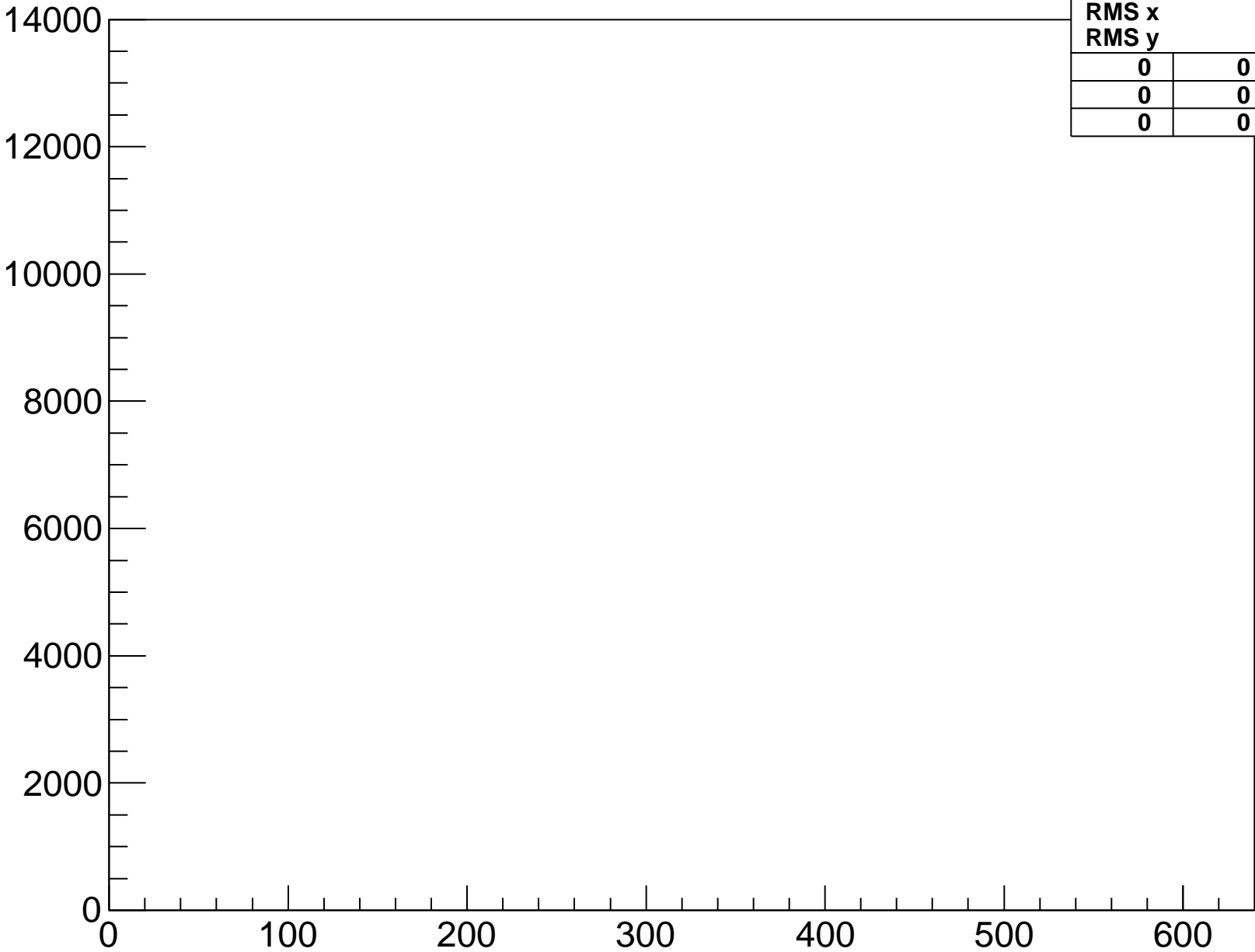
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-9-hyb-2-sample-4



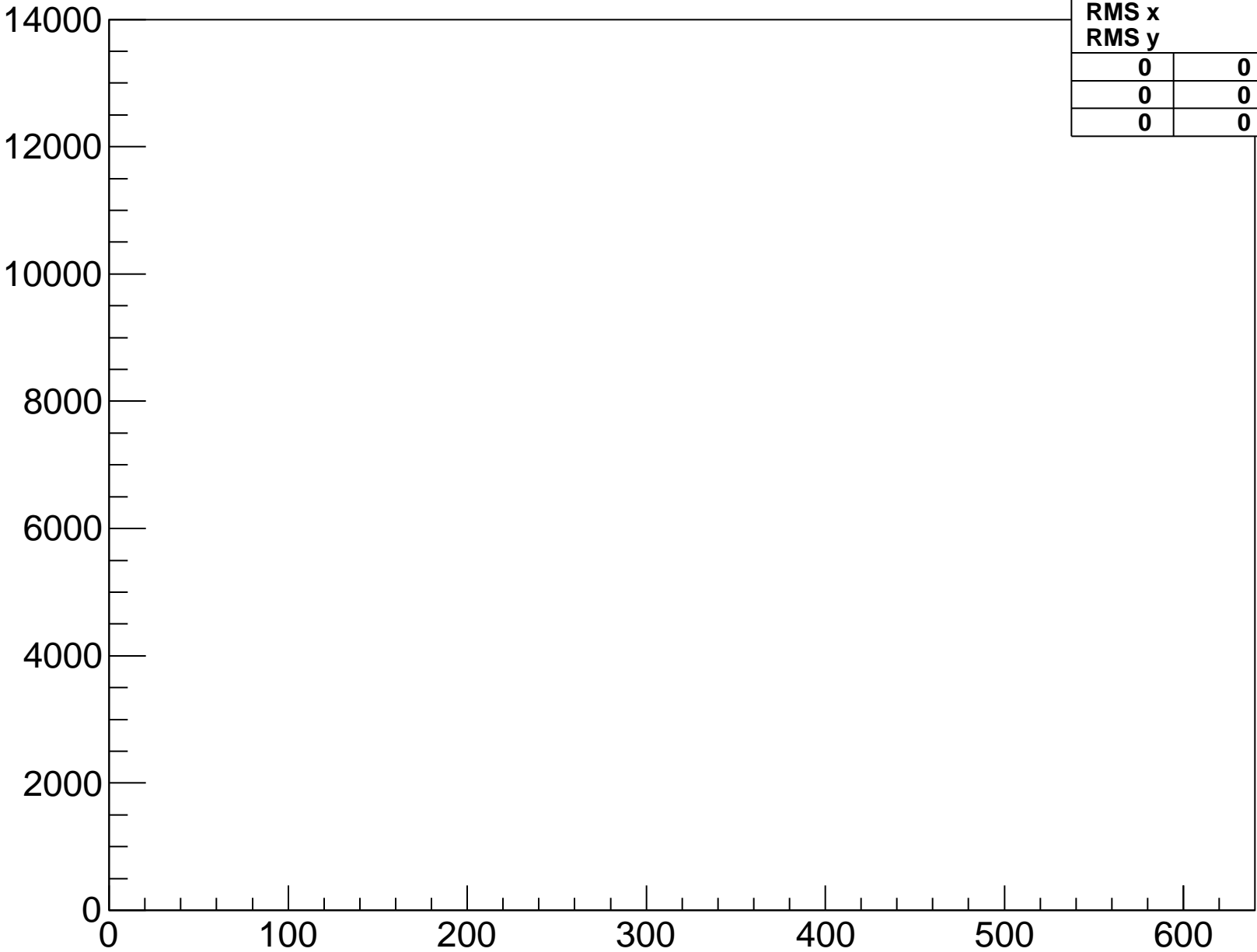
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-9-hyb-2-sample-5



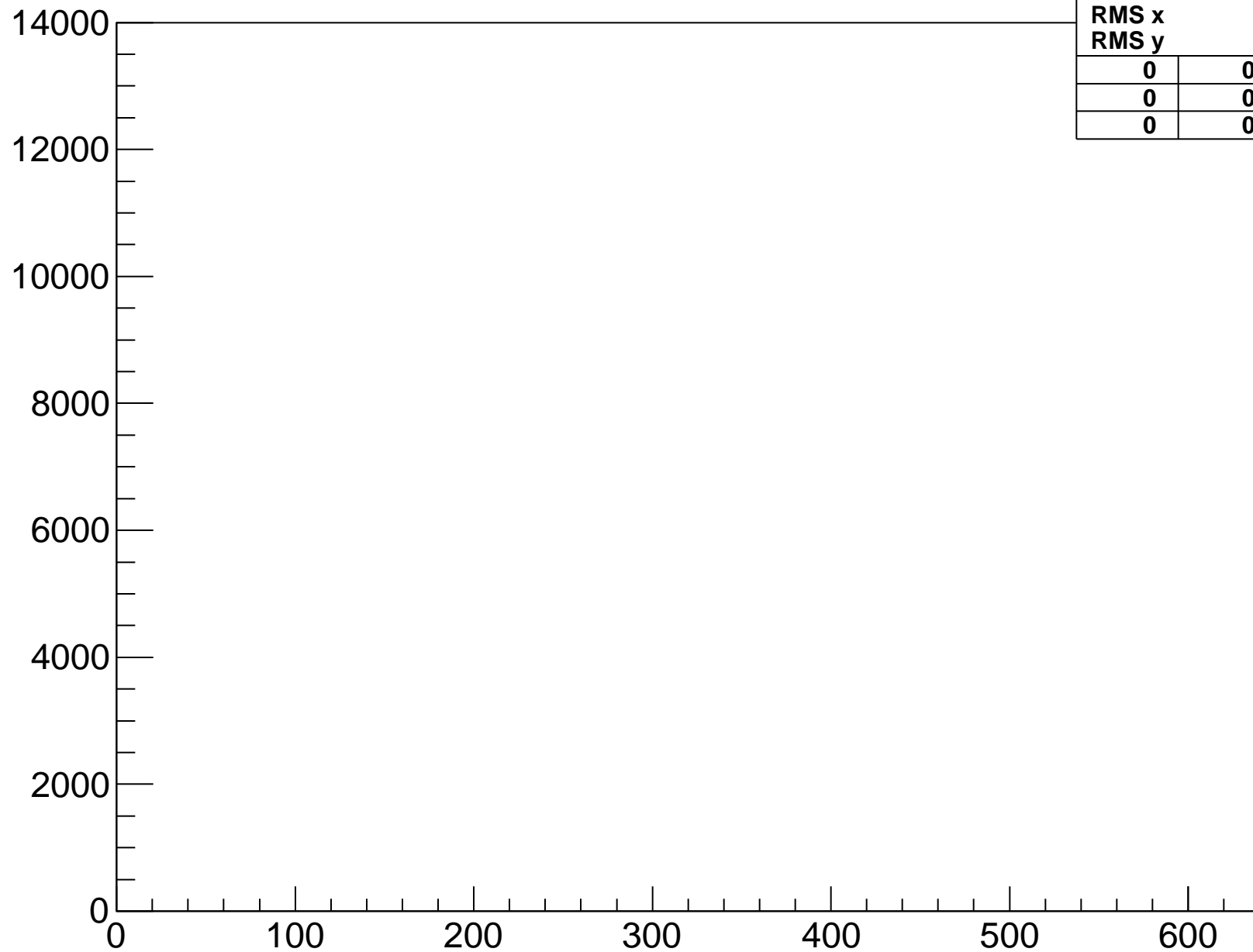
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-9-hyb-3-sample-0



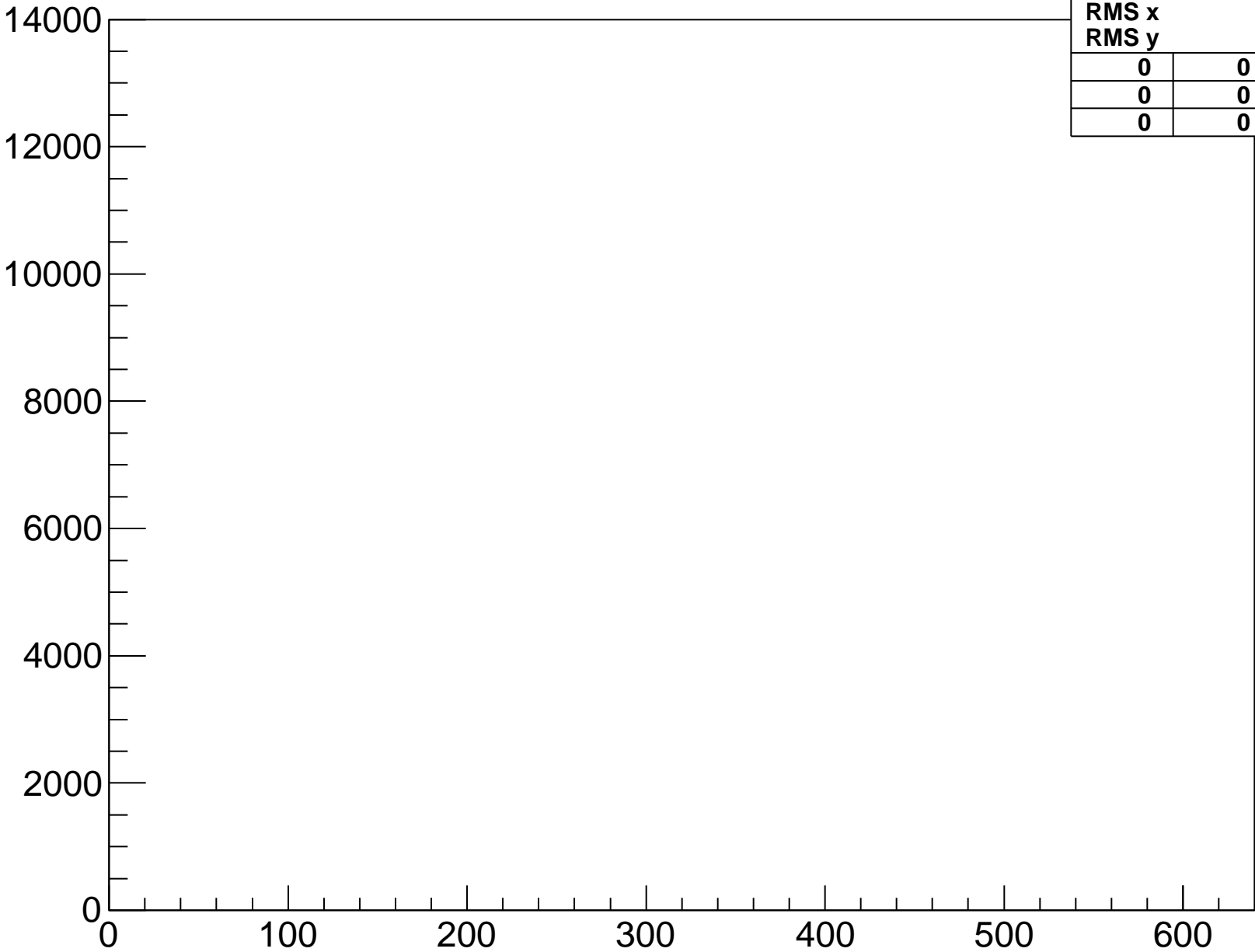
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-9-hyb-3-sample-1



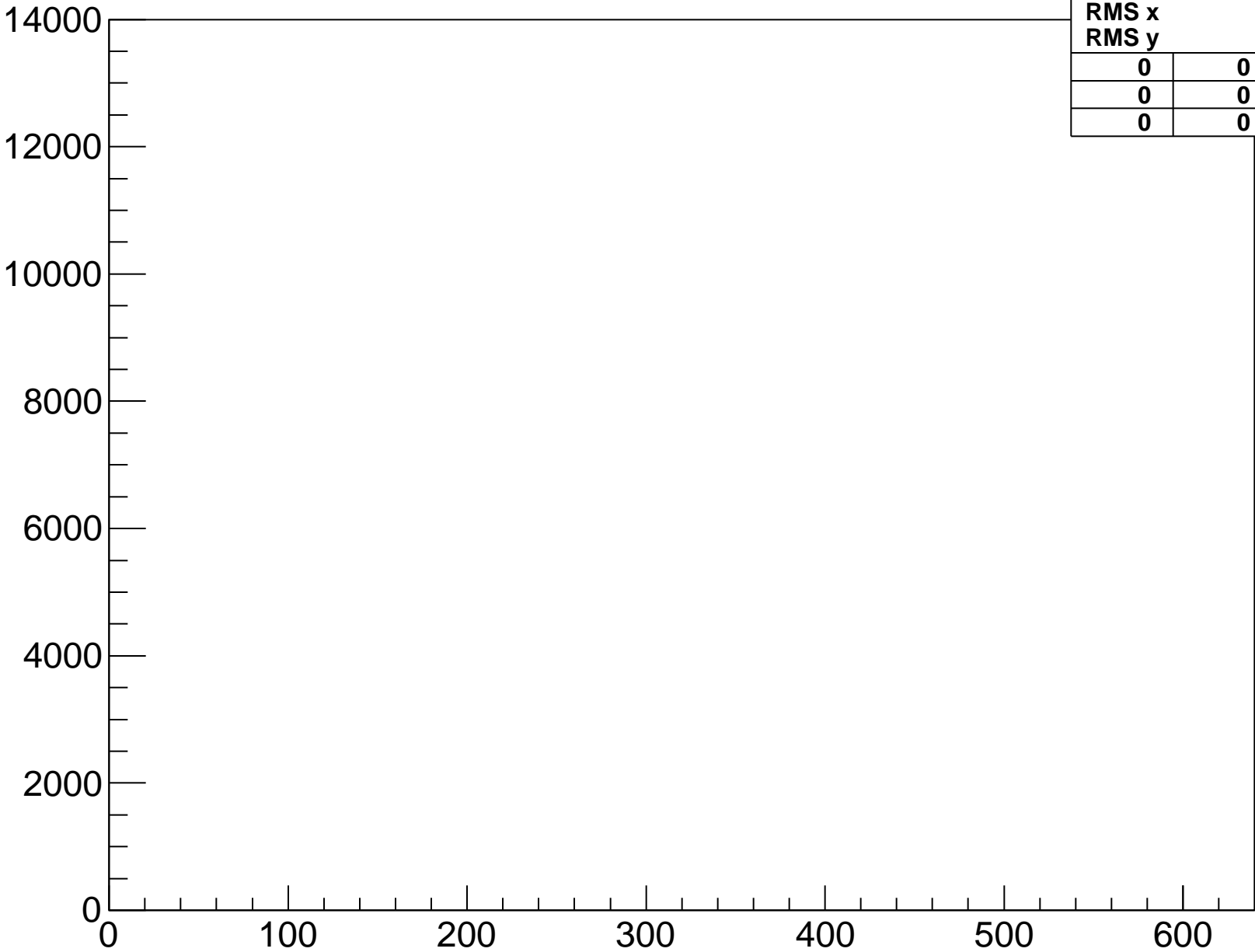
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-9-hyb-3-sample-2



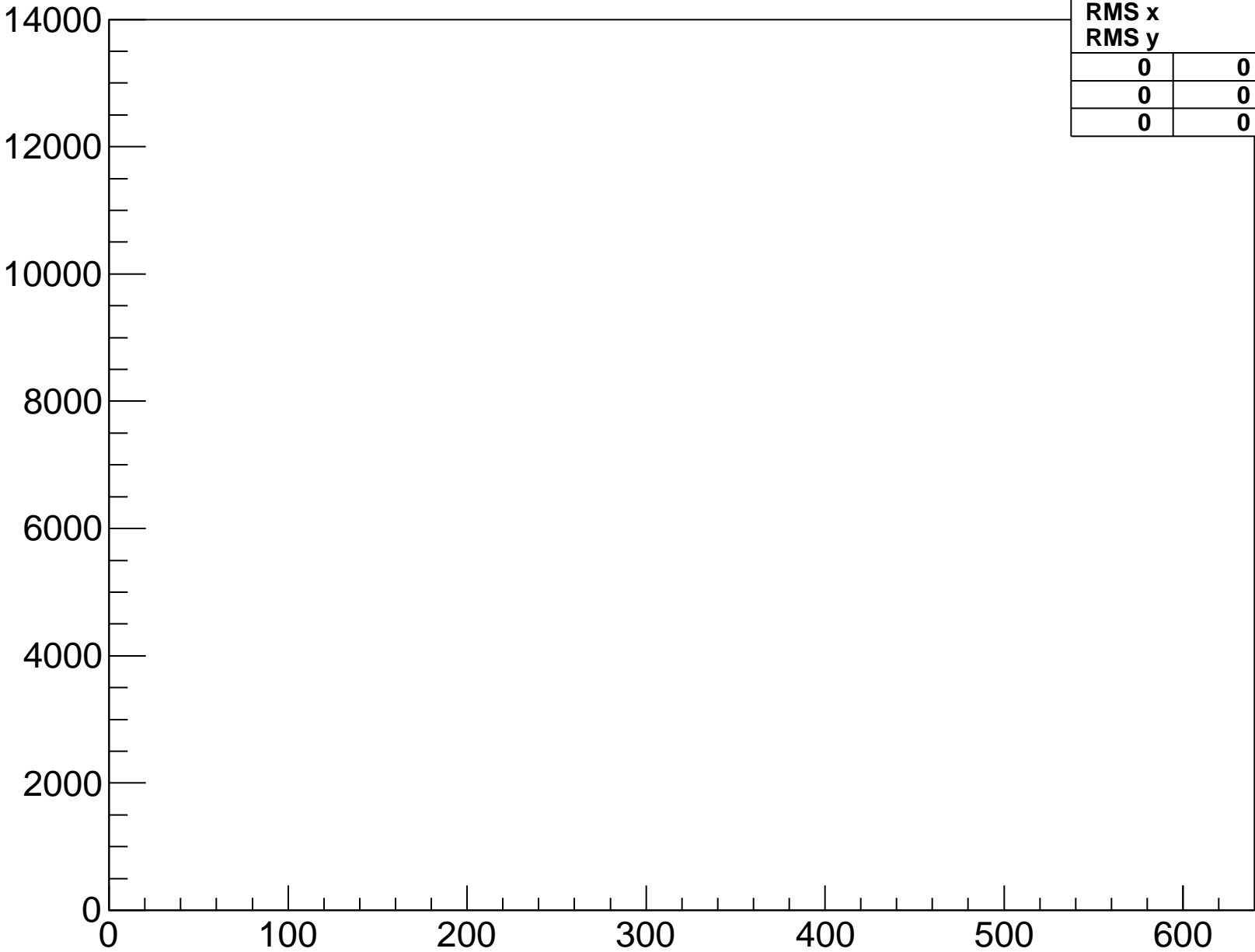
Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0

baselinesamples-fpga-9-hyb-3-sample-3



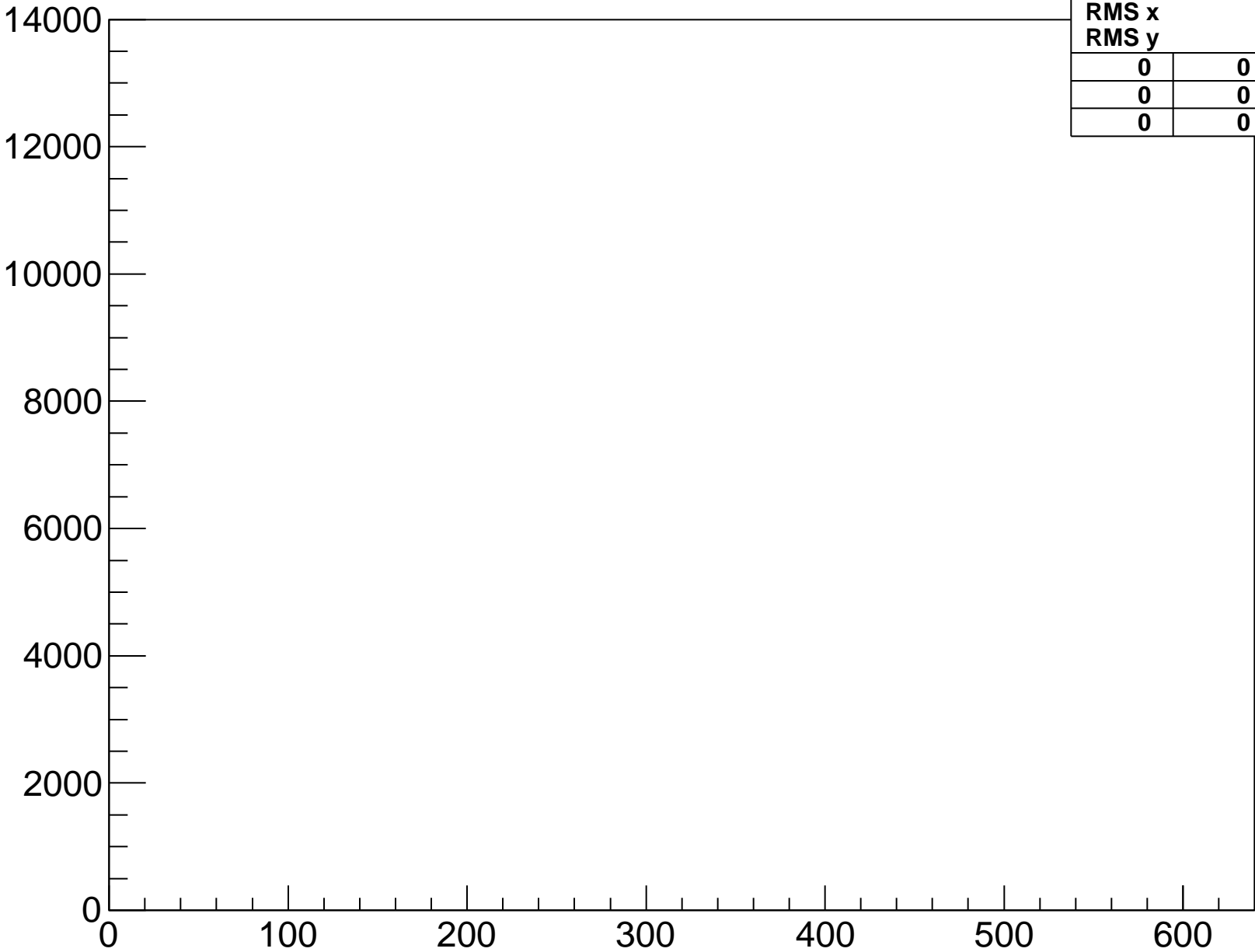
Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-9-hyb-3-sample-4



Entries	0	
Mean x	0	
Mean y	0	
RMS x	0	
RMS y	0	
0	0	0
0	0	0
0	0	0

baselinesamples-fpga-9-hyb-3-sample-5



Entries			0
Mean x			0
Mean y			0
RMS x			0
RMS y			0
0	0	0	0
0	0	0	0
0	0	0	0