Rate of FPGA Single Event Upset from Neutron Exposure

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Abstract

Rates of single event upset (SEU) events in FPGAs in a rich neutron background environment are reported based on data from the Heavy Photon Search (HPS) experiment running at Thomas Jefferson National Accelerator Facility (JLab). The HPS experiment deploys ten Xilinx Artix-7 FPGAs distributed between 10 and 70 cm from a thin fixed-target foil and approximately 15 cm from the CEBAF electron beam in Hall B. The resulting neutron doses during steady state running of the HPS experiment are of the order of X neutrons/cm^2/s. Neutron doses are based on simulations using FLUKA and validated with neutron detectors. In total X number of SEUs was recorded during steady state running and the estimate During the 2016 spring run a total of Y SEUs were detected over an active detection time of approximately X days which corresponds to X Failure In Time per Mb. This paper describes the estimation of the radiation environment and the error detection mechanism and compares them to existing data from other applications.

Keywords: FPGA, Xilinx, Artix-7, single event upset, soft error, SEU

Contents

1. Introduction

Reliability of electronic devices placed in environments with large radiation is of continuous importance to a wide variety of applications in industries such as aerospace and defense and satellite- or accelerator based basic science experiments. With program lifetimes that span over decades and hard requirements on reliability the technology choices are complex and evaluated based on a variety of criteria. For accelerator-based experiments stringent requirements on data corruption rates requires experiments to estimate and evaluate different technologies available for deployment in such environments. Reconfigurable FPGAs are now a cornerstone of the data processing for most accelerator-based experiment with mature products where vendors provide long life-cycle support as well as radiation-tolerant designs. The FPGAs offer advantages of low power, high reliability and almost unlimited number of circuit programming lowering the engineering risks and increasing flexibility compared to custom ASICs. In practice, modern experiments often deploy both custom ASICs and FPGAs as described in this paper.

The effect of radiation in electronics is a rich subject handled in depth in Ref. x-y and depends on a wide vari-

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ety of parameters that includes the exact technology and of course what type of radiation that is being considered. This paper has two main goals: one is the describe the estimation of neutron induced errors in Xilinx FPGAs detected from a real-world particle physics experiment and the other is to provide a comparison data point for other, similar, experiment to normalize their expected rates of errors of this kind. For the latter, we compare our estimation with information available from tests under supervision of Xilinx.

The data we present in this paper comes from the Heavy Photon Search experiment (HPS) which is a fixed-target experiment [**?**] at the the CEBAF accelerator at the Thomas Jefferson National Accelerator Facility (JLab). The HPS experiment deploys Xilinx FPGAs close the high intensity electron beam target and beamline leading to large neutron fluxes. Using the Xilinx soft error detection mechanism we were able to measure SEUs and compute failure probabilities using data-verified neutron flux simulations.

This paper is organized as follows. Section 2 gives a brief introduction of the HPS experiment and the location and usage of the the FPGAs. Secion 3 explains the modeling of the radiation environment and the estimates of the neutron flux used to compute the failure rate probability. The error detection mechanism is described in Sec. 4 and the measured SEUs are detailed turned into a failure rate probability from the results in Sec. 5.

2. The HPS Experiment and its FPGAs

The HPS experiment deploys ten Xilinx Artix-7 FPGAs (actually Art. nr here) to process data from a total of 23,004 channels spread out on 36 silicon microstrip sensors readout by a analog front end ASICs. The FPGAs are also used to configure the ASICs and to monitor and control power. The experiment, in Hall b at JLab, places the sensors only 10 cm behind the thin, 0.25% radiation lengths, Tungsten target foil with the core of the scattered beam as close as 0.5 mm from the sensor edges. The target is illuminated by the CEBAF nearly continuous electron beam with currents ranging from 50-300 nA. The proximity to the beam and practical considerations has the sensors placed inside an existing magnet with a vacuum chamber part of the accelerator beam vacuum. To minimize cable lengths and avoid excessive vacuum penetration counts the first stage data processing after the analog front end ASIC are ten so-called Front End Boards (FEBs). These share the load of digitizing and packaging data from the 36 sensors before sending it out on high-speed optical links to the DAQ platform 30 m away. The FEBs also have to configure the ASICs in addition to control power and monitor the state of the sensor electronics inside the vacuum chamber. The only realistic choice for the FEBs was to use an FPGA to handle the wide set of tasks.

Continue here...the below are placeholders with too much information. Not sure we need any of this except for a description of how resources are used in the FGPA?

2.1. Front End Board

The FEB serves two purposes: distribute power to the hybrids and digitize analog readout data from each hybrid APV25. Its design and placement inside the SVT vacuum chamber is motivated by a desire to reduce vacuum penetration count and analog signal length. The design centers around a Xilinx Artix-7 FPGA to interface to the ADCs, transmit digitized data up-stream, distribute clock, trigger, and I^2C communication to the hybrids, and control and monitor hybrid power distribution. Deployment of FEBs inside the SVT chamber presents a number of challenges. Due to the presence of a 2 T magnetic field, great care was taken with the design of all onboard power regulators. Ferrite core inductors commonly used with DC-DC switching regulators will saturate in such high fields and lose effectiveness. It was also desired that no magnetically conduct-ing material be used on the board, so as not to distort the magnetic field inside the chamber. This necessitated the use air-core inductors in power regulation circuits and throughout the board. Radiation is also a concern inside of the SVT chamber. Beam interactions with the Tungsten target produce both neutrons and x-rays, which can have adverse effects on the FEBs. Neutrons can cause Single Event Upsets (SEUs) in the digital circuits of the FPGA, and x-ray doses can degrade integrated circuits over time. Simulations indicated that these sources should be within acceptable limits, but additional measures were taken just in case. A Borated-Polyethylene shield was installed around the FEBs to block neutrons, and the boards are installed on a serviceable custom cooling plate so that they can be replaced if needed. Each FEB connects to 4 hybrids, for a total of 20 APV25 analog channels. A preamplifier circuit converts the 4 mA signal from each APV25 into a voltage scaled to the range of the AD9252 14-bit ADC. The ADC sample clock runs at the same frequency as the APV25 clock, but has a programmable phase offset so that each sample can be taken at the center-point be-tween analog transitions. The FPGA monitors each APV25 ADC stream looking for readout frames. Every readout frame is then sent upstream by a multi-gigabit

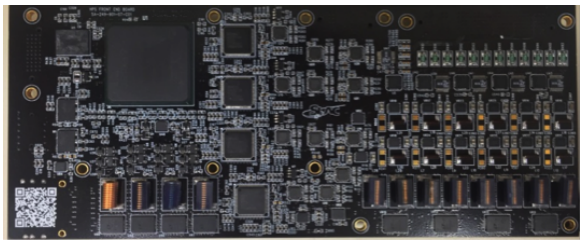

Figure 1: One COB ATCA blade used in the RCE platform.

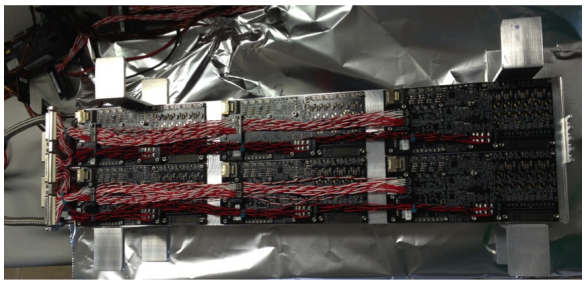

Figure 2: The partially cabled data acquisition front end boards screwed to the aluminum support plate before installation .

transceiver (MGT). The FEB has four upstream-only MGTs, with one dedicated to each hybrid. By dropping the two least significant noise bits from each ADC sample, each hybrids readout data can be packed on to a 3.125 Gbps link at rates approaching 50 kHz. Performing APV25 frame recovery on the FPGA in this manner allows the link speed to scale with the trigger rate, as well as robust error recovery on the upstream end. At the maximum trigger rate of 48.7 kHz, the combined data output rate from all of the FEBs is 89.6 Gbps. An additional full duplex MGT provides for configuration, trigger, and clock to be received from the upstream system. This link operates in a special fixed-latency mode so that every FEB in the system can recover the same 125 MHz beam-synchronous clock with minimal skew. The recovered clock is divided on each FEB to create the 41.667 MHz APV25 and ADC clocks. Triggers and clock alignment commands can be sent down these links with a guaranteed latency, assuring that all APV25s in the system receive the same clock and triggers in lockstep with each other. The FEB is also responsible for distributing and monitoring hybrid power. Switched-mode regulators are used to efficiently step down a 6V reference to three intermediate voltages 2.9V, 2.9V and 1.4V. Linear regulators then convert these voltages into the 2.5V (DVDD), 2.5V (AVDD) and 1.25V needed by each hybrid. AD5144 SPI digital potentiometers placed in the resistor feedback of each regulator allow for all of the regulated voltages to be trimmed by the FPGA to account for cable drops. LTC2991 I^2C ADCs are deployed to monitor the output voltage, feedback voltage and output current on each of the twelve hybrid voltage outputs. All of these monitors are accessible on the control link, and are sampled every second for delivery to EPICS slow controls.

3. Radiation Environment

3.1. Overview

3.2. Simulation

3.3. Normalization using Neutron Detectors

4. Single Event Upset Detection and Monitoring

Description of how, what and when we detect.

5. Results

Normalization of the neutron.
The probability of a SEU, p, in HPS is given by,

$$p = \frac{N}{\Phi} \times Q_{tot} \tag{1}$$

where N is the observed number of SEUs, Φ is the neutron flux per cm^2 per Coulomb of charge at the FPGAs and Q_{tot} is the total integrated charge while the error detector was enabled during stable running.

- Pelle finds N and Q_{tot}.
- Takashi finds Φ
- Ben finds out how the error probabilities are defined in industry e.g. FIT/Mb and the like and then we'll figure out how we compute it.

6. Conclusion

7. Acknowledgements

Thanks you.